

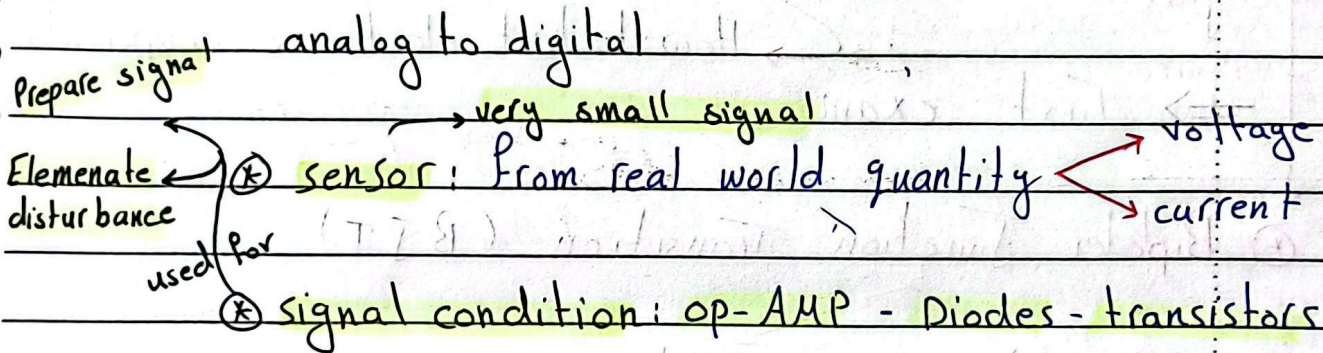
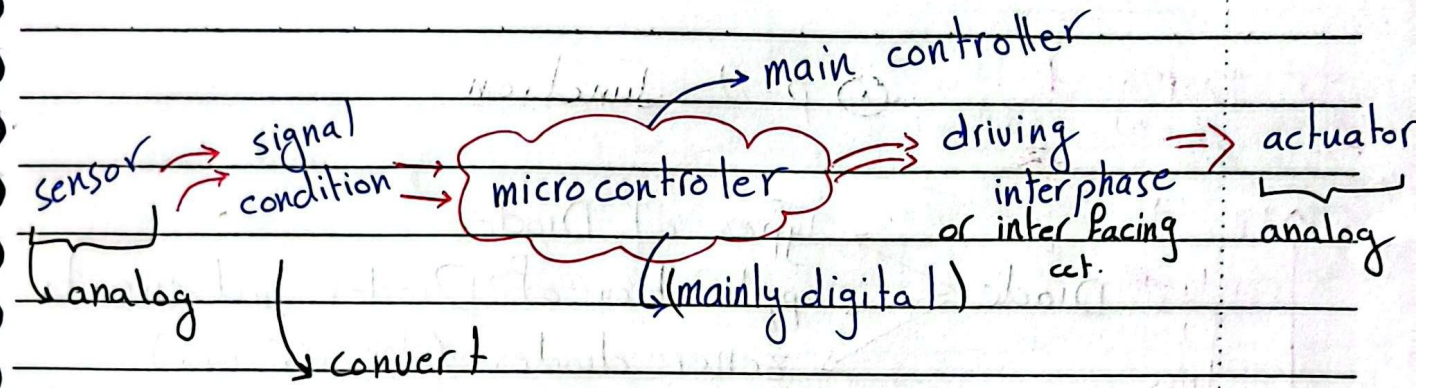


# الكترونيات للميكاترونكس

د. محمد القادري

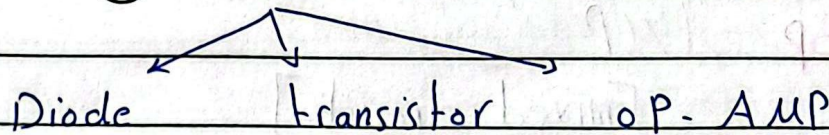
للطالب المبدع  
كريم عبدالهادي

إرادة - ثقة - تغيير



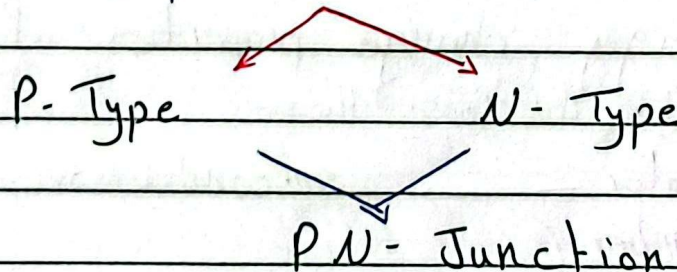
⊗ Driving inter phase circuit: convert digital to analog

⊗ P-N Junction:-



⊗ semiconductor material:-

⊗ pure semiconductor:-





## \* p-N- Junction

Diode → Types of Diodes  
→ application of Diodes and circuits  
→ zener diodes (الدايودات المتغيرة)  
→ How to test electronic components

⇒ First exam

## \* Bipolar Junction Transition (BJT)

MosFet → JFet

⇒ second exam

## \* op- AMP

[mixed circuit]

↳ Diodes, transistor world, op- AMP, passive components.

\* High energy - change properties of material and make it loose them

insulator → semiconductor

↳ after losing properties



⊛ we are interested in electronics to design either signal conditioning circuits or driving interfacing circuits, both of them are needed to communicate with microcontroller unit.

✓ ⊛ Types of material based on electrical conductivity:-

- |                 |                                   |              |
|-----------------|-----------------------------------|--------------|
| ① conductor     | } depend on movement of electrons | } mainly (I) |
| ② semiconductor |                                   |              |
| ③ insulator     |                                   |              |

⊛ we classify these three material by based number of electrons in (last shell) → Free electrons

⊛ we know that there is 3 Type cct. is

- | ① First       | ② Second                              | ③ Third                                           |
|---------------|---------------------------------------|---------------------------------------------------|
| 1- Diode      | 1- driving interphase                 | interference                                      |
| 2- Transistor | ↓ cct.                                | [octocoupler]                                     |
| 3- amplifier  | 2- change nature of signal from D → A | ⇒ $\hat{V} \hat{I}$ electro magnetic field $\sim$ |
|               | 3- increase power of signal           |                                                   |

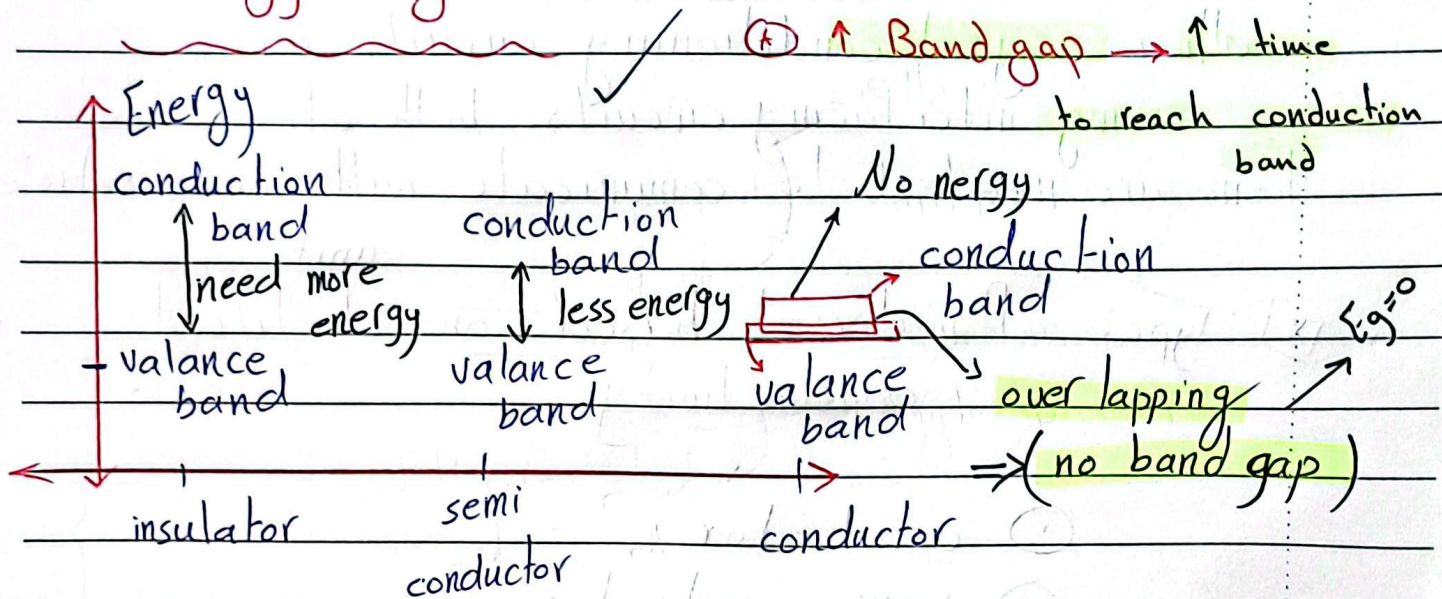


To break a covalent bond  $\rightarrow$  valance electron gain minimum energy  $\rightarrow$  Band gap  $E_g = E_c - E_v$

$E_v$ : maximum energy for valance band  
 $E_c$ : minimum energy for valance band

No.

## \* Energy diagram:-



\* valance band: most outer shell (الطارة الأخرى)

\* conduction band: amount of energy that electron need to move freely.

there is no electron  $\rightarrow$  \* Band cap: A. amount of energy for electron to be in conduction from valance

B. Difference in energy between valance and conduction

\* in conductor: we don't need any energy to move electron.

\*  $\uparrow$  temprature  $\rightarrow$   $\uparrow$  covalent bond broken  $\rightarrow$   $\uparrow$  electron free movement and  $\uparrow$  holes

\* maximum number of electron in shell can be controlled by equation  $2n^2$  where  $n$  is shell number

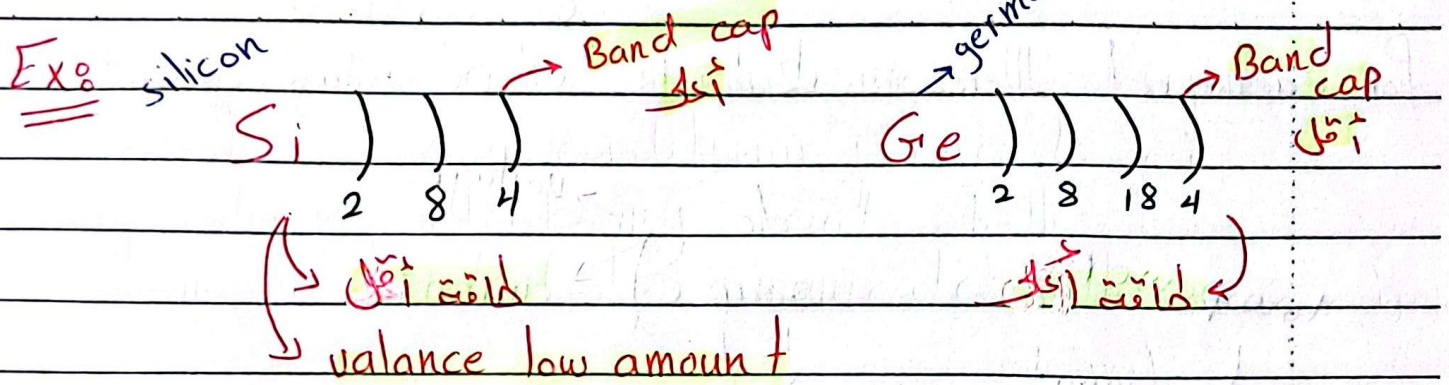


dopping: adding atoms from another group

Subject

Date

No.



1. all above because: 1. there is more attractive force with atom in (Si)

2. electrons in last shell closer to the atom

[\*] all materials are (conductor) ← but practically: if the material be large it will change the structure

[\*] conductor: valence electron in valence shell ( $E_g = 0$ ) can break free and reach conduction band  $\uparrow$  conductivity contain very large electron in conduction band (very low resistivity)

[\*] semiconductor: adding impurity  $\rightarrow \uparrow$  conduction (group 4 material) ( $E_g$  around 1) (can be changed by dopping)

[\*] insulator: valence shell is satisfied, (no  $e^-$  in conduction band) no valence electrons can be shared ( $E_g$  (3-6)) (all electrons in valence band) (very high resistivity) (very low conductivity)

[\*]  $\uparrow$  shell radius  $\rightarrow \uparrow$  electron energy

$\uparrow$  shell number  $\rightarrow \uparrow$  electrons from nucleus  $\rightarrow \downarrow$  attractive force

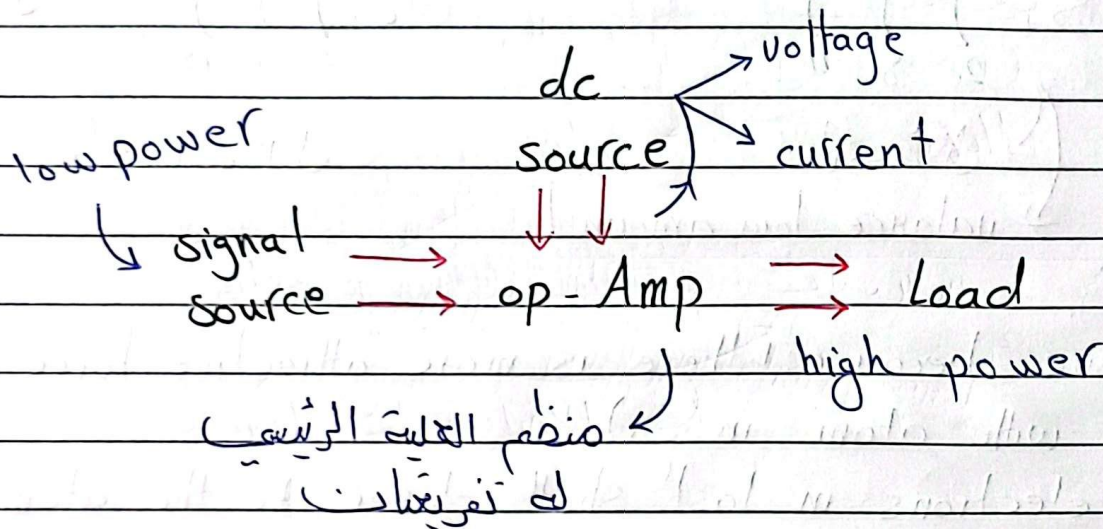
$\rightarrow \downarrow$  Band gap  $\rightarrow \uparrow$  free electron

$\rightarrow \uparrow$  electron energy



② amplified

For each cct. there is 2 inputs: ① DC voltage, current



① مصدر ذو ديار

② تنظيم الطاقة إلى طاقة أعلى

input of electronic cct.



⊛ we have two types of signals

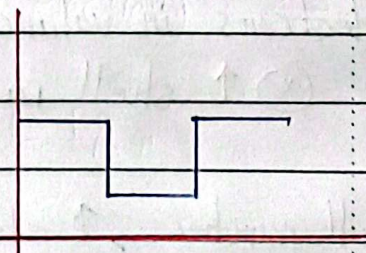
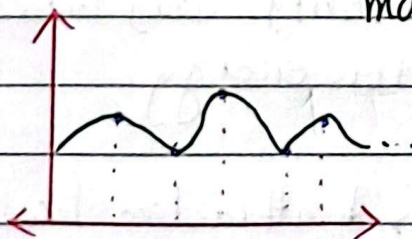
analog signal

discreat signal

There is a value in each signal

constant values just (0,1)

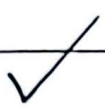
this is the main factor to classify analog signals;





⊗ in this course :-  
we deal with DC values (capital)  
 $I_B$   $V_{BE}$

⊗ First component we need to know



Diode

- ① non linear element → (i-v) non linear
- ② basic electronic device
- ③ two terminals

positive term <sup>(+)</sup>  (-) negative term  
anode cathode

⊗ properties of semiconductor materials:

① it will be mainly (Si and Ge)

(crystal structure) ← pure semiconductor material (intrinsic) (insulator)

② semiconductor lies between conductor and insulator.

③ in outer most shell there is just 4 electrons



concentration of electrons =  $\frac{\text{number of electrons}}{\text{volume (cm}^3\text{)}}$  (\*) تنوية: احنا نفرض

concentration of holes:  $\frac{\text{number of holes}}{\text{cm}^3}$  النزلة ← نواة

يوثرونات ← متعادلين الشحنة د پروتونات

بالإضافة إك إليكترونات

توزع في أغلفة 4 مسافات مختلفة

تزداد الطاقة بزيادة نصف قطر الغلاف

shared between atoms to form covalent bond  
valence electron (\*) اليكترون الموجود في المدار الأخير  
interact to form crystal outermost shell (valance shell)

impurities ← معلومة 1 - السبب الرئيسي لإضافة  
increase Free electron 2

(Free electrons) ← تتغير اعتمادا على (Temperature)

$\uparrow T \longleftrightarrow \uparrow \text{Free electron}$



The net flow in the conduction band generate current.

(\*) at  $T = 0K$  → electron is in lowest possible energy

→ and silicon is insulator  
no free electrons ↪

(\*) Different Types of energy affect on crystal structure

(\*) main factor that make semiconductor → conduct Temperature

(\*)  $\uparrow T$  →  $\uparrow$  thermal energy on valence electron

→ break covalent bond → move from original position

Free electrons في الحرة الإلكترونات (\*)

(\*) Types of energy that move free electron

(1) thermal energy

(2) electrical energy

(3) Kinetic energy

(4) mechanical energy

Kinetic

potential

☑ To break covalent bond the valence electron must gain minimum energy.



Breaking of covalent band for  $(T > K)$  creat  $\rightarrow$  2-Holes

(\*) Extrinsic semiconductor

(Doped semiconductor)

(impure atom)

n-Type semi. - pure semiconductor + material (impurity)

pentavalent

Trivalent

increase of conductivity

group 5 atom

5 bonds

increase of conductivity

intrinsic semiconductor + impurities

Si  $\xrightarrow{\text{high } T}$  change crystal structure

No thermal energy

$\uparrow$  Free electron  $\rightarrow \uparrow T \rightarrow$  donor impurity or doping

$\uparrow$  atom

Types of Base current:-

# Types of electrons:- I] current due a Free electron

II] recombination between hole and

p-Type of semiconductor.

$3e^- + 4e^- = 7e^-$  electron

# Boron (acceptor impurity) contain  $3e^-$  in valance shell

connect with the  $4e^-$  Si and the hole space is filled with electron From another Si electron

forming (hole current)

This activity called: doping: adding of impurity

Penta

try

impurity also es semi in  $N^0$   $T^0$   $E^0$   $B^0$   $K^0$



↑ Free electrons → ↑ conductivity → ↑ holes.

[\*] we know that (any pure semiconductor) is (intrinsic)  
→ Base of current is (Free electron)

⇒ concentration of Free electron isn't enough to connect current to any device

so we need to increase Free electron

by doping → {pentavalent material  
→ {trivalent material

[\*] each band Si connect with 4 similar atoms  
because in outer most shell there is 4 electron

نفس (Ge) في الطبقة الخارجة الـ 4 إلكترونات

(Si) في الطبقة، في (Ge) في الطبقة،

because:-

(1) attraction force between nucleus and valance shell

(2) ↑ shell → ↑ energy

so it doesn't need a lot of energy to escape



→ in pure semiconductor  
 [\*] The reason of holes:-  
 because of thermal energy

[\*] hole → attract new electron

hole في ← → الإلكترونات في

[\*] The number of free electron in semiconductor isn't enough so we need to increase thermal energy

→ but we can't increase  $T$  as much as we need because it change properties of material.

→ So we go to doping

(\*) penta valent :- material characterize as the number of electron in the outermost shell (valance shell)

(\*) Drift current :- movement caused by electric field  
 → Direction always in direction of electric field

(\*) Diffusion current :- movement caused by variation carriers concentration, Direction Depend on slope  
 (High → lower) concentration

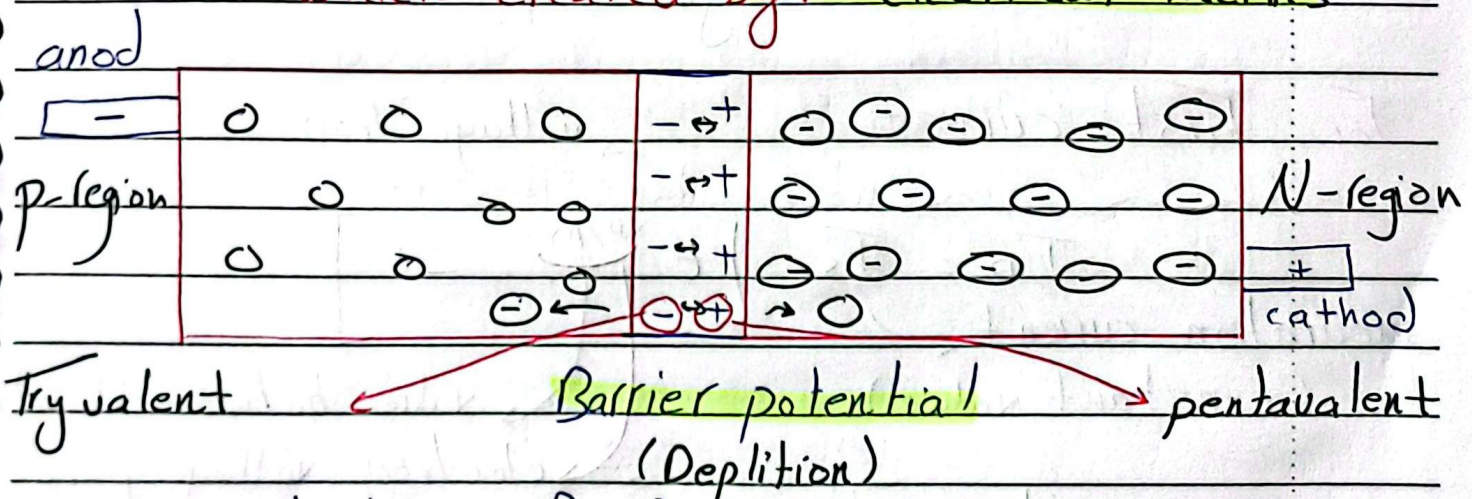


[\*] N-Type material: (trivalent)

5 electrons  
 4 electrons make covalent bond  
 1 electron it's free electron

[x] This Type of material semiconductor is formed by add a class of material called (pentavalent) which characterize as atom with 5 electron in outer most shell (valance shell)

→ This Type of add is called doping process which created by:- electrical thermis



⊗ concentration of Free electron > holes  
 majority carrier in N-region: Free electron  
 majority carrier in p-region: holes



vbi change From one semiconductor to another or by changing amount of impurities

For Ge 0-3  
 $T$ , Type of material, impurities number (n-p) Type / permittivity

(\*) Barrier potential:-

(\*) Break down point:- point where large reverse bias current and max reverse bias voltage

(\*) Ideal current:-

$I_V$  characteristic For different model of diode

we have 3 models:

(practical)

1. (exponential, experimental, realistic)  
 → approximation of real world

2. Ideal model

3. constant voltage drop model

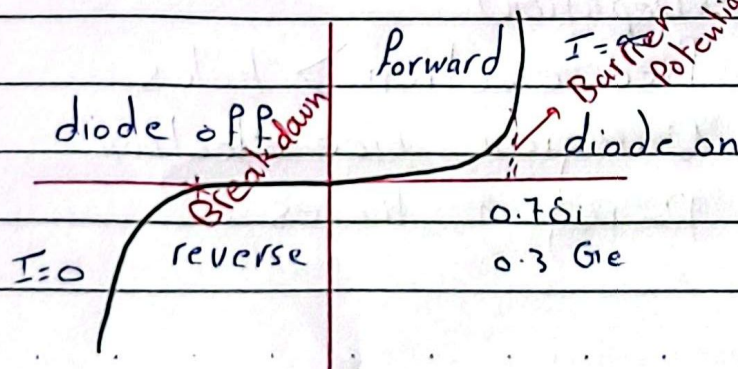
For First curve:

voltage drop

$$I_D = I_S \left[ e^{V_D / nV_T} - 1 \right]$$

saturation current  
 (constant value)

value between (1~2)  
 electron voltage pure





(\*) second curve:-

if

$$V_D > 0$$

diode is on (closed switch) Forward

if

$$V_D < 0$$

diode is off (open switch) reverse

(\*) third curve:-

constant voltage drop

$V$

0.7 Si  
0.3 Ge

if

$$V_D > \begin{matrix} 0.3 \text{ Ge} \\ 0.7 \text{ Si} \end{matrix}$$

diode is on

$$V_D < \begin{matrix} 0.3 \\ 0.7 \end{matrix}$$

diode is off

(\*) in Forward biasing if we switch the polarities

it will be reverse biasing

↑ Barrier potential

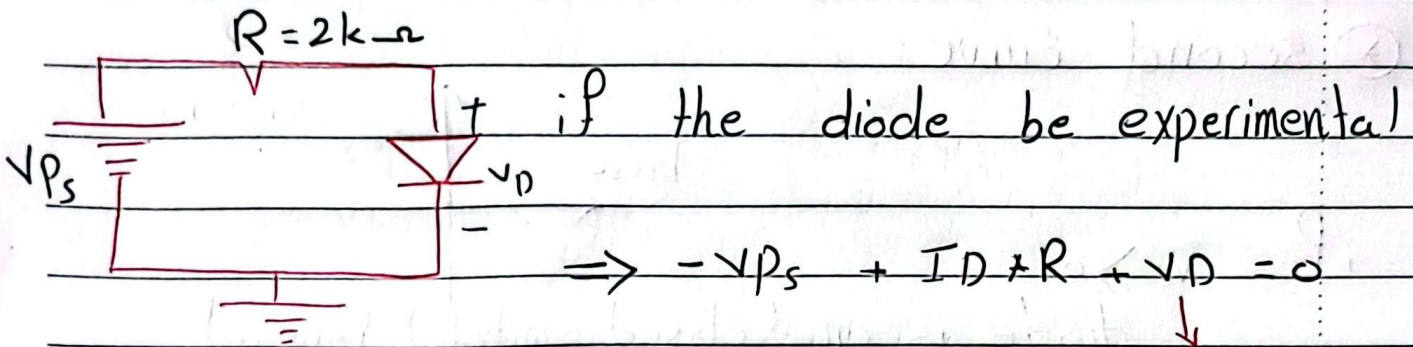
Free electrons

(\*) إذا اختلفت قطبتي ملامات عن نوع (diode) يكون

(1) constant voltage drop

(2) Si





↑ Free electron → ↑ electron energy. voltage drop

$$-5 + I_D \cdot 2k + V_D = 0$$

$$-5 + I_S \left[ e^{\frac{V_D}{nV_T}} - 1 \right] \cdot 2k + V_D = 0$$

There are two ways to solve the above equations either by trial and error or graphical.

Sol<sup>n</sup> H.w Find  $V_D$  and  $I_D$  by trial and error method??

if  $V_D = 0.6$

↙  
 $I_D = -2.3$

if  $V_D = 0.65$

↙  
 $I_D = 10.1$

if  $V_D = 0.619$

↙  
 $I_D = 0.01$



① clipper circuits (limiter ckt.)



④ إذا ما أتينا إلى ذال نوع (diode) constant voltage (Si) }  
Forward biasing. ←

① assume the diode in open switch  $I=0$   
(reverse biasing)

② Take KVL

③ Find the condition that make diode on and off for finding the out put voltage in both cases

if the ckt. in open switch  $I = 0$



$$-V_n + I R_1 + V_D + V_{BIAS} = 0 \quad \text{--- (1)}$$

(\*) when diode on  $V_D > V_B(0.7)$



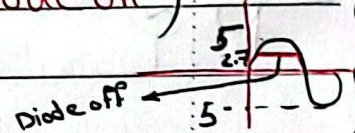
\* From equation 1

$$V_D = V_{in} - V_{BIAS} \geq 0.7$$

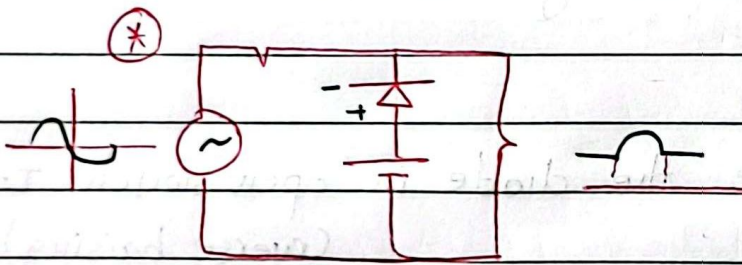
Diode on  $\leftarrow \boxed{V_{in} \geq 0.7 + V_{BIAS}}$

$\rightarrow$  if the condition is satisfied (Diode on)

$$V_{out} = V_{BIAS} + 0.7$$



if the condition doesn't satisfy (Diode off)



$$-V_{in} + IR - V_D + V_{BIAS} = 0$$

$$V_D = V_{BIAS} - V_{in}$$

when  $V_D \geq 0.7$  diode is on

$$V_{out} = V_{BIAS} - 0.7$$

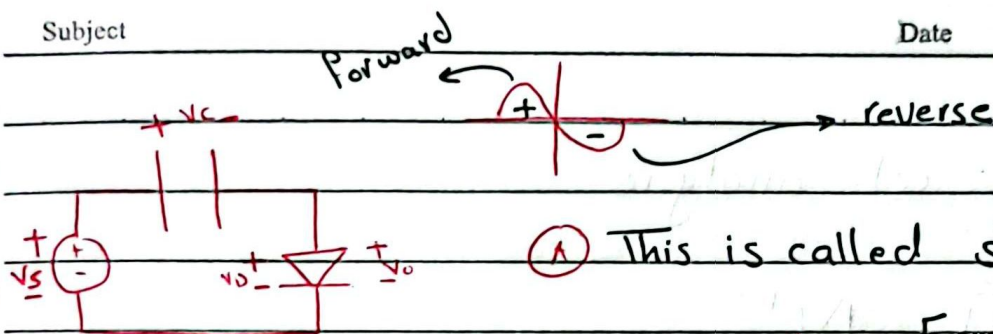
when  $V_D < 0.7$  diode is off

$$V_B - V_{in} \geq 0.7$$

$$-V_{in} \geq 0.7 - V_B$$

$\boxed{V_{in} \leq 0.7 + V_B} \rightarrow$  Diode on





(A) This is called shifter ckt.

$$V_s(t) = V_m \sin \omega t$$

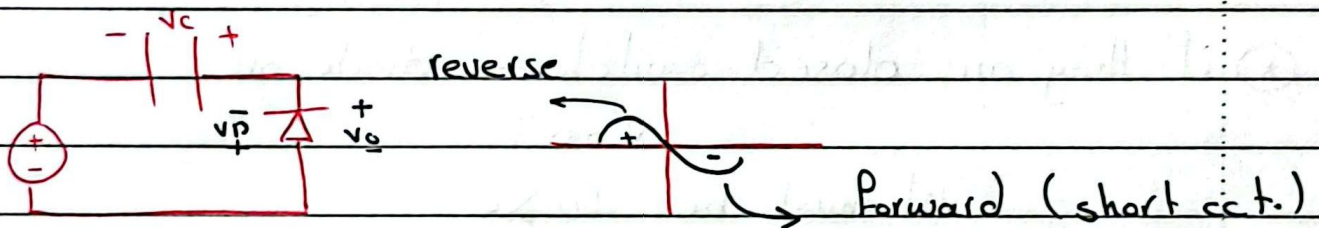
$$V_c(0) = 0V$$

$$V_{on} = 0.7V \rightarrow V_x \text{ (constant voltage drop)}$$

$V_o$   $\rightarrow$  Forward biasing  
 $\rightarrow$  reverse biasing

$$-V_s + V_c + V_{out} = \text{zero}$$

$$V_{out} = V_s - V_c$$



$$-V_s - V_c + V_{out} = 0$$

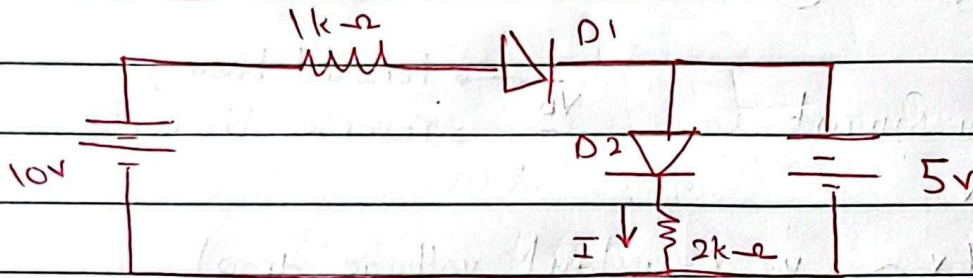
$$V_{out} = V_s + V_c$$

$\rightarrow$  max 9.3 if Ideal min 0  
 min -0.3 max 1

[X]  $V_{out}$  (+) because in 2 cases it is reference



## \* multi diode ckt. analysis:



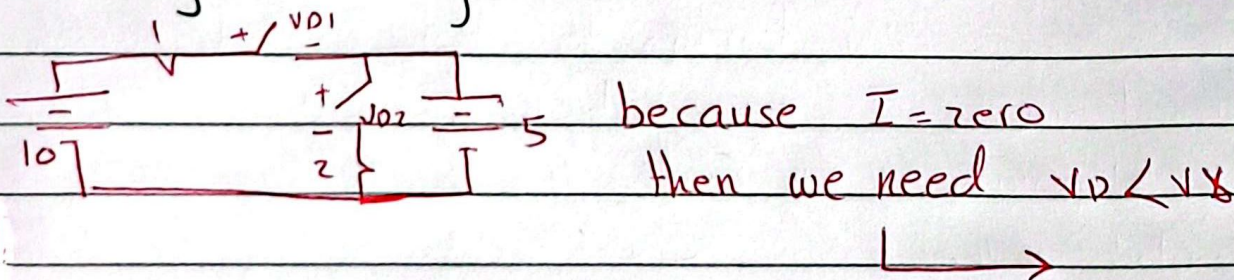
\* There is equation for  $D_1$  } two equations  
 there is equation for  $D_2$  } non linear

\* if they are closed switch  $\rightarrow$  diode on  
 $V = 0.7$   
 it must be  $I_D > 0$

\* if diode off  $V_D \rightarrow \begin{cases} 0 \\ 0.3 \\ 0.7 \end{cases}$

| $D_1$ | $D_2$                                       |
|-------|---------------------------------------------|
| off   | on                                          |
| off   | off $\rightarrow$ 2 unknowns (few unknowns) |
| on    | on                                          |
| on    | off                                         |

\* by checking ( $D_1$  and  $D_2$ ) off





$$-10 + I_D \times 1k + V_{D1} + 5 = 0$$

$$\boxed{V_D = 5} \rightarrow V_D > 0.7 \text{ X}$$

(OFF, OFF) X

نو تا  
عن  
concept  
نفس الی

switch (1) For  $D_1$  must be on

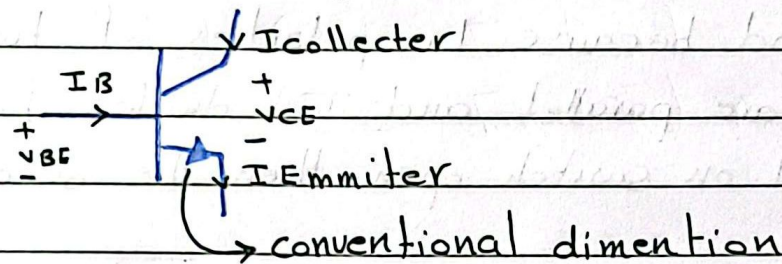
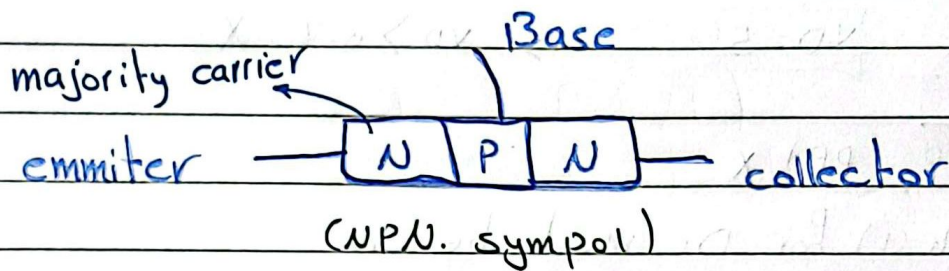
and because two polarities of two batteries are parallel and two diodes forward and on switch open then the second switch is on.

☒ Week 4 on doctors slides

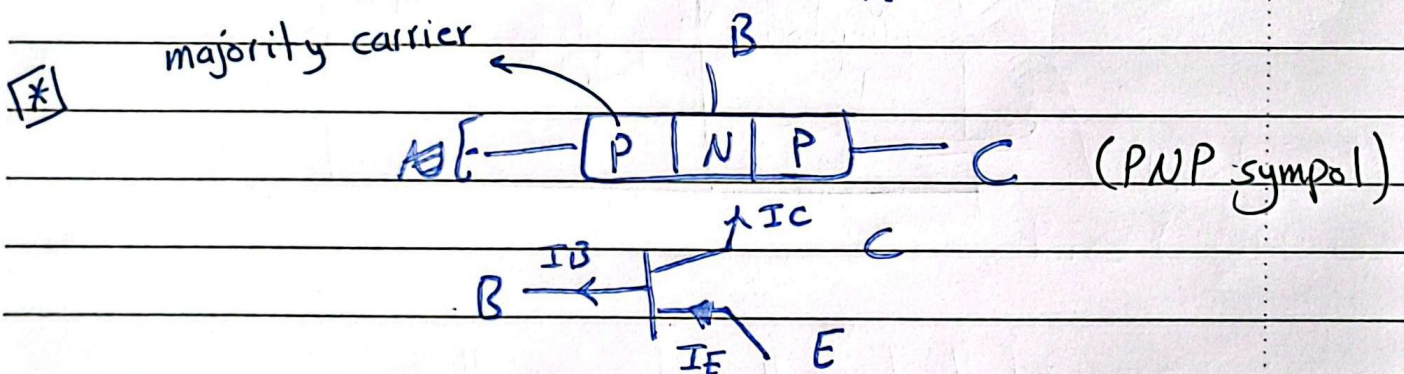


1. (3 separate doped junction)

[X] (BJT), we have 2. 3 terminals device 3. 2 PN Junction



[X] اتجاه حركة الإلكترونات دائماً من السالب إلى الموجب



[X] The current in NPN = out of E ( $I_E$ )

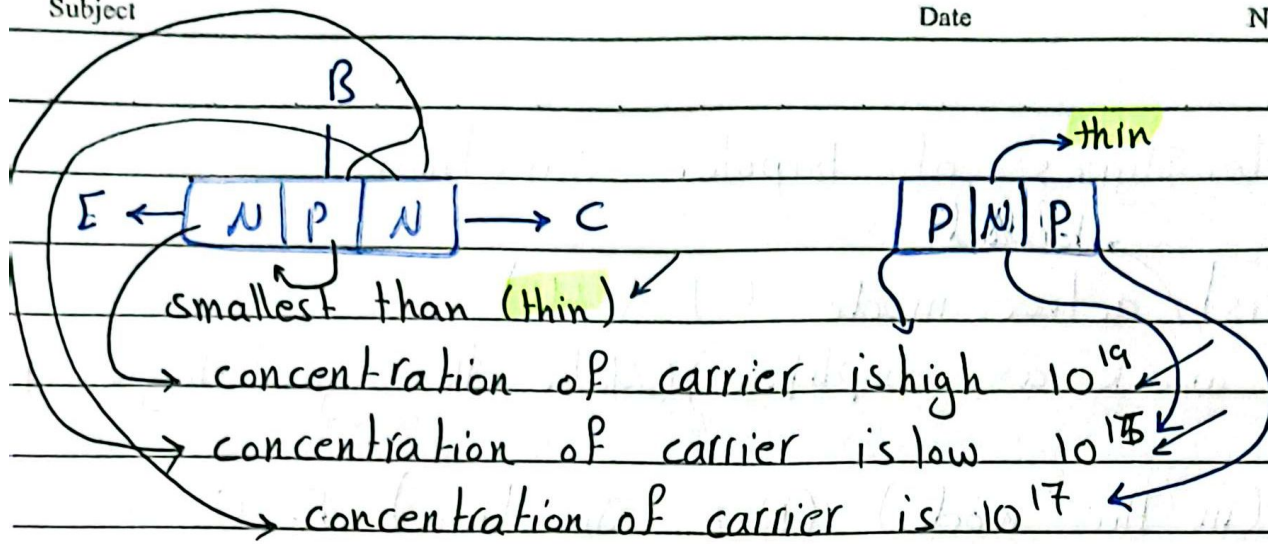
[X] The current in PNP = out of C ( $I_C$ )

[X] we have 4 mode of operation:-

| BE  | BC   | mode                          |
|-----|------|-------------------------------|
| F.W | F.W  | saturation $V_{CE} \leq 0.2$  |
| F.W | R.V. | active $V_{CE} > 0.2$         |
| R.V | R.V  | cut off $I_C = I_E = I_B = 0$ |
| R.V | F.V  | Reverse                       |

Basic transistor principles-  
voltage between 2 terminals and current through third terminal.





[\*] In NPN the concentration of  $e^-$  will decrease? because of recombination with holes in (P-Junction)

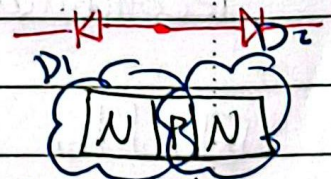
[\*] In PNP the concentration of holes will decrease? because recombination of holes with electrons (N-Junction)

[\*] In the base, it is :- (1) thin (2) has low doping level } why??

to minimize number of carrier lost by recombination in Base region

[\*] in (BJT) we have two diodes

↳ we say that they are diodes back to back but they didn't work as diodes



(Forward, reverse)

[\*] in (P-N) we have two mode diode operation then in (BJT) we have four mode levels.

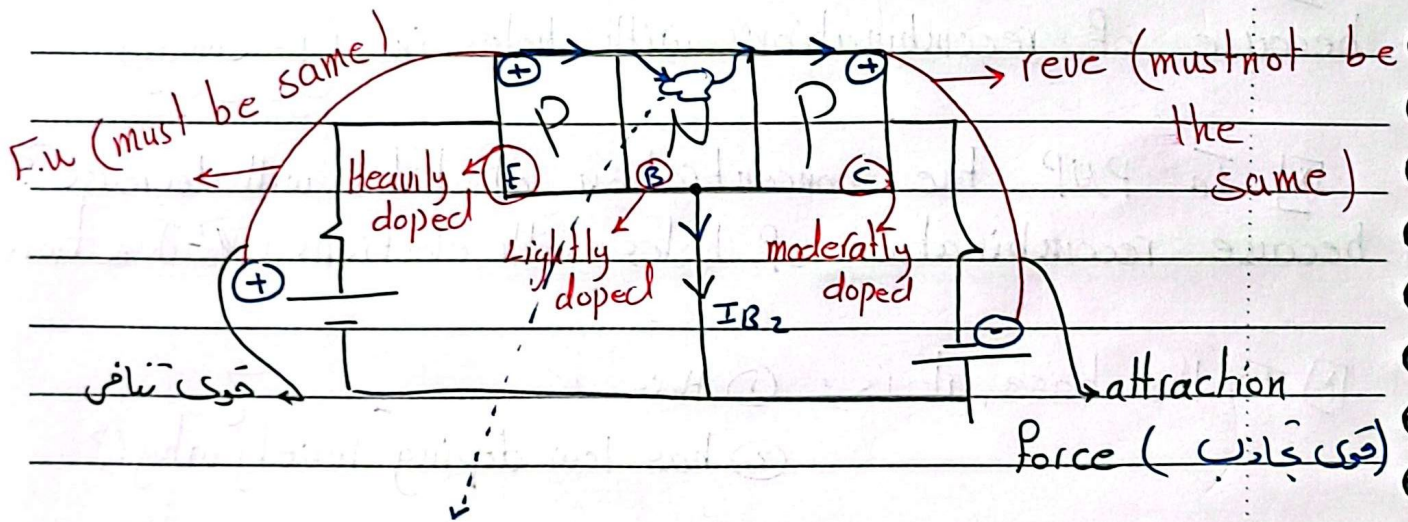


## \* mode Types of Bipolar Junction:-

Forward  
 [1] First active mode (F.A.M.)

very important (it is work as amplifier) (Make AC signal higher)

\* (in this mode) (B-E Junction) F.W  
 ( $I_B, I_C, I_E \geq 0$ ) (B-C Junction) reverse



There is a small amount will be lost because?  
 recombination between holes and electrons

\* after this purpose it will creat (current)



\* In (F. A. M.)

E F. W. biase C r. v. base

collector will collect the majority carrier from base due to E-Field on collector.

very small component will be lost in base by recombination

→ it will continue like this until current flow conventionally out of E in NPN and In E for PNP

\* Cutt of mode:

E reverse

C reverse

BJT will behave open switch

I<sub>c</sub> = 0, V<sub>CE</sub> = V<sub>CC</sub>

\* Inverse:

E rev

C F. W.



[\*] current in F.W.A. mode.

[\*]  $I_E = I_{E0} e^{\frac{V_{BE}}{V_T}}$  which  $V_{BE}$  voltage between Emmitter and base

[\*]  $I_C = \alpha I_E = I_S e^{\frac{V_{BE}}{V_T}} - \beta I_B$

$\alpha$ : current gain  $0.9 < \alpha < 1$   
 $[I_C < I_E]$

[\*]  $I_B = I_{B1} + I_{B2}$   
 diffusion  $\rightarrow$   $\rightarrow$  From combersation

[\*]  $I_B = I_{B0} e^{\frac{V_{BE}}{V_T}} = \frac{I_S}{\beta} e^{\frac{V_{BE}}{V_T}} = \alpha e^{\frac{V_{BE}}{V_T}}$

$\beta$ , common emmitter current gain of PNP

[\*]  $I_E = I_C + I_B$

[\*]  $I_C = \beta I_B$

[\*]  $I_E = (1 + \beta) I_B$

[\*]  $I_C = \left( \frac{\beta}{1 + \beta} \right) I_E = \alpha I_E \rightarrow \alpha = \left( \frac{\beta}{\beta + 1} \right)$

[\*]  $\alpha = \frac{\beta}{\beta + 1} \quad \beta = \frac{\alpha}{1 - \alpha} = \frac{I_C}{I_B}$

$\rightarrow$  very important.

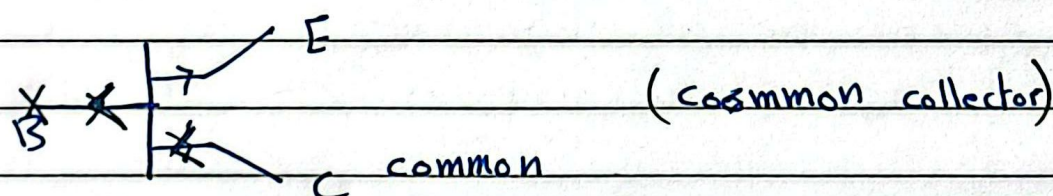
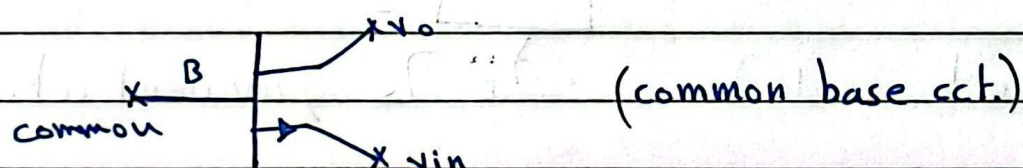
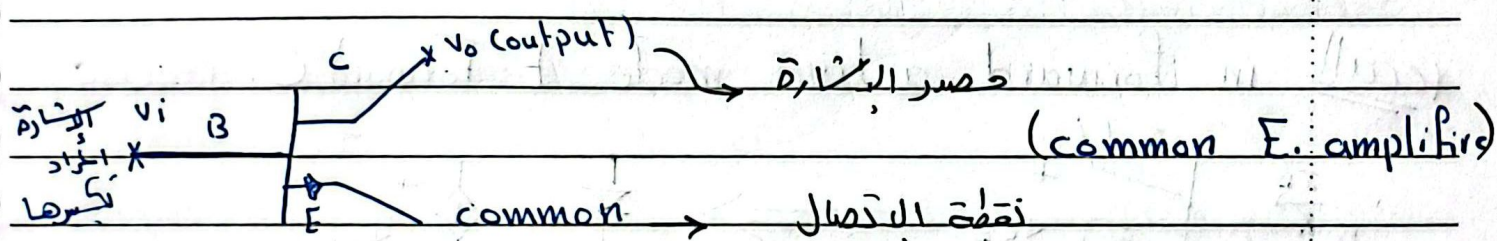


[X] Saturation current mode EF CF

it will work as closed switch  $V_{CE} = 0$

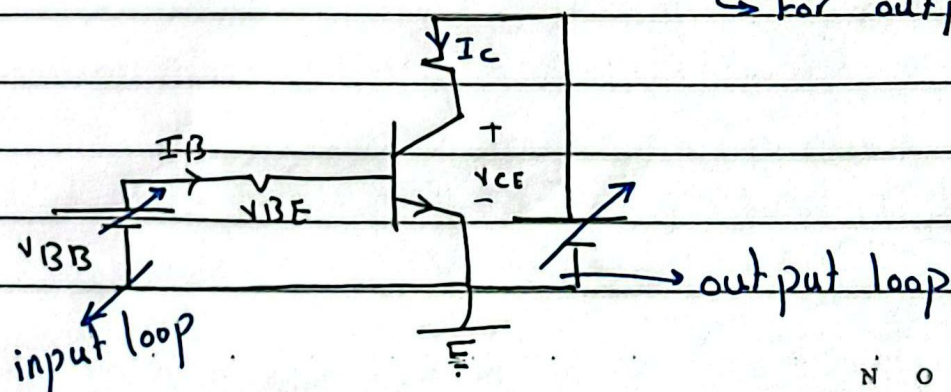
$V_{CE} < V_{CE(sat)} < 0$  For Ideal BJT

[X] (BJT) configuration (connections)



(current voltage characteristic) ( $I$  vs  $V$ )

For output loop  $I_C, V_{CE}$



$\uparrow V_{CE} \rightarrow \uparrow V_{CB}$

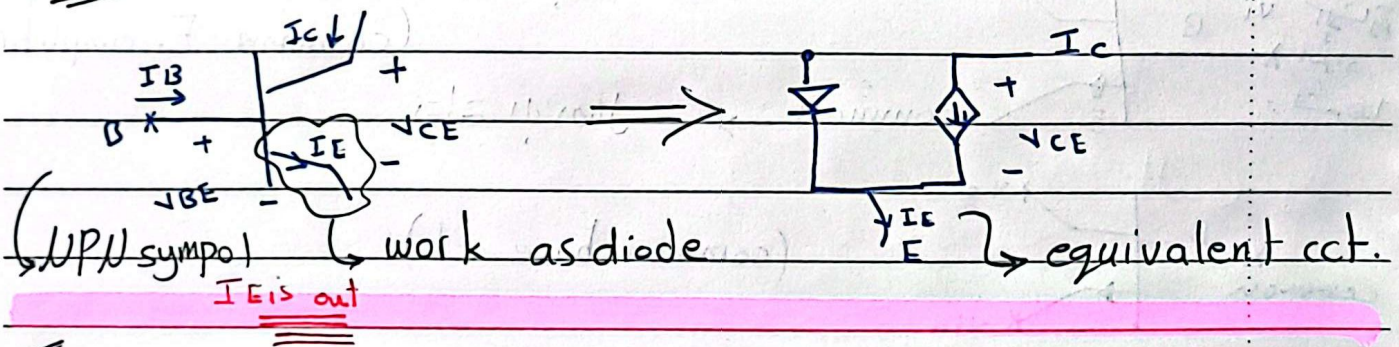


\* we cannot increase the value of  $V_{CE}$  at a certain value the (BJT) will be breakdown given as  $(BV_{CEO})$  measured at  $I_B = 0$

→ \* if  $I_B$  increase Breakdown happen earlier

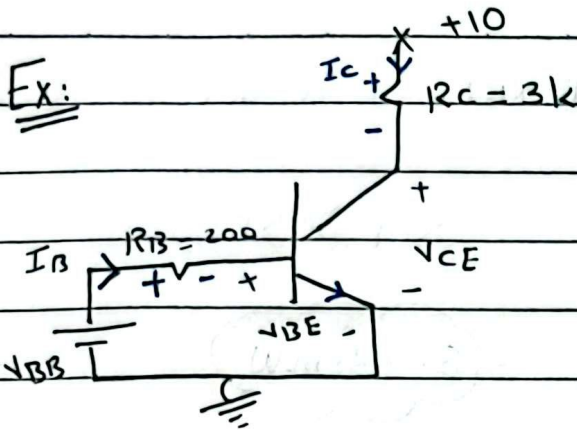
\* DC analysis for BJT ckt. \*

recall in Forward active mode E: Forward C: reverse



Ex





$$V_{CE} = V_{CE(sat)} = 0.3$$

$$\beta = 100, V_{BE} = 0.6$$

calculate  $I_B, I_C, I_E, V_{CE}, P_D$

if  $V_{BB} = 4, 8, 0.5$

Note:  $V$  (saturation)

$V_{CE} = 0$  in Ideal mode

$V_{CE} \approx (0.2 - 0.3)$  in other modes

steps for analysis:

①  $I_E$  direction (polarities)

②  $V_{CE}$  across  $R_C$  (voltage drop)

③ KVL in (Node) (Node) (Node)

④  $V_{BE}$  in (BJT) (F.A.M.)

⑤  $I_B$  in (BJT) (F.A.M.)

BE is Forward  $I_B > 0 \rightarrow V_{BB} > V_{BE}$

BC is reverse  $V_{CE} > V_{BE}$

①  $V_{BB} = 4V$

on input loop:  $-V_{BB} + I_B R_B + V_{BE} = 0$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{4 - 0.6}{200k} = 0.017mA$$

Because we  $\Rightarrow I_C = \beta I_B = 1.7mA$ ,  $I_E = I_B + I_C = 1.717mA$   
assume F.A.M.

$$-10 + I_C R_C + V_{CE} = 0 \Rightarrow V_{CE} = 4.9V$$

by checking if (BJT) in F.A.M.

$$I_B > 0$$

$$V_{BB} > V_{BE} \text{ Forward}$$

$$V_{CE} > V_{BE} \text{ reverse}$$

so the Junction is F.W.



$$[*] P = P_{BE} + P_{BC} = I_B V_{BE} + I_C V_{CE}$$

but

$$I_C \gg I_B$$

$$V_{CE} > V_{BE}$$

so

always like this  $\leftarrow P = I_C V_{CE} = 8.33 \text{ mW}$

② when  $(V_B = 8)$

$$-8 + I_B R_B + V_{BE} = 0$$

$$I_{BE} = 0.037 \text{ mA}$$

$$[*] I_C = 3.7 \text{ mA}$$

$$V_{CE} = -1.11 \text{ V}$$

Since  $I_B > 0 \rightarrow$  B-E Junction is Forward  
 Since  $V_{CE} < V_{BE} \rightarrow$  B-C Junction is Forward  
 So the junction is in saturation mode

$$V_{CE} = V_{CE}(\text{sat}) = 0.3 \text{ V}$$

$$I_C = I_C(\text{sat}) = 10 - V_{CE}(\text{sat}) / R_C = 3.233 \text{ mA}$$

$$I_E = I_C(\text{sat}) + I_B = 3.25 \text{ mA}$$

$$P_D = 0.9818 \text{ by } P_{BE} + P_{BC}$$

Note: in saturation mode

$$I_C V_{CE} \gg I_B V_{BE}$$

$$\frac{I_C}{I_B} < \beta$$

$$\frac{I_C(\text{sat})}{I_B} = \beta_{\text{forced}} = 87.4$$



[3] when  $V_{IB} = 0.5V$   $-0.5 + I_B R_B + V_{BE} = 0$

$I_B = < 0$

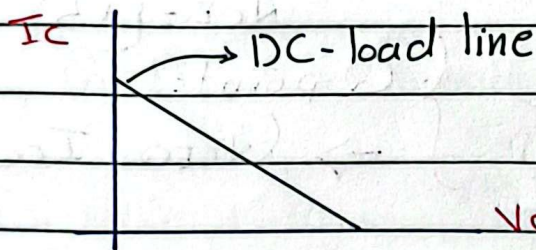
B.E. Junction in reverse

$I_C = 0$ ,  $I_B = 0$ ,  $I_E = 0$ ,  $V_{CE} = 10 - I_C R_C = 10V$   
 $P_D = 0$

[\*] D.C Load line and Q point

[\*] D.C.L.L. (is straight line drawn on transistor)  $(I_C \text{ Vs } V_{CE})$  represent the relation between  $(I_C, V_{CE})$  For BJT in the cct.

[\*] For Q-point:-  $(I_C = I_{CQ}, V_{CE} = V_{CEQ})$



[\*]  $\uparrow V_{IB}$   $\downarrow V_{IB}$   
 $\uparrow I_B$  or  $\downarrow I_B$   
 $\uparrow I_C$   $\downarrow I_C$

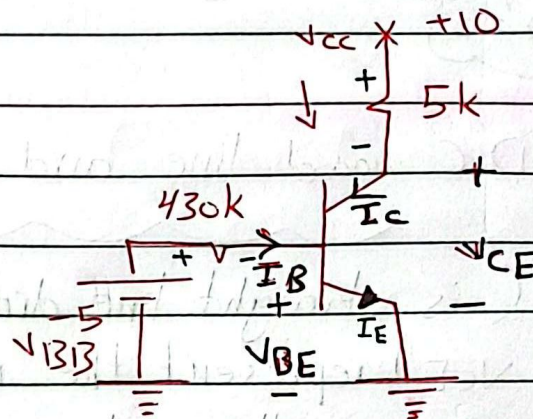
$\Rightarrow \uparrow V_{CC}$  (No change)

$\downarrow Q: up$   $\downarrow Q: down$



Ex: For ckt. shown the (BJT) has  $V_{BE} = 0.7V$  and  $\beta = 100$

- ① calculate  $I_B, I_C, V_{CE}, P_D$
- ② Draw D.C.L. indicate its slope and Q-Point



$$\boxed{1} \quad -5 + 43 I_B + V_{BE} = 0 \Rightarrow I_B = 0.01 \text{ mA}$$

The device is in **F.A.M**  $I_C = \beta I_B = 1 \text{ mA}$

$V_{CE} = +5$

$$\boxed{x} \quad I_C = I_{CQ} = 1 \text{ mA} \quad \left. \begin{array}{l} Q \text{ point:} \\ V_{CE} = V_{CEQ} = 5 \text{ V} \end{array} \right\} \Rightarrow (V_{CEQ}, I_{CQ}) = (5, 1 \text{ mA})$$

② write KVL for C-E loop  $-V_{CC} + I_C R_C + V_{CE} = 0$

OR  $\Leftarrow \boxed{I_C = \frac{V_{CC} - V_{CE}}{R_C}} \quad \text{--- (1)}$

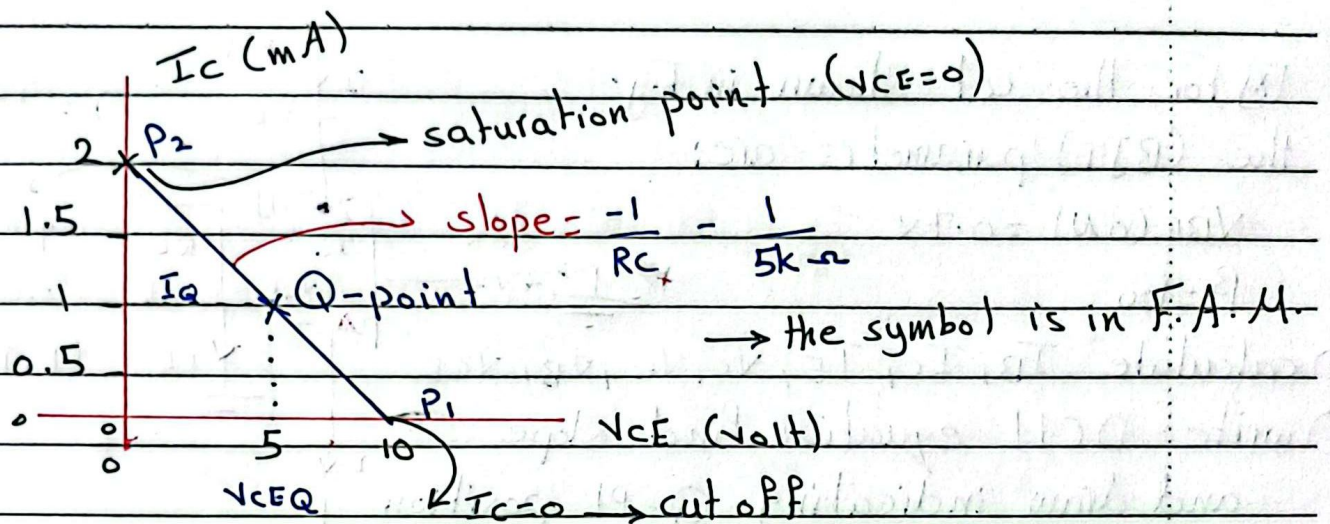
$V_{CE} = V_{CC} - I_C R_C$   
 $\left( m = \frac{-1}{R_C} \right) \quad \text{--- (2)}$

$\boxed{x}$  For  $I_C = 0$   
 $V_{CE} = V_{CC} = 10 \text{ V}$

$\boxed{x}$  For  $V_{CE} = 0$

$$I_C = \frac{V_{CE}}{R} = \frac{10}{5} = 2 \text{ mA}$$





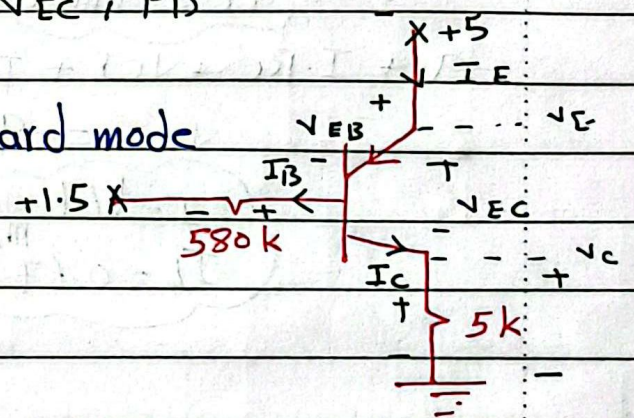
[\*] The previous Question was For NPN Junction  
the next question is For PNP Junction

[\*] For the ckt. shown the BJT has  $\beta = 100$ ,  $V_{EB} = 0.6V$   
calculates  $I_B$ ,  $I_C$ ,  $I_E$ ,  $V_{EC}$ ,  $P_D$

By assuming the BJT in Forward mode

$$-5 + V_{EB} + I_B R_B + 1.5 = 0$$

$$I_B = 0.005 \text{ mA}$$



$$I_C = \beta I_B = 100 * 0.005 = 0.5 \text{ mA}$$

$$V_C = I_C R_C = 2.5 \text{ V}$$

$$V_{EC} = 2.5 \text{ V by KVL}$$

by Testing the Junction is in F.A.M.



[\*] For the ckt shown in Fig. the (BJT) parameters are:

$$V_{BE(ON)} = 0.7V$$

$$\beta = 100$$

① calculate  $I_B, I_C, I_E, V_C, V_E, V_B, V_{CE}$

② write DCLL equation find slope and draw indicating Q-pt position

solution:

by assuming the Junction in Forward mode

$$I_B R_B + V_{BE} + (\beta + 1) I_B R_E - 5 = 0 \quad (\text{KVL For B-E loop})$$

$$I_B = 0.01 \text{ mA}$$

$$I_C = 1 \text{ mA}$$

$$I_E = 1.01 \text{ mA}$$

$$-9 + I_C R_C + V_{CE} + I_E R_E - 5 = 0$$

$$V_{CE} = 9.96 - 3I \rightarrow \text{For } I \rightarrow I = I_C + I_L$$

$$I = 0.67 \text{ mA}$$

$$I_L = 0.67$$

$$V_C = 4$$

$$9 = \frac{V_C}{3} = 1 + \frac{V_C}{6}$$

$$V_{CE} = 4.96 \text{ V}$$

$$P_D = I_C V_{CE} = 4.96 \text{ mW}$$

$$V_E = -0.96 \text{ V}$$

$$V_B = -0.26 \text{ V}$$

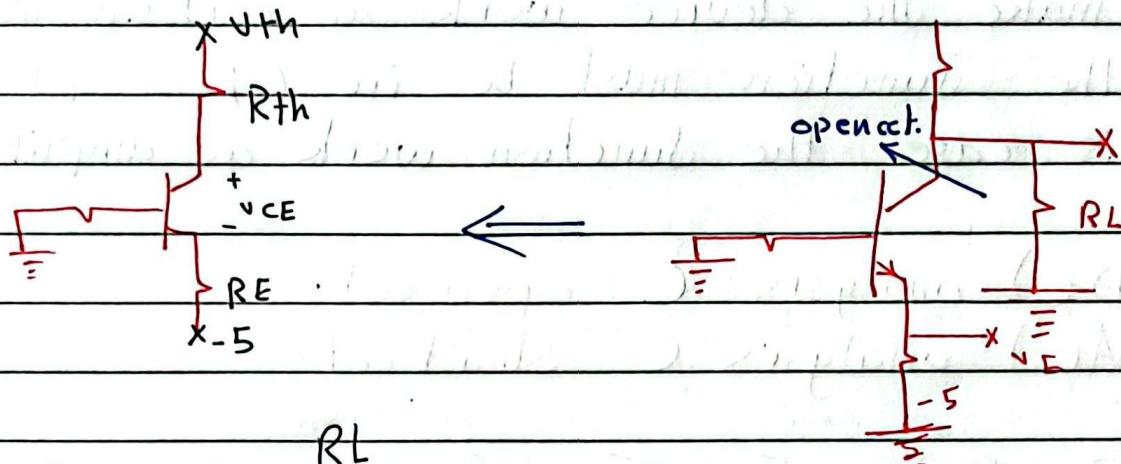
$$\text{From } V_B = -I_B R_B$$

or

$$V_B = V_{BE} - V_E = -0.26 \text{ V}$$



To write D.C.L.L. equation (we must use thivin)



$$[*] R_{th} = R_c \parallel R_L = 3 \parallel 6 = 2k\Omega$$

$$[*] V_{th} = \frac{V_{CC} R_L}{R_c + R_L} = 6V$$

[\*] Now write KVL For C-E loop

$$-V_{th} + I_C R_{th} + V_{CE} + I_E R_E - 5 = 0$$

but  $I_E = \frac{\beta + 1}{\beta} I_C$  : (Because relation between  $I_C, V_C$ )

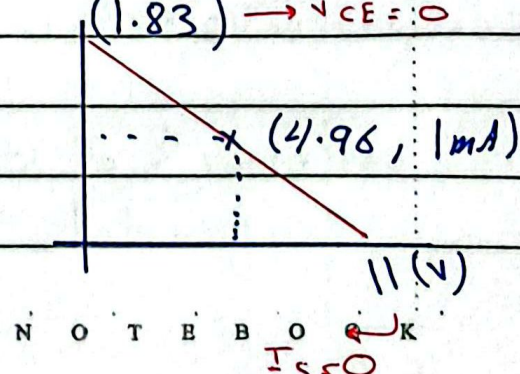
$$V_{CE} = 11 - I_C \left( R_{th} + \frac{\beta + 1}{\beta} R_E \right) \quad \text{D.C.L.L. Equ.}$$

← slope =  $(-1) / \left( R_{th} + \frac{\beta + 1}{\beta} R_E \right)$

[\*] Q point :  $V_{CEQ} = V_{CE} = 4.96V$

$$I_{CEQ} = I_{CE} = 1mA$$

Now by plotting D.C.L.L. eq. (1.83) →  $V_{CE} = 0$





apply (DC) voltage to the electronic device to make the device work at certain mode and the Junction must be in (F.A.M) in this case the Junction work as amplifier

in (DC) analysis C open cct.

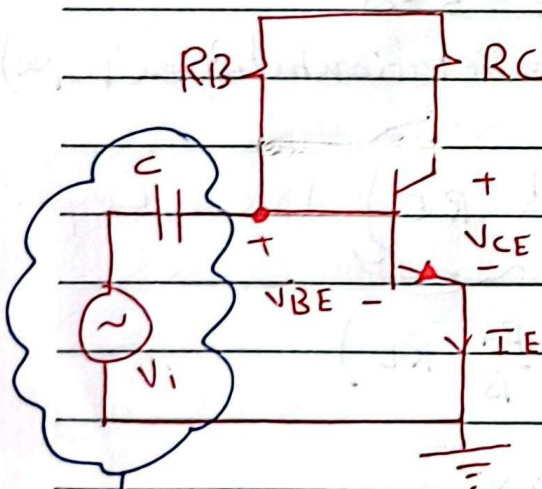
in (AC) analysis C short cct.

[\*] we have Two Types of Biasing:-

First Type

① Single Base resistor Biasing

Q point is very sensitive for changing of  $\beta$



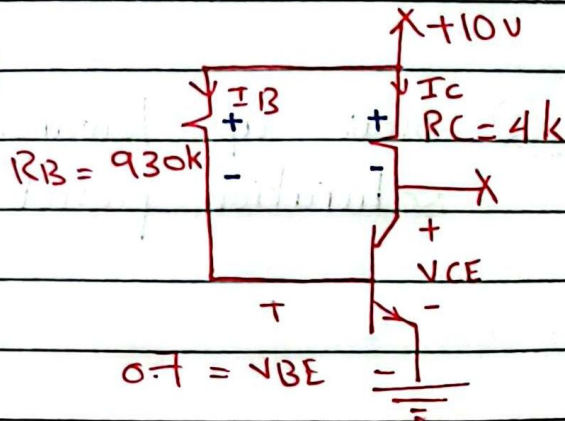
C: is used to isolated the DC from AC

$R_B$ : control the base current  $I_B$

$R_C$ : control C-E voltage

→ in DC it will be: open cct.



Ex 8

For the cct above calculate

- ①  $I_B$ ,  $I_C$ ,  $V_{CE}$  when  $\beta$  is varied from 100  $\rightarrow$  200
- ② calculate  $\Delta I_C\%$ ,  $\Delta V_{CE}\%$  corresponding to change in  $\beta$

SollFor DC analysis  $\rightarrow C \rightarrow$  open cct.  $\rightarrow (X_C = \infty)$ 

$$-10 + I_B R_B + V_{BE} = 0 \rightarrow I_B = 0.01 \text{ mA}$$

$$\textcircled{1} \text{ For } \beta = 100 \rightarrow I_C = \beta I_B = 1 \text{ mA}$$

$$-V_{CC} + I_C R_C + V_{CE} = 0 \rightarrow V_{CE} = 6 \text{ V}$$

$$\textcircled{2} \text{ For } \beta = 200 \rightarrow I_C = \beta I_B = 2 \text{ mA}$$

$$\rightarrow V_{CE} = 2 \text{ V}$$

$$\Delta I_C = \frac{I_{C2} - I_{C1}}{I_{C1}} \times 100\% = \frac{2 - 1}{1} \times 100\% = 100\%$$

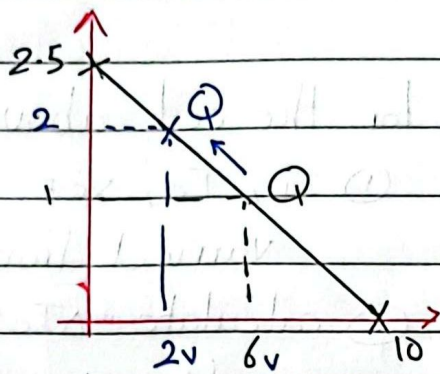
$$\Delta V_{CE} = \frac{V_{CE2} - V_{CE1}}{V_{CE1}} \times 100\% = \frac{2 - 6}{6} \times 100\% = -66.6\%$$

By looking for previous values: when  $\beta$  increased by 100%  $\rightarrow I_C$  increased by 100%  $\rightarrow V_{CE} \downarrow$  by 66.6%

✱ The Q-point is very sensitive to  $\beta$  variation of the cct. has (poor biase stability.)

N O T E B O O K

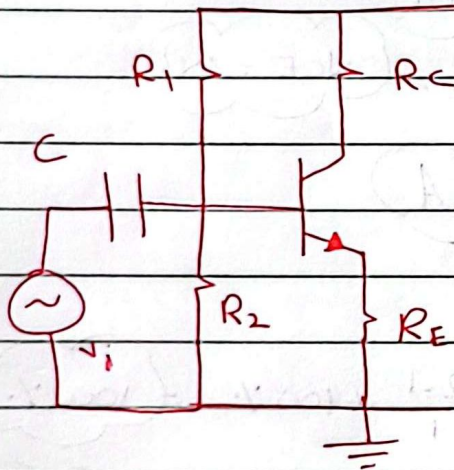




② move up toward saturation point

Second Type:

② voltage divider biasing



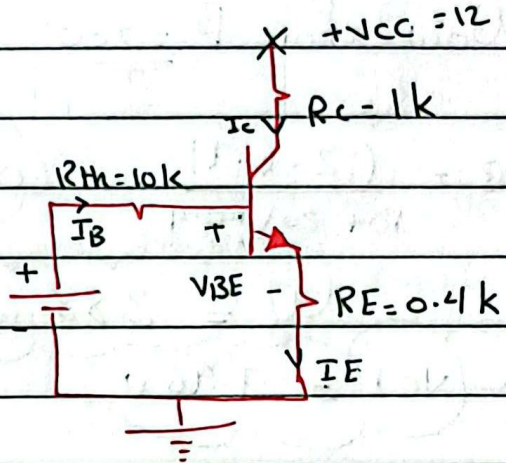
\* Q point doesn't depend on  $\beta$

→ Example in next page.



[\*] For the ckt shown  
the BJT has  $V_{BE(on)} = 0.7$   
calculate  $I_B, I_C, I_E, V_{CE}$   
when  $\beta$  changed ( $100 \rightarrow 200$ )

[\*] calculate  $\Delta I_C\%$ ,  $\Delta V_{CE}\%$   
when  $\beta$  varies ( $100 \rightarrow 200$ )



sol%. To analyse the ckt. it is required to convert the base ckt. into thevenine ckt.

so we need to find  $R_{th}$  when ( $V_{CC} = 0$  (o.ckt.))

[\*]  $R_{th} = R_1 \parallel R_2 = 60 \parallel 12 = 10 \text{ k}\Omega$

[\*]  $V_{th} = \frac{12 \times 12}{60 + 12} = 2 \text{ V} \rightarrow$  by voltage divider.

For finding  $I_B$  by KVL on B-E loop:

$$-V_{th} + I_B R_{th} + V_{BE} + I_E R_E = 0$$

$$I_E = (\beta + 1) I_B \text{ For } \beta = 100$$

$$-V_{th} + I_B (R_{th} + (\beta + 1) R_E) + V_{BE} = 0$$

$$I_B = 25.8 \mu\text{A} \rightarrow I_C = \beta I_B = 2.58 \text{ mA}$$

For finding  $V_{CE}$

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0 \rightarrow V_{CE} = 8.38 \text{ V}$$

$$I_E = (\beta + 1) I_B = 2.6 \text{ mA}$$



[\*] Now For  $\beta = 200$

$$I_B = \frac{(2 - 0.7)}{10 + 201 \times 0.4} = 0.0144 \text{ mA}$$

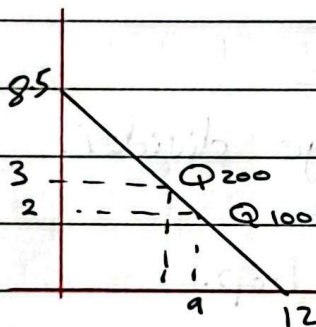
$$I_C = 2.88 \text{ mA}$$

$$I_E = 2.89 \text{ mA}$$

$$V_{CE} = 7.96 \text{ V}$$

Now:-  $\Delta I_C \% = \frac{I_{C2} - I_{C1}}{I_{C1}} \times 100\% = 11\%$

$$\Delta V_{CE} \% = \frac{V_{CE2} - V_{CE1}}{V_{CE1}} \times 100\% = -5\%$$



This ckt has a very good stability

there is very small change

in  $Q$  so (that) the second Type is preferred in Amplifier design.



[X] we first consider the voltage divider on the expression of

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_E} \rightarrow I_C = \beta I_B = \beta \left( \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_E} \right)$$

if  $R_{TH} \ll (\beta + 1)R_E$  and  $\beta \gg 1$

then

$(\beta + 1) \approx \beta$  and  $I_C$  will be independent on  $\beta$

so that (Q-point) independent on  $\beta$  and the ckt. will be biase stable

then  $I_C = \cancel{\beta} \left( \frac{V_{TH} - V_{BE}}{\cancel{R_{TH} + (\beta + 1)R_E}} \right) = \frac{V_{TH} - V_{BE}}{R_E}$

$\swarrow \quad \searrow$   
 $\gg \quad \ll$

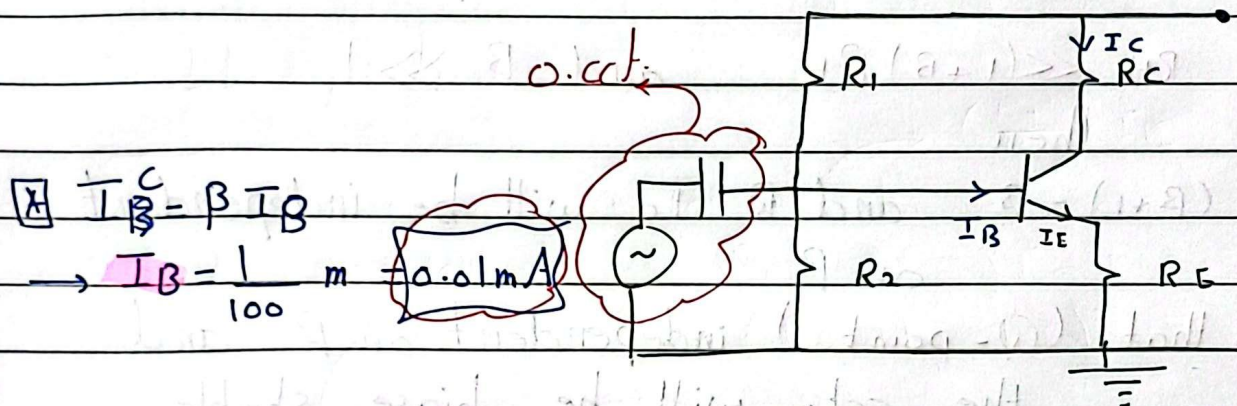
Theory:- ① For a voltage divider when  $R_{TH} \leq 0.1 (\beta + 1) R_E$  the ckt. in biase stable

② For design a ckt.  $R_{TH} = 0.1 (\beta + 1) R_E$



Ex: if  $I_{CQ} = 1 \text{ mA}$ ,  $V_{CEQ} = 5$ ,  $\beta = 100$ ,  $V_{BE} = 0.7$   
 $R_E = 0.2 \text{ k}\Omega$ ,  $V_{CC} = 10 \text{ V}$

Design a bias stable to have the previous quantities:



we need to find  $R_1, R_2, R_C$

⇒ by taking kvl For CE loop

$$-10 + I_C R_C + V_{CE} + I_E R_E = 0 \Rightarrow I_E = \left( \frac{\beta + 1}{\beta} \right) I_C$$

$$R_C = \frac{10 - 5 - 1.01 \times 0.2}{I_C} = 4.798 \text{ k}\Omega \leftarrow (I_E = 1.01 \text{ mA})$$

⇒ For finding  $R_1$  and  $R_2$ , we know that the cct is bias stable so ⇒

$$R_{Th} = R_1 // R_2 \rightarrow R_{Th} = 0.1 (\beta + 1) R_E \rightarrow R_{Th} = 2.02 \text{ k}\Omega$$

⇒ For  $V_{Th}$  using kvl on BE loop

$$-V_{Th} + I_B R_{Th} + V_{BE} + I_E R_E = 0 \rightarrow V_{Th} = 0.922$$

⇒ No For finding  $R_1, R_2$

we know that

$$(V_{Th} = \frac{V_{CC} \cdot R_2}{R_1 + R_2}) \times R_1 \rightarrow R_{Th}$$

$$R_1 V_{Th} = V_{CC} R_{Th} \rightarrow R_1 = 21.9 \text{ k}\Omega$$

by using  $R_{Th} = \frac{R_1 R_2}{R_1 + R_2} \rightarrow R_2 = 2.225 \text{ k}\Omega$



Ex: For the cct shown Find,  $R_{th}$ ,  $V_{th}$ ,  $I_C$ ,  $V_{CE}$   
write DCLL and ~~the~~ draw the line.

when  $\beta = 50$   $V_{BE} = 0.6$

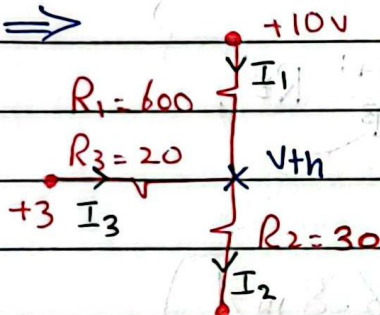
in this cct. we can't

use  $V_{th} = \frac{V_{CC} R_2}{R_1 + R_2}$

because there isn't any  
ground connection all

are connected with sources, so we need to analyze the  
cct.

So  $\Rightarrow$

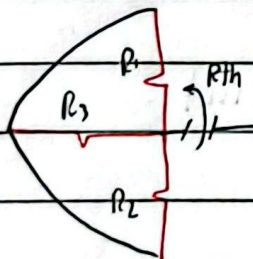


For finding  $(V_{th})$  we must  
kill the sources and  
replace it with short cct.

or we can use KCL as we  
will see

by using KCL:-

$$I_1 + I_3 = I_2$$



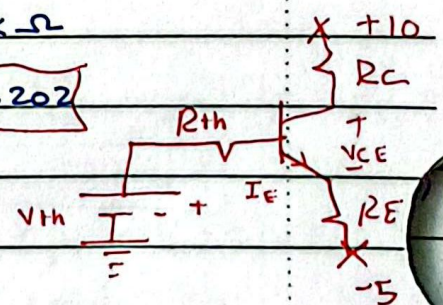
$$\frac{3 - V_{th}}{20} + \frac{10 - V_{th}}{60} - \frac{V_{th} + 4}{30} \text{ by math } \Rightarrow V_{th} = 1.83V$$

For  $R_{th}$   $R_1 \parallel R_2 \parallel R_3 = 10k\Omega$

$$(\beta + 1) I_B = 5.202$$

$$-V_{th} + I_B R_{th} + V_{BE} + I_E R_E - 5 = 0$$

$$I_C = \beta I_B = 5.1mA \quad I_B = 0.102mA$$





For finding  $V_{CE}$ :  $-V_{CC} + I_C R_C + V_{CE} + I_E R_E - 5 = 0$

$$V_{CE} = 3.678V$$

Since  $I_B > 0$   $V_{CE} > V_{BE}$  The junction is in F.A.M.

DC LL equation:

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E - 5 = 0$$

$$\text{but } I_E \rightarrow V_{CE} = 15 - I_C R_C - \left(\frac{\beta+1}{\beta}\right) I_C R_E$$

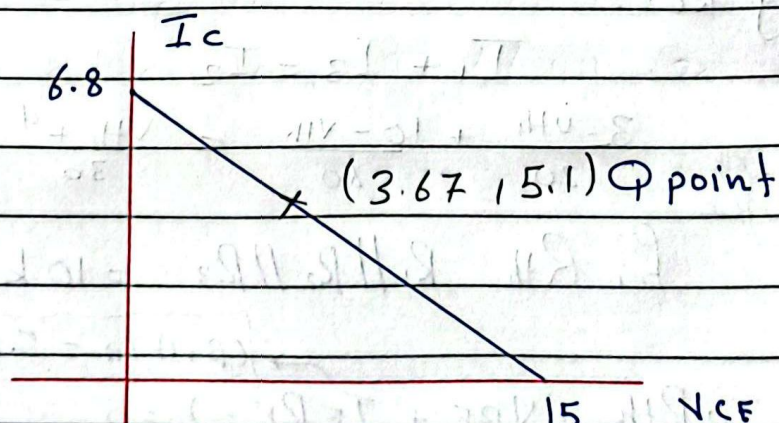
$$V_{CE} = 15 - I_C \left( R_C + \frac{\beta+1}{\beta} R_E \right)$$

$$\text{slope} = - \frac{1}{R_C + \frac{\beta+1}{\beta} R_E}$$

the Q-point  $(3.67V, 5.1mA)$

$$\text{A) when } V_{CE} = 0 \rightarrow I_C = 6.8mA$$

$$\text{A) when } I_C = 0 \rightarrow V_{CE} = 15V$$



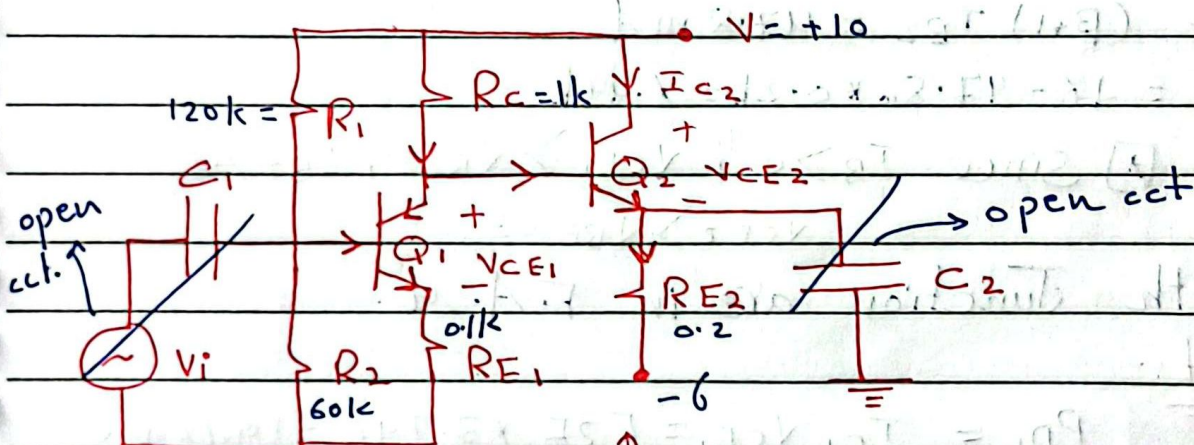


Now, we will deal with ccts that contain more than one transistor which can be the same type or ~~than~~ two types

\* Types of connected:

- A. cascade connection
- B. cascode connection

\* cascade multistage:



Ex: For the cct. shown given  $Q_1, Q_2$  identical with  $\beta = 100$ ,  $V_{BE} = 0.6V$ ,  $V_{CE(sat)} = 0.3V$  Find

$I_{B1}, I_{C1}, V_{CE1}, P_{D1}, I_{B2}, I_{C2}, V_{CE2}, P_{D2}$

For  $Q_1$ ,  $R_1 \parallel R_2 = 120 \parallel 60 = 40k\Omega$

$$V_{th} = \frac{10 \times 60}{180} = 3.33 \text{ volt}$$

$$V_{th} - I_{B1} R_{th} + V_{BE} + (R_1 + 1) I_{B1} R_{E1} = 0$$

$$I_{B1} = 0.0525 \text{ mA}$$

$$V_{CE1} = 10 - I_{C1} R_C - 5.3 \times 10^{-1}$$

$$I_{C1} = \beta I_{B1} = 5.25 \text{ mA}$$

$$V_{CE1} = 9.4 - I_{C1} R_C$$

$$I_{E1} = 5.3 \text{ mA}$$

NOTEBOOK



For Finding  $I$

$$I = I_{C1} + I_{B2}$$

$$[*] -V_{C1} + V_{BE} + (\beta + 1) I_{B2} R_{E2} - 6 = 0$$

$$I_{B2} = \frac{(V_{C1} + 6) - V_{BE}}{(\beta + 1) R_{E2}} = \frac{V_{C1} + 5.3}{20.2k}$$

$$[*] \frac{10 - V_{C1}}{R_C} = 5.25 + \frac{V_{C1} + 5.3}{20.2k}$$

For  $R_C = 1k\Omega \rightarrow V_{C1} = 4.27V$

So that:-

$$I_{B2} = 0.47mA \quad I = 5.7mA$$

$$V_{CE1} = 9.47 - 5.7 \times 1 = 3.7V$$

$$I_{C2} = \beta I_{B2} = 100 \times 0.47 = 47mA$$

$$I_{E2} = (\beta + 1) I_{B2} = 47.8mA$$

$$V_{CE2} = 16 - 47.8 \times 0.2k = 6.44V$$

$$[*] \text{ Since } I_B > 0, V_{CE1} > V_{BE}, I_{B2} > 0, V_{CE2} > V_{BE}$$

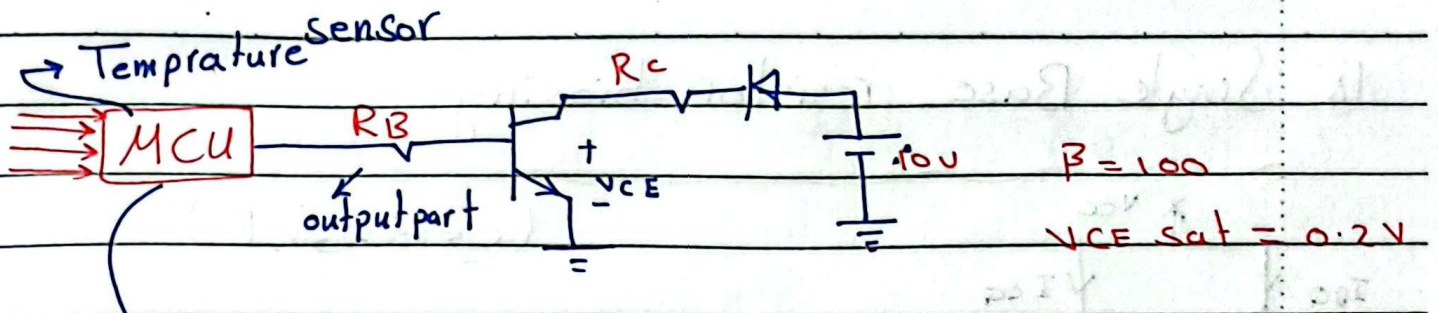
Both Junction are in F.A.M

So that:-

$$P_{D1} = I_{C1} V_{CE1} = 5.25 \times 3.746 = 19.66mW$$

$$P_{D2} = I_{C2} V_{CE2} = 47 \times 6.44 = 302.68mW$$





Temp  $> 25^\circ C \rightarrow 5V$  (on)

Temp  $< 25^\circ C \rightarrow 0V$  (off)

$\rightarrow I_C = 20 \text{ mA}$  when Temp  $> 25^\circ C$  (5V)

$\rightarrow I_C = 0$  when Temp  $< 25^\circ C$  (0V)

by taking KVL on the output loop

$$-V_{CC} + V_D + I_C R_C + V_{CE} = 0$$

in F.A.M.

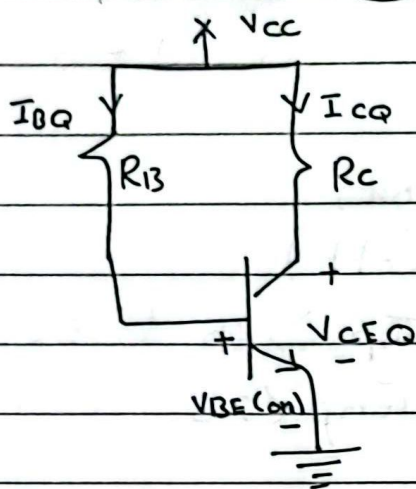
in Sat.

$$I_C = \beta I_B$$

$$\frac{I_C}{I_B} \ll \beta$$



## [\*] Single Base resistor biasing



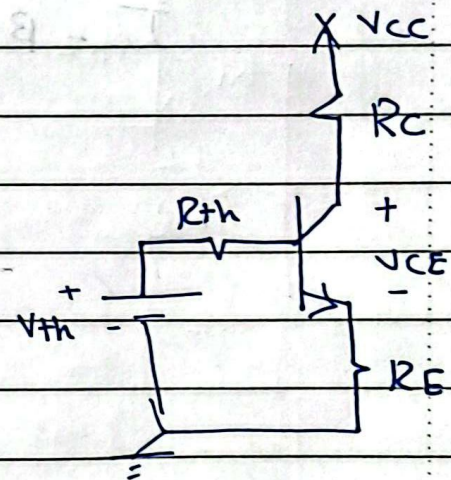
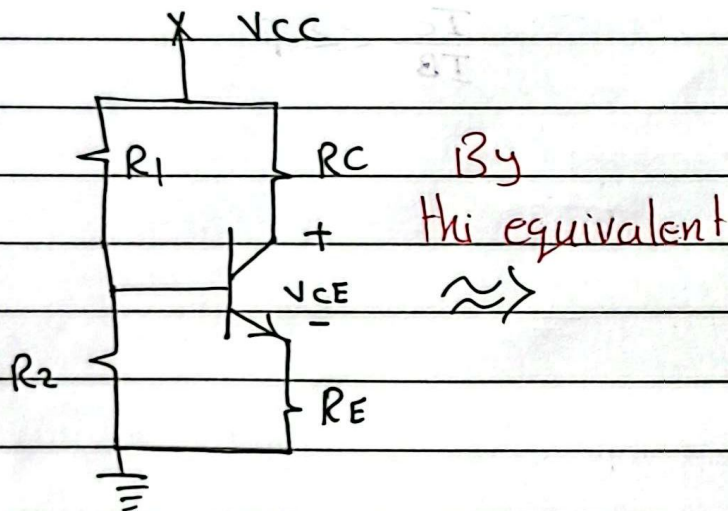
(E. بيوتنه خافى)

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = \beta I_B$$

$$V_{CE} = V_{CC} - I_C R_C$$

## [\*] voltage divider bias



$$V_{TH} = \frac{V_{CC} \cdot R_2}{R_1 + R_2}$$

$$R_{TH} = R_1 \parallel R_2$$

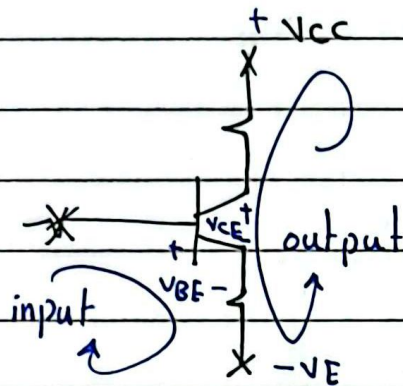
$$I_C \approx I_E$$

$$R_{TH} = 0.1 (1 + \beta) R_E$$



[\*] positive and negative cycle:

( $R_B$  is not)



$$I_E \approx I_C$$

$$V_{Th} = \frac{R_2}{R_1 + R_2} (V^+ - V^-) + V^-$$

[\*] Emmitter Biase

[\*] collector Biase

→ more stable

[\*] in cascode cct.

$$V_{CE1} = V_{CE2} \Rightarrow$$

$$I_{C1} \approx I_{C2}$$

$$I_{R1} \approx I_{R2} \approx I_{R3} \approx I_{Biase}$$

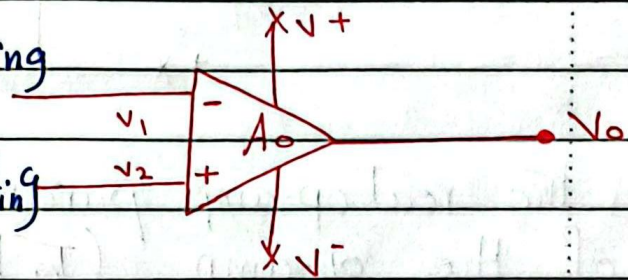
$$R_1 + R_2 + R_3 = \frac{V^+}{I_{Biase}}$$



OP-amp is an electronic device in IC form contain multistage (direct connected) with a very higher voltage gain, compared to BJT and Diode. It is a (voltage controlled voltage source).

Inverting

noninverting



where:  $v_o = A_o (v_2 - v_1)$

where:

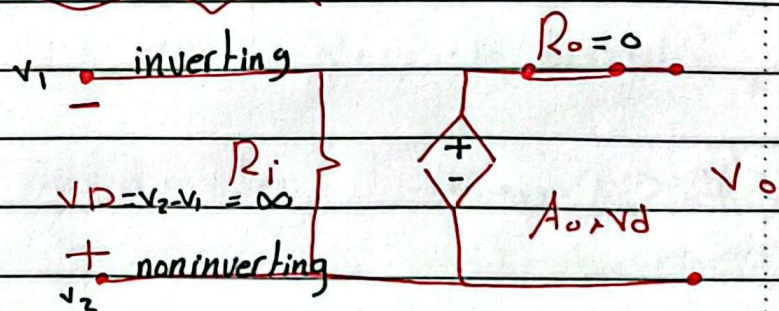
$A_o$ : open-loop gain

$v_1, v_2$ : (signal of inverting and noninverting)

$v^+, v^-$ : (positive, negative biasing voltage)

⊗ Ideal op-amp parameters:

- 1)  $R_{in} = \infty$
- 2)  $R_o = 0$
- 3) open loop gain =  $\infty$
- 4) Band width =  $\infty$





✱ Non-ideal op-Amp parameters: (real op-amp)



✱ The real op-amp parameters depend on the type of the op-amp (Technology: Bipolar, BiFET, MosFET) where:

- ①  $R_{in} \neq \infty = 2 \text{ mega}$
- ②  $R_o \neq 0$  (60-70)  $\Omega$
- ③ B.W  $\neq \infty$  1 mega Hz
- ④  $A_o \neq \infty = 10^7$

✱ If  $R_L$  is connected, then:

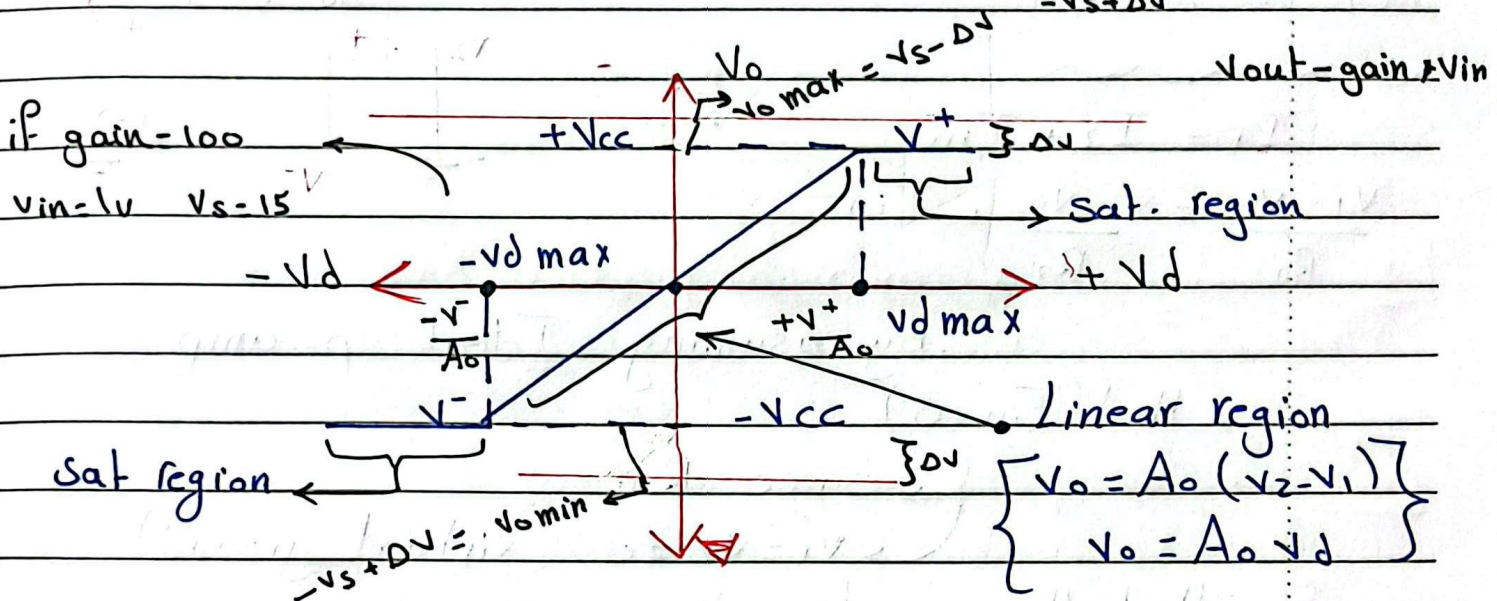
✱ In ideal op-Amp:  $v_o = A_o v_d$  (Independent on  $R_L$ )

✱ In nonideal op-Amp:  $v_o = A_o v_d \frac{R_L}{R_L + R_o}$   
(depend on  $R_L$ )



[x] Transfer characteristic (plot of  $V_o$  versus  $V_i$ )

[\*] The plot is obtained from the equ.  $v_0 = A_0(v_2 - v_1)$  but it is not exceed  $(+v)$  ex  $[v^- < v_0 < v^+]$



⊛ operating region:

① Non-saturation region:- when  $[-V_{dmax} > V_d < V_{dmax}]$   
 In this region:  $V_o = A_o (V_2 - V_1) \rightarrow V_A$   
 (linear region)

② saturation region: when  $[-V_{dmax} < v_d < V_{dmax}]$

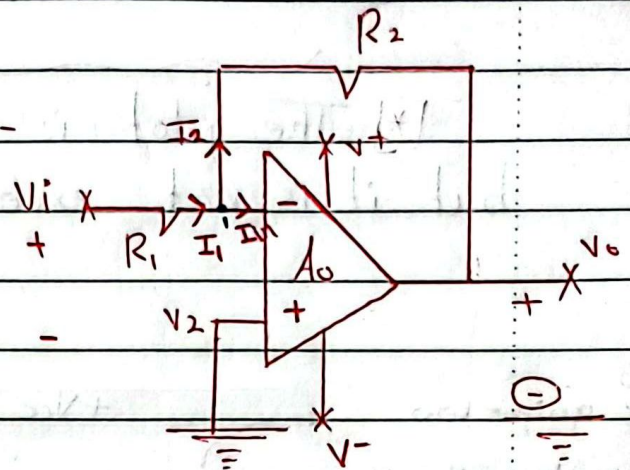
in this region:  $v_0 = \mp V$



## ① Linear applications

## ② inverting amplifier :-

KCL at Node 1



$$I_1 = I_2 + I_{in}$$

$$\frac{V_i - V_1}{R_1} = \frac{V_1 - V_o}{R_2} + I_{in}$$

by assuming Ideal Op-amp

→ so that ( $I_{in} = 0$ )→ Since  $R_{in} = \infty$ →  $V_1 = V_2 = 0$  (virtual ground)

→ So that the equation become:-

$$\frac{V_i}{R_1} = -\frac{V_o}{R_2}$$

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1} = A_v$$

 **$A_v$ :-** closed loop gain → (180° phase shift)

⊠ Input resistance:  $R_{in}$

$$-V_i + I_1 R_1 = 0$$

$$R_i = \frac{V_i}{I_1} = R_1$$

$$R_{in} = R_1$$

⊠ notice that:-  $A_o$  = open loop gain  
 $A_v$  = closed loop



[\*] virtual short and virtual ground:

[\*] when  $V_1 = V_2$  (v. short)  $\rightarrow$  Node 1, 2 not connected

[\*] IF  $V_1, V_2$  is connected to ground

$\rightarrow V_1 = V_2 = 0$  (virtual ground)

Ex: design an Inverting amplifier to have

$A_v = -50$   $R_{in} = 10k\Omega$  draw  $V_o(t) \Rightarrow v_i = 0.1 \sin \omega t$

Solution:-

we deal with inverting amplifier

$\rightarrow R_i = R_1 = 10k\Omega$

$\rightarrow A_v = -\frac{R_2}{R_1} \Rightarrow R_2 = 50 R_1 = 500k\Omega$

$\rightarrow A_v = \frac{V_o}{V_i} \Rightarrow V_o = A_v \cdot V_i = -50 \times 0.1 \sin \omega t$

$V_o = -5 \sin \omega t$

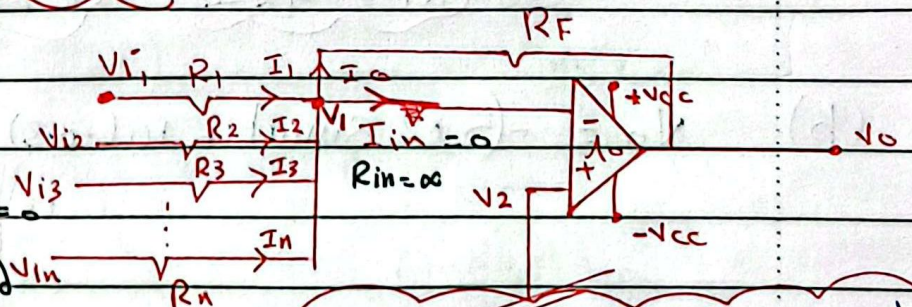
[\*] b. Summing amplifier:

KCL at node 1

$I_1 + I_2 + I_3 + \dots = I_{in} + I_o$

$\rightarrow I_{in} = \frac{V_i - V_o}{R_F}$   $V_1 = V_2 = 0$

ground



$\rightarrow \frac{V_{i1}}{R_1} + \frac{V_{i2}}{R_2} + \frac{V_{i3}}{R_3} = -\frac{V_o}{R_F}$

$\rightarrow V_o = -\left(\frac{R_F V_{i1}}{R_1} + \frac{R_F V_{i2}}{R_2} + \dots\right)$

N O T E B O O K



$$V_o = - \left( \frac{R_F}{R_1} V_{i1} + \frac{R_F}{R_2} V_{i2} + \frac{R_F}{R_3} V_{i3} + \dots \right)$$

↳ each  $V_i$  will be multiple by a certain Factor summed and inverted

→ If all signals are amplified by same gain then  $R_1 = R_2 = R_3 = R_4 = \dots = R$

$$V_o = - \frac{R_F}{R} (V_{i1} + V_{i2} + V_{i3} + \dots)$$

Ex: Design an amp to produce  $V_o = -(5V_a + 10V_b)$

b) For  $V_a = 2 \sin \omega t$ ,  $V_b = -0.3$  draw  $V_o(t)$

وئسول

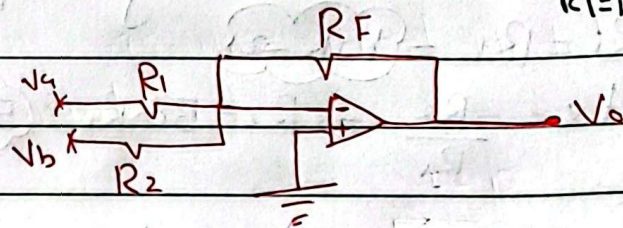
وئسول

$R_1 = R_2 = R_3 = \dots$

$$V_o = -10(V_a + V_b + V_c)$$

$$R_1 = R_2 = R_3$$

وئسول

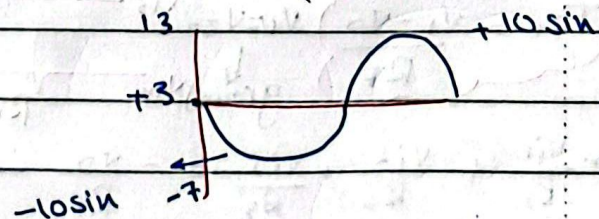


$$V_o = - \left( \frac{R_F}{R_1} V_a + \frac{R_F}{R_2} V_b \right) \rightarrow \frac{R_F}{R_1} = 5 \quad \frac{R_F}{R_2} = 10$$

assuming  $R_F = 20k\Omega$   $k\Omega = 10^3 \Omega$

$$\text{So } R_1 = 4k\Omega \quad R_2 = 2k\Omega$$

$$(b) \quad V_o = -(5 \times 2 \sin \omega t + 10(-0.3)) = (3 - 10 \sin \omega t)$$





Ex: Design a cct to produce  $V_o = -10(V_a + V_b)$   
draw  $V_o(t)$  when  $V_a = 0.4$

Solution:

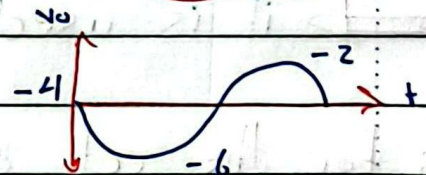
$$V_b = 0.2 \sin \omega t (V)$$

$$[*] \quad V_o = -\frac{R_F}{R} (V_{i1} + V_{i2})$$

$$\frac{R_F}{R} = 10$$

→ by assuming  $R_F = 10k\Omega$  →  $R = 1k\Omega$

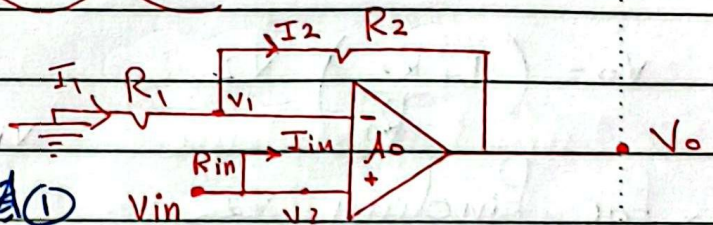
$$V_o = -10(0.4 + 0.2 \sin \omega t) \rightarrow -4 - 2 \sin \omega t$$



[\*] [C] No. 1 = inverting amplifier:

input is given to non inverting terminal

by taking kcl at node A (1)



$$I_1 = I_2 + I_{in} \rightarrow \text{Ideal model} \rightarrow I_{in} = 0$$

$$V_1 = V_2 = V_i \text{ (virtual short)}$$

$$-\frac{V_{in}}{R_1} = \frac{V_{in} - V_o}{R_2} \rightarrow \frac{V_o}{R_2} = \frac{V_{in}}{R_1} + \frac{V_{in}}{R_2}$$

$$V_o = \left(1 + \frac{R_2}{R_1}\right) V_{in}$$

$$\frac{V_o}{V_{in}} = A_v = \left(1 + \frac{R_2}{R_1}\right)$$

→ it will be amplified not inverted ( $R_{in} = \infty$ )



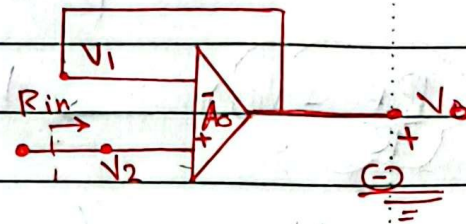
## [D] voltage Follower: (Buffer)

it is a special case of noninverting which  $R_1 = \infty$   $R_2 = 0$   
 $V_1 = V_2 = V_{in}$  (virtual short)

[X] Since  $V_1 = V_0$

$$V_0 = V_{in}$$

$$A_v = \frac{V_0}{V_{in}} = 1$$

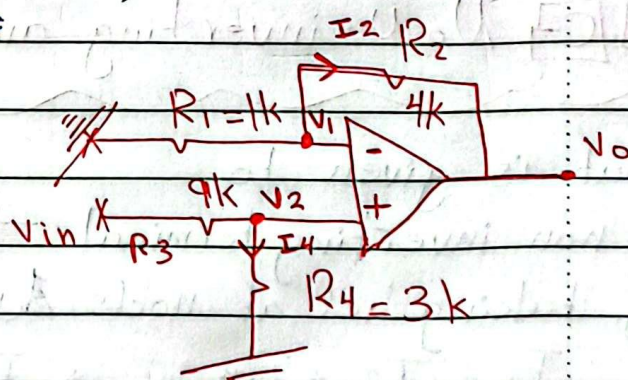


it is used to minimize loading effect.

Ex: For the ckt. shown assume ideal model Design  
 For ( $V_i = 8 \sin \omega t$  V)

~~We have voltage follower~~

$$[X] V_0 = \left(1 + \frac{R_2}{R_1}\right) V_2$$



For Finding  $V_2$

$$V_2 = \frac{V_{in} R_4}{R_3 + R_4} \rightarrow V_0 = \left(1 + \frac{R_2}{R_1}\right) \left(\frac{R_4}{R_3 + R_4}\right) V_{in}$$

$$\frac{V_0}{V_{in}} = \left(1 + \frac{R_2}{R_1}\right) \left(\frac{R_4}{R_3 + R_4}\right) = \left(1 + \frac{4}{1}\right) \left(\frac{3}{9+3}\right) = 1.25$$

$$V_0 = A_v V_{in} \rightarrow 1.25 \times 8 \sin \omega t = 10 \sin \omega t$$



Ex: For the ~~args~~ above cct. calculate  $I_4, T_2, V_1$  For the same input. For the last cct.

$$V_2 = \frac{R_4}{R_3 + R_4} V_i = \frac{3}{9+3} (8 \sin \omega t) = 2 \sin \omega t$$

$$I_4 = \frac{V_2}{R_4} = 2 \sin \omega t / 3k = 0.66 \sin \omega t \text{ mA}$$

$$V_1 = V_2 \text{ virtual short} = 2 \sin \omega t \text{ V}$$

$$I_2 = \frac{V_1 - V_o}{R_2} = 2 \sin \omega t - 10 \sin \omega t / 4k = -2 \sin \omega t \text{ mA}$$

E Difference Amp. (in this cct. both terminals are used)  $\rightarrow$  (inverting, noninverting)

This cct. will be:

$$V_o = A_d (V_{i2} - V_{i1})$$

$\rightarrow$  the gain of diff. amp.

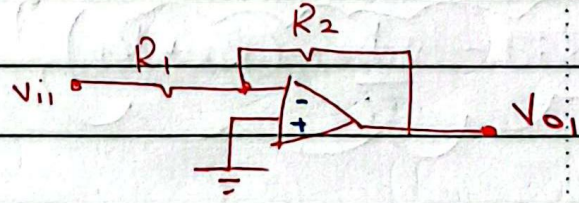
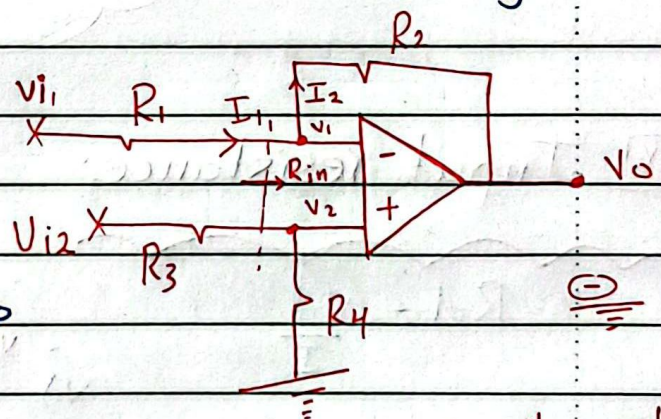
we will use (superposition) to

find expression of  $A_d$

1) For  $V_{i1}$  ( $V_{i2} = 0$ )  $\rightarrow V_2 = \frac{V_{i2} \times R_4}{R_4 + R_3} = 0$  so the cct.

The cct. become (inverting amp.)

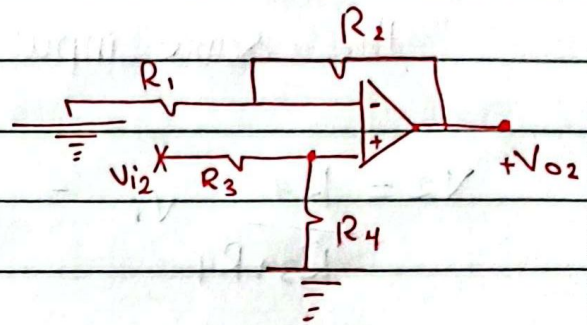
$$V_{o1} = -\frac{R_2}{R_1} V_{i1}$$





2) For  $V_{i2}$  ( $V_{i1} = 0$ )

$$V_{o2} = \left( \frac{R_4}{R_4 + R_3} \right) \left( 1 + \frac{R_2}{R_1} \right) V_{i2}$$



(Non inverting)

So:-  $V_o = V_{o1} + V_{o2}$

$$-\frac{R_2}{R_1} V_{i1} + \left( \frac{R_4}{R_4 + R_3} \right) \left( 1 + \frac{R_2}{R_1} \right) V_{i2}$$

if  $\frac{R_4}{R_3} = \frac{R_2}{R_1}$  then  $V_o = \frac{R_4}{R_3} (V_{i2} - V_{i1})$

So:-  $A_d = \frac{V_o}{V_{i2} - V_{i1}} = \left[ \frac{R_4}{R_3} = \frac{R_2}{R_1} \right]$

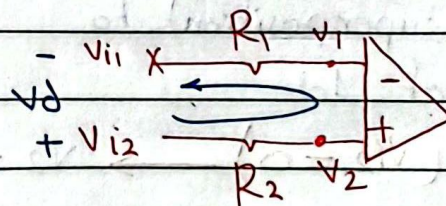
Input resistance:

$$R_d = \frac{V_d}{I}$$

$$-V_d + I_i R_3 + I_i R_1 = 0$$

$$V_d = I_i (R_3 + R_1)$$

$$R_{id} = \frac{V_d}{I_i} = (R_3 + R_1)$$





Ex: Design a difference Amp. to have  $R_{id} = 6k$  and  $A_d = 50$ ? calculate  $V_o$  for  $V_{i1} = 2V$

$$V_{i2} = 2.1V$$

solution: we need a difference-amp.

→ For this ckt.  $A_d = \frac{R_2}{R_1}$  (with assumption  $\frac{R_2}{R_1} = \frac{R_4}{R_3}$ )  
also  $R_{id} = R_1 + R_3$

→ TF we assume  $R_2 = R_4$ ,  $R_1 = R_3$

$$(R_1 + R_3) = 6k = R_{id} \rightarrow R_1 = R_3 = 3k$$

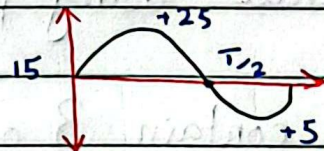
$$\rightarrow A_d = \frac{R_2}{R_1} = 50 \rightarrow R_2 = R_4 = 50 \times 3 = 150k \Omega$$

$$\rightarrow V_o = A_d (V_{i2} - V_{i1}) = 50 (2.1 - 2) = 5V = V_o \text{ dc}$$

$$\text{if } V_{i1} = -0.2 \sin \omega t$$

$$V_{i2} = 0.3 V_{dc}$$

$$\text{So } V_o = 50 (0.3 - -0.2 \sin \omega t) = (15 + 10 \sin \omega t) = V_o$$



Ex2: Design a difference Amp to have  $A_d = 100$ ,  $R_{id} = 20k$  using an ideal op-Amp

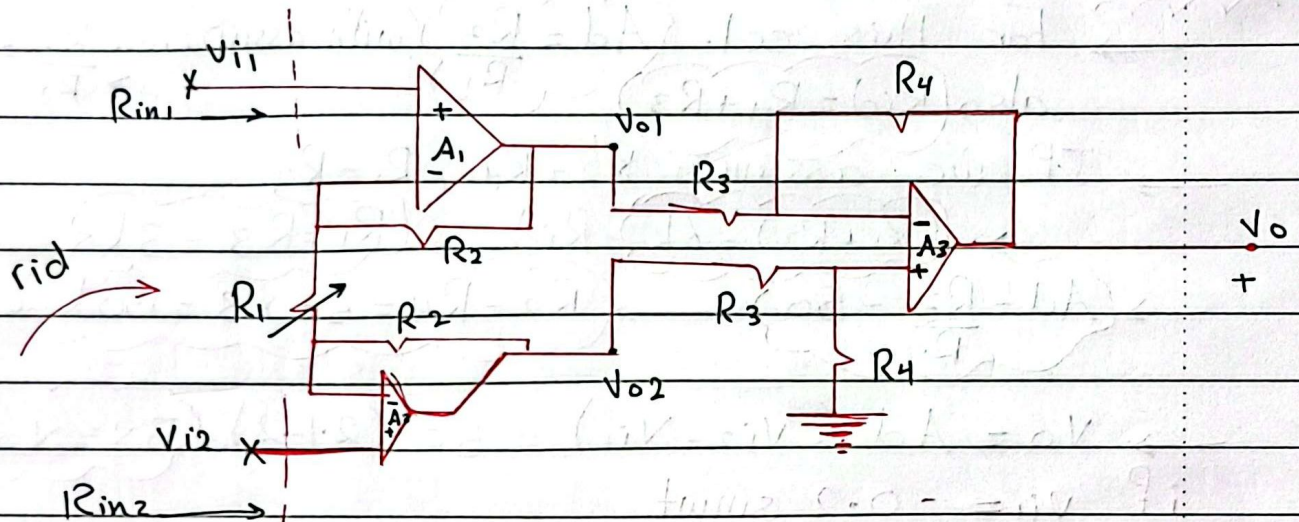
To satisfy  $\frac{R_2}{R_1} = \frac{R_4}{R_3}$ , let  $R_1 = R_3$ , and  $R_2 = R_4$

$$\rightarrow R_1 = R_3 = 10k \text{ because } R_{id} = 2R_1 = 20k$$

$$\text{Since } A_d = \frac{R_2}{R_1} = \frac{R_4}{R_3} = 100 \rightarrow R_2 = R_4 = 1000k \Omega = 1M \Omega$$



[X] To increase  $R_{in}$  or  $A_d$  we must accept high value for  $R_2, R_4$  which is Not desired in design  $\rightarrow$  to solve this problem we use (Instrumentation) amplifier



[X] This amp. achieves high, adjustable single element dependent gain and very high input resistance using proper values for resistance

$\rightarrow$  it contain 3 op-amp:

$A_1, A_2 \rightarrow$  non-inverting

$A_3 \rightarrow$  Different-amp

$R_{in1} = \infty, R_{in2} = \infty$

$R_{id} = \infty$

To derive this cct. we use (super position)

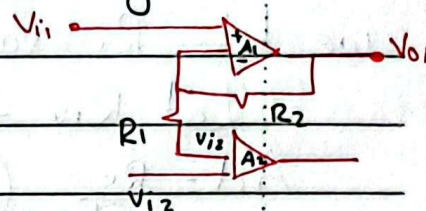


① Effect of  $V_{i1}$  ( $V_{i2} = 0$ ) ( $A_1$  is non inverting)

$$V_{o1}' = \left(1 + \frac{R_2}{R_1}\right) V_{i1}$$

② Effect of  $V_{i2}$  ( $V_{i1} = 0$ ) ( $A_1$  inverting)

$$V_{o1}'' = -\frac{R_2}{R_1} V_{i2}$$



$$\rightarrow V_{o1} = V_{o1}' + V_{o1}''$$

$$\text{So } V_{o1} = \left(1 + \frac{R_2}{R_1}\right) V_{i1} - \frac{R_2}{R_1} V_{i2}$$

For  $A_1$  and  $A_2$

$$\text{But } V_o = (V_{o2} - V_{o1}) \frac{R_4}{R_3} \quad (\text{Difference amp})$$

$$V_o = \frac{R_4}{R_3} \left[ \left(1 + \frac{R_2}{R_1}\right) V_{i2} - \frac{R_2}{R_1} V_{i1} \right] - \left[ \left(1 + \frac{R_2}{R_1}\right) V_{i1} - \frac{R_2}{R_1} V_{i2} \right]$$

$$\rightarrow V_o = \frac{R_4}{R_3} \left(1 + \frac{2R_2}{R_1}\right) (V_{i2} - V_{i1})$$

$$A_d = \frac{V_o}{V_{i2} - V_{i1}} = \frac{R_4}{R_3} \left(1 + \frac{2R_2}{R_1}\right)$$

There is two of ( $R_2, R_3, R_4$ ) single ( $R_1$ )

So  $A_d$  depend only on  $R_1$

so to change  $A_d$  we change  $R_1$  only.



Ex: Design an (I.A) to have a gain ranging from (5  $\rightarrow$  500) using a max resistance  $100k\Omega$  assuming ideal op-amp.

we take  $R_1$  variable which it is  $\begin{matrix} \nearrow R_{Fixed} \\ \searrow R_{variable} \end{matrix}$   $R_1 = R_{if} + R_{iv}$

Let  $R_{iv} = 100k\Omega$

$$A_d = \frac{R_4}{R_3} \left( 1 + \frac{2R_2}{R_1} \right) \text{ when } \begin{matrix} \nearrow R_1 \text{ is min} \rightarrow A_d \text{ max} \\ \searrow R_{min} = R_{if} \quad (R_{iv} = 0) \end{matrix}$$

$$R_{max} = 100k + R_{if}$$

$$500 = \frac{R_4}{R_3} \left( 1 + \frac{2R_2}{R_{if}} \right) \rightarrow 2R_2 = 249 R_{if} \quad \text{--- (1)}$$

let  $= 2$

$$5 = \frac{R_4}{R_3} \left( 1 + \frac{2R_2}{100 + R_{if}} \right) \rightarrow 2R_2 = 150 + 1.5 R_{if}$$

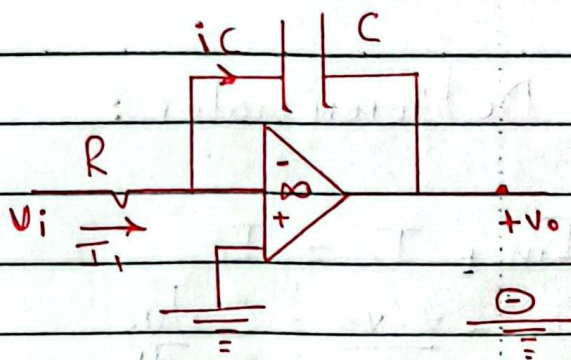
From (1) and (2)  $R_{if} = 0.606k\Omega$   $R_2 = 75.5k\Omega$   
 $R_3 = 1k\Omega$   $R_4 = 2k\Omega$



KCL at node ①

$$I_1 = I_{in} + I_c$$

$$\frac{V_i - V_1}{R} = I_{in} + C \frac{dV_c}{dt}$$



where  $V_c = V_1 - V_o$  but  $I_{in} = 0$ ,  $R_{in} = \infty$ ,  $V_2 = V_1 = 0$  (virtual short)

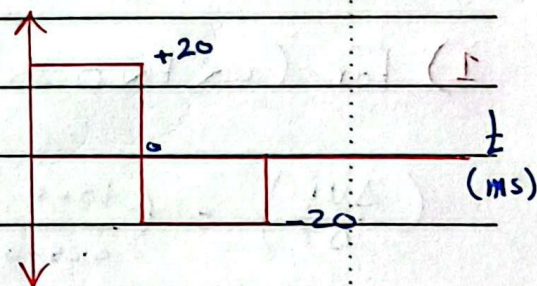
$$\boxed{\times} \frac{V_i}{R} = 0 + -C \frac{dV_o}{dt} \rightarrow dV_o = -\frac{V_i}{RC} dt$$

$$\rightarrow V_o = -\frac{1}{RC} \int V_i \cdot dt \rightarrow \text{eqn}$$

Ex: calculate and Draw  $v_o(t)$  for indicate input when  $R = 1k\Omega$ ,  $C = 1\mu F$

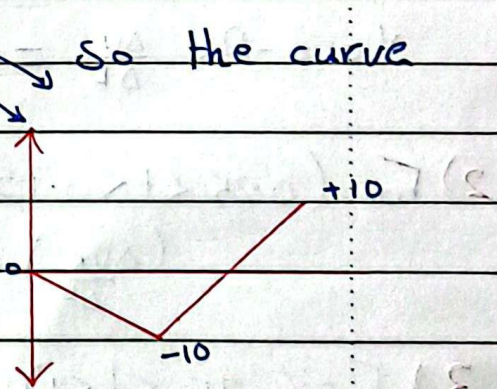
1) For  $0 < t < 0.5 \text{ ms}$

$$V_o = \frac{-1}{10^3 \times 10^{-6}} \int (0.5 \times 20) = -10 \text{ V}$$



2) For  $(0.5 < t < 1) \text{ ms}$

$$\begin{aligned} V_o &= \frac{-1}{RC} \int -20 dt = 1000 \times 20t \\ &= 1000 \times 20(1 - 0.5) \\ &= +10 \text{ V} \end{aligned}$$





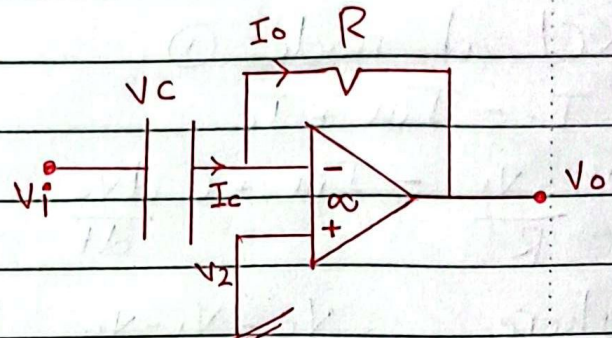
### \* Differentiator:

$$I_{in} \approx I_o = I_c$$

$$I_{in} + \frac{V_i - V_o}{R} = C \frac{dV_c}{dt}$$

$$\rightarrow V_1 = V_2 = 0 \text{ (virtual ground)} \quad I_{in} = 0 \rightarrow (R_{in} = \infty)$$

$$V_c = V_i - V_1 = V_i$$

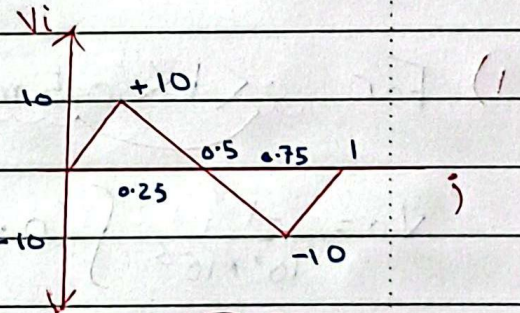


So  $V_o$  will be  $V_o = -RC \left( \frac{dV_i}{dt} \right)$

\* Ex: For the diff. shown, draw  $V_o(t)$  for the indicated input, when  $R = 500 \Omega$   $C = 1 \mu F$

1) For  $(0 < t < 0.25) \text{ ms}$

$$\left( \frac{\Delta V_i}{\Delta t} \right) = \left( \frac{10 - 0}{0.25 - 0} \right) = 40 \times 10^3$$



$$V_o = -RC \frac{\Delta V}{\Delta t} = -0.5 \times 10^3 \times 10^{-6} \times 40 \times 10^3 = -20 \text{ V}$$

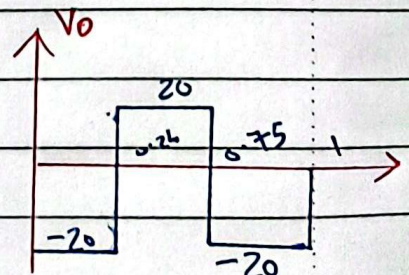
2) For  $(0.25 < t < 0.75)$

$$\left( \frac{\Delta V_i}{\Delta t} \right) = (-10 - 10) / (0.75 - 0.25) = +20 \text{ V}$$

3) For  $(0.75 < t < 1)$

$$\frac{\Delta V_i}{\Delta t} = 4 \times 10^4$$

$$V_o = -20 \text{ V}$$

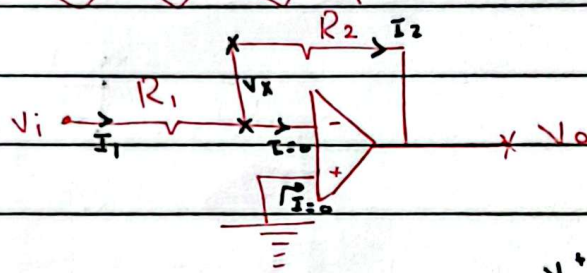


N O T E B O O K



### \* inverting op-amp :

$$I_1 = \frac{V_i - V_x}{R_1}$$



$$I_2 = \frac{V_x - V_o}{R_2}$$

(KCL on node x)

$$\sum I_{in} = \sum I_{out}$$

$$I_1 = I_2 + 0$$

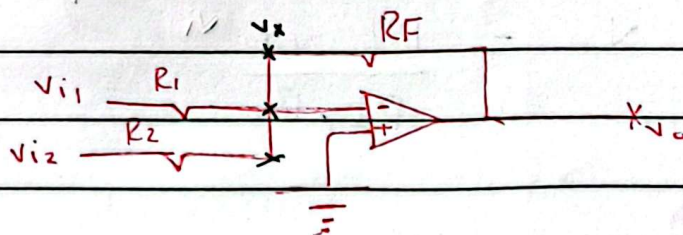
$$\frac{V_i - V_x}{R_1} = \frac{V_x - V_o}{R_2}$$

$$V_x = 0$$

$$V_o = -\frac{R_2}{R_1} V_i$$

$$\text{gain} = \frac{V_o}{V_{in}}$$

### \* Summation amplifier:



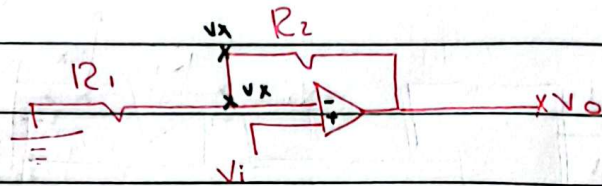
KCL / node x

$$I_1 + I_2 = I_F + I^-$$

$$V_o = -R_F \left( \frac{V_{i1}}{R_1} + \frac{V_{i2}}{R_2} \right)$$



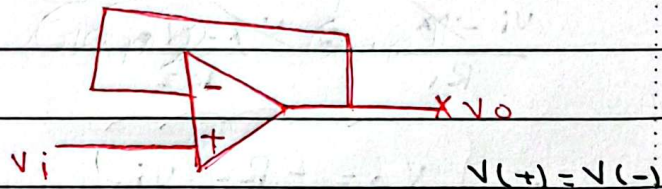
Non inverting



$$V_o = V_i \left( 1 + \frac{R_2}{R_1} \right)$$

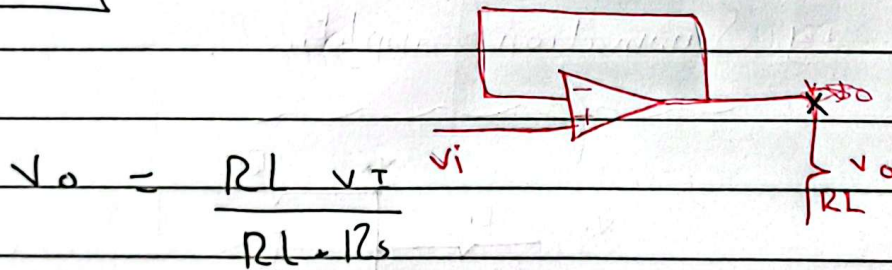
Voltage Follower (Buffer)

~~$$V_o = \left( 1 + \frac{R_2}{R_1} \right) V_i$$~~



$$V(+) = V(-)$$

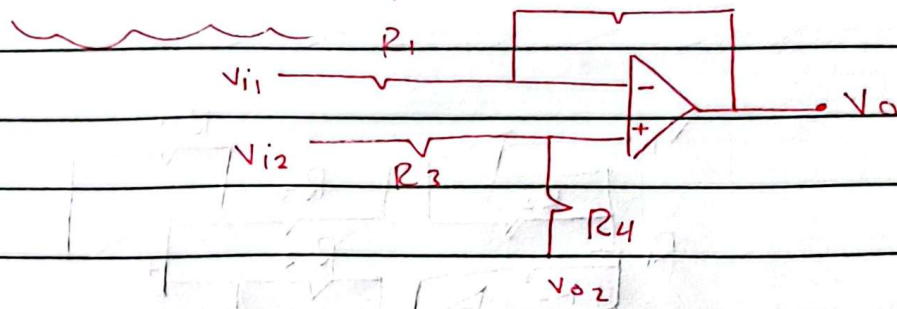
$$V_o = V_i$$



$$V_o = \frac{R_L}{R_L + R_s} V_i$$



### [\*] Difference amplifier $R_2$

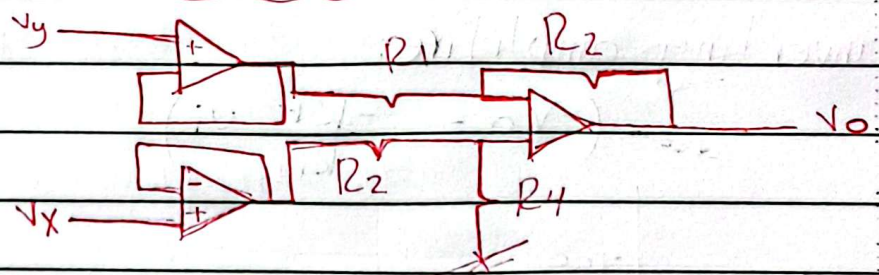


$$V_o = -\frac{R_2}{R_1} V_{i1} + \left(1 + \frac{R_2}{R_1}\right) \left(\frac{R_4}{R_3 + R_4}\right) V_{i2}$$

$$\left(\frac{R_4}{R_3} = \frac{R_2}{R_1}\right)$$

$$V_o = \frac{R_2}{R_1} [V_{i2} - V_{i1}]$$

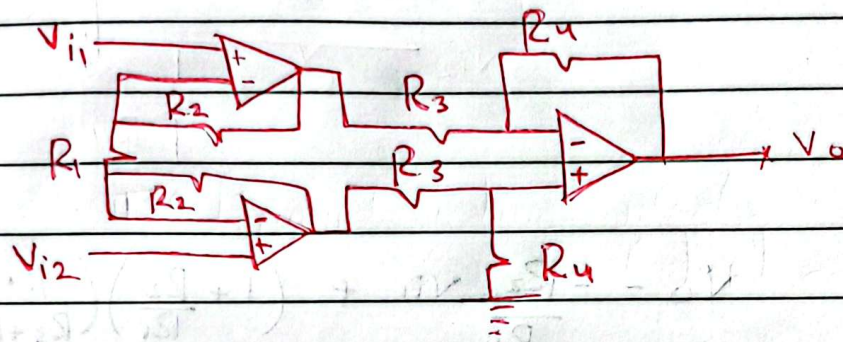
### [\*] Difference with buffer:



$$V_o = \frac{R_2}{R_1} [V_x - V_y]$$



## [X] instrumentation amplifier:



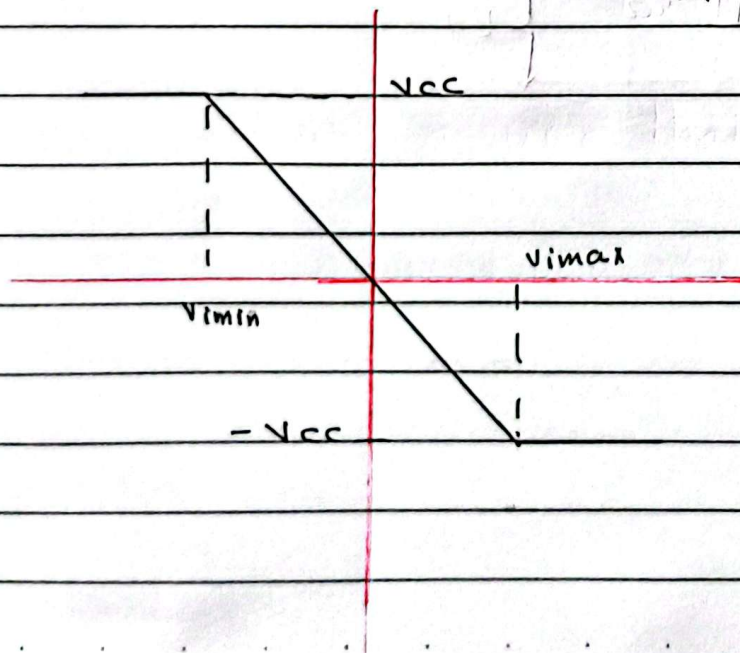
$$V_{i1} \neq V_{i2}$$

$$V_o = \underbrace{\left( \frac{R_4}{R_3} \right)}_{\text{Gain 2}} \underbrace{\left( 1 + \frac{2R_2}{R_1} \right)}_{\text{Gain 1}} (V_{i2} - V_{i1})$$

## [X] relation between input and output:

### [i] inverting amplifier:

$$V_o = -\frac{R_F}{R_i} V_i$$





## \* Difference summing:

due to  $u_1$

$$V_{o1} = -\frac{R_F}{R_1} u_{i1}$$

due to  $u_2$

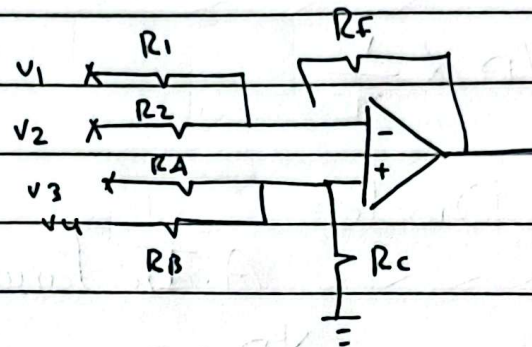
$$V_{o2} = -\frac{R_F}{R_2} u_{i2}$$

due to  $u_3$

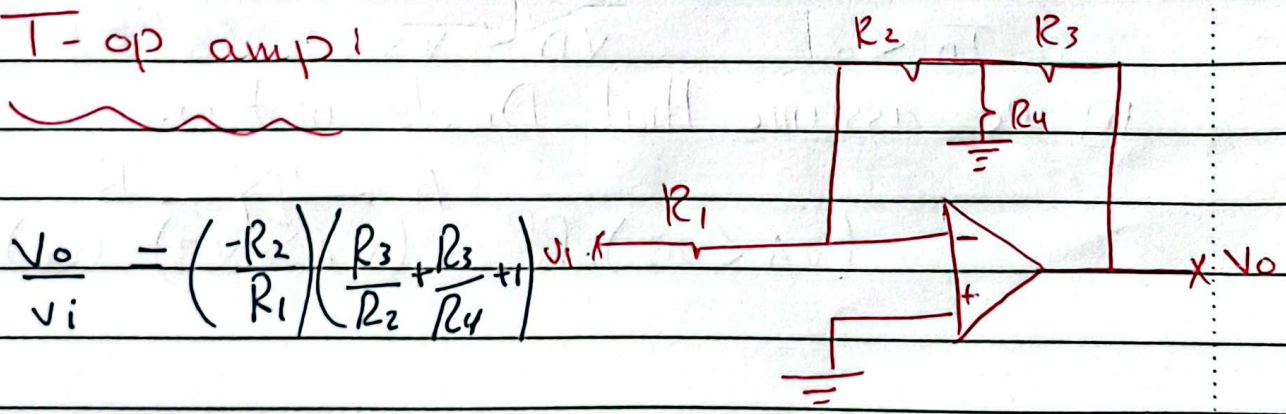
$$V_o = \frac{(R_C \parallel R_B) u_3}{R_A + (R_C \parallel R_B)} * \left( 1 + \frac{R_F}{R_1 \parallel R_2} \right)$$

due to  $u_4$

$$V_o = \frac{(R_C \parallel R_A) u_{i4}}{R_B + (R_C \parallel R_A)} \left( \frac{R_F}{R_1 \parallel R_2} + 1 \right)$$



T-op amp



$$\frac{V_o}{V_i} = \left( -\frac{R_2}{R_1} \right) \left( \frac{R_3}{R_2} + \frac{R_3}{R_4} + 1 \right)$$



$\uparrow T \rightarrow \uparrow$  covalent bond breaking  $\rightarrow \uparrow \bar{e}$  Free movement  
 $\uparrow$  holes

$\uparrow$  shell radius  $\rightarrow \uparrow$  electron energy

$\uparrow$  shell number  $\rightarrow \uparrow$  electron from nucleus  
 $\downarrow$  attractive force  $\rightarrow \downarrow$  band gap  $\rightarrow \uparrow$  Free electron  
 $\rightarrow \uparrow$  electron energy

$\uparrow T \rightarrow \uparrow$  of thermal energy on valance e.

$\uparrow$  Free electron  $\rightarrow \uparrow$  conductivity  $\rightarrow \uparrow$  holes

$\uparrow$  current  $\rightarrow \uparrow$  conductivity

$\uparrow T \rightarrow \downarrow V$  Diode  $\rightarrow$  (constant I)

$\downarrow \uparrow V_i \rightarrow \downarrow \uparrow I \rightarrow I_L$  Fixed  $\downarrow \uparrow I = \downarrow \uparrow I_z + I_L$

$\downarrow \uparrow R_L \rightarrow \uparrow \downarrow I_L \rightarrow I$  Fixed  $I_{Fixed} = \downarrow \uparrow I_z + \uparrow \downarrow I_L$

$\downarrow R$



$$\downarrow C = \frac{I_c}{R_c} \downarrow$$

[1]  $F_{in} = 60 \text{ Hz}$ ,  $F_o$  of a half wave  
 $F_o = 120$  For Full wave 120

[2] The peak output voltage = 100V, Ideal diode  
 PIV for each diode in a center tap rectifier

$$V_{peak} = \frac{V_{sec}}{2} \rightarrow V = 50$$

[\*] when the base resistor increase the collector voltage (increase)

[\*] collector resistance  $\downarrow$  collector voltage  $\uparrow$

[\*] ~~Full~~ wave rectifier has most ripple

[\*] when reverse voltage  $\downarrow$  Depletion region become smaller

[\*] For normal operation of NPN transistor

[\*] positive with respect to emitter

[\*] negative with respect to collector

[\*] at zero Temperature The intrinsic semiconductor has no electrons or free or holes

[\*] small variation in the output voltage of DC power supply (ripple voltage)



\*) peak output voltage is  $100V$  the PIV for each diode in center tap full wave  $50$  in ideal diode.

\*) when  $V_{source} \uparrow$  in zener which current become constant. load current

\*) Trivalent atom have 3 electrons

\*) width of diode depletion layer will  $\downarrow$  decrease when diode forward bias.

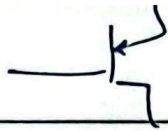
\*) if one diode of center tap rectifier, the average voltage will  $\downarrow$

\*) how many free electrons does P-Type semiconductor contain? same produced by thermal energy

\*) The merge between free electron and holes? recombination

\*) The purpose of a pentavalent impurity is to? increase number of free electron





\*) when the peak output voltage is 100 the PIV for each diode in a center tap Full wave rectifier ~~is 100~~ 50

\*) if zener diode in zener regulator is connected to wrong polar it must be closet to 0.7

\*) when the same secondary voltage and filter which has the most ripple?  
half ~~full~~ wave rectifier

\*) The purpose of pentavalent impurity increase number of free electrons

\*) if one of the diodes in Full wave bridge rectifier open the average voltage will decrease

\*) cct. that add a positive or negative dc voltage to an input sin wave clipper

\*) the voltage follower has a closed loop voltage gain of unity.



\*) The practical op-amp IC 741 has a high voltage  $200,000$

\*) if the emitter resistance doubles in a VDB ckt.

The collector current will drop in half

\*) if  $R_C \uparrow$  the collector voltage  $\downarrow$

$$I_E = I_B + I_C$$

\*) The Q point of a VDB ckt is a Hyper sensitive to change in current gain almost totally insensitive to change in current gain

\*)  $R_E \downarrow \Rightarrow$  collector voltage  $\downarrow$

\*) NPN positive with respect to emitter  
negative with respect to collector

\*) pnp transistor in certain ckt (active mode)  
collector is connected to ground, emitter is  
connected to negative voltage

\*)  $R_B \uparrow \Rightarrow$  collector  $V \uparrow$

\*)  $R_E \uparrow \Rightarrow$  collector  $V \uparrow$

\*)  $R_E$  open  $\Rightarrow$  collector  $V =$  supply voltage

\*) TSEB, Base current must be small

\*) common-emitter configuration amplifier provide  
medium voltage gain, medium current gain

\*) pnp transistor the major carrier in emitter are Holes

\*) Beta is the ratio of  $I_C / I_B$

\*) The collector voltage is not sensitive to change in  
emitter resistance, current gain

\*)  $R_C \uparrow$  voltage gain  $\downarrow$



- ☒ lower  $Q$  point minimum current gain
- ☒ output signal of a collector is always out phase of input signal
- ☒ current gain of PNP transistor is ratio  $(C)$  to  $(B)$
- ☒ base voltage less than the base supply voltage
- ☒ voltage divider is noted to stable  $Q$  point
- ☒  $\uparrow$  collector supply voltage (none of above)
- ☒ PNP transistor (negative) to emitter (positive) to collector
- ☒ the largest theoretical voltage gain with a common collector configuration (1)
- ☒  $\downarrow$  in base resistor move  $Q$  point up
- ☒  $R_E \downarrow \rightarrow Q$  move up
- ☒  $\uparrow R_E \rightarrow \downarrow I_E$
- ☒ emitter base has stable  $Q$ -point
- ☒  $V_{DB}$  needs only one supply. operate in active region
- ☒ voltage emitter less than Base voltage
- ☒ Base voltage less than Base supply voltage
- ☒  $V_{BD}$  is noted for Stable  $Q$ -point.
- ☒ Base voltage of two supply Near 0v
- ☒  $R_E \uparrow \rightarrow I_E \downarrow$  ☒  $R_C \downarrow \rightarrow V_C \uparrow$
- ☒ emitter resistance same as voltage between emitter and Ground
- ☒ on characteristic of a voltage follower inversion
- ☒ when comparing energy gap ( $S_i$ ) is higher



most of electrons in NPN flow out of base lead

Summing amplifier Two or more input signals

Summing amplifier produce the negative sum of input voltages.

Feedback path in an ideal op-amp consist of a capacitor