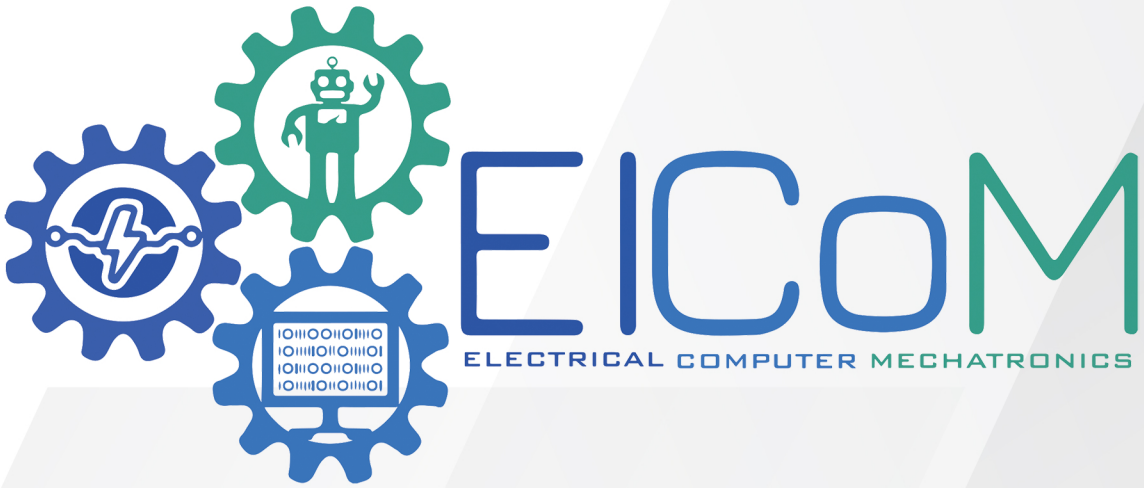
تقدم لجنة ElCoM الاكاديمية



دفتر لمادة:

الكترونيات رقمية

من شرح:

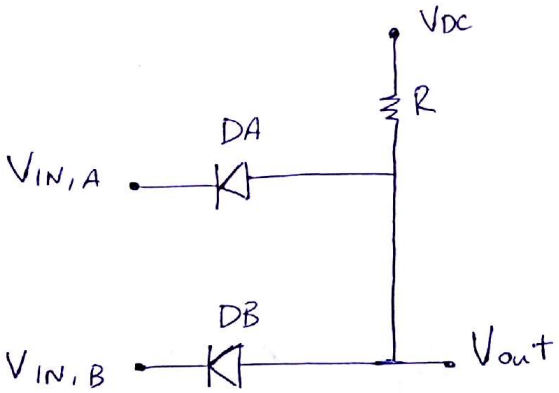
د.رولى طوالبه

21/9/2016

DIGITAL ELECTRONICS

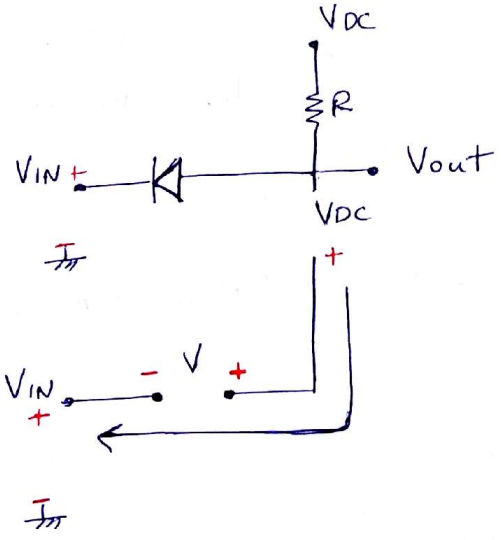
2.5 Diode - Resistor Logic

DIODE AND Gate



Logic 1 ≡ Logic H

Logic 0 ≡ Logic L



$V \geq V_{D(ON)} \rightarrow$ on

$V < V_{D(ON)} \rightarrow$ off

* By KVL :-

$$-V_{DC} + V + V_{IN} = 0$$

→ If $V \geq V_{D(ON)}$ then DIODE is ON

Any $V_{IN} \leq V_{DC} - V_{D(ON)}$ at least one diode is ON

$V_{out} = V_{D(ON)} + V_{IN}$

↳ low output because low input

$$I_R = \frac{V_{DC} - V_{out}}{R} = \frac{V_{DC} - V_D - V_{IN}}{R}$$

* Truth Table

A	B	o/p
L	L	L
L	H	L
H	L	L
H	H	H

⇒ AND GATE

→ If $V < V_{D(ON)}$ then DIODE is OFF

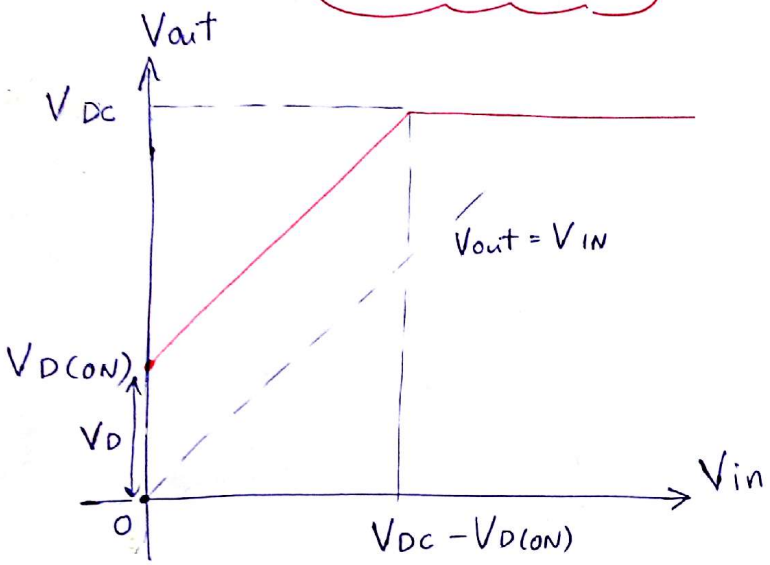
$V_{DC} - V_{IN} < V_{D(ON)}$

Any $V_{IN} > V_{DC} - V_{D(ON)}$ ⇒ high input

$V_{out} = V_{DC}$ ⇒ high output

$I_R = 0$

AND VTC



$$\text{slope} = \frac{\Delta V_{out}}{\Delta V_{IN}}$$

$$= \frac{V_{DC} - V_D}{V_{DC} - V_D - 0}$$

$$= 1$$

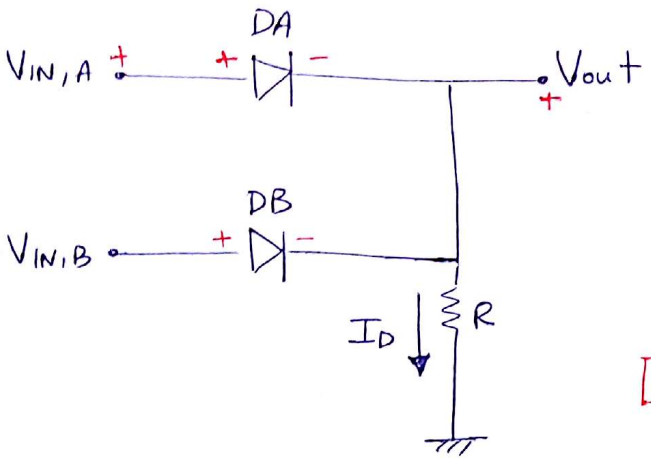
out ⇒ 3 letters like AND

$V_{out} = V_{D(ON)} + V_{IN}$

when diode is at $V_{IN} = 0$, $V_{out} = V_D$

at $V_{out} = V_{DC}$ → $V_{IN} = V_{DC} - V_{D(ON)}$

DIODE OR Gate



All $V_{IN} < V_{D(ON)} \Rightarrow$ Diodes OFF
↳ input low

- $I_R = 0$
- $V_{out} = 0$ ∴ output low

→ Any $V_{IN} \geq V_{D(ON)}$ corresponding diode is ON

* By KVL :-

$-V_{IN} + V_D + V_{out} = 0$

$V_{out} = V_{IN} - V_{D(ON)}$

$V_{out} = V_{IN} - V_{D(ON)}$

input high ⟶ output high

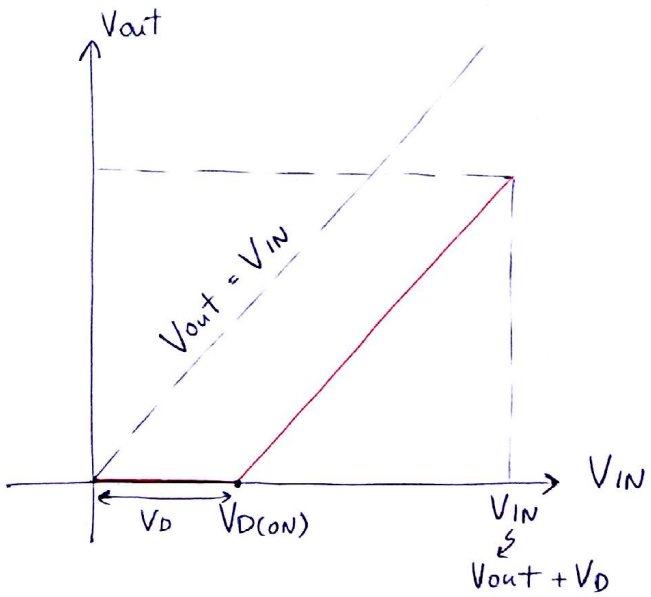
$I_R = \frac{V_{out}}{R} = \frac{V_{IN} - V_{D(ON)}}{R}$

* Truth Table **OR GATE**

A	B	o/p
L	L	L
L	H	H
H	L	H
H	H	H

IN ⇒ 2 letters like OR

OR VTC



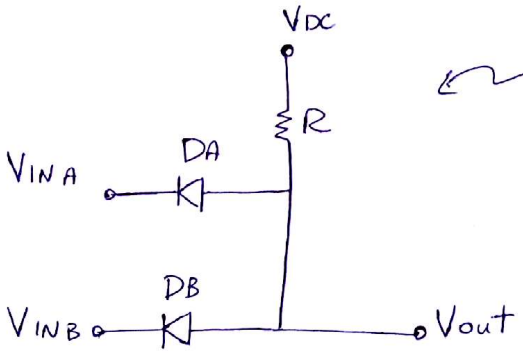
$V_{out} = V_{IN} - V_{D(ON)}$

$slope = \frac{V_{out} - 0}{V_{out} + V_D - V_D} = 1$

26/9/2016 اثنين

DIGITAL ELECTRONICS

EX 2.3



Diode - Resistor AND gate

Show that DA is off if V_{INA} is 1 V higher than V_{INB}.

$V_{D(ON)} = 0.7$ V

SOLUTION

Assume DA is on

$V_{DA} = V_{out} - V_{INA}$ ... ①

$V_{DB} = V_{out} - V_{INB}$ ... ②

$V_{out} = 0.7 + V_{INA}$ ... ③

$\Rightarrow V_{DB} = 0.7 + V_{INA} - V_{INB}$ ... ④

By replacing $V_{INA} = 1 + V_{INB}$ in ④

$V_{DB} = 0.7 + 1 + \cancel{V_{INB}} - \cancel{V_{INB}} \Rightarrow V_{DB} = 1.7$ V inapplicable

↳ assumption wrong

Assume DB is on and check for DA

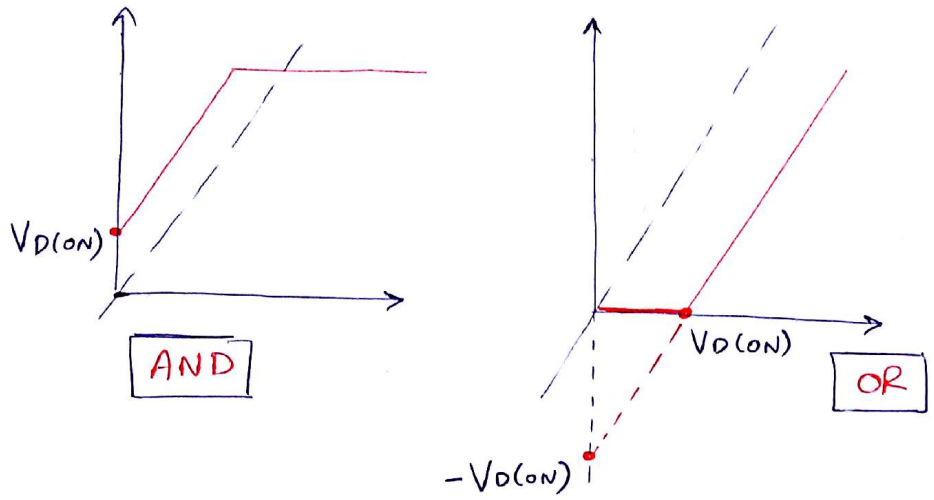
$V_{out} = V_{DB} + V_{INB} = 0.7 + V_{INB}$

$V_{DA} = 0.7 + V_{INB} - V_{INA}$

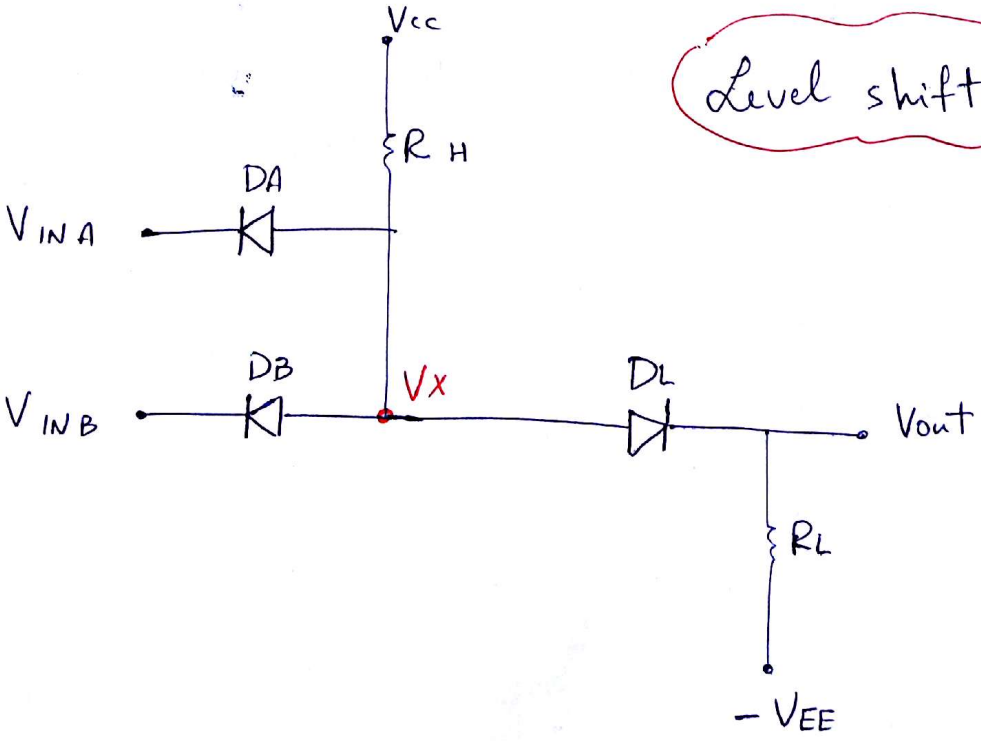
$V_{DA} = 0.7 + \cancel{V_{INA}} - 1 - \cancel{V_{INA}} \Rightarrow V_{DA} = -0.3$ V then DA off, DB on

assumption correct

2.6 Level Shifted DRL



Degradation :- increase or decrease in o/p voltage compared to i/p. To remove degradation a level shifted diode is added.



Level shifted AND Gate

① Any input low

$V_{IN} < V_X - V_D \Rightarrow$ corresponding diode is ON

1.a $V_{IN} < -V_{EE}$

$$V_X = V_{IN} + V_D$$

$V_{IN} + V_D < -V_{EE} + V_D$

$V_X < -V_{EE} + V_D$

D_L is off $\Rightarrow V_{out} = -V_{EE} = V_L$

1.b $V_{IN} > -V_{EE}$

$V_X > -V_{EE} + V_D$

D_L is on $\Rightarrow -V_{IN} - V_{D_{IN}(ON)} + V_{D_L(ON)} + V_{out} = 0$

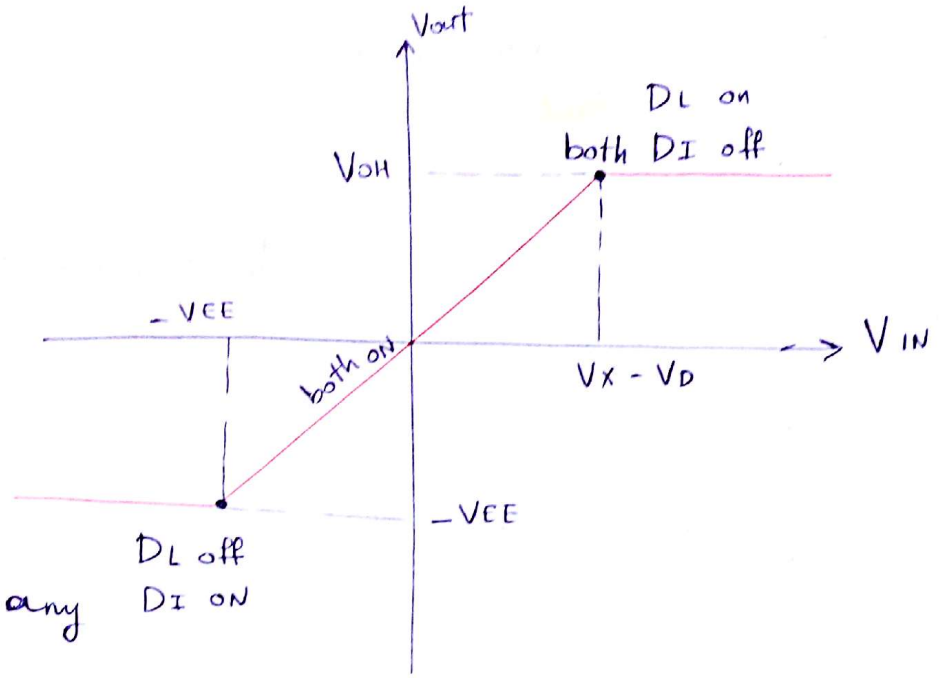
$V_{out} = V_{IN}$

② $V_{IN} > V_X - V_D \Rightarrow$ input diodes are both off

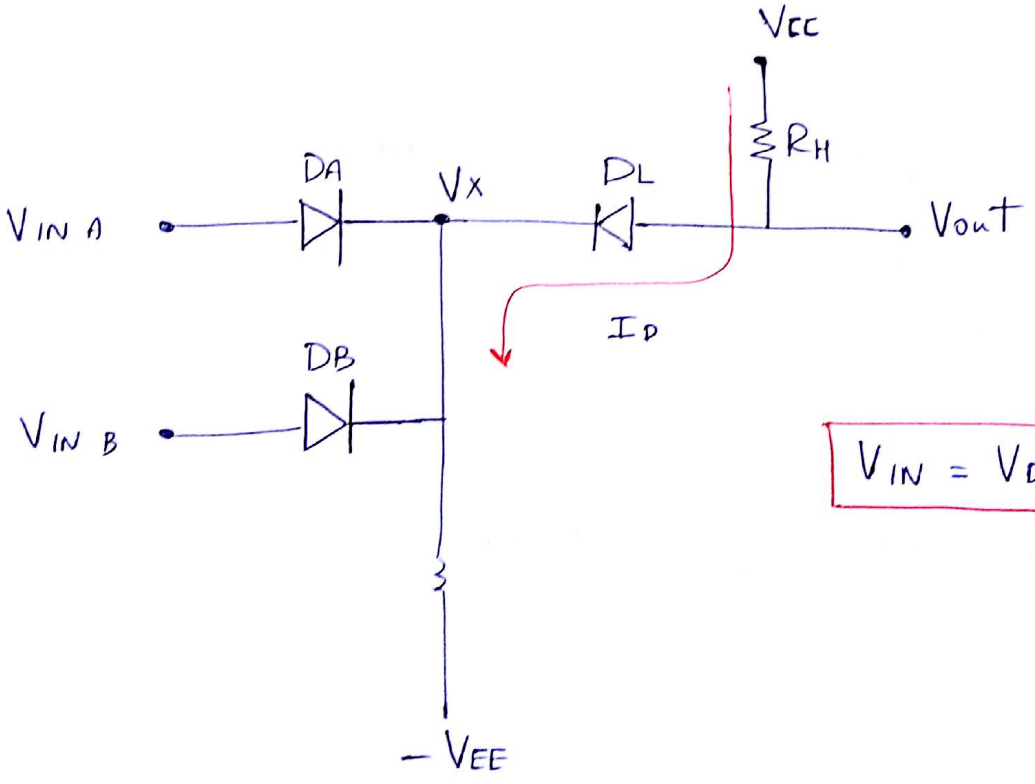
$$I_D = \frac{V_{CC} + V_{EE} - V_{D(ON)}}{R_L + R_H}$$

$V_{out} = V_{OH} = V_{CC} - I_D R_H - V_{DL(ON)}$

$= I_D R_L - V_{EE}$ independent of V_{IN}



Level Shifted OR Gate



$$V_{IN} = V_D + V_X$$

All inputs low

$V_{IN} < V_D + V_X \Rightarrow$ both diodes are off

$$I_D = \frac{V_{CC} + V_{EE} - V_{DL(ON)}}{R_H + R_L}$$

$$V_{out} = V_{OL} = V_{CC} - I_D R_H$$

$$= V_{DL(ON)} + I_D R_H - V_{EE} \Rightarrow \text{independent of input}$$

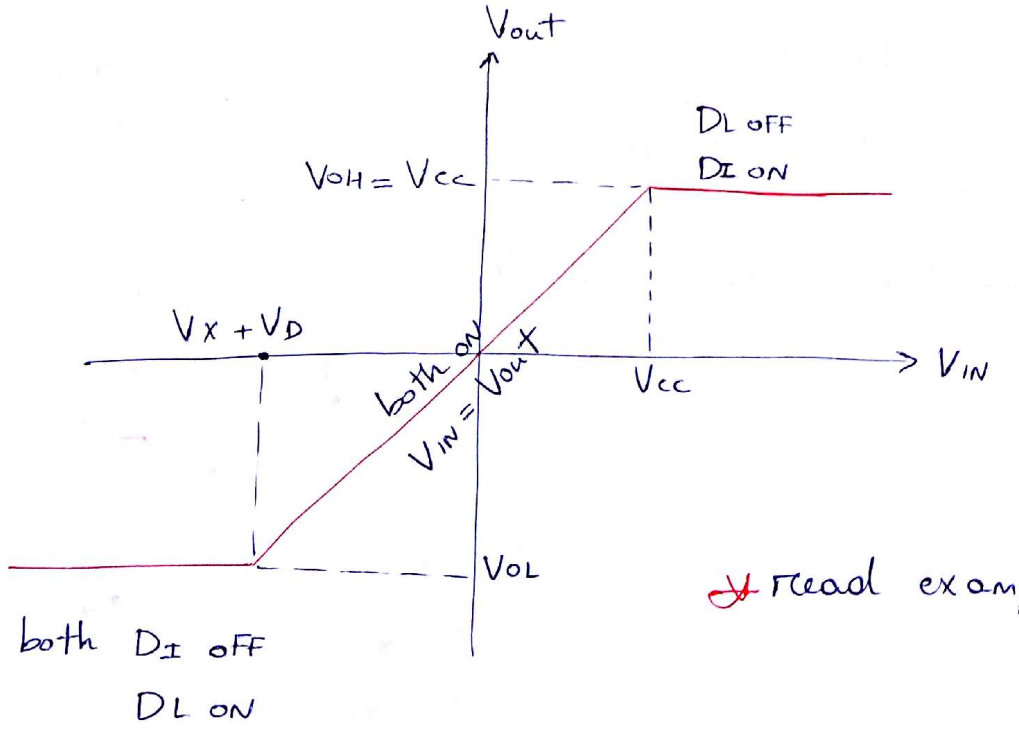
(2) At least one input $> V_X + V_D \rightarrow$ corresponding diode is ON

2.a $V_X < V_{CC} - V_{DL} \rightarrow$ DL is ON

$V_{out} = V_{IN}$

2.b $V_X > V_{CC} - V_{DL} \rightarrow$ DL is OFF

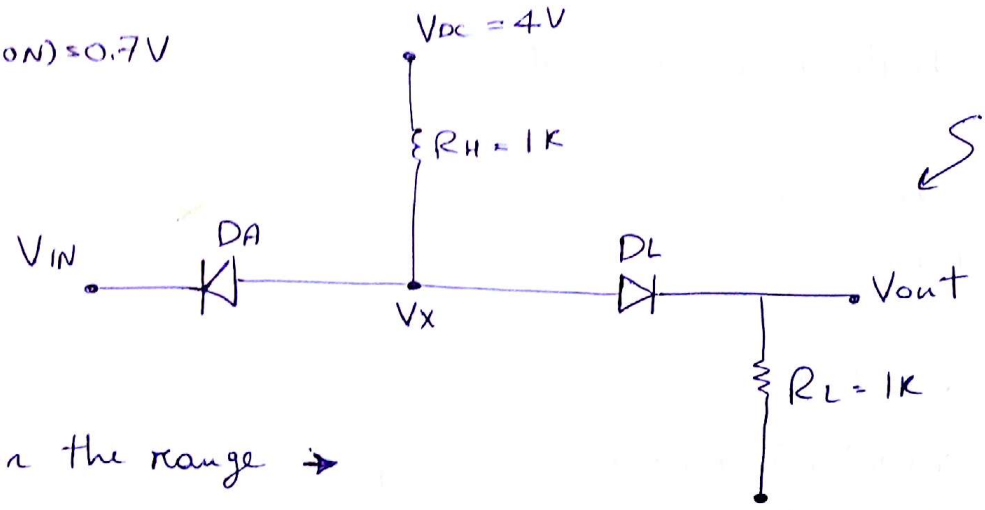
$V_{out} = V_{OH} = V_{CC}$



Read example 2.4

Problem 2.18 :-

$V_{D(ON)} = 0.7\,V$



For the range →

$-V_{DC} \le V_{IN} \le V_{DC}$ Draw VTC

Solution :-

① $V_{IN} < V_X - V_D \rightarrow$ DA ON

a. $V_X > V_{DL(ON)} - V_{DC} \rightarrow$ DL is ON ⇝ $V_{IN} > -V_{DC}$

$V_{out} = V_{IN}$

b. $V_X < V_{DL(ON)} - V_{DC} \rightarrow$ DL is OFF ← same as $V_{IN} < -V_{EE}$, $V_{IN} + V_D < -V_{EE} + V_D$, $V_X < -V_{EE} + V_D$

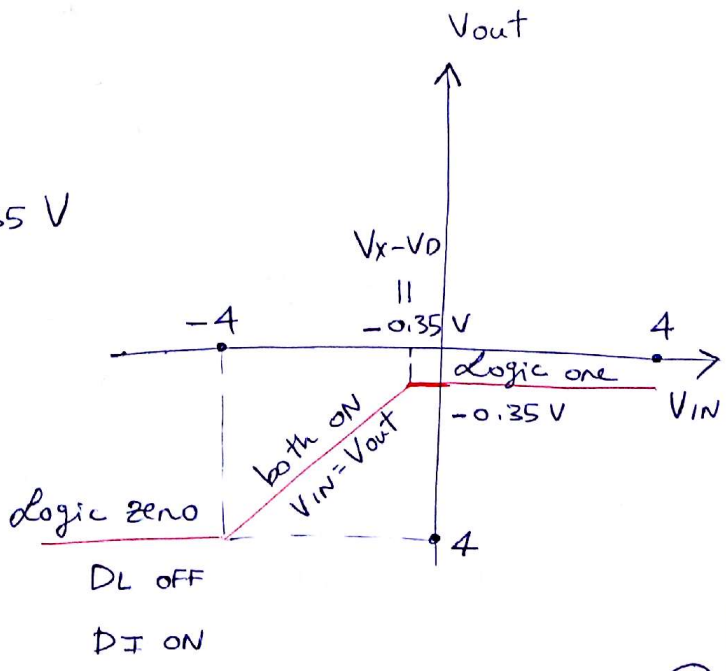
$V_{out} = -V_{DC} = V_X = -4\,V$

↳ $V_{IN} < -V_{DC}$

② $V_{IN} > V_X - V_D \rightarrow$ DA OFF

$$I_D = \frac{4 + 4 - 0.7}{2K} = 3.65\,mA$$

$V_{out} = V_{OH} = I_D R_L - V_{DC} = -0.35\,V$



DIGITAL ELECTRONICS

2.7 clamping diodes
2.8 level shifting diodes } داخلين بالامتحان

CH.4 Introduction to Bipolar Digital Circuits

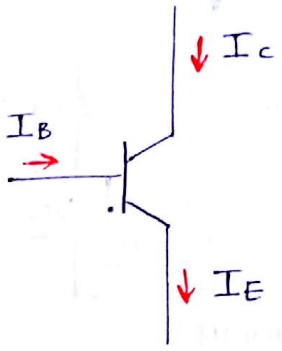
4.1 Analysis for BJT

1 Cut-off mode

B-E jun. → reverse biased

B-C jun. → reverse biased

$I_E = I_C = I_B = 0$



2 Forward active mode (FA)

B-E jun. → forward

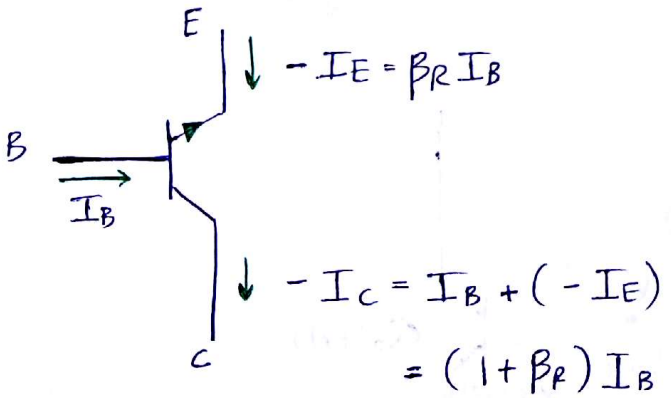
B-C jun. → reverse

$I_E = I_B + I_C = (\beta+1) I_B$

$I_C = \beta I_B$

$\Rightarrow V_{BC(RA)} = 0.7\,V$

3 Reverse active mode (RA)



B-E jun. → reverse

B-C jun. → forward

$\beta_R \ll \beta_F$

4 Saturation mode

B-C jun → forward biased

B-E jun → forward biased

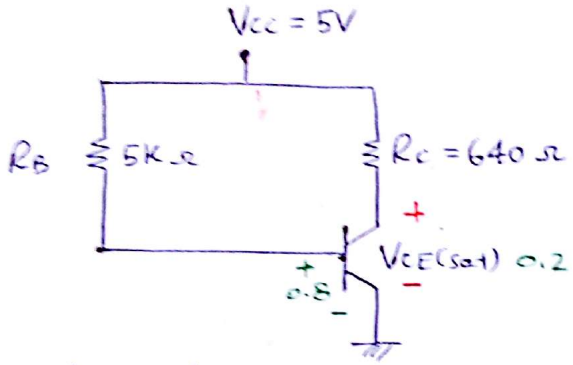
$I_C = \alpha\beta_F I_B$, $0 < \alpha < 1$

$I_E = I_B + I_C = (1+\alpha\beta_F) I_B$

NOTE:-

* If $I_B < 0$ → cut off
* If $I_B > 0$ → $V_{CE} < V_{CE(sat)}$ → sat
  → $V_{CE} > V_{CE(sat)}$ → FA

Ex 4.1



STANDARD VALUES

$V_{BE(sat)} = 0.8$	$V_{BE(FA)} = 0.7$
$V_{CE(sat)} = 0.2$	
$V_{BC(sat)} = 0.6$	$V_{BC(FA)} = 0.7$

Find α ? using $\beta_F = 65$

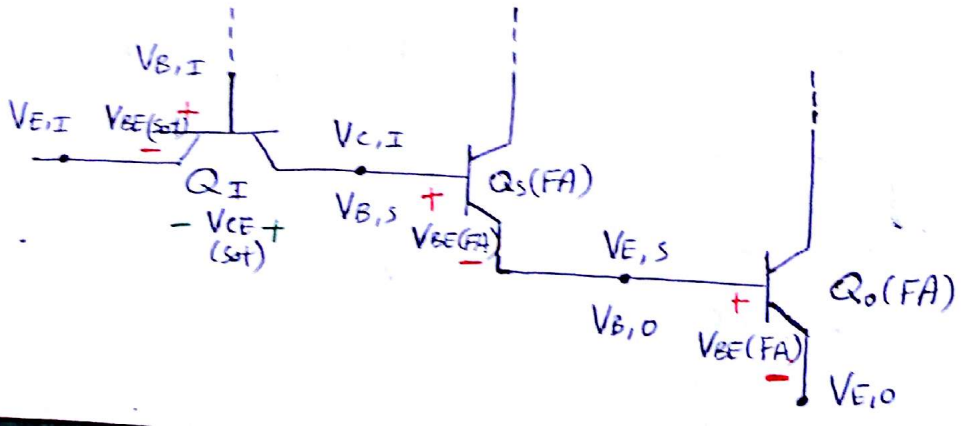
$$I_C = \frac{V_{cc} - V_{CE(sat)}}{R_c} = 7.5\,mA$$

$$I_B = \frac{5 - 0.8}{5k} = 840\,\mu A$$

$$\alpha = \frac{I_C}{\beta I_B} = 0.137$$

$V_{BE} = V_{BC} + V_{CE}$

Ex 4.2



Find voltage at each emitter and collector for all transistor

$V_{E,I} = -V_{CE,I(sat)} + 2V_{BE(FA)}$

$= 1.2V$

$V_{B,I} = V_{E,I} + V_{BE,I(sat)}$

$= 1.2 + 0.8 = 2V$

$V_{B,S} = V_{BE,S(FA)} + V_{BE,O(FA)}$

$= 1.4V$

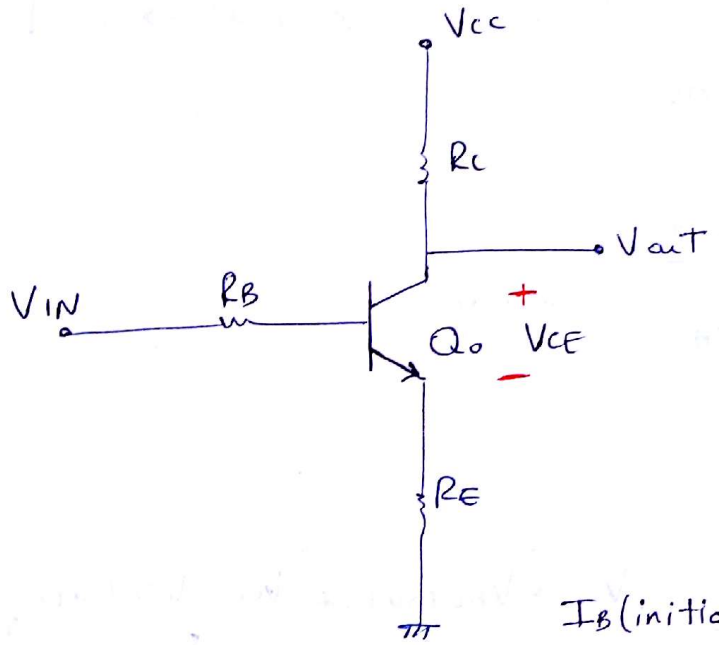
$V_{B,O} = V_{BE,O(FA)} = 0.7V$

$V_{E,O} = 0$

V_{IL} → from cut off to FA

V_{IH} → from FA to sat

4.2 BJT - Inverter



I_B (initially) = 0

① V_{OH} → Vout high

$V_{IN} < V_{BE(FA)}$

Q_0 is off

$I_{Rc} = 0$

$\boxed{V_{out} = V_{OH} = V_{cc}}$

② V_{IN} low (V_{IL})

input increases until Q_0 turns FA

at $\boxed{V_{BE(FA)} = V_{IL}}$

* V_{IL} → input @ which Q turns ON ③

As input increases I_B increases → I_C increases → V_{RC} increases

⇒ $V_{out} = V_{CC} - V_{RC}$ → decreases.

③ V_{out} low (V_{OL})

input increases until Q_0 saturates

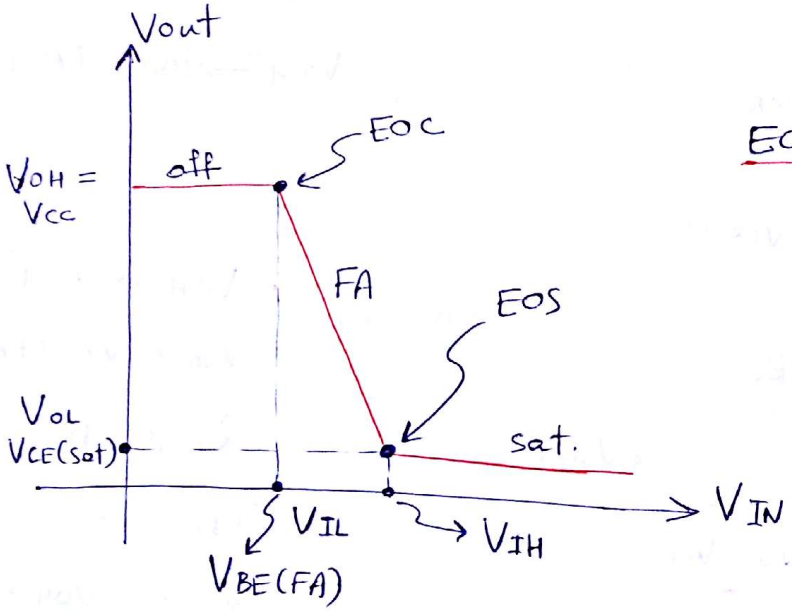
$$\boxed{V_{out} = V_{OL} = V_{CE(sat)}}$$

④ V_{IN} high (V_{IH})

Input at which Q_0 saturates

V_{OH}, V_{OL}, V_{IH}, V_{IL} : critical voltages

EOC : edge of conductance



EOS : edge of saturation

@ EOS → $\sigma = 1$

$$I_{C(EOS)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

$$I_B = \frac{I_C}{\beta_F} = \frac{V_{CC} - V_{CE(sat)}}{\beta_F R_C}$$

→

$$V_{IH} = V_{BE(sat)} + \frac{V_{CC} - V_{CE(sat)}}{\beta} * \frac{R_B}{R_C}$$

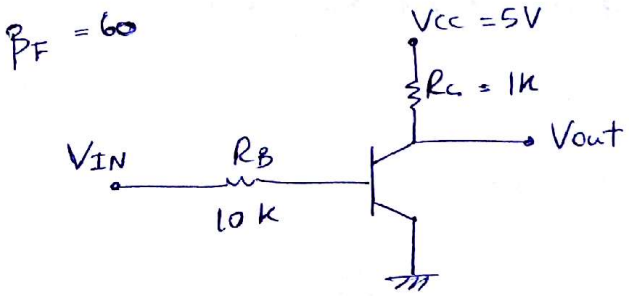
Noise Margins ✳

Safety margins for high and low voltage levels

$V_{HNM} = V_{OH} - V_{IH}$ (high noise margin) for logic 1

$V_{LNM} = V_{IL} - V_{OL}$ (low noise margin) for logic 0

ex 4.4



$V_{IL} = 0.7$

$V_{OL} = 0.2$

$V_{OH} = 5V$

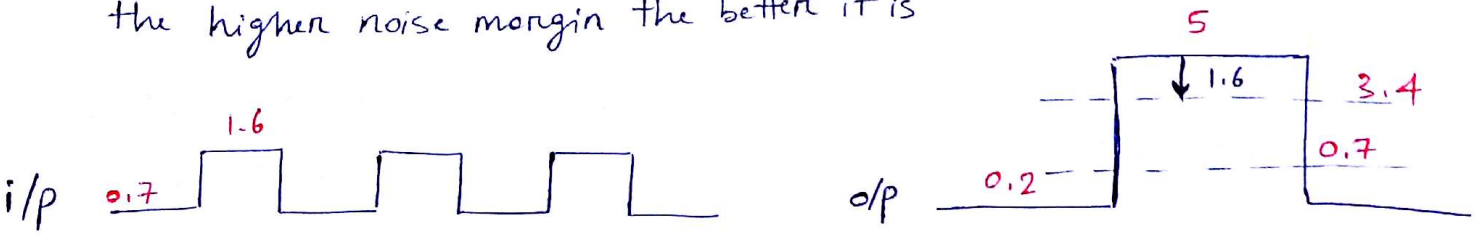
$V_{IH} = 1.6\ V$

$HNM = 5 - 1.6 = 3.4$

$LNM = 0.7 - 0.2 = 0.5$

↳ is small not practical

the higher noise margin the better it is



⇒ @ high-state output of Q_0 can't be smaller than V_{IH} so that the transistor of the next stage is able to saturate

4.3 TTC cct block diagram

4.4 Level shifting BJTs

4.5 Discharging Paths & Base driving circuits

⇒ Fan-out & Fan-in

- **Fan-out** :- is the max number of load gates that can be connected to the o/p of a driver
- **Fan-in** :- is the number of inputs allowed at one gate.

DIGITAL ELECTRONICS

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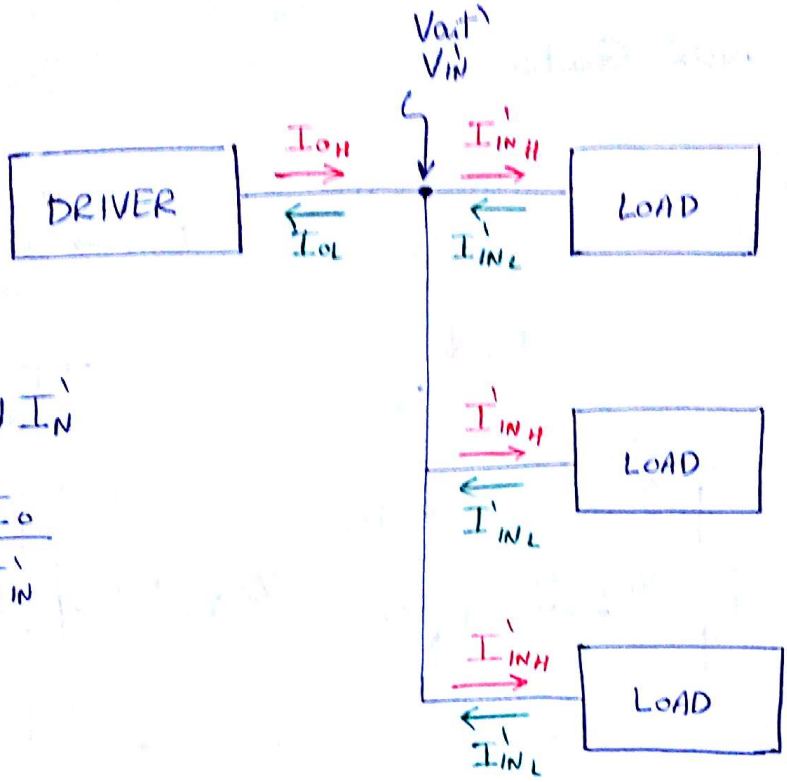
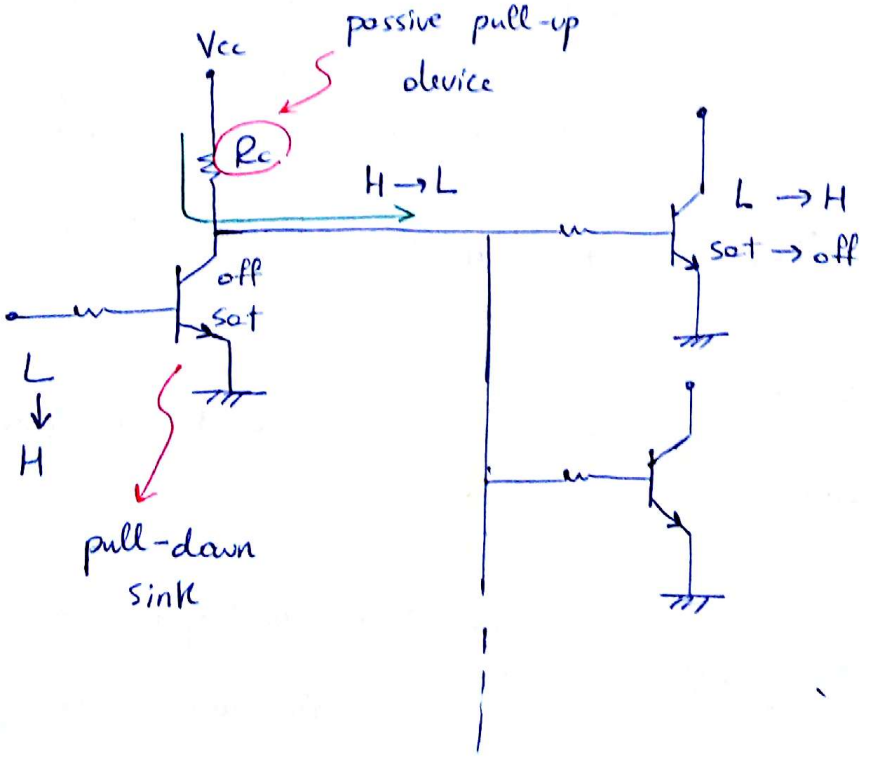


$$I_o = N I'_N$$

$$N = \frac{I_o}{I'_{IN}}$$

Fan-out



NOTE :-

At logic 1

$$N_{high} = \frac{I_{out(high)}}{I'_{IN}(high)}$$

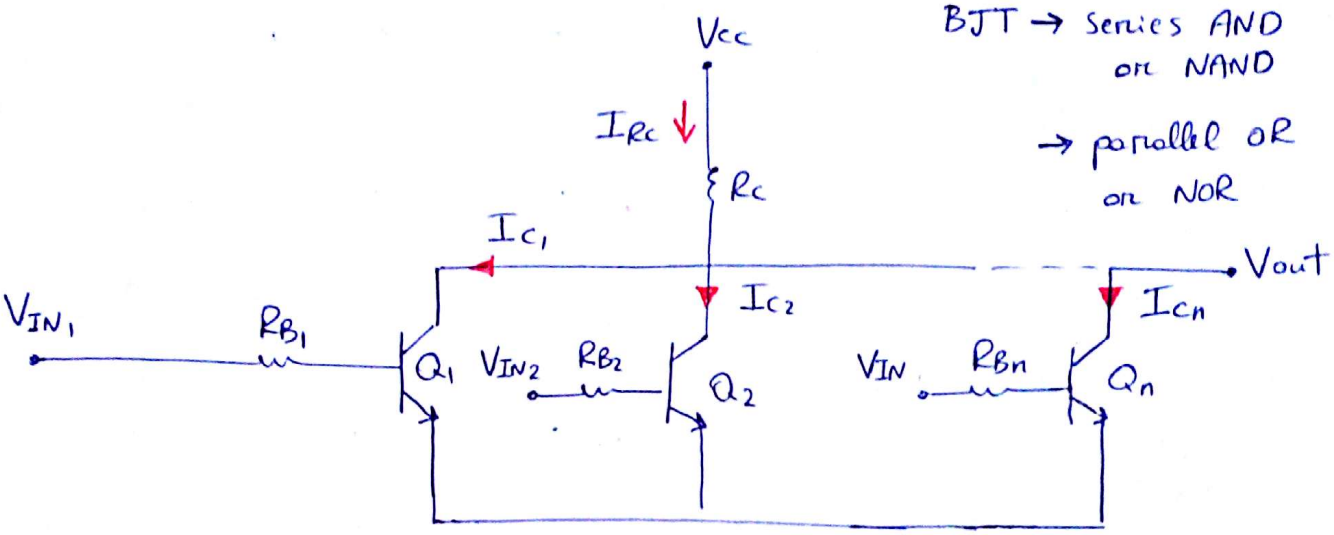
At logic 0

$$N_{low} = \frac{I_{out(low)}}{I'_{IN}(low)}$$

CHAPTER 5 Resistor Transistor Logic RTL

5.2 Basic RTL NOR Gate

NOTE :-
BJT → Series AND or NAND
→ parallel OR or NOR



In general :-

$$I_{Rc} = \sum_{i=1}^{n} I_{c,i} = I_{c_1} + I_{c_2} + \dots + I_{c_N}$$

$$V_{out} = V_{cc} - I_{Rc} R_c$$

(1) If all inputs are low

All BJTs are off

$I_{Rc} = 0$

$V_{out} = V_{OH} = V_{cc}$

③ Any input low or all inputs low

Both transistors are off

$I_{R_C} = 0$

$V_{out} = V_{CC} = V_{OH}$

NOTE!-

لل FAN-IN بال
محدودة بعدد trans.
$V_{CE(sat)}$ حسب قيمة

$\sum V_{CE(sat)} < V_{BE(FA)}$

② All inputs high

$V_{IN_1} = V_{IH}$

Q_1 is saturating

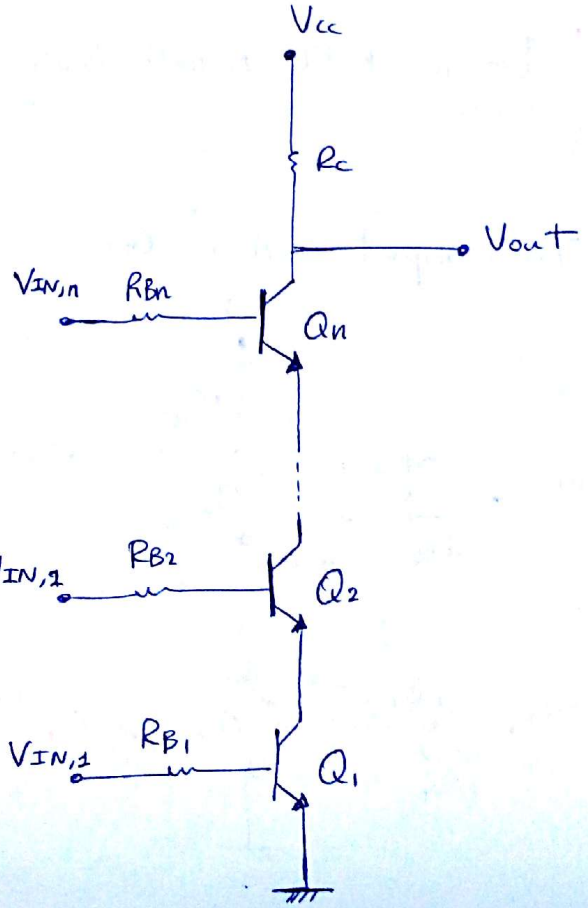
for Q_2 to turn FA

$V_{IL_2} = V_{BE_2}(FA) + V_{CE_1}(sat)$

for Q_2 & Q_1 saturating

$V_{out} = V_{OL} = 2V_{CE(sat)}$

IN_1	IN_2	Vout
0	0	1
0	1	1
1	0	1
1	1	0



⇒ Multi-input NAND Gate

① Any input low → BJT off

$V_{out} = V_{OH} = V_{CC}$

② All inputs high

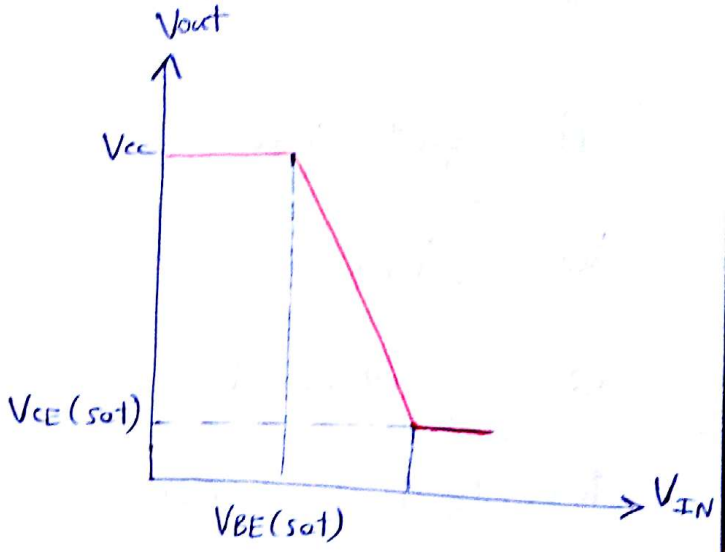
→ BJTs saturate

$V_{out} = n V_{CE(sat)}$

② Any or all inputs high corresponding BJT is saturating

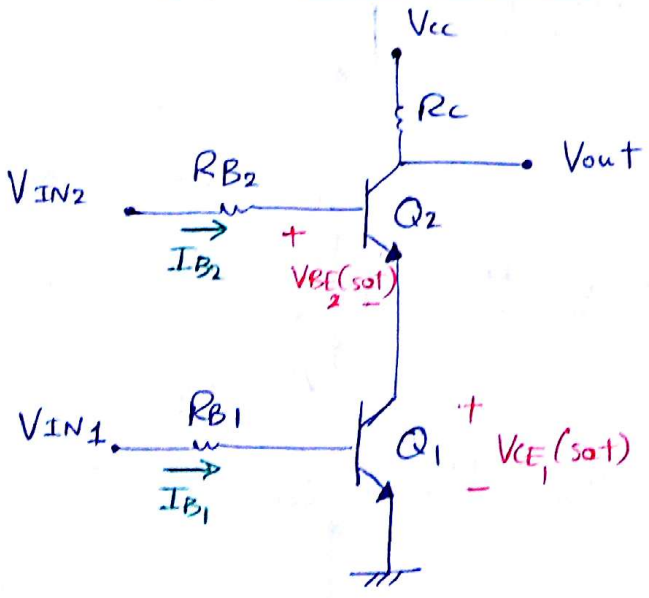
✱ Logic Table ✱

IN_1	IN_2	IN_3	IN_4	V_{out}
0	0	0	0	1
0	0	0	1	0
0	0	1	1	0
0	1	1	1	0
1	1	1	1	0



5.3 Basic RTL NAND Gate

⇒ Two inputs NAND Gate



In general :-

$V_{out} = V_{cc} - I_{Rc} R_c$

For simplicity ignore $I_{B(FA)}$

$I_{Rc} = I_{C1} \approx I_{E1} = I_{C2} \approx I_{E2}$

ample 5.7 Find max FAN-IN for RTL NAND Gate if

$V_{CE(sat)} = 0.17\ V$, $V_{BE(FA)} = 0.7\ V$

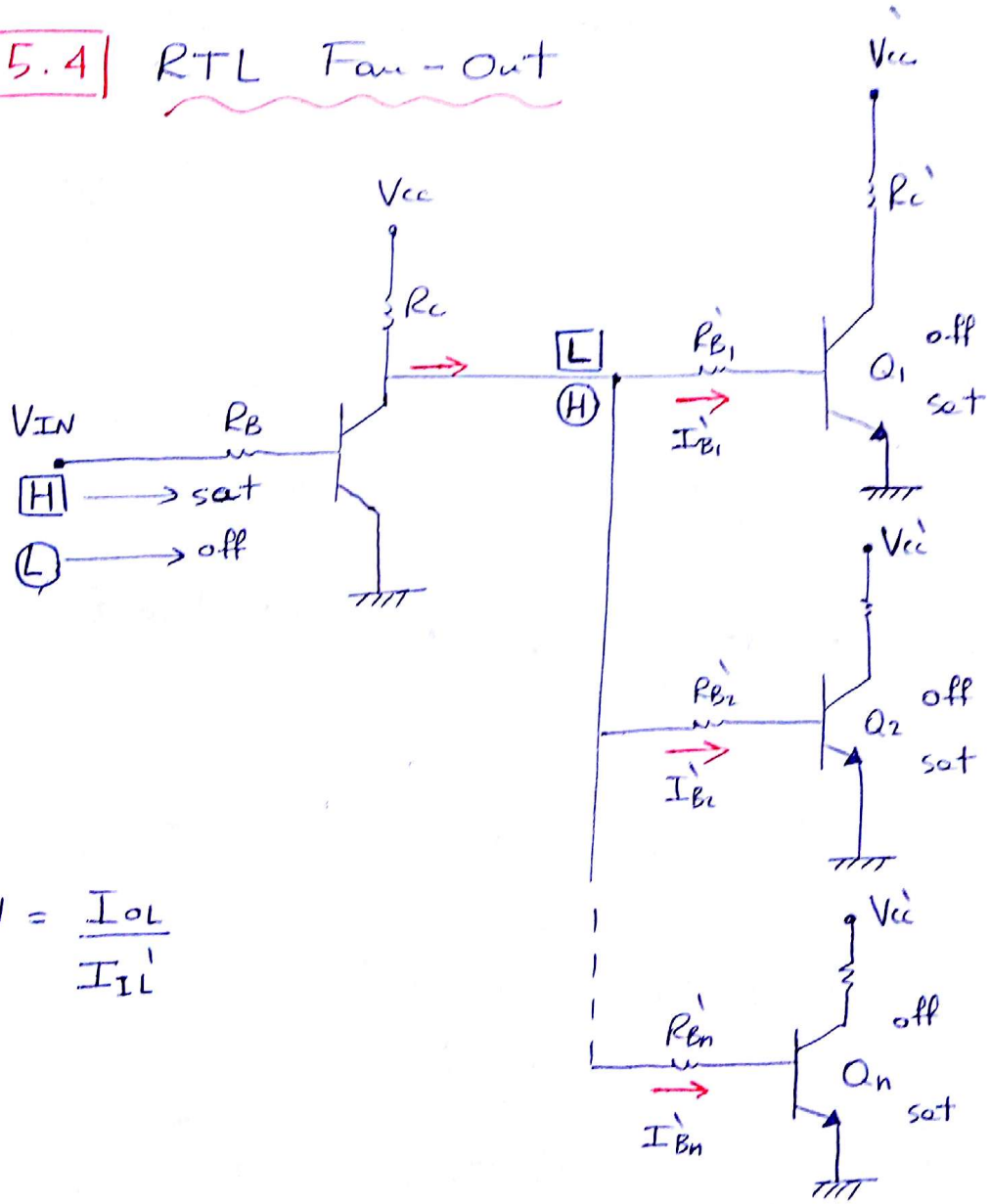
$\Rightarrow n V_{CE(sat)} < V_{BE(FA)}$

$n(0.17) < 0.7$

$n < \frac{0.7}{0.17} = 4.12$

$n = 4$

5.4 RTL Fan-Out



$N = \frac{I_{OL}}{I_{IL}}$

① When o/p of driver is low; load gate is off ⇒ no input current at load and Fan-out can't be calculated

② When o/p of driver is high, load transistors saturate and current flows through R_B's

⇒ o/p high is used to find Fan-out for RTL inverter

⇒ current supplied through R_C, must be enough to saturate all load gate BJTs ⇝ no. of load gate are limited

③ To assure the saturation of load BJTs

$$V_{OH} = V_{IH}'$$

$$= I_B' R_B' + V_{BE}'(sat)$$

$$= \frac{I_C'}{\beta} R_B' + V_{BE}'(sat)$$

$$= \frac{V_{CC}' - V_{CE}'(sat)}{\beta R_C'} R_B' + V_{BE}'(sat) \quad \ldots ①$$

$\alpha = 1$ @ EOS

$$I_{RC} = \frac{V_{CC} - V_{OH}}{R_C} \longrightarrow V_{OH} \text{ from eq. } ①$$

Load gates identical $\Rightarrow I_{RB}' = \frac{V_{OH} - V_{BE}'(sat)}{R_B'}$

$$N = \frac{I_{RC}}{I_{RB}'} = \frac{V_{CC} - V_{OH}}{R_C} * \frac{R_B'}{V_{OH} - V_{BE}'(sat)} = \frac{V_{CC} - V_{OH}}{V_{OH} - V_{BE}'(sat)} * \frac{R_B'}{R_C}$$

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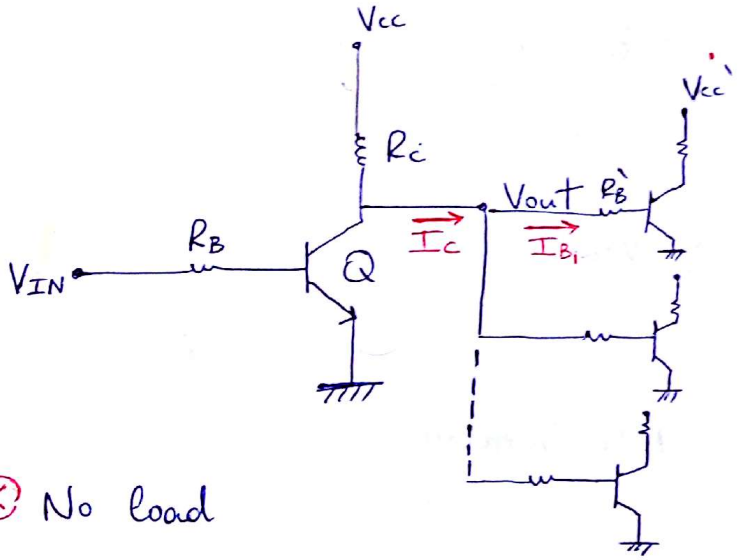
$$\text{Fan-out} \rightarrow N = \frac{V_{cc} - V_{out}}{V_{out} - V_{BE(sat)}} \frac{R_B}{R_c}$$

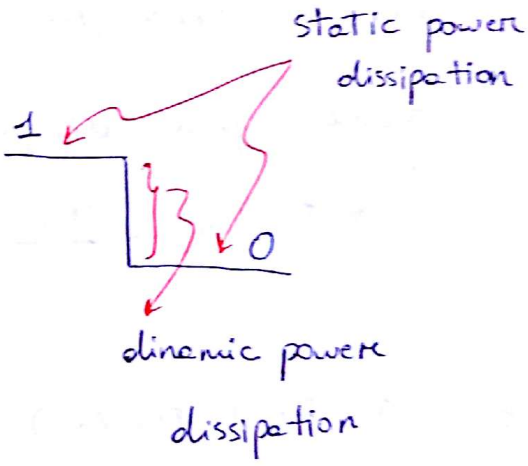
ex 5.2 from the book → Find N

$V_{out} = V'_{IH}$

$N = 12$

5.5 RTL Power Dissipation





✳ No load

OH $P_{cc(OH)}$

$P_{cc} = I_{cc} V_{cc}$

when input is low

Q is off

$I_{cc} = I_{RC} = 0$

$P_{cc(OH)} = 0$

✳ With load

OH $P_{cc(OH)}$

$$I_{cc} = I_{RC} = \sum_{i=1}^{N} I'_{B,i}$$

$$I_{RC} = N I'_B$$

$$= N \frac{V_{cc} - I_{RC} R_c - V'_{BE(sat)}}{R'_B}$$

eq. 1 $\Rightarrow$ $$I_{RC} = I_{cc(OH)} = \frac{V_{cc} - V'_{BE(sat)}}{R_c + \frac{R'_B}{N}} \quad (1)$$

$$I_{Rc} + \frac{N R_c I_{Rc}}{N} = \frac{V_{cc} - V_{BE}'(sat)}{R_B'}$$

$$I_{Rc}\left(1 + N\frac{R_c}{R_B'}\right) = \frac{V_{cc} - V_{BE}'(sat)}{R_B'}$$

$\Rightarrow$ eq. [1]

(X) **OL $P_{cc}(OL)$**

input high, Q sat

$V_{OL} = V_{CE}(sat)$

$I_{cc}(OL) = I_{Rc} = \frac{V_{cc} - V_{CE}(sat)}{R_C}$ (load & no load)

average power dissipation

↳ $P_{cc}(avg) = \frac{I_{cc}(OH) + I_{cc}(OL)}{2} V_{cc}$

ex 5.3 Find $P_{cc}(avg)$ for basic RTL inverter

① no load

② Fan-out = 1 ($N = 1$)

sol

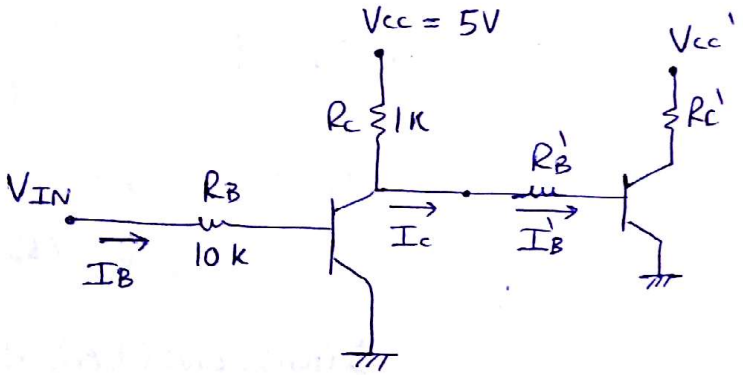
① $I_{cc}(OH) = 0$

$I_{cc}(OL) = \frac{V_{cc} - V_{CE}(sat)}{R_c}$

$= \frac{5 - 0.2}{1K} = 4.8\,mA$

$P_{cc}(avg) = \frac{0 + 4.8m}{2} * 5$

$= 12\,mW$



$\beta = 25$

common emitter

$N = 1$

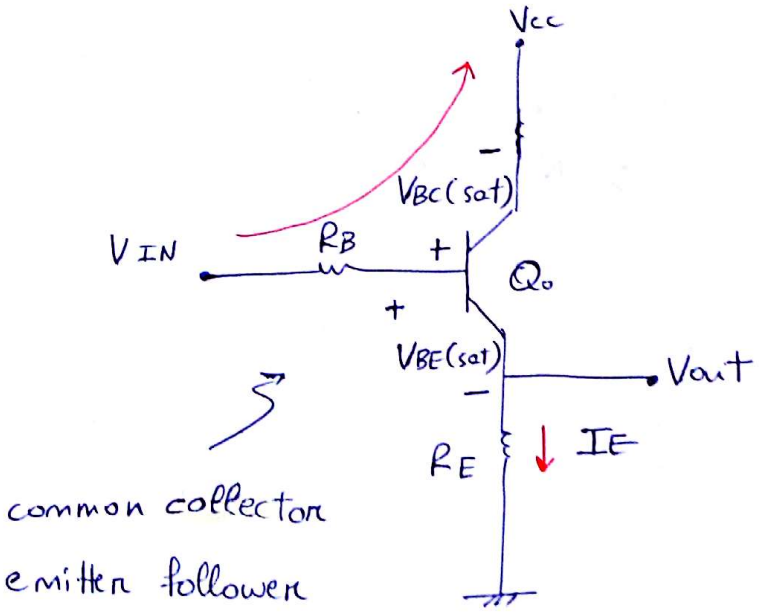
$$I_{cc(OH)} = \frac{V_{cc} - V'_{BE(sat)}}{R_c + \frac{R'_B}{N}} = \frac{5 - 0.8}{1K + \frac{10K}{1}} = 382\ \mu A$$

$$I_{cc(OL)} = 4.8\ mA$$

$$P_{cc(avg)} = \frac{4.8m + 0.382m}{2} * 5 = 12.96\ mW$$

when load ↑ ⇒ P_{cc} ↑

5.6 Basic RTL non-inverter



common collector emitter follower

$V_{out} = V_{cc} - V_{CE}$

$= I_E R_E$

✳ OL

when $V_{IN} < V_{BE(FA)}$

Q_o is off

$I_E = 0$

$V_{out} = 0 = V_{OL}$

✳ IL

At $V_{IN} = V_{IL}$

$= V_{BE(FA)}$

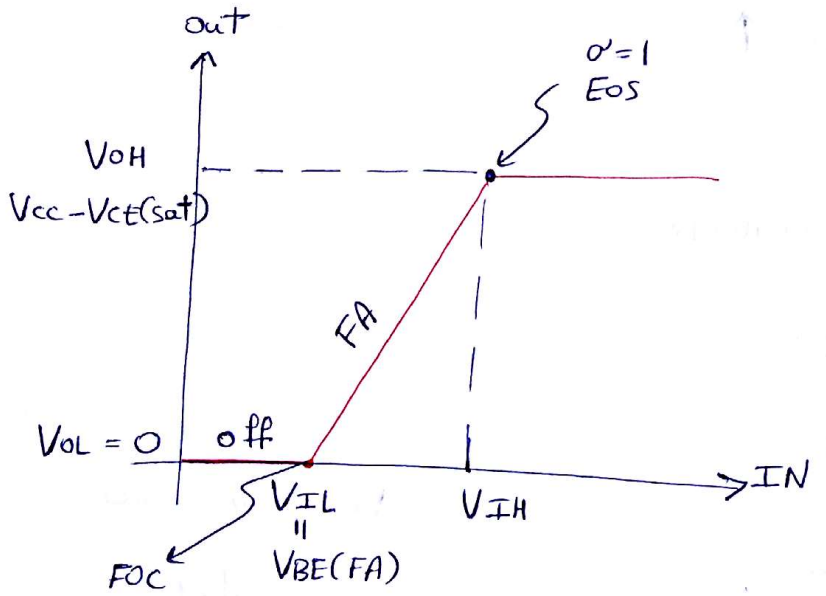
BJT turns on (FA)

✳ As input increases beyond $V_{IL} = V_{BE(FA)}$,

I_B & I_E increase $V_{out} = I_E R_E$ increases

✳ Input keeps increasing until Q saturates

$V_{out} = V_{OH} = V_{CC} - V_{CE(sat)}$



- V_{IH} when Q turns sat

$$I_E = \frac{V_{cc} - V_{CE(sat)}}{R_E}$$

$$I_{B(EOS)} = \frac{I_E}{\beta_F + 1}$$

$$-V_{IN} + I_B R_B + V_{BC(sat)} + V_{cc} = 0$$

$$V_{IN} = \frac{V_{cc} - V_{CE(sat)}}{\beta_F + 1} \frac{R_B}{R_E} + V_{BC(sat)} + V_{cc} = 0 \quad \dots \text{ eq. } [2]$$

$$V_{IN} > V_{cc}$$

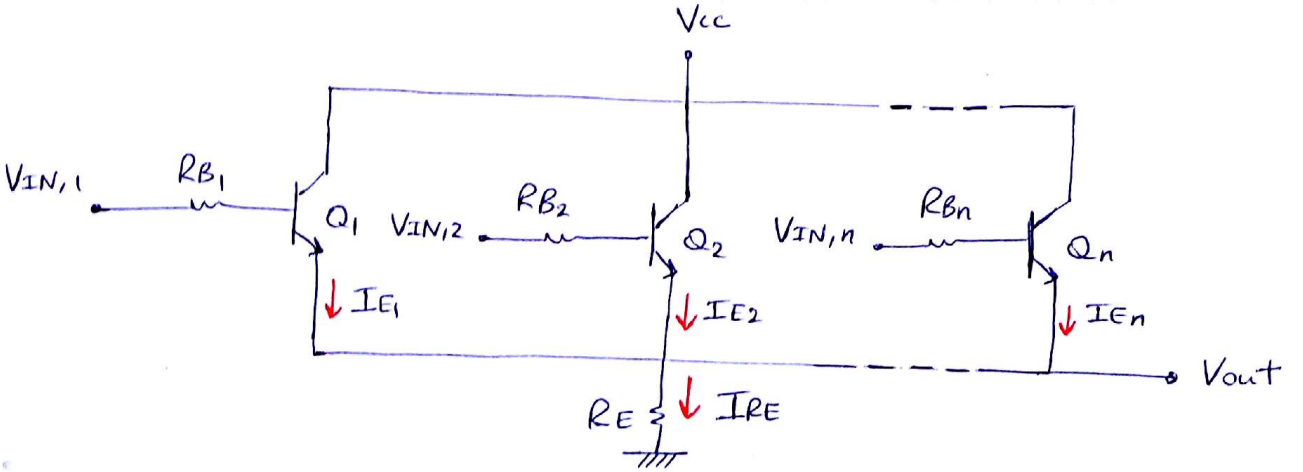
ex 5.4 $V_{cc} = 5V$, $R_B = 10k\Omega$, $R_E = 1K$, $\beta_F = 25$, $V_{OL} = 0$

$V_{IL} = 0.7$, $V_{OH} = 4.8\ V$, $V_{IH} = 7.4\ V > V_{cc}$ (from eq. [2])

Q saturates

$\rightarrow V_{out} = V_{OH} = V_{cc} - V_{CE(sat)}$

5.7 Basic RTL "OR" & "NOR"



In general

$$I_{RE} = I_{E_1} + I_{E_2} + \dots + I_{E_n}$$

$$V_{out} = I_E R_E$$

$$= V_{CC} - V_{CE}$$

IN_1	IN_2	IN_3	out
0	0	0	0
0	0	1	1
0	1	1	1
1	1	1	1

(1) All inputs low

All BJTs are low

$V_{out} = 0 = V_{OL}$

(2) Any or all inputs high

corresponding BJT saturates

$V_{out} = V_{CC} - V_{CE(sat)} = V_{OH}$

$$\Rightarrow I_B = \frac{I_E}{\beta_F + 1}$$

$$I_E = \frac{I_{RE}}{\#\text{ of saturating transistors}}$$

$$V_{IH} = I_B R_B + V_{BC(sat)} + V_{CC}$$

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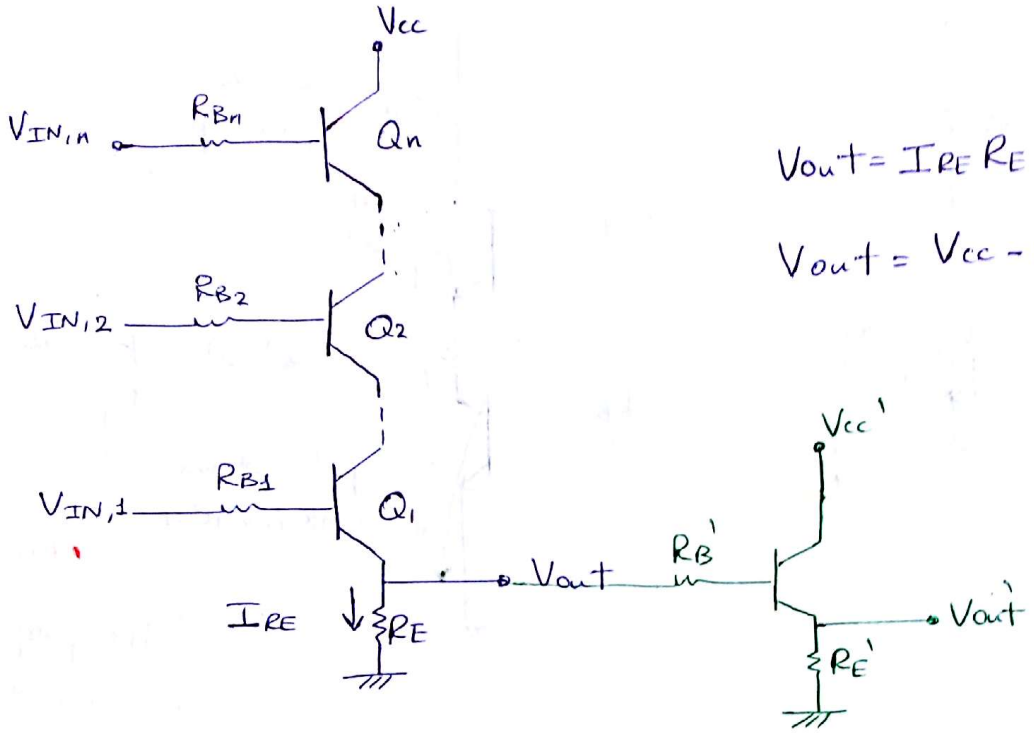
* AND Gate



$V_{out} = I_{RE} R_E$

$V_{out} = V_{cc} - n V_{CE}$

① Any or All inputs low

corresponding Q is off, also all other Q are off $I_{RE} = 0$

$V_{out} = 0 = V_{OL}$

IN_1	IN_2	Out
0	0	0
0	1	0
1	0	0
1	1	1

② Both inputs high

For a 2-input AND Gate

* when Q_2 is FA, Q_1 sat.

$V_{out} = V_{cc} - V_{CE,2}(FA) - V_{CE,1}(sat)$

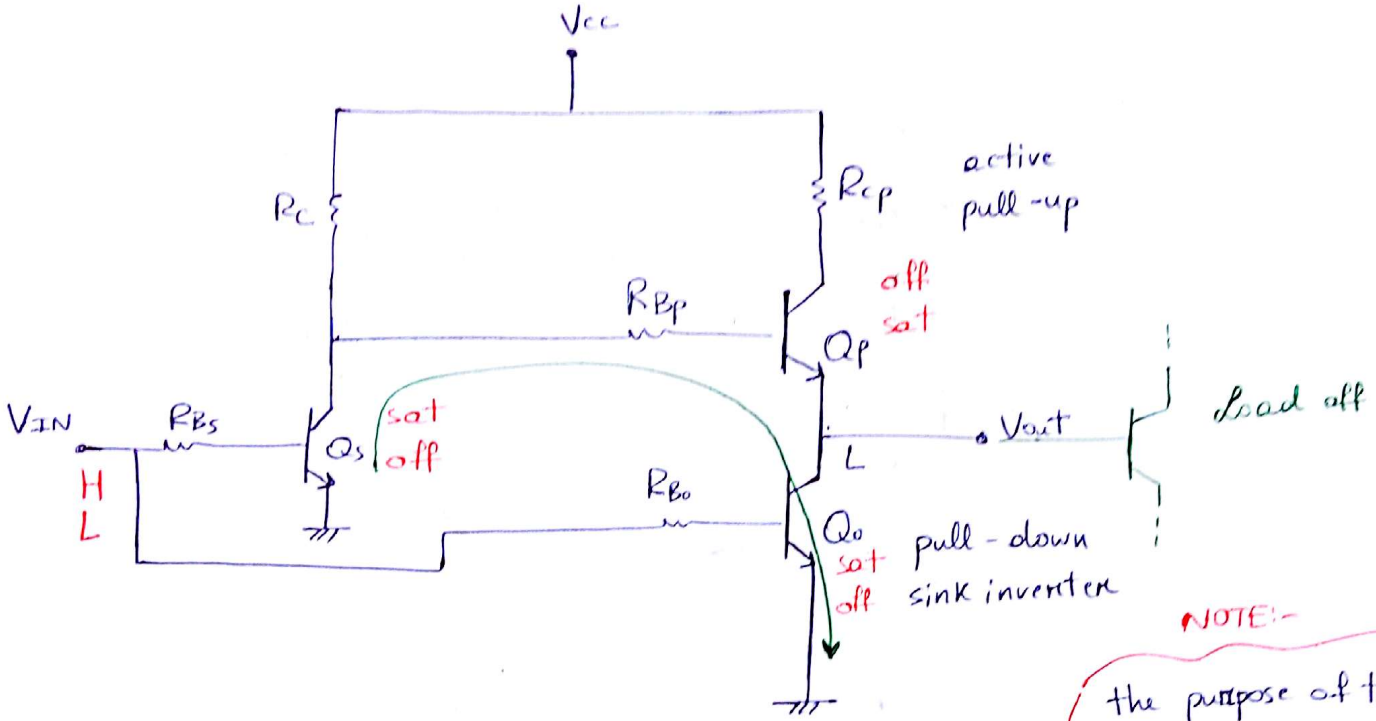
* when both saturate

$V_{out} = V_{cc} - 2 V_{CE}(sat)$

⇒ if for n-inputs all Qs saturate

$V_{OH} = V_{cc} - n V_{CE}(sat) \geq V_{IH}'$

5.8 RTL with active pull-up



NOTE:-
the purpose of this cct is to ↑ Io, so FAN-OUT ↑ too

why Qo is sink & Qs is not? for the exam

* $R_{cp} \approx 0.1 R_c$ for design

  ⇒ more sourcing current & high fan-out

* $R_{Bs} = R_{Bo} = R_B$

  and Qs & Qo operate at the same time

* if V_{IN} is high, Qs & Qo saturate

  $V_{out} = V_o = V_{CE,o}(sat)$

TEST Qp $\quad -V_{CE,s}(sat) + I_{Bp} R_{Bp} + V_{BE,p} + V_{CE,o}(sat) = 0$

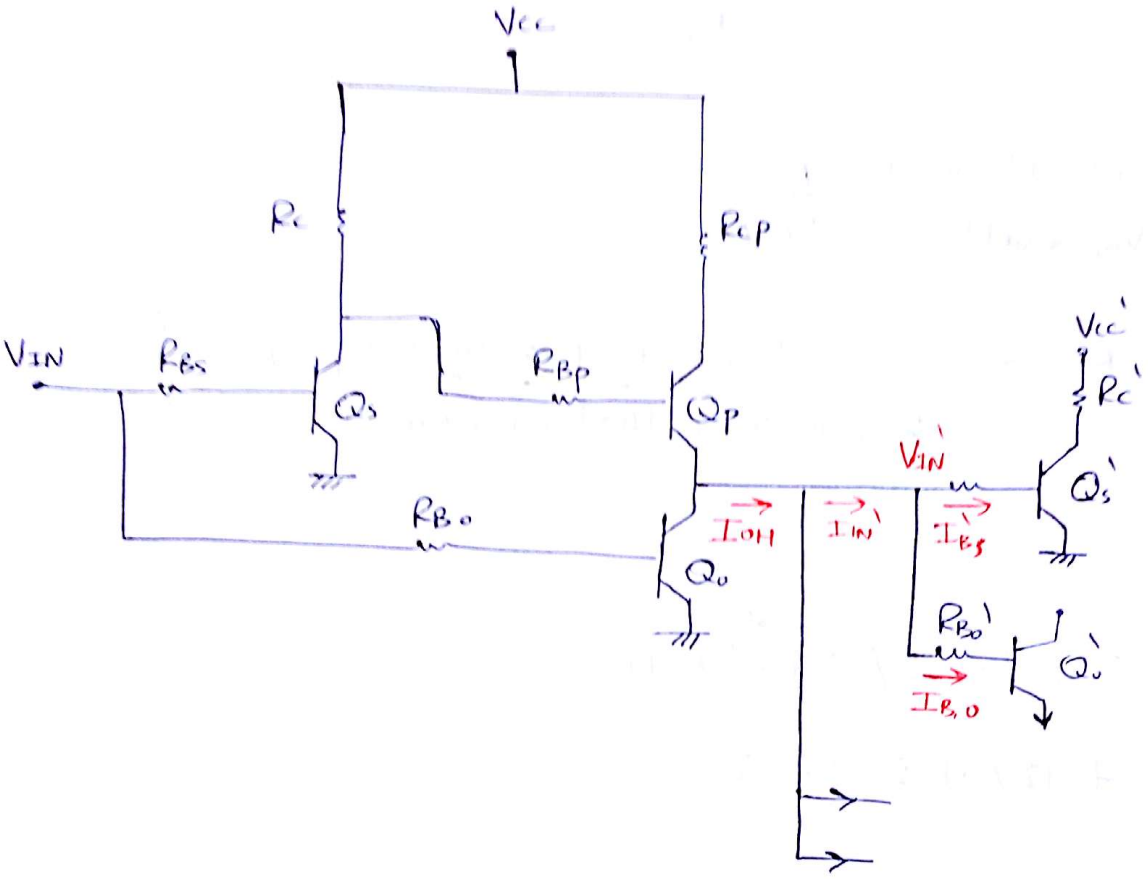
$$I_{Bp} = \frac{-V_{BE,p}}{R_{Bp}} \Rightarrow \text{negative} \Rightarrow Q_p \text{ off}$$

* if V_{IN} is low, $V_{IN} < V_{BE(FA)} \Rightarrow$ Qs & Qo are off

  $V_{out} = V_{OH} = V_{cc} - I_{cp} R_{cp} - V_{CE,p}(sat)$

~~fan-out~~

for low o/p at driven, load gates will be off and I'_{IH} will be zero ⇒ can't use for fan-out calculations.



* $V_{OH} = V'_{IH}$ to ensure saturation of load gates BJTs

$$V_{OH} = V'_{IH} = I'_B R'_B + V'_{BE}(sat)$$

$$= \frac{V'_{cc} - V'_{CE}(sat)}{\beta} \frac{R'_B}{R'_c} + V'_{BE}(sat)$$

for simplicity ignore I_{BP}.

$$I_{OH} = I_{E,P} \approx I_{C,P} = \frac{V_{cc} - V_{CE,P}(sat) - V_{OH}}{R_{cP}}$$

$$I'_{IH} = 2 I'_B$$

$$I_{OH} = 2N I_B' = N I_{IH}'$$

$$I_B' = \frac{V_{OH} - V_{BE}'(sat)}{R_B'}$$

$$\frac{V_{cc} - V_{CE,p}(sat) - V_{OH}}{R_{cp}} = 2N \frac{V_{OH} - V_{BE}'(sat)}{R_B'}$$

$$N = \frac{V_{cc} - V_{CE}(sat) - V_{out}}{V_{out} - V_{BE}'(sat)} \frac{R_B'}{2R_{cp}}$$

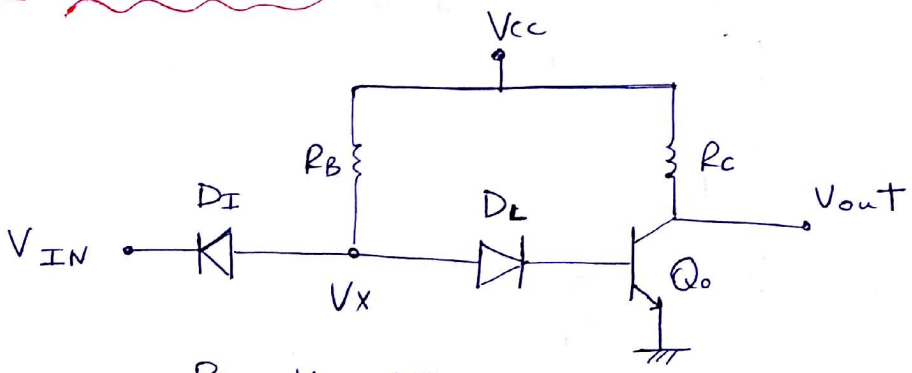
since $R_{cp} \ll R_c \Rightarrow$ fan-out for RTL with active pull is higher than that of basic RTL inverter

chap.5 ⇒ 5.11 / 5.32 / 5.40 / 5.17

chap 4 ⇒ 4.12 / 4.20 / 4.3

CHAPTER 6 Diode Transistor Logic (DTL)

6.1 Basic DTL



$$R_B = \frac{V_{cc} - V_X}{I_B}$$

for R_B design ⇒ V between V_{cc} & V_X must be < than V between V_X & V_{IN}

following analysis: $V_{IN} < V_X$

V_{OH} → $V_X = V_{DI}(on) + V_{IN} < V_{DL}(on) + V_{BE}(FA)$

$V_{IN} < V_{BE}(FA)$

Q_0 is off , $I_{RC} = 0$, $V_{OH} = V_{CC}$

D_L is off

V_{IL} → D_L & Q_0 are on

when $V_X = V_{IN} + V_{DI}(on) = V_{DL}(on) + V_{BE,0}(FA)$

$V_{IN} = V_{IL} = V_{BE}(FA)$

V_{OL} → as input increases, Q_0 saturates

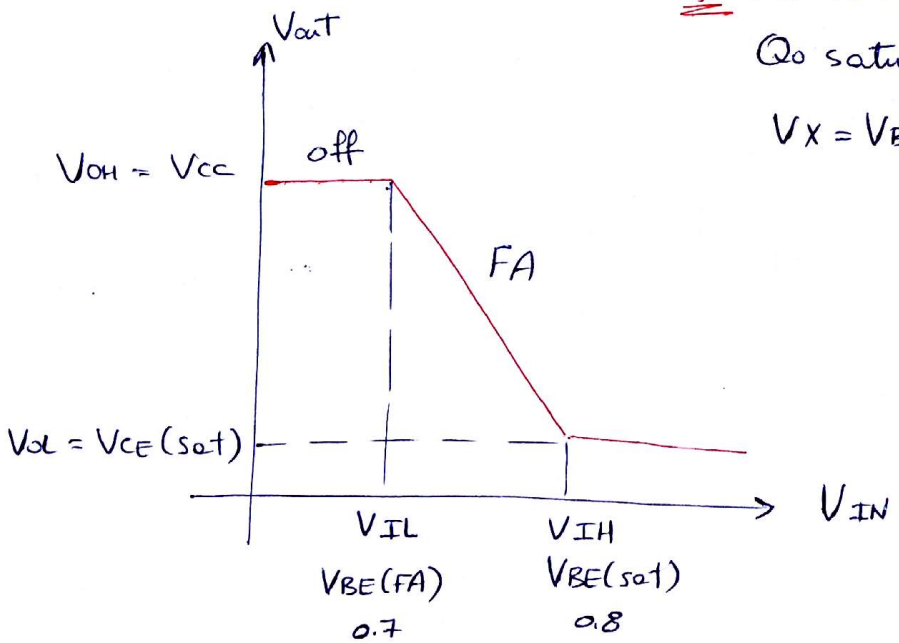
$V_{out} = V_{OL} = V_{CE,0}(sat)$

V_{IH} → $V_X = V_{IN} + V_{DI}(on) = V_{DL}(on) + V_{BE,0}(sat)$

$V_{IN} = V_{IH} = V_{BE}(sat)$

* R_B is choosen such that Q_0 saturates when

$V_X = V_{BE}(sat) + V_D(on)$



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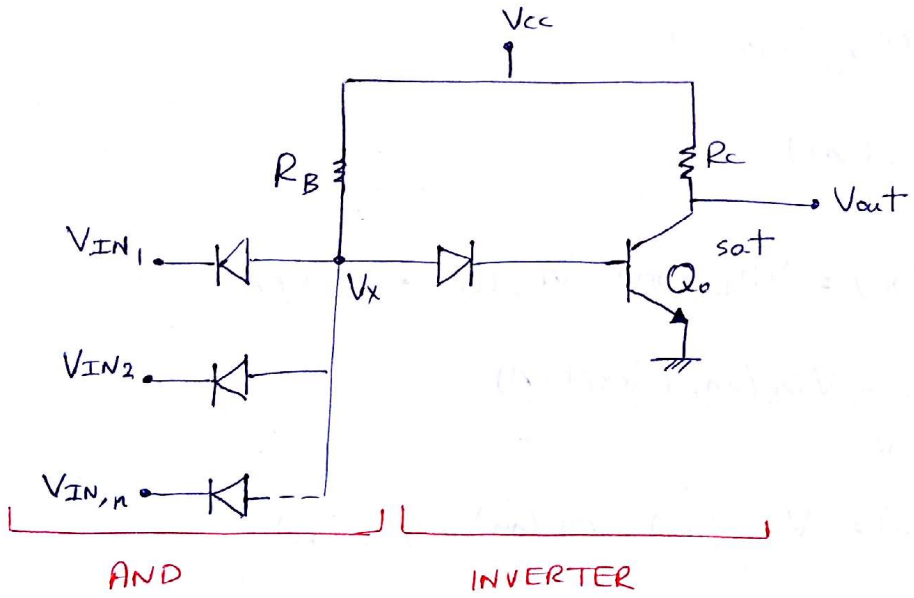
* For basic DTL

$HNM = V_{OH} - V_{IH} = 5 - 0.8 = 4.2\ V$ good margin

$V_{cc} = 5$, $V_{CE(sat)} = 0.2$

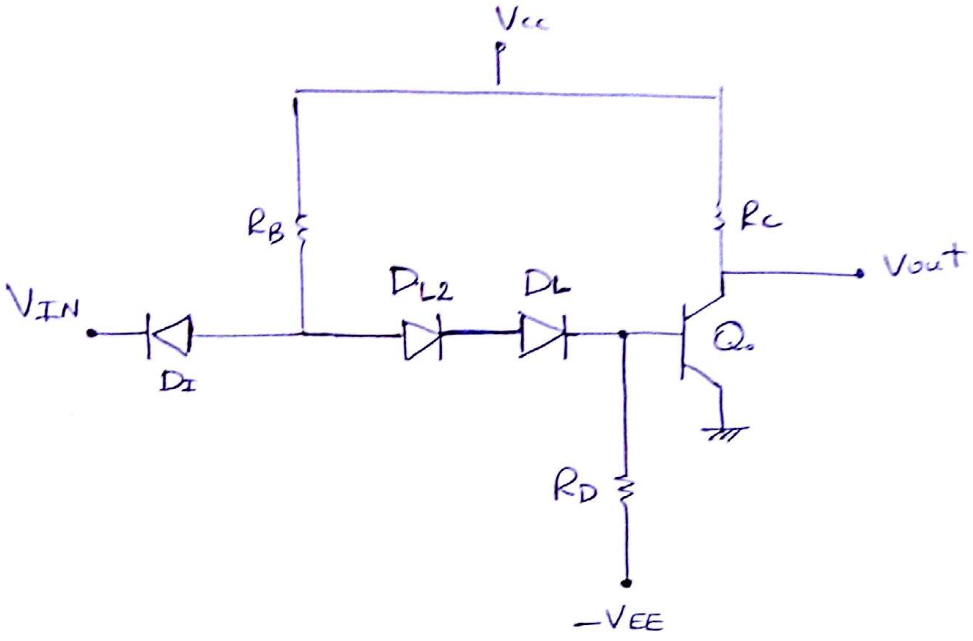
$LNM = V_{IL} - V_{OL} = 0.7 - 0.2 = 0.5\ V$ bad margin

* Basic DTL NAND Gate



L	L	H
L	H	H
H	L	H
H	H	L

6.2 Modified DTL ⇒ Additional level shifting



* Q_0 off $V_{OH} = V_{CC}$, $I_{Rc} = 0$

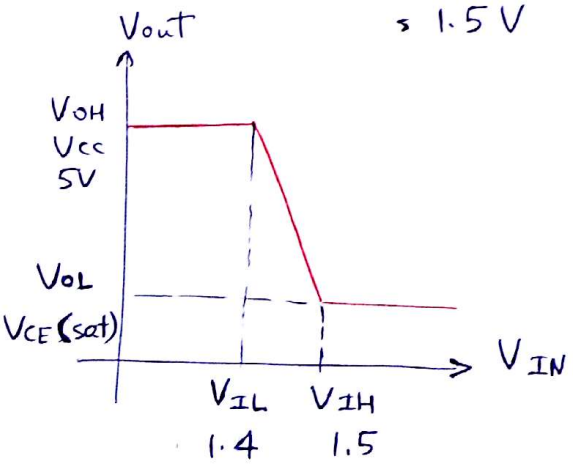
* Q_0 sat $V_{OL} = V_{CE(sat)}$

* $V_X = V_{IN} + V_{DI(on)} = V_{DL2(on)} + V_{DL(on)} + V_{BE(FA)}$

$$V_{IN} = V_{IL} = V_{DL(on)} + V_{BE(FA)}$$
$$= 1.4\,V$$

* $V_X = V_{IN} + V_{DI(on)} = V_{DL2(on)} + V_{DL(on)} + V_{BE(sat)}$

$$V_{IN} = V_{DL(on)} + V_{BE(sat)}$$
$$= 1.5\,V$$



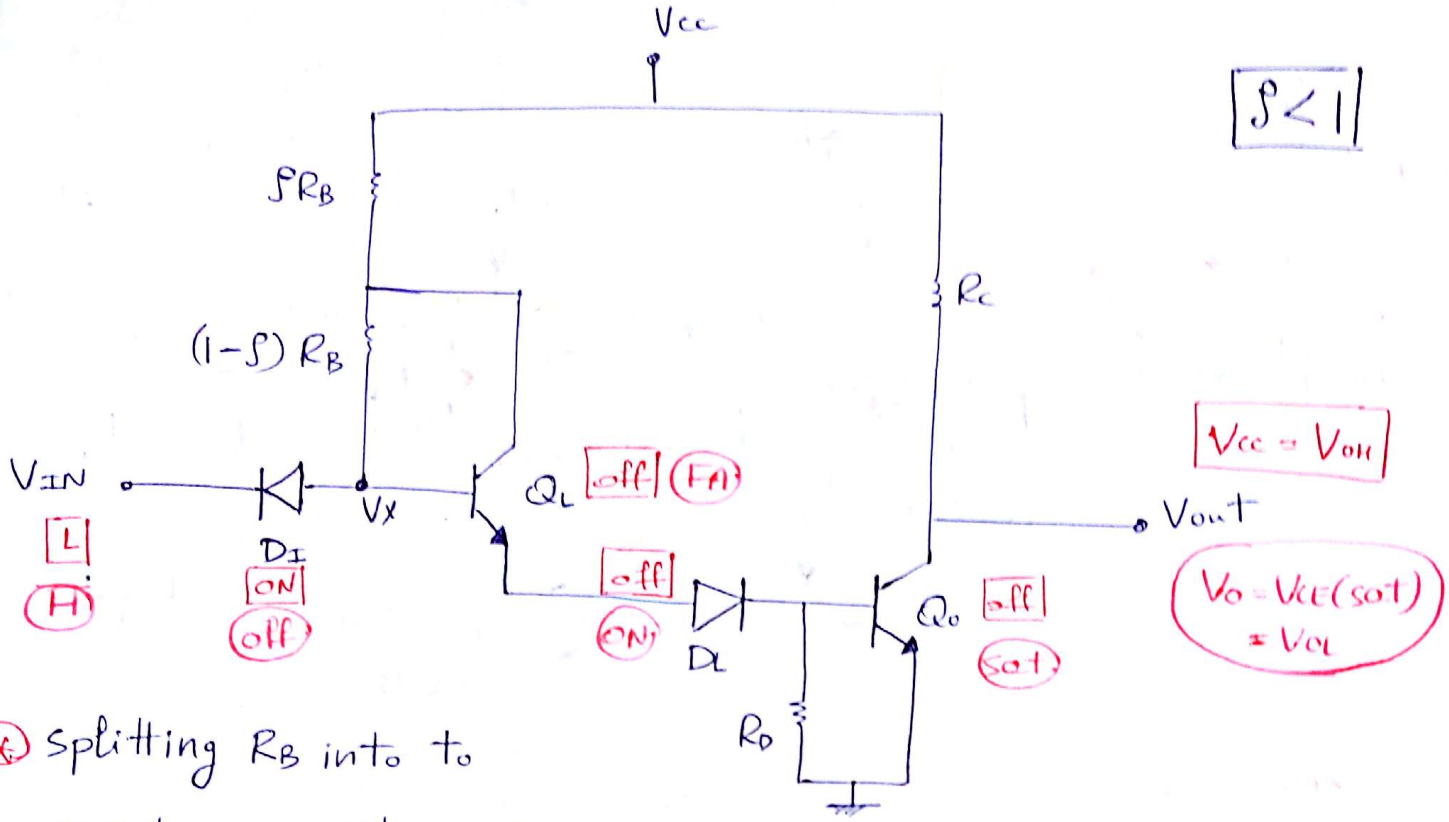
* the addition of a level shift diode, increases V_{IL} ⇒ LNM increased

* R_D & -VEE are used as discharge paths

→ HNM = 5 - 1.5 = 3.5V good.

→ LNM = 1.4 - 0.2 = 1.2V

6.3 Transistor Modified DTL

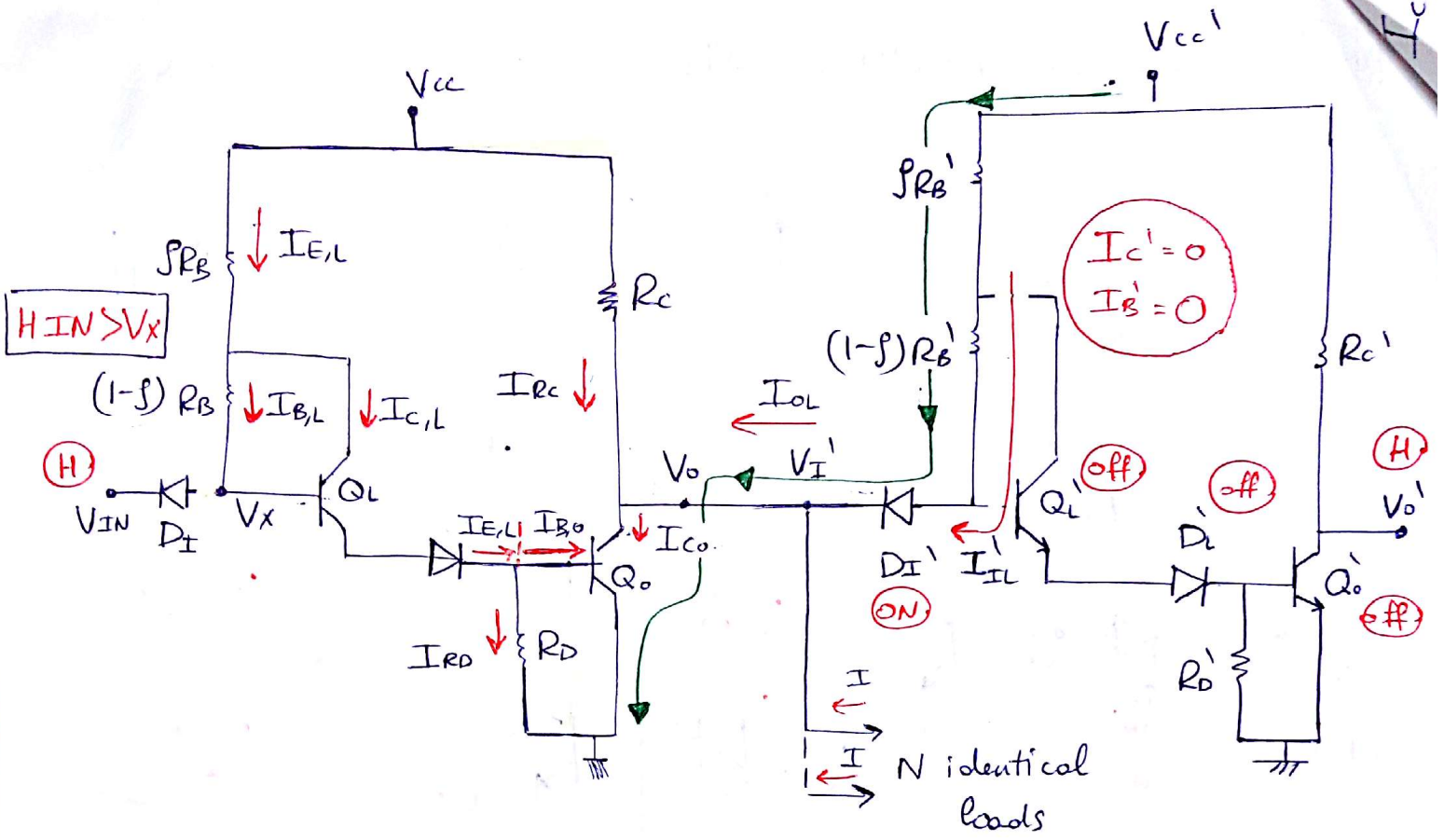


(X) Splitting R_B into to resistors, provides more current at output for driven in OL state, decrease current for load in IL state $\Rightarrow \beta R_B + (1-\beta) R_B = R_B$

(X) for Q_L when ON, we have a voltage drop on $(1-\beta)R_B \Rightarrow V_{C,L} > V_{B,L}$

$V_{BC,L} = V_{B,L} - V_{C,L} \Rightarrow$ negative

BC junction is reverse biase $\Rightarrow Q_L$ FA (does not saturate)



EXAMPLE 6.1

$V_{OH} = V_{CC}$

$V_{OL} = V_{CE(sat)}$

$V_{IL} = \underbrace{2\,V_{BE(FA)}}_{\hookrightarrow Q_L, Q_o} = 1.4\,V$

$V_{IH} = V_{BE,L\,(FA)} + V_{BE,o\,(FA)}$

$= 1.5\,V$

$$I'_{IL} = \frac{V_{CC}' - V_{DI}'(on) - V_{CE,o}(sat)}{R_B'} = \boxed{I\beta'_{RB\,(OH)}}$$

$$I_{OL} = I_{C,o} - I_{Rc}$$

$$I_{Rc} = \frac{V_{CC} - V_{CE(sat)}}{R_c} = \boxed{I_{Rc\,(OL)}}$$

$I_{C,0} = \alpha' \beta_F I_{B0}$

@ EOS , $\alpha = 1$, $I_{C,0} = \beta_F I_{B,0}$

$I_{B,0} = I_{E,L} - I_{RD}$

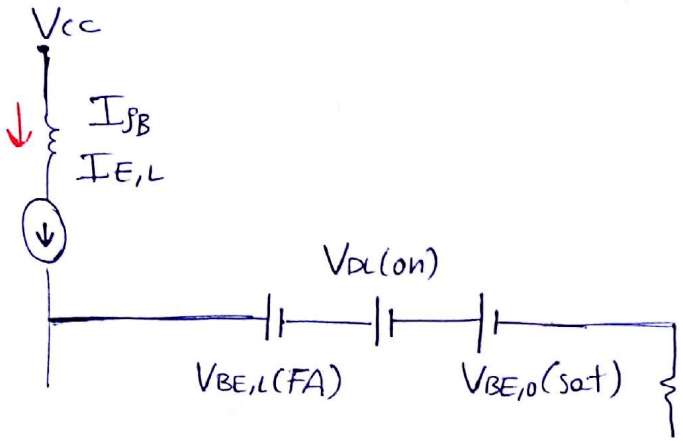
$I_{RD} = \dfrac{V_{BE,0}(sat)}{R_D}$

$I_{E,L} = \dfrac{V_{CC} - V_{BE,L} - V_{DL} - V_{BE,0}}{\rho R_B + \cancel{\dfrac{(1-\rho) R_B}{1+\beta}}}$ → ignore

NOTE:-

pnp → start sat
→ finish off

npn → start off
→ finish sat



$\Rightarrow I_{\rho B} = I_{E,L} = \dfrac{V_{CC} - V_{BE,L}(FA) - V_{DL} - V_{BE,0}(sat)}{\rho R_B} = I_{\rho R_B}(OL)$

$I_{RC}(OH) = 0$

Load : current through R_B'

$I_{R_B}' \downarrow \Rightarrow I_{IL}'$

* Driver : current through $\int R_B \Rightarrow I_{\int R_B} \uparrow$, $I_{E,L} \uparrow$

$I_{B,0} \uparrow$, $I_{C,0} \uparrow$, $I_{OL} \uparrow$

$$N = \frac{I_{OL}}{I_{IL}} \uparrow$$

6.6 DTL Power Dissipation

→ examples ←
- ✓ 6.2
- ✓ 6.3

* OH

$$I_{CC(OH)} = I_{RB(OH)} + \cancel{I_{RC(OH)}}^{\,0}$$

$$I_{RB(OH)} = \frac{V_{CC} - V_{DI} - V_{IN(low)}}{R_B}$$ ← logic 0 not V_{IL}

* OL

$$I_{CC(OL)} = I_{\int RB(OL)} + I_{RC(OL)}$$

$$I_{RC(OL)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

$$I_{\int RB(OL)} = \frac{V_{CC} - V_{BE,L(FA)} - V_{DL} - V_{BE,0(sat)}}{\int R_B}$$

$$P_{CC(avg)} = \frac{I_{CC(OL)} + I_{CC(OH)}}{2} V_{CC}$$

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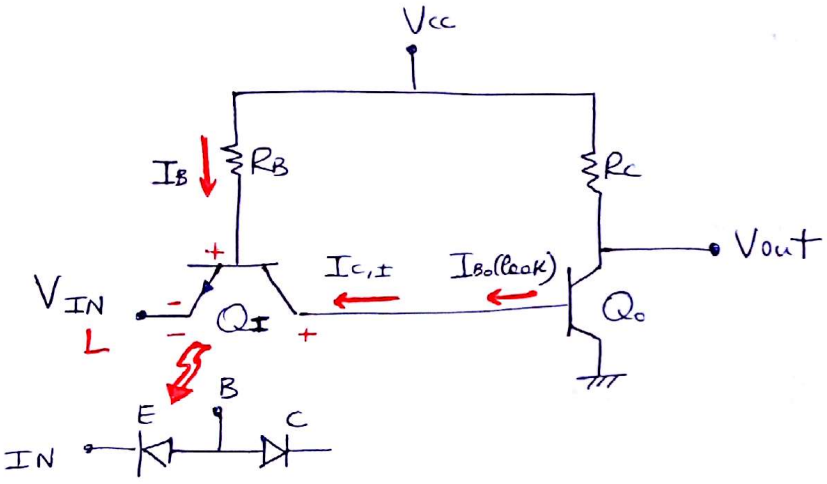
* Chapter 7 Transistor Transistor Logic

7.1 Basic TTL inverter



*Advantages :-
→ smaller size
→ higher fan-out

$V_{B,I} > V_{E,I}$

$$I_B = \frac{V_{cc} - V_{BE,I}(sat) - V_{IN}(low)}{R_B} \text{ in mA}$$

$V_{IN}(low) \neq V_{IL}$ & logic zero (@Eoc)

then $I_{B,I} \gg I_{c,I}$

Q_I operates in a kind of unconventional way :-
at low input (B-E)J is Forward-Biased,
I_{B_I} enters Q_I and I_{EI} exits E_I to low input.
This transistor action forces $I_{c,I}$ into Q_I
But $I_{c,I} = I_{B_o}$ (leakage) and is less than $I_{B,I}$
Q_o is off! voltage at base is not enough to turn Q_o ON.

$I_{RC} = 0$

* $V_o = V_{CC} = \boxed{V_{OH}}$

* $-V_{IL} - V_{CE,I}(sat) + V_{BE,o}(FA) = 0$

$V_{IL} = 0.7 - 0.2 = 0.5\ V$

$\boxed{V_{IL}} = V_{BE,o}(FA) - V_{CE,I}(sat)$

$\Rightarrow V_{IL}$: when Q_o turns FA

* $-V_{IH} - V_{CE,I}(sat) + V_{BE,o}(sat)$

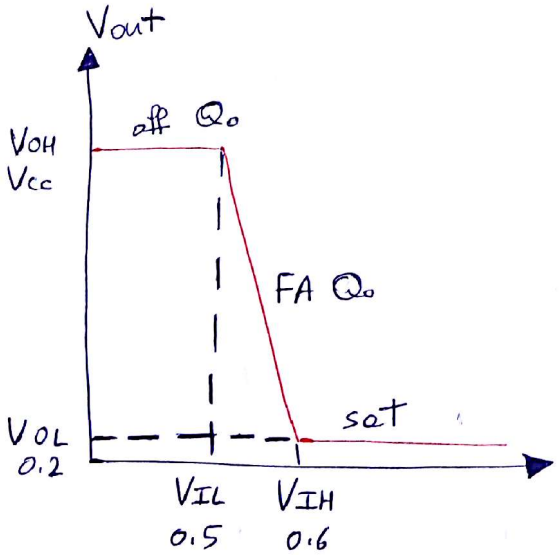
$\boxed{V_{IH}} = V_{BE,o}(sat) - V_{CE,I}(sat)$

$= 0.8 - 0.2 = 0.6\ V$

$\Rightarrow V_{IH}$: when Q_o turns to sat mode

* $V_{OL} = V_{CE,o}(sat) = 0.2$

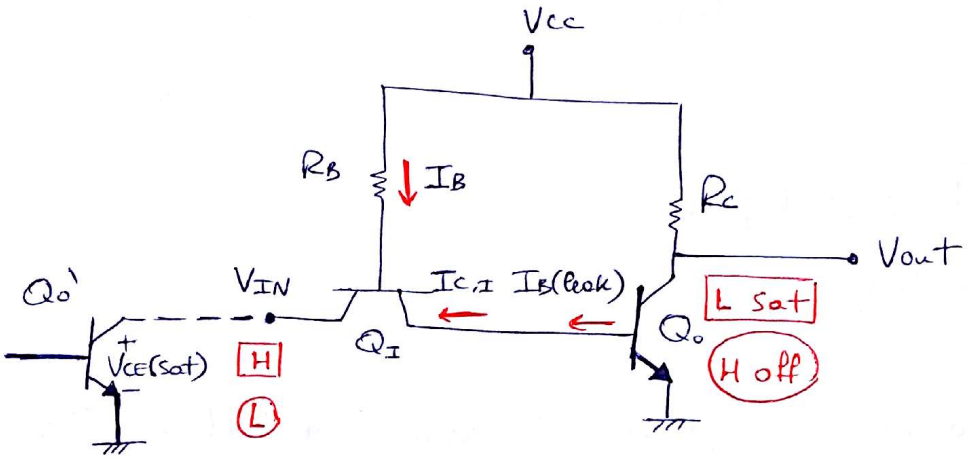
Until now, $V_{E,I} < V_{B,I}$ and Q_I is in saturation region while input increases



As input increases, $V_{E,I}$ becomes higher than $V_{B,I}$ $\Rightarrow$ (B-E)J for Q_I is reverse biased, with (B-C)J still forward biased $\Rightarrow Q_I$ operates in RA region, supplying large current to Q_o and Q_o will still saturate.

7.2 Comparison of stored charge removal between DTL and Basic TTL circuit

For TTL



B-C : 0.6

B-E : 0.8

$$V_{B,I} = V_{BE,I}(?) + V_{IN}(low)$$

$$= V_{BE,I}(?) + V_{CE}(sat)$$

$V_{B,0} = V_{C,I} = V_{BE,0}(sat)$ → initially

$$V_{BC,I} = V_{BE,I} + V_{CE}(sat) - V_{BE,0}(sat)$$

0.1 or 0.2 < $V_{BC,I}(sat)$ ⇒ Q_I is considered FA

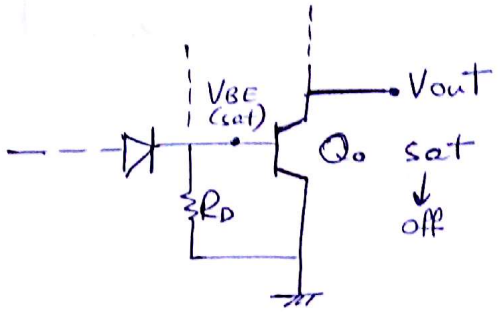
$$I_{C,I} = \beta_F I_{B,I}$$

$$I_{B,I} = \frac{V_{cc} - V_{BE}(FA) - V_{IN}(low)}{R_B}$$ ($V_{IN}(low)$ → $V_{CE}(sat)$)

$I_{C,I}$: charge removal current for Q_0

For DTL

$$I_{SCR} = I_{RD} = \frac{V_{BE,on(sat)}}{R_D}$$



⇒ For TTL charge removal current is much higher than that of DTL

⇒ Delay time of DTL is bigger, and TTL is faster.

ex 7.1 Find factor of improvement comparing TTL & DTL

$R_D = 5K$, $R_B = 2K$, $V_{cc} = 5$, $\beta_F = 50$

$$I_{RD,SCR}(DTL) = \frac{0.8}{5K} = 160\mu A = 0.16\ mA$$

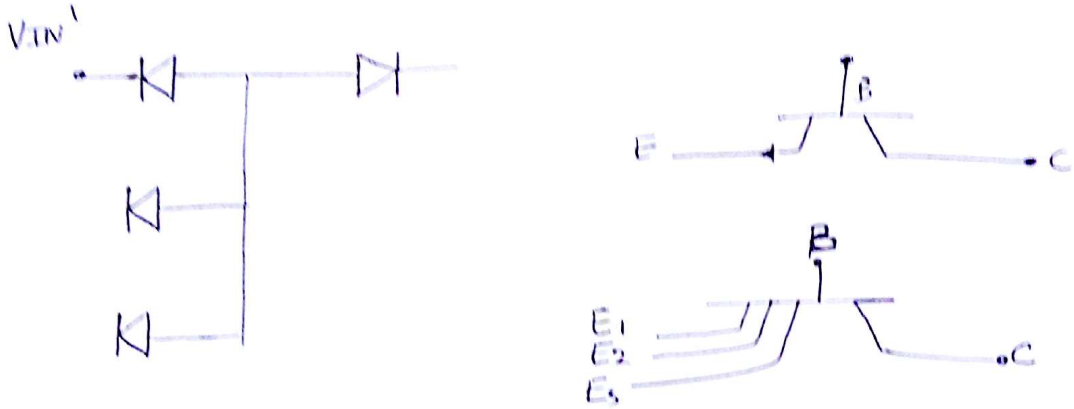
↳ stored charge removed

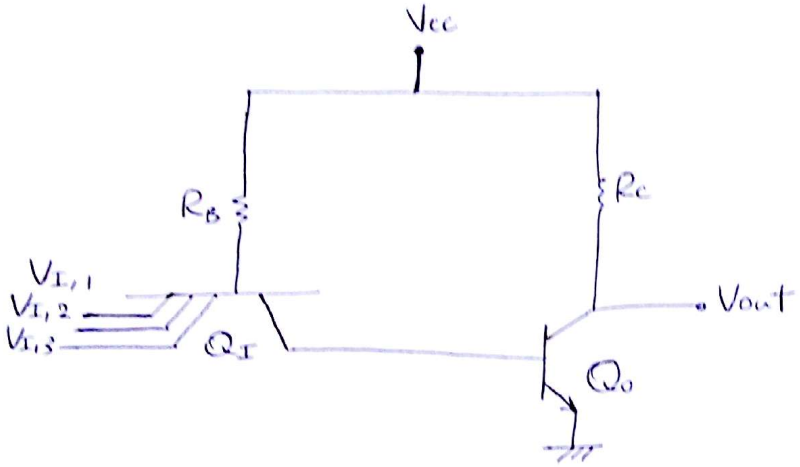
$$I_{CI,SCR}(TTL) = 50\left(\frac{5-0.7-0.2}{2K}\right) = 102.5\ mA$$

$$\frac{102.5}{0.160} = 640.6 \rightarrow \text{Factor of improvement}$$

5] Basic TTL NAND Gate

→ with multi-emitter inputs





① Any or all inputs low

(B-E)J forward, Q_I sat, Q_o off

$V_o = V_{cc} = V_{OH}$

② All inputs high

(B-E)J reverse biased, Q_I is RA

Large current is supplied to Q_o & Q_o is sat

$V_{OL} = V_{CE}(sat)$

* For two inputs :-

I_1	I_2	o/p
L	L	H
L	H	H
H	L	H
H	H	L

NAND

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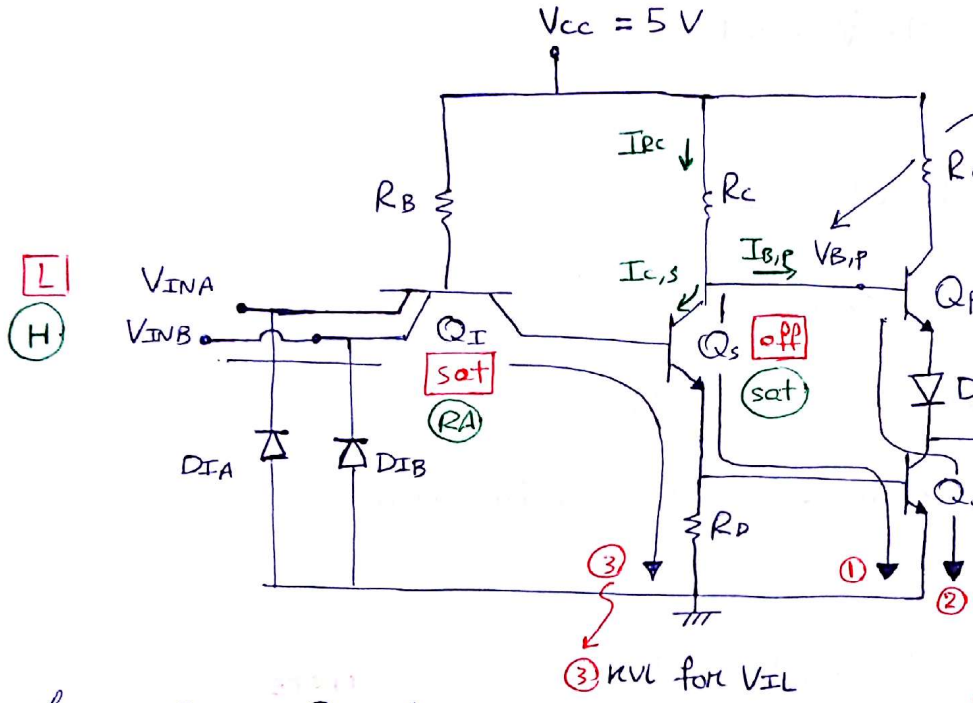
7.4 Standard TTL NAND Gate with TOTEM Output



① $V_{B,P} = V_{CE,S(sat)} + V_{BE,O(sat)}$

② $V_{E,P} = V_{D,L} + V_{CE(sat)}$

$V_{BE,P} \cong 0.1 < V_{BE(FA)}$ ↳ Q_P off

③ KVL for V_{IL}

- Logic 0 → Q_I sat
- Logic 1 → Q_I RA

* Q_O → pull down
* Q_P → pull up
* R_D → discharge path for Q_S

⇒ DI's: clamping diodes (used for protection if low i/p goes below −0.7)
when i/p H we don't considere them

* At high input

Q_S sat

Q_O sat

Q_S → for logic inversion
when Q_I, Q_S sat & Q_P is off

7.5 Standard TTL VTC

V_{OH}

Input low

$$I_{B,I} = \frac{V_{CC} - V_{BE,I(sat)} - \cancel{V_{IN(low)}}^{V_{CE(sat)}}}{R_B}$$

high enough to saturate Q_I

$I_{C,I} = -I_{B,s}$ (leakage) small

$I_{B,s} = V_{CE,I(sat)} + V_{IN(low)} < V_{BE(FA)}$

$Q_s \Rightarrow$ off then $Q_o \Rightarrow$ off , $Q_p \Rightarrow$ EOC , DL $\Rightarrow$ ON

$I_{B,p(FA)}$ ignored

$V_{OH} = V_{CC} - V_{BE,p(FA)} - V_{DL(ON)} = 3.6\,V$

NOTE

without R_D ⇒ there isn't a break voltage

V_{IL} voltage at which Q_s turns FA

$V_{IL} = V_{BE,s(FA)} - V_{CE,I(sat)} = 0.5\,V$

$I_{C,s} \approx I_{Rc}$

$V_{IN} \uparrow$, $I_{B,s} \uparrow$, $I_{C,s} (\approx I_{Rc}) \uparrow$, $V_{Rc} \uparrow$, $V_o \downarrow$

V_{IB} break input voltage when Q_o is also FA

$V_{IB} = V_{BE,s(FA)} + V_{BE,o(FA)} - V_{CE,I(sat)} = 1.2\,V$

V_{OB} break output voltage

$V_{OB} = V_{CC} - I_{Rc} R_C - V_{BE,p(FA)} - V_{DL(ON)}$

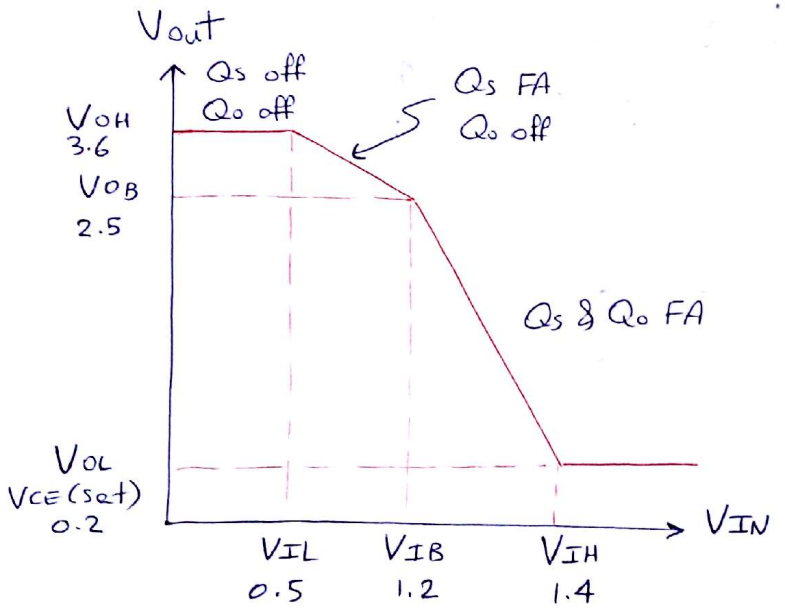
initially currents of Q_o are zero $\Rightarrow I_{Rc} \approx I_{C,s} \approx I_{E,s} \approx I_{RD}$

then $I_{E,s} \approx I_{RD}$ & $I_{B,p(FA)}$ ignored

$$I_{RC} = \frac{V_{BE,o(FA)}}{R_D}$$

$$\rightarrow V_{OB} = V_{CC} - \frac{V_{BE,o(FA)}}{R_D} R_C - V_{BE,P(FA)} - V_{DL(ON)}$$

$$V_{OB} = V_{CC} - \left(\frac{R_C}{R_D} - 1\right) V_{BE(FA)} - V_{DL(ON)} = 2.5\,V$$

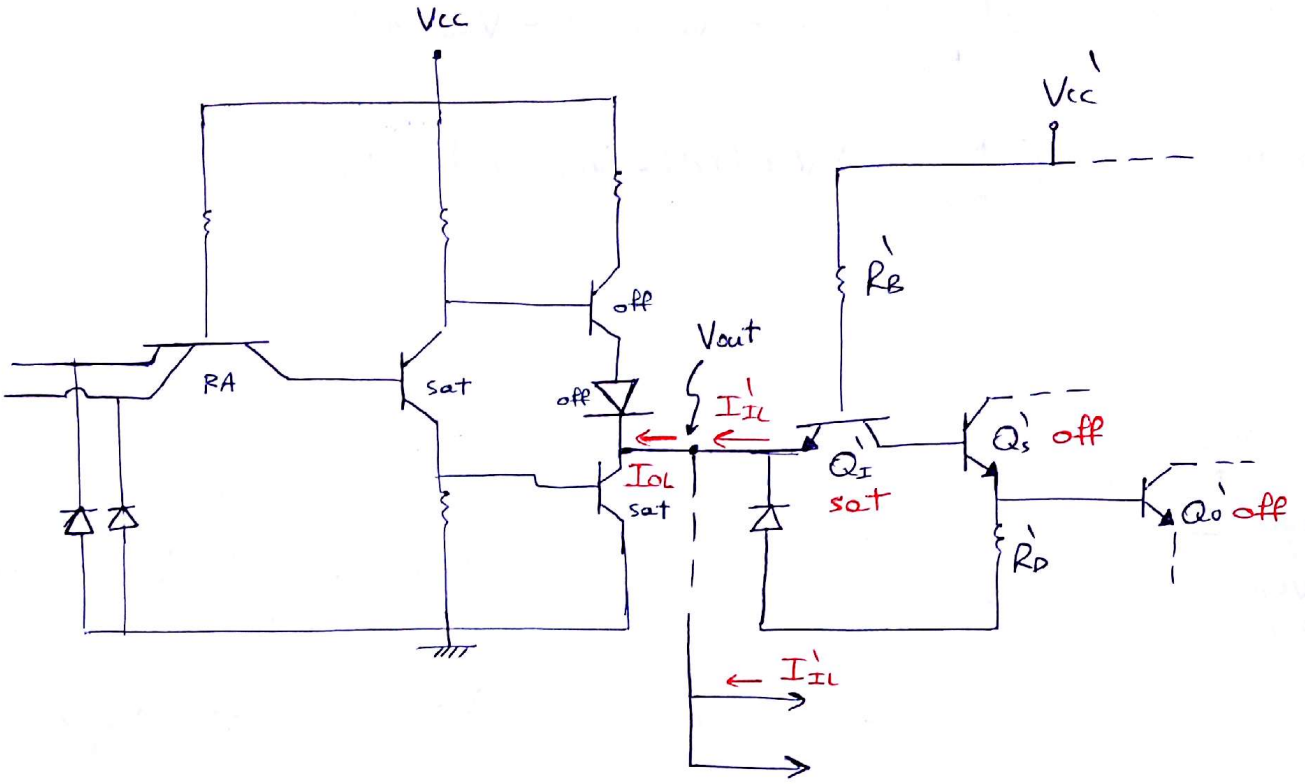


$$V_{IH} = 2V_{BE(sat)} - V_{CE,I(sat)}$$
$$= 1.4\ V$$

$$V_{OL} = V_{CE,o(sat)} = 0.2\ V$$

As input increases and both Q_o & Q_s are FA, output goes down faster with a steeper slope of the VTC is high enough to saturate both Q_o & Q_s.

7.6 Fan-out



Inglect $I'_{c,I}$ current

$$I'_{IL} = \frac{V'_{cc} - V'_{BE,I}(sat) - V_{CE,o}(sat)}{R'_B}$$

$$I_{OL} = I_{c,o} = o'\beta_F I_{B,o}$$

$$I_{B,o} = I_{E,s} - I_{RD}$$

$$I_{RD} = \frac{V_{BE,o}(sat)}{R_D}$$

$$I_{E,s} = I_{RC} + I_{B,s}$$

$$I_{RC} = \frac{V_{cc} - V_{CE,s}(sat) - V_{BE,o}(sat)}{R_c}$$

$$I_{B,s} = I_{c,I}(RA) = (1+\beta_R) I_{B,I}$$

$$I_{B,I} = I_{RB} = \frac{V_{cc} - V_{BC,I}(RA) - V_{BE,s}(sat) - V_{BE,o}(sat)}{R_B}$$

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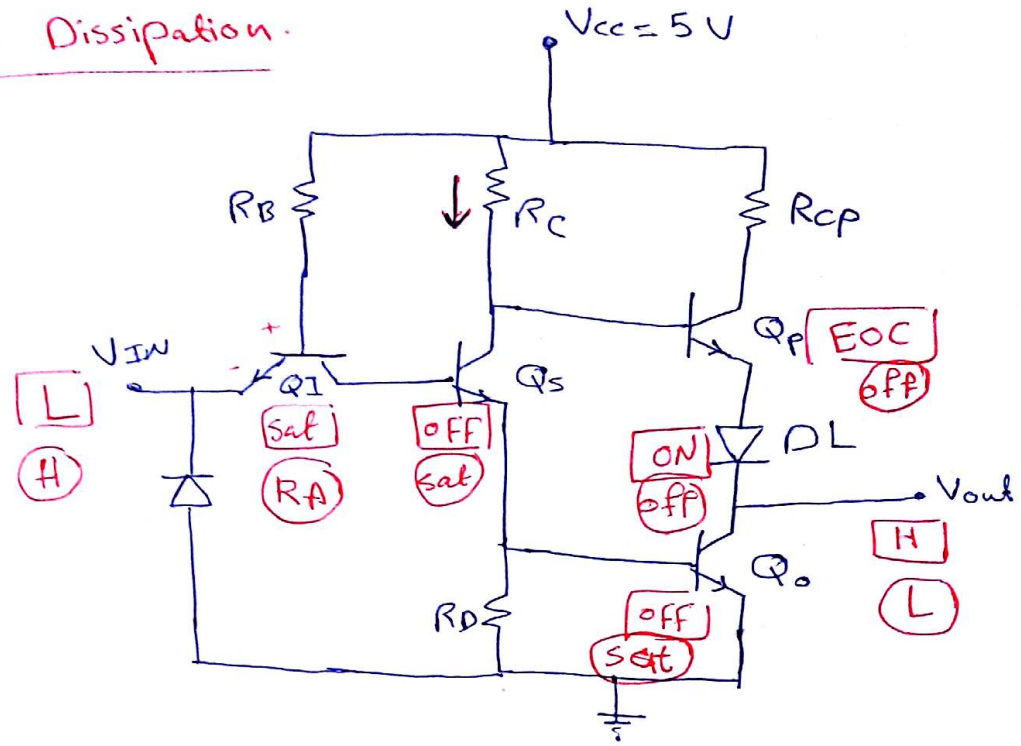
not included in first exam

7.7 Power Dissipation.



$I_{CC(OH)}$

$I_{RC} = I_{BP(FA)}$

small

neglect

I_{RCP} neglect (small)

$$I_{RB(OH)} = \frac{V_{CC} - V_{BE,I(sat)} - V_{CE(sat)}}{R_B}$$

$$I_{CC(OH)} = I_{RB(OH)}$$

$I_{CC(OL)}$

$$I_{RB(OL)} = \frac{V_{CC} - V_{BC,I(RA)} - 2V_{BE(sat)}}{R_B}$$

$$I_{RC(OL)} = \frac{V_{CC} - V_{CE,S(sat)} - V_{BE,O(sat)}}{R_C}$$

$I_{RCP} = 0$

$$I_{CC}(oL) = I_{FB}(oL) + I_{RC}(oL).$$

$$P_{cc(avg)} = \frac{I_{CC}(oL) + I_{CC}(oH)}{2} \; V_{CC}$$

7.9 Low power TTL. (LTTL)

same circuit but smaller current, ≡ higher resistance values.

* advantage: less power dissapation.

dissadvantages: less fan out.

* Example 7.5

$P_{cc(avg)}$ 919 μW ⟶ compare them when we change the resistance.

but in example 7.4 $P_{cc}(avg) = 10.4$ mW

7.10 High speed TTL

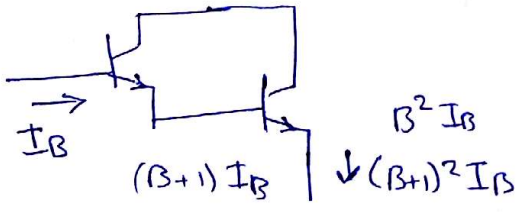
higher current, less R values

advantages: higher speed and better Fan-out.

disadvantages: worse power dissapation.

to have higher current ⇒ 1- less R values

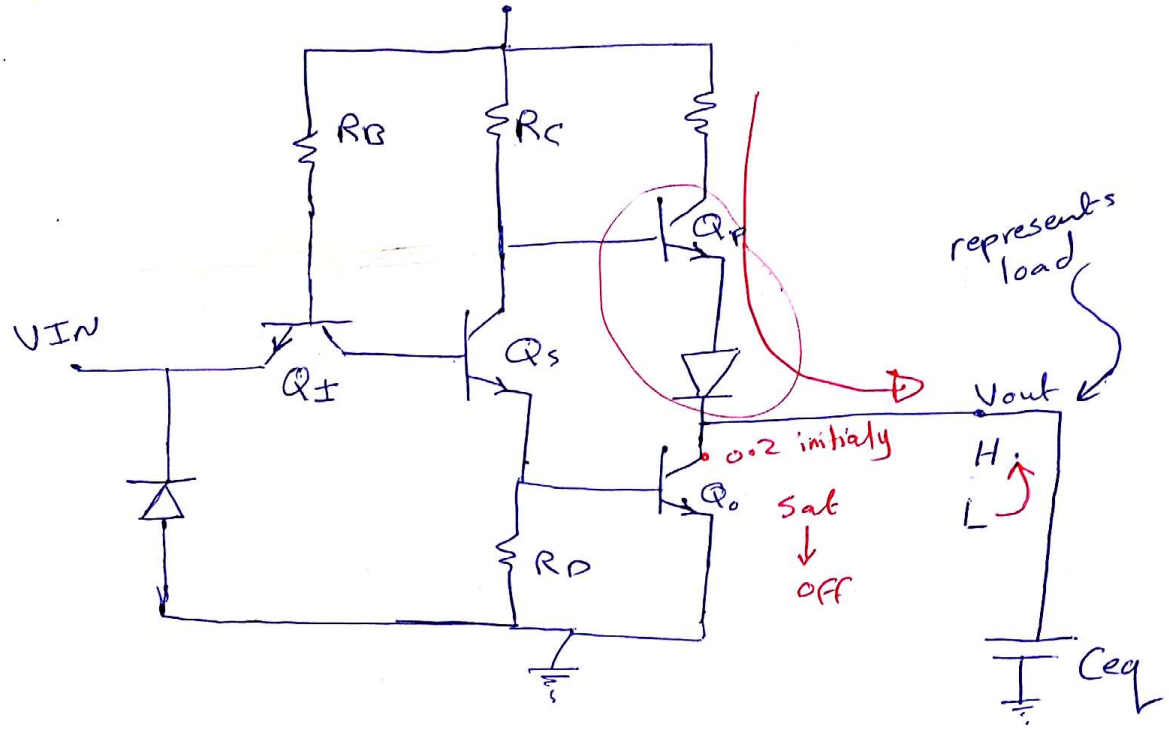
2- Also Q_P and DL are replaced by Darlington pair.



Back to 7.4

Comparison of load capacitance charging between basic TTL and TTL with TOTEM pole.

* TOTEM pole.



Q_0 sat → off

O/P L → H

$\tau = R_{cp} C_{eq}$

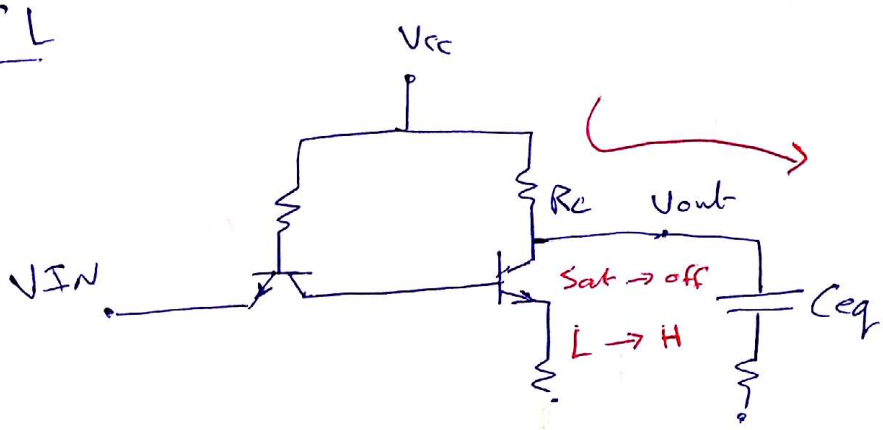
$$I_{ch.} = \frac{V_{cc} - V_{CEP} - V_{DL(on)} - V_{CE,0(sat)}}{R_{cp}}$$

(initialy)

* Basic TTL

$\tau = R_c C_{eq}$
Passive

$I_{ch} = \frac{V_{cc} - V_{CE(sat)}}{R_c}$ → Initially



- $RCp = 0.1\ R_c$
- $\tau_{active} < \tau_{passive}$
- Basic TTL is slower.
- $I_{active} > I_{passive}$

⇒ TTL with TOTEM pole is fasten than Basic TTL.

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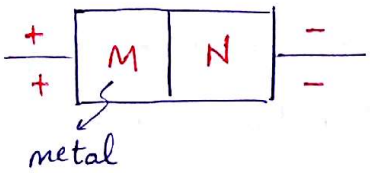
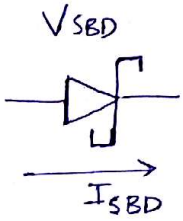
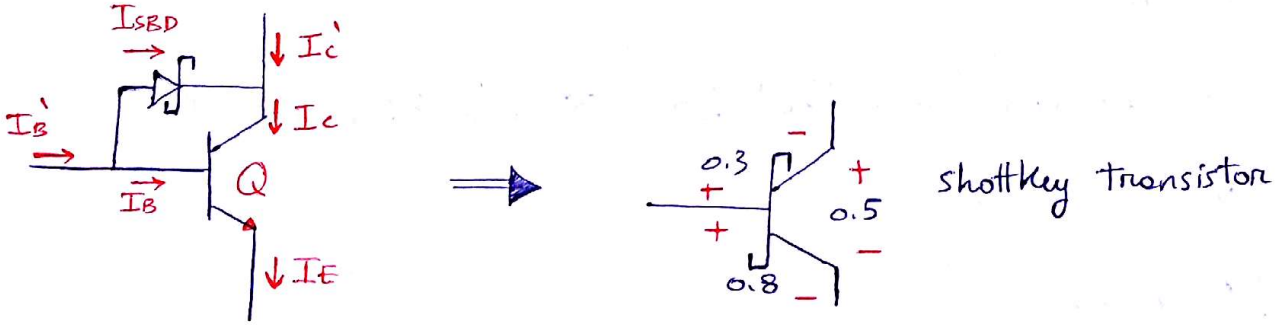
⊛ Chapter 8 Schottkey Transistor Transistor Logic (TTL)



V_{SBD} : shottkey barrier diode

* SBD turns on at $V_{SBD} = 0.3\ V$





shottkey transistor

* Shottkey Clamped BJT

→ For regular BJT :-

$$V_{BC}(sat) = V_{BE}(sat) - V_{CE}(sat)$$
$$= 0.6\ V$$

→ To avoid saturation an SDB is connected in parallel with the (B-C) JN of BJT

→ I_B' increases until SBD turns on at 0.3 V ⇒ Diverting current through SBD, and clamping (B-C) voltage at 0.3 V

→ BJT is prevented from saturating because $V_{SBD} < V_{BC}(sat)$

$0.3 < 0.6$

→ SBJT is said to operate in **hard mode** (some refrences call it EOS)

→ ADVATAGES :- provides less time spent in discharging saturation current when transistor turns from sat to off

⊛ Modes of operation

① Cut off

Small current, such that both SBD and BJT are off

$I_B' = I_C' = I_E = 0$

② FA mode

(B-E) JN → forward biased $V_B > V_E$

(B-C) JN → reverse biased $V_B < V_C$, SBD off

like a BJT in FA

$V_{BE(FA)} = 0.7$

③ Hard mode

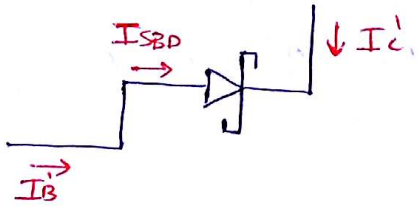
BE & BC junctions are forward, with (B-C) voltage clamped at V_{SBD} (0.3 V).

$V_{BE(hard)} = 0.8\ V$, $V_{BC(hard)} = V_{SBD(hard)} = 0.3\ V$

$V_{CE(hard)} = 0.5\ V$, $I_{C(hard)} = \beta I_B(hard)$

$I_C'(hard) = I_C - I_{SBD} = \beta I_B - I_{SBD}$

④ Reverse - Shottky mode



(B-E) JN → reverse biased

(B-C) JN → forward at V_{SBD}

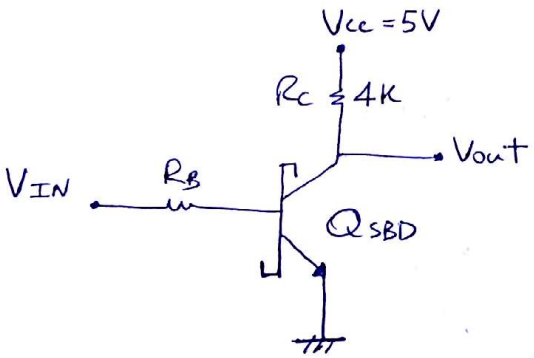
V_{BC} can't reach 0.7 V ⇒ BJT can't be RA (for a BJT to RA $V_{BC}=0.7$ & V_{BE} reverse)

$I_B = I_C = I_E = 0$ → BJT is off

Current only flows in SBD $I_B' = I_{SBD} = -I_C'$

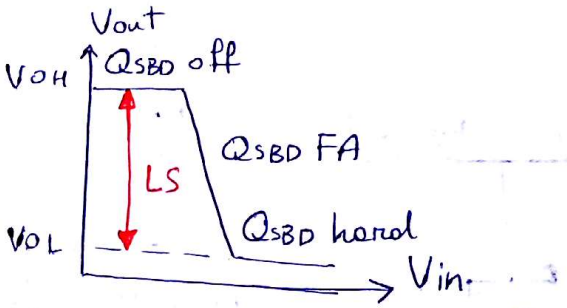
EX 8.1 (Inverter Logic Swing)

find the logic swing



* Logic Swing : LS

$$LS = V_{OH} - V_{OL}$$



* V_{OH}

$V_{IN} < V_{BE(FA)}$

Q_{SBD} is off , $I_{RC} = 0$, $V_{out} = V_{OH} = V_{cc} = 5V$

* V_{OL}

Input high enough for Q_{SBD} to operate in hard mode

$V_{OL} = V_{CE(hard)} = 0.5V$

⇒ $LS = V_{OH} - V_{OL} = 5 - 0.5 = 4.5$ V

* V_{IL}

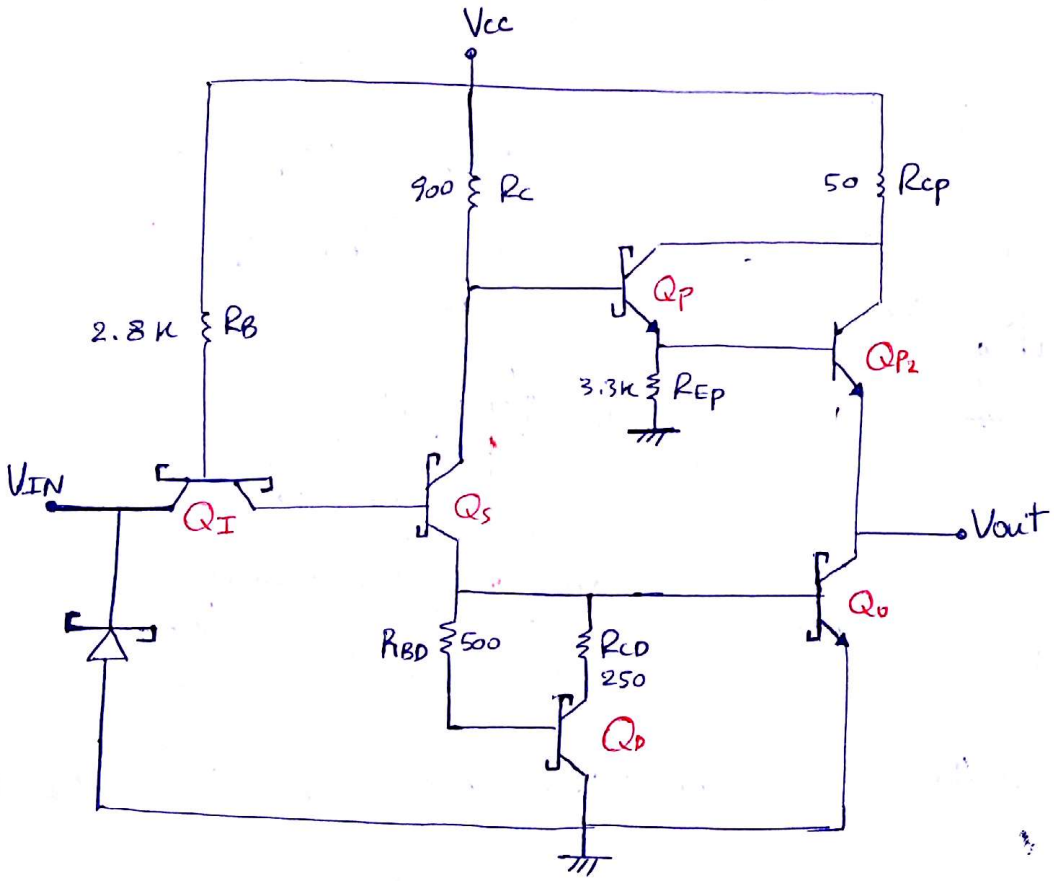
$V_{IL} = V_{BE(FA)} = 0.7\ V$

* V_{IH}

$V_{IH} = I_B R_B + V_{BE(hard)}$

$I_B = \frac{I_C}{\beta} = \frac{V_{CC} - V_{CE(hard)}}{R_C \beta}$

8.3 Shottkey - Clamped TTL (STTL)



Q_p & Q_{p2} : Darlington pair

→ To provide higher current

R_{EP} : Discharge path for Q_{p2}

Q_{p2} can't saturate ⇒ no need to Q_{SBD}

$V_{CEp2} = V_{BE,p2}(FA) + V_{CE,p}(hard)$

$= 0.7 + 0.5$

$= 1.2\ V > V_{CE}(hard)$

→ Q_{p2} ⇒ FA mode

* R_D in TTL is replaced by Q_D

R_{BD} & R_{CD} : Discharge paths for Q_o

* R_{BD} & R_{CD} are designed such that Q_o & Q_D run simultaneously

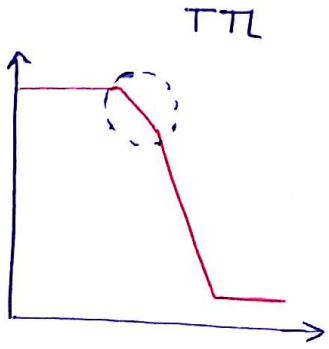
* Q_s won't operate unless, Q_o & Q_D are on

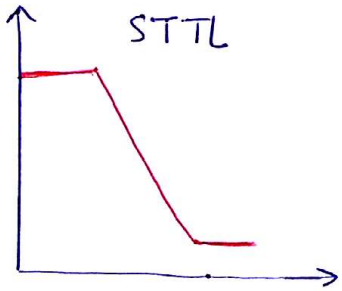
→ Removes break point

→ VTC sharpen (less transition width)

→ Faster than TTL

→ Better noise margin





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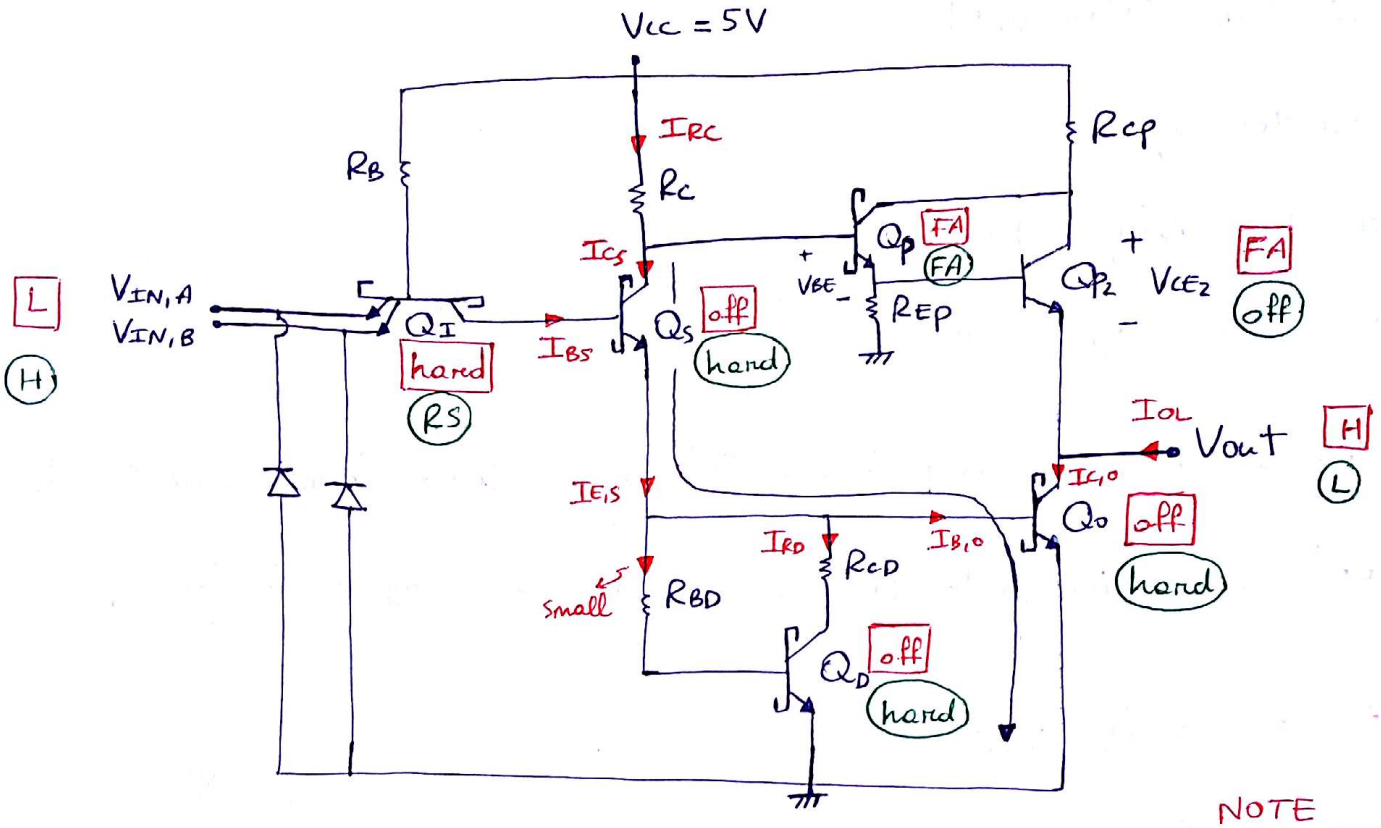
8.3 Shottkey - Clamped TTL (STTL)



NOTE

current in R_{BD} is very small

$I_{BD} < I_{CD}$ ← ignore

* When Q_{p_2} is on, if Q_p is in (saturation) hard

$$V_{CE,p2} = V_{CEp}(sat) + V_{BE,p_2} > V_{CE}(sat)$$

$\Rightarrow$ Q_{p_2} does not saturate $\rightarrow$ no need for a QSBD

* Q_p is always ON

Q_S: logic inversion drive splitter

* Q_S turns ON only when Q_o & Q_D are ON

⇒ Removal of break point

① Lower V_{IH} (compared to TTL)

② Better HNM

③ Less transition width

⇒ Fasten by 8 ns

for TTL delay = 10 ns

for STTL delay = 2 ns

Q_D : active discharge path for Q_0 when Q_0 turns from hard to off

R_{EP} : connection path for Q_0 to ground discharge path for Q_{P2}

ex 8.2 SSTL VTC

* input low

$V_{OH} = V_{CC} - 2V_{BE(FA)} = 3.6\,V$ (ignore $I_{BP(FA)}$)

→ when Q_0, Q_5 turn FA

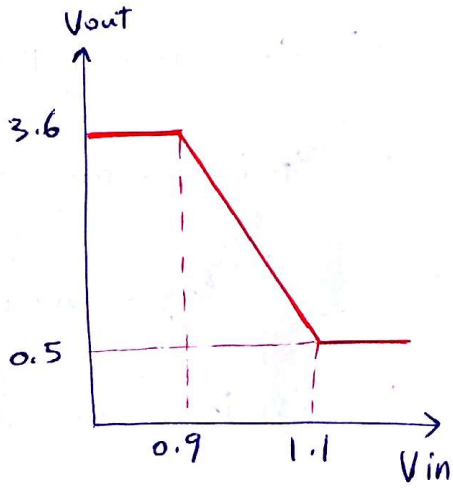
$V_{IL} = -V_{CE(hard)} + 2V_{BE(FA)} = 0.9\,V$

* input high

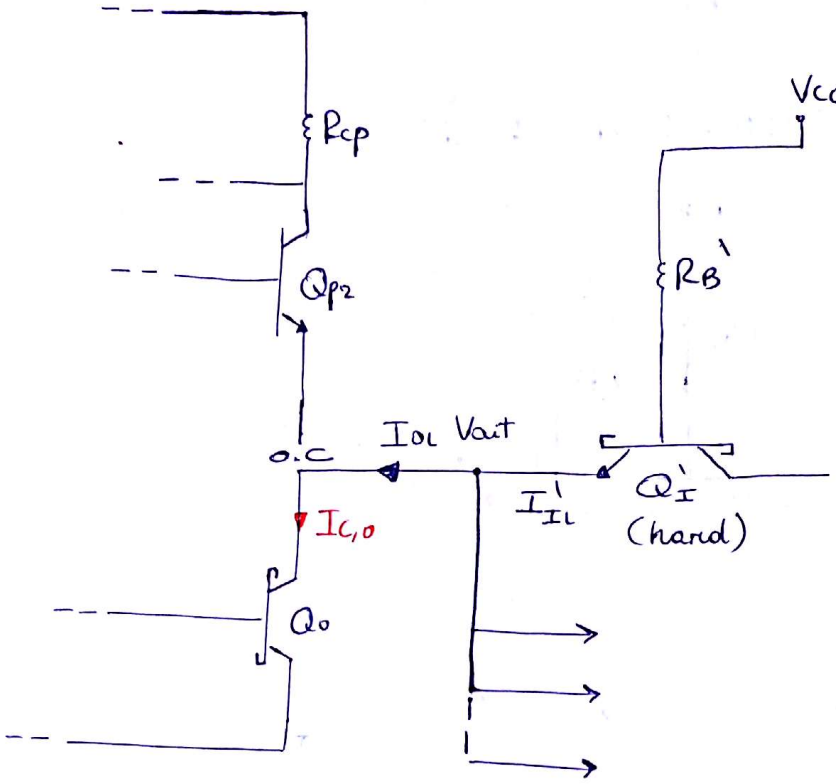
→ when Q_0, Q_5 turn hard

$V_{IH} = -V_{CE(hard)} + 2V_{BE(hard)} = 1.1\,V$

$V_{OL} = V_{CE,0(hard)} = 0.5$



8.4 STTL Fan-out (output low at driver)



$$\Rightarrow I'_{IL} = \frac{V_{CC}' - V_{BE,I}'(hard) - V_{CE,O}(hard)}{R_B'}$$

$$\Rightarrow I_{OL} = I_{C,O}$$

neglect I_{SBD} (small)

$I_{CO} = \beta_F I_{BO}$ ⤳ go back to page ⑬ to see the currents

$I_{BO} = I_{ES} - I_{RCD}$

$$I_{RCD} = \frac{V_{BE,O}(hard) - V_{CE,D}(hard)}{R_{CD}}$$

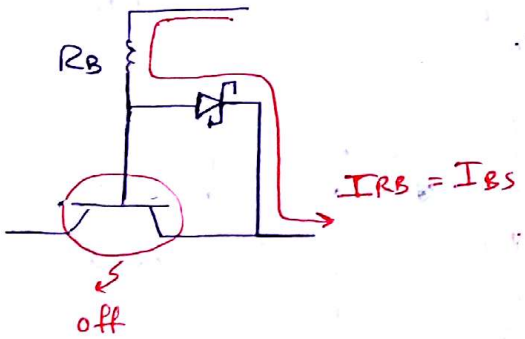
$I_{ES} = I_{CS} + I_{BS}$

$I_{BP}(FA)$ is negligible

$$I_{CS} = I_{RC} = \frac{V_{CC} - V_{CE,s}(hard) - V_{BE,o}(hard)}{R_C}$$

$$I_{BS} = I_{RB} = \frac{V_{CC} - V_{SBD} - 2\,V_{BE}(hard)}{R_B}$$

because



$$\Rightarrow N = \frac{I_{OL}}{I'_{IL}}$$

example 8.3 $\rightarrow N = 149$

8.5 Power Dissipation

* $I_{CC}(OL)$

ignore FA Base currents

$$I_{RCP}(OL) \cong I_{REP} = \frac{V_{CE,s}(hard) + V_{BE,o}(hard) - V_{BE,P}(FA)}{R_{EP}}$$

$$I_{RC}(OL) = \frac{V_{CC} - V_{CE,s}(hard) - V_{BE,o}(hard)}{R_C}$$

$$I_{RB(OL)} = \frac{V_{CC} - V_{SBD} - 2V_{BE(hard)}}{R_B}$$

$$\Rightarrow I_{CC(OL)} = I_{RCP} + I_{RC} + I_{RB}$$

* $I_{CC(OH)}$

$$I_{RCP(OH)} = I_{REP} = \frac{V_{CC} - V_{BE,P(FA)}}{R_{EP}}$$

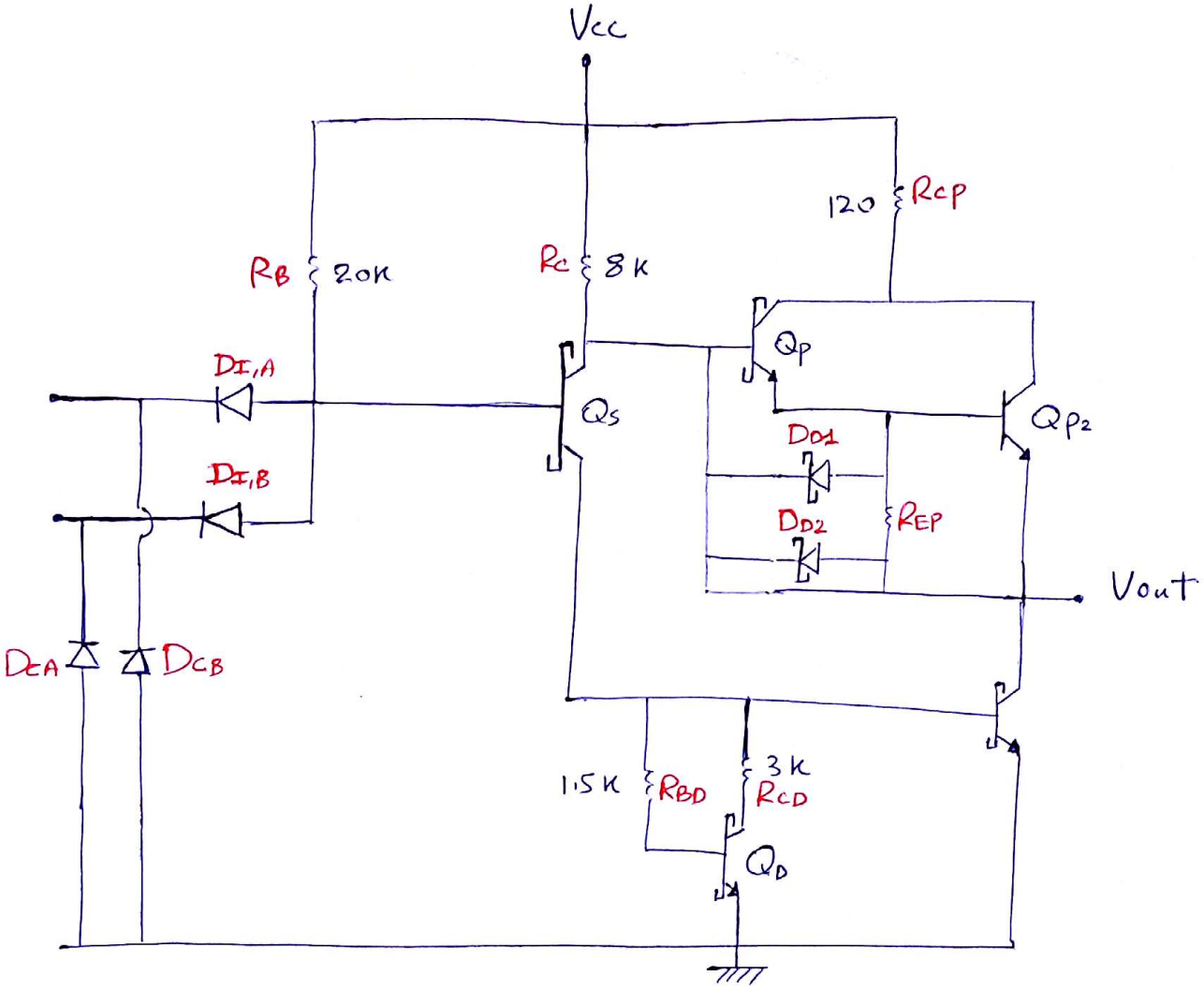
$$I_{RC(OH)} = I_{BP(FA)} \approx 0$$

$$I_{RB(OH)} = \frac{V_{CC} - V_{BE,I(hard)} - V_{CE(hard)}}{R_B}$$

$$I_{CC(OH)} = I_{RCD} + I_{RB}$$

$$\rightsquigarrow P_{CC(avg)} = \frac{I_{CC(OH)} + I_{CC(OL)}}{2} \times V_{CC}$$

8.6 Low Power STTL



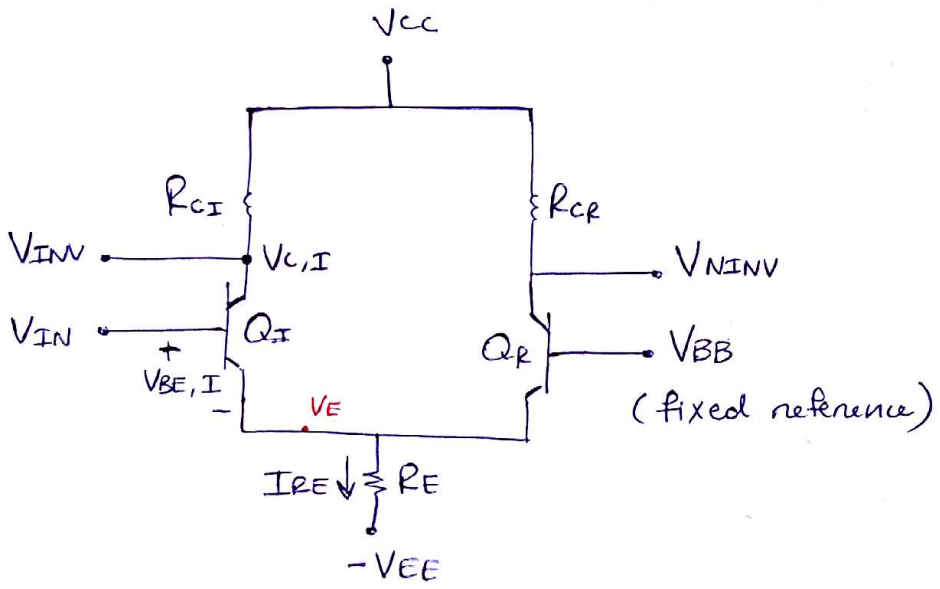
* Q_I is replaced by D_{IA} & D_{IB} since Q_I in regular TTL was used as a discharge path for base current from Q_S, when it switches from saturation to off.

For STTL Q_S does not saturate ⇒ no need for Q_I

* For output low → Q_P currents are ignored.

CH. 11 Basic Emitter Coupled Logic (ECL)

11.1 Basic BJT Current Switch



* $I_{RE} = \frac{V_E + V_{EE}}{R_E}$

⇒ Ignore Base currents

* $I_C \approx I_{RE}$ (if one of the transistor is ON and the other is OFF)

* $I_C \cong \frac{I_{RE}}{2}$ (if both are ON)

⇒ Outputs :-

$V_{INV} = V_{c,I} = V_{cc} - I_{cI} R_{cI}$

$V_{NINV} = V_{c,R} = V_{cc} - I_{cR} R_{cR}$

* $V_{IN} < V_{BB}$, Q_I off, Q_R on

$V_{INV} = V_{CC}$ (Logic high)

$V_{NINV} = V_{CC} - I_{RE} R_{CR}$ (Logic low)

* $V_{IN} > V_{BB}$, Q_I on, Q_R off

$V_{INV} = V_{CC} - I_{RE} R_{CI}$ (Logic low)

$V_{NINV} = V_{CC}$ (Logic high)

* $\boxed{V_{OH}}$ $V_{IN} < V_{BB}$

Q_R is on, $V_E = V_{BB} - V_{BE}$

$V_{BE,I} = V_{IN} - V_E = \underbrace{V_{IN} - V_{BB}}_{-ve} + V_{BE(ECL)}$

$- V_{IN} - V_{BB} + V_{BE(ECL)} < V_{BE(ECL)}$

Q_I is off

$I_{CR} = I_{RE}$

$I_{CI} = 0$

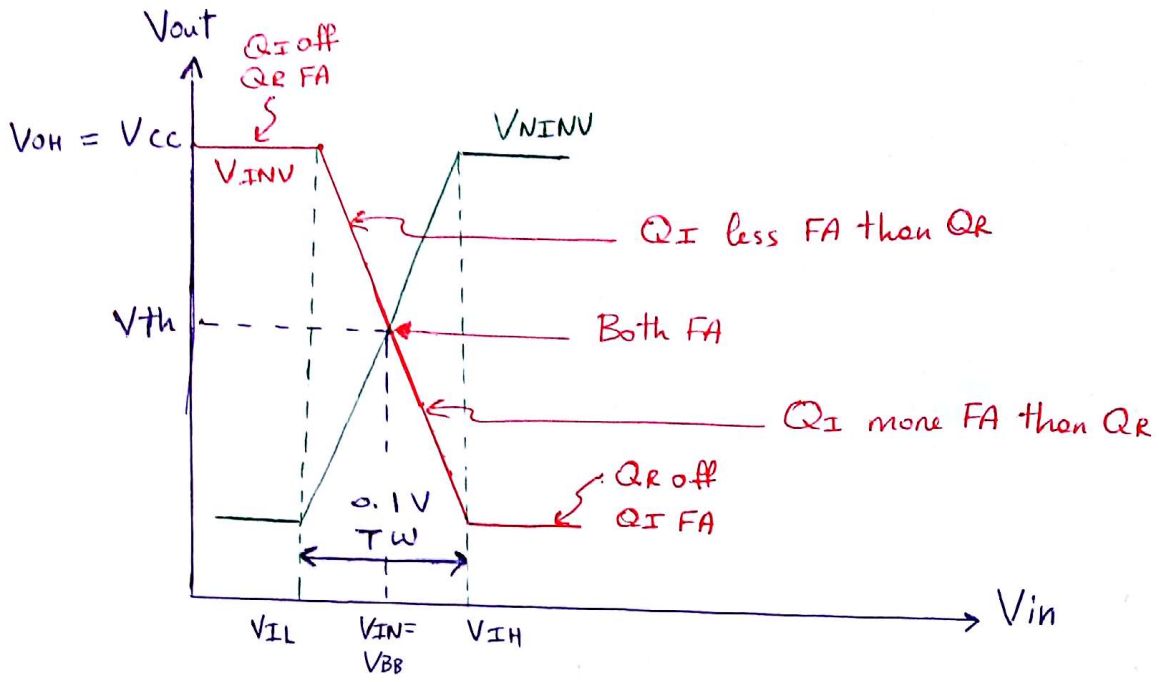
$\boxed{V_{OH} = V_{CC}}$

* Threshold Voltage V_{TH}

$V_{IN} = V_{BB}$, Q_I & Q_R are on

$$I_{CI} = I_{CR} = \frac{I_{RE}}{2} = \frac{V_{BB} - V_{BE} + V_{EE}}{2R_E}$$

V_{INV} ($V_{IN} = V_{BB}$) $= V_{CC} - I_{CI} R_{CI}$



* With proper selection of R_{CI} and R_{CR}, $V_{IN} = V_{INV} = V_{TH} = V_{BB}$
* Input low and high voltages V_{IL}, V_{IH}
* By experimentation, transistion width (TW) equal 0.1 V

→ $V_{IL} = V_{BB} - 0.05\ V$

→ $V_{IH} = V_{BB} + 0.05\ V$

↳ When $V_{IL} < V_{IN} < V_{BB}$, both Q's are on but Q_R has more current than Q_I

↳ When $V_{BB} < V_{IN} < V_{IH}$, both Q's are on but Q_I has more current than Q_R

* V_{OL} (output low voltage)

$V_{IN} > V_{BB} \rightarrow V_{IH} = V_{BB} + 0.05V$

Q_I is on

$V_E = V_{IN} - V_{BE,I(ECL)}$

$V_{BE,R} = V_{BB} - V_E = V_{BB} - V_{IN} + V_{BE,I(ECL)}$

$V_{BE,R} = V_{BB} - (V_{BB} + 0.05) + V_{BE,I(ECL)}$

$= V_{BE,I(ECL)} - 0.05 < V_{BE(ECL)}$

$\Rightarrow Q_R$ is off

$I_{CR} = 0$

$I_{CI} = I_{RE} = \dfrac{V_{IN} - V_{BE,I(ECL)} + V_{EE}}{R_E}$

$V_{OL} = V_{CC} - I_{CI} R_{CI}$

$= V_{CC} - \dfrac{V_{IN} - V_{BE,I(ECL)} + V_{EE}}{R_E} R_{CI}$

$\Rightarrow$ As input increases Q_I reaches saturation (Q_R does not saturate since V_{BB} is constant)

$V_S = V_{IN}$ when Q_I saturates

$V_o(V_s) = V_{INV} = V_{CC} - \dfrac{R_{CI}}{R_E}\left[V_s - V_{BE(sat)} - V_{EE}\right] \ldots (1)$

$-V_{IN} + V_{BC,I(sat)} + V_{INV} = 0$

$V_o(V_s) = V_{INV} = V_{IN} - V_{BC,I(sat)} \ldots (2)$ ($V_{IN} \rightarrow V_s$)

Solve (1) and (2) for $V_o(V_s)$ and V_s

$$V_S = \frac{V_{CC} + V_{BC}(sat) + \frac{R_{CI}}{R_E}(V_{BE}(sat) - V_{EE})}{1 + \frac{R_{CI}}{R_E}}$$

Find V_o from either (1) or (2)

$\Rightarrow V_o = V_S - V_{BC,I}(sat)$

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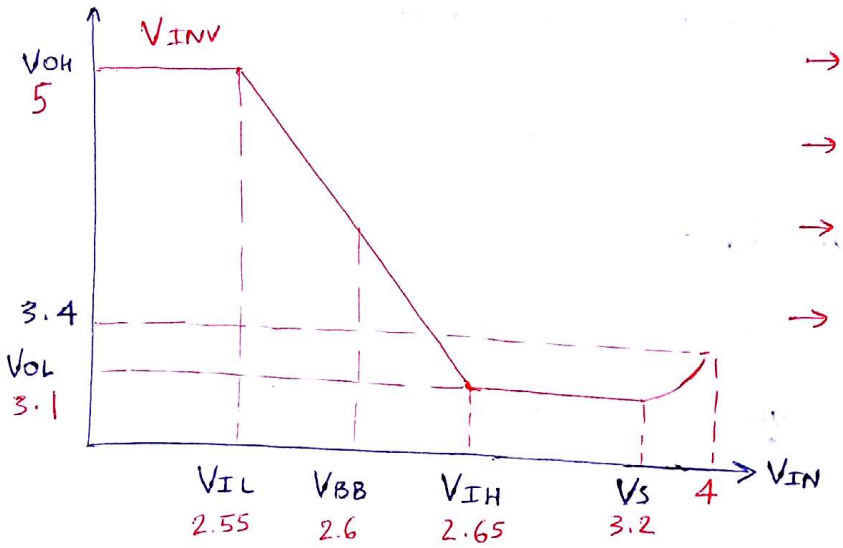
ex 11.1 Find critical voltages $V_{cc} = 5\,V$, $-V_{EE} = gnd = 0$

$V_{BB} = 2.6\,V$, $R_{CI} = R_{CR} = R_E = 1\,k$, $V_{BE(ECL)} = 0.75\,V$

$V_{BC(sat)} = 0.6\,V$



→ $V_{OH} = V_{cc} = 5\,V$

→ $V_{IL} = V_{BB} - 0.05 = 2.55\,V$

→ $V_{IH} = V_{BB} + 0.05 = 2.65\,V$

→ $V_{OL} = V_S - \frac{R_{CI}}{R_E}[V_{IH} - V_{BE,I(ECL)} + V_{EE}]$ (0.75, 0)

$V_{OL} = 3.1\,V$

$$V_S = \frac{V_{cc} + V_{BC(sat)} + \frac{R_{CI}}{R_E}[V_{BE(sat)} - V_{EE}]}{1 + \frac{R_{CI}}{R_E}} = 3.2\,V$$

(5, 0.6, 0.8, 0)

* @ $V_{IN} = 4\,V$

$V_{INV} = V_{IN} - V_{BC(sat)}$

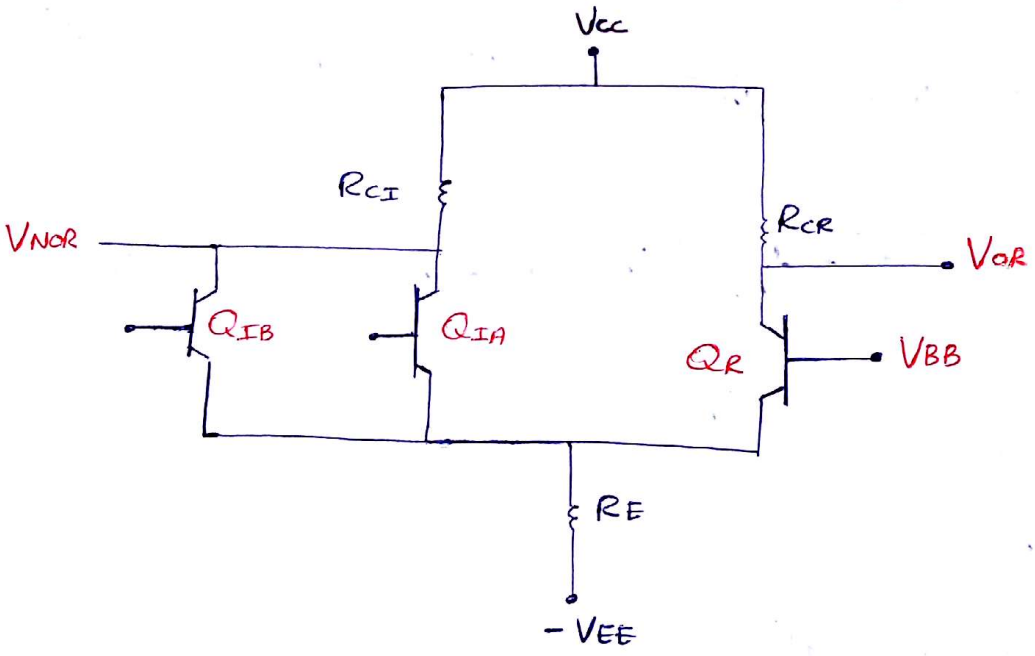
$= 3.4\,V$

* Q_R has fixed input at Base ⇒ does not saturate

* ADVATAGES OF ECL Switch

1. Low sensitivity to noise because of the differential nature of the circuit
2. Current drawn from power supply is constant during switching
3. O/p is referenced to Vcc, and if Vcc is replaced with ground with decreasing VEE, o/p will be more stable.

11.4 Basic ECL NOR/OR Gate



* Any input high

Corresponding Q_I is on, current flows in R_{cI}, Q_R is off

V_{NOR} low, V_{OR} high

* All inputs low

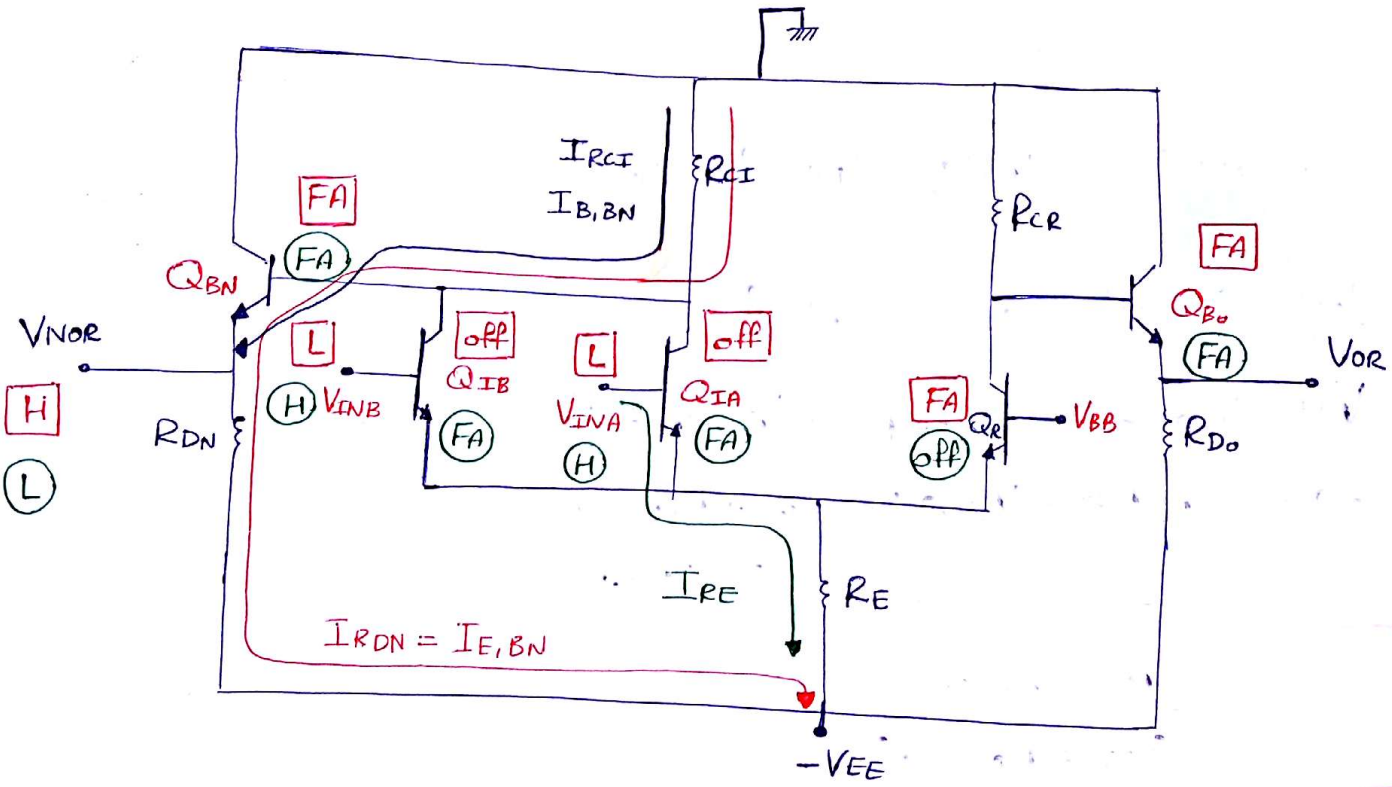
Q_I's are off, Q_R is on, $I_{RCI} = 0$

V_{NOR} high, V_{OR} low

A	B	NOR	OR
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

11.5 (M)ECLI NOR/OR Gate with Buffers

motorolla



→ Buffers :- Q_{BN}, Q_{Bo} alway FA

* Provide high o/p current and low o/p resistance → FAN-OUT high

* Do not saturate ⇒ time-delay is low for some ECL cct's instant.

* High switching capability

* o/p at current shitch is level shifted by $V_{BE,BN}$ (ECL) so that inputs & outputs are compatible

* DISADVANTAGES

→ High power dissipation

→ Large current spikes, with the decreased switching time

↳ Vcc is replaced by GND, and power supplies NOR H & OR L buffers are isolated from rest of the circuit

11.6 MECL I Voltage Transfer ch.

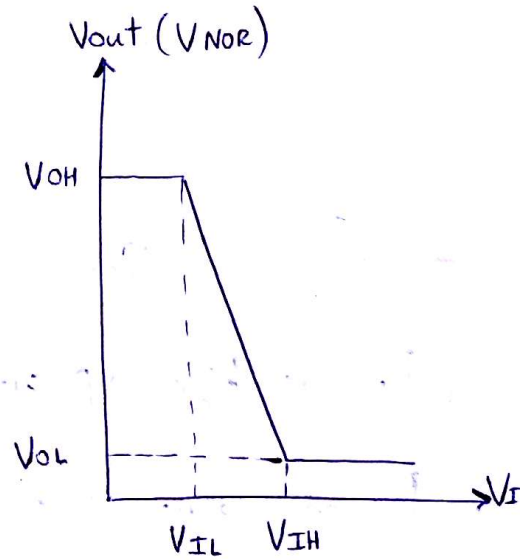
* V_{OH} Q_I off, Q_R on (input low)

$$V_{OH} = V_{NOR} = 0 - I_{B,BN} R_{CI} - V_{BE,BN}(ECL)$$

$$-0 + I_{B,BN} R_{CI} + V_{BE,BN} + I_{E,BN} R_{DN} - V_{EE} = 0$$

$$I_{E,BN} = (1+\beta_F) I_{B,BN}$$

$$I_{B,BN} = \frac{V_{EE} - V_{BE,BN}}{R_{CI} + R_{DN}(1+\beta_F)}$$



* V_{IL}, V_{IH}

Like for current switch

$V_{IL} = V_{BB} - 0.05$

$V_{IH} = V_{BB} + 0.05$

* V_{OL} input high Q_I on, Q_R off

Ignore $I_{B,BN} \Rightarrow I_{RCI} \approx I_{RE}$

$$I_{RE} = \frac{V_{IN} - V_{BE,I} + V_{EE}}{R_E}$$

$V_{IN} \rightarrow V_{IH}$

$$V_{OL} = V_{NOR} = 0 - I_{RE} R_{CI} - V_{BE,BN}(ECL)$$

* V_S when Q_I saturates

$$V_S = \frac{V_{BC(sat)} + \frac{R_{CI}}{R_E}\left[V_{BE(sat)} - V_{EE}\right]}{1 + \frac{R_{CI}}{R_E}}$$

$$V_{B,BN} = V_{IN} - V_{BC,I(sat)}$$

$$V_{NOR}(V_S) = V_{B,BN} - V_{BE,BN}(ECL)$$

$$= V_S - V_{BC,I(sat)} - V_{BE,BN}(ECL)$$

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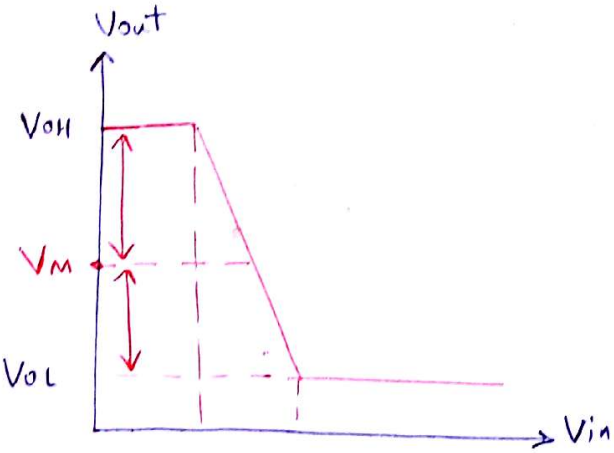
* Noise sensitivity :- quantifies the effects of input variations

$$NSH = V_{OH} - V_m$$

$$NSL = V_M - V_{OL}$$



* Noise immunity :- $\frac{\text{sensitivity}}{\text{Logic swing}}$

$$NIH = \frac{NSH}{LS}$$

$$NIL = \frac{NSL}{LS}$$

$$LS = V_{OH} - V_{OL}$$

ex 11.2 Find LS, noise margins, noise immunities

$V_{BB} = -1.175\ V$, $V_{OH} = -0.76\ V$, $V_{OL} = -1.55\ V$

$V_{IL} = -1.225\ V$, $V_{IH} = -1.125\ V$, $V_S = -0.29\ V$

→ $LS = -0.76 - -1.55 = 0.79\ V$

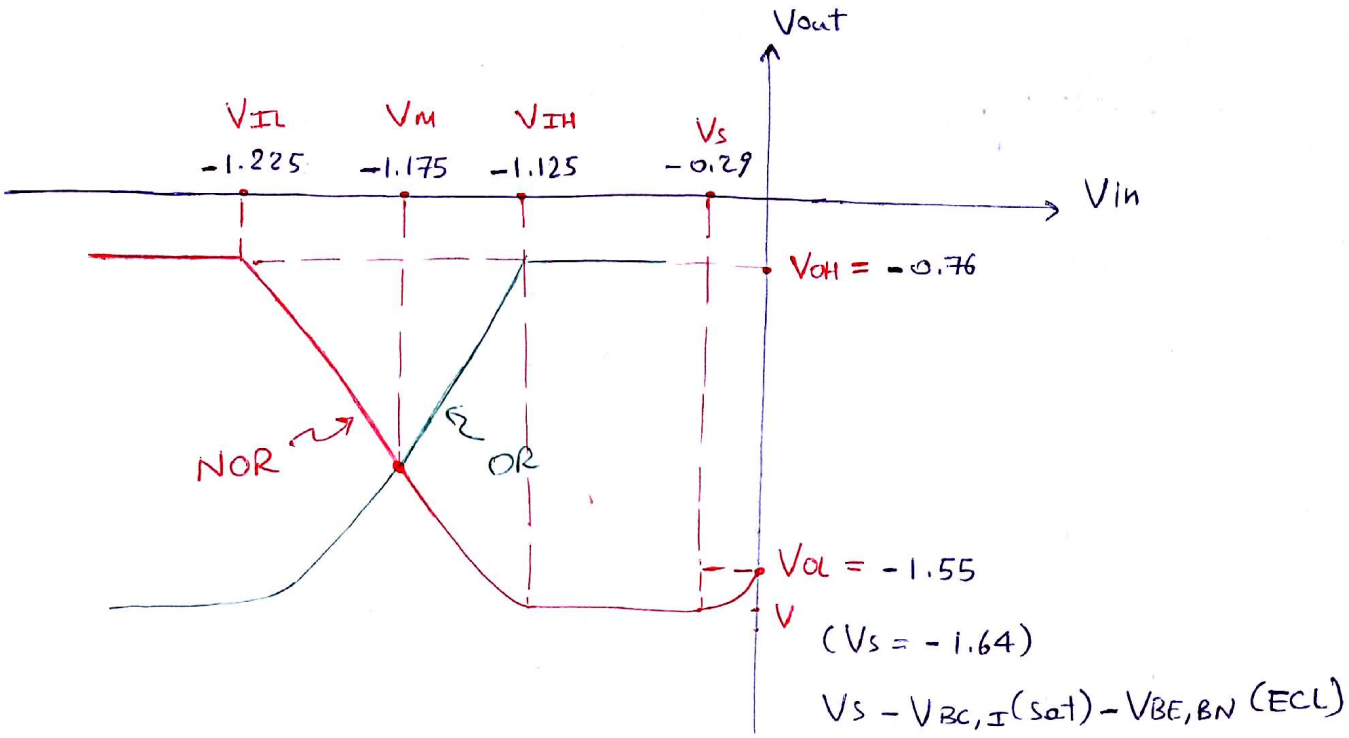
→ $NMH = -0.76 - -1.125 = 0.365\ V$

→ $NML = -1.225 - -1.55 = 0.325\ V$

→ $NIH = \frac{-0.76 - -1.175}{0.79} = 0.53\ V$

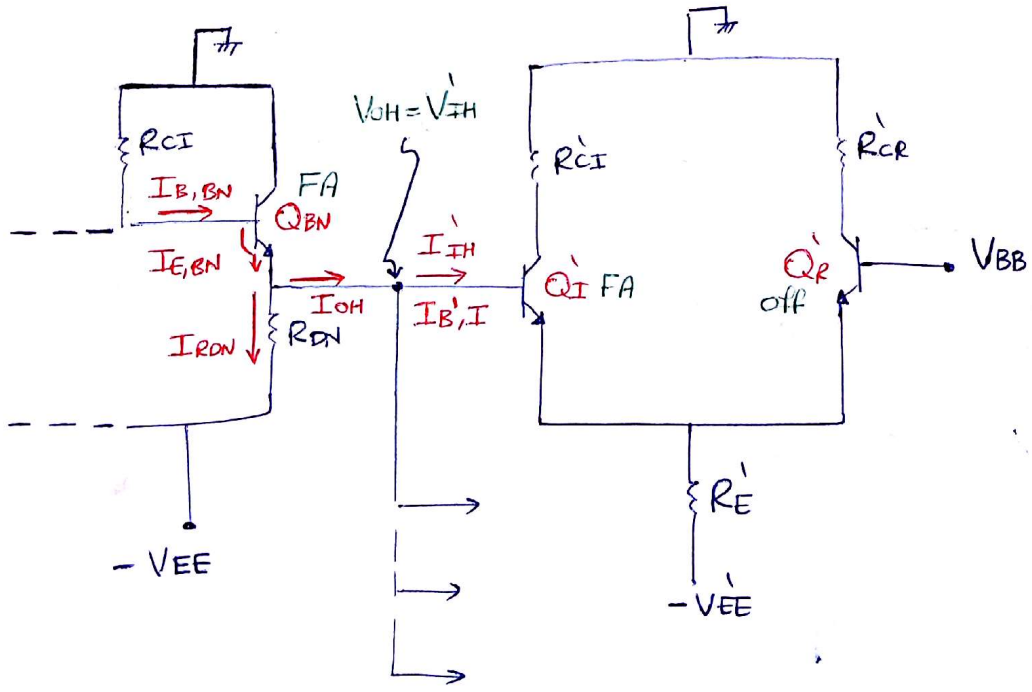
→ $NIL = \frac{-1.175 - -1.55}{0.79} = 0.475\ V$

$V_{BB} = V_M$



11.7 MECLI Fan-out

* Output at NOR Driver, input at Q_I'
* During low input, no current in $Q_I' \Rightarrow$ fan-out $\approx \infty$ not acceptable



$$I_{OH} = I_{E,BN} - I_{RDN}$$

$$I_{E,BN} = I_{B,BN}(\beta_F + 1)$$

$$I_{B,BN} = \frac{0 - V_{BE,BN}(ECL) - (V_{OH})}{R_{CI}}$$

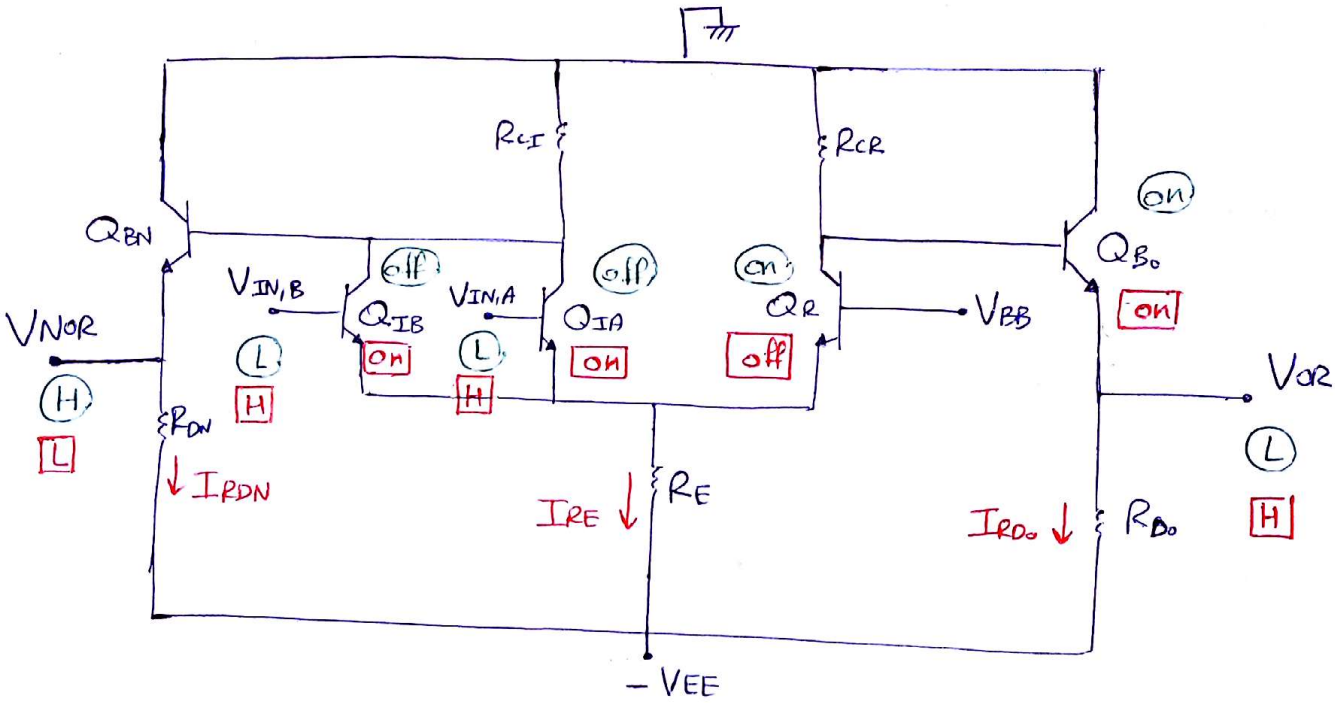
$$I_{RDN} = \frac{V_{OH} + V_{EE}}{R_{DN}}$$

$$I'_{IH} = I'_{B,I} = \frac{I'_{E,I}}{\beta_F + 1}$$

$$I'_{E,I} = I'_{RE} = \frac{V_{OH} - V'_{BE,I}(ECL) + V'_{EE}}{R_{E'}}$$

⇒ Unlike TTL, where drivers o/p sink the load current, and thus does not affect the outputs voltage, the ECL load drags current from the ECL's drivers, which decreases the drivers output voltage ⟹ voltage at output of drivers must be kept at V_{OH}

11.8 MECL Power Dissipation



* NOR High → (NOH)

Input low

$$I_{RD_o}(OH) = \frac{V_{OL} + V_{EE}}{R_{Do}}$$

$$I_{RE}(OH) = \frac{V_{BB} - V_{BE,R} + V_{EE}}{R_E}$$

$$I_{RDN}(OH) = \frac{V_{OH} + V_{EE}}{R_{DN}}$$

$$I_{EE}(OH) = \sum I_S$$

* NOR Low (NOL)

$$I_{RD_0}(OL) = \frac{V_{OH} + V_{EE}}{R_{D_0}}$$

$$I_{RE}(OL) = \frac{V_{IH} - V_{BE,I}(ECL) + V_{EE}}{R_E}$$

$$I_{RDN}(OL) = \frac{V_{OL} + V_{EE}}{R_{DN}}$$

$$I_{EE}(OL) = \Sigma I_S$$

$$\Rightarrow P_{EE}(avg) = V_{EE} * \frac{I_{EE}(OL) + I_{EE}(OH)}{2}$$

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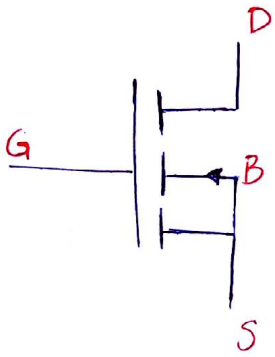
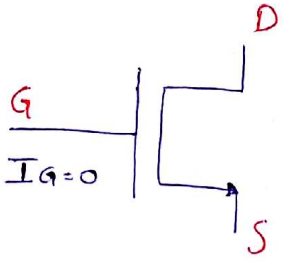
CH. 16 Metal Oxide Semiconductor FET

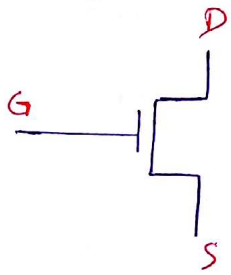
N-channel MOSFET

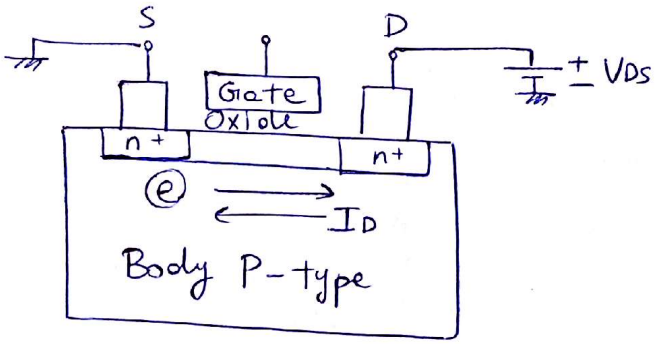
16.3 Modes of operation

N- CHANNEL

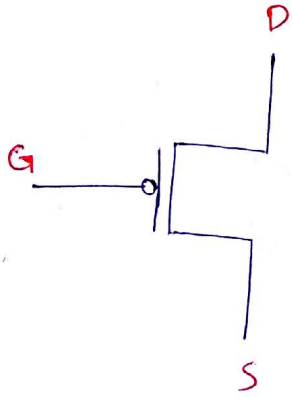


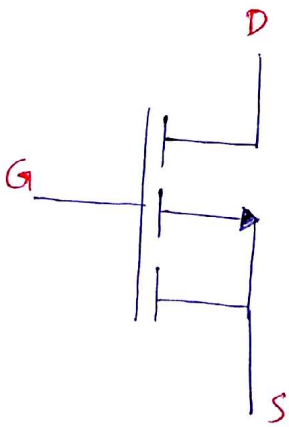


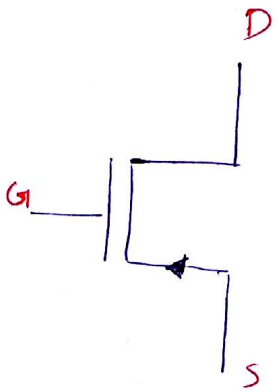




P- CHANNEL







* N-channel

Threshold Voltage

$V_{GS} > V_{TN}$, $V_{DS} > 0$ for current to flow from drain to source

① Cut-off

$V_{GS} < V_{TN}$, $I_D = 0$

② Linear mode

$V_{GS} > V_{TN}$, $V_{DS} < V_{DS(sat)}$

$V_{DS} < V_{GS} - V_{TN}$

bias

$\Rightarrow I_{D(lin)} = K\left[(V_{GS} - V_{TN}) * V_{DS} - \frac{V_{DS}^2}{2}\right]$, K: transconductance parameter

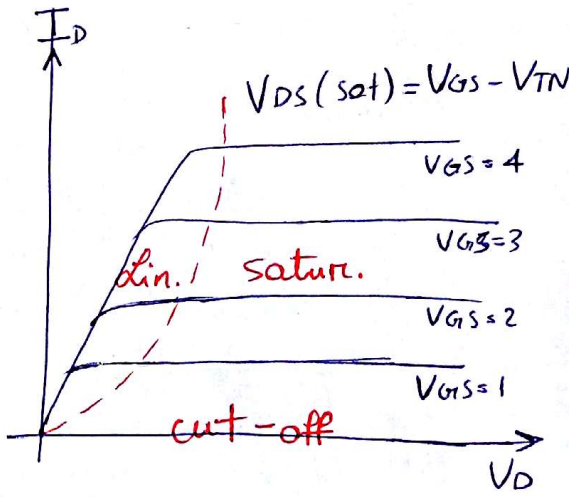
③ Saturation mode

$V_{GS} > V_{TN}$

$V_{DS} \geq V_{DS(sat)}$

$V_{DS} \geq V_{GS} - V_{TN}$

$I_{D(sat)} = \frac{K}{2}(V_{GS} - V_{TN})^2$



16.4 MOSFET Transconductance

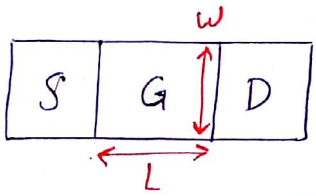
$$K = \mu C_{ox}' \frac{W}{L}$$

* μ : mobility

* C_{ox}' : capacitance for oxide

$$K' = \mu C_{ox}'$$

→ W, L : width & length of gate



enhancement : $V_{TN}+W$

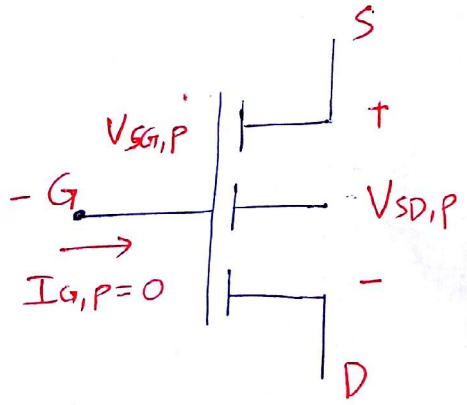
depletion : $V_{TN}-W$

$$C_{ox}' = \frac{\epsilon_{ox}}{t_{ox}}$$

* ϵ_{ox} : permittivity for oxide

* t_{ox} : thickness

16.6 P-channel MOSFET



① Cut-off mode

$V_{SG,P} < -V_{T,P}$

$V_{T,P}$: enhancement -ve

depletion +ve

$I_{D,P}(off)=0$

② Linear mode

$$V_{SG,P} \geq -V_{T,P}$$

$$V_{SD,P} < \underbrace{V_{SG,P} + V_{TP}}_{\rightarrow V_{SD,P(sat)}}$$

$$I_{D,P(lin)} = K_P \left[(V_{SG,P} + V_{TP}) V_{SD,P} - \frac{V_{SD,P}^2}{2} \right]$$

③ Saturation mode

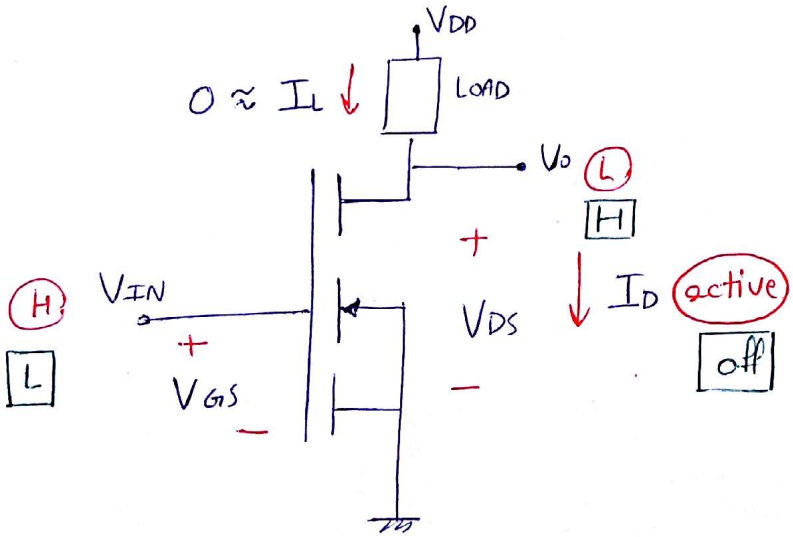
$$V_{SG,P} \geq -V_{T,P}$$

$$V_{SD,P} \geq \underbrace{V_{SG,P} + V_{T,P}}_{V_{SD,P(sat)}}$$

$$I_{D,P(sat)} = \frac{K}{2} (V_{SG,P} + V_{T,P})^2$$

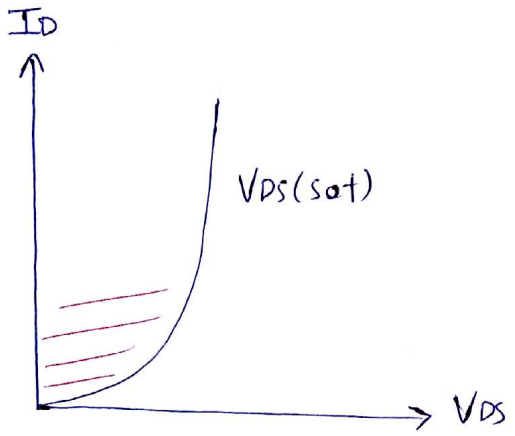
CH. 17 Introduction to MOSFET Digital Circuits

General NMOS inverter



$V_{IN} = V_{GS}$
$V_{out} = V_{DS}$
$I_D = I_L$
} VTC

17.2 Zero Drain Current active MOSFET



↝ V_{DS} small but +ve

↝ $I_D \approx 0$ $V_{DS} < V_{DS(sat)}$
active

↝ $V_{DS} < V_{GS} - V_T$

↝ $V_{DS} > 0 \longrightarrow V_{GS} - V_T > 0 \longrightarrow V_{GS} > V_T \Rightarrow$ ON in active mode

* By increasing the value of R_L, $I_D \approx 0$ and transistor is in active mode if V_{GS} large enough.

•• Analytically ••

$$I_{D(lin)} = K\left[(V_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$0 = K[\quad\quad\quad\quad\quad\quad\quad\quad]$$

when $V_{DS} = 0$, $I_D = 0$ solution ① ✓

$V_{DS} = 2(\underbrace{V_{GS} - V_{TN}}_{\hookrightarrow V_{DS(sat)}})$ solution ② X

$V_{DS} > 2\,V_{DS(sat)}$ does not apply

ex 17.1 Find the resistance of D-S channel (R_{DS}) for $V_{GS} = 5V$, $V_{TN} = 1V$, $K = 40\ \mu A/V^2$ & when

V_{DS} = (a) 3V
(b) 0V

(a) $V_{DS} = 3V$

$$I_D = K\left[(V_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$R_{DS} = \frac{dV_{DS}}{dI_D}$$

$$\frac{dI_D}{dV_{ds}} = K\left[(V_{GS} - V_{TN}) - V_{DS}\right]$$

$$R_{DS} = \frac{1}{K\left[(V_{GS} - V_{TN}) - V_{DS}\right]}$$

$$R_{DS}\Big|_{V_{DS}=3} = \frac{1}{40\mu[(5-1)-3]} = 25\ K\Omega$$

(b) $V_{DS} = 0\ V$

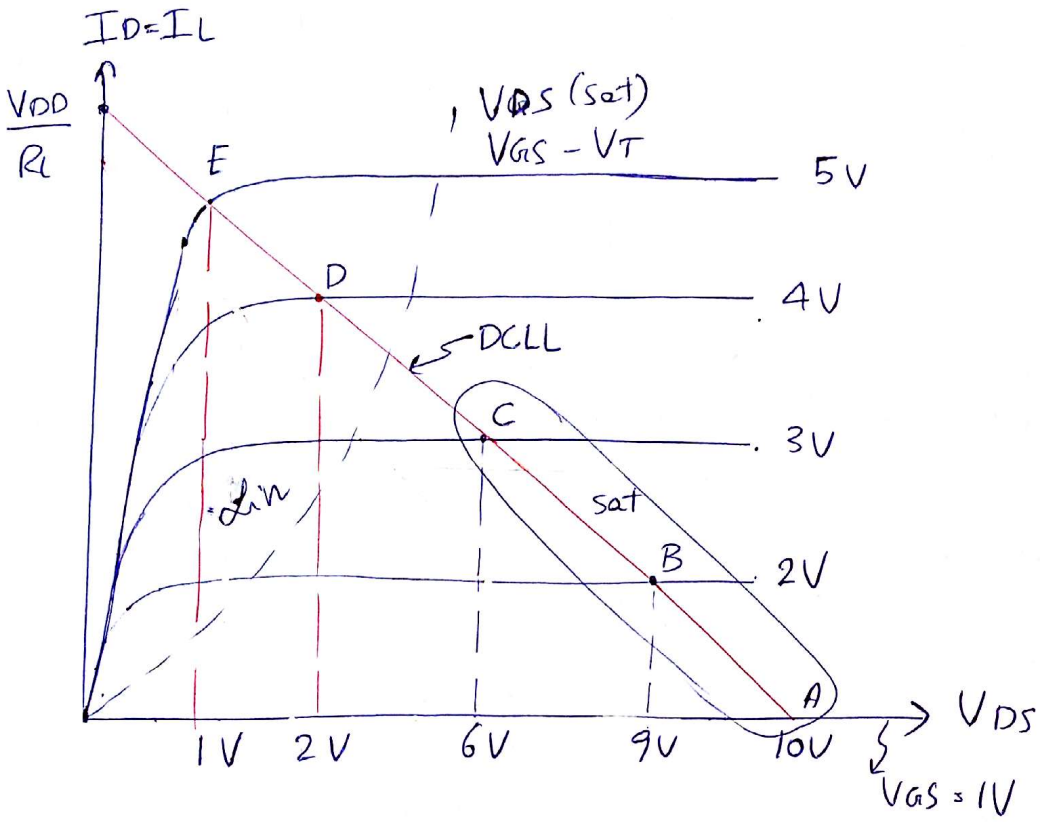
$$R_{DS}\Big|_{V_{DS}=0V} = \frac{1}{40\mu\left[(5-1)-0\right]} = 6.25\ K\Omega$$

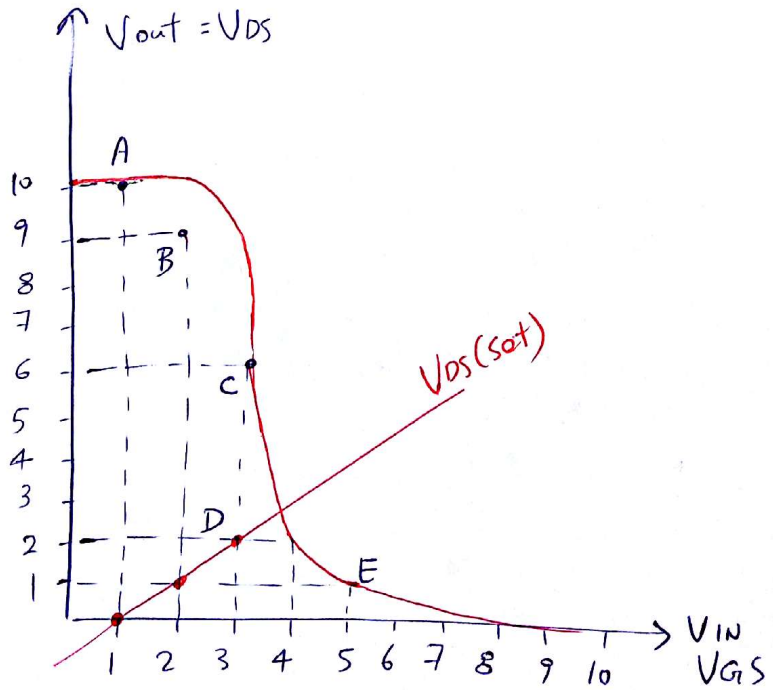
* As V_{DS} decreases, R_{DS} decreases and MOSFET conductance increases ⇒ for higher conductivity, less V_{DS} is used.

→ NMOS is used as a pull-down circuit.

ex 17.2 $V_{DD}=10V$, $R_L=1K\Omega$, $K_o=2mA/V^2$, $V_T=1$

Draw VTC.



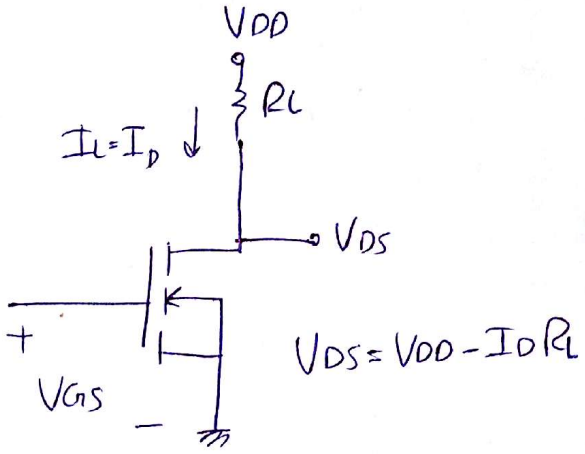


~~VDD~~

$$I_D = \frac{V_{DD} - V_{DS}}{R_L}$$

@ $V_{DS} = 0 \rightarrow I_D = \frac{V_{DD}}{R_L}$

@ $I_D = 0 \rightarrow V_{DS} = V_{DD}$



$V_{DS} = V_{DD} - I_D R_L$

Lin : $I_D(lin)$, V_{DS} } solve for both variable $V_{GS} = 1$, $V_{DS} = 0$

$V_{GS} = 2$, $V_{DS} = 1$

$V_{GS} = 3$, $V_{DS} = 2$

Sat : $I_D(sat) \Rightarrow$ find V_{DS}

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* Partial differential of an NMOS I_D expression

ex 17.4 for a linear mode

$$I_D(lin) = K\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$dI_D(V_{GS}, V_{DS}) = \frac{dI_D}{dV_{GS}} dV_{GS} + \frac{dI_D}{dV_{DS}} dV_{DS} \rightarrow \text{to know the slope}$$

$$\frac{dI_D}{dV_{GS}} = K V_{DS}$$

$$\frac{dI_D}{dV_{DS}} = K\left[(V_{GS} - V_T) - V_{DS}\right]$$

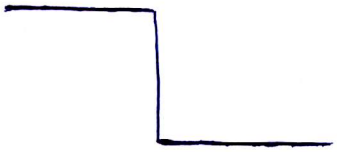
$$dI_D(V_{GS}, V_{DS}) = K V_{DS}\, dV_{GS} + K\left[V_{GS} - V_T - V_{DS}\right] dV_{DS}$$

17.6 Power Dissipation

* high load resistance → low current → low power dissipation

* MOSFET ccts have the lowest power dissipation amongst all digital circuits.

* Static Power Dissipation (avg) [H, L]



$$P_{D(avg)}_{stat} = V_{DD} \frac{I_{DD(OH)} + I_{DD(OL)}}{2}$$

* Dynamic Power Dissipation (avg) [transient P_D - between H & L]

In BJT is neglected, because it is small compared to P_{D}_{stat}

$$P_{D,dyn} = C_L \, \nu \, V_{DD}^2$$

→ C_L : total load capacitance

→ ν : the frequency at which gate is switched (Hz)

$$P_{tot} = P_{dyn} + P_{stat}$$

ex 17.5 $V_{DD} = 5V$, $\nu = 0.5\,MHz$, $C_L = 10pF$, $I_{DD(OH)} = 5\mu A$

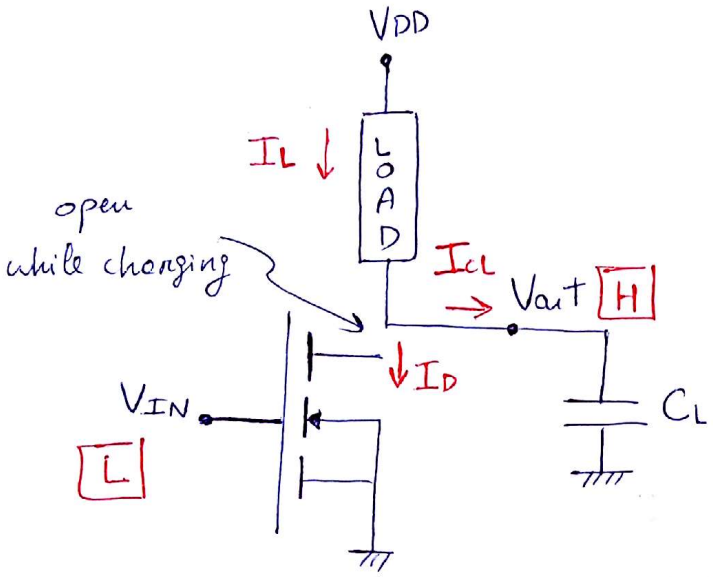
$I_{DD(OL)} = 100\mu A$. Find P_T

$$P_{DD(stat)} = \frac{100\mu + 5\mu}{2} \times 5 = 262\mu W$$

$$P_{dyn} = 10p \times 0.5M \times 25 = 125\mu W$$

$$P_T = 262\mu + 125\mu = 387\mu W$$

17.7 Fan-out



* Current at gate = 0
  → current can not restrict fan-out

* fan-out is restricted by propagation delay which is determined by C_L

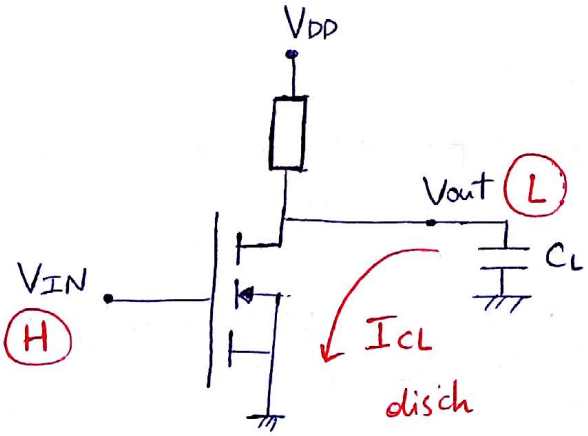
① During charging load (o/p L→H) (i/p H→L)

$$I_L = I_D = I_{CL} = C_L \frac{dV_{out}}{dt}$$

② During discharging of C_L (o/p H→L) (i/p L→H)

$$I_{CL} = C_L \frac{dV_{out}}{dt} = I_L - I_D$$

$$I_L < I_D \Rightarrow I_{CL} \text{ is -ve} \Rightarrow I_{CL} = -C_L \frac{dV_{out}}{dt}$$



linear conducting pull-down

ex 17.6 Find maximum C_L if $I_{CRG} = 50\mu A$, $I_{DISC} = -20\mu A$

$\Delta t = 1\mu s$, $V_{OL} = 0.5V$, $V_{OH} = 5V$

SOLUTION :-

$$I_c = C\frac{dV_{out}}{dt} \Rightarrow I_c = C\frac{\Delta V_{out}}{\Delta t}$$

$$dt = C\frac{dV_{out}}{I_c} \quad \text{assume low variation in } I_c$$

$$\int_{t_1}^{t_2} dt = \frac{C}{I_c}\int_{V_1}^{V_2} dV_{out} \rightarrow t\Big]_{t_1}^{t_2} = \frac{C}{I_c} V_{out}\Big]_{V_1}^{V_2}$$

$$\Delta t = \frac{C}{I_c}\Delta V_{out}$$

$$C = I_c\frac{\Delta t}{\Delta V_{out}}$$

$$\Rightarrow C_{CRG} = 50\mu * \frac{1\mu}{(5-0.5)} = 11.1\,pF$$

$$\Rightarrow C_{DISC} = -20\mu * \frac{1\mu}{(0.5-5)} = 4.44\,pF$$

CRG

* If we choose $C = 11.1\,pF$ then $\Delta t = \frac{11.1\times10^{-12}\times4.5}{50\times10^{-6}} = 1\mu s$

DISC

* If we choose $C = 11.1\,pF$ then $\Delta t = \frac{1.11\times10^{-11}}{-20\times10^{-6}}\times(-4.5) = 2.5\mu s$

∴ We can't use $C_L = 11.1\,pF$

* If we choose $C_L = 4.44\ pF$ then Δt at discharging will be 1 μs and at charging it will be even less.

$\Rightarrow$ $\boxed{C_L = 4.44\ pF}$ is the max C_L allowed

→ High-to-low transition limits the value of C_L, which is obvious since discharge current is less than the charge current

$\Rightarrow$ FAN-OUT :- is the max load capacitance that can be driven and mantain an acceptable switching time.

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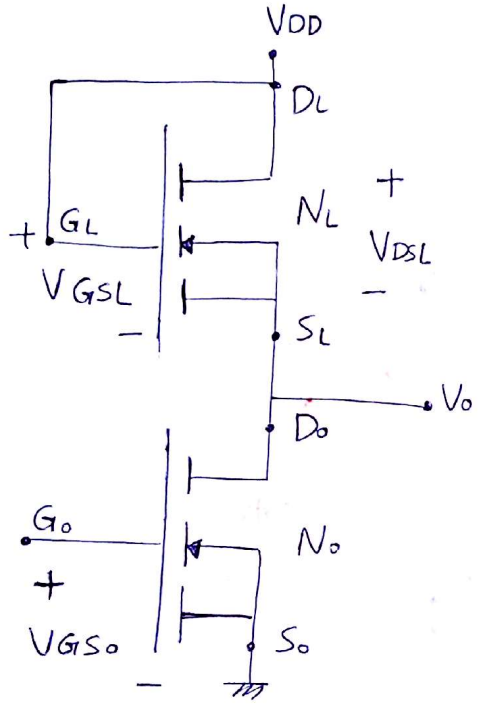
CH. 19 Saturation Enhancement only loaded NMOS Inverter



$V_{IN} = V_{GS,o}$

$V_{out} = V_{DS,o}$

$= V_{DD} - V_{DS,L}$

$V_{GS,L} = V_{DS,L}$

$V_{out} = V_{DD} - V_{GS,L}$

$V_{GS,L} > V_{GS,L} - V_{T,L}$

$V_{DS,L} > V_{GS,L} - V_{T,L}$

↳ $V_{DS,L}(sat)$

* N_L operates in the saturation region, no metter in what mode N_o is operating

19.1 – 19.3 NMOS Inverter VTC

* **V_{OH}** $V_{IN} < V_{T,o}$, N_o is off

$I_{D,o}(off) = I_{D,L}(sat) = 0$

$\frac{K_L}{2}(V_{GS,L} - V_{T,L})^2 = 0 \rightarrow V_{GS,L} = V_{T,L} = V_{DS,L}$

$V_{out} = V_{DD} - V_{GS,L} \rightarrow$ **$V_{OH} = V_{DD} - V_{T,L}$**

* V_{IL}

NOTE

MOSFET :-

V_{IN} → 1° sat , 2° lin

BJT :-

V_{IL} → 1° lin , 2° sat (FA)

at $V_{IN} = V_{T,0}$.

No turns to sat region and

$\boxed{V_{IL} = V_{T,0}}$ at edge of conductance

→ at $V_{IN} > V_{T,0}$

No is sat and N_L is sat

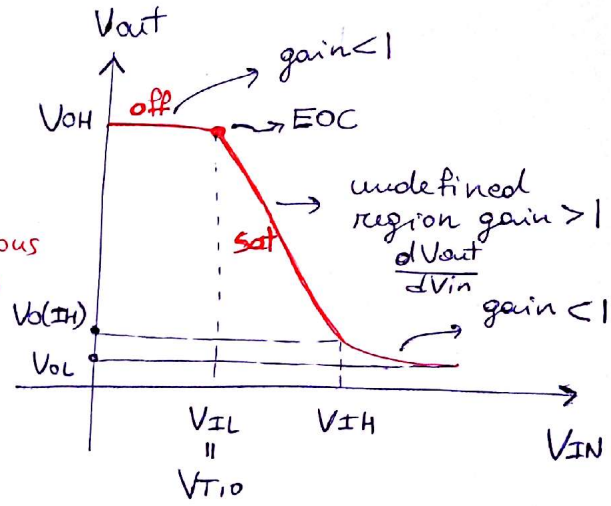
$$I_{D,L}(sat) = I_{D,0}(sat)$$

$$\frac{K_L}{2}(V_{GS,L} - V_{T,L})^2 = \frac{K_0}{2}(V_{GS,0} - V_{T,0})^2$$

$V_{GS,0} = V_{IN}$

$V_{GS,L} = V_{DS,L} = V_{DD} - V_{out}$ ← in the previous equation

بعد التعويض



$$\frac{K_L}{2}(V_{DD} - V_{out} - V_{T,L})^2 = \frac{K_0}{2}(V_{IN} - V_{T,0})^2$$

SOLVE FOR Vout

$$V_{out} = -\sqrt{\frac{K_0}{K_L}}\,V_{IN} + V_{T,0}\sqrt{\frac{K_0}{K_L}} + V_{DD} - V_{T,L}$$

↳ during transformation from [H] to [L]

* Output drops linearly with $-\sqrt{\frac{K_0}{K_L}}$
* The larger $\frac{K_0}{K_L}$, the steeper the transition is.

* V_M (middle voltage)

when $V_{IN} = V_{out} = V_M$ (No & N_L sat)

In one set $V_{IN} = V_{out} = V_M$ and solve for V_M

$$V_M = \frac{V_{DD} - V_{T,L} + V_{T,0}\sqrt{\frac{K_0}{K_L}}}{1 + \sqrt{\frac{K_0}{K_L}}}$$

* V_{IH} NL sat, No is linear.

$$I_{D,L}(sat) = \frac{K_L}{2}(V_{GS,L} - V_{T,L})^2$$

$$V_{GS,L} = V_{DD} - V_{out}$$

$$I_{D,0}(lin) = K_0\left[(V_{GS,0} - V_{T,0})V_{DS,0} - \frac{V_{DS,0}^2}{2}\right]$$

$$V_{GS,0} = V_{IN}$$
$$V_{DS,0} = V_{out}$$

$$\rightarrow I_{D,0}(lin) = K_0\left[(V_{IN} - V_{T,0})V_{out} - \frac{V_{out}^2}{2}\right]$$

$$\rightarrow I_{D,L}(sat) = \frac{K_L}{2}(V_{DD} - V_{out} - V_{T,L})$$

$$dI_{D,0} = \frac{dI_D}{dV_{IN}} * dV_{IN} + \frac{dI_D}{dV_{out}} * dV_{out} \quad \ldots (2)$$

$$dI_{D,L} = \frac{dI_D}{dV_{out}} * dV_{out} \quad \ldots (3)$$

Let (2) = (3) and solve for $\frac{dV_{out}}{dV_{in}}$

$$\frac{dI_{D,0}}{dV_{IN}} dV_{IN} = \frac{dI_{D,L}}{dV_{out}} * dV_{out} - \frac{dI_{D,0}}{dV_{out}} * dV_{out}$$

$$\Rightarrow \frac{dV_{out}}{dV_{IN}} = \left(\frac{dI_{D,0}}{dV_{IN}}\right) \Big/ \left(\frac{dI_{D,L}}{dV_{out}} - \frac{dI_{D,0}}{dV_{out}}\right) = -1$$

Substitute for the partial derivatives and solve for V_{out}

$$V_{out}(V_{IN}) = \frac{K_0 (V_{IN} - V_{T,0}) + K_L (V_{DD} - V_{T,L})}{2K_0 + K_L} \quad \text{... (4)}$$

(V_{IN} → V_{IH})

from quadratic equations, find another relation between V_{out} & V_{IN} and with eq. (4) solve for V_{out} & V_{IH}

$$V_{IH} = V_{T,0} + \frac{2(V_{DD} - V_{T,L})}{\sqrt{\frac{3K_0}{K_L} + 1}}$$

Use eq. (4) to find V_{out} at V_{IH}

* V_{OL} NL sat, No linear

$$I_{D,L}(sat) = I_{D,0}(lin)$$

$$I_{D,L}(sat) = \frac{K_L}{2}(V_{GS,L} - V_{T,L})^2 = K_0\left[(V_{GS,0} - V_{T,0})V_{DS,0} - \frac{V_{DS,0}^2}{2}\right] = I_{D,0}$$

$V_{GS,L} = V_{DD} - V_{out}$

$V_{GS,0} = V_{IN}$

$V_{DS,0} = V_{out}$

$V_I(high) \neq V_{IH}$

Let $V_I(high) = V_{OH}$ (previous stage)

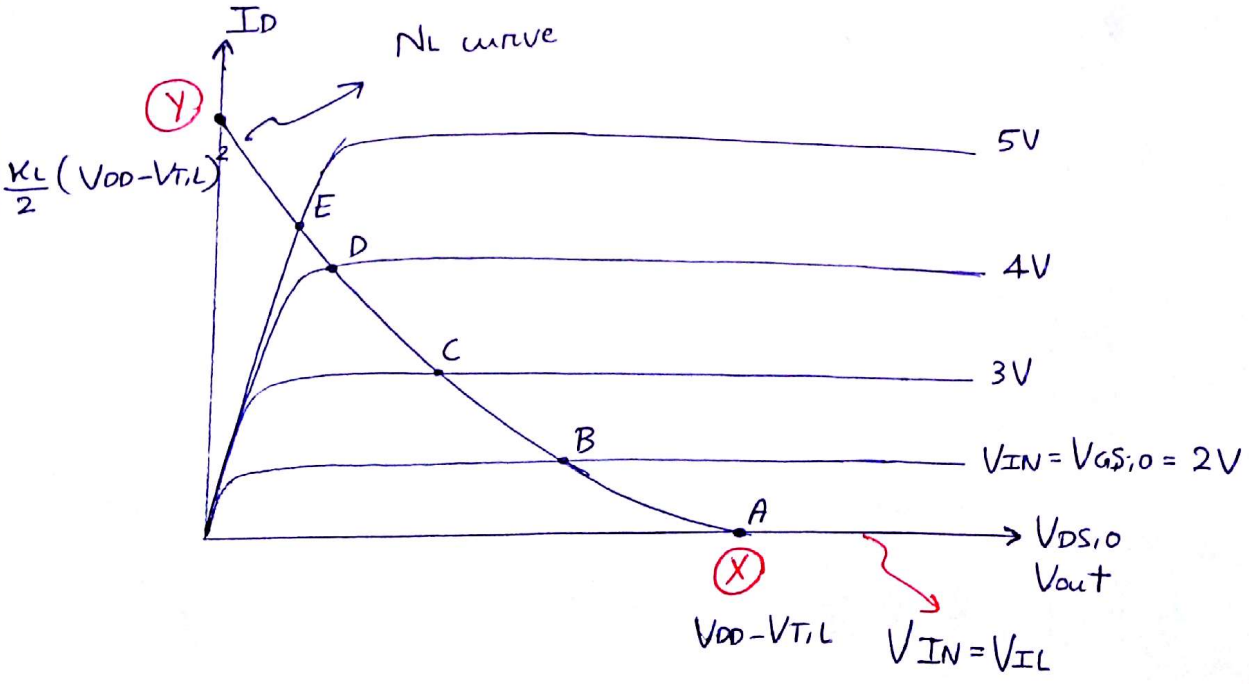
$= V_{DD} - V_{T,L}$

$\rightarrow V_{GS,0} = V_{IN} = V_{DD} - V_{T,L}$

then $V_{OL} = \dfrac{K_L(V_{DD} - V_{T,L})^2}{2K_L(V_{DD} - V_{T,L}) + 2K_0(V_{DD} - V_{T,L} - V_{T,0})}$

$V_I(V_{OL}) = V_{DD} - V_{T,L}$

Graphical Solution



* at point (Y)

$V_{DS,0} = 0$

$I_{D,L}(sat) = \frac{K_L}{2}(V_{GS,L} - V_{T,L})^2$

$V_{GS,L} = V_{DD} - V_{DS,0} \Rightarrow V_{GS,L} = V_{DD}$

$I_{D,L}(sat) = I_{D,0} = \frac{K_L}{2}(V_{DD} - V_{T,L})^2$

* at point (X)

$I_D = 0 = I_{D,L}(sat)$

$0 = \frac{K_L}{2}(V_{GS,L} - V_{T,L})^2$

$V_{GS,L} = V_{T,L}$

$V_{DS,0} = V_{DD} - V_{GS,L} = V_{DD} - V_{T,L}$

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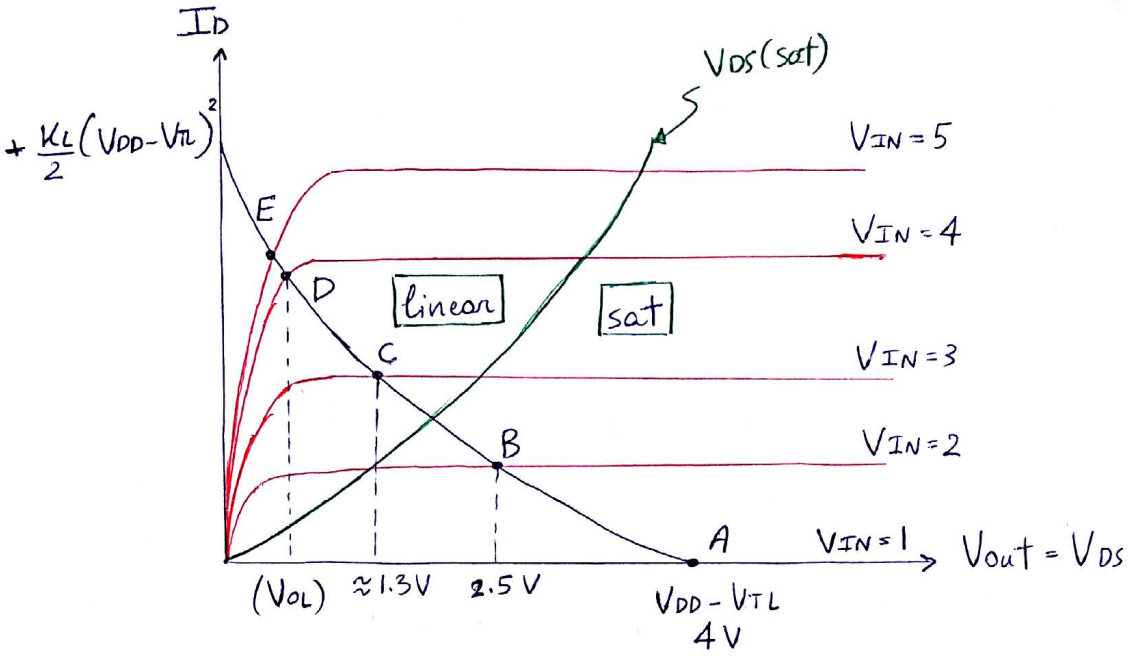
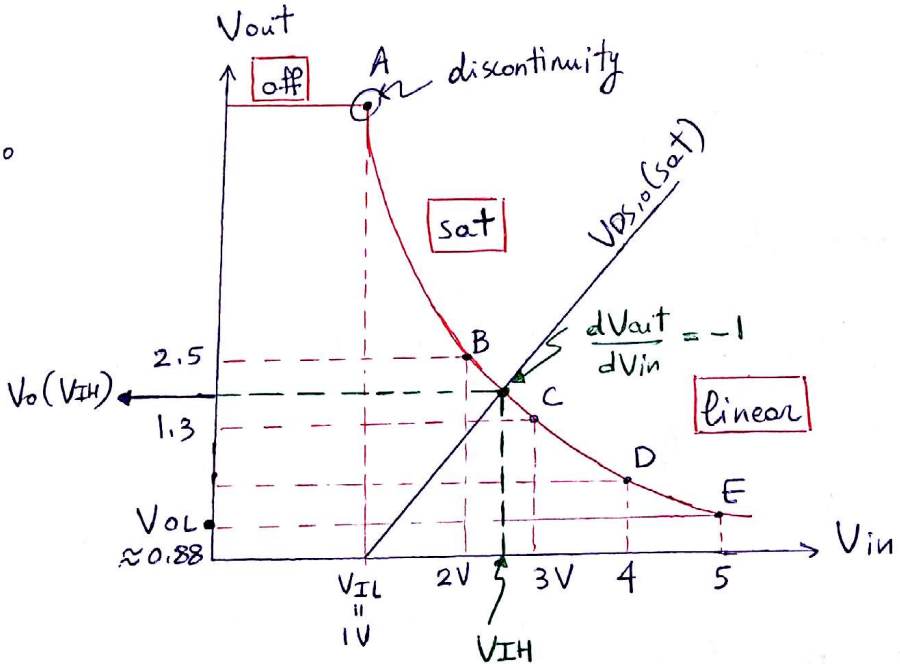


$V_{OH} = V_{DD} - V_{TL}$

$V_{OH} = 5 - 1 = 4\ V$

$V_{DS,o}(sat) = V_{GS,o} - V_{T,o}$



$V_o(V_{IL})$

$HNM = V_{OH} - V_{IH}$

$LNM = V_{IL} - V_o(V_{IH})$

19.5 Power Dissipation

* $I_{DD(OH)}$ N_O (off), N_L (sat)

$$I_{DD(OH)} = I_{D,L}(sat) = I_{D,O}(off) = 0$$

* $I_{DD(OL)}$ N_L (sat), N_O (lin)

$$I_{DD(OL)} = I_{D,L}(sat) = I_{D,O}(lin)$$

$$= K_O\left[(V_{GS,O} - V_{T,O})V_{DS,O} - \frac{V_{DS,O}^2}{2}\right]$$

$$\Rightarrow P_{DD,stat} = \frac{I_{DD(OH)} + I_{DD(OL)}}{2} V_{DD} = \frac{I_{DD(OL)}}{2} V_{DD}$$

$$\Rightarrow P_{DD,dyn} = C_L \nu V_{DD}^2$$

* read example 19.3

ex 19.1 find critical points $V_{DD} = 10V$, $\left(\frac{W}{L}\right)_O = \frac{10\mu m}{5\mu m}$

$\left(\frac{W}{L}\right)_L = \frac{5\mu m}{15\mu m}$, $k' = 20\,\mu A/V^2$ $V_T = 1.2V$ for N_O & N_L

$$\Rightarrow K = k'\frac{W}{L}$$

$$K_O = \frac{10}{5} \times 20\,\mu A/V^2 = 40\,\mu A/V^2$$

$$K_L = \frac{5}{15} \times 20\,\mu A/V^2 = 6.67\,\mu A/V^2$$

$$\Rightarrow \frac{K_O}{K_L} = 6$$

$V_{IL} = V_{T,0} = 1.2\ V$

$V_{OH} = V_{DD} - V_{T,L} = 10 - 1.2 = 8.8\ V$

$V_{OL} = 0.71\ V$

$V_{IH} = 4.6\ V$

$V_{O(IH)} = 2.25\ V$

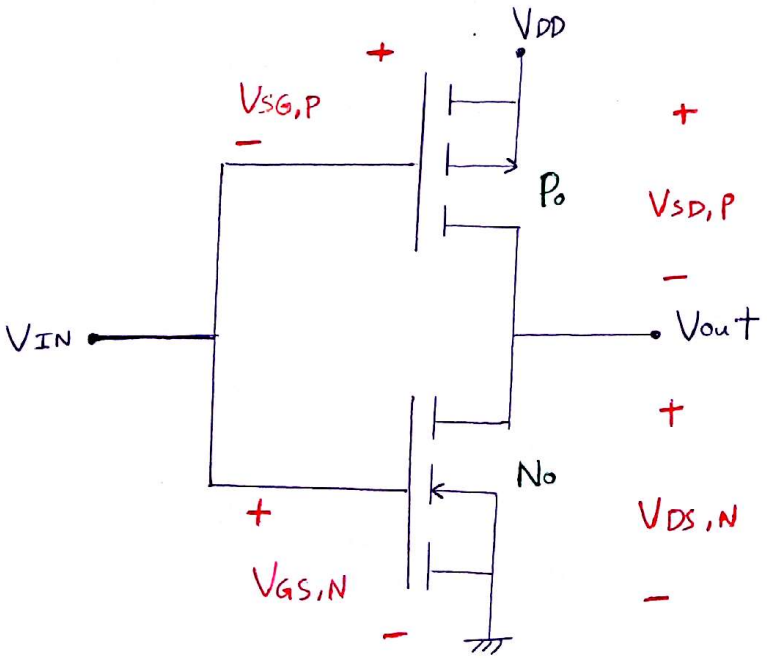
$V_M = 3.4\ V$

} from derived equations

CH. 23

23.1 CMOS Inverter

complementary



* $V_{IN} = V_{GS,N}$
* $V_{SG,P} = V_{DD} - V_{IN}$
* $V_{out} = V_{DS,N}$
* $V_{SD,P} = V_{DD} - V_{out}$

N → off sat lin

P → lin sat off

23.1 – 23.4 VTC

* V_{OH} input low at $V_{IN} = 0$

$V_{GS,N} = 0 < V_{TN} \rightarrow N_o$ is off

$V_{SG,P} = V_{DD} - \cancel{V_{IN}}^{0} = V_{DD} > -V_{TP}$

$V_{SD,P}(sat)$

$V_{SD,P} < V_{SG,P} + V_{TP} \rightarrow P_o$ is linear

$V_{DD} + V_{TP}$

$I_{D,P}(lin) = I_{D,N}(off) = 0$

$0 = K_P \left[(V_{SG,P} + V_{TP}) V_{SD,P} - \frac{V_{SD,P}^2}{2} \right]$

$V_{SD,P} = 0$

$V_{SD,P} = 2(V_{SG,P} + V_{TP})$ not applicable

* $V_{out} = V_{DD} - \cancel{V_{SD,P}}^{0} = V_{DD}$

* V_{OL} input high at $V_{IN} = V_{DD}$

$V_{GS,N} = V_{DD} \rightarrow N_o$ is linear

$V_{SG,P} = V_{DD} - V_{IN} = V_{DD} - V_{DD}$

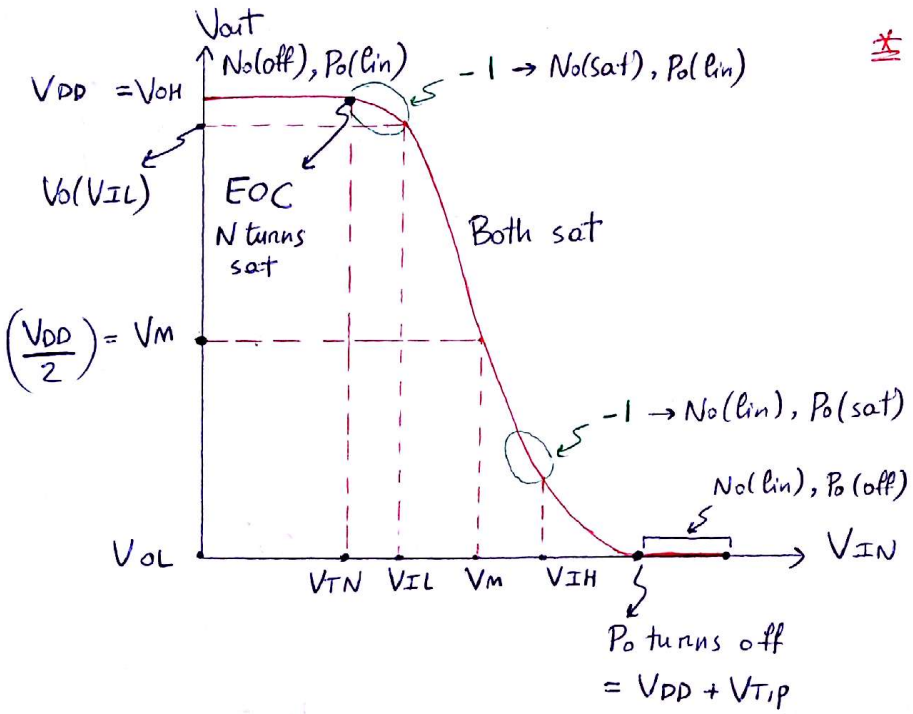
$V_{SG,P} < -V_{T,P} \rightarrow P_o$ is off

$I_{D,N}(lin) = I_{D,P}(off) = 0$

$K \left[(V_{GS,N} - V_{TN}) V_{DS,N} - \frac{V_{DS,N}^2}{2} \right] = 0$

$V_{DS,N} = 0$

* $V_{out} = V_{OL} = 0\ V$



* P turns off at $V_{SG} < -V_{T,P}$

$V_{DD} - V_{IN} < -V_{T,P}$

$\Rightarrow V_{IN} > V_{DD} + V_{T,P}$

* V_M mid point

$V_{IN} = V_{out} = V_M \rightarrow$ both sat

$I_{D,p}(sat) = I_{D,N}(sat)$

$$\frac{K_p}{2}\left[V_{SG,p} + V_{T,p}\right]^2 = \frac{K_N}{2}\left[V_{GS,N} - V_{T,N}\right]^2$$

$V_{SG,p} = V_{DD} - V_M$; $V_{GS,N} = V_M$

* $$V_M = \frac{V_{DD} + V_{TP} + V_{TN}\sqrt{\frac{K_N}{K_P}}}{1 + \sqrt{\frac{K_N}{K_P}}}$$

* V_{IL} N(sat), P(linear)

$$I_{D,N}(sat) = I_{D,P}(lin)$$

$$\frac{K_N}{2}\left[V_{GS,N} - V_{T,N}\right]^2 = K_P\left[(V_{SG,P} - V_{T,P})V_{SD,P} - \frac{V_{SD,P}}{2}\right]^2$$

$$\frac{K_N}{2}\left[V_{IN} - V_{T,N}\right]^2 = K_P\left[(V_{DD} - V_{IN} + V_{T,P})(V_{DD} - V_{out}) - \frac{(V_{DD} - V_{out})}{2}\right]$$

$$dI_{D,N}(V_{IN}) = dI_{D,P}(V_{IN}, V_{out})$$

$$dI_{D,N}(V_{IN}) = \frac{dI_{D,N}}{dV_{IN}} dV_{IN} \quad \cdots (1)$$

$$dI_{D,P}(V_{IN}, V_{out}) = \frac{dI_{D,P}}{dV_{IN}} dV_{IN} + \frac{dI_{D,P}}{dV_{out}} dV_{out} \quad \cdots (2)$$

$$\frac{dI_{D,N}}{dV_{IN}} dV_{IN} = \frac{dI_{D,P}}{dV_{IN}} dV_{IN} + \frac{dI_{D,P}}{dV_{out}} dV_{out} \Rightarrow (1) = (2)$$

$$\frac{dV_{out}}{dV_{IN}} = \frac{\frac{dI_{D,N}}{dV_{IN}} - \frac{dI_{D,P}}{dV_{IN}}}{\frac{dI_{D,P}}{dV_{out}}} = -1$$

$$\frac{dI_{D,N}}{dV_{IN}} - \frac{dI_{D,P}}{dV_{IN}} = -\frac{dI_{D,P}}{dV_{out}}$$

V_{IL} $\qquad$ $V_{out}(V_{IL})$

$$K_N(V_{IN} - V_{T,N}) - K_P(V_{DD} - V_{out}) = -K_P\left[-(V_{DD} - V_{IN} + V_{TP}) + (V_{DD} - V_{out})\right]$$

solve for V_{IL} =

$$\frac{2V_{out} - V_{DD} + V_{T,P} + \frac{K_N}{K_P} V_{T,N}}{1 + \frac{K_N}{K_P}}$$

and $V_{out}(V_{IL})$ is found from

$$I_{D,N}(sat) = I_{D,P}(lin)$$

$$\frac{K_N}{2}(V_{IN} - V_{T,N})^2 = K_P\left[(V_{DD} - V_{IN} + V_{TP})(V_{DD} - V_{out}) - \frac{(V_{DD} - V_{out})^2}{2}\right]$$

* V_{IH} P.(sat), N.(linear)

$$I_{D,P}(sat) = I_{D,N}(lin)$$

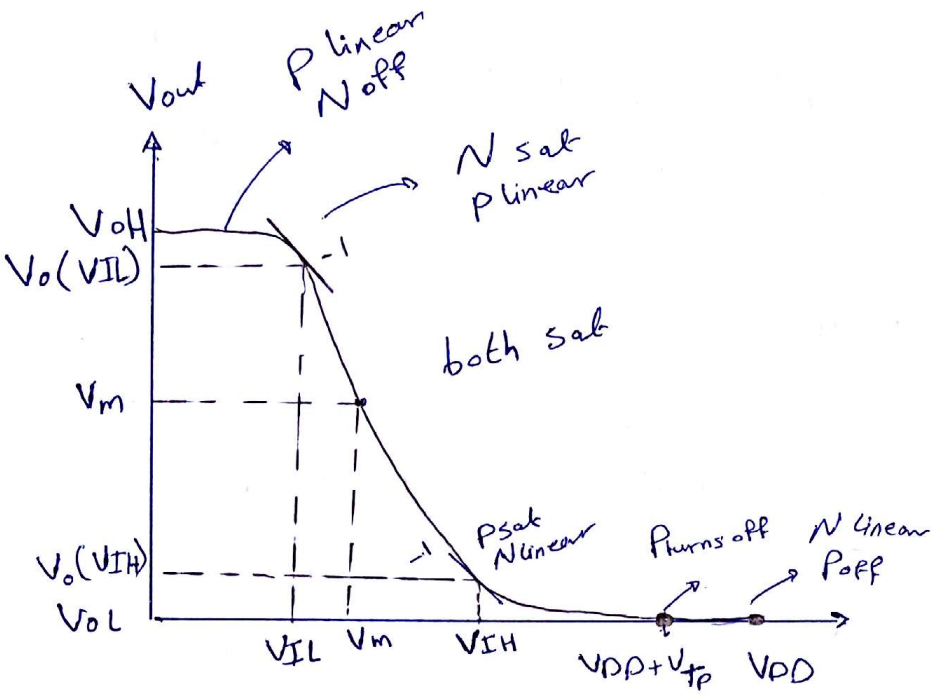
$$dI_{D,P}(sat) = dI_{D,N}(lin)$$

solve for V_{IH}, $V_{out}(V_{IH})$

$$V_{IH} = \frac{V_{DD} + V_{T,P} + \frac{K_N}{K_P}(V_{T,N} + 2V_{out})}{1 + \frac{K_N}{K_P}}$$

30/11/2016 الأربعاء

DIGITAL ELECTRONICS



For symmetry:

① $k_n = k_p$

$$\mu_n C_{ox}' \left(\frac{W}{L}\right)_N = \mu_p C_{ox}' \left(\frac{W}{L}\right)_P$$

$\mu_n = 580$

$\mu_p = 230$

$$580 \left(\frac{W}{L}\right)_N = 230 \left(\frac{W}{L}\right)_P$$

$$\Rightarrow \left(\frac{W}{L}\right)_P = 2.5 \left(\frac{W}{L}\right)_N$$

$$V_m - V_{IL} = V_{IH} - V_m$$

$$V_m = \frac{V_{DD}}{2}$$

Power dissipation

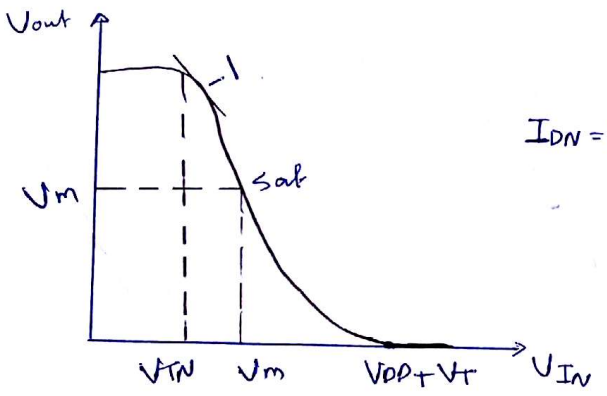
* Static power dissipation = 0

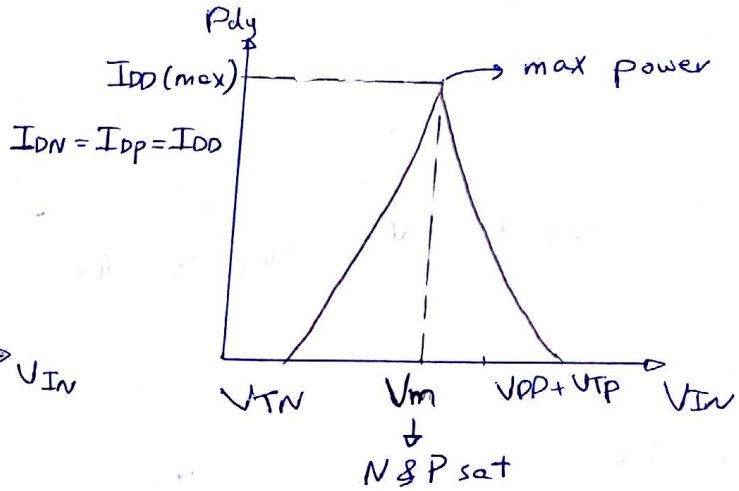
for OH, IL P lin, N off $I_D(OH) = 0$

for OL, IH P_{off}, N lin $I_D(OL) = 0$

$P_{stat} = 0$

$P_T = P_{dyn} = C_L V V_{DD}^2$





Example 23.3

design CMOS for symmetry (and check). $V_{DD} = 5$, $k_n' = 40 \frac{\mu A}{V^2}$, $k_p' = 16 \frac{\mu A}{V^2}$, $V_{TN} = 1$, $V_{TP} = 1$, $L_N = L_p = 2\mu m$, $W_n = 4\mu m$

$$\frac{W_p}{k_p} = 2.5 \frac{W_N}{L_N} = 2.5 \times 4\mu = 10\mu m$$

$$k_n = k_n' \left(\frac{W}{L}\right)_N = 40\mu \left(\frac{4}{2}\right) = 80 \frac{\mu A}{V^2}$$

$$k_p = k_p' \left(\frac{W}{L}\right)_p = 16\mu \frac{10}{2} = 80 \frac{\mu A}{V^2}$$

$$V_m - V_{IL} = V_{IH} - V_m$$

$$V_m = \frac{V_{DD}}{2} = 2.5\ V$$

$$V_m = \frac{5 + (-1) + 1\sqrt{\frac{80}{80}}}{1 + \sqrt{\frac{80}{80}}}$$

$$= 2.5\ V$$

$$V_{IL} = \frac{2\,V_{out}(V_{IL}) - 5(-1) + \frac{80}{80}(1)}{1 + \frac{80}{80}} = V_{out}(V_{IL}) - 2.5$$

$$\Rightarrow V_{out}(V_{IL}) = V_{IL} + 2.5$$

$$I_{Dp}(lin) = I_{DN}(sat)$$

$$K_L\{(V_{GS} + V_{TN})V_{DS} \cdots\cdots$$

$$\frac{80}{M}\left\{[5 - V_{IL} - 1][5 - (V_{IL} + 2.5) - \frac{5 - (V_{IL} + 2.5)^2}{2}\right\}$$

$$= \frac{80M}{2}[V_{IL} - 1]^2$$

$$\Rightarrow V_{IL} = 2.125\ V$$

$$V_{IH} = \frac{5 - 1 + \frac{80}{80}[1 + 2\,V_{out}(V_{IH})]}{1 + \frac{80}{80}}$$

$$V_{out}(V_{IH}) = V_{IH} - 2.5$$

$$I_{D_N}(lin) = I_{Dp}(sat)$$

$$I_{DN(lin)} = I_{Dp(sat)}$$

$$80M\left[(V_{IH}-1)(V_{IH}-2.5) - \frac{(V_{IH}-2.5)^2}{2}\right]$$

$$= \frac{80}{2} M \left[5 - V_{IH} - 1\right]^2$$

$$\Rightarrow V_{IH} = 2.875\,V$$

$$V_m - V_{IL} = 2.5 - 2.125 = 0.375$$

$$V_{IH} - V_m = 2.875 - 2.5 = 0.375$$

Fan out :-

Fan out depends on load capacitance allowed, and still has an acceptable propagation delay.

⇒ t_{pHL} : propagation delay when output "H → L" input "L → H".

* difference between input rising to 50% of max and output dropping to 50% of max.

⇒ t_{pLH} : time difference between input dropping to 50% and output rising to 50% of max

pull down N is ON

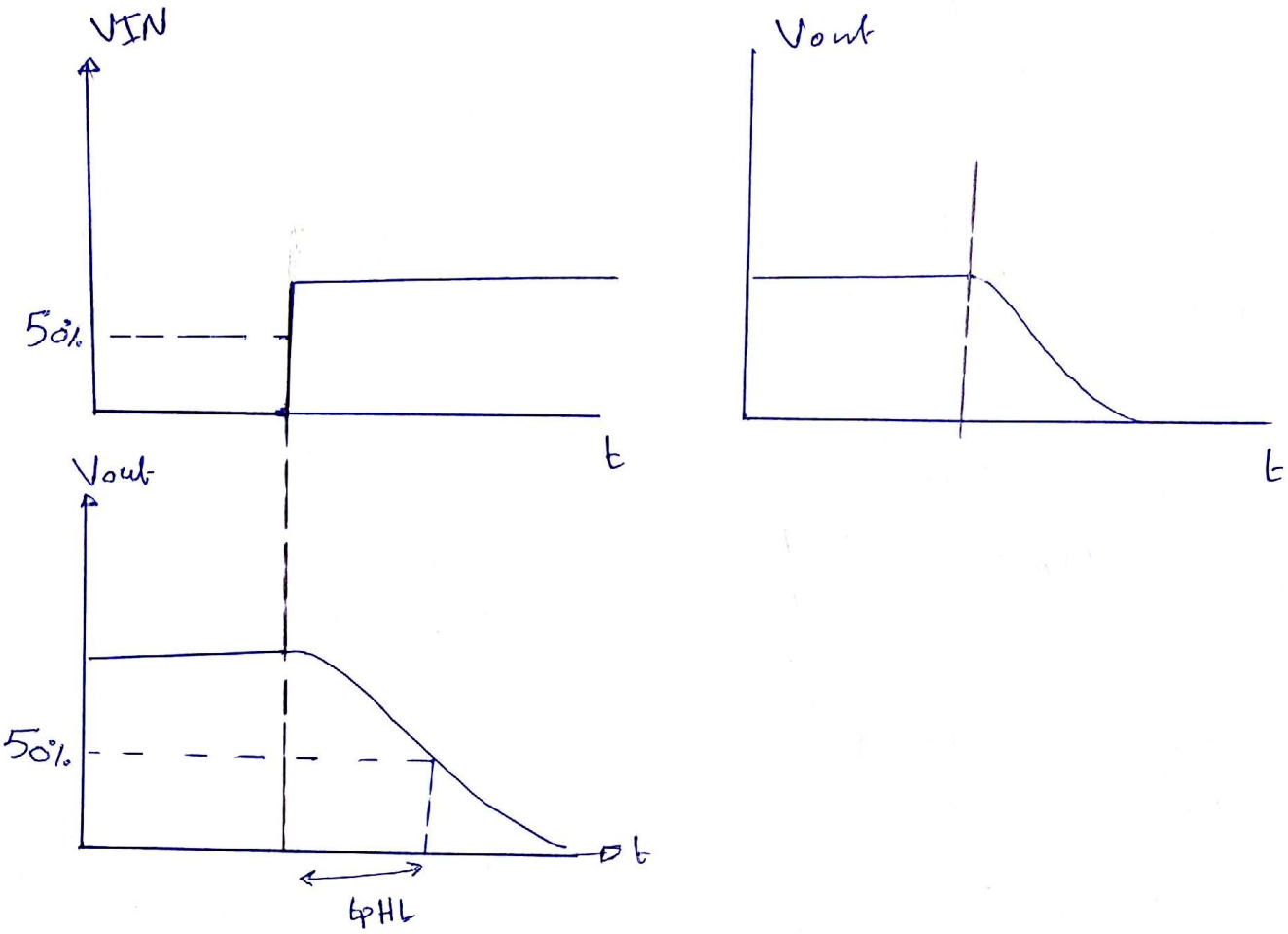
dis: t_{pHL} (o/p ↓) $= \left[\frac{2V_{TN}}{K_n(V_{DD}-V_{TN})^2} + \frac{1}{K_n(V_{DD}-V_{TN})} \ln\left(\frac{(1.5V_{DD}-2V_{TN})}{0.5V_{DD}}\right)\right] C_L$

pull up P is ON

ch: t_{pLH} (o/p ↑) $= \left[\frac{-2V_{TP}}{K_n(V_{DD}+V_{TP})^2} + \frac{1}{K_P(V_{DD}+V_{TP})} \ln\left(\frac{(1.5V_{DD}+2V_{TP})}{0.5V_{DD}}\right)\right] C_L$

find C_L from both equations and choose smaller one.

→ total capacitance of all loads.



FAN-OUT for symmetry

Capacitance for single load.

$$C_{IN}' = (W_N' L_N' + W_P' L_P') C_{ox}'$$

driver and load are identical.

$$C_L = F\, C_{IN} \quad \text{—①}$$

F ← Fan out

For symm. $\left(\frac{W}{L}\right)_P = 2.5 \left(\frac{W}{L}\right)_N$

For simplicity let $L_P = L_N$.

$$C_{IN} = (W_N L_N + 2.5\, W_N L_N) C_{ox}'$$

$$= 3.5\, W_N L_N C_{ox}'$$

$$t_N = t_P$$

$$t_N = \alpha_N C_{ox} \left(\frac{W}{L}\right) N \quad \text{—②}$$

deviide ① by ②

$$\frac{C_L}{K_N} = \frac{F\, C_{IN}}{\mu_n C_{ox}' \frac{W_N}{L_N}}$$

$$= \frac{F(3.5) W_N L_N C_{ox}'}{\mu_n C_{ox}' \frac{W_N}{L_N}}$$

$$\frac{C_L}{K_N} = \frac{3.5 L_N^2 F}{\mu_N}$$

$$\Rightarrow F = \frac{\mu_n}{3.5 L_N^2} \left(\frac{C_L}{K_N}\right)$$

→ From t_{pHL} equation

$$f = \frac{\mu_n t_p}{3.5 L^2 \left[\frac{2 V_{TN}}{(V_{DD} - V_{TN})^2} + \frac{1}{V_{DD} - V_{TN}} \ln\left(\frac{1.5 V_{DD} - 2V_{TN}}{0.5 V_{DD}}\right)\right]}$$

Cmos logic gate 24

Schmitt trigger 10

DA / AD converters ext

Multivibrators ext

RAM, ROM

Ch.31 Ch.32

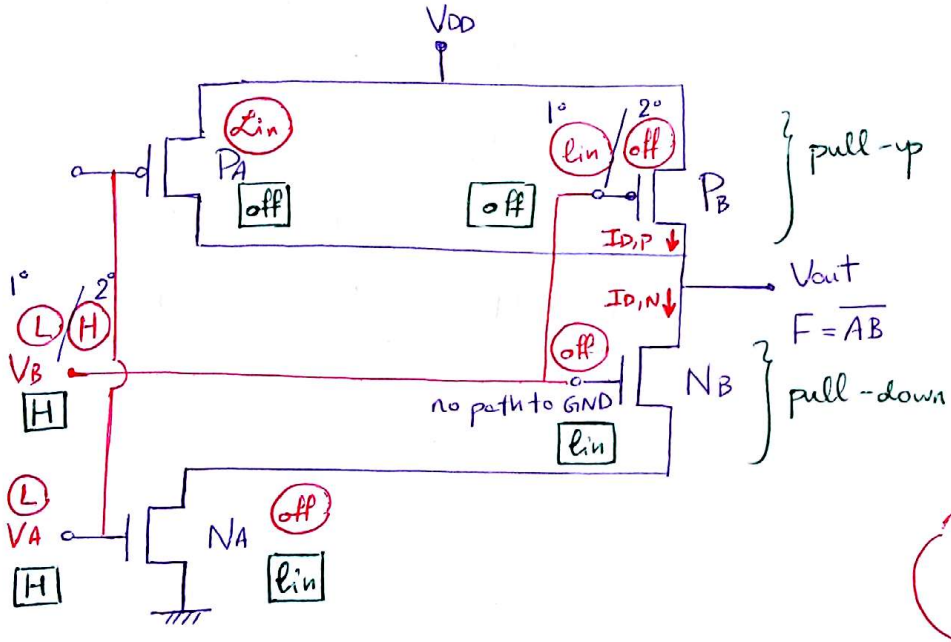
5/12/2016 الاثنين

DIGITAL ELECTRONICS

CH.24 CMOS Logic Gates

24.2 - 24.4 NAND, AND, OR, NOR + AOI

✳ NAND CMOS Gate



✳ NANDing : NMOS series
PMOS parallel

✳ NORing : NMOS parallel
PMOS series

NOTE: → P → bubble
→ N → without bubble

✳ Output high state

Any or both inputs low

① Both inputs low NA, NB off
PA, PB Lin.

$$I_{DPA} + I_{DPB} = 0 \Rightarrow V_{SD,P} = 0 \Rightarrow V_{out} = V_{OH} = V_{DD}$$

② Any input low : $V_A \rightarrow L$, $V_B \rightarrow H$

NA off , NB off (no path to ground)

PB off , PA lin $\Rightarrow I_{DPA}(lin) = 0 \Rightarrow V_{SDA} = 0 \Rightarrow V_{out} = V_{OH} = V_{DD}$

③ Any input low : $V_A \to H$, $V_B \to L$

P_A off , P_B lin $\Longrightarrow V_{SDP} = 0$

N_A floated , N_B off

$V_{out} = V_{OH} = V_{DD}$

④ All inputs high

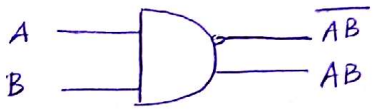
N_S lin , P_S off

$I_{DN} = I_{DP} = 0$

$V_{SDA} = 0 = V_{SDB}$

$V_{out} = V_{OL} = 0$

AND / NAND



A	B	$V_{o,NAND}$	$V_{o,AND}$
L	L	H	L
L	H	H	L
H	L	H	L
H	H	L	H

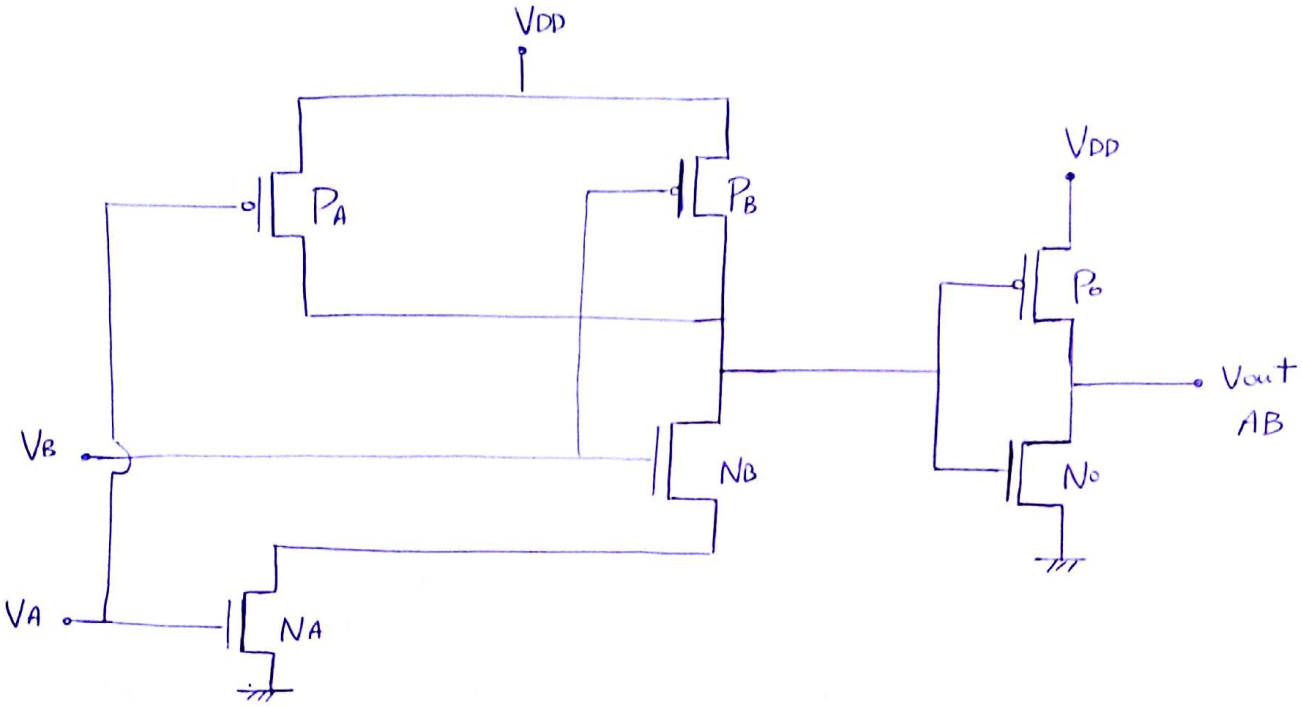
→ For summary

① Single input $\frac{W_P}{L_P} = 2.5 \frac{W_N}{L_N}$

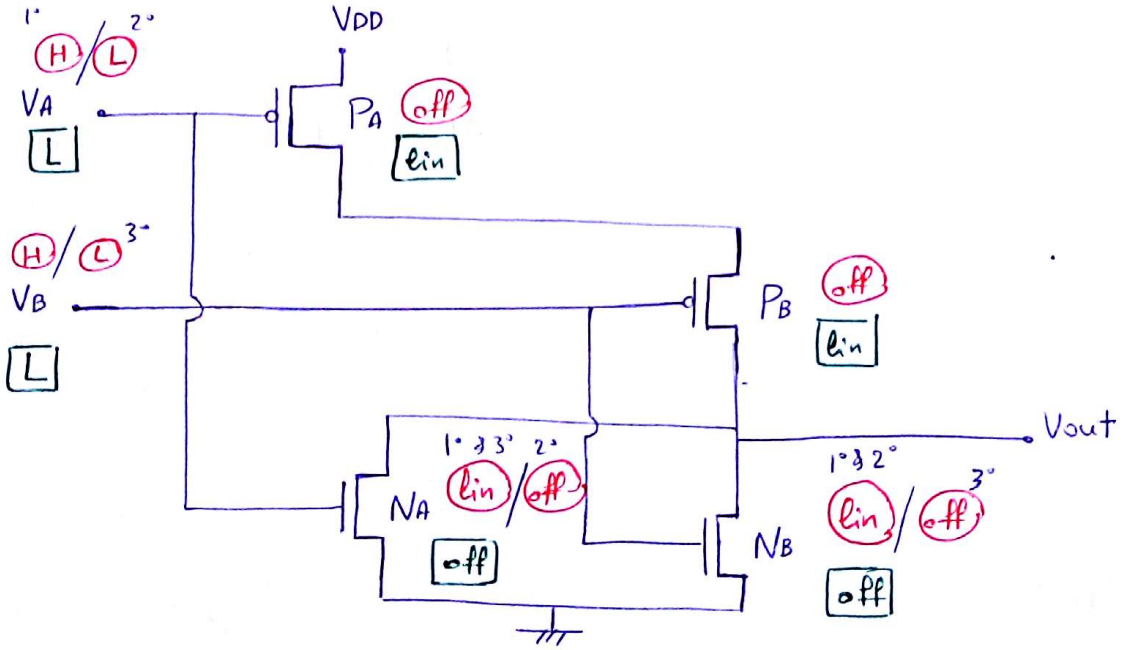
② 2 - inputs NAND gate $2 \frac{W_P}{L_P} = 2.5 \frac{W_N}{L_N}$

③ i - inputs NAND gate $i \frac{W_P}{L_P} = 2.5 \frac{W_N}{L_N}$

* AND CMOS Gate



* NOR CMOS Gate



* V_{OL}

All or inputs high

1° ⇒ All high Ps off , Ns lin

$V_{DS\,NA} = V_{DS\,NB} = 0$

$V_{out} = V_{OL} = 0$

2° ⇒ V_A low , V_B high

N_B is lin $\rightarrow V_{SD_B} = 0 \rightarrow V_o = V_{OL} = 0$

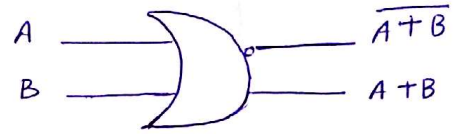
Rest are off

3° ⇒ V_A high , V_B low

N_A is lin $\rightarrow V_{SDA} = 0 \rightarrow V_o = V_{OL} = 0$

Rest are off

OR/NOR



* V_{OH}

All inputs low

Ns off , Ps lin

$V_{SD} = 0$

$V_{out} = V_{OH} = V_{DD}$

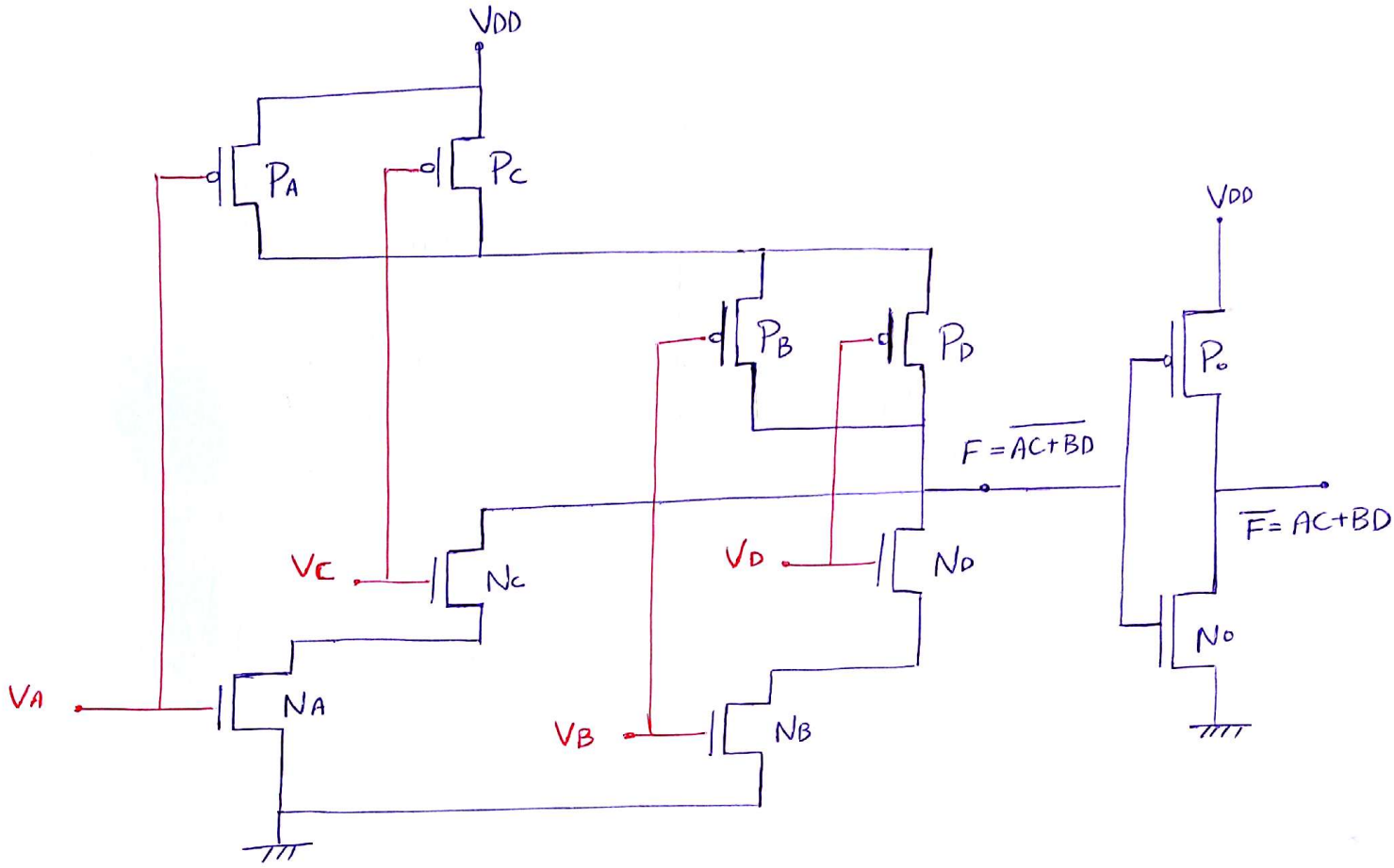
A	B	$V_{o,NOR}$	$V_{o,OR}$
L	L	H	L
L	H	L	H
H	L	L	H
H	H	L	H

2 → For summary

* 2-inputs NOR Gate $\frac{W_P}{L_P} = 5 \frac{W_N}{L_N}$

* i-inputs NOR Gate $\frac{W_P}{L_P} = i\ 2.5 \frac{W_N}{L_N}$

AND-OR Inverter Logic Function AOI



* Keep inversion until the end

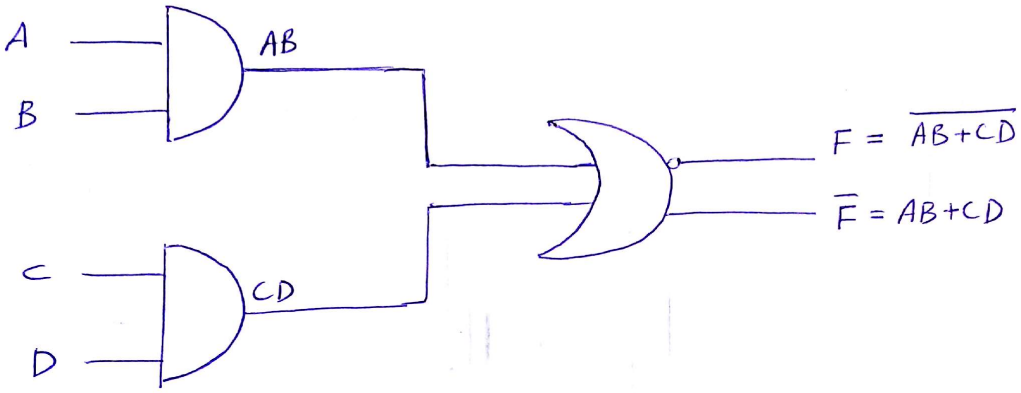
* Enough to look at NMOS or PMOS

for NMOS : in series AC
BD

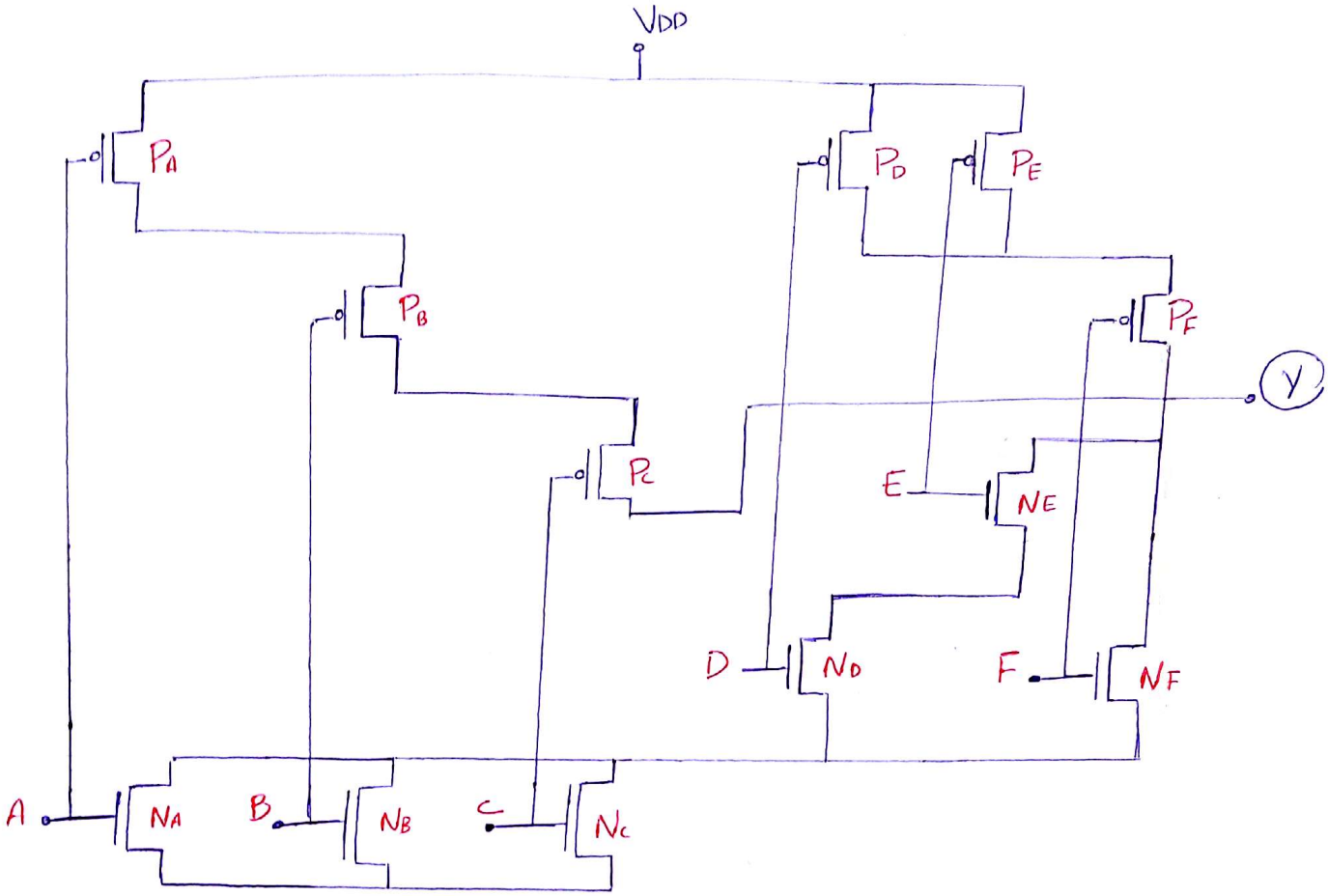
in parallel AC + BD

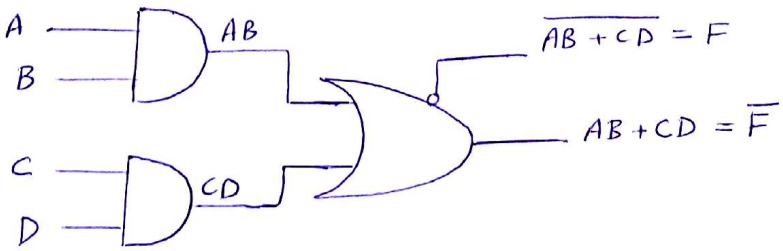
for PMOS : in parallel AC
BD

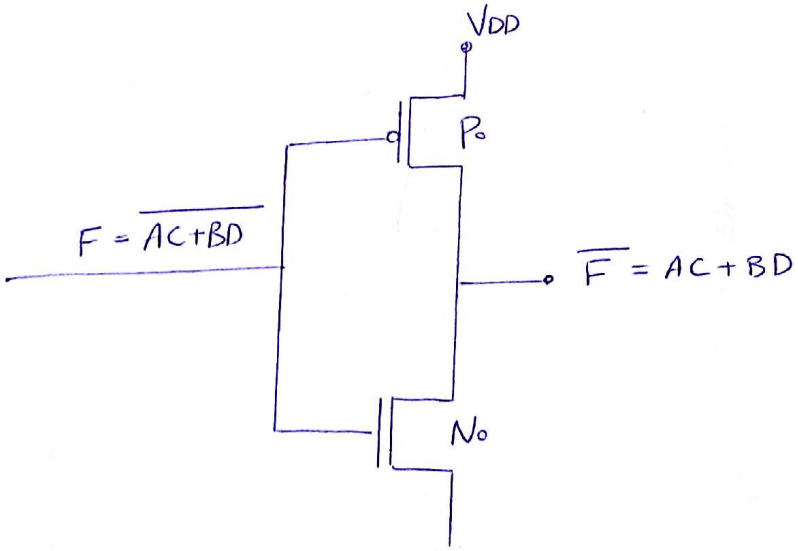
in series AC + BD



ex Draw the function $Y = \overline{(A+B+C)(DE+F)}$ usig CMOS







⇒ Chapter ("32") : Read only memory

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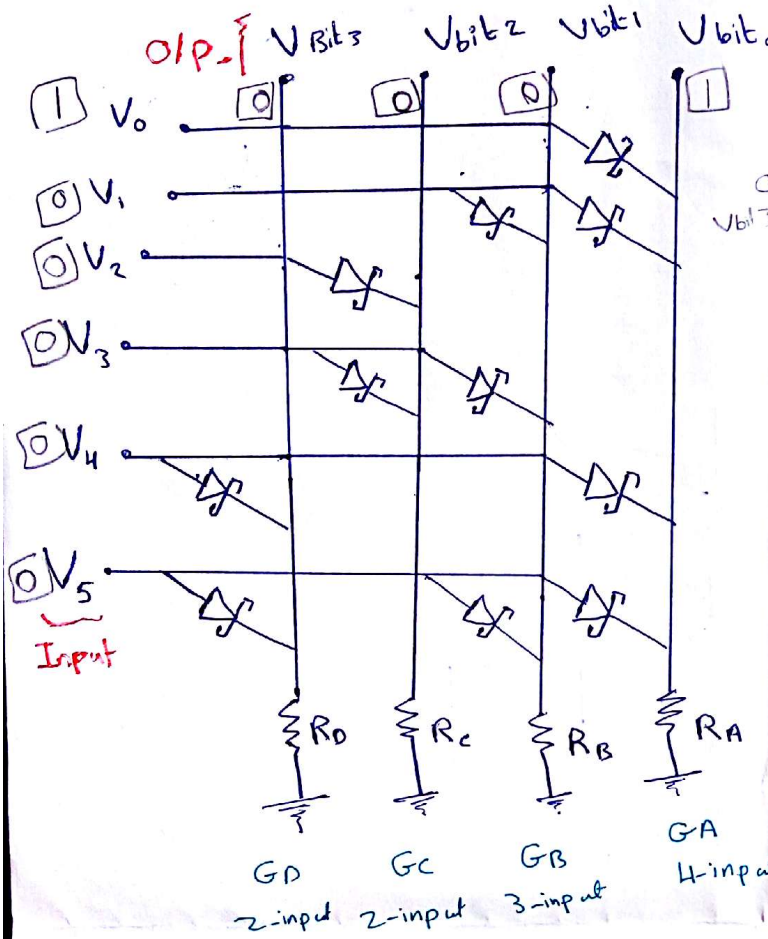


32.1, 32.2 : Diode and BJT Rom .

0001
Vbit3 Vbit0

⇒ GA, GB, GC, and GD are resistor OR Gates.

Function : one single input is high at a time starting with V_0

$V_0 = 1$, rest $= 0$

$V_{Bit_0} = V_0 + V_1 + V_4 + V_5 =$

$1 + 0 + 0 + 0 = 1$

$V_{Bit_1} = V_1 + V_3 + V_5 =$

$0 + 0 + 0 = 0$

$V_{Bit_2} = V_2 + V_3 =$

$0 + 0 = 0$

$V_{Bit_3} = V_4 + V_5 = 0 + 0 = 0$

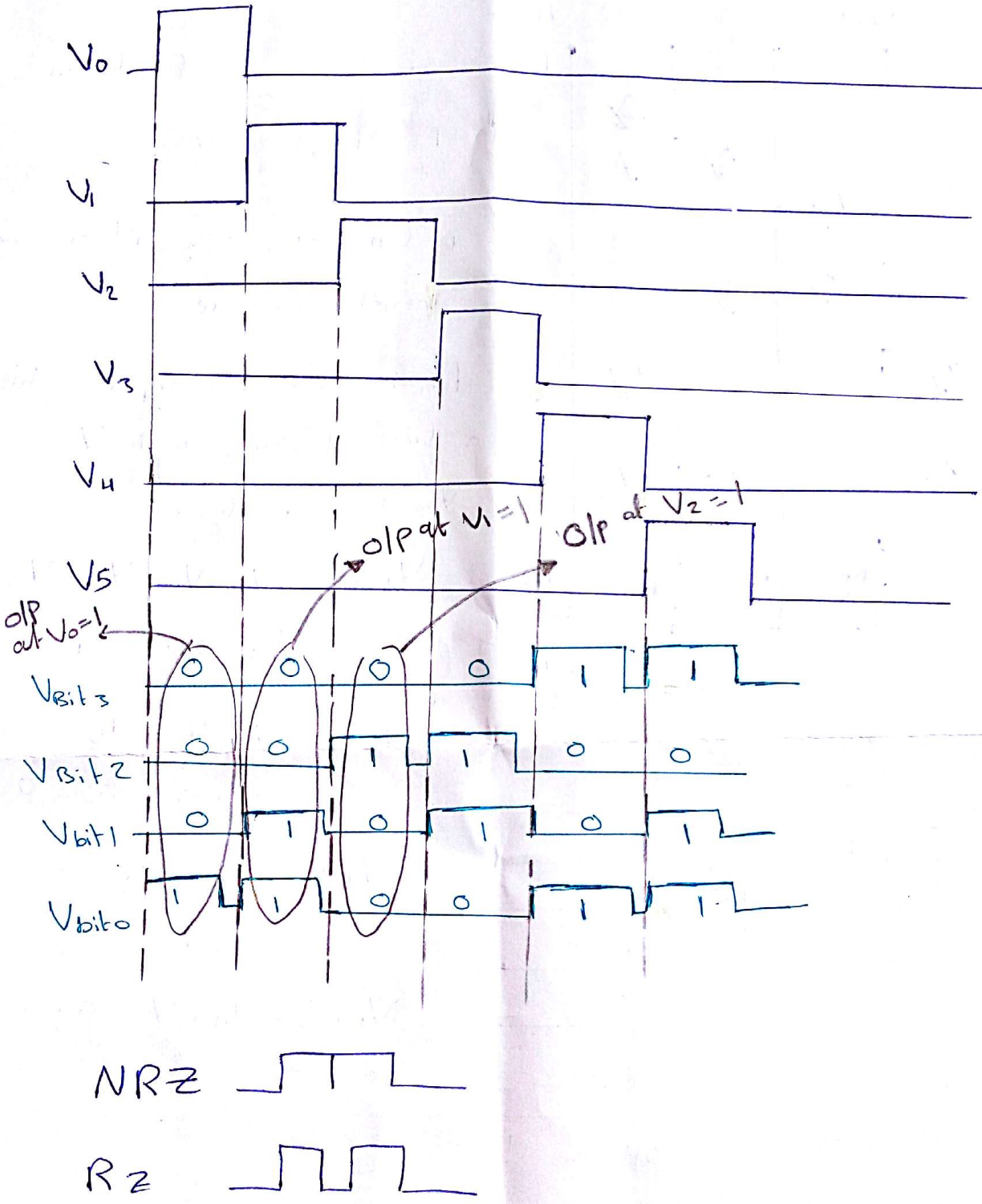
V_0	1	0	0	0 ...
V_1	0	1	0	0 ...
V_2	0	0	1	0 ...
V_3	0	0	0	1 ...
V_4	0	0	0	0 ...
V_5	0	0	0	0 ...

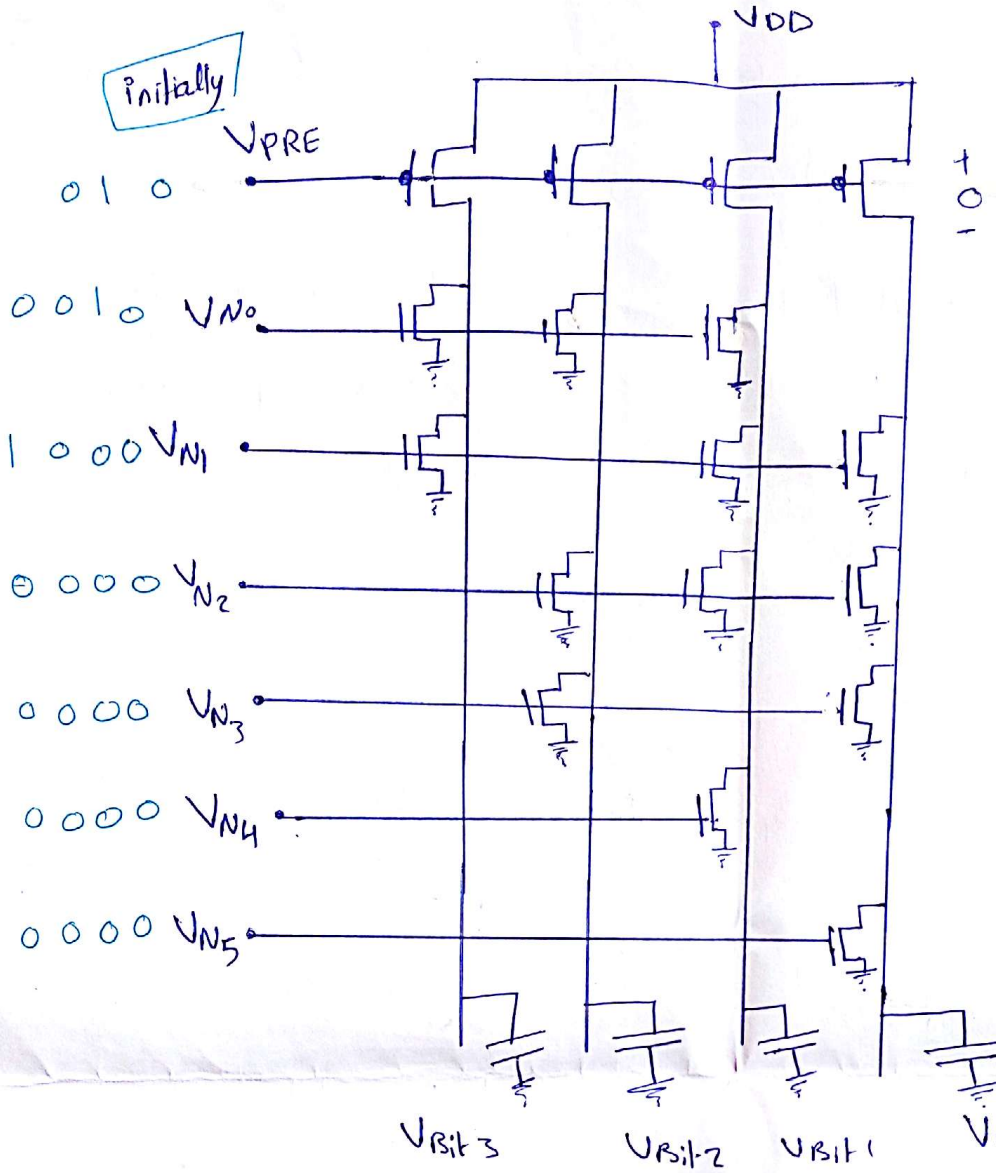
V_{out}	$(0001)_2$	$(0011)_2$	$(0100)_2$	$(0110)_2$	$(1001)_2$	$(1011)_2$
	$(1)_{10}$	$(3)_{10}$	$(4)_{10}$	$(6)_{10}$	$(9)_{10}$	$(11)_{10}$

Output : «MS» V_{bit3} V_{bit2} V_{bit1} V_{bit0} «LS»

0 0 0 1

next , set $V_1 = 1$ and rest is logic zero and O/p.





O/P			
B_3	B_2	B_1	B_0
0	0	0	1
0	1	0	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Initially, V_{PRE} is set at low, and all V_N's are low, PMOS are linear and Voutput is high

$\Rightarrow$ Capacitance will charge to V_{DD}. Next V_{N0} is set at logic 1 and rest are 0. NMOS with input 1 is linear and $V_{DSN}=0$

Capacitors will discharge and o/p is logic zero,

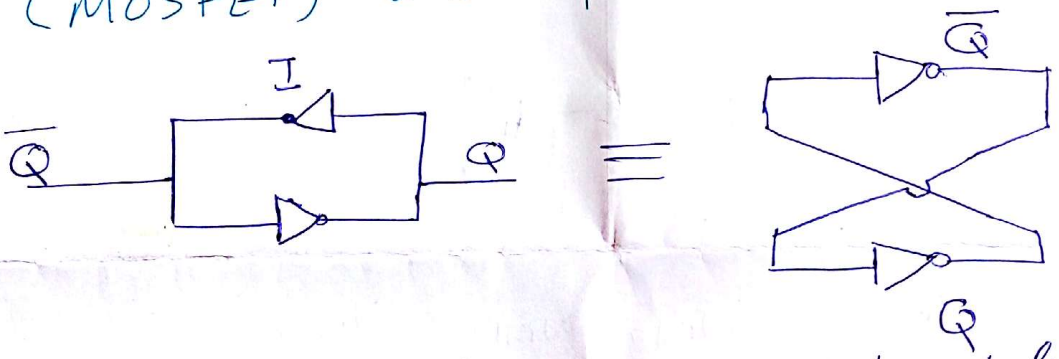
NMOS with logic zero will be off.

* When all inputs at one gate are zero all NMOS will be off and $V_{out} = V_{OH} = V_{DD}$, logic (1)

* Before setting $V_{N_1} = 1$, transistors need to be reset with all inputs (including V_{PRE}) are set to zero, so that capacitors can change to V_{DD}.

Chapter 33: Random Access memory

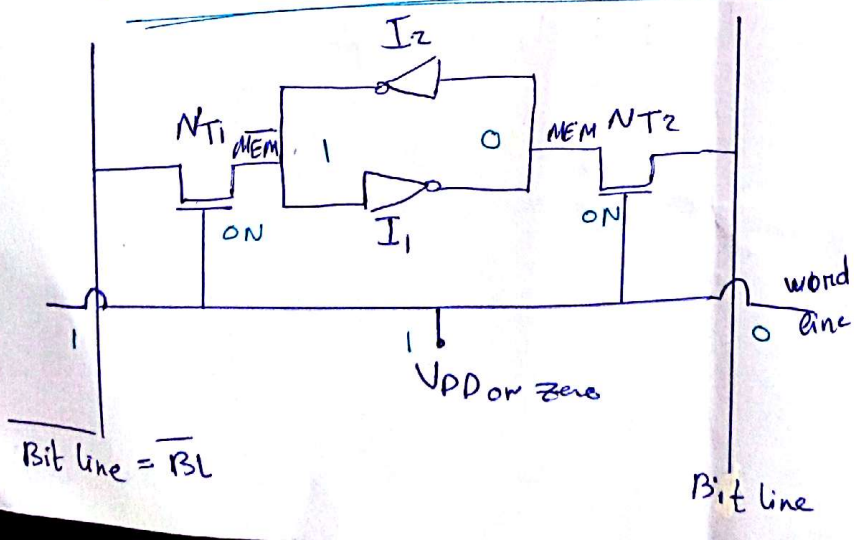
33.1, 33.2: static RAM cell with transmission gate. (MOSFET) Cross Coupled Inverter Latch.



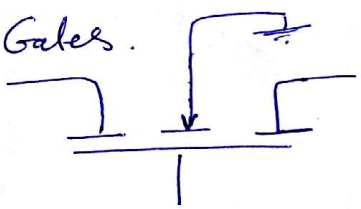
RAM: Data can be read in a sequence independent of the order it was originally written.

SRAM: Maintains storage of Data as long as power applied to the semiconductor cct employing it is un-interupted.

Basic static RAM cell



N_1 and N_2 are transmission Gates.



* when input high Nt conducts
* when input low Nt is off

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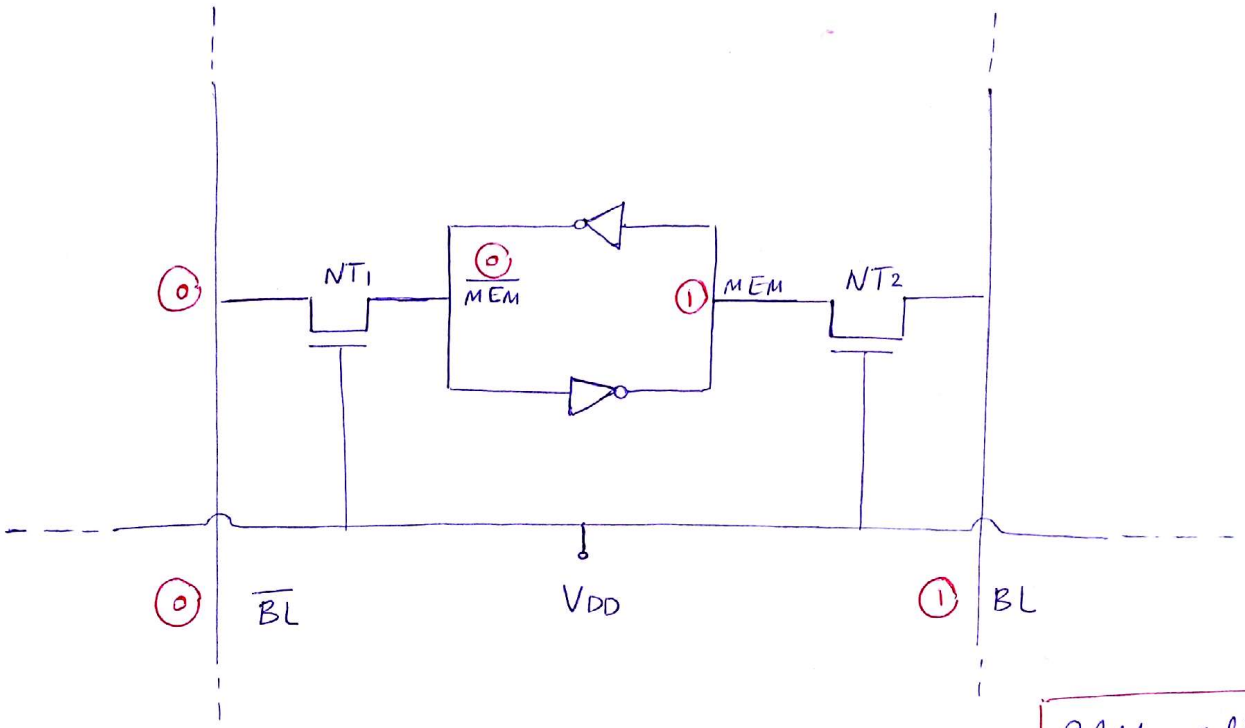


RAM cell

* Writing data into cell

To write data, WL = 1

NT1 & NT2 are on

→ if BL = 1 ($\overline{BL}$ = 0)

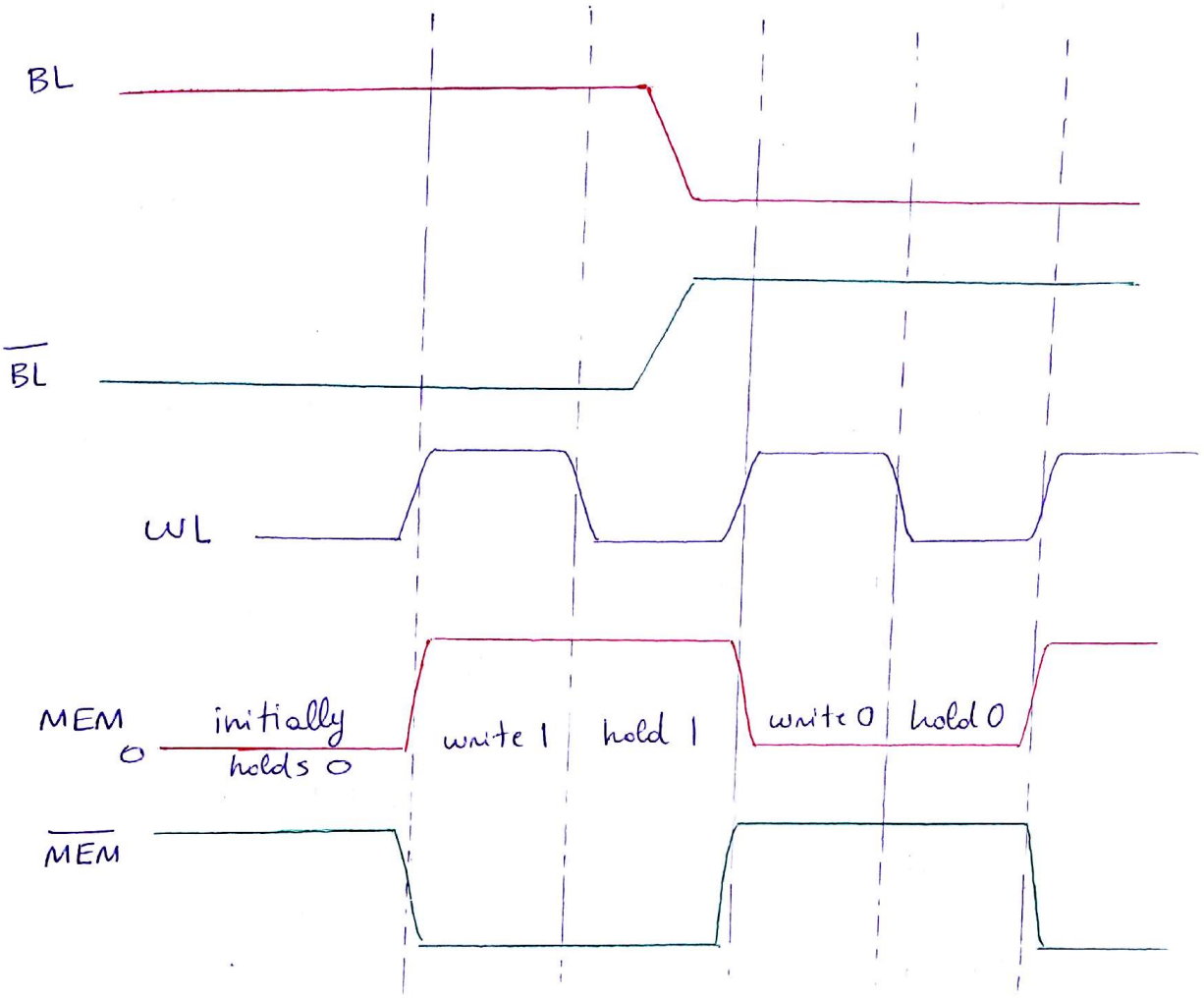
MEM = 1 , $\overline{MEM}$ = 0

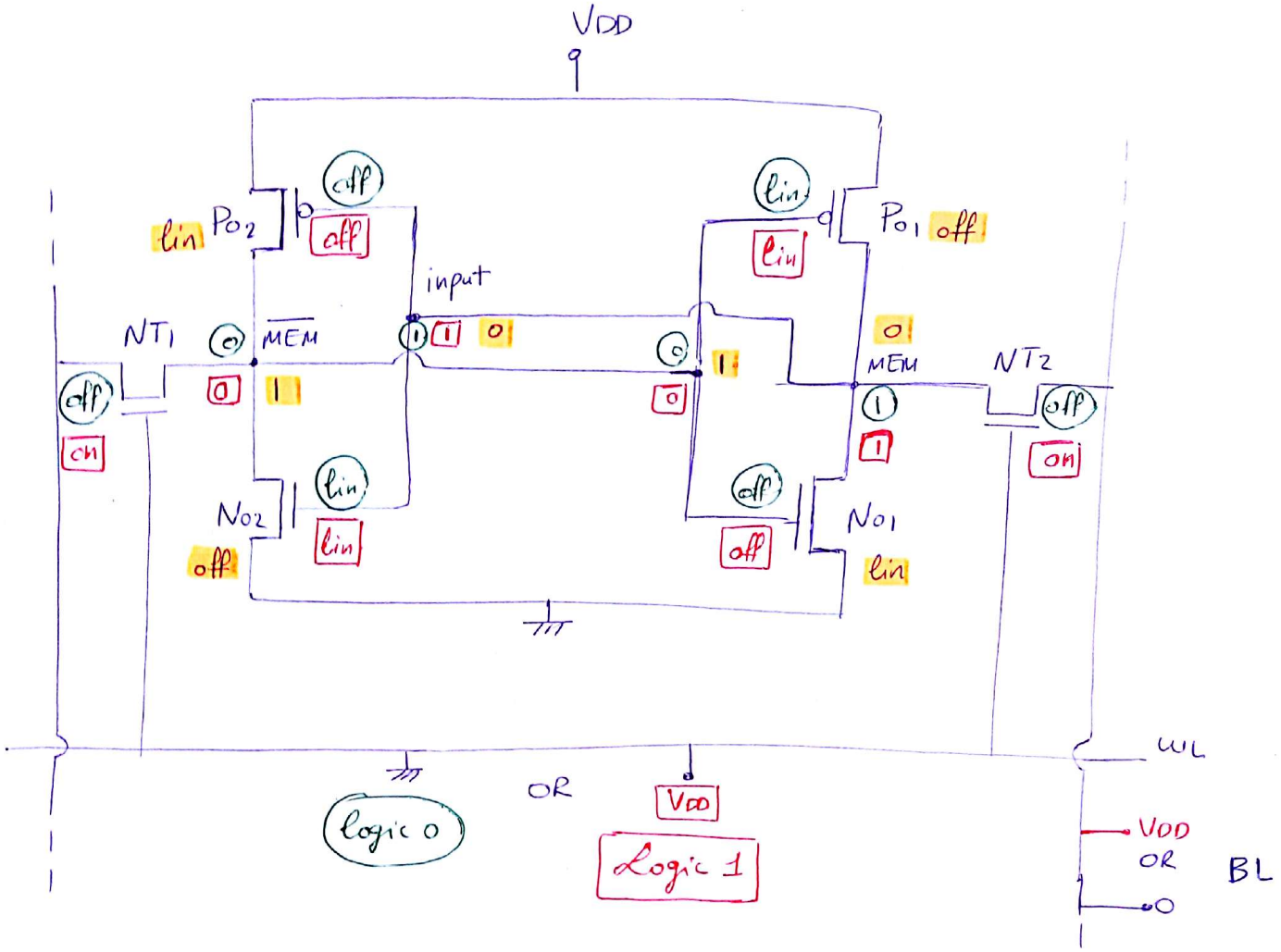
→ if BL = 0 ($\overline{BL}$ = 1)

MEM = 0 , $\overline{MEM}$ = 1

* Reading data from cell

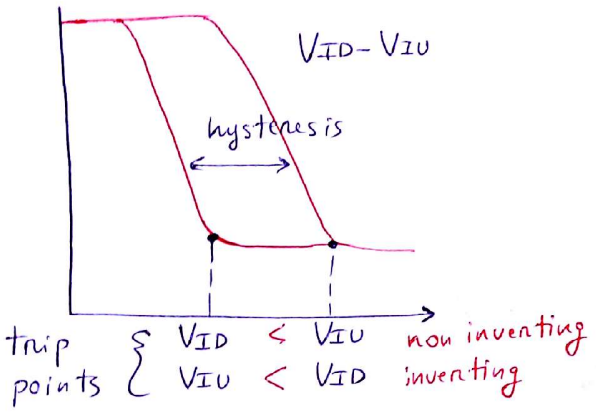
WL = 1 , BL & $\overline{BL}$ are allowed to read data from cell

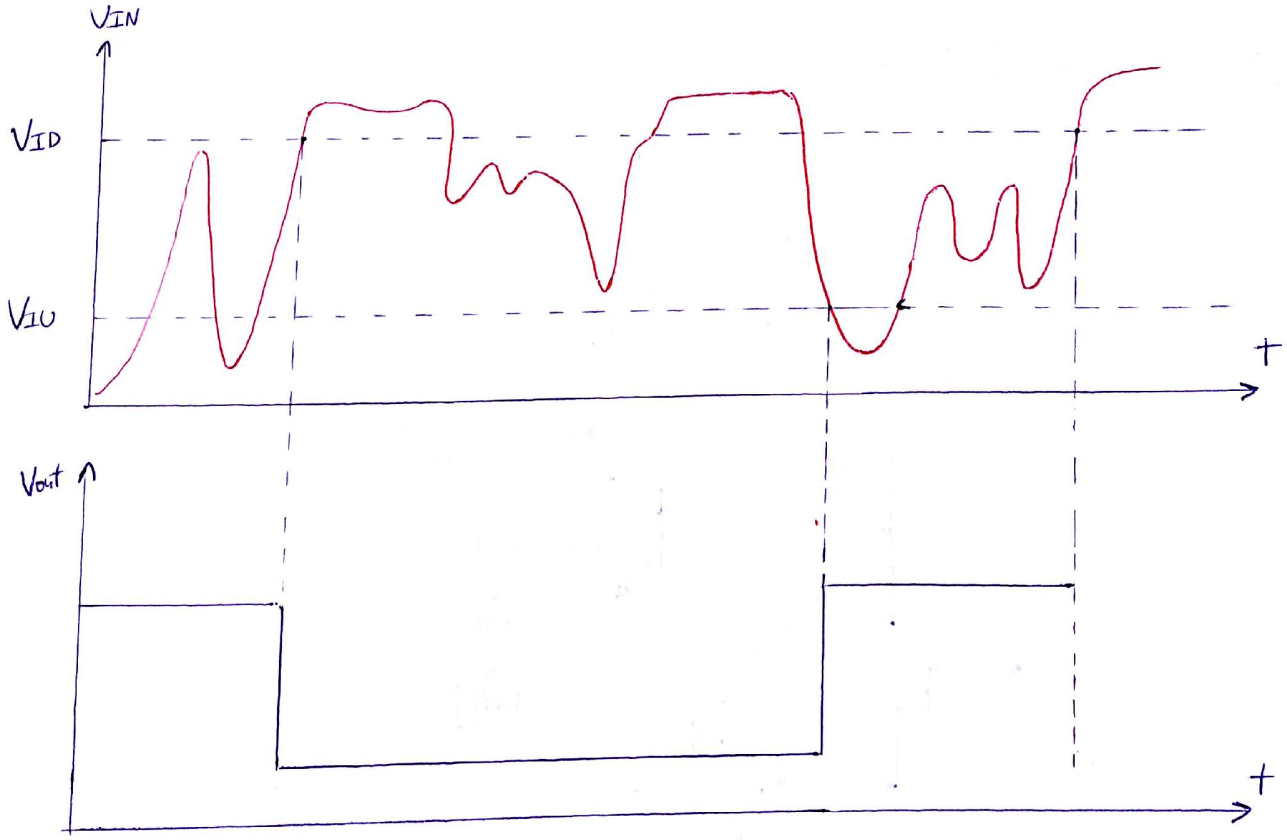




DIGITAL ELECTRONICS

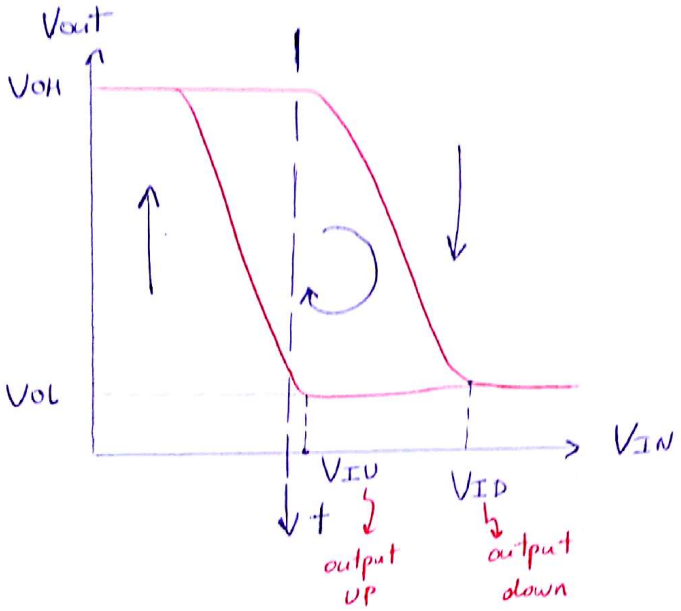
10.6 Shmitt Trigger



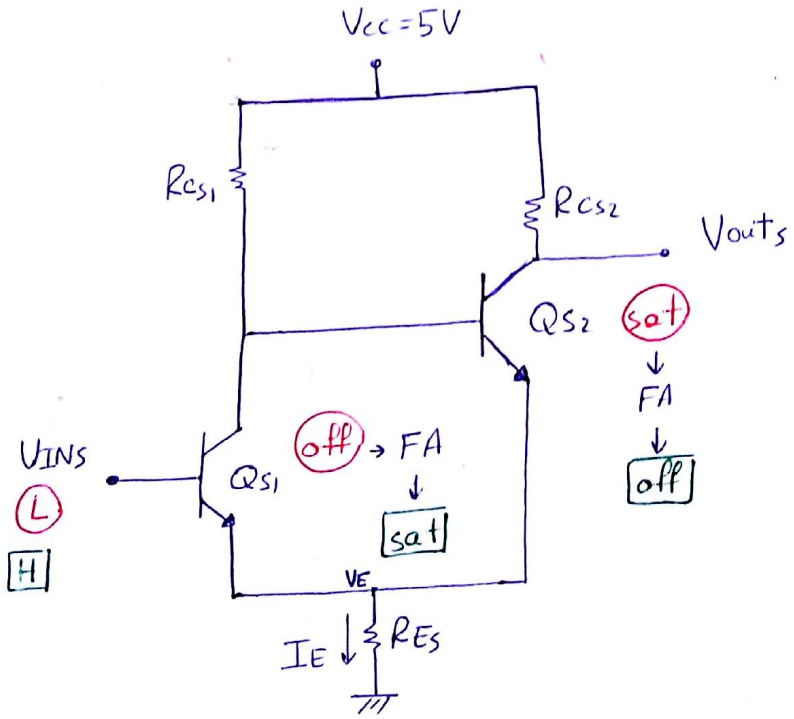


Inverting Schmitt Trigger

* VTC → Hysteresis loop inverting ST



* Emitter Coupled Shmitt Trigger



* V_{OL}

$$I_{BS2} + I_{CS2} = I_{ES2} = I_E$$

$$V_E = \frac{\frac{V_{CC} - V_{BE(sat)}}{R_{CS1}} + \frac{V_{CC} - V_{CE(sat)}}{R_{CS2}}}{\frac{1}{R_{CS1}} + \frac{1}{R_{CS2}} + \frac{1}{R_E}}$$

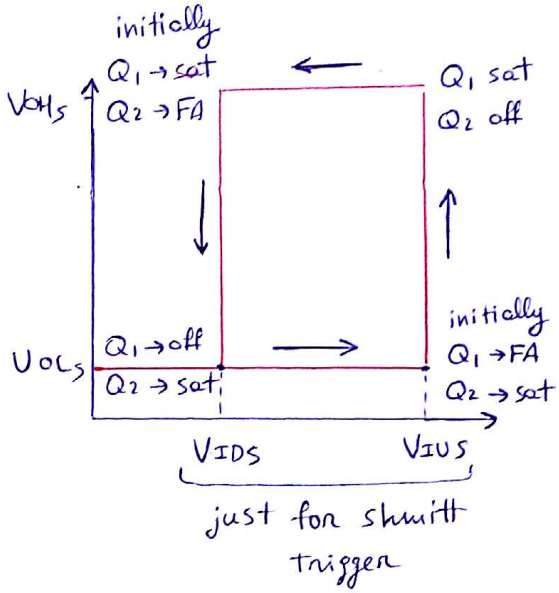
$$V_{OL} = V_{CE_2(sat)} + V_E$$

Initial V_E from previous step

$$V_{IUS} = V_{BE_1(FA)} + V_E$$

$$\hookrightarrow V_{IUS} = \frac{\frac{V_{CC} - V_{BE_2(sat)}}{R_{CS1}} + \frac{V_{CC} - V_{CE_2(sat)}}{R_{CS2}}}{\frac{1}{R_{CS1}} + \frac{1}{R_{CS2}} + \frac{1}{R_E}} + V_{BE_1(FA)}$$

$$V_{IDS} = \frac{V_{CC} + \left(\frac{R_{CS1}}{R_E} + 1\right) V_{BE,S1(sat)} - V_{BE,S2(FA)}}{\frac{R_{CS1}}{R_E} + 1}$$

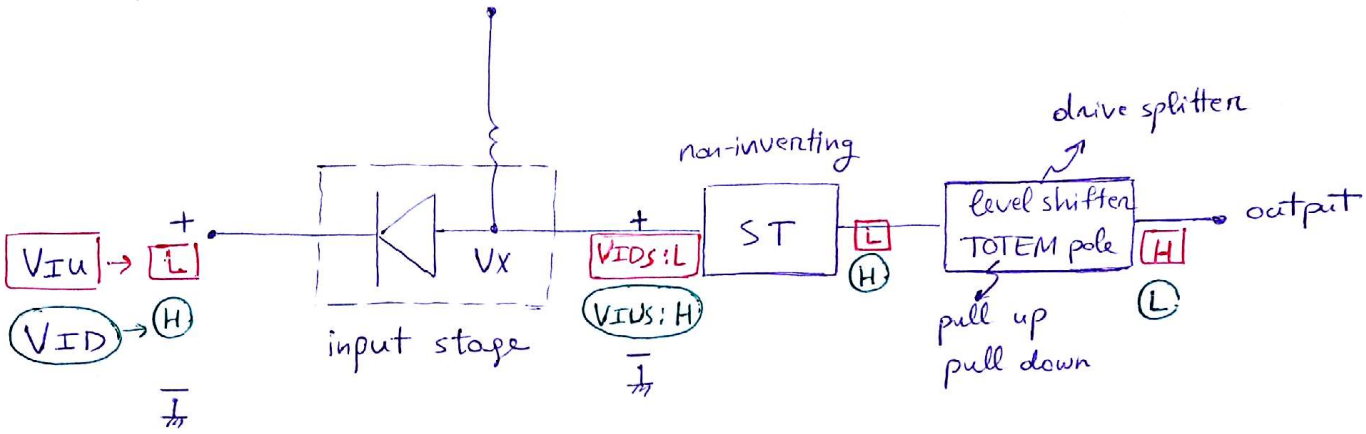


just for shmitt trigger

* V_{OH}

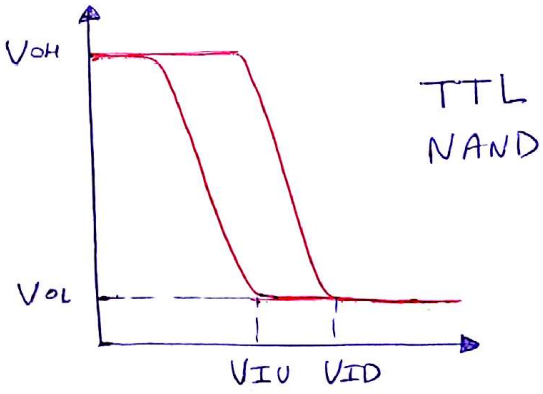
$Q_{S2} \to$ off

$$V_{OH} = V_{CC}$$

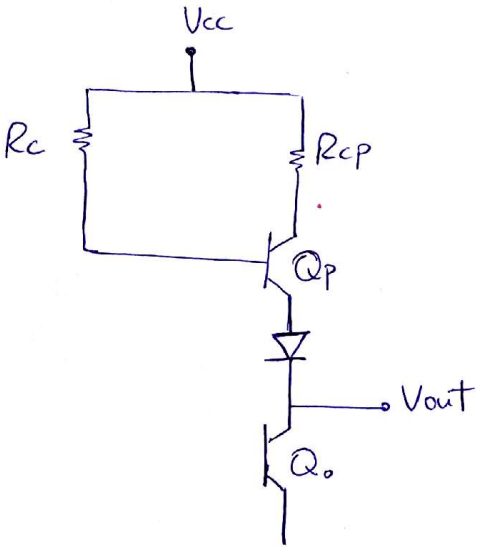


* $V_{IU} = V_{IDs} - V_\gamma$

* $V_{ID} = V_{IUs} - V_\gamma$



from TTL cct



$V_{OH} = V_{CC} - V_{BE} - V_{D(ON)}$

$V_{OL} = V_{CE(sat)}$