TABLE OF CONTENTS

TABLES

FIGURES

1 INTRODUCTION TO PRACTICAL POWER SYSTEM PROTECTION

PURPOSE

The purpose of this text is to provide a comprehensive guide to power system protection using SEL-based products. The anticipated audience is both the experienced protection engineer and the engineer just learning the art and science of power system protection. The information is organized in a way that permits easy information location and retrieval. SEL's goal in producing this document is to equip power engineers with the best opportunity to make electric power as safe and economical as possible.

REQUIREMENTS

The information in this text assumes that the reader has fundamental knowledge of electrical engineering, but not necessarily power system protection. A suitable level of knowledge would be a senior electrical engineering student or a mid-level electrical technician. Electrical engineering fundamentals that pertain significantly to power system protection are included. The text also includes references to direct readers needing or wanting additional information.

WHAT IS POWER SYSTEM PROTECTION?

Power system protection is the process of making the production, transmission, and consumption of electrical energy as safe as possible from the effects of failures and events that place the power system at risk. It is cost prohibitive to make power systems 100 percent safe or 100 percent reliable. Risk assessments are necessary for determining acceptable levels of danger from injury or cost resulting from damage. Protective relays are electronic or electromechanical devices that are designed to protect equipment and limit injury caused by electrical failures. Unless otherwise noted, the generic term relay will be synonymous with the term protective relay throughout this text. Relays are only one part of power system protection, because protection must be designed into all aspects of power system facilities. Protective relays cannot prevent faults; they can only limit the damage caused by faults. A fault is any condition that causes abnormal operation for the power system or equipment serving the power system. Faults include but are not limited to: short- or low-impedance circuits, open circuits, power swings, overvoltages, elevated temperature, off-nominal frequency operation, and failure to operate.

Power system protection must determine from measurements of currents and/or voltages whether the power system is operating correctly. Three elements are critical for protective relays to be effective: measurements, data processing, and control. Figure 1.1 shows a typical application of relays to a power system. This example system contains a single source that is connected to bus S through a step-up transformer, two transmission lines that connect bus S to bus R, and a load that is connected to bus R through a step-down transformer.

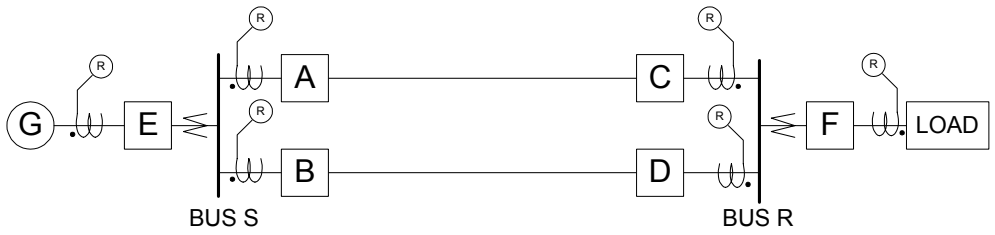


Figure 1.1: Example of Power System Single-Line Diagram

Breakers A through F provide the control to isolate faulted sections of the power system. Breaker F would not be required for this example except that customer-owned generation is becoming more common and a load can change to a source. The current transformers attached to the relays at strategic points in the power system provide the necessary instrumentation for relays to determine the presence of faults. Voltage instrumentation for protection systems may also be required, depending on the relaying scheme used. Any number of relay devices may use any single-voltage or current instrumentation device. It is important that the load or burden the relay devices create does not adversely affect the quality or accuracy of the measurements by these or other devices.

It is not clear from this diagram what is being protected or what function is being performed. Usually a designation number is put into the circles that Figure 1.1 shows as 'R'. The power system protection is divided into zones based on the type of equipment and location, as shown in Figure 1.2. Overlapping these zones increases protection reliability; if one protection system fails to perform, another is ready to provide the needed protection. Each protection zone consists of a sensing current transformer, a power control breaker that can deenergize the protected zone. The CTs shown in Figure 1.1 and Figure 1.2 have polarity marks to indicate that positive current flow is into the mark. CTs are necessarily outside the protection zone.

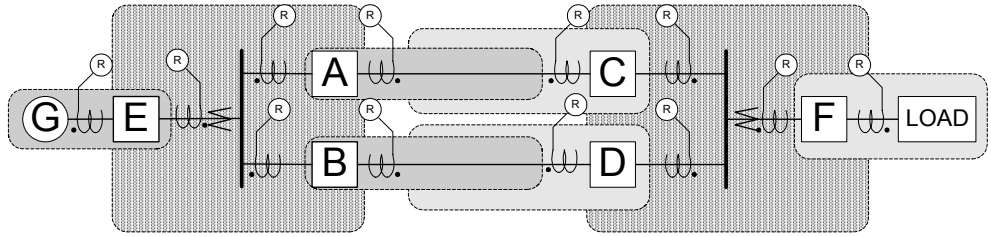


Figure 1.2: Examples of Zones of Protection

GOALS OF PROTECTION

Maintain the Ability to Deliver Electric Power

Power systems that have evolved in the 20th century consist of generation plants, transmission facilities, distribution lines, and customer loads, all connected through complex electrical networks. In the United States, electrical energy is generated and distributed by a combination of private and public utilities that operate in interconnected grids, commonly called power pools, for reliability and marketing.

Elsewhere in the world, generation is tied to load through national or privatized grids. Either way, power flows according to electrical network theory.

Interconnection improves the reliability of each pool member utility because loss of generation is usually quickly made up from other utilities. However, interconnection also increases the complexity of power networks. Power pool reliability is a function of the reliability of the transmission in the individual members. Protection security and dependability is significant in determining the reliability of electrical service for both individual utilities and the interconnected power system pool.

Public Safety

Relays are designed to deenergize faulted sections as quickly as possible, based on the premise that the longer the power system operates in a faulted condition, the greater the chance that people will be harmed or equipment damaged. In some cases power system stability and government regulatory commissions set the speed requirements of extra high voltage (EHV) systems. Because of cost constraints, relays are not designed to prevent the deaths of people or animals who make direct contact with high voltage lines. Instead, designers use physical separation and insulation to prevent direct contact. Still, the faster a faulted system element can be detected, isolated, and deenergized, the lower the probability that anyone will encounter hazardous voltages.

Equipment Protection

The primary function of power system protection is to limit damage to power system apparatus. Whether the fault or abnormal condition exposes the equipment to excessive voltages or excessive currents, shorter fault times will limit the amount of stress or damage that occurs. The challenge for protective relays is to extract information from the voltage and current instrumentation that indicates that equipment is operating incorrectly. Although different faults require different fault detection algorithms, the instrumentation remains the same, namely voltages and currents. (See Table 4.1 in Section 0 for a more complete list of instrumentation requirements.)

Power System Integrity

Properly operating relay systems isolate only the portions on the network directly involved with the fault. If relays operate too quickly or fail to operate, the fault-affected area expands and some circuits are deenergized. Parts of the power system can become isolated from the rest of the network. A large mismatch between generation and load can put an islanded network in jeopardy of losing the generation control that holds frequency and voltage within acceptable limits. Without generation control, the isolated systems will eventually be tripped off by other relays. Widespread outages caused by cascading voltage or frequency excursions require many work hours to restore power, which is costly from both a labor and a lost revenue perspective.

Power Quality

The factors measured to determine the quality of power are voltage amplitude, frequency, and waveform purity. Voltage amplitude quality takes into account persistent RMS value, flicker, and intermittent dips and peaks, as well as momentary and long-term outages. Frequency changes at most a few hundredths of a hertz, unless the power system has lost generation control. Induction motors have the most sensitivity to power system frequency. Waveform purity is largely a function of harmonic content and is predominantly influenced by load.

The quality of electrical power is an issue for loads that are sensitive to momentary outages and harmonics. In the past, when loads were primarily resistive and inductive, harmonics were either inconsequential or nonexistent. Also, momentary outages had little effect on residential customers. Commercial and industrial customers compensated for momentary outages either with multiple feeds from the utility power sources or with local generation.

Today, every residential customer knows that there was an outage whether she or he was home to experience it. Outages affect home computers and the digital clocks on VCRs, microwave ovens, and other numerous appliances. Although the inconvenience may seem trivial to the relay engineer and perhaps the actual number of outages is even less than in years past, the customer may perceive that the power system is not as reliable today. Good relay selectivity is key to reducing the number of outages and faster relaying minimizes the duration of power dips.

PROTECTION SYSTEM MANAGEMENT

Protection Quality

There are four primary causes of protection system failures: instrumentation distortion, control failures, relay equipment failures, and incorrect relay settings. Instrumentation distortion is usually caused by saturation from excessive inputs or remnant flux. Breaker failures or faults in the dc controls can cause control failures. Relay equipment reliability depends on design and manufacturing processes. In addition to overlapping zones of protection, both redundant and backup protection increase reliability for critical applications. Improper settings render relay systems useless. Hence protection systems designers must know which relay is best suited for a particular application and how to set the relay parameters to obtain the proper selectivity and sensitivity. Proper relay application is the single most important factor in the quality of power system protection.

Continuous Improvement

Power systems are not static networks. Transmission lines and generators are continuously put into or taken out of service. Each change in the network potentially affects the operations of protective relays. Protection engineers must decide how to alter the relay settings to compensate for a change in the power network configuration.

Analysis of Data

Each fault tests the power system relays in the vicinity of the fault and presents an opportunity to analyze the behavior of the entire protection system. The fault location, type of fault, fault impedance, and relay sensitivity determine which relays respond to the fault. Relays either operate correctly (including in a timely manner) or incorrectly (including too slowly or too quickly). Microprocessor-based relays can now report information that provides the data to determine just how correct the operations were. Prior to microprocessor-based relays, oscillographs and sequential events recorders were used to determine the correctness of operations. Section 6.1 provides examples of this type of analysis.

Economics of Protection

Plant equipment represents a significant investment to electric utilities. Figures from a representative utility that has a significant amount of hydro-based generation show that 50 percent of the plant investment is allocated to production, 14 percent to transmission, and 27 percent to distribution. In actual year-2000 dollars for a moderately sized utility, the investment in transmission and distribution alone is over one billion dollars. The cost of protection equipment is but a very small part of this investment.

Capital Expense

A rule of thumb is an installed cost of $30,000 per terminal end regardless of relay type. If the relaying scheme includes pilot protection, the cost of the communications is an additional expense.

Operating Costs

Operating costs for relays are not the same as operating costs for protection systems. The former includes the costs of servicing and maintenance. Electromechanical and solid-state relays (also called static relays) require regular testing to determine their functionality. This means personnel must go to the substation and take the relay out of service during testing and calibration. If power system network changes require new relay settings, then personnel must again go to the substation to make appropriate modifications and tests. The expense of this humanpower adds to the operating costs of relays.

Microprocessor-based relays are able to perform self-diagnostics and automated reporting with little or no additional investment, other than the original cost of the relays. They can be reconfigured remotely for new power system needs. Some relays have multiple group settings that automatically reconfigure the relays based on the open or closed position of one or more breakers. Communication with the relays eliminates service visits to the substation. The self-checking ability of microprocessor-based relays allows immediate detection of failed relays without waiting for the next scheduled maintenance visit or a misoperation to reveal the defective unit. Automation also provides performance data that is not economically possible with static and electromechanical relays. Maintenance issues are discussed in more detail in Section 0.

The cost of maintaining a protection system includes both the cost of maintaining the relays and the cost of assessing system performance. Every relay operation tests the protection system by verifying correct operations or exposing incorrect operations. Each fault has an area of effect where some relays are expected to operate and others to inhibit operation. If they do not all react correctly to the fault, the protection system has failed. Various instruments monitor the performance of the protection system (see Section 6.1), with varying degrees of expense associated with the cost of data collection and analysis. In the past, relay operations have been rather binary in that they either trip or don't trip. Today, microprocessor-based relays can also provide information on the certainty of a decision by recording the type of fault, fault location, and relative strength of the restraint and operate signals. Such information is invaluable for revealing potential problems and avoiding future misoperations. This analysis takes time, but the microprocessor-based relay is reducing the required time to achieve improved performance.

Lifetime Costs

Lifetime costs include the purchase price, the cost of installation, and the operation of the protection system. The cost of protection must be justified by the value of potential losses from decreased revenue or damaged equipment. As greater demand is placed upon power systems, the cost of overtripping (tripping when not needed) is becoming as important as undertripping (slow tripping or not tripping when needed). Proper protection requires a balance between speed and security, based on the needs of the system.

PERFORMANCE MEASURES

Protection engineers define dependability as the tendency of the protection system to operate correctly for in-zone faults. They define security as the tendency not to operate for out-of-zone faults. Both dependability and security are reliability issues. Fault tree analysis is one tool with which a protection engineer can easily compare the relative reliability of proposed protection schemes. Quantifying protection reliability is important for making the best decisions on improving a protection system, managing dependability versus security tradeoffs, and getting the best results for the least money. A quantitative understanding is essential in the competitive utility industry.

Resolution, Precision, and Accuracy

All too often, these terms are used interchangeably. However, they describe signals from totally different perspectives. These three attributes of measurement are completely independent; they are easiest to illustrate with examples from analog metrology.

Resolution is the difference between calibrated markings. For example, an outside thermometer might have markings every two degrees Fahrenheit, a two-degree Fahrenheit resolution. A higher resolution is possible by interpolating between markings, but doing so influences precision.

Precision is the ability to achieve repeatability. For analog measurements, precision is actually based upon both the instrument and the observer. For the instrument,

precision is the ability to produce the same output every time the same input is applied. Many environmental factors influence the precision of analog instruments, but friction and temperature tend to dominate. Observers can also influence precision by their position when making the observation, ability to interpolate correctly, and judgment skills. Using the thermometer example once again, if 10 different observers are asked to read the temperature when the outside temperature is exactly 77.20 degrees Fahrenheit and they all read the same temperature every time, the instrument has high precision. This is true even if they always read 75 degrees.

Accuracy is the ability to measure exactly. The thermometer in our example has an inaccuracy of 2.2 degrees, even though it has two degrees of resolution and a high degree of precision. Accuracy can only be determined by calibration using a standard that has a higher degree of accuracy than the instrument being calibrated. The Air Force calibration laboratories require standards to be at least ten times more accurate than the instruments being calibrated. All standards used in those Air Force laboratories are directly traceable to the National Institute for Standards and Technology (NIST) in Boulder, Colorado. Analog instruments get out of calibration because of changes caused by temperature, mechanical and electrical stress, and wear from friction.

Measurements using digital systems are subject to the same inaccuracies and errors as analog systems except for friction and mechanical stress. The observer, whether human or machine, depends strictly on the resolution, precision, and accuracy of the primary instrumentation. The measurement is only affected by data truncation or errors introduced by communications noise. It would be a mistake to attribute any higher degree of accuracy to a system than is actually verified through calibration.

Reliability

Above all else, relays must be reliable, both dependable and secure. This definition of reliability contains conflicting goals or goals that cannot be mutually maximized. Dependability includes timely operation, which denotes speedy detection and decision. The Heisenburg uncertainty principal (the speed of a particle and its position cannot be determined with the same degree of certainty) can be loosely applied to relaying. The longer one has to make a measurement, the more accurate the measurement can be (within the limitations of the measuring equipment) and the more certain the decision that is based upon this measurement.

Relays operate continuously by making correct decisions that discriminate between loads and faults and discriminate between faults that are in the zone of protection and all other faults. Protection reliability is affected by equipment failures and by appropriate application and installation.

Determining device reliability is more important for relays that cannot perform self-diagnostics and alarming. Failure rate (the inverse of device reliability) is usually expressed in mean time between failures (MTBF). For example, suppose the reliability of a device is expressed with a mean-time-between-failure (MTBF) of 100 years. The failure rate is 1/100 failure per year. Therefore, if a system has 300 of these devices, the expected failure rate is $300 \cdot (1/100) = 3$ devices per year.

Failure rates are used to determine maintenance intervals to test for failed relays. The optimal maintenance interval is determined by computing the probability of a failure

over an interval, multiplied by the expected cost of an incorrect operation caused by a relay failure and the cost of maintaining the relay. The interval that makes the two costs equal is the optimal maintenance interval. The difficulty is determining the expected cost of an incorrect operation.

The reliability of other equipment besides the protective relay must be considered when computing the reliability of a protection system. This equipment includes instrumentation, control power (station batteries), auxiliary control devices, and the primary controls such as circuit breakers. Techniques for making reliability assessments are described in Section 0.

Three ways of improving reliability for protective relay systems are: redundant systems, backup systems, and overlapping zones of protection. Critical applications may use all three methods as well as redundant instrumentation and control circuits. Redundant protection uses multiple installations of identical equipment, whereas a backup protection scheme uses multiple relays that are based on different concepts of detecting and identifying faults.

Redundancy

In protection systems, recent use of the term redundant refers to ensuring reliability by duplicating effort. Systems that are 100 percent reliable do not require redundancy, but few systems are 100 percent reliable. As the cost of protection equipment declines, the feasibility of ensuring reliability by duplication increases. Two different approaches to improving reliability by redundancy are discussed below.

Backup Protection

The two most common types of redundancy are dual and parallel redundancy. Dual redundancy is where two identical units are operated with identical inputs. The outputs are placed in parallel for added reliability and in series for added security. Parallel redundancy uses two units of different design but the two units are functionally equivalent. They may or may not use the same inputs but the outputs are connected as they are in dual redundancy.

Diversity – Overlapping Zones of Protection

Protection systems improve reliability by organizing the protection function with overlapping zones in such a way that each relay has a primary zone and provides backup protection for one or more other zones. Relays frequently have multiple operational zones, as illustrated in Figure 1.3. The speed of trips for faults in zone two is generally slower to allow opportunities for other relays that see the fault in zone 1 to clear the fault. Zone 2 therefore provides backup protection by overlapping other zones that are normally protected by other relays. Zone 3 sends signals to block other relays from operating.

Each particular relay has one or more zones of operation. The relay is designed to operate for any fault within the assigned zone or zones. As Figure 1.2 shows, the zones overlap, so more than one relay may operate for a specific fault. Figure 1.3 shows how different zones can be assigned for a relay whose primary function is to

protect the transmission line between breakers A and B. The different zones usually have different operating times worked out in relay coordination plans.

In the example in Figure 1.3, zone one trips for faults from breaker A to 80 percent of the line length toward breaker C. Zone two operates for faults beyond bus R including some percentage of the transmission line between breakers D and B and the transformer supplying the load at bus R. Zone three looks backward toward the source and covers the step-up transformer, plus a percentage of the transmission line between breaker B and D. After the initial fault, as time passes and the fault persists, the relay expands its reach by activating more zones of protection.

The backup protection provided by this scheme can be illustrated using the following example. Consider a fault on the transmission line between breakers B and D. Assume that breaker B operates correctly but breaker D does not. The relay at breaker A waits until Zone 2 activates, and then trips because it sees the fault on the increased sensitivity as the reach expands. The fault is now cleared because breakers at A and B are open. If the fault is closer to breaker B, then the relay at A would not have sufficient sensitivity until the timers allow Zone 3 operations.

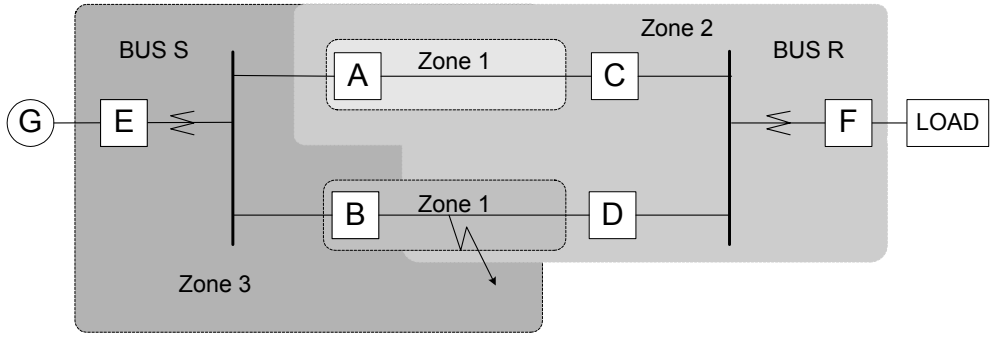


Figure 1.3: Zone Assignments for a Three-Zone Relay

Older relays with limited functionality implemented the various zones of protection using independent devices. Newer microprocessor-based relays are able to implement the functions of numerous protection, control, and monitoring devices.

Analysis of Reliability Using Fault Tree Methods [6060][1] [6073][2]

The method of combining component failure rates is called “fault tree analysis,” a concept first proposed by H. A. Watson of Bell Telephone Laboratories to analyze the Minuteman Launch Control System. This method, used and refined over the years, is attractive because it does not require extensive theoretical work and is a practical tool any engineer can learn to use. While computer programs are available to assist in developing and analyzing complex fault trees, this text shows that small fault trees, which are easily analyzed manually, are also very useful.

If a device consists of several components, then a fault tree helps us combine component failure rates to calculate the device failure rate. Refer again to our device that has a failure rate of 1/100 failure per year. It might consist of two components, each with a failure rate of 1/200 failure per year. Both components must operate properly for the device to be sound. The individual failure rates of the two

components add up to the total failure rate of 1/100. We add the component failure rates to obtain the device failure rate if either component can cause the device to fail.

On the other hand, our device with the 1/100 failure rate might consist of two redundant components each with a failure rate of 1/10 failures per year. Either component can give the device satisfactory performance. The product of the individual component failure rates is the device failure rate. We multiply component failure rates to obtain the device failure rate if both components must fail to cause the device to fail.

Fault tree analysis is not the only tool used for reliability studies. Among other techniques, the Markov models compare relative performance of communications-based protection schemes, and predict optimum routine test intervals for protective relays. [3, 4] Markov models cover the entire system of interest and incorporate all failure and success modes and transitions. The outputs of a Markov model are the probabilities that the system resides in any one of the modeled states. This technique models both normal and abnormal states. Since the Markov technique models the entire system, model development requires considerable effort, and Markov model analysis typically requires a computer. Markov modeling also assumes that all state transitions are exponentially distributed, which is sometimes difficult to justify.

Fault Tree Construction

A fault tree, tailored to a particular failure of interest, models only the part of the system that influences the probability of that particular failure. The failure of interest is called the Top Event. A given system may have more than one top event that merits investigation. Figure 1.4 shows a protective system consisting of a circuit breaker, a CT, a relay, a battery, and associated control wiring. The fault tree in this figure helps us analyze the chance that the protective system will not clear a fault.

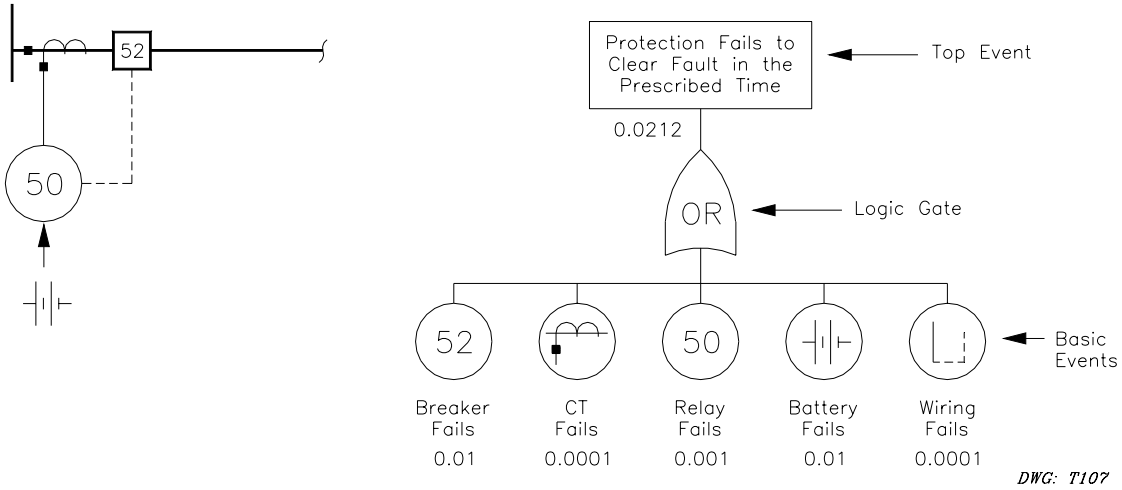


Figure 1.4: Fault Tree for Radial Line Protection

The Top Event is a box containing a description of the failure event of interest. This description usually includes the event that occurred and the maximum tolerable delay for successful operation. For example, our top event here is “Protection Fails to

Clear Fault in the Prescribed Time." We assume the power system is faulted and we assume the protection system is intended to detect and isolate the fault in question in a very short time, usually a few cycles. We wish to know the probability that the protection system will fail to clear the fault in the prescribed time limitation.

The fault tree breaks down the Top Event into lower-level events. Logic gates show the relationship between lower-level events and the Top Event. The OR gate in Figure 1.4 shows that any of several failures can cause the protection system to fail. If the dc system, the current transformer, the protective relay, the circuit breaker, or the control wiring fail, then the Top Event, "Protection Fails to Clear Fault in the Prescribed Time," occurs. Assume the following chances of failure of the individual devices: 0.01 for the breaker, 0.0001 for the CT, 0.001 for the relay, 0.01 for the battery, and 0.0001 for the control wiring. (These component reliability estimates are for purposes of this example only. We will develop more substantiated estimates later.) The chance the system will fail to clear a fault is the sum: 0.0212 failures to clear per fault. We can improve the system by finding better components, which lowers the individual failure rates, by designing simpler systems, or by adding redundancy.

Let us improve the system by adding a redundant relay. The fault tree of Figure 1.5 contains an AND gate. This AND gate shows that both protective relays must fail for the event "Relays Fail to Trip" to occur. Our failure rate for the relays taken together is $0.001 \cdot 0.001 = 0.000001$. The sum implied by the OR gate is 0.0202. The reliability improvement in this case is small, because failures other than those of the relay dominate the system.

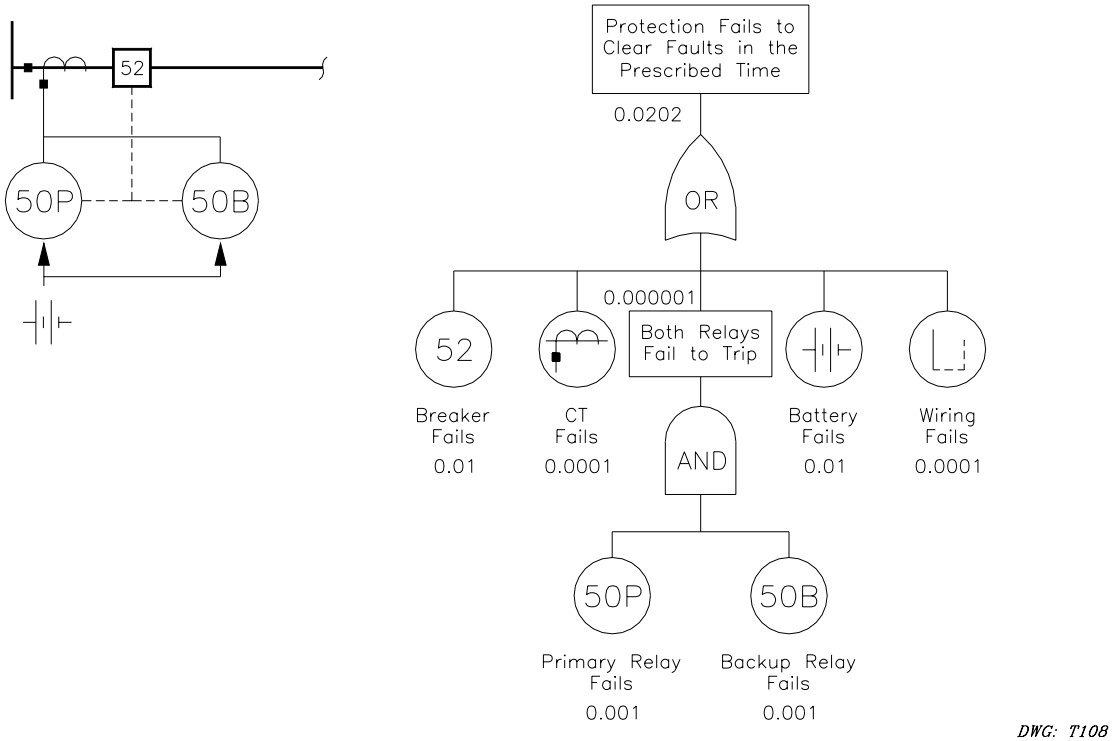


Figure 1.5: Fault Tree for Radial Line Protection With Redundant Relays

There are other gates besides AND and OR gates [1,6]. However, many fault trees require only those gates, and we restrict our discussion to these basic items in this introductory text.

The roots of our fault tree are failures of devices such as the breaker and the relay. Are these basic enough? Should we, for instance, break the relay down into a coil, contacts, disk, bearings, tap block, etc.? If we are comfortable with the failure rates for the devices, then we need not break the devices into their components. The roots are referred to as basic events.

Device Failure Rates and Unavailability

A device failure rate gives us the number of failures we can expect per unit time. During the useful lifetime of a device, we frequently assume a constant failure rate. Failure rates can come from theoretical calculations, such as MIL-HDBK-217F [7] parts-count procedures, or from field experience. For example, suppose there is an in-service population of 10,000 devices, and we observe 10 failures of devices in one year. An estimate of the failure rate from these field data is 10/10,000 = 0.001 failures per year. The reciprocal gives an estimated MTBF of 1000 years. This does not imply that a device is likely to last 1000 years. Instead it is a reliability figure valid during the useful lifetime of the device.

Our experience with relays shows that the MIL-HDBK-217F parts-count procedure gives very pessimistic figures. For example, a parts-count analysis might predict an MTBF of 20 years, yet field failure rates might convert to a field MTBF of 100 years or more. Also, the "217F" parts-count procedure does not consider manufacturing or design quality.

The strict definition of MTBF is the sum of Mean Time To Fail (MTTF) and the Mean Time To Repair (MTTR). MTTF is the reciprocal of failure rate. However, MTTR is usually small and, in this text, we assume MTBF is approximately equal to MTTF.

Failure rates are very useful in predicting maintenance costs, but do not tell the whole story about whether a device will be available when called upon to perform. Thus we need to consider unavailability, the fraction of time a device cannot perform. It is without units.

Roberts, et al. describe calculating unavailability from a failure rate and the time it takes to detect and repair a failure.[5]

$$q \cong \lambda T = \frac{T}{MTBF} \qquad \text{Equation 1.1}$$

where: q is unavailability
λ is some constant failure rate
T is the average down-time per failure
$MTBF = \frac{1}{\lambda}$ is Mean Time Between Failures.

Each failure causes downtime T. Therefore, the system is unavailable for time T out of total time MTBF. The fraction of time the system is not available is therefore T/MTBF.

As an example, consider a protective relay with self-tests that detect all relay failures. If the relay has an MTBF of 100 years, then it has a failure rate of 0.01 failures/year.

First, assume self-tests detect problems within seconds, but it takes two days to repair the failure once it is detected. If the alarm contact of the relay is monitored, then the relay can be back in service in two days, and the unavailability is 0.01 failures/year · 2 days = 0.02 days/year.

On the other hand, if the alarm contact is NOT monitored, we must consider how we discover relay failures. Suppose we test the relay every two years, and repair it the same day we test it. If a test detects a failure, then on the average the relay was down for a year. The unavailability is 1 year · 0.01 failures per year = 3.65 days/year. This is 183 times worse -- so monitoring the alarm contact really pays off!

Protection using relays with self-tests, and with monitored alarm contacts, has better availability if periodic testing is not performed. This is because one day of service lost to testing every two years is much greater than the expected loss of service from automatically-detected failures which are promptly (2 days) repaired.

For the purpose of this text, we have estimated some failure rates, downtimes, and unavailability. We have confidence in our relay failure rates, which we have tracked for years. However, we have less confidence in other figures, and would appreciate field information that will refine our estimates of the failure rates of other components.

Reliability Protective Relay Equipment

Based on our field experience, an MTBF of 100 years is conservative for modern digital relays of quality design and construction. Our products demonstrate a self-test effectiveness of 80 percent or better. When loss-of-voltage and loss-of-current monitoring is enabled and monitored in the relay, the coverage of the relays and their instrument transformers increases to 98 percent effectiveness. These figures and some other assumptions lead to an unavailability of $100 \cdot 10^{-6}$. See Reference 4 for a detailed analysis.

Relays can fail to perform because they are applied improperly. Human factors are very difficult to represent in statistical models; however, based on field experience, we believe that human factors are of the same order of magnitude as relay failures themselves. Therefore we will assume the unavailability contribution caused by human error in installing and setting a relay is also $100 \cdot 10^{-6}$.

Claiming relay unavailability caused by to hardware failures is equal to the unavailability caused by human failures does not mean that hardware failures and human failures are equally likely. The time to detect and repair human errors is indefinite while hardware failures are quickly detected and repaired. Assume human failures take 1 year to detect and repair and are 100 times less likely than relay hardware failures. In this case, unavailability caused by human failures would be:

$$q = \frac{\lambda relay}{100} \cdot 1year = \frac{1}{100years} \cdot \frac{1}{100} \cdot 1year = 100 \cdot 10^{-6} \qquad \text{Equation 1.2}$$

Table 1.1: summarizes the unavailability of commonly-used equipment in power system protection in descending order of unavailability.

Table 1.1: Unavailability of Several Protection Components

Component	*Unavailability x 10^6*
Leased telephone line	1000
Circuit breaker	300
Analog microwave equipment	200
Protective relay misapplications	100
Protective relay hardware	100
Tone equipment	100
Microwave transmission channel	100
Fiber Optic Channel	100
Multiplexing Fiber Optic Transceiver	100
DC power system	50
Modem	30
Simple Fiber Optic Transceiver	10
Current transformer (per phase)	10
Voltage transformer (per phase)	10

Fault Tree Analysis

After entering basic event data, analysis of the fault tree shown in Figure 1.4 is very straightforward with a single simplifying assumption known as the rare event approximation. It ignores the possibility that two or more rare events can occur simultaneously. For two events, each of which occurs with probability less than 0.1, the rare event approximation produces less than 5 percent error. When the events in question are failures, the rare event approximation is always conservative; the approximated probability of failure is always greater than the actual probability of failure.

Employing the rare event approximation, we calculate the unavailability associated with each event expressed with an OR gate as the sum of the unavailability for each input to the OR gate. For example, the unavailability associated with event "Protection at S Fails to Clear Fault in the Prescribed Time When Comm Channel OK" is the sum of the unavailability of the eight inputs to that OR gate. The fault tree of Figure 1.4 contains only basic events and OR gates. Therefore the unavailability associated with the Top Event is simply the sum of all of the basic events, or $2020 \cdot 10^{-6}$.

Suppose we add a redundant relay to the system depicted in Figure 1.3. Assume that the backup relay uses the same instrument transformers, communications gear, dc system, most of the same control wiring, and trips the same circuit breakers as the primary relay. The AND gate in Figure 1.5 shows that both relays must fail for event

"Both Primary and Backup Relays Fail to Trip" to occur. The simultaneous unavailability of both relays is the product of the unavailability of each relay. This calculation assumes the failures are independent (a failure in one relay does not influence the other relay), and are not triggered by a common cause.

In fact, we explicitly separated many possible common-cause failures higher in the fault tree (common instrumentation transformers, common dc supply, common communications gear, some common control wiring, common circuit breakers, and common operating principles). If you determine that other common causes of failure are important (extreme temperature, radio frequency interference, relay misapplications, etc.), include those as separate inputs to OR gates 2 and 3 in Figure 1.6. The unavailability of this protection system to clear faults is $1620 \cdot 10^{-6}$.

When constructing and analyzing fault trees, keep these simple rules in mind:

Use an OR gate to express a failure caused by any of several possible lower level failures. The unavailability of a subsystem represented by an OR gate is the sum of the device unavailabilities.

Use an AND gate to express a failure caused only when all (usually two) lower level failures occur. The unavailability of a subsystem represented by an AND gate is the product of the device unavailabilities.

Use AND gates to express redundancy. Be careful to isolate common causes of failures above the AND gate that expresses redundancy.

Express basic event data in terms of unavailability when the Top Event is of the form "System Fails to Operate." For top events of the form "System Operates Unexpectedly," basic event data in the form of failure rates are more appropriate. This is because unexpected operations or false trips typically occur at the instant a component fails. Therefore the probability of a false trip is not as dependent on component downtime per failure.

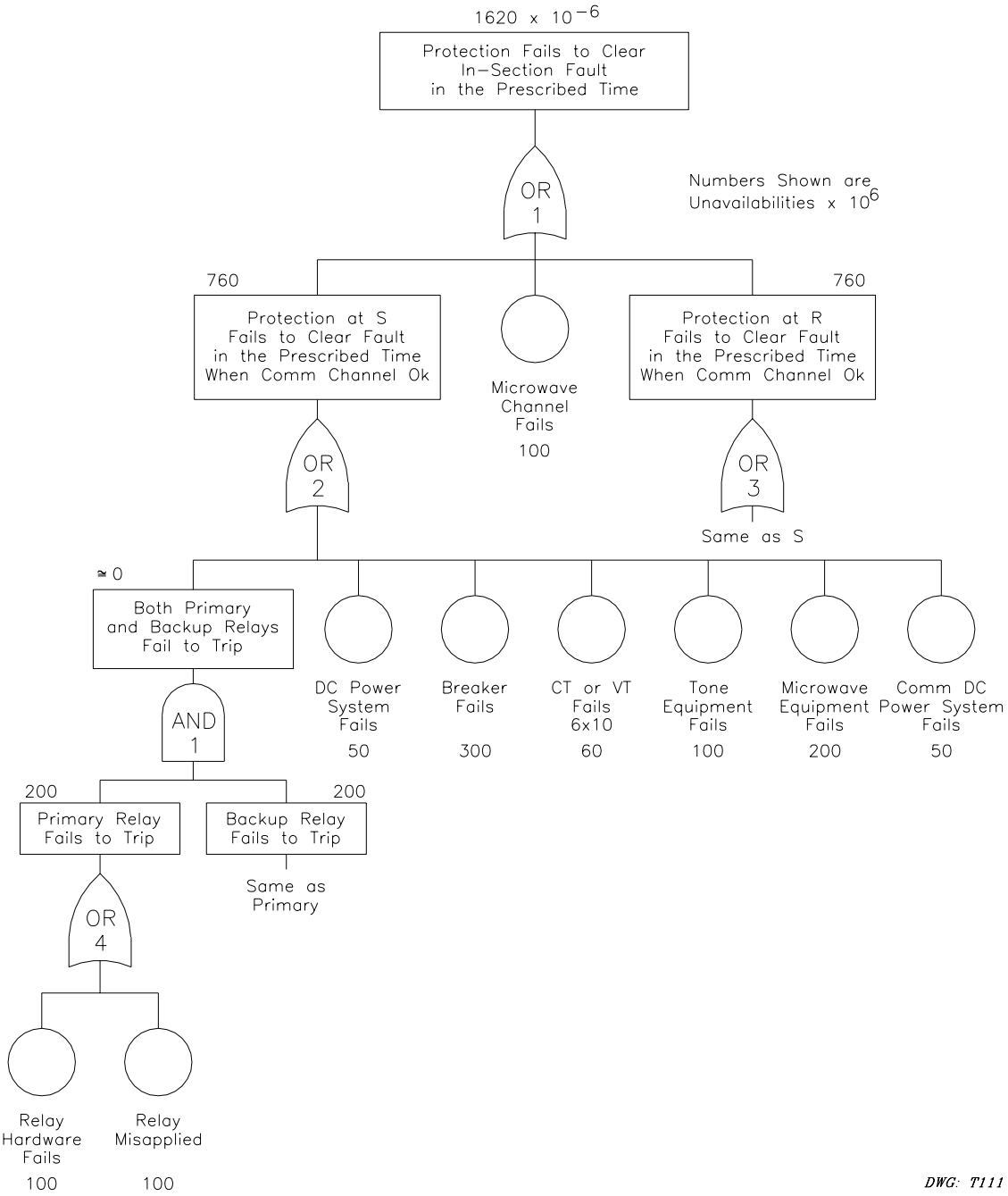


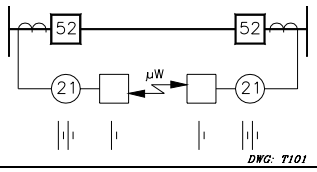
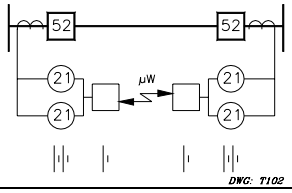
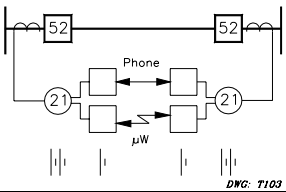
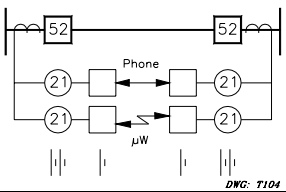
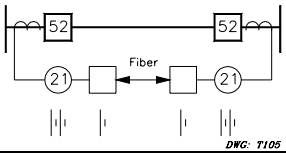
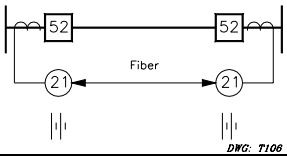
Figure 1.6: Fault Tree for Tone/Microwave Based POTT Scheme With Redundant Relays

Protection Unavailability Comparisons

We have already calculated unavailability for two possible protection schemes. The first was a basic POTT (See Section 4.1.2.2.1.4) scheme with a single relay and a single communications medium. In the second we added redundant protective relays.

The unavailability of each of those systems, and several others to be described later, is shown in Table 2.1.

Table 1.2: Unavailability Comparison of Several POTT Schemes

POTT Scheme	Description	Unavailability x 10^6 Ignoring Zone 1 Coverage	Unavailability x 10^6 Considering Zone 1 Coverage
	Single Relay Single Channel Microwave	2020	1660
	Redundant Relays Single Channel Microwave	1620	1260
	Single Relay Redundant Channels Microwave and Relay-to-Relay on Leased Line	1320	1275
	Redundant Relays Independent Channels Microwave and Relay-to-Relay on Leased Line	920	875
	Single Relay Single Channel Multiplexed Fiber	1620	1440
	Single Relay Single Channel Relay-to-Relay on Dedicated Fiber	1340	1286

Each row of the table above describes a protection scheme. For instance, the first row describes a protection system consisting of a single relay and breaker with associated CTs and VTs at each line terminal, communicating via tone equipment and analog microwave gear. This is the system depicted in Figure 1.3.

While we limited our study to the POTT scheme, the same results would be obtained for any scheme where a communications failure results in a slow trip.

So far we have not considered the role of Zone 1 elements in the fault trees. Zone 1 elements set to 80 percent theoretically cover 100 - 20 - 20 = 60 percent of the line, independent of the channel. That does not imply the Zone 1 elements cover 60 percent of the faults. Fault resistance coverage of the Zone 1 distance elements may be no better than half that provided by the POTT scheme. If we assume one-half, and further assume 25 percent of the faults have enough resistance to (at least initially) not be detectable by Zone 1, then the apparent 60 percent coverage drops to 75 percent · 60 percent = 45 percent. So, less than half the faults might be covered by the Zone 1 elements. To determine the unavailability across all faults that can be seen by either the POTT or the Zone 1 elements, we apply 55 percent of the faults to the unavailability of the POTT fault tree, and the remaining 45 percent of the faults to the unavailability given by the POTT fault tree, with the communications terms set to zero.

For example, assume the unavailability of the POTT scheme is $2020 \cdot 10^{-6}$, and that of the scheme, neglecting the communications, is $2020 - 800 = 1220 \cdot 10^{-6}$. The unavailability across all faults that can be seen by either scheme is: $2020 \cdot 55\% + 1220 \cdot 45\% = 1660 \cdot 10^{-6}$. Alternatively, we could have considered Zone 1 coverage while constructing the fault tree. Figure 1.6 shows how to include the effects of Zone 1 coverage in a fault tree.

Figure 1.7 introduces a new symbol. The triangle is used as a connector that allows us to reuse “Distance Protection at S Fails” without replicating that portion of the fault tree.

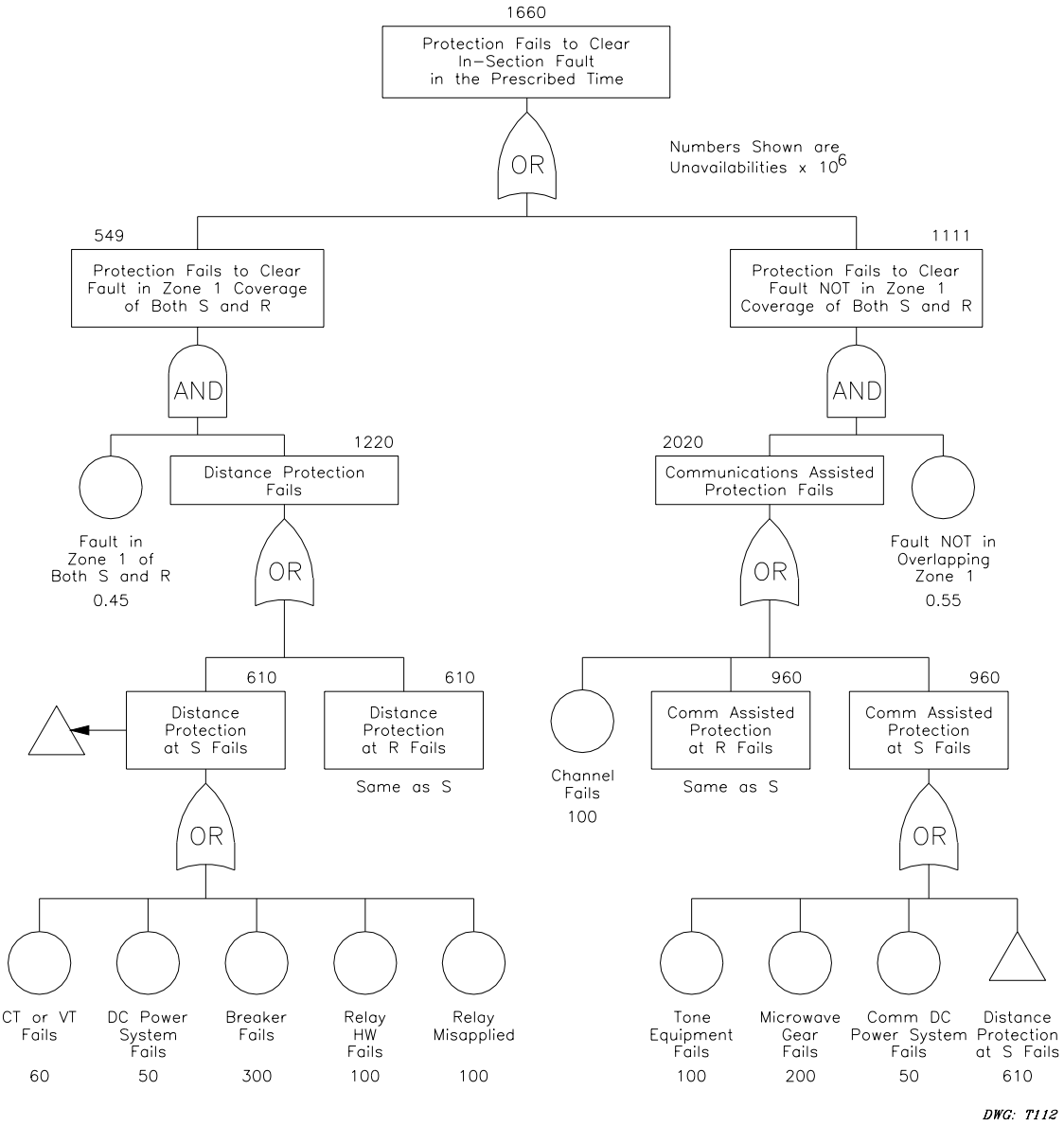


Figure 1.7: Expanded Fault Tree for Tone/Microwave-Based POTT Scheme Showing Effects of Zone 1 Coverage

Unavailability, Frequency of Faults, and Cost

If we assume faults occur randomly and independently of protection system failures, then we can interpret unavailability as the likelihood that the system is not available when a fault happens.

Suppose the unavailability to clear faults in the prescribed time is $2000 \cdot 10^{-6}$. Suppose our power system has 100 lines and each line faults 10 times per year on the average. The system experiences $100 \cdot 10 = 1000$ faults per year. The number of faults we expect to occur when the system is not available is 1000 faults per year $\cdot$ $2000 \cdot 10^{-6} = 2$ faults per year that are not promptly cleared. If actuaries can tell us the cost of

one such uncleared fault, then we could find the cost of this level of unavailability and next evaluate the cost benefit of any proposed improvement.

Analysis Results of Example POTT scheme

The following analysis refers to the results of the last column of Table 1.2: which considers the the effects of Zone 1 coverage.

- Adding redundant relays improves unavailability by 24 percent.
- The improvement is limited because other component unavailabilities, especially the circuit breakers, dominate the fault tree.
- Adding a redundant channel improves unavailability by 23 percent.
- We use a digital relay-to-relay communications scheme on a leased telephone line. The fault tree shows that the unavailability of the redundant channel is relatively unimportant. We assume a channel unavailability of 1000·10-6, or ten times the unavailability of the microwave channel, and still get a large increase. Improving the redundant channel to an unavailability of 100·10-6 would not be of any real benefit.
- Unavailability with a dedicated fiber using traditional multiplex/demultiplex units is 13 percent better than with tone gear and a microwave channel.
- Direct relay-to-relay digital communications over a dedicated fiber using relay-powered transceivers improved unavailability by 23 percent.
- Compared to adding a redundant channel, this method not only improves unavailability but also significantly reduces cost. Relay-powered transceivers cost about 1/10th as much as contact-sensing multiplex/demultiplex units.
- Just improving the communications channel using direct relay-to-relay communication improves unavailability about the same amount as redundant relays or a second channel when the first channel is microwave.
- Adding redundant relays with independent communications channels decreases unavailability by nearly half (47 percent). Adding a redundant channel to a scheme that already employs redundant relays improves unavailability by 31 percent.

Dependability

Dependability is the ability to detect and respond to a fault in a correct and timely manner. Dependable operation requires that the fault be detected (sensitivity), that detected faults in the protection zone be differentiated from those outside the protection zone (selectivity), and that the detection and discrimination effort be fast enough to be of value (speed). A completely dependable relay will always trip properly for a detected fault. This degree of dependability is obtained at the expense of an increased probability of operations when not required.

Sensitivity

Sensitivity is critical to being able to detect high-impedance faults. There are three components to a measurement, accuracy, precision, and resolution. These components are independent qualities of a measurement.

Selectivity

Selectivity is important for relays to be able to discriminate between load and faults and to distinguish one fault location and/or type from another. Sensitivity, or lack thereof, limits selectivity. Consider the two fault locations on either side of breaker 2, represented by F1 and F2 in the system shown in Figure 1.8. The relay to the right of breaker 1 will not be able to discriminate between the two faults by direct measurements of current and/or voltage alone. For these types of cases, fault discrimination is by time and/or communication. An example of discrimination by time is if faults detected in Zone 2 are delayed. Figure 1.8 also illustrates the concept of overreaching. If the sensitivity of Zone 2 is set too high, the relay at breaker 1 may operate for faults inside the customer's load if the customer's protection is slower than the Zone 2 delay. Figure 1.8 also illustrates discrimination by direction. Zone 3 detects faults to the right of the relay and may be used for backup protection of the transformer and generator or to inhibit other relays from operating.

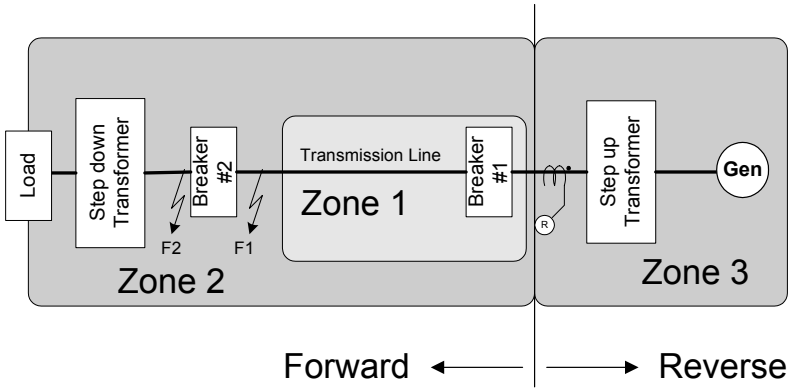


Figure 1.8: Sensitivity Limits Selectivity for Faults F1 and F2

Speed

Speed is important for limiting exposure and potential damage. The time to clear a fault is mainly determined by two elements, the speed of the circuit breaker and the time it takes for the relay to make the decision. Relay decision time is based on three functions inside the relay. Relay designers determine the time needed for two of these functions, filtering to isolate the 60 Hz information and processing the information to determine the appropriate output. The application engineer determines the third function, the time spent waiting for restraints to be removed from external inputs and which inputs will inhibit or delay outputs.

Security

Security, in some respects, reflects the sureness of the relay decision. In the area of protective relaying, it refers to the quality of not operating for faults outside the zone of protection or not operating under heavy load conditions.

MAINTENANCE [6047], [6052], [6073], [6060]

Maintenance has two purposes: to repair relays known to be defective and to verify that relays are not defective. Before the advent of microprocessor-based relays, defective devices could only be found by testing or by incorrect operations. The goal of protective relay testing is to maximize the availability of protection and minimize risk of relay misoperation. With this in mind, we must define adequate test intervals for the various types of protective relaying equipment.

Traditional relays do not provide self-tests or status monitoring, so they require routine testing to verify proper operation. If a problem exists in a traditional relay, the problem may go undetected until routine maintenance is performed or the relay fails to operate for a fault. The reliability of the traditional relay is, therefore, largely dependent on the frequency of routine maintenance.

Digital relay failures can also cause relay misoperation and prevent operation for faults. However, relay characteristics are typically not affected by failures. Failures tend to be significant enough to either generate a self-test failure indication or cause the user to recognize the problem during normal relay operation.

Type Testing

When a utility engineer selects a new relay design, it is essential to test the selected relay to ensure proper operation for the intended application. These tests are referred to as type tests and are usually implemented on a single representative relay from the manufacturer. During type tests, the utility staff is introduced to new relay models and functions. If there are specific application questions, utility staff discusses these questions with the relay manufacturer until there is a clear understanding of all the protective functions. Type tests include detailed tests of the relay characteristics such as mho circle plots, time-overcurrent curve plots, relay element accuracy, etc. The main objective of type tests is verification of the relay algorithms and characteristics.

Commissioning Testing

Utilities typically require commissioning or installation tests of each relay prior to placing the relay in service. Once the utility accepts the results of the digital relay type tests, the requirement for commissioning testing is reduced. The operating characteristics of microprocessor-based relays are consistent, which allows us to rely on the type tests for detailed characteristic tests and focus the commissioning tests on simple tests of the relay hardware.

Digital relay commissioning tests may include tests for calibration, input/output functionality, simple element accuracy tests, etc. Commissioning tests should also verify the effectiveness of calculated relay element and logic settings. Greater

reliance on type tests for the detailed relay characteristic tests is well justified because those characteristics are fixed in the relay algorithms.

Routine Maintenance Testing

Routine testing of protective relays has been the primary method of detecting failures in traditional relays. The only other way of determining that a traditional relay has failed is to observe a misoperation. Routine testing is scheduled on the basis of utility experience with the devices in question. However, there is risk involved, both with performing the test and with leaving the relay untested. The goal of routine maintenance is to verify that the protective relay will not operate unnecessarily and will operate when required.

Typically, routine maintenance is performed at specified intervals. A common belief is that a shorter test interval increases overall system reliability. There are limitations to this statement, however, such as the possibility that a system failure could be introduced while performing routine maintenance. Performing a routine test creates the risk that a functioning relay may be damaged by the tests or may be left in an unserviceable condition following the test.

The time between tests is typically measured in years. If a failed relay does not misoperate in that period, its failure goes unnoticed and unrepaired for what may be a significant portion of the testing interval. So, the risk of leaving the relay untested is that it may not operate properly when necessary.

To schedule routine testing, the utility engineer must balance the risk of leaving a failed relay in service versus the smaller risk of damaging a sound relay. Examining the types of problems that can occur in both classes of relays is often helpful for finding problems that might be present. Then examine the types of tests being performed to see if they are exercising the relays in meaningful ways.

Routine Testing of Traditional Relays

Traditional relays are often built with induction disks or cylinders that turn on jewel bearings. Heavy-duty resistor, inductor, and capacitor networks shape operating characteristics. Springs and levers define operating times. Tests of traditional relays necessarily check the operating characteristics that are affected by the individual components: pickup settings, operating times, and characteristics.

If routine testing detects a problem with a traditional relay, there is no way to know how long the problem has existed. The only date available for reference is the last time the relay was shown to operate properly in a fault record or a test report. The relay could have failed on the day following the last correct operation, on the day before this misoperation, or on any day in between.

Routine Testing of Digital Relays

Digital relays are built using a microprocessor, an ac signal data acquisition system, memory components containing the relay algorithms, contact inputs to control the relay, and contact outputs to control other equipment. Digital relay operating

characteristics are defined by the algorithms and settings contained in the relay memory.

Digital relays are often equipped with automatic self-test functions that verify correct operation of critical relay components. If a self-test detects an abnormal condition, it can close an output contact, send a message, or provide some other indication of the failure. When the alarm occurs, a technician can be dispatched to repair or replace the device quickly.

It is helpful to define the requirements of digital relay routine maintenance by dividing the hardware into three categories and specifying maintenance practices that adequately test each section. For the purposes of testing, it is convenient to divide the relay into the following three sections:

- Analog Input Section
- Contact Input/Output Circuitry
- Processing Section

The analog input section is typically monitored by automatic self-testing. This may be somewhat limited because a steady-state condition cannot be fully defined. With a protective relay, there are often many steady-state conditions possible under each mode of operation. Since the analog input portion of the digital relay is only partially self-tested, routine maintenance assists in verification of the analog measuring components.

Many digital relays offer metering features that give the user a convenient means of verifying the accuracy of the relay analog input section. The user can verify metering quantities and be assured the relay is using valid data for its relay element computations. This practice is sound if the digital relay uses the same measuring circuitry for both metering and relaying. However, if the relay uses separate circuitry for its metering functions, the metering data checks only the components common to both the metering and relaying circuitry.

The contact input/output circuitry is another part of the digital relay that allows only partial automatic testing. For this reason, it may be appropriate to implement a routine trip check. Many digital relays provide a trip feature that allows the user to locally or remotely trip the relay. The trip check verifies the trip circuit wiring and the integrity of the trip coil. This trip command feature provides a convenient means of tripping the circuit breaker without injecting a simulated fault into the relay. If the relay is routinely operating for faults, the actual relay operations may be adequate verification of the relay input/output functions.

The digital processing section, typically a microprocessor, is the interface between the analog input section and the contact input/output section. Since the analog and contact input/output sections cannot function without the processing section, normal relay use and maintenance checks act as routine verification of the microprocessor. Additionally, manufacturers are able to offer very thorough self-tests to continually monitor the status of the computer.

Utility engineers should work closely with relay vendors to determine which relay functions are not checked by relay self-tests and how those functions should be

checked in the field. There are typically no special tests required for the processing section.

Many of the maintenance features are executable by remote command and often could replace routine maintenance altogether. Also, the analysis of digital relay fault data is comparable to routine relay maintenance. Those relays that do not encounter faults may require more thorough routine maintenance checks.

Because the digital relay provides an indication when a problem occurs, the possibility that a failed digital relay could remain in service for a significant amount of time is reduced. If the utility monitors relay self-test alarm contacts, a failed relay can generally be repaired or replaced within hours or days of a failure.

Digital Relay Data Analysis

As a minimum, digital relay self-tests include tests of memory chips, a/d converter, power supply, and storage of relay settings. These periodic self-tests monitor the status of the digital relay and close an alarm contact when a failure is detected. Additionally, the digital relay may disable trip and control functions upon detection of certain self-test failures. Since the relay self-tests are executed often, component failures are usually discovered when the failure occurs.

Digital relays provide event reporting and metering features that supplement routine maintenance. Event reports typically provide a record of each relay operation with the same resolution as the sample rate of the digital relay. If testing personnel devote a small percentage of their time to analyzing these fault records, they can find relay problems displayed in the event report data. Analysis of actual fault data is a true test of the instrument rather than a simulated test. Careful analysis of relay event reports and meter information indicates problems that could otherwise go undetected by digital relay self-tests.

Event reports can also indicate problems external to the digital relay. Transformers, trip circuits, communications equipment, and auxiliary input/output devices are examples of external equipment that may be monitored indirectly using the event report.

A Summary of Relay Maintenance Concepts

The features of digital relays reduce routine tests to a very short list: meter checks and input/output tests. Routine characteristic and timing checks are not necessary for digital relays. Probability analysis shows that relays with self-tests do not need to be routinely tested like relays without self-tests. If the relay is measuring properly, and no self-test has failed, there is no reason to test the relay further.

Use the digital relay reporting functions as maintenance tools. Event report analysis should supplement or replace routine maintenance checks of relays with self-tests. Event report analysis increases a tester's understanding of the digital relay and of the power system.

Because self-tests quickly indicate the vast majority of relay failures, the MTBF of a digital relay does not have a large impact on the power system unavailability. When a relay is equipped with self-tests, the benefit of a high MTBF is that fewer relays

need replacement or repair. A high MTBF saves maintenance time and money. Relay self-testing saves routine testing time. When a relay is not equipped with self-tests, a high MTBF and a short test interval are both essential for minimizing system unavailability.

Reducing the complexity and frequency of routine digital relay tests saves labor. These labor resources can then be applied to more frequent and complete tests of traditional relays. The result will be higher overall reliability and availability from all relays, both digital and traditional.

2 MATHEMATICS AND ENGINEERING FUNDAMENTALS

ENGINEERING METHODOLOGY

Engineering design is a process. As with many other processes, following the steps of the process provides no guarantee against failure but does enhance the chance of success. Each specific design application will have unique features thus requiring additional engineering in every application. Feedback in the design process takes into account that requirements can change or become more complicated. The design process should result in a system that meets all the requirements and specifications. The quality of the end product can be no better than the accuracy and completeness of the specifications.

Problem definition

Because problems are usually more complex than they seem, defining the problem to be solved by a design can be more difficult than developing the solution. The list of issues the solution system is to address and issues it is not to address is based on this definition. The problem can initially seem to be simple, such as the tripping of a home circuit breaker. But there can be many reasons for a circuit breaker to trip. Was the circuit breaker defective or did it trip to protect the circuit from an overloaded condition? Was there too much current for the circuit rating? Is the wiring faulty? Each of these reasons requires a different solution. None of them would have been resolved by simply resetting the circuit breaker.

Of course, the more complex the problem, the more effort is required to flush out the range of appropriate solutions. Be careful not to rush to a solution that solves either the wrong problem or a nonexistent problem. A thorough, accurate definition of the problem is the most important part of engineering design. The challenge in this phase is determining when you have collected adequate information to lead to a viable and economical solution.

System specifications

System specifications are measurable characteristics that describe the behavior of a system or action that solves the problem identified in the above engineering phase. Specifications constrain the solution to having a finite set of characteristics. Some of these characteristics have ranges of acceptable operation while others have exact attributes. Specifications are the targets that the solution must shoot for.

Specifications have a secondary function of validation. During subsequent design activities, the proposed solution must be tested for compliance to the specifications. If the problem definition phase was correctly completed and the proper specifications generated, the problem will be solved if and only if the solution system meets all the specifications.

Solution identification

Solution proliferation

Only very simple problems have obvious very best solutions. All other problems require a methodical search for possible solutions. At this point in the design phase, gather as many possible solutions as can be found. A fundamental rule is: the higher the number of identified potential solutions, the greater the chance of finding the optimal solution.

Solution selection

There will probably be many good potential solutions but few, if any, that exactly meet the requirements. Create a weighted matrix to rank the usefulness of each solution. List all specifications in the right hand column of the matrix and the various design approaches across the top. Then assign a subjective weighting or multiplier to each specification, giving the highest weight to the most critical specifications. Enter the product of the specification weight and the degree to which the design approach meets that specification for each element under the different approaches. The sum of the column with the highest total is the favored approach for the problem under the given constraints.

If the chosen solution does not meet all the specifications, you may need to negotiate a compromise on the specifications or enhance the design approach (at some cost) to meet the requirements. If there are no suitable solutions, the choices are: look for more solutions, reevaluate the specifications, study the problem for ways to relax the specifications, or stop the design altogether because it is unfeasible. The first three alternatives represent the iterative nature of the design process. The fourth alternative, eliminating weak or unsuitable design approaches, has far fewer economic consequences at this point than later in the design cycle.

Design Implementation

So far, the process has only created a theoretical design and possibly some preliminary modeling or proof-of-concept studies to better qualify or rank the different approaches. The design implementation phase breaks the problem into manageable parts and assigns resources to the various parts. Such resources include engineering time, development tools, and of course, money. The process of developing many modules simultaneously is called concurrent engineering. A good approach to dividing the project up is to encapsulate it in such a way that each part can be tested separately from all others. The test plan should also ensure that minimal effort is needed to merge the various modules into the final system.

As testing and design progress, some modules may still not meet specifications. At this point, consider the same four alternatives that were discussed at the end of the previous section. Assuming all is progressing satisfactorily, testing processes and result documentation provide valuable and necessary information for validating redesigns and maintenance.

Final testing

A test plan should verify that the newly designed system meets all specifications. It is desirable that testing is time invariant, which means that once a system tests as valid, it is valid for all time. Software is time invariant. Excluding the software virus, any software bugs that show up after the equipment has spent time in the field were originally shipped in the new equipment. Hardware, however, is not time invariant since mechanical, thermal, and electrical stresses eventually wear out equipment.

Unfortunately, testing can only identify existing faults. It cannot verify the complete absence of faults. Power systems are far too complex to permit exhaustive testing from both a time and an economic perspective. A good test plan is fast and effective, providing repeatable expectation results. The bibliography at the end of this section lists references for additional information on developing approaches to testing and developing test plans.

Documentation

Documentation is time consuming, but vital for good life cycle engineering. It covers test documents, manufacturing plans and instructions, patents, users' manuals, field maintenance guides, application notes, and so on. These should be cross-referenced for easy information retrieval. Generating good documentation and maintaining documentation to track revisions requires meticulous attention but can be invaluable.

Installation and Commissioning

Good designs have thorough documentation and unambiguous labeling to minimize the chances of improper installation. Following well-documented procedures ensures nothing is forgotten. The less complicated the interface, the lower the risk of improper installation. Employing multiple levels of inspection also helps ensure proper installation and minimize potential damage to equipment.

Continuity, voltage profiles, and input-output actions tests are examples of multiple levels of inspection. The continuity test uses an ohmmeter to verify that equipment inputs and outputs have low resistance connections to the proper locations. Add to the thoroughness of the inspection by using a highlighter to identify circuits that have been checked. Correct any errors found before proceding with the inspection. Once the continuity inspection is completed, you can energize the system. A good test procedure identifies voltages or currents at key locations. A chart is a good checklist for this inspection. Finally, applying known inputs and verifying the operations for proper response or outputs verifies system functionality.

BASIC ELECTRICAL SYSTEMS THEORY

Signal Representations

We can observe any signal from a perspective that focuses on the characteristics that have the greatest interest to us. Fourier analysis shows that we can represent any periodic waveform as the superposition sum of pure sine waves of different

amplitudes and phases for the fundamental and harmonics. We can do the same for a periodic signal if we assume that the signal is periodic over the interval of observation. The four domains discussed below demonstrate how each domain presents pertinent data.

Time Domain

Equation 2.1 is the mathematical representation for a single frequency sinusoidal signal. The four dimensions of freedom are amplitude, frequency, phase, and time. You must know all four variables to determine the explicate value x(t) at any point in time. Complex signals may have mathematical representations that are too complicated to be meaningful just from observation. We frequently use time domain analysis to observe peak amplitude and/or timing relationships on an oscilloscope.

$$x(t) = Am \cdot \sin(2 \cdot \pi \cdot f \cdot t + \varphi) \qquad \text{Equation 2.1}$$

Frequency Domain – Fourier Series Analysis

Consider the time domain representation of a square wave as represented by Equation 2.2. We know from Fourier analysis that we can represent such a signal as a sum of sine and cosine function of varying amplitudes and at integer multiples of the fundamental frequency. Recall that this frequency is the inverse of the square wave period, T. Equation 2.3 shows the expression representing any periodic signal.

The terms *cos(n ω_0 t)* and *sin(n ω_0 t)* in Equation 2.3 describe fixed frequency sinusoidal signals that are common to all periodic signals. The only variables that depend strictly upon the characteristics of the signal under investigation are the coefficients $B1_n$ and $B2_n$. The magnitude and phase of the n^{th} harmonic of time domain signal x(t) are expressed by Equation 2.4 and Equation 2.5, respectively. The first harmonic is called the fundamental and the 0^{th} harmonic is the dc component. This mechanism of separating one particular frequency from a group of frequencies is fundamental to power system protection using the magnitude and phase relationships of voltages and currents.

$$x(t) = Am \cdot u(t - n \cdot \tau) - Am \cdot u(t - m \cdot \tau) \qquad \text{Equation 2.2}$$

for n = 0, 2, 4, 6, …. And m = 1, 3, 5, 7, …

$$x(t) = \sum_{i=0}^{\infty} Bl_i \cdot \cos(i \cdot \omega_0 \, t) + j \sum_{k=1}^{\infty} B2_k \, m \cdot \sin(k \cdot \omega_0 \, t) \qquad \text{Equation 2.3}$$

where $\omega_0 = 2\,\pi/T$

$$Xm(n\,\omega_0) = \sqrt{Bl_n^2 + B2_n^2} \qquad \text{Equation 2.4}$$

$$Xp(n\omega_0) = \arctan\left(Bl_n / B2_n\right)$$ Equation 2.5

Fourier analysis is a whole topic in itself; many good college texts cover the subject thoroughly.

Phase Domain

In the phase domain, the fundamental frequency is assumed to be fixed and time, other than for establishing a reference point, is inconsequential. Therefore the characteristics of a signal represented by Equation 2.1 can be expressed in the two remaining degrees of freedom, amplitude and phase. Equation 2.6 provides the same information as Equation 2.1 if the fundamental frequency, f, is known or is normalized to unity. Such representations are common in single frequency systems such as power systems. (See Bosela reference, Ch. 1, Pg. 13 [6] for additional information.)

$$X = Am \angle\varphi$$ Equation 2.6

Phasors are normally used to represent a system of signals that operate at one frequency. Equation 2.7 through Equation 2.11 mathematically represent two such sinusoidal signals that are also illustrated in Figure 2.1. Three independent variables describe a sinusoid, frequency, amplitude, and phase. Phase is related to the variable, time, insomuch as phase is relative to the t = 0. Phase between two sinusoidal signals is only constant when the two signals are at the same frequency.

$$X(t) = Xm \cdot \cos(2\pi f t)$$ Equation 2.7

$$Y(t) = Ym \cdot \cos(2\pi f (t + td))$$ Equation 2.8

$$Y(t) = Ym \cdot \cos(2\pi f t + \theta)$$ Equation 2.9

$$\theta = 2\pi f td$$ Equation 2.10

$$f = 1/Pd$$ Equation 2.11

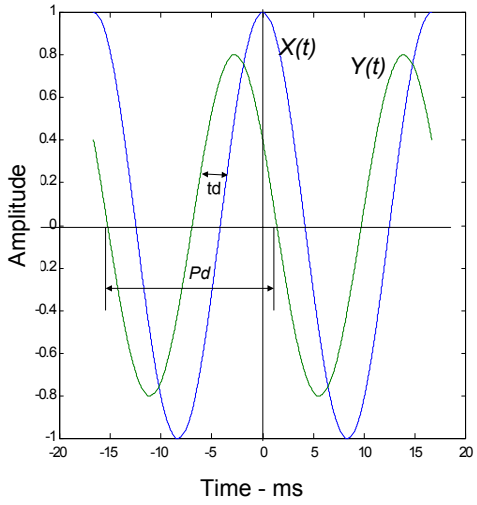


Figure 2.1: Single Frequency Sinusoidal Signals

As Equation 2.12 illustrates, we can also represent sinusoidal signals graphically as phasors, again under the assumption that the signals are operating at the same frequency. The two degrees of freedom for phasors are magnitude (usually with units RMS) and phase (with units of degrees or radians) as expressed in Equation 2.12. Static phasor representations of sinusoidal signals require that all signals be at the same frequency. Dynamic representations allow signals to have time-varying RMS amplitude as well as different frequencies. Such dynamic behavior would result in vectors rotating around some fixed origin while the vector length would be modulated.

$$X_{polar} = X_{RMS} \angle\theta \quad \text{where } X_{RMS} = X/\sqrt{2} \qquad \text{Equation 2.12}$$

Complex Variables [Bosela Ch. 1, Pg. 6]

Because phasors discussed thus far use the polar notation, Figure 2.2 suggests another form of vector representation using rectangular notation as expressed by Equation 2.13 and Equation 2.14. (see Bosela reference [6].) The imaginary operator simply implies a 90-degree phase shift. It can now show that a sinusoid of an arbitrary magnitude and phase can be represented as the superposition sum of two signals, one a cosine wave and one a sine wave with the appropriate amplitudes as expressed by Equation 2.15.

$$X_{COMPLEX} = X_{RMS}\cos(\theta) + jX_{RMS}\sin(\theta),\ j = \sqrt{-1} \qquad \text{Equation 2.13}$$

$$X_{COMPLEX} = X_{RMS}(re) + jX_{RMS}(im) \qquad \text{Equation 2.14}$$

$$\begin{aligned} Y(t) &= Y \cdot \cos(2\pi f t + \theta) \\ &= Ym \cdot \cos(\theta) \cdot \cos(2\pi ft) + Xm \cdot \sin(\theta) \cdot \cos(2\pi ft) \end{aligned} \qquad \text{Equation 2.15}$$

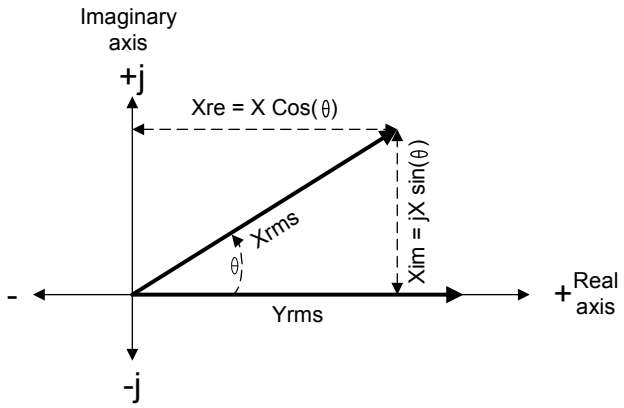


Figure 2.2: Phasor Representations of Signals X and Y

The transformation from Equation 2.15 to Equation 2.12 uses the mathematical identities in Equation 2.16 and Equation 2.17. These identities can also transform Equation 2.8, the exponential form shown by Equation 2.18, provided that Equation 2.8 has been normalized by the operating frequency, (2 π f t).

$$\cos(\alpha) = \frac{e^{j\alpha} + e^{-ja}}{2} \qquad \text{Equation 2.16}$$

$$\sin(\alpha) = \frac{e^{j\alpha} - e^{-ja}}{j2} \qquad \text{Equation 2.17}$$

$$Y_{exp} = Y_{RMS}\, e^{j\theta} \qquad \text{Equation 2.18}$$

The equations in Table 2.1 summarize the common methods for expressing sinusoidal signals as phasors. The variables "c" and θ in Table 2.1 are computed from Equation 2.19 and Equation 2.20, respectively, and represent a rectangular-to-polar coordinate conversion. Equation 2.21 and Equation 2.22 allow conversion of vectors from polar back to rectangular coordinates.

$$|c| = \sqrt{a^2 + b^2} \qquad \text{Equation 2.19}$$

$$\theta = \arctan\left(b/a\right) \qquad \text{Equation 2.20}$$

$$a = |c| \cdot \cos(\theta) \qquad \text{Equation 2.21}$$

Error! Objects cannot be created from editing field codes. Equation 2.22

Table 2.1: Phasor Form Identities

Rectangular Form	Complex Form	Exponential Form	Polar Form	Phasor Form
a + jb	|c| •[cos(θ) + jsin(θ)]	|c| $e^{j\theta}$	|c| ∠θ	c
a – jb	|c| •[cos(θ) – jsin(θ)]	|c| $e^{-j\theta}$	|c| ∠-θ	c^*

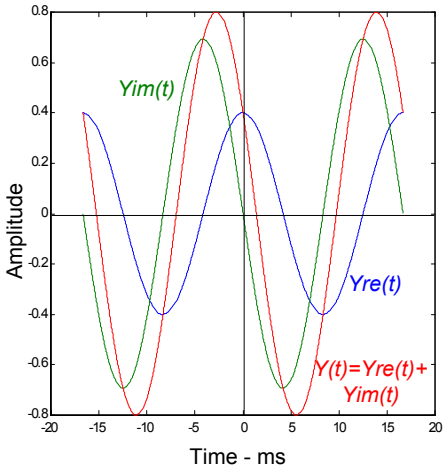


Figure 2.3: Superposition Sum of Real and Imaginary (orthogonal) Sinusoidal Signals

The relationship expressed in Equation 2.15, as illustrated in Figure 2.3, is the basis for Fourier analysis of periodic waveforms. Of course the concept of imaginary numbers and signals is an artifact of orthogonal basis vectors used to represent one signal with a phase shift by two signals with no phase shift. In reality, the imaginary terms are no more imaginary than the y-axis on a two-dimensional x-y plot.

Vector Algebra

Vectors as expressed in Equation 2.12 and illustrated in Figure 2.2 have a math of their own. Add vectors in either polar or rectangular coordinates as represented in Table 2.1.

Vector addition and subtraction in polar coordinates

Adding two vectors using polar coordinates is easy to visualize. It involves translation of the origin of one vector to be added by connecting the tail of one vector to the head of another while maintaining the magnitude and direction of the original vectors. Figure 2.4 illustrates the process for adding vectors C1 and C2. The origin of C2 is translated to C2' and the resultant vector, C3, is determined by drawing a new vector from the tail of the first vector to the head of the last vector. You can add vectors in any order with identical results.

Vector addition and subtraction in rectangular coordinates

Adding vectors in rectangular coordinates requires that the real and imaginary vectors be algebraically summed separately. For the example shown in Figure 2.4, a3 = a1+a2 and b3 = b1+b2. Applying Equation 2.19 and Equation 2.20 to a3 and b3 results in the vector C3.

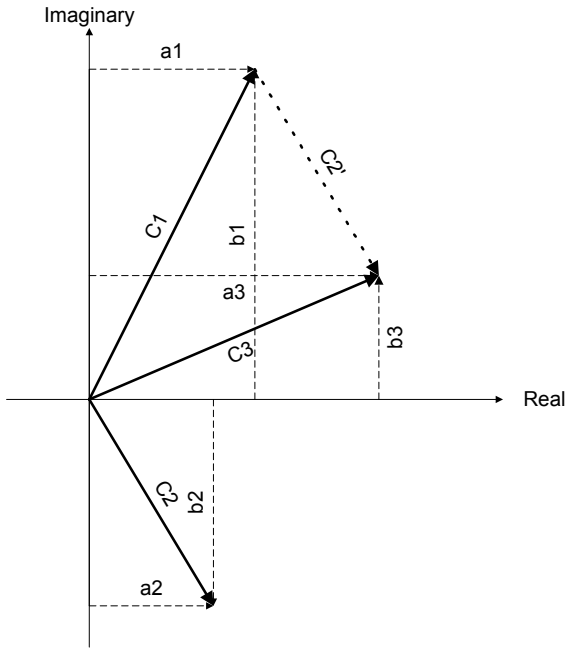


Figure 2.4: Graphical Vector Addition

Subtracting vectors in polar coordinates requires adding 180° to the negated vector (the vector being subtracted) and then adding the vectors as described above. Changing the algebraic sign on the negated vector and adding the real and imaginary parts subtracts vectors in rectangular coordinates.

Vector multiplication and division

To multiply vectors use vectors represented in either exponential or polar form. Using polar notation, multiply the magnitudes and add the angles. For example, given vectors C1 and C2, at angles θ1 and θ2, the resultant product, C3, is determined from either Equation 2.23 or Equation 2.24.

$$C3 = C1 \cdot C2 \angle (\theta 1 + \theta 2) \qquad \text{Equation 2.23}$$

$$C3 = C1 \cdot e^{j\theta 1} \cdot C2 \cdot e^{j\theta 2} = (C1\ C2)\ e^{j(\theta 1 + \theta 2)} \qquad \text{Equation 2.24}$$

To divide two vectors, simply divide the magnitude and subtract the denominator phase from the numerator phase. Equation 2.25 and Equation 2.26 illustrate this process where C3∠θ3 = C1 ∠θ1 / C2 ∠θ2.

$$C3 = \left(C1 \big/ C2\right) \angle (\theta 1 - \theta 2) \qquad \text{Equation 2.25}$$

$$C3 = \left(\frac{C1 \cdot e^{j\theta 1}}{C2 \cdot e^{j\theta 2}}\right) = \left(C1 \big/ C2\right) \cdot \left(e^{j\theta 1} \cdot e^{-j\theta 2}\right) = \left(C1 \big/ C2\right)\ e^{j(\theta 1 - \theta 2)} \qquad \text{Equation 2.26}$$

Per Unit Computations

For additional information, consult any quality text on the fundamentals of power system analysis. The reference for the companion Bosela text is Ch. 5, pg. 123-155. [6,10, 11, 15] Section 11.10.5 in Appendix 11 also has a discussion of per-unit calculations.

Three Phase AC Theory

We are assuming that readers have a rudimentary knowledge of this subject. Refer to the companion text by Bosela Ch. 1, pg. 37-44 [6] for additional information????.

Transmission Line Models

Transmission lines and distribution lines are in the strictest sense conductors of electrical energy. They consist of one or more energized lines and a neutral line. Utilities using multigrounded neutral systems tie the neutral wire to an earth ground at multiple places along the line length. Lines in general refer to bipolar and unipolar dc transmission lines, single and three phase ac overhead transmission and distribution lines, and single and multiphase underground cables.

The line model chosen to represent the characteristics of an electrical line depends on three factors: 1) the frequency range under consideration, 2) the degree of accuracy required, and 3) the available data on which to base the model. For background information on mathematical models of power lines, refer to the Bosela reference text.6

Single-Phase Representations

Single-phase models usually include the electrical characteristics of the supply conductor but rarely consider parameters associated with the return path. If return path considerations are included, they are generally included in the supply path. Splitting the line into a supply conductor and a return conductor usually requires a multiphase line model, as discussed in section 0.

LR Models

The most basic line models include approximations of the line self-impedance or positive-sequence impedance. Nominal values for common conductors are provided in numerous texts and wire vendor data sheets.[6, 7] Further simplifications are possible depending on the expected range of frequencies for signals that will be imposed on the line. If the source is dc, then consider only the resistive component of the line. For ac signals and dc signals including transient effects, consider both the resistance and inductance until either the reactive impedance is much greater than the resistance or the error introduced by ignoring the resistance is acceptable. LR models are also suitable for short (zero to 10 miles) single and multiphase bare overhead lines when they are modeled as three single-phase lines.

LRC Lumped Parameter Pi Models

There are two different uses of the LRC transmission line models. The first use is for studying systems for steady-state phenomena only. It is then appropriate to use the LRC model regardless of line length. The LRC line model is also appropriate for modeling medium length (10-30 miles) bare overhead lines in transient studies. Only use single-phase LRC models to model single-phase lines.

The nominal line-to-ground capacitance is usually evenly distributed between two capacitors that are placed next to the line terminals as shown in Figure 2.5.

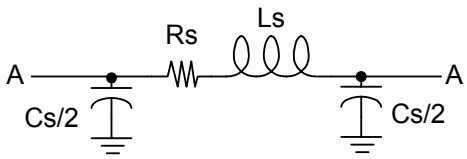


Figure 2.5: Single-Phase Lumped-Parameter Line Model

Distributed Line Parameter

Electromagnetic Transient Program (EMTP) studies use distributed parameter line models for modeling bare overhead lines longer than 30 miles. The chief characteristics of this model are the characteristic impedance and the propagation time. When dealing with long lines, remember that the effects of transient reflections and Ferranti voltage rise occur frequently on long, improperly terminated transmission lines.

This line model is appropriate for modeling single-phase or single-phase representations of balanced three-phase lines that have low losses (the resistance is small relative to the reactive impedance of the lowest signal frequency).

There are one-to-one correlations between the line inductance and capacitance shown in Figure 2.5 and the characteristic impedance, Zc, and the travel time, τ. Equation 2.27 and Equation 2.28 express the relationships for the lossless line models. If Ls and Cs in these equations have units per unit length, then the total travel time is determined by multiplying by the line length. Losses can be included by modifying Zc computed in Equation 2.27 to be Zc' computed by Equation 2.29.

(Need references for formal development of distributed line parameter model)????

$$Zc = \sqrt{\frac{Ls}{Cs}} \qquad \text{Equation 2.27}$$

$$\tau = \sqrt{Ls \;\; Cs} \qquad \text{Equation 2.28}$$

$$Zc' = \sqrt{\frac{Zc + Rs}{Cs}} \qquad \text{Equation 2.29}$$

Frequently the characteristic impedance is also called the surge impedance. This impedance is real in value, rather than complex. It is the impedance of the

transmission line and does not include the terminating impedances at the opposite ends of the line. If the transmission line is not terminated into its characteristic impedance, then the mismatched impedance generates reflections.

Equation 2.30 shows the amount of reflection, expressed as a dimensionless reflection coefficient that is determined by the degree of mismatch. In this equation, *Zt* is the terminating impedance and *Zc* is the line characteristic impedance. This coefficient of reflection can take on values between –1 and +1. As shown in this equation, if the line terminates in its characteristic impedance, the coefficient of reflection is zero. Transmission lines that have loads matched to their characteristic impedance generate no reflections.

$$k = \frac{Zt - Zc}{Zt + Zc} \qquad \text{Equation 2.30}$$

For termination less than the characteristic impedance, the reflected signals are the opposite sign of the incident initiating signal. If the source impedance is different from the characteristic impedance, additional reflections occur when the reflection from the receiving end reaches the termination at the sending end. At any time and any point on a transmission line, the voltage is the algebraic sum of incident wave plus all reflected waves.

Line terminations, in general, are any place where the impedance changes. It may be where two transmission lines with different characteristic impedances connect or where a device is tapped into the middle of a single transmission line. Consider two connected transmission lines as one line, since there are no reflections generated by impedance mismatch.

Figure 2.6 is a visual aid for analyzing voltage reflections on transmission lines. Before the advent of digital computer programs such as EMTP, lattice diagrams were a popular tool for studying transients generated by switching, faults, and lightning strikes. Greenwood presents a detailed analysis of insight-based transient analysis.[8] This diagram assumes that the source is terminated in impedance *Zsend* and the receiving end is terminated in impedance *Zrecv*. Use Equation 2.30 to determine the two different coefficient reflections, *Kr* and *Ks*.

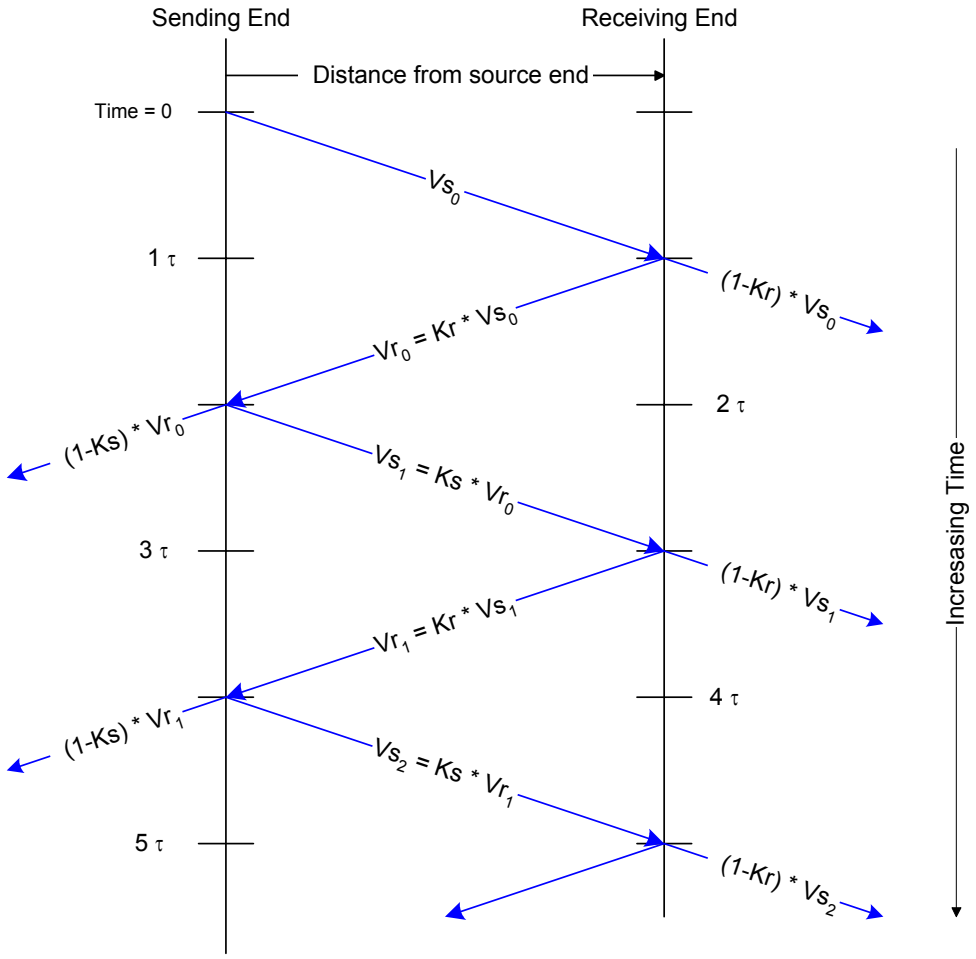


Figure 2.6: Lattice Diagram for Single Transmission Line With Source Reflection, Ks, Receiving Reflection, Kr and Propagation Travel Time, τ.

At time equal to zero, a step voltage is applied to the transmission line at the sending end. As time increases, the wave front propagates toward the receiving end. Each time the wave front reaches a termination; part of the signal reflects back toward the sending end. The other part of the signal is either absorbed by the terminating impedance or transmitted down another section of transmission line. The system represented by Figure 2.6 assumes no reflections back from signals refracted to mismatched terminations beyond the sending and receiving ends.

To use the diagram, first select the point of interest on the transmission line by moving horizontally from the sending end toward the receiving end. Then move down the diagram (representing increasing time) until intersecting one of the diagonal lines representing a signal wave front. At each new wave front, the new voltage is added to existing voltages. The voltage at the predetermined point on the line appears to jump in steps, either increasing or decreasing depending upon the sign of the reflection coefficient.

For example, imagine a strictly hypothetical case where the sending end impedance is zero and the receiving end is an open circuit. In this case, the reflection from the

receiving end would increase the line to *2Vs,* while the reflection from the sending end would decrease the line voltage to zero. Theoretically, the line voltage would oscillate indefinitely between *2Vs* and zero. However, losses in the line, as well as the impossibility of zero source and infinite receiving end impedance, make this unrealistic.

Losses can be included into this model by computing a loss reflection coefficient, *Kloss,* based on a new characteristic impedance determined from Equation 2.30. Subsequently, the new coefficients for the model presented in Figure 2.6 are represented by Ks' and Kr' from Equations Equation 2.31 through Equation 2.23, below. For finite *Rs*, *Kloss* is always less than unity and the reflections will eventually decay to zero.

$$Kloss = \frac{Zc' - Zc}{Zc' + Zc} \qquad \text{Equation 2.31}$$

$$Ks' = Ks \cdot Kloss \qquad \text{Equation 2.32}$$

$$Kr' = Kr \cdot Kloss \qquad \text{Equation 2.33}$$

It is easy to imagine the difficulty of modeling multiple transmission lines with differing travel times and characteristic impedances. Such intuitions are very useful if not absolutely necessary when validating EMTP models. EMTP is invaluable for developing a sense of what kind of voltage and current transients might be generated by a lightning surge as it propagates down a transmission line into a substation. This tool is also good for developing intuitions about transient behavior.

Because lattice diagrams are strictly a time domain tool, inductive and capacitive terminations give rise to exponential responses. Capacitive terminations change with time from short circuits to open circuits as the capacitor charges. Inductive terminations change from open circuits to short circuits. Termination in either device results in time-varying coefficients of reflection.

Multiphase Lumped Parameter Line Models

Multiphase line models shown in Figure 2.7 include the effects of mutual coupling between phases. For phase A, the parameters RAA and LAA are identical to those defined for the single-phase case and shown in Figure 2.5 for the series impedance. Similarly, RBB, LBB, RCC, and LCC are the series resistance and inductance for phases B and C.

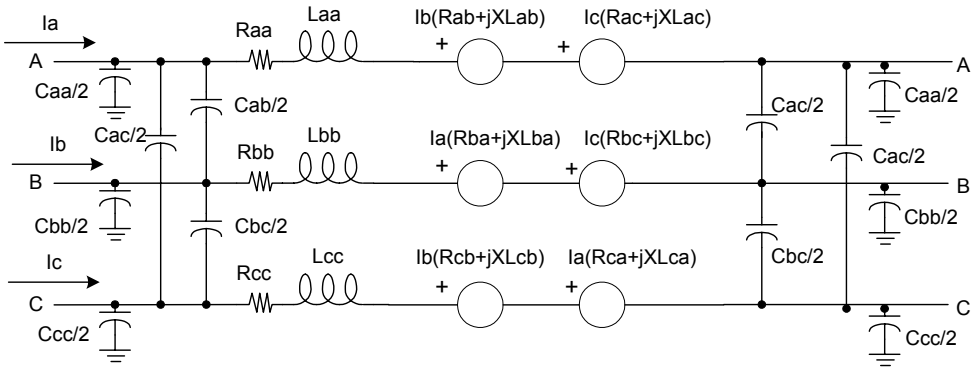


Figure 2.7: Lumped-Parameter Electrical Model of a Three-Phase Transmission Line

$$\begin{bmatrix} Z_{AA} & Z_{AB} & Z_{AC} \\ Z_{BA} & Z_{BB} & Z_{BC} \\ Z_{CA} & Z_{CB} & Z_{CC} \end{bmatrix} \qquad \text{Equation 2.34}$$

Equation 2.34 mathematically describes the impedance network for this line model. The inductive coupling between all phases causes a current in one phase to induce a voltage in another phase, a magnitude equal to the product of primary phase current and the mutual impedance between the two phases. Figure 2.8 illustrates this point, showing a hypothetical experiment with the sending end open and the receiving end shorted to ground. Consider a current injected into phase A equal to I_A. The three-phase-to-ground voltmeters measure the voltages at the sending end according to Equation 2.35 through Equation 2.37. Only the mutual impedance of coupled transmission lines generates the voltages in phases B and C. Individually injecting currents in phases B and C and recording the voltages produced in all three phases gives similar results. Using superposition, compute each of the three-phase voltages from Equation 2.38 through Equation 2.40 or as a single equation in matrix form shown in Equation 2.41.

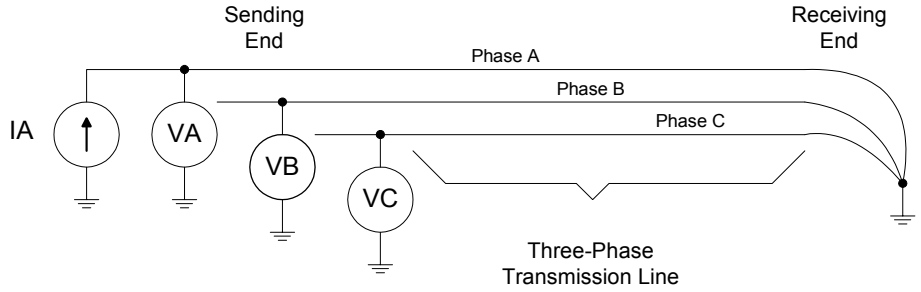


Figure 2.8: Experiment for Determining Mutual Impedance

$$V_A = Z_{AA}\ I_A \qquad \text{Equation 2.35}$$

$$V_B = Z_{AB}\ I_A \qquad \text{Equation 2.36}$$

$$V_C = Z_{AC}\ I_A \qquad \text{Equation 2.37}$$

$$V_A = Z_{AA}\ I_A + Z_{AB}\ I_B + Z_{AC}\ I_C \qquad \text{Equation 2.38}$$

$$V_B = Z_{BA}\ I_A + Z_{BB}\ I_B + Z_{BC}\ I_C \qquad \text{Equation 2.39}$$

$$V_C = Z_{CA}\ I_A + Z_{CB}\ I_B + Z_{CC}\ I_C \qquad \text{Equation 2.40}$$

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \begin{bmatrix} Z_{AA} & Z_{AB} & Z_{AC} \\ Z_{BA} & Z_{BB} & Z_{BC} \\ Z_{CA} & Z_{CB} & Z_{CC} \end{bmatrix} \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \qquad \text{Equation 2.41}$$

To complete the line model, two sets of capacitors model the line-to-line and line-to-ground capacitance. As in the single-phase case shown in Equation 2.13, the total capacitance is divided equally and placed at the two ends of the transmission line.

Figure 2.9 shows that the currents at the sending and receiving ends of the transmission line actually split into two paths. One path for the current, $Iseries_{abc}$, flows toward the terminals at the far end of the line. The other current, $Ishunt_{abc}$, is shunted through the capacitors at the near terminals. Nodal analysis from basic electrical circuit theory allows us to compute the currents into the network representing the multiphase transmission line.

Use Equation 2.42 to compute *Is[abc]series* from the terminal voltages at the sending and receiving ends. Then use formulas *Zii* is $Rii + j\omega Lii$ *and* $Yii = j\omega Cii$ to find the elements of the impedance matrix. Compute the Is[abc]shunt from each terminal end voltage separately with Equation 2.43. Use Equation 2.44 to compute the sending end currents but only if all six terminal voltages are known, because these are necessary for determining the three terminal currents. Generate similar expressions for computing the receiving end currents.

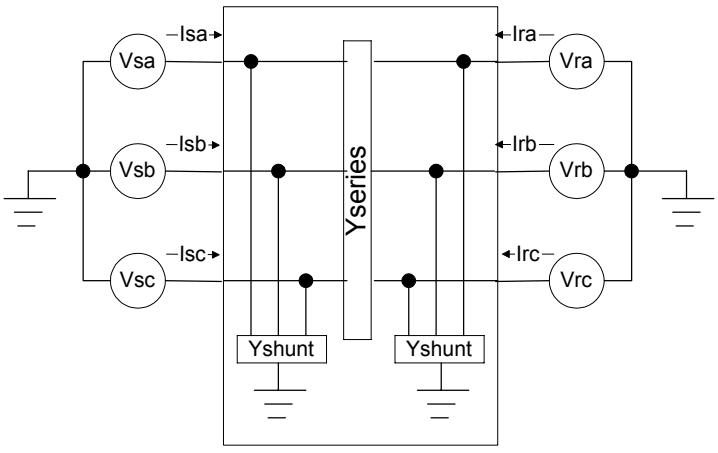


Figure 2.9: Voltage and Current Relationships for a Three-Phase Line Model

$$\begin{bmatrix} \mathrm{Isa}_{\mathrm{series}} \\ \mathrm{Isb}_{\mathrm{series}} \\ \mathrm{Isc}_{\mathrm{series}} \end{bmatrix} = \begin{bmatrix} \mathrm{Z}_{\mathrm{AA}} & \mathrm{Z}_{\mathrm{AB}} & \mathrm{Z}_{\mathrm{AC}} \\ \mathrm{Z}_{\mathrm{BA}} & \mathrm{Z}_{\mathrm{BB}} & \mathrm{Z}_{\mathrm{BC}} \\ \mathrm{Z}_{\mathrm{CA}} & \mathrm{Z}_{\mathrm{CB}} & \mathrm{Z}_{\mathrm{CC}} \end{bmatrix}^{-1} \begin{bmatrix} (\mathrm{Vsa} - \mathrm{Vra}) \\ (\mathrm{Vsb} - \mathrm{Vrb}) \\ (\mathrm{Vsc} - \mathrm{Vrc}) \end{bmatrix} \qquad \text{Equation 2.42}$$

$$\begin{bmatrix} Isa_{shunt} \\ Isb_{shunt} \\ Isc_{shunt} \end{bmatrix} = \begin{bmatrix} Y_{AA}/2 & Y_{AB}/2 & Y_{AC}/2 \\ Y_{BA}/2 & Y_{BB}/2 & Y_{BC}/2 \\ Y_{CA}/2 & Y_{CB}/2 & Y_{CC}/2 \end{bmatrix} \begin{bmatrix} Vsa \\ Vsb \\ Vsc \end{bmatrix} \qquad \text{Equation 2.43}$$

$$\begin{bmatrix} Isa \\ Isb \\ Isc \end{bmatrix} = \begin{bmatrix} Isa_{shunt} \\ Isb_{shunt} \\ Isc_{shunt} \end{bmatrix} + \begin{bmatrix} Isa_{series} \\ Isc_{series} \\ Isc_{series} \end{bmatrix} \qquad \text{Equation 2.44}$$

Combining Equation 2.42 through Equation 2.42 creates six simultaneous equations for computing the six currents into the network. Consider first that the inverse impedance matrix used in Equation 2.42 can be expressed as Y_{SERIES} and the admittance matrix in Equation 2.43 as Y_{SHUNT}. This network is illustrated in Figure 2.9. A single six-by-six admittance matrix now represents the entire network admittance as shown in Equation 2.45. Note that the sub-matrices $[Y_{SERIES} + Y_{SHUNT}]$ and $[Y_{SHUNT}]$ are themselves three-by-three matrices making the complete admittance a six-by-six matrix. Equation 2.45 also provides a means for computing the six terminal voltages if the six currents into the network are known. Simply multiply the current vector by inverse of the six-by-six admittance matrix.

$$\begin{bmatrix} Isa \\ Isb \\ Isc \\ Ira \\ Irb \\ Irc \end{bmatrix} = \begin{bmatrix} [Yseries + Yshunt] & [-Yshunt] \\ [-Yshunt] & [Yseries + Yshunt] \end{bmatrix} \begin{bmatrix} Vsa \\ Vsb \\ Vsc \\ Vra \\ Vrb \\ Vrc \end{bmatrix} \qquad \text{Equation 2.45}$$

Although they are not shown in this model, a more complete model would include the image conductors that modeled below the ground plane. Such a model includes effects such as ground resistivity on the transmission line zero impedance and frequency dependency. See Power System Analysis by Hadi Saadat**[REFERENCE]????** for additional information on the effects of ground resistance on line impedance models.

For transmission lines with overhead shield using segmented grounding or ungrounded shield wires, mutual coupling for these conductors is added to the line models as well. Since the mathematics for even the simplest of line models is complex, line models are usually developed using line constant-parameter computer programs. To further understand the physics that gives rise to these parameters, refer to a text on power system analysis such as those written by Stevenson, Saadat, or Elgred **[need reference????]**.

Balanced lines

A balanced line implies that, for the series impedance matrix and the shunt admittance matrix, all diagonal elements are equal and all off-diagonal elements are equal. For the series impedance matrix, the diagonal terms are assigned to the term *Zs* and the off-diagonal terms to *Zm*. Balanced lines lead to simplifications in computing power and detecting faults. However, they rarely ever exist except for the special case of cables (see 0 moved to "balanced lines").????

[Need to say something about shunt admittance here not sure what. Stans model ignores them. Another experiment --- assume receiving end is grounded and three phase voltage is applied to the sending end. Then [Z] = [V]*[I]-1. (hum… inverting a 1x3 matrix). The impedance seen by the source includes capacitance. Consider two cases: receiving end open and receiving end shorted to ground. First case … receiving end capacitance has an effect, second case, no, just the sending end capacitance. Here's the point – if the capacitance is not balanced then the current under light or no load is not balanced. If the series impedance is not balanced, then the current is not balanced for heavy loads or three phase faults. Has it ever been known that unbalanced lines balance currents for unbalanced faults?]
????

Unbalanced Lines

Unbalanced lines generate unbalance currents from balanced or unbalanced voltages and vice versa. There are no constraints on the self- and mutual-impedance and shunt capacitance, creating unsymmetrical matrices in Equation 2.42 and Equation 2.43. Unbalanced systems cannot be reduced to single-line equivalent systems without losing accuracy. Additional ramifications appear when applying symmetrical components to unbalanced impedance networks.

Multiphase Distributed Line Parameter Models

Multiphase distributed line modes extend the basic model presented in 0. However, they require a transformation to generate an orthogonal set of equations that allows the three-phase transmission line to be represented by three single-phase lines. The symmetrical components discussion in0 includes the mathematics for the base transformation. The multiphase distributed line parameter model is valid only if the matrix equations can be transformed to an orthogonal basis vector using a similarity transformation, to be discussed next. Once this is accomplished, the multiphase transmission lines can be represented as multiple independent single-phase lines. This results in no coupling between phases in the transformed mode.

Balanced Lines in Distributed Line Parameter Models

Use the Karenbauer transformation to generate multiphase distributed parameter line modes. This model, long used for analyzing high frequency signal propagation for power line carrier applications, is appropriate for studying power system transients because such signals can be generated by excitation of resonance of natural modes in the system. Balanced lines with single-value Zs and Zm produce single-value Z0 and Z1, generally called the zero and positive-sequence impedance. Matrix operations expressed by Equation 2.46 through Equation 2.50 describe transformations from

phase domain to modal domain for a general M-phase balanced transmission line. Equation 2.51 and Equation 2.52 provide a simplification to the matrix operations. Note that there is no negative-sequence impedance for balanced three-phase transmission lines. This is true of all balanced passive networks.

$$[T]=\begin{bmatrix} 1 & 1 & 1 & \dots & 1 \\ 1 & (1-M) & 1 & \dots & 1 \\ 1 & 1 & (1-M) & \dots & 1 \\ : & : & : & \dots & : \\ 1 & 1 & 1 & \dots & (1-M) \end{bmatrix} \qquad \text{Equation 2.46}$$

$$[T]^{-1} = \left(1/M\right)\begin{bmatrix} 1 & 1 & 1 & \dots & 1 \\ 1 & -1 & 0 & \dots & 0 \\ 1 & 0 & -1 & \dots & 0 \\ : & : & : & \dots & : \\ 1 & 0 & 0 & 0 & -1 \end{bmatrix} \qquad \text{Equation 2.47}$$

$$[Z_{phase}]=\begin{bmatrix} Zs & Zm & Zm & \dots & Zm \\ Zm & Zs & Zm & \dots & Zm \\ Zm & Zm & Zs & \dots & Zm \\ : & : & : & \dots & : \\ Zm & Zm & Zm & \dots & Zs \end{bmatrix} \qquad \text{Equation 2.48}$$

$$[Z_{modal}]=[T]^{-1}\ [Zp]\ [T] \qquad \text{Equation 2.49}$$

$$[Z_{modal}] = \begin{bmatrix} Z0 & 0 & 0 & \dots & 0 \\ 0 & Z1 & & \dots & 0 \\ 0 & 0 & Z1 & \dots & 0 \\ : & : & : & \dots & : \\ 0 & 0 & 0 & \dots & Z1 \end{bmatrix} \qquad \text{Equation 2.50}$$

$$\begin{aligned} Z0 &= Zs+(M-1)\cdot Zm = R0+j\omega L0 \\ &= (Rs\ \ j\omega Ls)+(M-1)(Rm+j\omega Lm) \end{aligned} \qquad \text{Equation 2.51}$$

$$Z1 = Zs - Zm = Rs + j\omega Ls - (Rm + j\omega Lm) \qquad \text{Equation 2.52}$$

Completing the calculations described above only produces part of a multiphase distributed line parameter model. Compute parameters R0, R1, L0, L1, C0, and C1 using Equation 2.51 and Equation 2.52. Then use Equation 2.27 through Equation 2.29 to compute Z0, Z1, $\tau 0$, and $\tau 1$ from these six parameters.

$$R0 = Rs+(M-1)\ \ Rm \qquad \text{Equation 2.53}$$

$$L0 = Ls + (M-1)\ Lm \qquad \text{Equation 2.54}$$

$$C0 = Cs - (M-1)\ Cm \qquad \text{Equation 2.55}$$

$$R1 = Rs - Rm \qquad \text{Equation 2.56}$$

$$L1 = Ls - Lm \qquad \text{Equation 2.57}$$

$$C1 = Cs + Cm \qquad \text{Equation 2.58}$$

There are M-indented equations for computing the voltage and current relationships for an M-phase line. One phase uses Z0 and τ0, while all the rest use Z1 and τ1. The example illustrates how to use the modal domain to compute phase domain voltages and currents.

Unbalanced Lines in Distributed Line Parameter Models

Distributed parameter models of unbalanced lines are possible but the Karenbauer transformation cannot be used. Unique simultaneity transformations generate the M-linear independent equations representing the M-phases in the modal domain.

Frequency-Dependent Line Models

????

Cables

?????

Domain Transformations

The subject working in companion domains has already been introduced, as the Karenbauer transformation that is needed for modeling distributed line parameter models using the modal domain. As mentioned before, this is one of many transformations into a domain that results in an impedance matrix that has all zero off-diagonal elements. The value of such transformations is that independent equations can be used to solve for voltages and currents that have coupled three-phase impedance relationships. The disadvantage is that one must be able to interpret the results obtained in the uncoupled domain or easily convert back to the phase domain.

Symmetrical Components [6066], [Bosela Ch. 10, Pg. 332-370]????

Fortescue first introduced symmetrical components in 1918. He demonstrated that an M-phase unbalance system can be represented as M-1 M-phase systems of differing orders of sequences and one zero phase sequence. A thorough treatment on the subject of symmetrical components is provided in a text written by Dr. Paul Anderson.[9] Further treatment of this subject is provided in Appendix 11.11 and in the tutorial written by Stan Zocholl.[10]

Although not strictly limited to three-phase networks, symmetrical components are frequently used to analyze conventional three-phase power systems. To illustrate, consider a three-phase unbalanced system denoted as phases A, B, and C. We introduce a phase-shifting operator, "a" such that a phasor $aV\angle\theta° = V\angle(\theta+\phi)°$ and for this example, ϕ equal 120°. Raising α to a power is equivalent to multiplying 120° by that number.

Equation 2.60 provides the transformation from the phase domain to the symmetrical component domain. The matrix shown in Equation 2.60 is called the Fortescue transformation matrix. It is convention to refer to phase A zero-sequence voltage as V_A0, phase A positive-sequence voltage as V_A1, and phase A negative-sequence impedance as V_A2. The reference to phase A defines the rotational sequence for phase B and C such that the positive-sequence phasors align all three phases, A, B, and C, with phase A. It is sometimes convenient to assume phase A is the reference phase and therefore drop the reference to phase A notation. In such cases, the positive-, negative-, and zero-sequence voltages are the denoted by *V1, V2*, and *V3* respectively. Equation 2.60 through Equation 2.62 express the same information as Equation 2.59 but as three independent equations. Use similar expressions for current.

$$\begin{bmatrix} V_A0 \\ V_A1 \\ V_A2 \end{bmatrix} = \left(\frac{1}{3}\right)\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}\cdot\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \quad or \quad [V_{012}]=[A]\cdot[V_{ABC}] \qquad \text{Equation 2.59}$$

$$V_A0 = (V_A\angle\theta_A + V_B\angle\theta_B + V_C\angle\theta_C)/3 \qquad \text{Equation 2.60}$$

$$V_A1 = (V_A\angle\theta_A\cdot\alpha^0 + V_B\angle\theta_B\cdot\alpha^1 + V_C\angle\theta_C\cdot\alpha^2)/3 \qquad \text{Equation 2.61}$$

$$V_A2 = (V_A\angle\theta_A\cdot\alpha^0 + V_B\angle\theta_B\cdot\alpha^2 + V_C\angle\theta_C\cdot\alpha^1)/3 \qquad \text{Equation 2.62}$$

Equation 2.63 or Equation 2.64 through Equation 2.66 provide the transformation from the symmetrical component domain back to the phase domain. As before, use similar expressions for current.

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix}\cdot\begin{bmatrix} V_A0 \\ V_A1 \\ V_A2 \end{bmatrix} \; or \; [V_{ABC}]=[A]^{-1}\cdot[V_{012}] \qquad \text{Equation 2.63}$$

$$Va\angle\theta_A = V_A0 + V_A1 + V_A2 \qquad \text{Equation 2.64}$$

$$Vb\angle\theta_B = V_A0\cdot\alpha^0 + V_A1\cdot\alpha^2 + V_A2\cdot\alpha^1 \qquad \text{Equation 2.65}$$

$$Vc\angle\theta_C = V_A0\cdot\alpha^0 + V_A1\cdot\alpha^1 + V_A2\cdot\alpha^2 \qquad \text{Equation 2.66}$$

The line model developed in paragraph 0, and the impedance transformations shown in Equation 2.46 through Equation 2.58 are adequate for transforming impedance of balanced networks from the phase domain to the symmetrical component domain. The significance of working in the symmetrical component domain is that zero-

sequence currents only generate zero-sequence voltages if the zero-sequence impedance is not zero. The same can be said for positive- and negative-sequence currents, voltages, and impedances. Equation 2.67 expresses this relationship mathematically. Since the impedances are uncoupled, we can write Equation 2.67 as three individual equations, as shown in Equation 2.68 through Equation 2.70.

$$\begin{bmatrix} V_A 0 \\ V_A 1 \\ V_A 2 \end{bmatrix} = \begin{bmatrix} Z0 & 0 & 0 \\ 0 & Z1 & 0 \\ 0 & 0 & Z2 \end{bmatrix} \cdot \begin{bmatrix} I_A 0 \\ I_A 1 \\ I_A 2 \end{bmatrix} \quad or \quad [V_{012}] = [Z_{012}] \cdot [I_{012}] \qquad \text{Equation 2.67}$$

$$V0 = Z0 \cdot I0 \qquad \text{Equation 2.68}$$

$$V1 = Z1 \cdot I1 \qquad \text{Equation 2.69}$$

$$V2 = Z2 \cdot I2 \qquad \text{Equation 2.70}$$

An impedance transformation from the phase domain to the sequence domain follows from extensions of Equation 2.59, Equation 2.63, and Equation 2.67. In symmetrical component domain and phase domain, express Ohm's law as in Equation 2.67 and Equation 2.71, respectively. Substituting Equation 2.71 into Equation 2.59 yields Equation 2.72. The transformation of currents from the phase domain to the symmetrical component domain follows from Equation 2.63, as shown in Equation 2.73. Making the substitution for IABC from Equation 2.73 into Equation 2.72 expresses voltages and currents in the symmetrical component domain as a function of impedance in the phase domain shown in Equation 2.74. Compare Equation 2.67 and Equation 2.74 to deduce the relationship of symmetrical component impedance to phase domain impedance that is shown in Equation 2.75.

$$[V_{ABC}] = [Z_{ABC}] \cdot [I_{ABC}] \qquad \text{Equation 2.71}$$

$$[V_{012}] = [A] \cdot [Z_{ABC}] \cdot [I_{ABC}] \qquad \text{Equation 2.72}$$

$$[I_{ABC}] = [A]^{-1} \cdot [I_{012}] \qquad \text{Equation 2.73}$$

$$[V_{012}] = [A] \cdot [Z_{ABC}] \cdot [A]^{-1} \cdot [I_{012}] \qquad \text{Equation 2.74}$$

$$[Z_{012}] = [A] \cdot [Z_{ABC}] \cdot [A]^{-1} \qquad \text{Equation 2.75}$$

If phase domain impedance, ZABC, is generated for a balanced network, then the results from Equation 2.75 are identical to the results from Equation 2.51 and Equation 2.52 with the negative-sequence impedance set equal to the positive-sequence impedance. For balanced networks, all mutual- and all self-impedances are equal.

Figure 2.10 and Figure 2.11 have been extracted from ***Appendix 11.10: Tutorial on Symetrical Components*** to show how symmetrical component circuits are graphically represented. Figure 2.11 is a typical single-line diagram of a balanced three-phase electrical network. It shows a phase-A-to-ground fault applied to Bus 2, which represents a physical bus in the network or an artificial bus in the middle of a

transmission line. Bus 1 is where the generator connects to transmission line L1. The generator shown here represents a wye-connected source with the neutral point connected to ground through resistance R0. A delta-connected or ungrounded wye-connected motor load is connected to Bus 3. The object of this analysis is to determine the post-fault current at any point in the circuit.

Figure 2.10, the electrical network equivalent of Figure 2.11, uses symmetrical components and contains valuable information. Three independent networks connect at the point of fault. Figure 2.10 shows the total fault current at Bus 2 equal to Ia1, which is also equal to Ia2 and Ia0. Additional symmetrical component configurations are provided in ***Appendix 11.12: Transformer Connection Symmetrical Component Networks***.

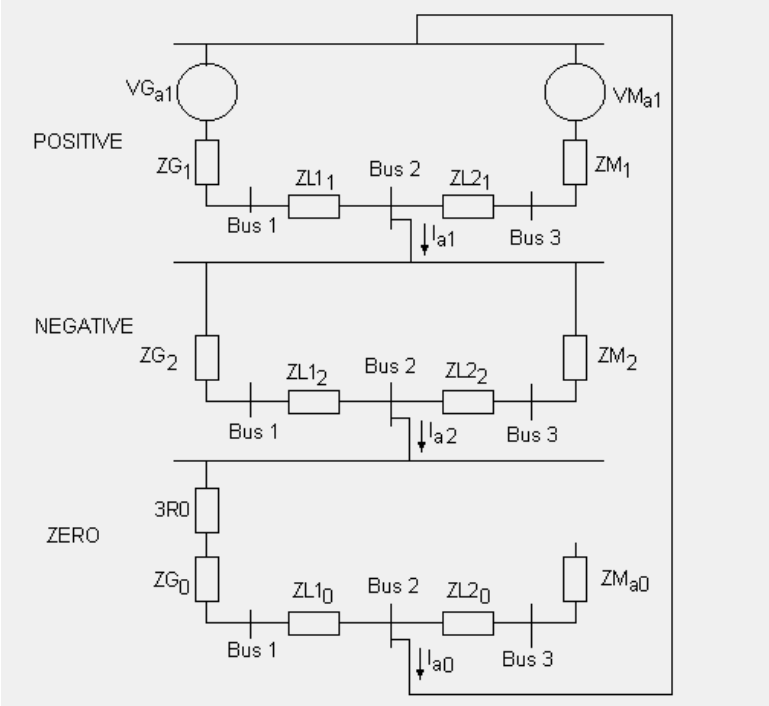


Figure 2.10: Sequence Network Connection for Bus 2 A-to-Ground Fault

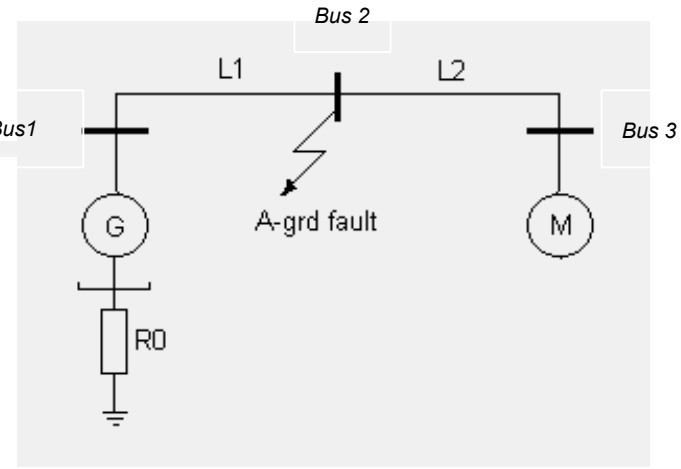


Figure 2.11: A-Phase Fault Location

Both generator and motor can provide positive-sequence voltage as shown in the positive-sequence network. ZG1 and ZM1 are the positive-sequence impedances for these devices and ZL1 and ZL2 are the transmission line positive-sequence impedances. A Thevinen equivalent voltage source and source impedance, as determined by Equation 2.76 and Equation 2.77, can replace the positive-sequence.

$$V_A 1_{TH} = VG_A 1 - \left(VG_A 1 - VM_A 1\right) \cdot \left(\frac{ZL2_1 + ZM_1}{ZG_1 + ZL1_1 + ZL2_1 + ZM_1} \right) \qquad \text{Equation 2.76}$$

$$Z1_{TH} = \left(\frac{\left(ZG_1 + ZL1_1\right) \cdot \left(ZM_1 + ZL2_1\right)}{\left(ZG_1 + ZL1_1 + ZM_1 + ZL2_1\right)} \right) \qquad \text{Equation 2.77}$$

Equation 2.78 and Equation 2.79 show reductions of the negative-and zero-sequence networks, which have no sources. Because the motor in this example operates in an ungrounded configuration, it has no impedance path to ground, so the zero-sequence impedance for the motor branch is infinite. Generator ground resistance is included in the generator branch as three times R0 because this resistance is in the ground path for all three phases.

$$Z2_{EQU} = \left(\frac{\left(ZG_2 + ZL1_2\right) \cdot \left(ZM_2 + ZL2_2\right)}{\left(ZG_2 + ZL1_2 + ZM_2 + ZL2_2\right)} \right) \qquad \text{Equation 2.78}$$

$$Z0_{EQU} = \left(3R0 + ZG_0 + ZL1_0\right) \qquad \text{Equation 2.79}$$

$$I_A 1 = I_A 2 = I_A = \left(V_A 1_{TH} \Big/ \left(Z1_{TH} + Z2_{EQU} + Z0_{EQU}\right) \right) \qquad \text{Equation 2.80}$$

Finally, use Equation 2.80 to determine the sequence currents flowing into the fault. Once you find these sets of current, compute the sequence voltages and current contributions from each source. Further, you can use Equation 2.66 through Equation 2.68 to transform these sequence values back into phase domain.

The following SEL technical papers provide additional examples: [List of SEL Pubs].????

Parks Equations

????

Faulted Systems—[Bosela Ch. 11, Pg. 371-404]????

The tools and approach for analyzing power systems depend on the purpose of the study and the state of the power system. Mathematical analyses of power systems have different perspectives depending on how rapidly the systems are expected to change. The three most common power system models in use today are steady-state, dynamic, and transient models.

Steady-State models

Steady-state solutions are appropriate for determining power transfer, nominal operating conditions, and initial and final conditions. The values for resistance, inductance, capacitance, and operating frequency that define the network do not change with time and the amplitude and phase of RMS voltages and currents are computed from complex impedances. Depending on the complexity of the network, complete the analysis using either hand calculations or computer-engineering programs to perform the phasor mathematics. Computer programs include spreadsheets, MathCAD, MATLAB, and power system analysis programs like Easy Flow.

Dynamic Models

Dynamic modeling assumes that the power system dynamics under consideration change at a rate significantly less than the power system frequency. Analyze these systems using Laplace transforms or differential equations. Like steady-state solutions, complex voltages, currents, and impedances make solutions independent of frequencies at and above the nominal power system frequency. Since the network changes with time, there are multiple solutions representing a series of steady-state conditions. MATLAB, MathCAD, and EMTP, addressed next, are suitable tools. Analog computer networks, called transient network analyzers, were once widely used, but have given way to computer-based solutions, which are both less expensive and more accurate.

Transient Models

Transient models result in time domain solutions. Voltages and currents produced by the mathematics are in effect samples of these signals. Networks are described using either discrete differential or difference equations that approximate linear differential equations to model inductors, capacitors, and electromechanical dynamics.

As with dynamic modeling, each new output is the result of solving the network equations of a system that is assumed to be momentarily in a steady-state condition. Each new solution becomes the initial condition for the next solution. The period

representing the time between solutions limits the upper bounds of the frequency range included for a particular simulation. The same constraints that govern the validity of processes using digital filtering and sampled data systems, as discussed in paragraph 0, apply here.

When the program is first started, the initial conditions are computed using one of two methods. The first method is to generate a steady-state model as described in paragraph 0. Use Equation 2.9 to transfer the amplitude and phase results of this solution to the transient solution. This is not trivial because many of the difference equations need a history of many previous solutions to start off with a then correct next solution. With the advent of faster computers, this method has been replaced by simply letting the simulation start with zero initial conditions and running it long enough for initial transients to die out before initiating changes to the network.

Much research and engineering effort has been focused on improving computer transient simulations. Computer programs that are designed specifically to simulate transient responses for multiphase electrical networks are called Electromagnetic Transient Programs (EMTP). Some recent commercial products have developed real-time transient programs for testing instrumentation, monitoring, and control devices such as protective relays.

DIGITAL SYSTEMS

Digital systems include discrete signal theory and digital logic theory. Both use binary numbers to turn switches on and off. Computer control is often thought of in terms of Boolean operators such as AND, OR, and EXCLUSIVE OR. Computer control can also refer to algorithms that computers use to compute responses that, for relays, result in on-off controls as well as in reports that include numbers over a wide range of values. Discrete signal theory includes digital signal processing that uses computer algorithms to approximate analog filtering.

Signal Processing – Filtering Overview

Electromechanical relays are a type of analog filter. In the age of microprocessor-based relays, analog filters are still used for preprocessing, and in most cases, to mitigate high frequency noise caused by electrical transients, radio frequency interference (RFI), or electromagnetic interference (EMI). To understand this better, consider the following example. It is common practice to protect the CMOS ADC from overvoltage damage by connecting a surge protector from the input lead to chassis ground. Assume that a noise signal is coupled onto the circuit from an alien source and causes excessive voltage spikes. The transient-suppressing device clips (limits) the voltage magnitude and effectively protects the sensitive electronic circuits. However, clipping the signal magnitude corrupts the signal to be measured. Even if clipping does not actually alter the input signal, a new signal is now present. This new signal is the superposition sum of the original information signal and the noise.

For a filter to be effective, the noise must be in a different frequency band from that of the original signal in order to separate the good from the bad. If the noise is broadband, meaning that its energy is spread over a wide range of frequencies,

filtering can help reduce the amount of corruption that the signal experiences. This is why most protective relays use analog filters.

Many microprocessor relays only respond to voltages and currents at 60 Hz. When the power system is in a state of change caused by normal switching operations or from faults, it generates other frequencies. The relay must first extract the 60 Hz information. The following brief example illustrates the need for filtering in relaying. Figure 2.12 shows a simple block diagram of the voltage and current analog input signal conditioning. The signal conversion provides scaling and possibly conversion to a voltage level appropriate for electronic devices.

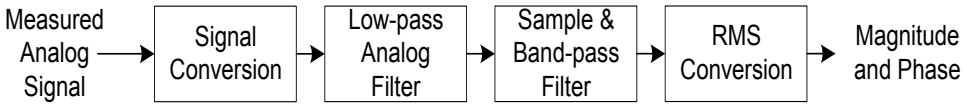


Figure 2.12: Block Diagram of Relay Signal Conditioning and Conversion

Next, an analog low-pass filter removes all high frequency components. Figure 2.13 shows the simulated result for the voltage of one phase of a power system that is energized and faulted. The analog filter removes some of the high frequency signals, but not all, depending on the filter design characteristics. For this example, the filter is second-order low-pass with a 3db cutoff set for 450 Hz. This plot also shows that there is a small but significant delay in the filtered signal. This delay shows up as phase shift for steady-state signals. Since all inputs pass through the same filter, the phase between signals remains constant. Keeping the cutoff frequency well above 60 Hz minimizes variations in delay caused by the component value deviations used to implement the analog low-pass filter.

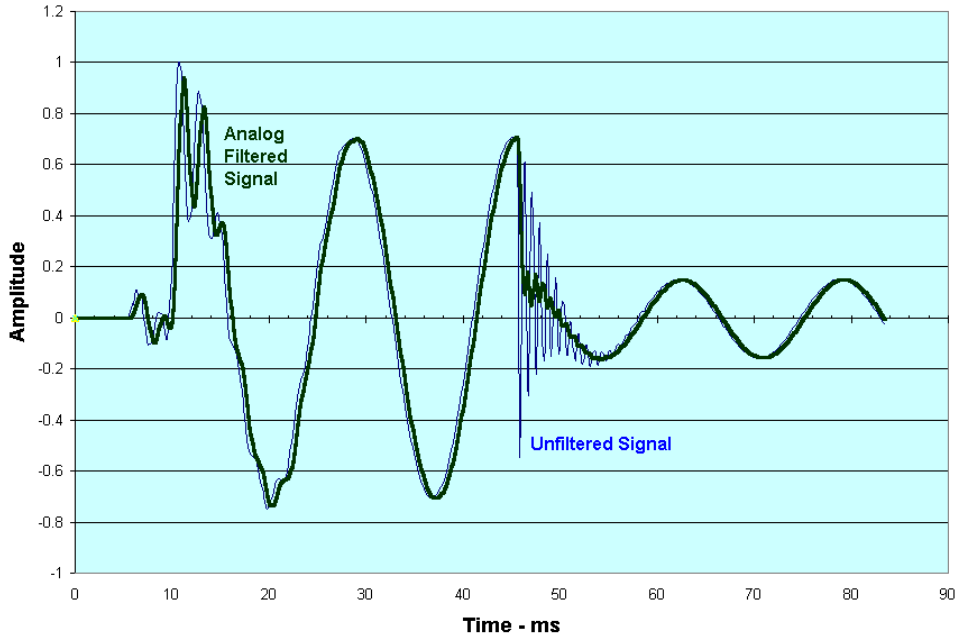


Figure 2.13: Simulated Power System Transient

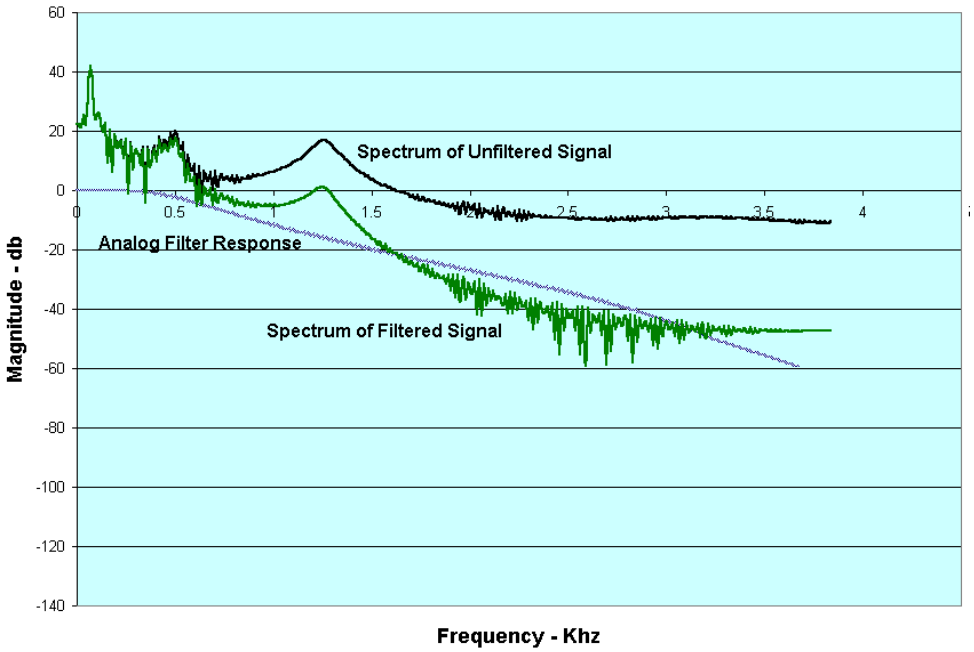


Figure 2.14: Frequency Spectrum of a Power System Transient Signal Before and After Analog Filtering

Figure 2.14 shows the frequency spectrum of the same two signals along with the analog filter response. The frequency response of the filtered signal is the simply the algebraic sum of the low-pass filter response and the input signal frequency spectrum at all corresponding frequencies. The low-pass filter characteristics have unity response until approximately 400 Hz and taper off to –3db at the 540 Hz cutoff frequency.

A digital filter now samples and processes the filter signal. For this example, the digital filter is a 16^{th} order cosine filter. Figure 2.15 shows the frequency response of a 16^{th} order digital filter. Characteristic of digital filters, the response repeats its shape every integer multiple of the sampling frequency. This figure also shows the mirror image around the Nyquist rate that is one-half the sampling frequency. Both of these characteristics give rise to the phenomena known as aliasing. For the filter response shown in Figure 2.15 (960 Hz-sampling rate) a signal at 900 Hz is aliased to appear like a 60 Hz signal.

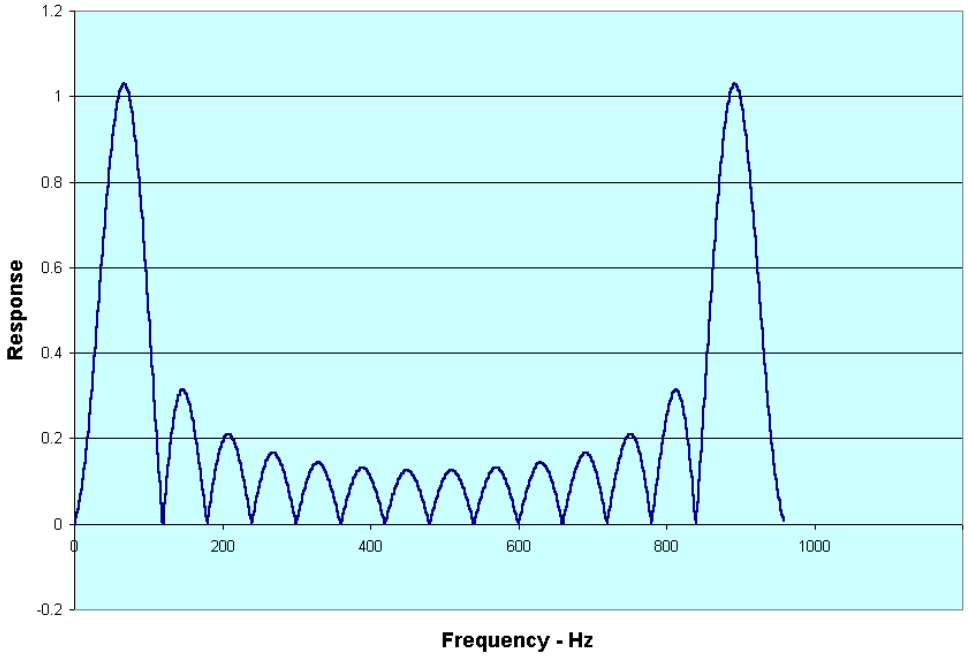


Figure 2.15: Frequency Response of a 16-Order Cosine Filter

The output of this process shows the effects of sampling as well as of analog and digital filters. The delay resulting from the digital filter is more apparent in Figure 2.16. The processing delay is identical for all sampled inputs, resulting in no phase errors. However, the processing delay will also delay trip decisions made from processing this signal. This delay is a necessary overhead. The frequency spectrum of the sampled and filtered signal shown in Figure 2.17 reveals additional signal peaks that are not present in the original signal. This result of sampling produces the step changes in Figure 2.16.

Figure 2.18 completes the process outlined in Figure 2.12. For convenience, the RMS magnitude is scaled for peak response by omitting the multiplication by $\sqrt{1/2}$. Now that you have seen the application of filtering in relaying, the next few sections discuss the final issues of digital signal processing.

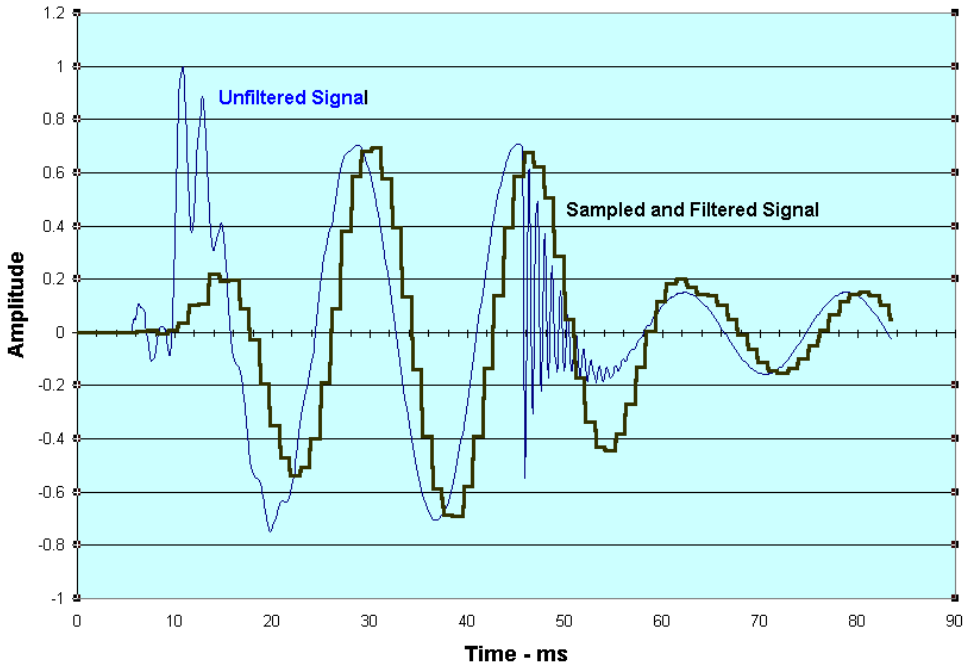


Figure 2.16: Result of Sampling and Filtering of a Power System Transient Signal

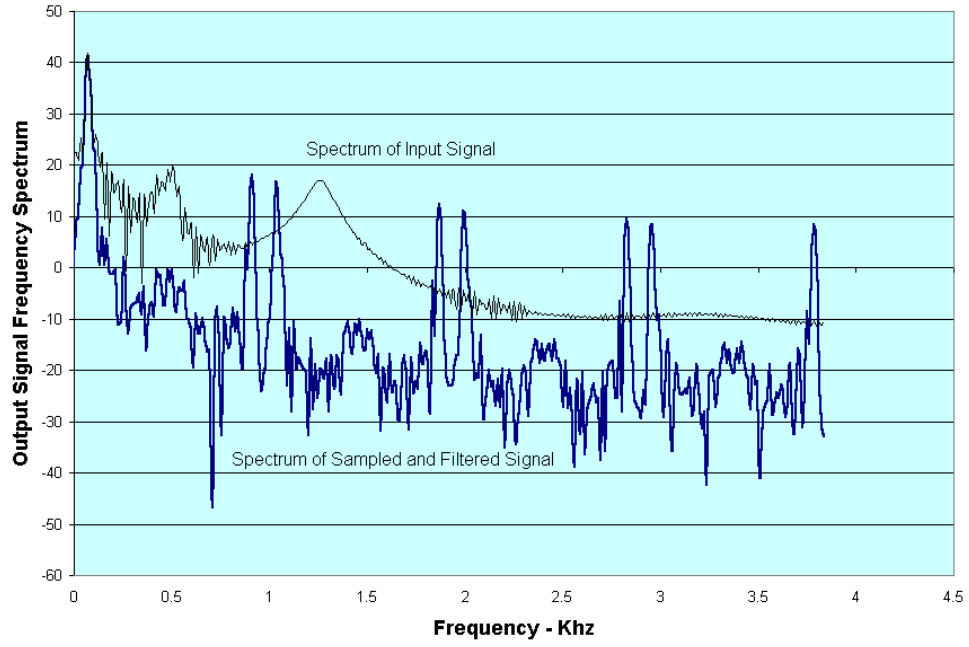


Figure 2.17: Frequency Spectrum of Filtered and Sampled Transient Signal

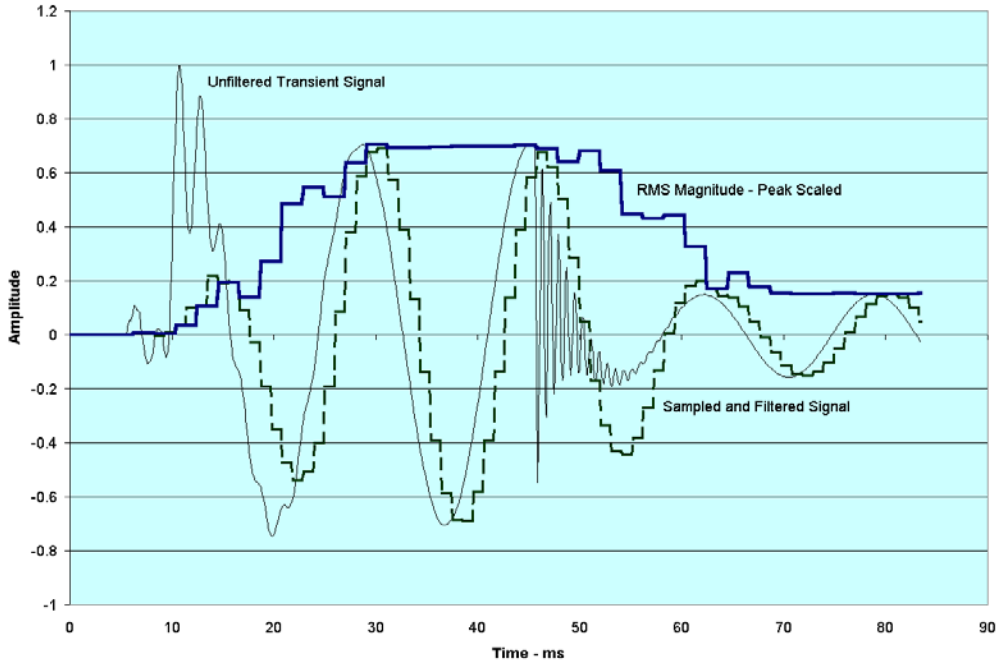


Figure 2.18: Response of the RMS Detector to a Transient Signal

Discrete Domain

Discrete signals have values for amplitude, time, and phase that change in discrete units. Consider the effect of using a digital-to-analog converter to sample the continuous signal shown in Figure 2.19. The vertical lines extending from the horizontal zero axes with large dots at the end represent the samples. The samples become a sequence of numbers spaced over time.

The dotted lines in Figure 2.19 illustrate that, although the analog signal continues to change with time, the sampled signal remains constant until the next sample is taken. This, in effect, converts the analog signal to a rectangular approximation of the original signal. The sample variables, X0 through X7, note the sequence in which the samples are taken with X7 being the oldest.

There are two delays associated with sampling. The first is because the rectangular approximation always follows the sample. This is in contrast to a true approximation where the sample falls in the center of the rectangular approximation. The second delay is associated with the pipeline delay that does not show the full effect of step change in phase, frequency, or amplitude until all the samples needed for processing are accumulated. Both of these delays create a transient behavior that is strictly a function of the digitizing and not of the input signal.

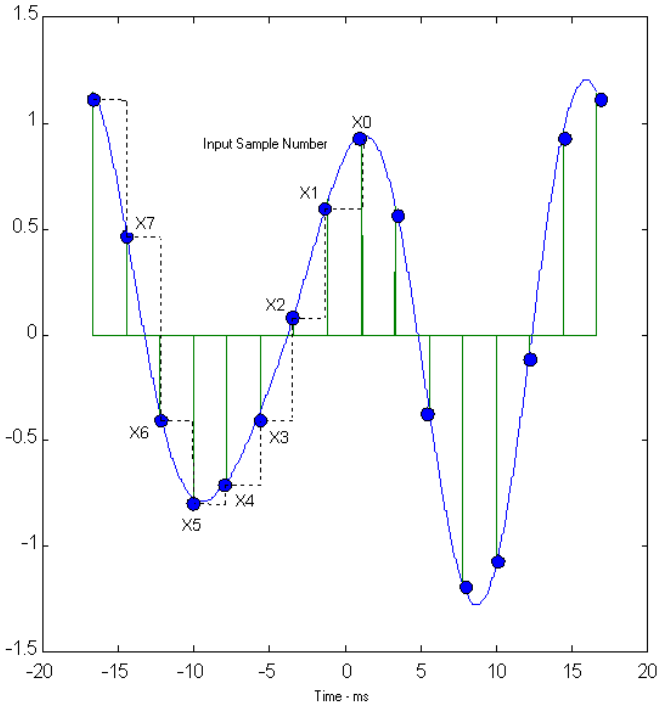


Figure 2.19: Sampled Signal

Filtering

Filtering is the process of selecting some specified information that is mixed with a whole collection of data. In power engineering, that selection is often based on frequency.[11] There are of course many other criteria for discriminating information, analog vs. digital, phase, amplitude, and so on. For power system protection, we usually consider only the 60 Hz information, although many other signals may be present on a power line. However, the 60 Hz signal could be filtered out, too, if the only signal of interest was the third harmonic of 60 Hz. Consider any signals other than those of interest to be noise.

Filter classifications are low-pass, band-pass, high-pass, and band-reject, depending on how a specified frequency range is to be treated or processed. Filter electronic signals by either using analog circuits or running digital filtering programs in a computer. Analog filtering circuits use electronic components such as operational amplifiers, resistors, capacitors, and inductors. Digital filters require that the electric signal be sampled and converted to a binary representation using a device generically called an analog-to-digital converter or ADC. Once processed, the string of digital samples can be converted back to analog using a digital-to-analog converter (DAC). Within specified constraints, the processes are approximately equal. Most modern protective relays use a combination of both analog and digital filters for processing power line signals.

Digital Filtering

Digital filters process a sequence of samples of the input signal using algorithms commonly called digital signal processing (DSP). There are two types of digital filters, recursive (also called IIR or infinite response) and nonrecursive (also called FIR or finite response) filters. IIR filters use past outputs as well as present and past inputs to compute the present output as expressed by Equation 2.82. FIR filters execute the algorithm expressed by Equation 2.81 where the output from the filter, yk, is only dependent upon present and past input samples, xi. The process of determining the values of the coefficients that weight the inputs and outputs is beyond the scope of this treatment of digital filters, but is discussed in references. [12, 13]

$$y_n = \sum_{i=0}^{N-1} x_i \cdot b_i \qquad \text{Equation 2.81}$$

$$y_n = \sum_{i=0}^{N-1} x_i \cdot b_i - \sum_{j=1}^{M-1} y_{(k-j)} \cdot a_j \qquad \text{Equation 2.82}$$

Use either IIR or FIR filters, depending on which filter characteristics of the response you need. One artifact of FIR filters is that the phase response is linear with changes in frequency. This characteristic is of particular interest to engineers dealing with signals that represent voltages and currents on a power system. FIR filters that evolve from discrete Fourier transforms are particularly useful for extracting out RMS magnitude and phase information from a signal that nominally contains a single frequency. Equation 2.83, where k represents the discrete frequency index and n is a variable of summation, expresses this filter. X(k) is a complex variable containing real and imaginary parts. Use common trigonometric functions to see this more easily, using the substitution shown in Equation 2.84 as shown in Equation 2.85.

$$X(k) = \sum_{n=0}^{N-1} x(n)\ e^{(-j2\pi k n / N)},\ 0 <= k <= N-1. \qquad \text{Equation 2.83}$$

$$e^{-j\theta} = \cos(\theta) - j\sin(\theta) \qquad \text{Equation 2.84}$$

$$X(k) = x(n) \cdot \left[\cos(2\pi k n / N) + j\sin(2\pi k n / N)\right] \qquad \text{Equation 2.85}$$

If the digital filter is applied to synchronously sample the system nominal single frequency such that the sampling rate in N times the system frequency, then the fundamental complex vector is computed when k = 1.[14,15] This results in two FIR filters each with N coefficients, each in the form expressed in (1) above. One of the FIR filters computes the real part of X and the other the imaginary part.

Such a filter, using the form of Equation 2.83 for N = 8, would have coefficients described by Equation 2.86 and Equation 2.87. Use Equation 2.88 and Equation 2.89 to transform the results from Equation 2.86 and Equation 2.87 into phasor variables. Subscript n on *Xnm* and *Xnp* means that a new phase and magnitude is available by executing Equation 2.86 through Equation 2.89 after each new sample. If the input is

a steady-state sine wave, then the magnitude would be constant and the phase would be continually rotating in a positive direction in 45° steps.

$$X_n(re) = \sum_{k=0}^{7} x_{(n-k)} \cos(k \cdot 45°) \qquad \text{Equation 2.86}$$

$$X_n(im) = \sum_{k=0}^{7} x_{(n-k)} \sin(k \cdot 45°) \qquad \text{Equation 2.87}$$

$$X_n m = \sqrt{X(re)^2 + X(im)^2} \qquad \text{Equation 2.88}$$

$$X_n p = \arctan\left(X_n(im) \Big/ X_n(re) \right) \qquad \text{Equation 2.89}$$

View the actual process of filtering as a sequence of instantaneous measurements moving through a series of boxes (or registers in a computer). Figure 2.20 shows the newest measurement put in one end and the oldest discarded when it is removed from the last register. Intermediate samples shift to the registers that are adjacent in memory. Second sets of registers contain the coefficients of the filter. Figure 2.21 shows these coefficients multiplied by the corresponding time data samples and summed together, producing output Y_n

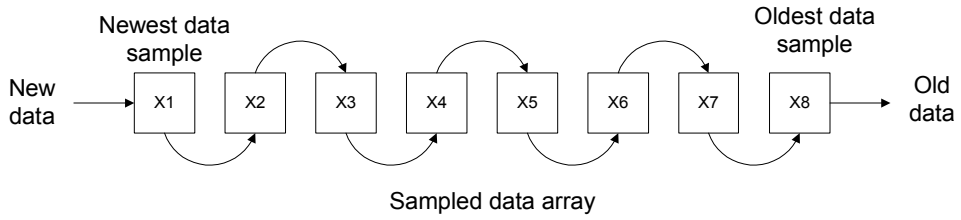


Figure 2.20: Sampled Data Flow Through Computer Registers

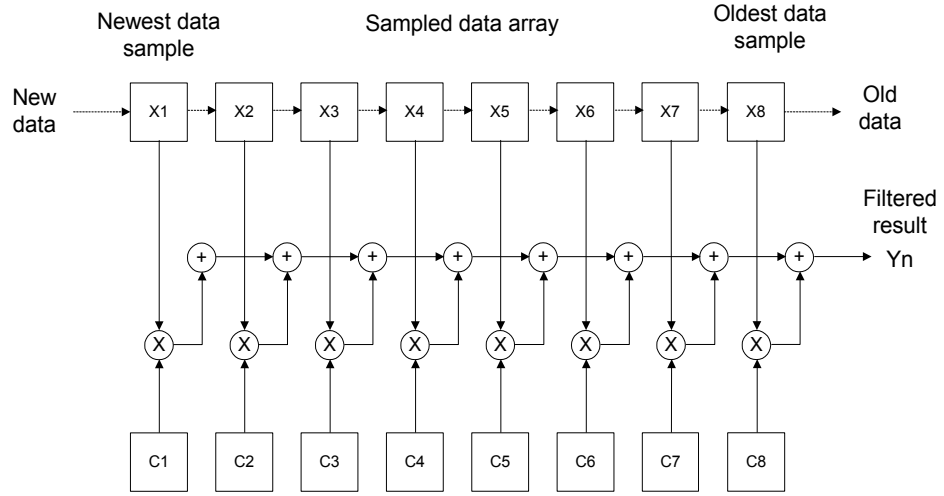


Figure 2.21: Graphical Diagram of the Filtering Process Described by Equation 2.83

Sampling

????

Performance Measurements

Since filters discriminate based on frequency, performance measures indicate how well signals in the desired frequency range are passed and those outside this band are rejected. Ideally, filters have characteristics with zero attenuation in the pass-band and zero response outside the pass-band. Because ideal filters are not possible, designers need to compensate for the limitations of nonideal filters and be realistic about performance and cost.

Bandwidth

DFT filters have two more characteristics important to their applications to power system relaying: a response bandwidth and a transient response. The bandwidth of a filter is a two-edged sword. This filtering reduces the undesirable frequencies that can distort the phase and magnitude results. However, the ability to respond to a sudden change in amplitude is restricted even though the frequency of the signal remains unchanged.

The fundamental truths illustrated in Figure 2.22 are listed below:

- The magnitude of the signal will weaken if the frequency of the signal is not in the center of the pass-band. Figure 2.22 shows the responses for a 16-point DFT filter designed for 60 Hz operation. The magnitude of a 50 Hz signal would only be 80 percent of true magnitude. The filtered magnitude of a 50 Hz signal passed through an 8-point DFT 60 Hz filter would be approximately 95 percent of actual value.
- Selectivity is a good feature only if it does not distort the results over the frequency range of expected operation.
- The 4-, 8-, and 16-point DFT filters all have zeros at harmonics.

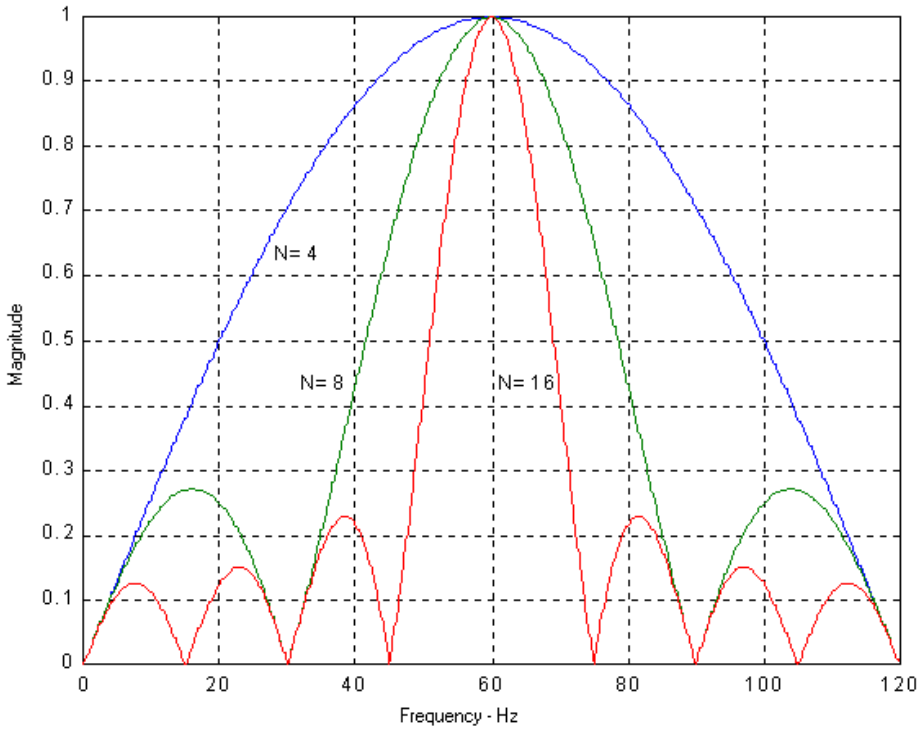


Figure 2.22: Filter Response for a 4-point, 8-Point and 16-Point DFT Filter

Phase Distortion, Digital Filter Signal Delay, and Transient Response

These three issues seem very different but actually have the same root cause in digital filtering. The problem begins when the input signal changes from one steady-state condition to another, regardless of whether that change is amplitude, frequency, phase, or a combination of the three. The new samples representing the new steady-state condition must propagate through the digital filters pipeline as illustrated in Figure 2.20 and Figure 2.21. Only after all input array values are replaced does the filter output accurately represent the response to the new steady-state condition.

All analog and digital filters inevitably introduce phase; it is the price of processing. Even so-called zero-phase filters actually have phase shifts on integer multiples of 360 degrees. Only FIR filters can have linear phase where the phase shift is determined by a constant times the frequency of the signal, as demonstrated in Figure 2.23. Since phase is important in power measurements, it is important to use filters that have linear phase or those that are approximately linear over a limited range of frequencies. Implement phase shifts using pure delays.

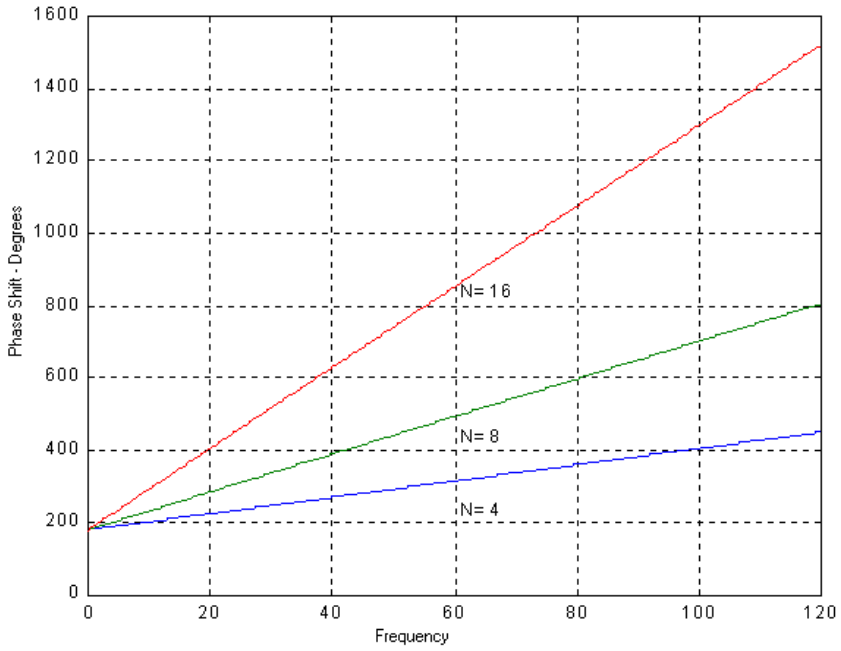


Figure 2.23: Phase Response for a DFT filter

The issue of delay considers the digital filter output as accurately representing a steady-state condition. Filter delays inherently create transient responses. FIR filters have a transient response limited to the amount of time needed to propagate updated values to every element in the filter algorithm. IIR filters, on the other hand, have memory of past outputs. Therefore the magnitude of the disturbance and the frequency response of the filter itself determine the duration of the transient.

Consider the example shown in Figure 2.24. The input to the filter starts out at some arbitrary value, as would be the case if a continuous sine wave were suddenly applied to a digital filter. The filter output remains at zero for a number of samples before beginning to respond to the input. The filter does not reach steady-state output until a significant number of additional samples are processed.

Figure 2.24 shows that the input undergoes a step change in amplitude at about sample 1500. Note that the filtered output is delayed and no longer has sharp transitions. This is caused by the low-pass filter characteristic that removes the higher frequencies associated with fast transitions.

Filtering for Protective Relays by Schweitzer and Hou provides additional details on filtering for power systems.[14]

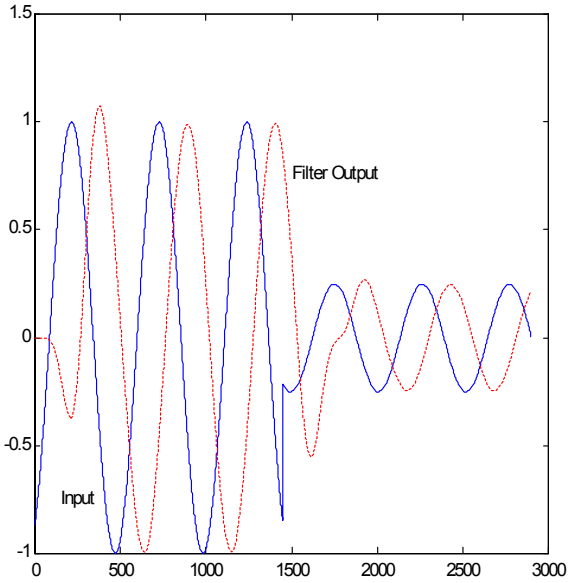


Figure 2.24: Example of Delaying and Transient Effects of Digital Filtering

Aliasing

Aliasing is an artifact of sampling alone and is only a problem for digital filters because they process data obtained from sampling signals that are continuous in time. An alias is an alternate identity. Signals that are higher than half the sampling rate will show up as phantom or pseudosignals with frequencies below half the sampling rate. The result of aliasing is that signals that are sampled above the Nyquist rate (equal to half the sampling rate) are indistinguishable from signals, real or imaginary, that are below the Nyquist rate.

We can look at aliasing from either the time or the frequency domains. From the time domain, consider the signal shown as a solid line labeled X1 in Figure 2.25. This signal is then sampled as noted by the large dots labeled S1 through S4. These sample values are identical as samples from the signal shown as the dashed line and labeled X2 in Figure 2.25. Hence the results after sampling are indistinguishable and X1 is aliased to appear as X2 or vice versa.

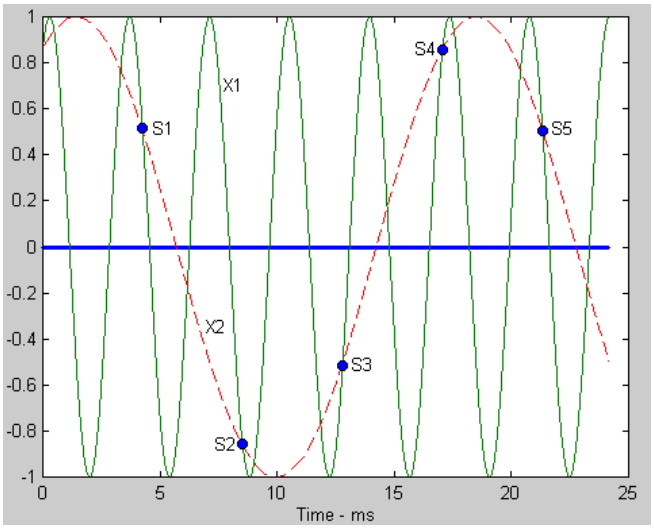


Figure 2.25: Example of Aliasing Caused by Sampling

Figure 2.26 shows a more dramatic illustration in the frequency domain. Adding signals X1 and X2 together generates a new composite signal. This signal is then sampled as shown in Figure 2.26. Sampling the pseudosignal is indistinguishable from sampling the composite signal. The pseudosignal used in this example is in phase and at the same frequency as one of the original components, X2, but this is necessarily the case. As long as a signal is below the Nyquist rate, sampling accurately represents the signal and, mathematically, it is possible to recover the phase and amplitude of the original signal. However, the process of sampling will misrepresent signals that, completely or in part (as the case for multiple frequency signals), have frequencies above the Nyquist rate. This distortion is called aliasing because high frequency signals disguise themselves as lower frequency signals when sampled.

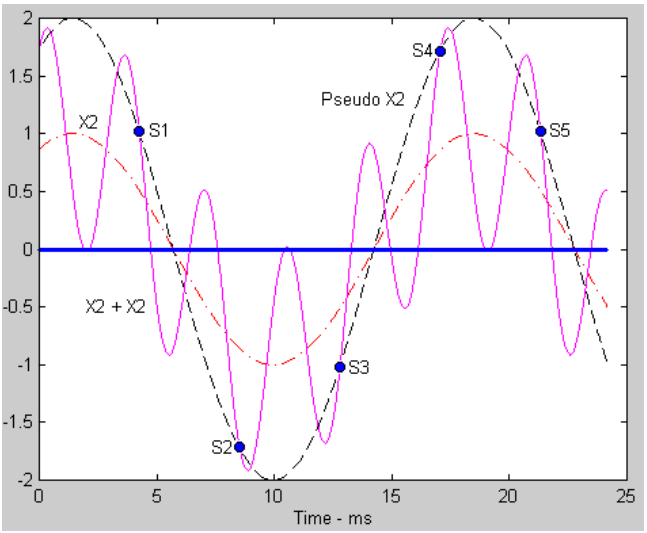


Figure 2.26: Effects of Aliasing on Signals Multiple Frequency Signal

The Cosine Filter

It is in the best interest of the power industry to reduce the response of the DFT to the offset initiated by a fault. The industry frequently uses a cosine filter, the coefficients of the real part of the DFT shown in Equation 2.83 that are generated by the cosine function in Equation 2.85. Figure 2.15 shows the frequency response of a 16th order cosine filter. Figure 2.27 shows the response of a cosine filter compared to the DFT filter. The cosine filter favors higher frequencies and attenuates the frequencies close to zero. This is good when trying to filter out a slowly decaying exponential. There is also a computational advantage to eliminating the multiply and accumulate instructions associated with imaginary terms. Note also from Figure 2.27 that the cosine filter matches the response on the DFT at 60 Hz so doesn't require amplitude compensation. However, off-frequency signals will be more affected by the cosine filter frequency response than by DFT filters. One solution is to adjust the sampling rate to be an integer number of the fundamental by matching the sampling rate with an integer multiple of the measured period with a zero-crossing detector. Adjustments to the sampling period should be slow, so as to track only the power system frequency changes and not the frequencies generated by transients.[16]

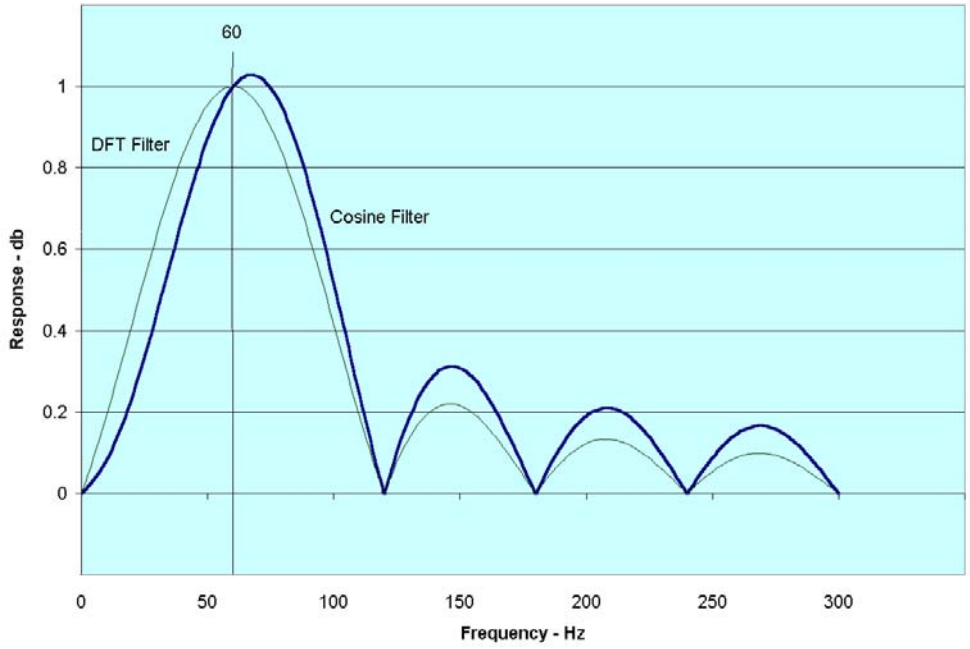


Figure 2.27: Frequency Response Comparison of a 16th-Order DFT and Cosine Filter From Zero to 300 Hz

To obtain another computational advantage, use the cosine filter for both the real and imaginary parts of the complex vector. Make the most recent cosine filter output the real term and the output that has been delayed a quarter of the period of the fundamental the imaginary term, as shown in Equation 2.90 and Equation 2.91. Both the real and the imaginary terms now have identical frequency responses.

$$Yc_n = \sum_{0}^{N-1} A_n X_n,\ A_n = \left(\frac{2}{N}\right)\cos\left(\frac{2\pi n}{N}\right) \qquad \text{Equation 2.90}$$

$$Y_n = Yc_n + jYc_{n-N/4} \qquad \text{Equation 2.91}$$

Figure 2.28 shows the transient response of the DFT and cosine filters. The magnitude transient shows that the filter output is indeterminate until the time equal to five-quarter 60 Hz cycles of steady-state input has passed. The advantage of the cosine filter is that there is less magnitude overshoot that can cause a relay using this output to overreach and operate incorrectly.

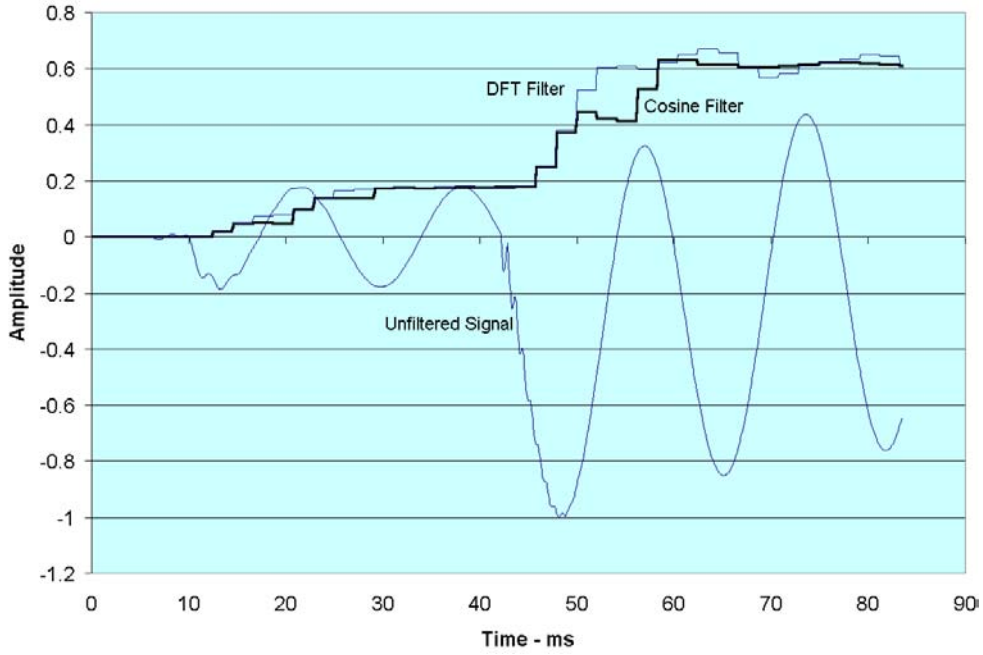


Figure 2.28: Magnitude Response of a 16th-Order DFT and Cosine Filter Processed Eight Times per 60 Hz Cycle

Since we know that the DFT of the pure sine wave is the desired output, we can make it our evaluation reference. Computing the absolute difference between the reference output and the outputs of the DFT filter and the cosine filter, we can see the improvement. The difference for the cosine filter response reduces overshoot and achieves an overall smaller difference. The cost of the improved offset rejection is that the filter transient is extended by the time equal to one quarter of the period of the fundamental. This is not obvious from Figure 2.28 because it is difficult to differentiate the signal transient from the algorithm transient.

Digital Logic

Digital logic theory applies logic control to all technologies, whether electro-mechanical relay contacts, bipolar and CMOS transistors, discrete logic gates, or microprocessors. Digital systems are becoming more important to power system monitoring and control because nearly all analog computers have been replaced by microprocessor systems.

There are four basic logical operations in digital logic, AND, OR, XOR, and NOT. An inverter integrated circuit (IC) usually implements the logical NOT function in hardware. Additional elementary logic elements with hardware IC implementations are the NOT AND, or NAND gate, and the NOT OR, or NOR gate. The simple elementary logic gates are AND, OR, NAND, NOR, XOR, and INVERTER gates.

Truth tables such as Table 2.2 through Table 2.5 explicitly describe input/output characteristics of logical systems. Table 2.6 lists some identities that allow complex Boolean expressions to be reduced to simpler expressions.

Logical values are restricted to values of TRUE (1), or some predefined voltage of a two-level system, or a False (0), or the other voltage levels in a two-level system. For digital systems using TTL and 5V CMOS technology, +5V is usually assigned to the TRUE or 1 condition and 0V to the False or 0 condition. Logic systems following this convention are said to be active high.

The result of logical operations is either a TRUE or a FALSE. A general rule of thumb for digital logic states the simplest expression usually results in a minimal hardware implementation. This rule is valid as long as the types of gates used for hardware implementations are limited to simple elementary logic gates.

Table 2.2. AND Operation Truth Table

Input A	AND	Input B		Result C
0	•	0	=	0
0	•	1	=	0
1	•	0	=	0
1	•	1	=	1

Table 2.3. OR Operation Truth Table

Input A	OR	Input B		Result C
0	+	0	=	0
0	+	1	=	1
1	+	0	=	1
1	+	1	=	1

Table 2.4. XOR Operation Truth Table

Input A	XOR	Input B		Result C
0	⊕	0	=	0
0	⊕	1	=	1
1	⊕	0	=	1
1	⊕	1	=	0

Table 2.5. Invert Operation Truth Table

Input B	Invert	Result C
0	NOT	**1**
1	NOT	**0**

Table 2.6. Boolean Identities

A • NOT(A)	=	0
A + NOT(A)	=	1
A ⊕ 0	=	A
A ⊕ 1	=	NOT(A)
NOT(A • B)	=	NOT(A) + NOT(B)
NOT(A + B)	=	NOT(A) • NOT(B)

Logical operations give no significance to bit position in bit sets, whereas arithmetic operators attribute such weighting and usually work with groups of 8-, 16-, 32-, and 64-bit sequences. Implement arithmetic operations such as add and subtract using the XOR function with the appropriate carry or inversion and borrow bit as represented by Equation 2.92 and Equation 2.93. The multiply and divide operations use algorithms involving add and subtract operations as well as other logical operations. Complex mathematics such as transcendental functions (sine, cosine, and logarithms) as well as raising a number to a power or taking roots of a number are also possible. Mathematical operations that require binary numbers use a numbering system such as the one described next.

$$A + B = A \oplus B + Carry \qquad \text{Equation 2.92}$$

$$A - B = A \oplus (NOTB) + Borrow \qquad \text{Equation 2.93}$$

Number systems

Modern digital computers operate in one of two stable states called high and low, true and false, or one and zero. When a set of binary values is given weighting based upon the bit position in the set, then the set of ones and zeros can represent larger values. This concept is no different from the commonly used decimal numbering system or the base ten numbering system. Use Equation 2.94 to convert a value to base ten from any other base. N_{10} is the base ten equivalent of value A in its native base, assuming that the least significant position is on the right. Table 2.7 lists the equivalency for numbers using three common bases, decimal (base ten), binary (base two), and hexadecimal ($base_{16}$).

$$N_{10} = A_k \cdot B^k + \cdots + A_2 \cdot B^2 + A_1 \cdot B^1 + A_0 \cdot B^0 \qquad \text{Equation 2.94}$$

Table 2.7: Equivalency Table for Common Number Bases

Decimal	Binary	Hexadecimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

Converting from base ten to an arbitrary base requires successively dividing the base ten number by the new base and recording the remainders. The integer value of the quotient from each successive computation is the dividend for the next. This process continues until the quotient is zero. Compute the least significant position first, then progress to the last remainder. Figure 2.29 illustrates this process for the conversion of 35000 to base$_{16}$. Read the result from the bottom to the top as 88B8$_{16}$.

Quotient	Re*mainder*
$16\overline{)35000}_{10}$	
$16\overline{)2187}_{10}$	8_{16}
$16\overline{)136}_{10}$	B_{16}
$16\overline{)8}_{10}$	8_{16}
$16\overline{)0}_{10}$	8_{16}

Figure 2.29: Operations in Converting 35000_{10} to $8B88_{16}$

Relay Ladder Logic

In the past, mechanical switches and solenoids completed logic. Relays encapsulated electromechanical switches such that one solenoid could operate many contacts. Contacts have three configurations, A, B, and C. Form A contacts are open when the solenoid is not energized, or normally open. Form B contacts are normally closed when the solenoid is deenergized. Form C contacts are three-terminal devices with a common connection, a terminal that is normally open, and one that is normally closed. Figure 2.30 represents these devices schematically. Multiple contacts may also have contact numbers.

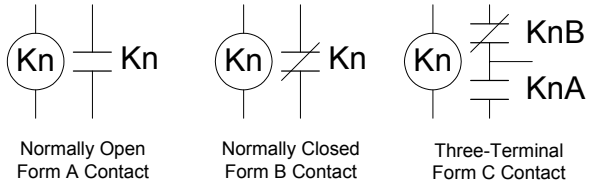


Figure 2.30 Relay Contact Configurations

Figure 2.30 shows how relay logic generates logic functions. Inputs and outputs are always contacts. A series of contacts makes a circuit to energize one or more coils or solenoids. Contacts in parallel form OR logic and contacts in series form AND logic. Using the normally closed contacts inverts the logic. Contacts can be manual switches, other relays, and in some cases transistors. There is no restriction on what constitutes a switch as long as the contacts can withstand voltage B+ to B- and the current necessary to energize the output coils and solenoids.

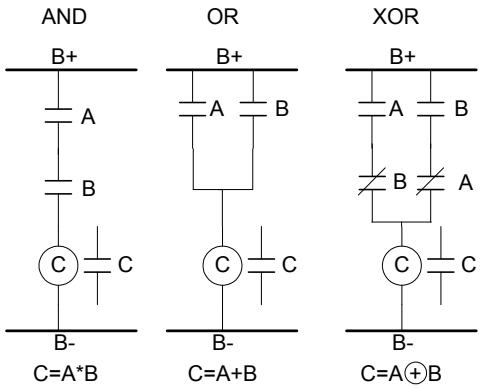


Figure 2.31: Elementary Logic Functions Using Relay Logic

Elementary logic functions make arithmetic operations. Since all relay logic can implement all elementary logic functions, relay logic can and has implemented computing machines, such as the large relay-operated computing machines used by the U.S. Army during World War II to compute artillery firing charts.

Logic Descriptions

When documenting logic systems, be sure to describe the Boolean algebra in a way that allows the reader to easily and quickly determine the function and operation of the logic without deciphering the math. The abstraction process removes details in

the same way that a hardware block diagram removes schematic diagram details for the sake of simplicity. An abstract description of a digital system is only the start of the design process.

Some recent description languages, such as VHDL, Verilog HDL, and state charts allow simulation and hardware synthesis. These tools help keep the design process in the correct order. We will discuss some of the more popular tools, such as flow diagrams and FSA.

Flow diagrams

Flow diagrams, widely used and relatively easy to follow, describe data processes for sequential systems. These descriptions normally don't contain timing information. Figure 2.32 shows some of the more common symbols, although symbol usage varies considerably and relatively few standards exist for using flow diagrams. Generally, the text within the symbols abstractly describes what is being done or the condition of the program at that point in the process. It is not easy to document multitasking and interrupt drive systems using flow charts because these systems have processes that are initiated by random, rather than sequential, events.

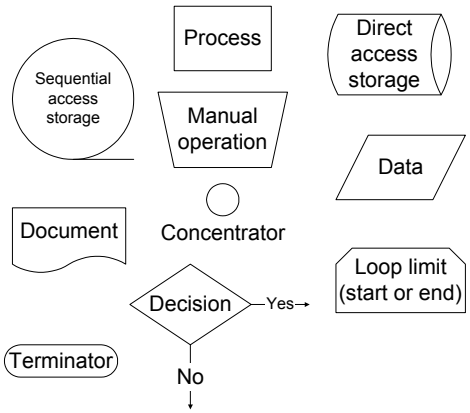


Figure 2.32: Common Flow Chart Symbols

FSA

Finite state automina describe digital systems that have stable states or conditions that the system remains in for a finite time. This requires feedback or memory to hold the system in suspension until conditions are right for the system to go to the next stable state. Flip-flops and latches are the most common forms of memory. Internal or external events, such as triggers from an internal timer or input actions, initiate transitions between stable states. View the system description from the events that cause the program to move from one process to the next. Processes represented by flow diagrams execute on the transition between stable states.

State machines are synchronous or asynchronous. Asynchronous state machines can transition from one state to the next any time the conditions for the transitions are met. Synchronous state machines transition between states only when a synchronizing clock makes either a positive or negative transition. Poor design methodologies can skew timing, causing asynchronous state machines to fail when

races or hazards occur. One source of skewed timing is differences in the sequencing of two or more inputs. Another source is differences propagation delays through multiple paths in the digital hardware of a common logic parameter.

A race occurs when the transition path can vary depending on the order in which the inputs to logic gates change. The race becomes critical if the two paths result in different stable states. Critical races can be eliminated by proper state assignment or by synchronization. A hazard occurs when the output generates one or more glitches during the process of making the transition from one stable state to another. A glitch is a positive or negative pulse that is not supposed to exist. Adding a consensus term that adds redundant logic and the output at one state during the course of the transition can eliminate hazards. Unfortunately, redundant systems cannot be fully tested.

Although not as fast as and usually requiring more logic, synchronous systems are less susceptible to both races and hazards than asynchronous systems. Nearly all state machine designs are synchronous today because the complexity of modern digital systems makes predicting propagation delays almost impossible.

State Diagrams

Use Figure 2.33, an example of the convention used for state diagrams, to describe both synchronous and asynchronous state machines. The state designations and sometimes the state variables are inside the circle representing a state. Transitions show as arcs between states. The arc labels are either a transition designation or the logic conditions that make the transition true. If using designations for state and transition identifiers, provide a table that explicitly defines the input or state variables. The output conditions are listed beside the state circles. Theoretically, a transition can occur between two states in the system, but this rarely happens. The design implementation dictates which particular transitions are permitted.

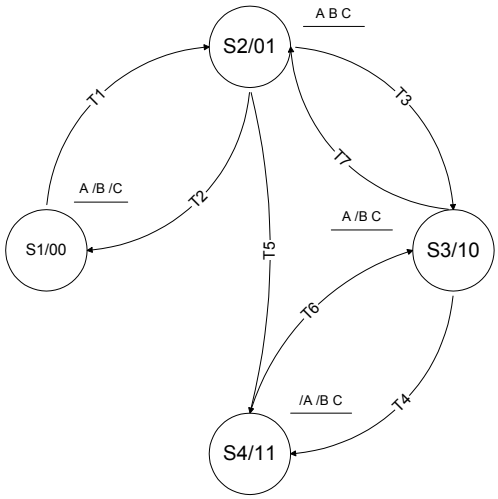


Figure 2.33: Example of a State Diagram

Unified Modeling Language (UML) State Charts

UML State Charts combine the process flow description of flow charts with the state descriptions of state diagrams and are extremely useful for describing multitasking event-driven processes. Some vendors can generate code directly from state chart description. Unfortunately, the only target processor for this code is the x86 family and the only language supported is Visual Basic by Microsoft. Since this is a fairly new technology, there are few vendors offering products at this time and information is limited to a few texts.

Computing Systems

Computing today distributes the intelligence of the CPU, but uses a shared information database. Although shared information allows users to save on investment and provides easy access to information, the system speed performance is compromised. Distributed computing systems replicate frequently needed information on local computers and maintain updated copies in the shared memory space.

No one processor can optimally do all the jobs assigned to computers today. Our discussion in this section is limited to the processors frequently used in control and embedded systems. Although present real-time control systems use PCs and workstations, their operating systems are usually incompatible with requirements for reliability and speed. The specific processors used in PCs and workstations are perfectly capable of performing in real-time control applications if they have the necessary hardware and software support.

Processor classifications fall along different lines. Processors use either the von Neumann architecture (shared with code and data bus) or Harvard architecture (separate code and data bus). Harvard architecture computers are generally faster and have larger memory capability; they are also more complex and have difficulty operating on nonvolatile data stored in the code memory space. Such differences are largely transparent to the programmer.

For convenience, we will maintain three further computer classifications: complex instruction set computers (CISC), reduced instruction set computers (RISC), and digital signal processors (DSP). Pentium processors are CISC and have instructions that require varying numbers of bytes. Some instructions involve compound operations such as the integer multiply, divide, and decrement-and-branch-if-zero instructions. It is difficult to learn the assembler language for such processors because of the quantity and complexity of the commands. Fortunately, high-level language programming insulates developers from most of these issues.

RISC processors use a minimal number of primitive instructions that execute one instruction per word. In this context, the word is a native width for code that is fetched using a single fetch operation. RISC processors are pipelined so that the processor can be simultaneously fetching and executing. There is still debate about whether CISC or RISC computers are faster and require less memory to complete tasks. The answer usually depends on the benchmark being used for the comparison.

DSP processors are really a subclass of RISC processors with additional computing hardware that makes them particularly efficient for executing multiply and

accumulate (MAC) instructions. Digital filtering algorithms use these instructions repeatedly, as discussed in paragraph 0. In addition to the conventional ALU contained in all computers, DSP processors also have a hardware multiplier and hardware adder that can operate in parallel with each other as well as with the ALU. A single word, usually 16 bits in width or greater, contains instructions, which are also divided into control fields that determine the operation for the ALU, multiplier, and adder.

Microprocessors and Microcontrollers

The usual concensus about the difference between microprocessors and microcontrollers is that microcontrollers are designed with a high degree of I/O capability and microprocessors are designed to handle large amounts of data efficiently. The two designs have more common characteristics than differences, but Table 2.8 lists some of these distinctions.

Table 2.8: Comparison of Microprocessors and Microcontrollers

	Microprocessors	**Microcontrollers**
Code Memory	Large	Small
Data Memory	Large	Small
Direct I/O pins	Few	Many
Autonomous operation	No – needs O.S.	Yes – O.S. built in
Number of Interrupt sources	Few	Many
Special functions	Few	Many
Cost	High	Low

Refer to ***How Microprocessor Relays Respond to Harmonics, Saturation, and Other Wave Distortions*** by Stanley E. Zocholl and Gabriel Benmouyal for additional information.

Memory

Digital computer systems require both code memory and data memory. Code memory contains the instructions that the processor executes. For a given application, this memory should not change. Some programmers develop computers that produce self-generated or self-modified code. Avoid this practice, except for rare instances, because such code is not testable. The memory for storing code and constant data must be nonvolatile so that when the power is deenergized and reenergized, this memory is not destroyed. Masked ROM, OTP ROM, UV-EPROM, EE-EPROM, FLASH memory, and battery backed-up static RAM are common technologies for nonvolatile memory embedded systems. Larger computer-based systems may use a combination of these, as well as a mass-memory media such as floppy disk, hard disk, and CD ROM.

The computer must be able to modify memory for storing variable data, usually by static or dynamic RAM technologies. Computers that need to retain data after the

system is deenergized may use nonvolatile memory that is easily modifiable such as battery backed-up static RAM, EEPROM, Flash memory or disk. Although the latter three options are less expensive, they also have limited lifetime write cycles and are considerably slower.

The amount of memory in a particular memory device is classified either by a single value representing the total number of memory bits or a two-dimensional array of the number of data bits wide by the number of address bytes deep. Dynamic memory in PCs is typically nine bits wide, having eight data bits and a one parity bit for error detection. In general, however, semiconductor memory is packaged as either eight or 16 bits wide. Disk memory is single-bit wide on the storage media but may be repackaged to a width suitable for the processor by a disk controller.

Equation 2.95 shows the depth of a memory device computed by the number of address lines.

$$Depth = 2^{Number\ of\ address\ lines} \qquad \text{Equation 2.95}$$

Input and Output

All microprocessors and many microcontrollers support access to external ROM and RAM memory devices. Access macrologic integrated circuits such as serial communications drivers (UARTS), interrupt controllers, analog-to-digital converters (ADC), and digital-to-analog converters (DAC) using memory address space and mapped-memory I/O.

Processors use three types of control lines or pins to access memory, both code and data, and mapped memory I/O; address lines, data lines, and control or hand-shaking lines. Use address and data lines for I/O devices in the same way as memory, discussed above. Data lines are bidirectional and are commonly shared with all devices that interface to the processor through the memory expansion lines.

Address decoding gives the processor a means to distinguish the access to one device from all the others connected to the external memory bus. Some processors have a set of chip-select control outputs while others rely on external ICs using combinational logic to decode specific address ranges and to generate the appropriate chip-select signals. Multiple address lines on an I/O device give the processor access to control, status, and data registers internal to the particular I/O device. For example, ICs that perform timekeeping functions typically have a register for the year, month, day, hour, minute, second, and tenth of a second. Other registers set up the timekeeping format. Since these timekeeping ICs have battery backup, there are often additional registers for applications requiring a small amount of nonvolatile memory. Such devices have five or more address lines to provide access to all the various internal registers.

Control lines, in addition to selecting the particular device to be accessed, also direct the flow of information on the data line either to or from the external I/O or memory device. Some processors share the address and data lines using time division multiplexing. The processor supplies a control line to signal when the shared address and data bus contain address information and when it is being used for data. Some ICs decode this signal directly, while others require external decoding and latching of address information.

Interrupts are special I/O control lines that require the processor to be managed by the user-developed code. These are hardware-generated program subroutine call instructions to a predetermined address. Mask bits that enable and disable their operation manage the interrupts. Catastrophic operations such as power failure require that some interrupts remain impervious to this disabling. These nonmaskable interrupts are extremely useful for allowing a processor system to fail in a safe and predictable way.

Special Functions for Microcontrollers

Computers need special purpose semiconductor devices to expand processor I/O capability and functionality. These include analog input, pulse width modulation (PWM) for analog output, event timers, synchronous and asynchronous serial communications, and multiple access serial networks. Individual ICs, commonly used for microprocessors, can also provide the functions and services provided by these devices.

Microcontrollers frequently include the special hardware on the same silicon wafer as the processor. Since the intended use for the microcontroller is in systems that require a minimum of support hardware, integrating the special purpose hardware with the processor eliminates external addressing and improves the access speed.

Gate Arrays

Gate arrays are semiconductor devices containing hundreds of thousands of logic gates and flip-flops that are massively interconnected in a two-dimensional array. End users or customer-developers can use inexpensive devices to program field programmable gate arrays (FPGA). Programming these devices consists of retaining or eliminating interconnections between gates and flip-flops that subsequently generate the desired logic functions.

System designers frequently use Gate arrays (extremely fast Boolean processors) to off-load computing requirements in a hardware-software co-design because either the processor is too slow or the demands would consume too much processor time. Gate array designs are quickly replacing designs using discrete logic circuits such as the 7400 series TTL and CMOS logic.

3 POWER SYSTEM INSTRUMENTATION

INSTRUMENTATION CHARACTERISTICS [6038[17], 6027[22]]????

Instrument transformers for measuring 60 Hz voltage and current function similarly to power transformers. Differences in construction accommodate the primary or high-side voltage and current. For example, the primary of both the voltage and the current instrumentation transformers must support the primary potential. The safety of both people and equipment requires electrical isolation from the primary voltage. The voltage transformer (VT) and the current transformer (CT) scale the magnitude so conventional instruments can process the system information.

The main objective for these devices is accurate reproduction of signal characteristics on the secondary side of the transformer in amplitude, phase, and frequency content. Construction and application control the accuracy of this signal reproduction. Instrument transformer load is called burden and has units of volt-amps (VA). Unless the instrument accuracy is specified at a specific burden, lower burden usually results in more accurate measurements, based on nameplate ratings.

The Ideal Transformer Model

Ideally, the transformer power input identically equals the power output and the primary amp-turns identically equal the secondary amp-turns, as shown in Equation 3.1. Application of these two identities results in the three equal ratios shown in Equation 3.2 for an ideal transformer.

$$Vp\ Ip \equiv Vs\ Is$$
$$Ip\ N1 \equiv Is\ N2 \qquad \text{Equation 3.1}$$

$$\left(\frac{N1}{N2}\right) = \left(\frac{Vp}{Vs}\right) = \left(\frac{Is}{Ip}\right) = N \qquad \text{Equation 3.2}$$

$$Zp' = N^2\ Zp,\ ZP' = N^2\ Rp + N^2\ 2\pi fLp \qquad \text{Equation 3.3}$$

Figure 3.1 shows the equivalent circuit of a nonideal transformer electrical model. This model relates all primary parameters to the secondary side using Equation 3.3 and includes wire resistance for the primary and secondary windings in R_p and R_s respectively. This model also includes the excitation reactance and the iron-core loss, which is the price paid (in watts) to energize the transformer regardless of the transfer power. The transformer with windings N1 and N2, shown in Figure 3.1, is now considered ideal. Equation 3.1 and Equation 3.2 are not valid for this model.

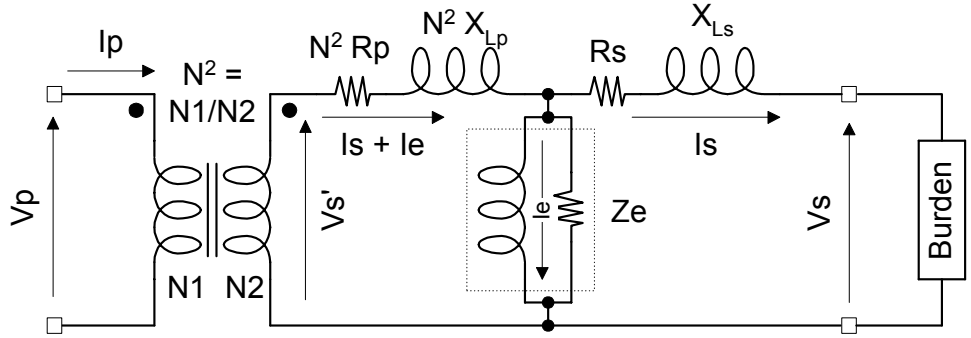


Figure 3.1: Schematic of Equivalent Circuit of Transformers

The model in Figure 3.1 shows the effects that burden has on how accurately Vs represents *Vp* multiplied by a constant. Since *Vs'* represents the theoretical secondary voltage, compute the percentage magnitude error using Equation 3.4, assuming the transformer has an ideal turns ratio. Equation 3.6, which follows from Equation 3.4 and Equation 3.5, shows that error is directly proportional to load current and leakage impedance. The approximation introduced by ignoring the excitation current to simplify the math is valid as long as the burden is much larger than the current through the excitation branch.

$$Amplitude\ Error = \left(\frac{Vs - Vs'}{Vs'} \right) 100\% \qquad \text{Equation 3.4}$$

$$Vs \cong Vs' - Is \left(\sqrt{\left(N^2 Rp + Rs\right)^2 + \omega^2 \left(N^2 Lp + Ls\right)^2} \right) \qquad \text{Equation 3.5}$$

$$\text{Amplitude Error} \cong \left(\frac{-\left(\text{Is} \left(\sqrt{\left(\text{N}^2\text{Rp} + \text{Rs}\right)^2 + \omega^2 \left(\text{N}^2\text{Lp} + \text{Ls}\right)^2} \right) \right)}{\text{Vs'}} \right) 100\% \qquad \text{Equation 3.6}$$

It is important to consider load impedance when computing the phase error, as shown in Equation 3.7 through Equation 3.11, in which *Rb* and *Lb* represent the burden resistance and inductive impedance. Simplify by ignoring the excitation branch. Use Equation 3.9 to determine the phase error and as an alternate to Equation 3.6 for expressing the amplitude error. Equation 3.7 through Equation 3.11 show that phase distortion and amplitude errors are small if the circuit inductance is small in comparison to the circuit total resistance. A low burden or low circuit inductance will reduce transformer scaling errors.

It is also important to consider the impedance of the control wiring when determining amplitude and phase errors. If the burden is capacitive, modify Equation 3.7 through Equation 3.11 appropriately.

$$Zb \angle \theta b = \sqrt{\left(Rb\right)^2 + \omega^2 Lb^2} \angle \arctan\left(\frac{\omega Lb}{Rb} \right) \qquad \text{Equation 3.7}$$

$$Zt\angle\theta t = \sqrt{(Rp + Rs + Rb)^2 + \omega^2 (Lp + Ls + Lb)^2} \angle \arctan\left(\frac{\omega(Lp + Ls + Lb)}{Rp + Rs + Rb}\right)$$ Equation 3.8

$$Vs\angle\theta s = Vs'\angle 0 \left(\frac{|Zb|}{|Zt|}\right)\angle(\theta b - \theta t)$$ Equation 3.9

$$Phase\,error = \theta s = \theta b - \theta t$$ Equation 3.10

$$Amplitude\,error = \left(\left(\frac{|Zb|}{|Zt|}\right) - 1\right)100\%$$ Equation 3.11

Polarity

Polarity designations of instrumentation transformers allow proper phasing of voltages and currents. The dots beside the transformer windings in Figure 3.1 denote the polarity terminals and are similarly identified on the physical transformer. Convention dictates that primary current into the polarity terminal induces secondary current out of the polarity terminal. Likewise, a positive voltage presented to the primary polarity terminal produces a positive voltage on the secondary polarity terminal.

CURRENT TRANSFORMERS (CTS)

Design

CTs are used anywhere ac current is measured, on transformer and circuit breaker bushings, on bus bars, on transmission line conductors, and on grounding straps.[17] They have single (or at most a few) turn(s) primary windings and many secondary windings. A typical rating specifies primary amps to 5 secondary amps, such as 600:5, although other standards are used as well. For instance, instead of a 5-amp secondary rating, use a 2-amp or 1-amp rating. The primary windings must have the capacity to carry the expected current, plus fault current for a short duration.

How are current transformers different from voltage transformers or power transformers? Consider first how CTs connect into the power circuit. As shown in Figure 3.2, the CT is wired in series with the source, line, and load impedances such that the phase current is also the primary CT current. Since the parameter of interest is current, not voltage, the instrumentation must have impedance that is much less than the impedance of the circuit being instrumented. Ideally, current transformers are constant current devices where low leakage impedance is desirable.

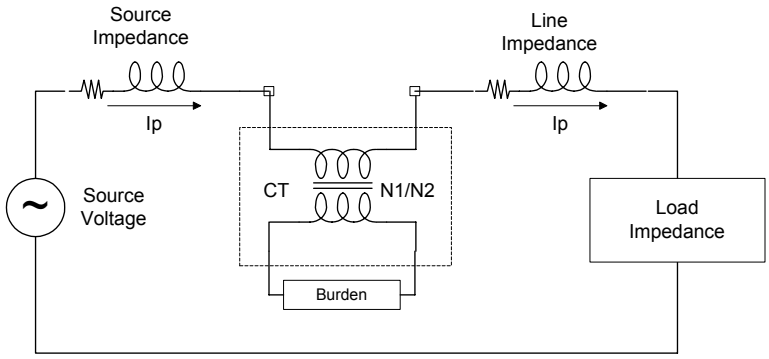


Figure 3.2: CT Connection for Measuring Line Amps

Operation and Errors????

Saturation????

CT Equivalent Circuits

A current transformer can be modeled as a constant current source where ratio current is injected into a magnetizing impedance in parallel with the burdens shown in Figure 3.3. Using a reactance to represent the magnetizing leg of a CT, as shown in Figure 3.3, is a useful visual concept. However, magnetization is a nonlinear phenomenon, and each level of excitation needs different values of reactance. For example, the three B-H diagrams in Figure 3.3, as flux φ versus magnetizing current I_M, represent low, medium, and high levels of excitation.

At low excitation, slope $d\phi/dl$ representing the inductance is low, indicating a disproportionate amount of magnetizing current compared to the burden current at low excitation. At medium excitation, $d\phi/dl$ is relatively high and the magnetizing current is small compared to the current in the burden. At high excitation, the B-H curve exhibits the maximum slope in transition between saturated states. Because magnetizing current is so small compared to the ratio current during the transition it can be ignored. Consequently, view the core simply as a volt-time switch, as shown in Figure 3.3, that opens during a rate of flux change and closes during saturation.

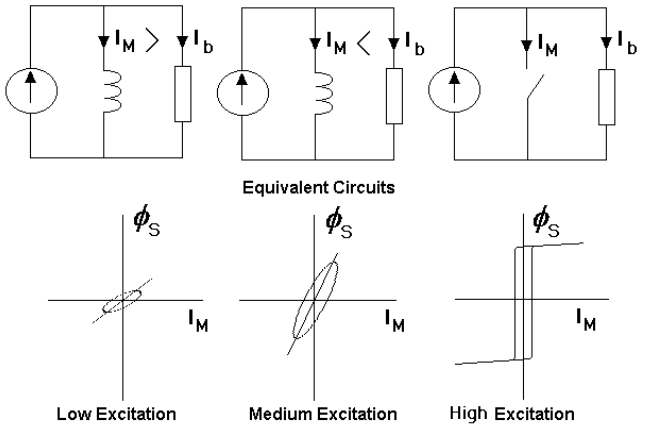


Figure 3.3: CT Equivalent Circuits at Various Levels of Excitation

Zocholl discusses a volt-time concept that assumes the magnetic core is a volt-time switch.[17] This concept assumes no magnetizing current when there is rate of change of flux and all the ratio current flows to the burden. When saturation flux is reached, as indicated by volt-time area, and there is no longer a change of flux, the switch closes. This shunts the entire ratio current away from the burden until a reversal of current and integration becomes negative, to reduce the flux. Here saturation occurs at a well-defined point indicated by specific value flux and turns.

However, establishing flux in the core requires finite ampere-turns, which can be expressed as magnetizing current measured at the secondary terminals. The excitation current, which is subtracted from the ratio current, has definite values for each voltage as shown by the excitation curve in Figure 3.4. This figure depicts steady-state voltage versus excitation current where voltage is measured with an average reading voltmeter calibrated in rms. It is actually a plot of flux versus magnetizing current, since the average voltage is the volt-time integral averaged over the period of the sine wave.

Excitation Curves

The excitation curve shown in Figure 3.4 represents a C800, 3000:5 multiratio bushing CT. This curve is a measure of CT performance that determines ratio correction factors at various levels of steady-state excitation. Where it has a well-defined knee-point, it has no discernable point of saturation. For this reason relaying accuracy ratings are based on a ratio correction not exceeding 10 percent and ratings are designated by classification and secondary voltage.

Multiratio CTs allow the CT to produce close-to-rated-secondary current at maximum expected load. This provides maximum resolution for both relays and metering. As indicated in the text in the bottom right of Figure 3.4, we can obtain a 3000:5 ratio by connecting the secondary current leads to terminals X1 and X5, resulting in 600 total turns. Using these taps, the transformer is capable of eight ohms of external load. Obtain the C800 rating by multiplying the maximum allowable load by 20 times the rated secondary, which, for this case, is 100A. Use terminals X2 and X5 to connect this CT as a 2000:5 ratio CT. However, the

excitation current now follows the next lower curve in Figure 3.4 and the excitation voltage is proportionally derated to (2000/3000) of 800 V or 533 V. Hence, the maximum allowable load impedance is 5.333 Ω. Table 3.1 has a complete summary of possible turns ratios for the transformer in Figure 3.4. Table 3.1 also shows the reduced allowable load resistance at lower CT ratios. A 300:5 C800 CT would again allow 800V excitation voltage and an eight-ohm load. Examine closely the merits of using the 3000:5 multiratio CT at 300:5 versus a 300:5 CT. Mitigating circumstances such as temporary station configurations or anticipated load growth may make the multiratio CT a suitable choice.

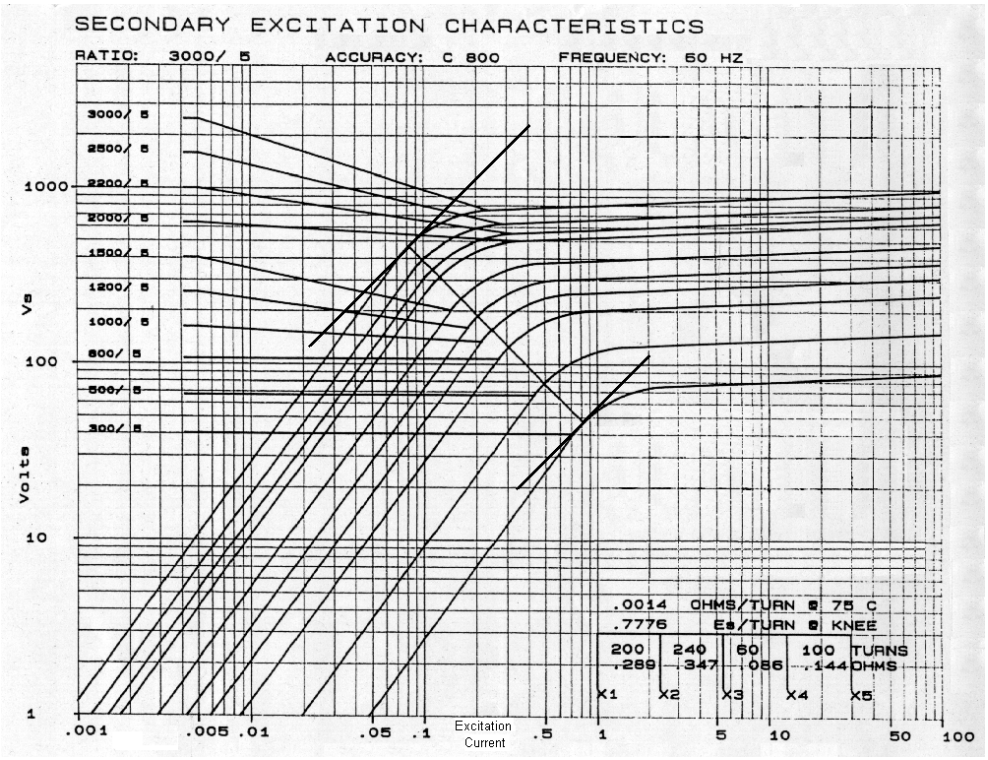


Figure 3.4: 3000:5 CT Excitation Curve and Various Taps Both With Knee-Point Tangents and With Normal Lines

Table 3.1: Terminal Connections for Possible CT Ratios for Multiratio 3000:5 CT With Characteristics Shown in Figure 3.4

Ratio	Total Turns	Terminals	Maximum V	Maximum Load
3000:5	600	X1 – X5	800	8.00 Ω
2500:5	500	X1 – X4	667	6.67 Ω
2200:5	440	X1 – X3	587	5.87 Ω
2000:5	400	X2 – X5	533	5.33 Ω
1500:5	300	X2 – X4	400	4.00 Ω
1200:5	240	X2 – X3	320	3.20 Ω
1000:5	200	X1 – x2	267	2.67 Ω
800:5	160	X3 – X5	213	2.13 Ω
500:5	100	X4 – X5	133	1.33 Ω
300:5	60	X3 – X4	80	0.80 Ω

The C and K classifications cover toroidal CTs with distributed windings. In these cases, neglect leakage flux and calculate the ratio using a standard burden to determine the excitation voltage. Then read the excitation current from the curve. The K rating is a proposed rating where the knee-point is at least 70 percent of the secondary voltage rating. The secondary voltage rating is the voltage the CT will deliver to a standard burden at 20 times rated secondary current without exceeding 10 percent ratio correction. The standard burden values for relaying are 1.0, 2.0, 4.0, and 8.0 ohms, all with an impedance angle of 60°. Consequently, at 20 times the rated current of 5 amperes the standard voltage ratings are 100, 200, 400, and 800 volts. Use standard burden values of 0.1, 0.2, and 0.5, with a 25.8° impedance angle, for rating metering CTs that are of insufficient accuracy for relaying.

A multiratio CT is voltage rated using the maximum turns ratio. The voltage read from the upper curve at 10 amps excitation current is 486 volts. This is less than the standard rating of C800 but above C400. Accordingly, the CT is rated C400. Calculate the magnetizing impedance of the CT by dividing each value of voltage read from the curve by the corresponding excitation current. The results are shown in Table 1. The magnetizing impedance is nonlinear, increasing from 1200 ohms at 0.001 amps excitation current to a maximum of 5625 ohms at 0.08 amperes of excitation. This is the point of maximum permeability and is located by the 45° tangent to the curve. The impedance values decrease from this point because the excitation is increased, reaching 90 ohms at 10 amperes of excitation current.

Table 3.2: Excitation Curve Values for the CT Characteristics of Figure 3.4

V(volts)	Ie(amperes)	Ze(ohms)
1.2	0.001	1200
3.0	0.002	1500
5.0	0.003	1667
10	0.004	2500
29	0.010	2900
70	0.020	3500
250	0.050	5000
450	0.080	5625
530	0.100	5300
720	0.200	3600
800	1.000	800
830	4.000	207
870	6.000	145
900	10.00	90

Refer any point on the maximum ratio curve to a lower ratio tap by using a constant volts-per-turn relation for the voltage and a constant ampere-turn relation for the current. Consequently:

$$V_2 = \frac{N_2}{N_1} V_1 \qquad I_2 = \frac{N_1}{N_2} I_1 \qquad \text{Equation 3.12}$$

so that the knee-point of each curve lies along the normal line to the 45° tangent drawn in Figure 3.4. Figure 3.4 also shows the curve for the 300:5 ampere minimum tap.

Burden

The electrical model presented in Figure 3.5 provides insight into how CTs work. Categorize the impedance in this circuit into the power system impedance, Z_{PS}, which consists of Zsource, Zline, and Zload. An equivalent circuit shows where the power system impedances are referred to the CT secondary side. For the secondary current to ideally represent the primary current, the referred power system impedance must be much greater than the CT impedance plus the burden impedance. If the burden is zero, then the secondary current is only affected by the leakage reactance, which by design is small compared to the expected power system impedance.

If the burden increases, the impedance in the magnetizing branch can go into saturation. This causes a significant amount of current to flow through the magnetizing branch instead of through the burden connected to the secondary.

Operating transformers in saturation causes both amplitude and phase errors, as well as deforming the current waveform.[18,19,20]

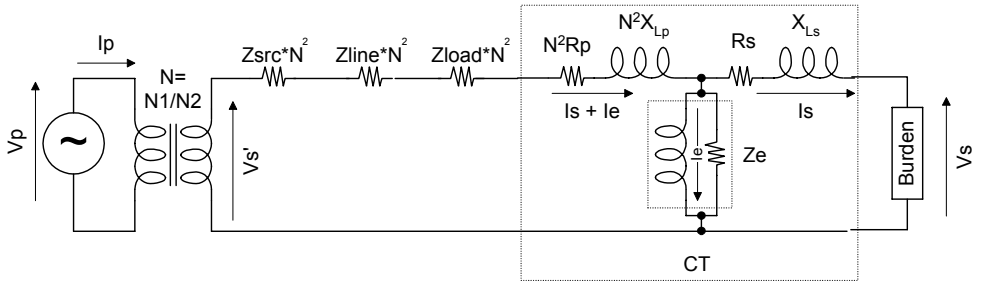


Figure 3.5: Equivalent Circuit of CT Interconnected into a Power System

To illustrate, consider the following example. Assume that the power system impedances are as follows: Zsource = 0.1 + j 0.4Ω, Zline = 0.3 + j1.2Ω, and Zload = 16 + j4.0. Also assume that we are using a CT with characteristics shown in Figure 3.5 on the 300:5 tap so that N = 60. Then the power system impedance, Z_{PS}, referred to the secondary side is the sum of Zsource = 360 + 1440Ω, Zline = 1080 + j4320Ω, and Zload = 57600 + j14400Ω. A typical value of CT impedance is 0.0014Ω/Turn. Since the number of turns is 60, the CT impedance is Z_{ct} equal to j0.084Ω and the burden impedance is 10VA with a 0.8 power factor at rated current of five amps. This results in a burden impedance of $Z_B = 0.32 + j0.08\Omega$. To determine the error introduced by the instrumentation, compare the current when the CT and burden are in the circuit to the current when the CT and burden are not in the circuit, while holding the source voltage constant. Again, the analysis in Equation 3.13 through Equation 3.16 ignores the magnetizing current branch. For the current example, the ratio error caused by burden is only 0.000057 percent.

$$Is1 = \frac{Vs'}{Z_{PS}} \qquad \text{Equation 3.13}$$

$$Is2 = \frac{Vs'}{Z_{PS} + Z_{CT} + Z_B} \qquad \text{Equation 3.14}$$

$$Current\ error = \left(\frac{Is1 - Is2}{Is1} \right) 100\% \qquad \text{Equation 3.15}$$

$$Current\ error = \left(\frac{Z_{CT} + Z_B}{Z_{PS} + Z_{CT} + Z_B} \right) 100\% \qquad \text{Equation 3.16}$$

If the error calculations include excitation impedance, then consult Figure 3.4 to obtain excitation current. The excitation voltage is the secondary current through the burden times the sum of the CT and burden impedances. For this example, the excitation branch voltage is 1.8V. The excitation current for the 300:5 tap in Figure 3.4 is approximately 0.1A. This results in a 2 percent current error. The total error is the sum for the burden current error plus the error caused by the exciting current. Examination of Figure 3.4 shows that using the largest tap that metering sensitivity requirements allow helps keep errors as small as possible. This also allows the

highest possible instrumentation burden. Equation 3.17 expresses the basic rule of thumb. High burden that results in CT saturation causes relay to under reach.

$$\left[\left(\frac{X}{R}+1\right)I_F \cdot Z_B\right]_{PU} < 20 \qquad \text{Equation 3.17}$$

Ratio Correction Factor (RCF)

RCF is the ratio of the true transformer ratio to the nameplate or marked transformer ratio.[21] Since the secondary voltage is also a function of the burden, the RCF is not a constant, as discussed in 0. The ANSI C37.15 classification of CTs guarantees specific accuracy if the burden is under specific limits, but only applies to 60 Hz currents. Adding compensation windings to instrument transformers corrects for amplitude errors at rated burden. Calculating the RCF for a given load requires knowledge of the characteristics for each individual transformer. Figure 3.6 includes typical ratio correction factor data to assist in the computations. CT manufacturers provide such curves for specific external burdens. Measuring the exact ratio in the field may provide more accurate results with similar or even less effort.

Saturation can change RCF at high currents. The low-pass nature of a CT transfer function makes the RCF different for currents at frequencies other than 60 Hz. This may be a problem for relays when the power system is in a transient condition from normal switching or faults. It may also present problems for relays that operate on current harmonics or relays that are based on traveling wave technology. The bandwidth of a typical CT is 5 kHz.

When multiratio CTs have characteristics such as the ones shown in Figure 3.4 and Figure 3.6, using reduced ratio taps also reduces accuracy. Likewise, higher burdens also reduce accuracy. Figure 3.6 shows RCF characteristics for a specified burden, which for this case is the rated load of eight ohms. Note the perceived increase of accuracy as the secondary current increases. This is because the excitation current that can be seen as the cost of energizing the CT dominates the errors at low currents. At higher currents, the magnetizing current is a smaller percentage of the total current. Transformer saturation from the voltage across the magnetizing branch reverses the accuracy trend as secondary current increases. Figure 3.6 shows this saturation occurring at progressively lower values of CT secondary current as the ratio is reduced by tap selection. Figure 3.6 also demonstrates that using the highest ratio produces the highest accuracy.

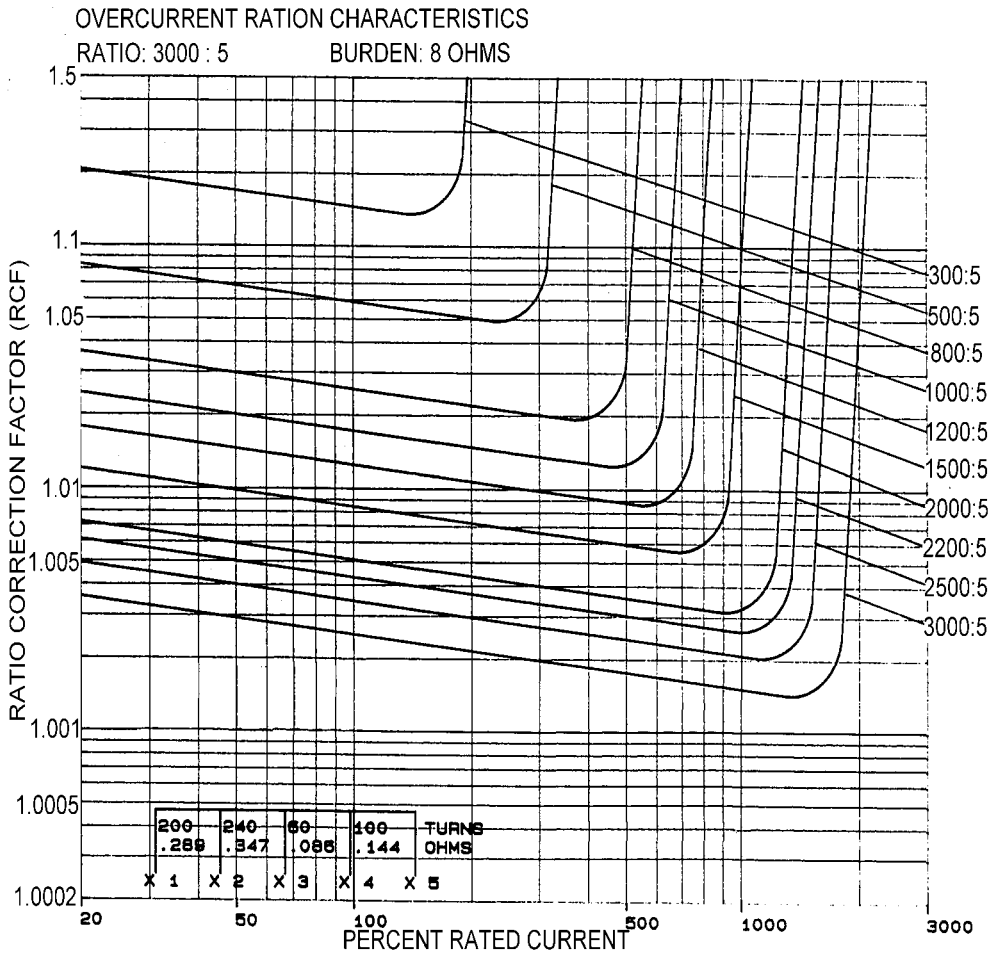


Figure 3.6: Typical Ratio Correction Factor Curves

Angle Correction Factor (ACF)

The transformer burden also affects the phase of the secondary current. Figure 3.5 and Equation 3.18 show this dependency clearly.

$$\angle Is = -\arctan\left(\frac{XLp + XLs + XLb}{Rp + Rs + Rb}\right) \qquad \text{Equation 3.18}$$

where *Xlp* and *Rp* are referenced to the transformer secondary side.

Standards

ANSI C37.15, available from IEEE Standards publications, lists the standards for construction and application.

Practices[22]

To select the proper CT for an application you must know the application environment and the accuracy required. The application environment includes primary voltage, maximum operating current, maximum fault current, network reactance to resistance ratio, and the instrumentation burden.

Generally, protective relays use fundamental frequency sine waves as inputs and their performance is not specified for other waveforms. Therefore, in a protective relay application, the voltage and burden of the CT should be specified to ensure undistorted secondary current for the maximum fault condition.

IEEE/ANSI Standard C57.13 suggests applying CTs for relaying based on the maximum symmetrical fault current not exceeding 20 times the CT current rating and the burden voltage not exceeding the accuracy class voltage of the CT. There is a rationale for choosing a CT to produce the knee-point on the excitation curve at the maximum symmetrical fault current since the magnetizing reactance is at a maximum. Observe that the knee-point of a typical excitation curve is about 46 percent of excitation voltage corresponding to 10 amperes excitation current. A rule-of-thumb suggests that the C-rating be twice the excitation voltage developed by the maximum fault current, which guarantees operation near the knee-point of the excitation curve for the maximum symmetrical fault.

Preventing saturation from the exponential component of fault current requires a C-rating exceeding the symmetrical rating by a factor equal to the X/R ratio of the faulted primary system plus one. Unfortunately it is routinely impossible to achieve such ratings despite the fact that saturation affects the performance of high-speed relays. In these cases, use simulations to assess the effects of transient saturation on relay performance.

Creating an open-circuit in the CT secondary while connected to an energized power system results in dangerously high potential across the open circuit. The model in Figure 3.2 shows how. The burden impedance reflected back to the primary side is the inverse of the turns ratio squared. If the load resistance is infinite, then the reflected impedance is also infinite regardless of the CT turns ratio. This theoretically causes the primary line-to-ground voltage to drop across the CT primary turns. The voltage is then coupled to the secondary side of the CT that is now operating as a step-up voltage transformer. As a result, the theoretical secondary voltage is the primary line-to-ground voltage divided by the turns ratio. Regardless of the primary voltage, dangerously high potentials can damage personnel and equipment.

Example Calculation of Errors

This example uses the CT curves shown in Figure 3.4 and Figure 3.6 and the circuit shown in Figure 3.5. Equation 3.19 includes the resistance of substation CT wiring with the burden resistance. As shown in the previous sections, the CT burden consists of internal burden, the CT impedance and external burden, and the impedance of the devices connected to the CT, plus the substation CT wiring resistance.

$$Rw = e^{0.232G - 2.32}\ \Omega / 1000\, ft. \qquad \text{Equation 3.19}$$

where *G* is AWG wire gauge.

The data in the lower right of Figure 3.4 shows that the CT secondary winding resistance is 0.0014 Ω per turn. Therefore, the greater the turns ratio, the greater the total resistance. We now consider three cases where the CT ratio is 3000:5, 2000:5, and 1000:5. In all three of these cases, the CT wiring length will be set to 1000 ft, so the resistance is 1 Ω.

Case 1: CTR = 3000:5

Initially, the device burden (or relay resistance) is set to zero. The CT resistance is 600 turns multiplied by 0.0014 Ω/turn or 0.84 Ω. Therefore, the total burden is 1.84 Ω. At rated current (5A) and at unity power factor, the voltage across the excitation branch is 1.84 Ω times 5 A or 9.2 V. Refer to Figure 3.4; for a 3000:5 ratio an excitation voltage of 9.2 V equates to 0.0045 A in the excitation branch. This current, which is shunted through the inductive branch, is orthogonal (90°) to the current through the burden. The current through the relay is now expressed by Equation 3.20. The magnitude and phase angle errors from the CT at the prescribed ratio are very small.

$$I_{RELAY} = 5.0000A\angle 0° - 0.0045A\angle -90° = 5.0000A\angle -0.05° \qquad \text{Equation 3.20}$$

Case 2: CTR = 2000:5

For this case the CT resistance is now 400 turns times 0.0014 Ω/turn, or 0.56 Ω. The total CT burden is now 1.56 Ω, resulting in an excitation voltage of 7.8 V when operating at the 5 A rated current. From Figure 3.4, the excitation current is now 0.008A∠-90°. The resulting relay current for this case is 5.0000A∠-0.09°. Again, the errors are small.

Case 3: CTR = 1000:5

Using the 1000:5 tap of a 3000:5 CT means that only one third of the CT voltage capability is being used. The CT resistance for this case is 200 turns times 0.0014 Ω/turn or 0.28 Ω. With the CT burden at 1.28 Ω, the excitation current is 0.0225A∠-90°. The relay current is now 5.0001A∠-0.26°. Even for this case, the magnitude and current errors remain small.

Example Summary

The data in Table 3.3 show the results of similar cases performed on two additional manufacturers' CTs using the same test conditions as the preceding three cases. This demonstrates that the CT performance is the same for other manufacturers. Microprocessor-based relays have burden on the order of 0.15 VA at 5 A rated current. This equates to 0.03 Ω, which justifies the assumption of zero device burden.

Table 3.3: CT Ratio Magnitude and Angle Errors for 5 A of Burden Current

	CT Brand 2		CT Brand 3	
CT Ratio	600:5	300:5	1200:5	600:5
R_{CT}	0.276 Ω	0.138 Ω	0.432 Ω	0.216 Ω
R_{TOT}	1.276 Ω	1.138 Ω	1.432 Ω	1.216 Ω
V_{EXCITE}	6.38 V	5.7 V	7.16	6.08 V
I_{EXCITE}	0.0225 A ∠-90°	0.060A∠-90°	0.0055 A∠-90°	0.017 A∠-90°
I_{RELAY}	5.0001 A ∠-0.258°	5.0040 A ∠-0.69°	5.0000 A ∠-0.063°	5.0000 A ∠-0.195°

POTENTIAL MEASURING DEVICES

Numerous instruments can measure the primary circuit voltage. Cost, accuracy, and application voltages vary to meet the requirements of the application account. Conventionally, the secondary voltage for power system voltage transformers is 120 Vac phase-to-phase or 69.3 Vac phase-to-ground.

VT

Voltage transformer (VT) devices are usually more accurate than other conventional potential measuring devices. VT devices use wire-wound construction in a similar manner to conventional power transformers with two windings wound around a common iron core. Discussions in section 0 about operations and errors for current transformers also apply to voltage transfomers. The main difference is in what constitutes burden. Although high load impedance constitutes a high burden for CTs, the opposite is true for VTs, which are constant voltage devices where it is desirable to have minimal magnetizing current.

For VTs, power can flow from the primary side or the secondary side. It is possible to generate, either intentionally or unintentionally, primary voltages by energizing VTs from the secondary side. If the VTs are installed in a substation, it is possible to energize portions of the substation by this back-feeding phenomenon.

CCVT

Capacitor-coupled voltage transformers use a capacitive voltage divider and a low voltage transformer for impedance matching as shown in Figure 3.7. These devices can also couple high frequency RF signals to the power line for communication.

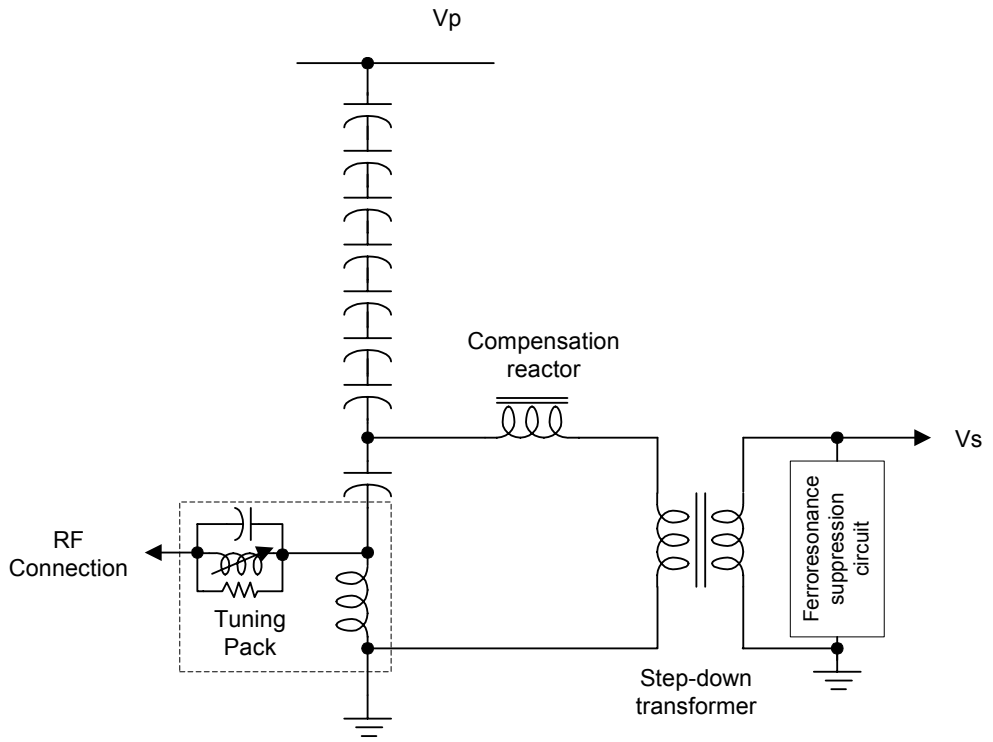


Figure 3.7: Schematic Diagram of a CCVT With RF Connection

Design

The capacitor stack is usually in a hollow porcelain insulator and filled with insulating oil. A bellows mechanism at the top of the stack allows the oil to expand and contract from variations in temperature. The top of the capacitor stack is connected to the high voltage bus. The parallel LC circuit, comprised of the bottom capacitor and the transformer, T, makes a resonant circuit tuned for 60 Hz. This construction, while good for metering accuracy, has degraded performance when operated out of its nominal operating range. This has adverse affects on relaying.

The tuning pack is an optional feature on some CCVTs to provide coupling for power line carrier communication. The nominal frequency range of these communications signals is 50 kHz to 400 kHz. The drainage reactor in the ground branch of the tuning pack provides a path to ground for the 60 Hz signal while providing a high impedance block to the RF signal. The parallel RLC network provides band-pass filtering for the RF signal. The high inductance of the power transformer at the bottom of the stack keeps the RF signal from leaking into the low voltage 60 Hz output.

Operation and Errors

Since the CCVT consists of both a capacitive voltage divider and a two-turn voltage transformer, ratio errors can occur from both capacitor inaccuracies and transformer inaccuracies, as discussed in sections 0 and 0. Higher accuracy VTs reduce standing voltages (sequence voltages measured during nonfault, line-energized conditions)

and improve RF coverage. Table 3.4 compares the performance of two possible classes of VTs: Class 1 and Class 2. Note that Class 1 errors are half the rate of Class 2 errors.

Table 3.4: Class 1 and 2 Maximum Magnitude and Phase Angle Errors

VT Class	Maximum Magnitude Error[1], δM	Maximum Phase Angle Error, δΘ
Class 1	±1%	±40 MOA[2] (±0.67°)
Class 2	±2%	±80 MOA[2] (±1.33°)

The coupling capacitors of the CVT function as voltage dividers to step down the line voltage to an intermediate-level voltage, typically 5 to 15 kV. The compensating reactor cancels the coupling capacitor reactance at the system frequency. This reactance cancellation prevents any phase shift between the primary and secondary voltages at the system frequency. The step-down transformer further reduces the intermediate-level voltage to the nominal relaying voltage, typically $115/\sqrt{3}$ volts.

The compensating reactor and step-down transformer have iron cores. Besides introducing copper and core losses, the compensating reactor and step-down transformer also produce ferroresonance caused by nonlinearity of the iron cores. Because of this, CVT manufacturers include a ferroresonance-suppression circuit. This circuit is normally used on the secondary side of the step-down transformer. Although it is necessary to avoid the dangerous and destructive overvoltages caused by ferroresonance, the ferroresonance-suppression circuit can aggravate the CVT transient, depending on the suppression circuit design. We discuss suppression circuits later.

When a fault suddenly reduces the line voltage, the CVT secondary output does not instantaneously represent the primary voltage. This is because the energy storage elements, such as coupling capacitors and the compensating reactor, cannot instantaneously change their charge or flux. These energy storage elements cause the CVT transient.

CVT transients differ depending on the fault point-on-wave (POW) initiation. The CVT transients for faults occurring at voltage peaks and voltage zeros are quite distinctive and different. Figure 3.8 and Figure 3.9 show two CVT transients for zero-crossing and peak POW fault initiations. For comparison, each figure also shows the ideal CVT voltage output (ratio voltage). Figure 3.8 shows a CVT transient with a fault occurring at a voltage zero. Notice that the CVT output does not follow the ideal output until 1.75 cycles after fault inception.

Figure 3.9 shows the CVT response to the same fault occurring at a voltage peak. Again, the CVT output does not follow the ideal output. The CVT transient for this case lasts about 1.25 cycles. The CVT transient response to a fault occurring at points other than a voltage peak or voltage zero takes a wave shape in between those shown in Figure 3.8 and Figure 3.9.

---

[1] *This error is specified for $5\% \le V_{measured} \le 100\%$ with W, X, and Y burdens for Class 1, and Z burden for //Class 2. Reference [3] further defines these burdens.*

[2] *MOA is the abbreviation for Minutes of Angle. 60 MOA = 1°*

Each CVT component contributes to the CVT transient response. For example, the turns ratio of the step-down transformer dictates how well a CVT isolates its burden from the dividing capacitors C_1 and C_2. The higher the transformer ratio, the less effect the CVT burden has on these capacitors. The different loading that different transformer ratios cause on the CVT coupling capacitors changes the shape and duration of CVT transients.

Next, we discuss how two key CVT components affect the CVT transient response: the coupling capacitors and ferroresonance-suppression circuit.

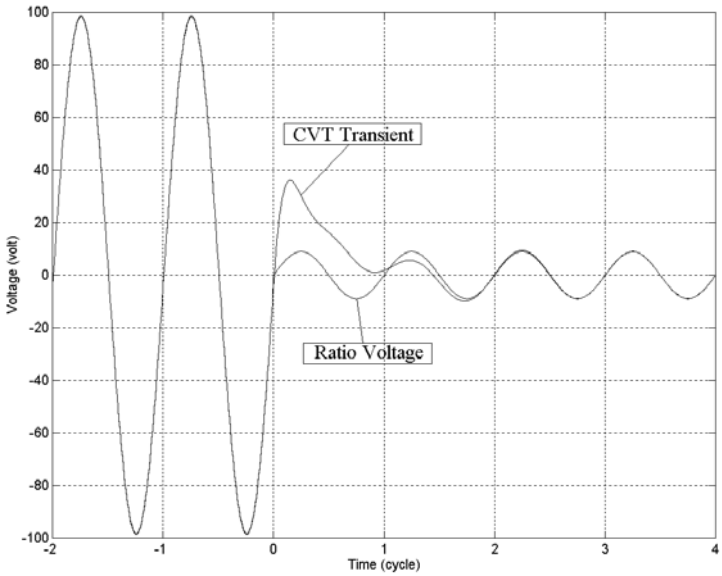


Figure 3.8: CVT Transient with Fault at Voltage Zero

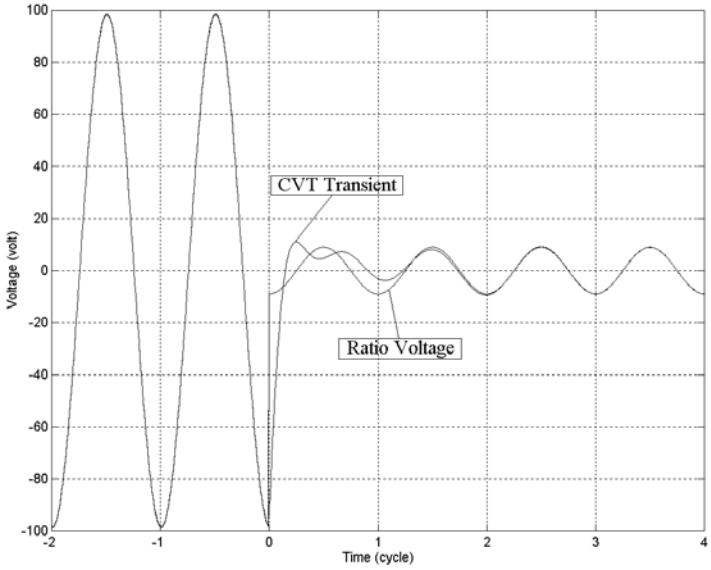


Figure 3.9: CVT Transient with Fault at Voltage Peak

Coupling Capacitor Value Affects CVT Transient Response

A CVT is made up of a number of capacitor units connected in series. The number of capacitor units depends on the applied primary voltage level. The CVT capacitance is represented by two values: one for the equivalent capacitance above the intermediate voltage point (C_1) and the other for the equivalent capacitance below the intermediate voltage point (C_2). The Thevenin equivalent capacitance value ($C_1 + C_2$) is different from the total capacitance $C_1 \cdot C_2/(C_1 + C_2)$ normally given by manufacturers. $C_1 + C_2$ is approximately 100 nF for the CVTs studied in this paper. Some CVT manufacturers differentiate CVTs as normal-, high-, or extra high-C CVTs.

The capacitance value associated with high-C CVTs decreases the CVT transient magnitude. To see this, compare the CVT transient plots of Figure 3.8 and Figure 3.10 for a fault initiated at a voltage zero. Figure 3.10 shows the transient response of a CVT with four times the total capacitance of that shown in Figure 3.10.

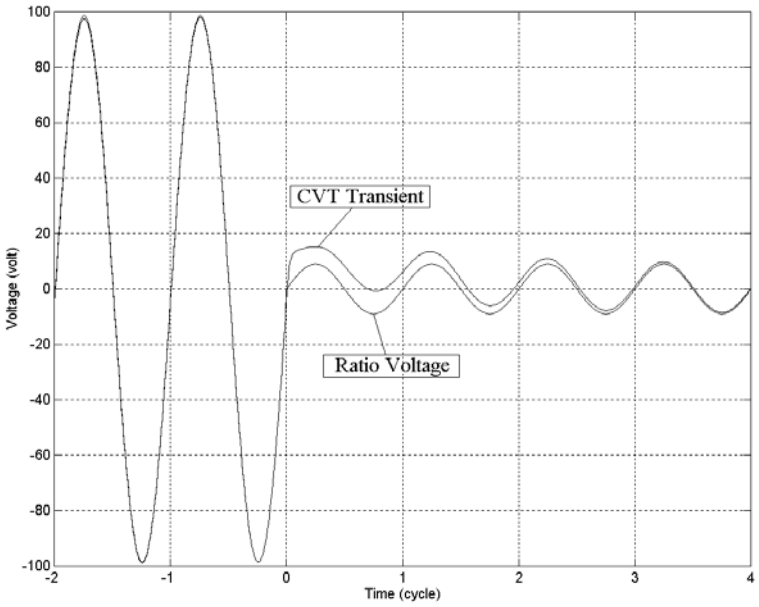


Figure 3.10: Transient Response of a High Capacitance CVT

Distance elements calculate a fault-apparent impedance based on the fundamental components of the fault voltage and current. The fundamental content of the CVT transient determines the degree of distance element overreach. Figure 3.11 shows the fundamental components of the same CVT outputs shown in Figure 3.8 and Figure 3.10. We obtained the fundamental magnitudes by filtering the CVT outputs using a digital band-pass filter. Note that the fundamental component of the higher capacitance CVT output voltage is closer to the true fundamental magnitude than that of the lower capacitance CVT. Therefore, any distance element overreach caused by a transient output of a higher capacitance CVT is much smaller than that caused by the transient output of a lower capacitance CVT.

Increasing the CVT capacitance value can increase the CVT cost but decreases the CVT transient response. Thus, engineers must strike a balance between CVT performance and CVT cost.

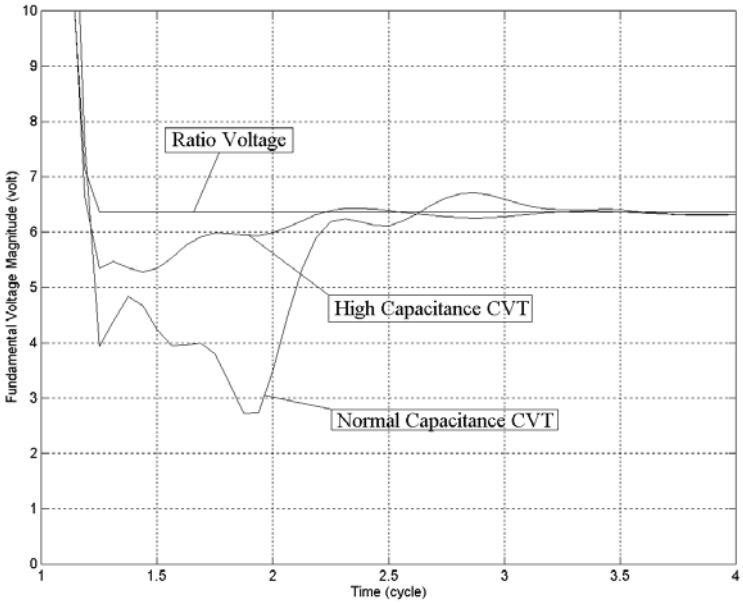


Figure 3.11: Higher Capacitance CVT Causes Less Reduction in the Fundamental Voltage Magnitude

Ferroresonance-Suppression Circuit Design Affects CVT Transient Response

Figure 3.12 shows two types of ferroresonance-suppression circuits.

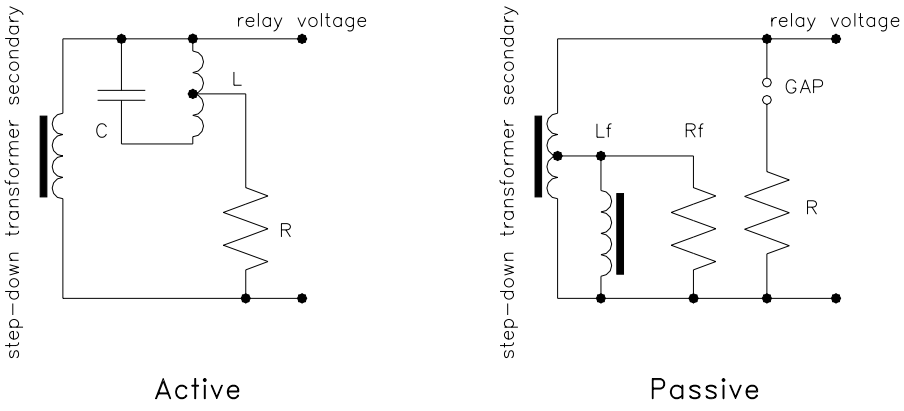


Figure 3.12: Active and Passive Ferroresonance-Suppression Circuits

Active Ferroresonance-Suppression Circuits

Active ferroresonance-suppression circuits (AFSC) consist of an LC-parallel tuning circuit with a loading resistor. The LC-tuning circuit resonates at the system frequency and presents a high impedance to the fundamental voltage. Connecting the loading resistor to a middle tap of the inductor increases the resonant impedance of the circuit. For frequencies above or below the fundamental frequency (off-nominal frequencies), the LC-parallel resonant impedance gradually reduces to the resistance of the loading resistor and attenuates the energy of off-nominal-frequency voltages.

Passive Ferroresonance-Suppression Circuits

Passive ferroresonance-suppression circuits (PFSC) have a permanently connected loading resistor Rf, a saturable inductor Lf, and an air-gap loading resistor R. Under normal operating conditions, the secondary voltage is not high enough to flash over the air gap, and the loading resistor R has no effect on the CVT performance. Once a ferroresonance oscillation exists, the induced voltage flashes over the gap and shunts in the loading resistance to attenuate the oscillation energy. Lf is designed to saturate at about 150 percent of nominal voltage to further prevent a sustained ferroresonance condition.

Ferroresonance-Suppression Circuit Effects on CVT Transient Performance

The AFSC acts like a band-pass filter and introduces extra time delay into the CVT secondary output. The energy storage elements in the AFSC contribute to the severity of the CVT transient.

In contrast, the PFSC has little effect on the CVT transient. Most components of the circuit are isolated from the CVT output when ferroresonance is not present. Figure 3.13 shows the difference of the CVT secondary outputs for a CVT with an AFSC and a CVT with a PFSC for the same fault voltage. Note that the CVT with a PFSC has a better, less distorted transient response than the CVT with an AFSC. This less-distorted transient results in a fundamental magnitude that is closer to the true fundamental magnitude shown in Figure 3.14.

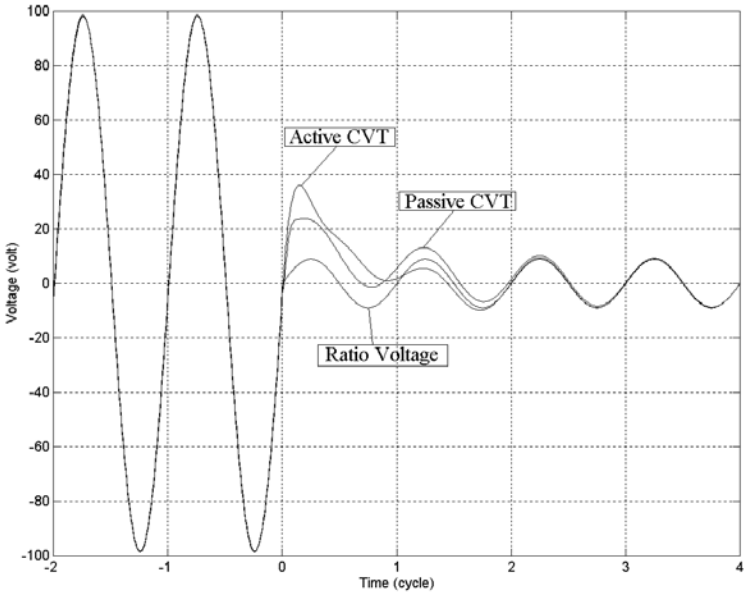


Figure 3.13: CVT Transients of AFSC and PFSC

?????

Figure 3.14: CVT with PFSC Causes Less Fundamental Component Reduction

The PFSC has a permanently connected resistor, which increases the VA loading of the intermediate step-down transformer. For the same burden specification, the CVT with PFSC requires a larger intermediate step-down transformer.

Distance Relay Performance

We modeled a simple power system, CVTs with AFSC and PFSC, and a generic distance relay to determine the performance of distance relays during CVT transients. Figure 3.15 shows the evaluation system.

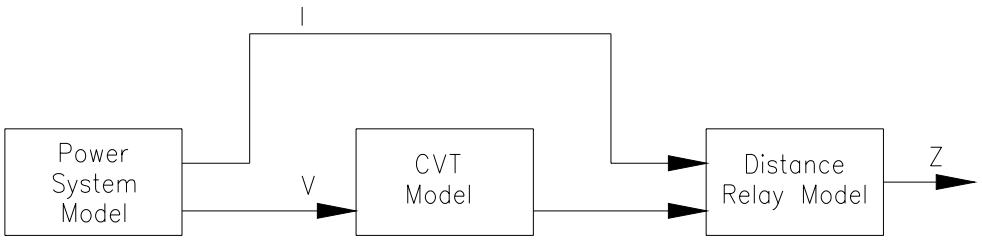


Figure 3.15: Distance Relay Evaluation System

Power-System Model

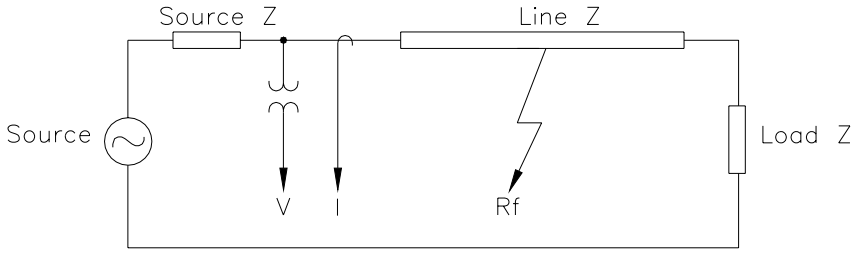


Figure 3.16: Power-System Model

Figure 3.16 shows the simple power-system model, a single-phase, radial system with fixed line impedance and variable source impedance. The difference between pre-fault and fault voltage levels heavily affects the CVT transient magnitude and duration. System SIR values, fault locations, and fault resistance (Rf) determine this voltage difference.

CVT Model

We used linear models for an active and a passive CVT. The parameters used in the models are from Reference [23]. The model includes the following CVT components:

- Coupling capacitors
- Compensating inductor
- Step-down transformer
- Ferroresonance-suppression circuit
- Burden

The stray capacitance and copper resistance of the compensating reactor and step-down transformer are included in the model to improve its accuracy at high frequencies.

We verfied all CVT model frequency responses against those obtained from [23]. In addition, we also compared the CVT transient outputs at voltage peaks and voltage zeros and verified that they were the same as those shown in reference [24].

The top plot in Figure 3.17 shows the frequency response of a CVT with an AFSC. Ideally, the frequency response should be a flat line at 0 dB, which means the CVT passes all frequency components without attenuation. Passing all frequency components makes the CVT output voltage a close representation of the CVT input voltage. If the frequency response shows attenuation at different frequencies, the CVT then behaves much like a filter and introduces transients and time delay.

The bottom plot of Figure 3.17 is the CVT output together with the ratio voltage. Ideally, the CVT output voltage is close to the ratio voltage. However, note that the CVT output voltage in Figure 3.17 does not match the ratio voltage for 1.75 cycles.

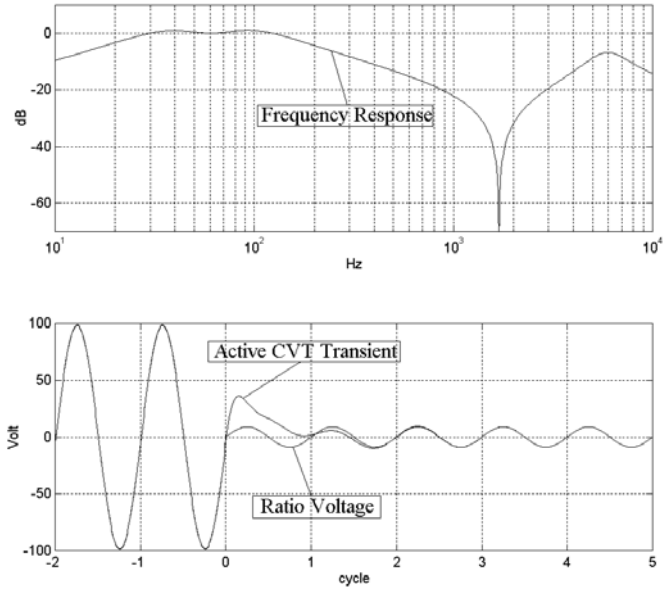


Figure 3.17: Active CVT Model Result

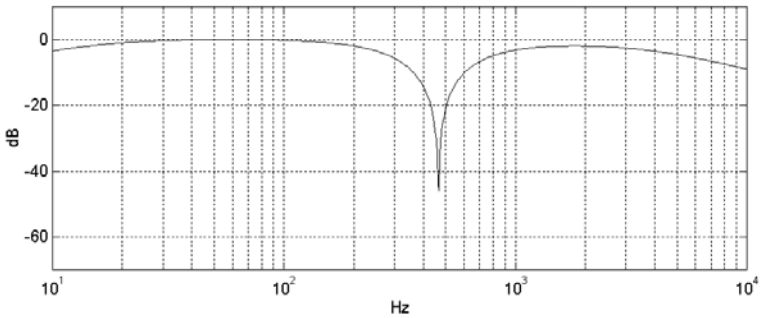


Figure 3.18: Frequency Response of Passive CVT Model

Figure 3.18 shows the frequency response of the CVT with a PFSC. Notice that this frequency response is much flatter than the one shown in Figure 3.17.

Relay Model

Figure 3.19 shows the distance relay model we used to evaluate the CVT transient effects. This model includes an analog anti-aliasing low-pass filtering, analog-to-digital conversion (decimation), digital band-pass filtering, and impedance calculation. The generic distance relay does not include security measures or other means of preventing CVT-transient-induced overreach.

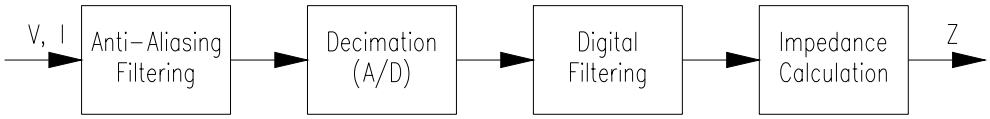


Figure 3.19: Relay Model

Distance Relay Performance Results

Figure 3.20 shows the generic distance relay response to the transients of CVTs with PFSC and AFSC. The fault applied is at the end of the radial line. The curves in the plot show the maximum Zone 1 reach setting that will not pick up from CVT transient errors.

From these curves, we see that the distance relay transient response for a CVT with a PFSC is much better because the relay has much less overreach. Using a CVT with a PFSC greatly reduces the need to decrease the Zone 1 distance element compared to using a CVT with an AFSC.

We limited fault POW initiations to voltage peaks and voltage zeros. Figure 3.20 shows the results in the worst distance element overreach cases, faults that occur at a voltage zero.

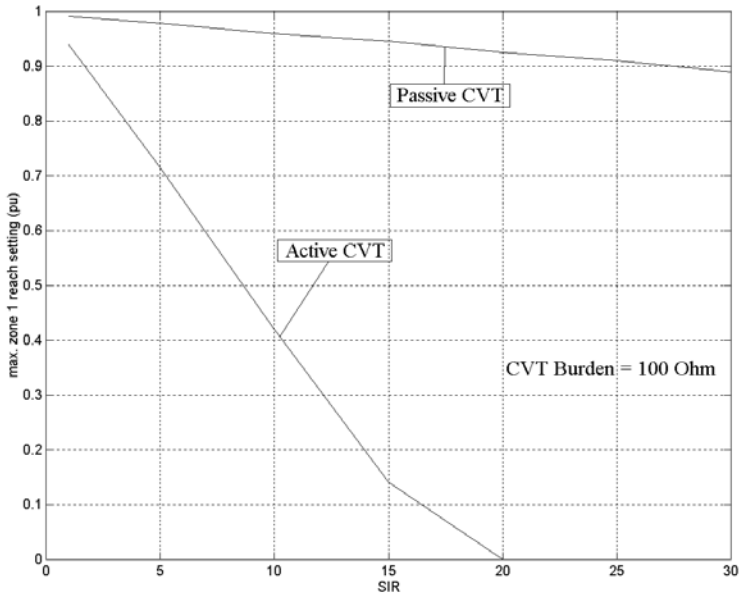


Figure 3.20: Distance Relay Performance with AFSC and PFSC

System Impedance Ratio (SIR)

The major factor that affects the severity of CVT transients is the fault voltage magnitude level. The smaller the fault voltage level, the greater the likelihood that the CVT will introduce a prolonged and distorted transient. System SIR directly influences the fault voltage level for a fault at a given location. Keep the SIR value in mind when assessing the influence of CVT transients.

Figure 3.20 shows a plot of maximum Zone 1 reach settings versus system SIR values. When used with the CVT having an AFSC, the Zone 1 element of the generic distance relay can tolerate CVT transients for systems with SIRs up to four. Eliminate the relay Zone 1 protection for systems with SIRs ≥ 20 unless there is additional logic.

The relay transient response when using a CVT with a PFSC is much better. Zone 1 protection is effective for system SIRs as high as 30.

CVT Burden

The magnitude and angle of the connected burden influence the CVT transient characteristic.

ANSI C93.1-1990 standard requires that the burden for CVT transient response testing be two impedances connected in parallel as in Figure 3.21. One impedance is a resistance (R_p), and the other impedance, (R_s and X_s), has a lagging power factor of 0.5. The burden value is 100 percent or 25 percent of the CVT maximum rated accuracy class voltamperes and has a power factor of 0.85.

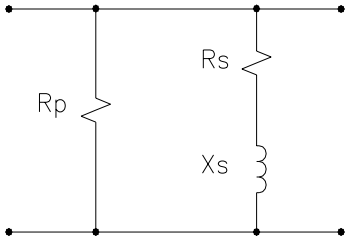


Figure 3.21: Burden for CVT Transient Testing

Figure 3.22 shows the maximum Zone 1 reach setting as a function of ANSI and resistive burdens for the CVT with a PFSC. The ANSI loading increases the CVT transient and distance element overreach compared to the resistive burden.

Solid-state and microprocessor relays have very small and nearly resistive input burdens. When using a CVT, ensure proper distance relay protection by calculating the total burden of all devices connected on the CVT and making sure the burden is not excessive and is nearly resistive.

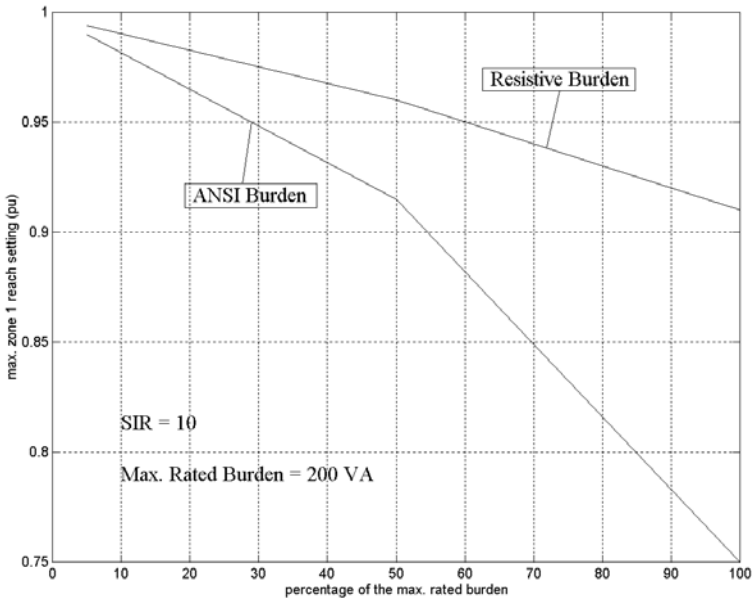


Figure 3.22: Relay Performance as a Function of CVT Burdens

CVT Transient Detection Logic

The generic distance relay has overreaching problems when:

- The system has a high SIR
- The CVT has an AFSC

This overreach problem is further aggravated if the CVT has a low C-value, and the CVT secondary has a heavy inductive burden.

This section introduces logic that:

- Eliminates the distance element overreach caused by CVT transients

- Causes minimum time delay for true in-zone faults
- Requires no special user settings
- Adapts to different system SIRs

Before introducing the CVT transient detection logic, we review some past solutions.

CVT Transient Overreach Solutions

Reach Reduction

One solution to CVT-transient-induced overreach is to reduce the Zone 1 reach. In some cases, the CVT transients could be so severe that Zone 1 protection must be eliminated.

Time Delay

Another method of avoiding Zone 1 distance relay overreach caused by CVT transients is to delay the Zone 1 elements. This time delay must be longer than the CVT transient duration.

The time delay solution is a simple and effective way to solve the problem. However, the time delay is then always present no matter what the system SIR value is or where the fault is located. Thus the time delay penalizes the fault clearing time even for a close-in fault on a low SIR system.

SIR Detection

Another solution is to detect the high SIR system condition using the measured voltage and current signals. When the voltage and current signals are below preset levels, the relay declares a high SIR condition. Once the relay detects a high SIR condition, it introduces additional filtering in the voltage channels, or a time delay into the distance element output decision. Both filtering and time delay methods have approximately the same effect.

The shortcomings with these SIR detection designs are:

- It is difficult to choose the overcurrent threshold setting. This setting is normally fixed by relay manufacturers. If the setting is small, the relay may overreach for some high SIR systems. If the setting is too large, the relay penalizes the fault clearing time for stronger systems.
- For high SIR systems, the fault currents for close-in and remote faults do not differ much. Relying only on the current level to detect high SIR conditions inevitably penalizes the tripping speed of close-in faults on high SIR systems.

Transient Detection Logic Description

The following text describes the proposed CVT transient detection logic. Recall from 0 SIR Detection that the distance element overreach increased with increasing SIR. The improved CVT detection logic uses this information to determine when

time delay is necessary to eliminate the CVT transient effect. The major improvements of this logic are:

- The relay automatically calculates voltage and current thresholds so does not require factory and user-entered settings.
- Distance calculation smoothness defeats the trip time delay for close-in faults on high SIR systems.

Figure 3.23 illustrates the block diagram of the CVT transient detection logic. The m is the distance calculation described in Reference [4] and δm is the incremental quantity of the distance calculation. In Figure 3.23, the 27 elements are phase-to-phase and phase-to-neutral undervoltage elements, and the 50 elements are phase-to-phase and phase-to-neutral overcurrent elements.

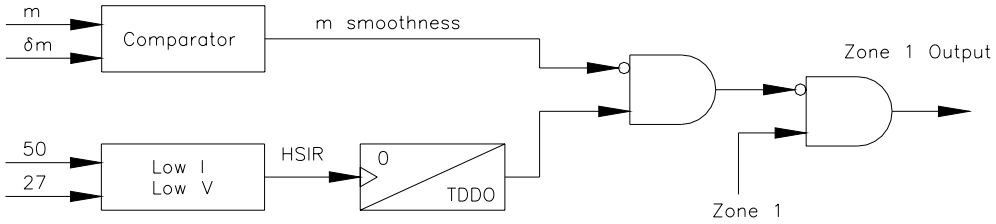


Figure 3.23: CVT Transient Detection Logic

Low-Voltage Detection

When the relay polarizing input voltage is depressed, we know that the relay voltage may include a CVT transient. We detect this low voltage with both phase-to-phase and phase-to-neutral undervoltage elements.

A high SIR system condition occurs when an undervoltage element picks up and the corresponding overcurrent element does not. HSIR output in Figure 3.23 picks up. Upon detecting a high SIR condition, the CVT logic adds a short time delay (TDDO in Figure 3.23) to the Zone 1 elements to prevent distance element transient overreach. We discuss this delay later.

Separate phase-to-neutral and phase-to-phase undervoltage elements are necessary because in phase-to-phase faults the phase-to-phase voltage decreases dramatically without an appreciable decrease in the phase-to-neutral voltage.

The CVT logic calculates the low-voltage thresholds based on a radial line with a predetermined SIR value. The threshold is the relaying voltage when a short-circuit fault occurs at the end of the radial line. As shown in Figure 3.24, the CVT transient detection logic calculates the phase-to-neutral voltage threshold as:

$$V_{phase} = \left|V_0 + V_1 + V_2\right| = \frac{V_{nom}}{(SIR+1)} \qquad \text{Equation 3.21}$$

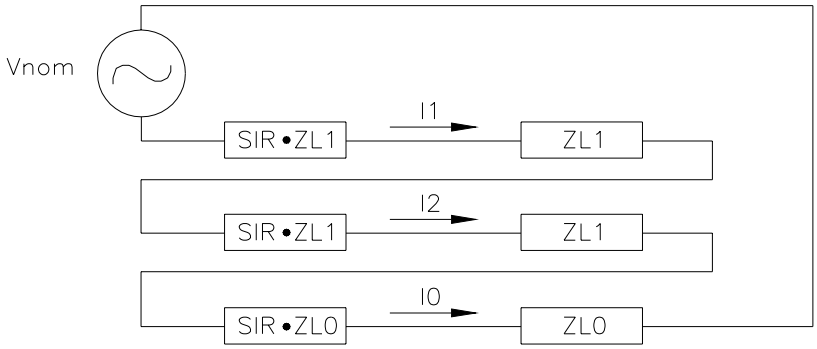


Figure 3.24: Sequence Network for an A-G Fault at Line End

As shown in Figure 3.25, the logic calculates the phase-to-phase voltage threshold as:

$$V_{phase-phase} = \left|\left(a^2 - a\right)\cdot\left(V_1 - V_2\right)\right| = \frac{\sqrt{3}\cdot V_{nom}}{(SIR+1)} \qquad \text{Equation 3.22}$$

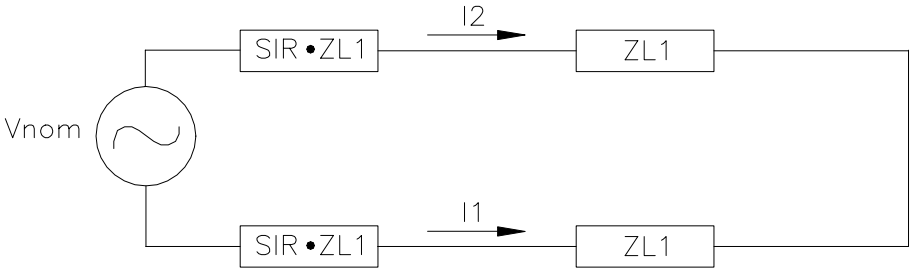


Figure 3.25: Sequence Network for a B-C Fault at Line End

High-Current Detection

A low-voltage condition is present for close-in faults and delays Zone 1 tripping because it is not, by itself, sufficient to declare a high SIR system condition. To prevent Zone 1 tripping delay for a low SIR application and/or for close-in faults, supervise the low-voltage elements with corresponding high-current elements.

The CVT transient detection logic calculates the current thresholds using the user-entered replica line impedance settings and a predetermined SIR radial line model with the assumed fault location at the end of the line. The calculated current thresholds are the phase-to-neutral and phase-to-phase current flow at the relay.

Using the sequence network shown in Figure 3.24 as a reference, the logic calculates the phase-to-neutral current threshold as follows:

$$I_{phase} = \left|I_0 + I_1 + I_2\right| = \left|\frac{3\cdot V_{nom}}{(SIR+1)\cdot(2\cdot Z_{L1} + Z_{L0})}\right| \qquad \text{Equation 3.23}$$

Using the sequence network shown in Figure 3.25 as a reference, the logic calculates the phase-to-phase current threshold as follows:

$$I_{phase-phase} = \left|(a^2 - a)\cdot(I_1 - I_2)\right| = \left|2\cdot\sqrt{3}\cdot I_1\right| = \left|\frac{\sqrt{3}\cdot V_{nom}}{(SIR+1)\cdot Z_{L1}}\right| \qquad \text{Equation 3.24}$$

The ratio of close-in to remote fault currents is (SIR + 1)/SIR. For a high SIR system, the fault current magnitudes do not differ greatly for different fault locations along the protected line section. Therefore, the high-current elements based on the thresholds calculated above do not override the undervoltage declaration for close-in faults on higher SIR systems. This means the distance element could be penalized with a delay for close-in faults. The logic we discuss next reduces this problem.

High SIR Time Delay and Distance Calculation Smoothness

As shown in Figure 3.23, with conditions of low voltage, low current, and the Zone 1 pickup, the CVT logic delays the Zone 1 element output. This delay is long enough to eliminate worst case CVT-transient-induced Zone 1 overreach.

For close-in faults on systems with high SIRs, use the distance-calculation smoothness detection to override the tripping delay caused by low voltage and low current.

The high SIR detection part (HSIR) of the CVT logic could assert for close-in faults on higher SIR systems, both low-voltage and low-current. This assertion is unavoidable on high SIR systems. However, there is a large difference in the distance calculation stabilization time for close-in faults and for remote faults. For remote faults, the distance calculation stabilizes by the time the CVT transient dies out. For close-in faults, the distance calculation stabilizes rather quickly, but the distance element operating speed is penalized by the CVT logic time delay. These observations show that detecting the distance calculation smoothness enables us to bypass the time delay introduced by the CVT detection logic and thereby decrease tripping time. This logic then minimizes the fault clearing time delay of close-in faults on higher SIR systems where low voltage and current cause the CVT detection logic to assert.

The threshold of distance smoothness detection is a function of distance calculation results, which is experimentally determined as $-a\cdot m+b$. This variable threshold allows us to tolerate more distance calculation fluctuations when a fault is close-in and fewer when the fault is remote. The distance calculation-dependent threshold gives us the ability to override the CVT tripping delay for close-in faults occurring on high SIR systems.

VT Magnitude and Angle Errors Create Standing Voltages

Table 3.5 and Table 3.4 show the standing V_{A2} and V_{A0} voltages for Class 1 and Class 2 VTs with a ratio error and an angle error from a single phase. The assumed ideal phase voltage magnitude is 66.4 V and all phase voltages are separated by 120°.

Table 3.5: Standing Sequence Voltages Present for VT Ratio Errors

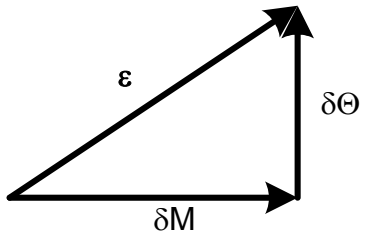
δM	δΘ	V_{A2}, $V_{A0, Stand}$
-2%	0	0.44 V ∠ 180°
-1%	0	0.22 V ∠ 180°
0%	0	0.00 V ∠ 0.00°
+1%	0	0.22 V ∠ 0.00°
+2%	0	0.44 V ∠ 0.00°

Table 3.6: Standing Voltages as a Result of VT Angle Errors

δM	δΘ	V_{A0}, $V_{A2, Stand}$
0	-1.33°	1.54 V ∠ -90°
0	-0.66°	0.76 V ∠ -90°
0	0.00°	0.00 V ∠ 0.00°
0	+0.66°	0.76 V ∠ +90°
0	+1.33°	1.54 V ∠ +90°

Each of the three VTs can have a plus or minus magnitude and/or a phase angle error. Any error produces a standing V_{A2} or V_{A0}, even on a perfectly balanced system. The magnitude and phase angle of this standing voltage depends on the individual VTs and possibly on their connected burdens. The standing voltage error has different effects on different faults, with different R_F on different phases.

Here is an easy way of looking at the errors shown in Tables 7 and 8. Calculate the error voltage **ε** that results from the ratio and phase angle errors using the equation shown in Figure 3.26.



$$\varepsilon = \sqrt{(\text{magnitudeerror})^2 + (\text{angleerror})^2}$$
$$= \sqrt{(\delta M)^2 + (\delta\Theta)^2}$$

Figure 3.26: ε is a Starting Point for Calculating RF Limitations Caused by VT Errors

For reliable operation for all fault types, the fault must generate V_{A2} or V_{A0} greater than two or three times that of **ε**. This ensures that the fault generated V_{A2} and V_{A0} overwhelms the standing voltages.

Calculate **ε** for the Class 1 VT using the data from Tables 7 and 8.

$$\varepsilon = \left(0.76\ V^2 + 0.22\ V^2\right)^{1/2} = 0.79\ V \qquad \text{Equation 3.25}$$

Standards

ANSI C57.13

Practices

????

BPD - Bushing Potential Devices

These devices use the dielectric of insulator bushings to provide high voltage capacitance.

NONCONVENTIONAL INSTRUMENTATION

Microprocessor-based relaying imposes very low burdens on voltage and current instrumentation. Microprocessor-based relays do not require the high current and high voltage instrumentation needed to operate electromechanical devices. If the burden range is restricted, improved accuracy is possible without increased cost. With lower burdens, new technologies can now be used for instrumentation with wider bandwidth than is needed for traveling wave-based relaying. Minkner and Schweitzer discuss many of these concepts in a 1999 WPRC paper. [25] These new technology instruments are also less susceptible to distortions during fault conditions.

Facilities employing both electromechanical and microprocessor-based technologies for metering and relaying are either confined to using the conventional instrumentation discussed above or to installing two sets of instrumentation.

4 FUNDAMENTALS OF PROTECTIVE RELAYING

Modern power system relays are electromechanical, electronic and/or computer-based devices that protect power system equipment and apparatus from abnormal currents and voltages. The two fundamental relay operations are to isolate faulted sections of the power system while maintaining the power delivery capability in the rest of the power system.

Relays can have numerous inputs on which to determine if a trip signal is required. Figure 4.1 illustrates the power instrumentation is provided by voltage transformers (PT) and current transformers (CT). DC power is needed to supply relay power as well as to provide trip coil power for the power circuit breaker. The 52 designation is the IEEE standard C37.2 device number for power circuit breakers (see Appendix11.9). Batteries normally provide dc power in the event that the station has lost all ac connections (see section 0). Other inputs can modify relay behavior to speed up or inhibit operations. Local control is normally bi-state logic while remote communications allows both multivalued data (digitized analog) as well as bi-level control (see section 00). Relay communications also allows remote control and event retrieval (see section 6.1).

This chapter focuses on the fundamentals of devices designed to provide power system protection.

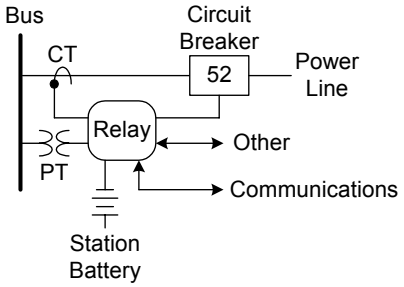


Figure 4.1: Single-Line Diagram of Relay Connection to Power System

HISTORY OF RELAYS

The term relay normally refers to the electronic or electromechanical device responsible for the processing portion of the relay system. In general terms, relays provide control to the breaker so that it has function similar to a fuse or residential circuit breaker. Residential circuit breakers and fuses both detect and interrupt fault current. This requires both relay and circuit breaker.

Initially, relays were electromechanical and used flux to produce torque that caused the breaker to open. Mason[26] derives a general torque equation shown in Equation 4.1 and proceeds to demonstrate how selecting the value and sign of constants K1 through K4 describes all fundamental relay operations. Positive torque results in forces that tend to close the trip contacts. Various forms of Equation 4.1 will be used to explain the fundamental operations of many types of protective relaying. Modern microprocessor-based relays still use many of the fundamental relationships derived from this expression.

$$T = K_1 I^2 + K_2 V^2 + K_3 V I \cos(\theta - \tau) + K_4 \qquad \text{Equation 4.1}$$

Many electromechanical relays are still being used by utilities, industrial, and commercial facilities today. They have limited capability and were packaged such that separate units, called elements, provided each control feature.

Transistors and integrated circuits replaced induction disk solid-state relays. Microprocessor relays, introduced in the early 1980s, have completely replaced both electromechanical and solid-state relays for new applications.

Terminology is relatively unchanged since relay engineers were already familiar with the terminology associated with electromechanical relays. Operate and restraint torque do not physically exist in microprocessor-based relays, but are derived mathematical quantities based on microprocessor code.

The purpose of the protective relay has remained consistent over the years: to efficiently and effectively deenergize faulted portions of the power system while causing minimum disruption to the remaining unfaulted sections. Relays provide the controls for automatically switching all aspects of the power system. Normally, the switching action is set to deenergize selected devices or portions of the power system.

Some automatic switching control provided by relays will reclose a breaker shortly after a trip in an attempt to quickly restore power to a circuit. Such reclosing operations are based on the experience that a high percentage of some types of faults are transitory and self-clearing after the line is deenergized. Relays have evolved to control, record, report, communicate, and in some cases, adapt to, events on the power system.

TYPES OF RELAYS

Relays are designed to protect every kind of apparatus and facility used in the generation, delivery, and consumption of electrical energy. Elements commonly protected by relay equipment are listed in Table 4.1. In a coordinated protected system, the effects on both the primary zone of protection and the adjacent zones must be carefully planned. In addition to the variables listed in Table 4.1, relays also monitor local and remote status contacts controlled by relays and switches.

Table 4.1: Protected Power Systems and Parameters Measured

		Parameters Measured						
		V	**I**	**F**	**ϕ**	**T**	**P**	**t**
Rotating Machinery	Generators	M	M	M	M	M		
	Motors	M	X			M		
	Synchronous Condensers	M	M	M	M	M		
Lines & Circuits	Transmission	M	M	D	D	M		M
	Distribution	M	M	D	D	M		
	Cable	M	M	D	D			M
	Series Capacitors	M	M			M		
	Shunt Reactor	M	M			M	M	
Station	Breaker Failure	M	M			M	M	
	Bus Fault	M	M			M		
	Transformer	M	M			M		
	Shunt Capacitor	M	M			M		
System Stability	Load Shedding	M	M	D	D			
	Load / Frequency Control	M	M	D	D			
	Reclosing	M	M	D	D			
	Sync Check	M	M	D	D			

Parameter symbol code:

V—Volts
I—Amps
F—Frequency
ϕ—Phase
T—Temperature
P—Pressure
M—Measured
D—Derived
t—Time

Relays that run autonomously or without local and remote supervision make trip/no-trip decisions based on local analog measurements and status contacts. Supervised relays are capable of autonomous operation but perform better when based on remote information using some means of communication. The supervision can block or permit trip operations or provide status. Supervised relays can perform faster and more securely, but are also more likely to fail.

Protecting Lines and Circuits

The three most common types of line relaying are overcurrent, impedance, and phase comparison, which includes pilot wire relaying. Another type, based on traveling wave theory, is less common. Derive the frequency and phase relationship between voltage and current for the relay algorithm from the measurements of voltage and current (see Table 4.1).

For dependable and secure functionality, the relay must be able to determine the direction and relative distance to the fault. From the relay perspective, fault direction is forward if the fault occurs in or beyond the zone of protection, as illustrated in Figure 1.3. Sometimes the direction is implied, such as with single source radial feed networks. Section 0 discusses various methods of deriving direction. Distance is an abstraction of the impedance between the point or relay instrumentation and the fault. It is only possible to measure physical distance to the fault if a relationship of ohms per mile is identified. For additional information on fault locating see 4.3.3. Determine distance from current measurements by assuming the source voltage is constant. More accurate measures of distance require voltage measurements and knowledge of line impedance (see line constants parameter program).

Relays frequently address phase-to-phase or simply phase faults separately from phase-to-ground faults (also called ground faults). This is because the detection algorithms are separate in order to tune or maximize the relay to the particular type of fault.

Overcurrent Relays

Instantaneous Overcurrent Relays (ANSI Type 50)

Model overcurrent relays similarly to overvoltage relays, using a modified form of Mason's general torque equation as described by Equation 4.2. The relay requires positive torque to operate. Negative K4 provides constant restraining. Solving to the balance point (zero torque) determines the trip current, also commonly called pickup current, as shown in Equation 4.3.

$$T = K_1 I^2 - K_4 \qquad \text{Equation 4.2}$$

$$I_{PU} = \sqrt{\frac{K_4}{K_1}} \text{, a constant} \qquad \text{Equation 4.3}$$

The induction disk electromechanical relay produces torque in a moveable disk similar to the disk in a residential electrical meter. Consider the case when two time-varying fluxes of the same frequency but different phase, θ, as expressed in Equation 4.4 and Equation 4.5 are imposed on a disk as shown in Figure 4.2.

$$\phi 1 = \Phi 1_M \sin(\omega t) \qquad \text{Equation 4.4}$$

$$\phi 2 = \Phi 2_M \sin(\omega t + \theta) \qquad \text{Equation 4.5}$$

At the instant when both fluxes are directed downward and are increasing in magnitude, each flux induces voltage around itself in the rotor, and currents flow in the rotor under the influence of the two voltages. The current produced by one flux reacts with the other flux, and vice versa, to produce forces that act on the disk. Assuming that the disk currents produce insignificant self-inductance, currents $i_{\phi 1}$ and $i_{\phi 2}$ are in phase with their voltages, resulting in Equation 4.6 and Equation 4.7. This produces two mechanical forces opposite in direction so the net force is the difference shown in Equation 4.8.

$$i_{\phi 1} \propto \frac{d\phi 1}{dt} \propto \Phi 1_M \cos(\omega t) \qquad \text{Equation 4.6}$$

$$i_{\phi 2} \propto \frac{d\phi 2}{dt} \propto \Phi 2_M \cos(\omega t + \theta) \qquad \text{Equation 4.7}$$

$$F = F2 - F1 \propto \left(\phi 2 \cdot i_{\phi 1} - \phi 1 \cdot i_{\phi 2} \right) \qquad \text{Equation 4.8}$$

Substituting the quantities of Equation 4.6 through Equation 4.7 into Equation 4.8 results in the net force. The result is Equation 4.9, which reduces down to Equation 4.10, which shows the force is proportional to the magnitude of the product of the two fluxes and the phase difference between them.

$$F \propto \Phi 1_M \Phi 2_M \left[\sin(\omega t + \theta)\cos(\omega t) - \cos(\omega t + \theta)\sin(\omega t) \right] \qquad \text{Equation 4.9}$$

$$F \propto \Phi 1_M \Phi 2_M \sin(\theta) \qquad \text{Equation 4.10}$$

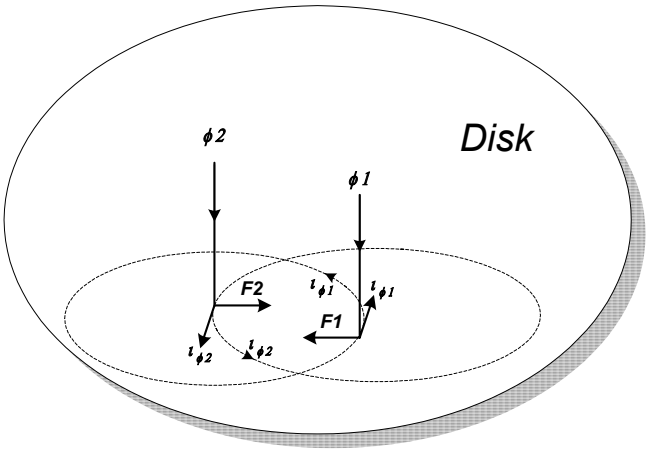


Figure 4.2: Induced Currents and Forces Resulting From Two Flux Paths on a Metallic Disk

Figure 4.3 shows the basis of both the residential electric meter and the induction disk relay. The pole shading forces a phase shift in the flux, θ, that produces the force in Equation 4.10. Since torque is a force times a distance and since the applied current produces identical flux for Φ1 and Φ2, Equation 4.10 can be expressed as Equation 4.2 where K_1 accounts for all the proportionality.

To complete the comparison of the induction disk relay to the residential electric meter, meter the power assuming a constant voltage and no restraining spring. This makes K_4 zero in Equation 4.2. The meter is free to rotate at a speed proportional to the square of the load current. A counter simply measures the number of disk rotations and applies a kWh conversion per disk revolution.

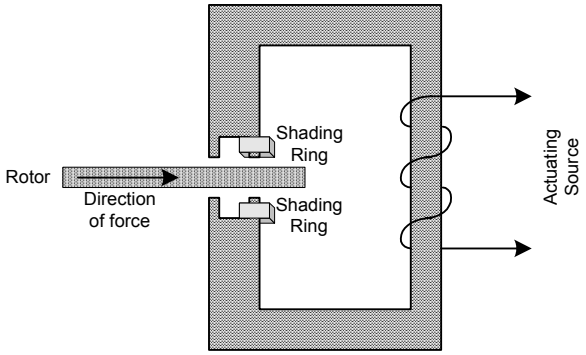


Figure 4.3: Shaded-Pole Induction Disk

Time-Overcurrent Relays (ANSI Type 51)

The overcurrent relay more or less approximates the operation of the thermal fuse. This similarity is a design characteristic of time-overcurrent relays to accomodate systems that integrate fuse protection with electromechanical, electronic, and microprocessor-based relays. For time-overcurrent relays, the magnitude of the applied or operating current determines the time to operate. Electromechanical devices had a disk that looked much like the ones in a conventional residential power meter. Figure 4.4 illustrates some of the mechanical components of the induction disk overcurrent relay.

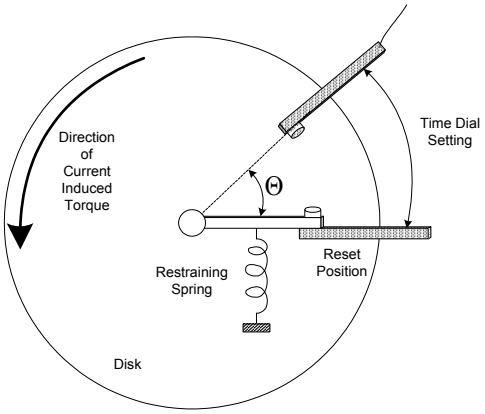


Figure 4.4: Diagram of Induction Disk Relay

A restraining spring forces the disk to rotate in the direction that opens the trip contacts while current creates operating torque to close the contacts. The net torque equation is expressed by Equation 4.1, where positive torque closes the contacts. The I_{PU} relay setting fixes the value of the pickup current. When the current applied to the relay equals the pickup current, the contact closing torque just equals the restraining torque and the disk will not move regardless of its position. If the applied current increases above the pickup current, the disk will begin to rotate so that the trip contacts come closer together. If the operating torque equals the restraining torque then the net torque inEquation 4.2 is zero. This allows us to solve the torque balance equation shown in Equation 4.11.[27]

Integrating Equation 4.12 with respect to time, Equation 4.13 shows that the rotation angle depends on the magnitude of the current and the time that the current is applied. The trip contacts, positioned with an adjustment called the time dial setting (TDS), determine how far the disk must rotate to close the contacts. The TDS units vary continuously from zero to a value typically greater than 10. The relationship of TDS to the time to operate is such that increasing the TDS setting by a number increases the time to trip by that same amount. For example, changing the time dial setting three to nine makes the time to operate three times longer.

Damping magnets and coils impedes the speed of rotation. Referencing the initial disk position to the reset location, and t_0 to when the ratio of I_{PU}/I is greater than unity, the trip time is the time required to rotate the disk through the angle determined by TDS as shown in Equation 4.14 and Equation 4.15.

$$T = \tau_s \left(\left(\frac{I}{I_p} \right)^2 - 1 \right) - K_d \left(\frac{\partial \theta}{\partial t} \right) \qquad \text{Equation 4.11}$$

$$\tau_s \left(\left(\frac{I}{I_p} \right)^2 - 1 \right) = K_d \left(\frac{\partial \theta}{\partial t} \right) \qquad \text{Equation 4.12}$$

where:

τs is the restraining spring torque

I is the applied current

IPU is the pickup current that is established by the zero torque from Equation 4.3

Kd is disk damping factor due to magnetic drag

θ is the disk rotation angle $\propto$ TDS

$$\theta_2 - \theta_1 = \frac{\tau_s}{K_d} \left(\left(\frac{I}{I_p} \right)^2 - 1 \right) (t_2 - t_1) \qquad \text{Equation 4.13}$$

$$TDS = \frac{\tau_s}{K_d} \left(\left(\frac{I}{I_p} \right)^2 - 1 \right) (\text{trip time}) \qquad \text{Equation 4.14}$$

$$(\text{trip time}) = TDS \frac{\frac{K_d}{\tau_s}}{\left(\left(\frac{I}{I_p} \right)^2 - 1 \right)} = TDS \frac{A}{(M^2 - 1)} \qquad \text{Equation 4.15}$$

where:

M is the multiples of pickup current = I/IPU and A = Kd/τs.

Equation 4.15demonstrates that three parameters determine the operating characteristics of the time-overcurrent relay, namely the pickup current, $I_{PU,}$ the time

dial setting, TDS, and the degree of inverseness. For the development shown in Equation 4.13 through Equation 4.15, the constant, *A,* and the power of *M* in Equation 4.15 establish the degree of inverseness. In practice, there are actually three parameters that determine the degree of inverseness. Equation 4.16 and Equation 4.17 show the form usually used to describe time-overcurrent relay operations. Equation 4.16 represents the reset time and Equation 4.17 the time to trip. This tripping time is only valid if the relay is the reset condition. Similarly, Equation 4.16 is accurate only if the relay starts when the time-overcurrent function has timed out.

Some sources claim that Equation 4.17 include disk inertia by using the parameter B. The result is that relay manufacturers design relays with particular characteristics using various factors for *A*, *B*, and *p*.[28] Although it is not required, most manufacturers facilitate relay coordination (discussed in section 0) by using the standard values shown in Table 4.2 for inverse characteristics. Figure 4.5 illustrates the family of curves for very inverse characteristics and a time dial setting of one through ten. This set of curves demonstrates that the time to operate is linearly dependent on the time dial setting for a given characteristic and multiple of pickup current. A complete set of I.E.C. and U.S. standard curves based on the IEEE standard C37.112-1996 can be found in appendix section 11.1.

$$\mathrm{tr} = \mathrm{TDS}\left(\frac{\mathrm{C}}{1-\mathrm{M}^2}\right) \qquad \text{Equation 4.16}$$

$$\mathrm{tt} = \mathrm{TDS}\left(\frac{\mathrm{A}}{\mathrm{M}^{\mathrm{p}}-1}+\mathrm{B}\right) \text{ for } \mathrm{M} \geq 1. \qquad \text{Equation 4.17}$$

Table 4.2: Degrees of Inverseness as a Function of A, B and p for U.S. and I.E.C Standard Curves

Curve	A	B	C	P
U.S. Moderately inverse (U1)	0.0104	0.2256	1.08	0.02
U.S. Inverse (U2)	5.95	0.180	5.95	2.00
U.S. Very inverse (U3)	3.88	0.0963	3.88	2.00
U.S. Extremely inverse (U4)	5.67	0352	5.67	2.00
U.S. Short-time inverse (U5)	0.00342	0.00262	0.323	0.02
I.E.C. Class A—Standard inverse (C1)	0.14	0.0	13.5	0.02
I.E.C. Class B—Very inverse (C2)	13.5	0.0	47.3	2.00
I.E.C. Class C—Extremely inverse (C3)	80.0	0.0	80.0	2.00
I.E.C Long-time inverse (C4)	120.0	0.0	120.0	2.00
I.E.C Short-time inverse (C5)	0.05	0.0	4.85	0.04

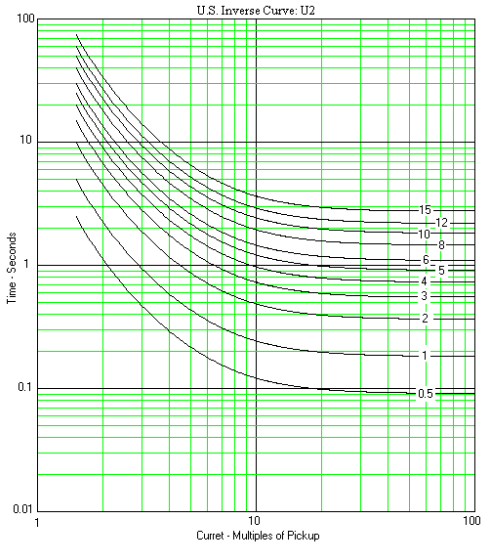


Figure 4.5: Family of Curves for U.S. Inverse U2 Characteristics

Benmouyal and Zocholl discuss time-current coordination in systems that use both thermal fuses and time-overcurrent relays.[27] The basic concept is that the higher the current, the faster the relay or fuse operates. Figure 4.6, reproduced from this reference, illustrates how the 50E fuse time-current characteristics compare with the extremely inverse relay characteristics. The shapes of these curves are well defined in IEEE standard C37.90. Fuses are generally used to clear specific loads or sections of a distribution system and are located on poles and in service entrances. Thermal fuses are rather inexpensive, but are destroyed in the process of clearing the fault. A worker must replace the fuse before service can be restored.

Breakers and other interrupting mechanisms are more expensive than fuses and are usually installed at the substation. As the cost of breakers declines, the trend is to replace fuses with relays and interrupters. Time-overcurrent relays discriminate faults by current magnitude and use time to coordinate operations in different zones. So the closer the fault, the faster the relay will operate. Faults farther away have higher impedance between the source and the fault, resulting in lower fault current and therefore longer operating times. For radial lines (lines with only one source) and with downstream fuses, the additional time allows the fuses to operate first. Relay-fuse coordination is important to minimize the extent that clearing the fault will deenergize the power network.

Figure 4.7 compares the time to operate as a function of multiples of pickup current for three different inverse characteristics. Equation 4.16 and Equation 4.17, together with Figure 4.5 and Figure 4.7, lead to several observations. One is that the time to operate is roughly inversely proportional to the inverse of the square of the current, making it responsive to energy. Another is that after 20 multiples of pickup current, the time to operate is nearly independent of current.

Fuses are nondirectional single-phase devices and should not be used where the loss of one phase could damage equipment. Since fuses are generally sized for load, increase the fuse rating, and in some cases, the hardware, if adding load. Figure 4.6 shows a shaded area between the minimum melting time and the maximum melting

time. Fuses have unpredictable performance whenever currents are in this region whether or not the fuse opens. Fuse coordination with upstream relays requires that the relays not operate faster than the maximum melting time in addition to time for fuse tolerance variations. The difference between the relay and fuse operating times for a specified fault current is the coordination time interval (CTI).

A repeated high surge of high current for which the fuse does not operate still causes the fuse to heat up. Coordination is useless without sufficient time to cool between applications of high current.

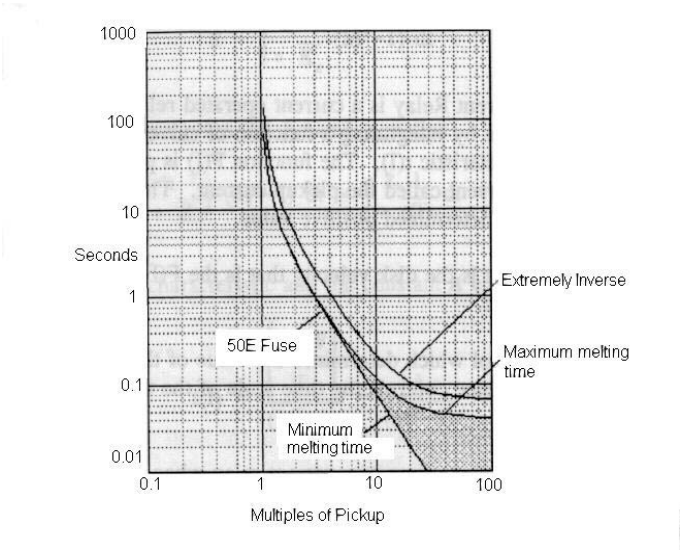


Figure 4.6: Extremely Inverse Relay Characteristics Compared With Minimum and Maximum Clearing Times of a 50E Fuse

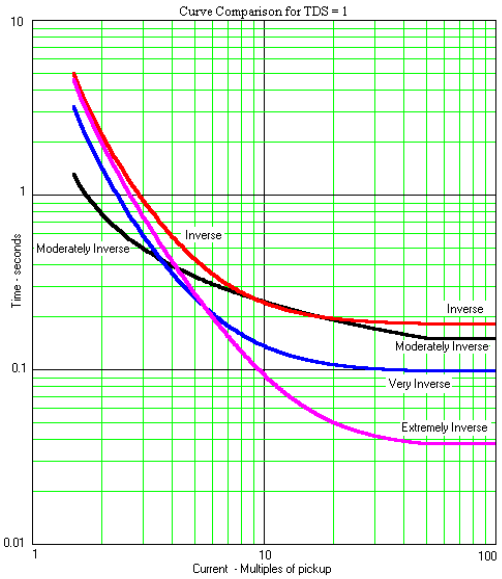


Figure 4.7: Comparison of Inverse Characteristics for Modified Inverse, Very Inverse, and Extremely Inverse Characteristics

As previously stated, time delay with relays allows coordination between other time overcurrent relays as well as fuses.[29] Consider a faulted single feed system as illustrated in Figure 4.8. The relay on the faulted line, R4, should be the only relay to trip. Equation 4.18 determines the maximum three-phase fault current that can be expected for a fault beyond bus #3 and, if the longest line leaving Bus #3 has impedance Z4, Equation 4.19 expresses the minimum fault current. Similar expressions developed for each line segment show that the closer the segment is to the source, the more the expected current for a fault on a particular segment increases. Achieve coordination by increasing the time dial settings while proceeding toward the source. If relay R2 should provide backup protection for relay R4, then set R4, the relay with the greatest source impedance, with the lowest time dial setting. Section 0 discusses relay coordination and coordination for distribution protection in more detail. Relay-relay and relay-fuse coordination should never be attempted for fault currents under1.5 times for pickup current because errors are greatly magnified and performance is not repeatable. Set the pickup above load but sensitive enough to see faults up to the next protection device. If I_{MIN} is defined as the minimum fault current, then set the pickup current at least as low as the current but above maximum load current. For relays R2 and R3, set the TDS to trip no faster then the next downstream device when the fault current is maximum for an out of zone fault. For example, if current, $I4_{MAX,}$ results from a fault is immediately downstream of R4, then set the TDS for relay R3 slower than that of R4 when the R3 current is $I4_{MAX,}$ plus the maximum expected load current at Bus #3.

$$I_f 3_{MAX} = Vs \big/ (Z1 + Z2 + Z3) \qquad \text{Equation 4.18}$$

$$I_f 3_{MIN} = Vs \big/ (Z1 + Z2 + Z3 + Z4) \qquad \text{Equation 4.19}$$

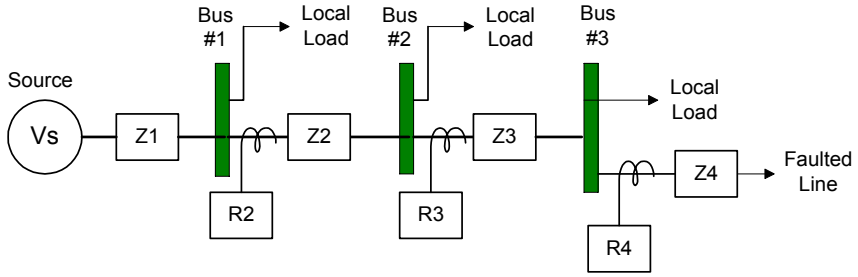


Figure 4.8: Single-End-Feed Power Network

Time-overcurrent relay dynamics [30,39]

The previous discussion on the trip times for time-overcurrent relays assumes that the line current is constant for the duration of the fault. Historically, coordination studies make that same assumption. To assume otherwise requires engineering tools capable of including the transitory dynamics and a means of predicting the sequence and magnitude of the dynamics. First ignore the transient dynamics and determine the fault current magnitude and phase with a single solution using Ohm's law to solve one or a set of simultaneous equations with complex variables. The computations are always made after the system is at steady state.

Since the 1960s, digital computers have analyzed power systems using time domain solution techniques, generically called EMTP or electromagnetic transient programs. Figure 4.10 and Figure 4.12, discussed below, show the results of such simulations. Time domain solutions use difference equations with algorithms that approximate numerical integration and differentiation. Equation 4.20 shows a mathematical relay model that can be rewritten as shown in Equation 4.20 and subsequently modified into a difference equation as shown in Equation 4.21 and uses the same definitions for A, B and p that are used in Equation 4.17.

$$\theta_2 = \frac{\tau_s}{K_d}\left(\left(\frac{I}{I_p}\right)^p - 1\right)(t_2 - t_1) + \theta_1 \qquad \text{Equation 4.20}$$

$$\theta_n = \left(\frac{1}{TDS}\right)\left(\frac{M_n{}^p - 1}{B\left(M_n{}^p - 1\right) + A}\right)T + \theta_{n-1} \qquad \text{Equation 4.21}$$

Where $M_n = I_n/Ip$ and I_n is the magnitude of most recent current sample

The single line diagram in Figure 4.9 represents a simulation of a 250Ω resistive fault initiated at 8.3 ms that progresses to a 25Ω fault at 62 ms. A tree branch coming in contact with the wire could cause this type of fault. The power system to the left of the 230 kV-transmission line is a lumped parameter Thevinen equivalent impedance and source. The two time-overcurrent (52) relays in this system are modeled identically except that the time dial setting is 2.4 for the S bus relay and 1.0 for the R bus relay.

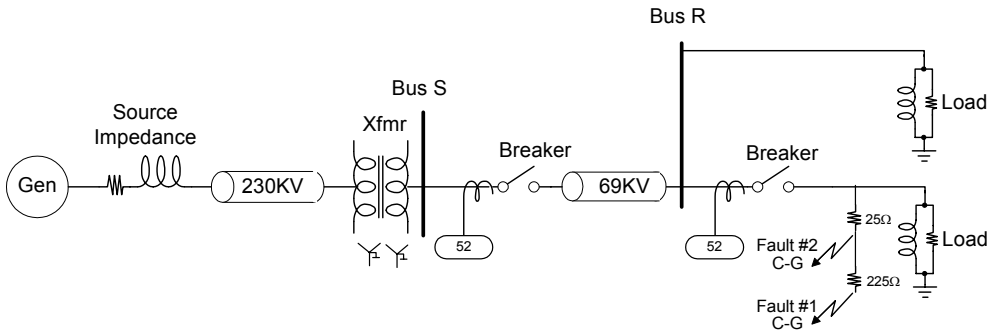


Figure 4.9: Single-Line Diagram of Simulated Faulted Power System With TOC Relays

Figure 4.10 simulates the response of an electromechanical type 52 relay at location Bus R to a phase-C-to-ground fault starting at the time of the initial 250Ω fault. The bus R phase current curve on this graph is the time domain phase-C current. The current magnitude algorithm computes the peak value of the phase domain current. The disk position curve is scaled so that 100 corresponds to the reset position and zero to the trip position.

The bus R phase current in Figure 4.10 shows that the current waveform is significantly offset immediately after the fault is initiated. The algorithm that computes the magnitude determines the transient response of the current magnitude to the step increase (see section0). Although the current is almost fully offset, the

relay response verifies that the computer algorithm filters out the offset component. The change of slope after the second fault is initiated is in response to the higher fault current that causes the disk to rotate faster. The steeper slope of the disk position line indicates this. Approximately 115 ms into the simulation, the contacts are trip closed but the line current continues to flow. The breaker-operate time for this simulation is 40 ms and the current will stop only at a current zero crossing. After the breaker opens, the response of the algorithm to the step change in current causes a transient response in the current magnitude.

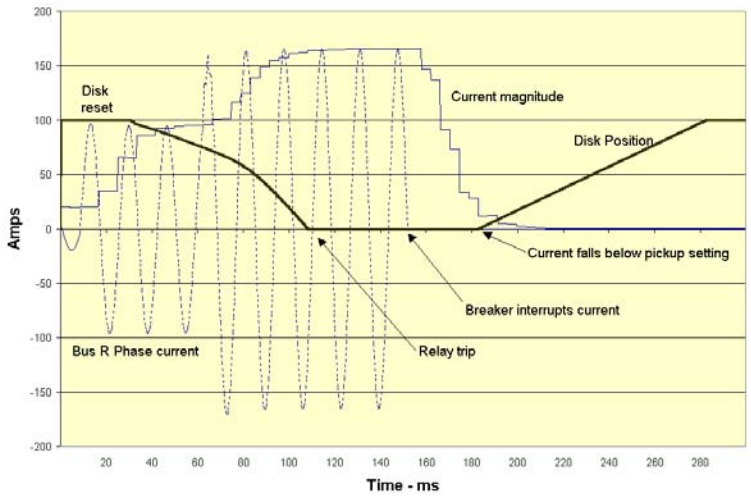


Figure 4.10: EMTP Simulation of a Faulted Power System and Operation of a Time-Overcurrent Relay With Trip Output

The relay begins to reset once the relay current is below the pickup value. The restraint spring torque and the time dial setting fixes the reset time for electromechanical relays. Slow reset time can cause coordination problems, called ratcheting, during reclose operations. If a reclose operation occurs before the fault clears and the relay is fully reset, then the time to trip is not predictable. Microprocessor relays are able to use very short reset times.

Figure 4.11 shows the Bus S relay response to the same fault. The plotted disk position for both relays demonstrates the effect of the TDS. Since TDS for the relay at Bus S is three times that of the relay at Bus R, we set the reset value three times higher. Because this relay did not trip, the additional load at Bus R causes line current to continue flowing after the Bus R switch opens. This example does not clearly show the differences in slope of the disk position that indicate the speed of the relay disk even though the current at Bus S includes the load.

The simulation also shows the disk on the Bus S relay as continuing to rotate after relay Bus R has already made the trip decision at 115 ms. In fact, the simulation shows that the rotation of this relay did not reverse until almost 190 ms. For this example, the breaker-operate time, set to 40 ms, is the biggest contributor to the persistence of fault current processed by the Bus S relay. Even though the fault current is interrupted at about 160 ms, the disk continues to rotate in a trip direction. Both electromechanical and microprocessor relays have this problem, although the causes are different. In electromechanical relays the cause is disk inertia; in microprocessor relays it is algorithm transient response (see section 0).

Figure 4.11 and Figure 4.12 demonstrate the importance of coordinating relay operating times. As relay performance and breaker-operate time become shorter and more predictable, the tendency is to reduce CTI to speed the clearing of faults near the remote terminal. The problem with using short CTI times is that maximum loads must be predictable or the fault current, in addition to load, may cause the relay at Bus S to operate even though the fault has already been cleared.

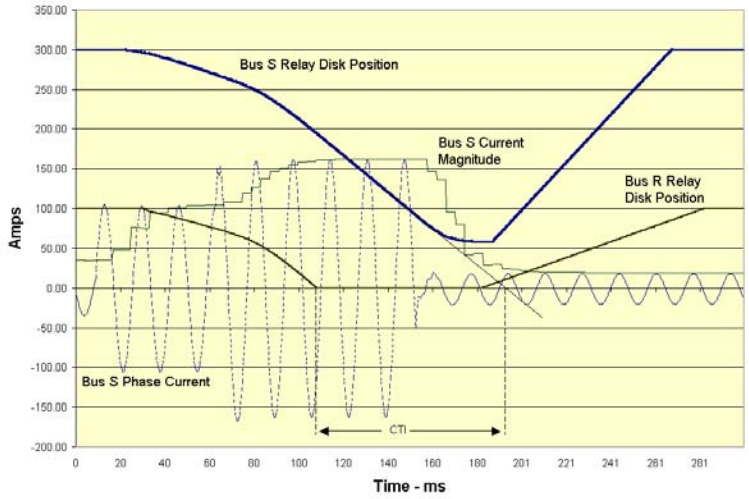


Figure 4.11: 52 Relay Operation at Bus S for Light Load at Bus R

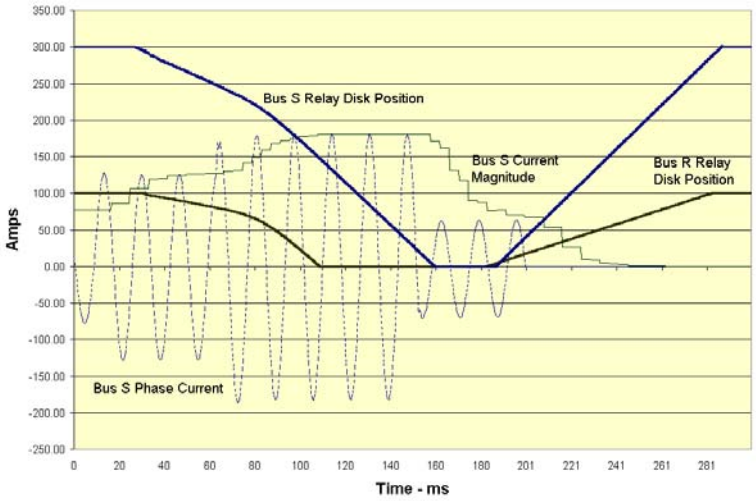


Figure 4.12: 52 Relay Operation at Bus S for Heavy Load at Bus R

Zero-Sequence Overcurrent Protection

To obtain sensitive ground fault detection, use a relay that responds only to the zero-sequence current of the system. A zero-sequence overcurrent relay simply measures the sum of the three phase currents, as shown in Equation 4.22. Unbalanced faults involving ground, such as phase-to-ground or phase-to-phase-to-ground faults, cause zero-sequence current, also referred to as ground or residual current. CT connection

configurations and the neutral current of a delta-grounded wye transformer are additional sources of zero sequence current (see section 0). Set zero-sequence overcurrent elements at very sensitive levels (i.e., a low pickup setting) because the zero-sequence current generated under load conditions is typically small compared to load currents.

$$Ir = Ia + Ib + Ic \qquad \text{Equation 4.22}$$

A common misconception is that zero-sequence current only exists under fault conditions. However, zero-sequence current can and does exist under no-fault, normal load conditions. Unbalanced system conditions, such as those caused by nontransposed transmission lines or unbalanced loading, can cause zero-sequence current to flow. ***Never set ground fault protection elements to be more sensitive than the normal system unbalance***. Doing so results in unintentional relay operations. This setting limitation means that load or system induced zero-sequence current can severely impact the sensitivity of a zero-sequence overcurrent element.[31]

Fault studies make zero-sequence fault quantities readily available. It is also very simple to determine pickup thresholds from fault study data. Because the majority of fault studies today also model intercircuit zero-sequence mutual coupling, zero-sequence currents from these studies already account for these effects.

Zero-sequence overcurrent elements can provide very effective resistive ground fault coverage, either independently with time delays or in pilot tripping schemes. Sensitive zero-sequence overcurrent elements in pilot tripping schemes provide the best, high-speed, resistive fault coverage.

Advantages Of Zero-Sequence Overcurrent Elements

Compared to using phase elements for ground protection, zero sequence overcurrent elements:

- Provide outstanding resistive fault coverage
- Are easy to set, understand, and visualize
- Are not affected by load flow for balanced lines and loads
- Are not affected by phase-to-phase or delta-connected load (i.e., delta-wye transformers)

Complications Of Zero-Sequence Overcurrent Elements

Zero-sequence overcurrent elements are affected by:

- Changes in the power system source
- Zero-sequence mutual coupling
- Normal system load unbalance
- In-line switching and open-phase conductors, which can have a negative impact on the security of a pilot scheme

Negative-Sequence Overcurrent Protection

Negative-sequence overcurrent elements have been gaining popularity as a method for detecting high-resistance ground faults. In the past, protection schemes using negative-sequence current elements were difficult to implement and complex in design. Many relays now offer negative-sequence current elements as a standard feature. Some utilities are using negative-sequence overcurrent elements to improve the sensitivity of their protection schemes.

Negative-sequence currents can arise whenever any system unbalance is present. Faults, nontransposed lines, and load unbalance are major sources of system unbalances. As with zero-sequence overcurrent elements, system unbalances can significantly impact the settable sensitivity of a negative-sequence overcurrent element.

Equation 4.23 gives the negative-sequence current, which is derived from the three phase currents. The negative-sequence current depends on phase rotation. Equation 4.23 assumes an ABC phase rotation. For an ACB phase rotation, the I_B and I_C terms are transposed.

$$I2 = \left(Ia + a^2 \cdot Ib + a \cdot Ic\right)/3 \quad \text{where } a = 1\angle 120° \text{ and } a^2 = 1\angle 240° \qquad \text{Equation 4.23}$$

For faults at the remote ends of long lines, negative-sequence current elements provide better resistive fault coverage than zero-sequence current elements because they are not affected by intercircuit mutual coupling. The negative-sequence impedance of a transmission line is significantly less than the zero-sequence impedance. Faults at the remote end of a long line typically have more negative-sequence current than zero-sequence current, depending on fault location and network configuration. Immunity to mutually coupled currents is equally important for distribution lines built under transmission lines.

Advantages Of Negative-Sequence Overcurrent Elements

Compared to using phase elements for ground protection, zero sequence overcurrent elements:

- Outstanding resistive fault coverage
- Better resistive fault coverage than zero-sequence overcurrent elements for faults at the end of long lines (for some line configurations)
- Insensitive to zero-sequence mutual coupling associated with parallel transmission line applications
- Not affected by load flow because the load current has very little impact on the negative-sequence current magnitude
- Preferred over zero-sequence overcurrent elements for wye-connected loads

Complications Of Negative-Sequence Overcurrent Elements

- Affected by changes in the power system source
- Affected by normal system load unbalance

- Affected by in-line switching and open-phase conductors, which can have a negative impact on the security of the pilot scheme
- Required to coordinate with phase and ground fault detecting elements

Directional Control of Negative- and Zero-Sequence Overcurrent Elements

The previous discussion on zero- and negative-sequence overcurrent elements only considered the operating or tripping quantities. These elements must be supervised by directional elements when used on multisource systems. In this text, directional control means that the input to the computing algorithm is enabled or disabled by the direction element as Figure 4.13 illustrates. The directional overcurrent relay can be a type 50 instantaneous element controlled by a type 32 directional, as illustrated in Figure 4.13b.

Using directional control eliminates a race condition that tends to cause relays to trip incorrectly. The following example illustrates the race condition for directional supervision. Consider the two-source system shown in Figure 4.14 that has a fault close to Bus R. If source Er is weak, then the contacts of the relay on Line #1 at Bus R may be closed when breaker 4 opens. The directional supervision contact inhibits that relay from tripping breaker 2. After breaker 4 opens, current from Er causes the current direction to change because fault current is now from Bus R via Bus S. If the dropout of the overcurrent element is slower than the pickup of the directional element, breaker 2 will trip. [34]

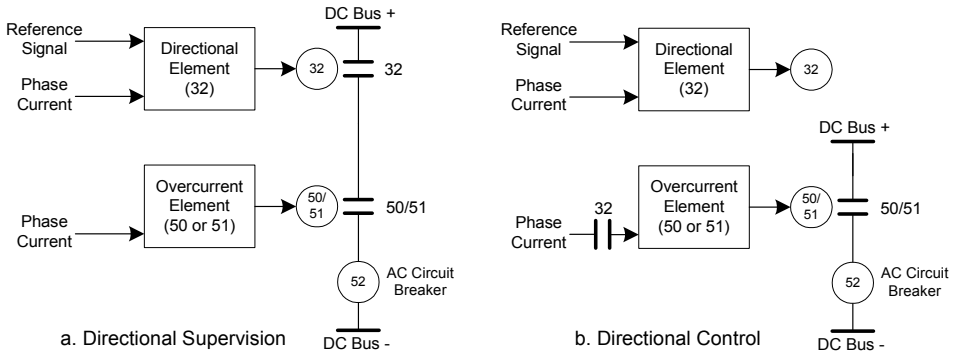


Figure 4.13: Circuits Showing the Difference Between a. Directional Supervision and b. Directional Control

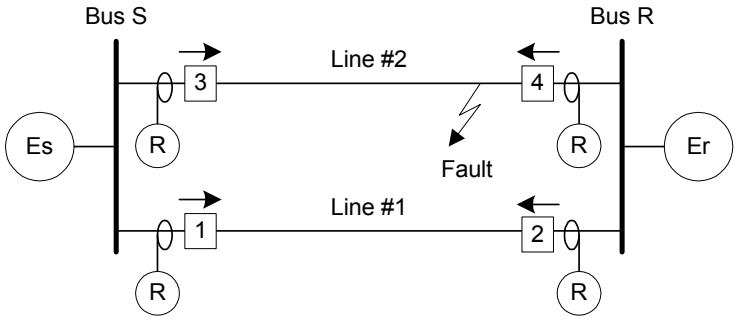


Figure 4.14: A Case for Directional Control

There are several methods for determining the correct direction of ground fault current. Zero-sequence voltage and current reference quantities are the most common. Negative-sequence voltage is also used for directional polarization. Section 0 discusses these methods in detail.

Directional Stepped-Time Overcurrent (ANSI Type 67)

If the type 67 relay element is to provide backup protection, use definite time delay for downstream coordination. The 67 element requires more attention to detail for coordination than type 51 relays. Figure 4.15 compares the stepped-time delay characteristics to the 51 relay continuous time delay characteristics. The advantage that the stepped-time has over the 51 is that the time steps are independently set. The disadvantage is that overreach errors have a more pronounced effect that often proves difficult to coordinate.

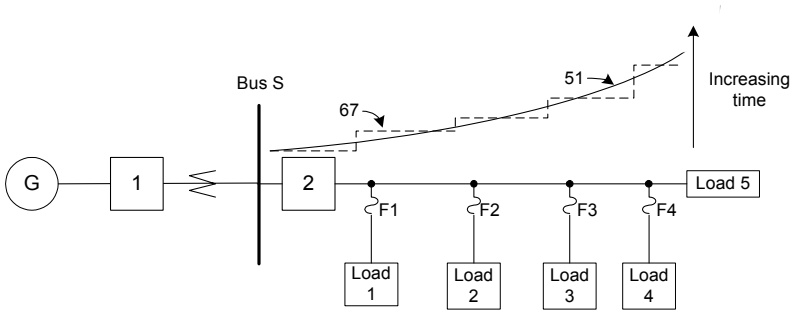


Figure 4.15: Comparison of Stepped-Time (67) and I^2t (51) Time-Overcurrent Relaying

Instantaneous Overvoltage relays

Overvoltage conditions can harm equipment by breaking down insulation, leading to a low-impedance fault to ground or to another circuit. Transient overvoltages are generally more severe than steady-state overvoltage conditions and rarely persist for more than a few cycles. Switching operations, faults, and lightning can cause transients. Surge or lightning arresters can limit the voltage at equipment terminals. The energy that can be dissipated by surge and lightning arresters is limited, but should be designed to exceed the energy in a potential transient. If not, the arresters will be damaged or destroyed leaving the circuit without further protection.

Arresters operate by flashing or generating a momentary low-impedance path to ground. As Figure 4.16 illustrates, the circuit inductance limits the instantaneous current. If the circuit impedance between the source of the voltage transient and the arrester is too small, then the arrester may fail if the current exceeds arrester capability. Such would be the case if lightning were to directly strike the terminals of a transformer. The resistance, inductance, and capacitance shown in Figure 4.16 represent the line, bus, or conductor model and not any actual equipment or device, although those can also be added to the analysis.

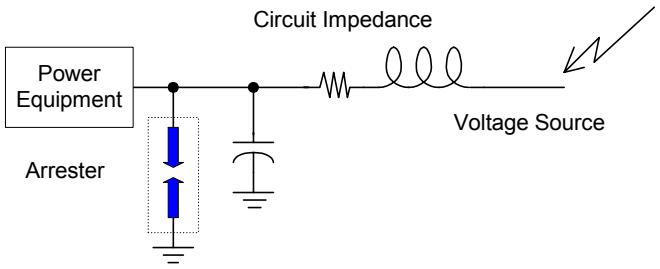


Figure 4.16: Arrester Circuit for Transient Suppression

Spark gap arresters and metal oxide arresters are two primary types of devices for transient overvoltage protection. Protective spark gaps are crude protection devices consisting of air gaps between electrodes of various shapes. The physical distance separating the line electrodes and ground points sets the flash-over voltage. Environmental conditions such as humidity, airborne dust, and contamination can affect the accuracy of this setting. The voltage across spark gap arresters drops to almost zero when flashed over. The circuit must be deenergized for a number of 60 Hz cycles to extinguish the arc across the arrester that sustains the low-impedance path to ground. Since the arc across the gap constitutes a line-to-ground fault, some type of overcurrent protection usually deenergizes the line.

The operating characteristics of arresters are similar to a reversed biased zener diode. Little or no current flows through the device until the voltage across the device terminals exceeds the sparkover voltage. Then current increases nonlinearly while voltage remains constant. The advantage of metal oxide arresters over spark gaps is that the line does not need to be deenergized to reset the transient protection.

Incorrect operations or anomalies such as subsynchronous resonance cause steady-state overvoltages. The duration of these events would soon destroy transient protection devices if they operated. Equation 4.24 expresses the modified version of Mason's generalized torque equation for a spring-restrained electromechanical overvoltage relay. Equation 4.25 is the solution of Equation 4.24 for the balance or zero torque condition. The solution shows that if the voltage is greater than a threshold equal to √K4/K2, then sufficient torque is produced to overcome the restraining spring and close the contacts.

$$T = K_2 V^2 - K_4 \qquad \text{Equation 4.24}$$

$$V = \sqrt{\frac{K_4}{K_2}} \text{ a constant} \qquad \text{Equation 4.25}$$

Direction (ANSI Type 32)

Sections 0 and 0 introduce the concept of direction without discussing how direction is determined. The sections that follow discuss various polarizing signals. These signals provide a dependable phase reference that is compared to the operate quantity affected by the fault to determine direction. The amplitude of the polarizing reference is not critical as long as there is enough magnitude to reliably determine the phase angle.

Fault direction relative to the relay instrumentation is either forward or reverse. Without direction control, relays will overreach, tripping incorrectly and unnecessarily deenergizing parts of the power system. The results of this type of incorrect operation can range from nothing at all to a significant loss of revenue caused by regional blackouts. The cost of incorrect operation depends on the generation, load, and system configuration at the time of interruption.

As section 4.2.8 shows, the arrival time of the fault signature determines direction in traveling wave relays. For conventional 60 Hz signal-monitoring relays, the phase angle relationship of the polarizing and operating quantities that are typically voltages and currents determines direction. Determining direction requires a phase reference that is independent of load and fault type.

Radial systems do not require direction supervision on protective relays because fault current can only be supplied for one direction. Hence relays are set to look toward the load. Systems with multiple sources have relays that look at the same zone of protection from both directions. Figure 4.17 shows a single-line diagram for such a system.

Directional elements have a sensitivity limit to guarantee sufficient voltage and current amplitude to reliably determine the direction of current flow. As section 0 shows, the directional element controls the input to the detection element. This requires that the 32 element be set to be slightly more sensitive than the detection element. For ground relaying, the sensitivity of the 32 should be set above the expected maximum load. Setting the sensitivity above load is desirable for phase relays, as well, but not always possible. If the 32 element is used to detect faults behind Zone 3, the relay for pilot relay schemes (see 4.1.2), then the sensitivity of the Zone 2 for the remote relay should always be less than the sensitivity of the local Zone 3. Failure to follow this rule will result in misoperations at the remote terminal.

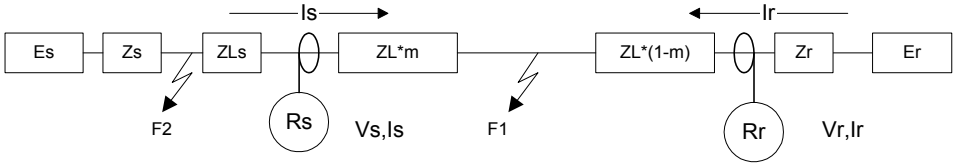


Figure 4.17: Dual Source Single-Line System for Two Nonsimultaneous Faults

General polarizing concepts

For protective relaying, the polarizing signal should be continuously available and should be valid regardless of fault type and distance. Torque equations, generally in the form of Equation 4.26, will determine fault direction; positive torque results from forward faults and negative torque from reverse faults. Schweitzer and Roberts demonstrate that Equation 4.27 is equivalent to Equation 4.26 but is more computationally efficient in microprocessor-based systems that use rectangular representations of complex variables.[32] No single approach works equally well for all types of faults and line configurations. [33] Therefore, computer-based relays frequently use multiple schemes in combination with a fault type selection to make the best determination of the fault direction. Appendix 11.11 presents examples of the ten possible fault types, as well as candidates for polarizing.

$$T = |Vpol| \cdot |Iop| \cdot \cos(\angle - Vpol - \angle Iop) \qquad \text{Equation 4.26}$$

where *Iop* is the current of the faulted phase.

$$T = \mathrm{Re}\left[-Vpol \cdot \overline{Iop}\right] \qquad \text{Equation 4.27}$$

Fault-Based Available Polarizing Signals [35]

Both phase and symmetrical component voltages and currents can provide a reference signal for polarizing. The degree that the faulted phase voltage collapses depends on the source impedance, the impedance between the relay, and the fault, as demonstrated in Figure 4.18. This plot shows that the phase voltage has its maximum value at the sources at both ends and decreases to a value equal to the fault current times the fault resistance. Therefore, determining direction when the fault is close to the relay or the source impedance behind the relay is significantly more than the fault resistance and the line impedance to the fault requires polarizing quantities with memory.

Conversely, the symmetrical component voltages for nonsymmetrical faults are zero at the sources and are maximum at the point of the fault as shown in Figure 4.19. The horizontal axis in both Figure 4.18 and Figure 4.19 represents either distance or increasing impedance. The generation of straight-line voltage profiles assumes a linear distribution of impedance as a function of distance. Represent discrete lumps of impedance, such as would be encountered in transformers, by vertical changes in voltage. Hence, symmetrical component voltages produce better polarizing quantities for nonsymmetrical faults close to the relays, whereas self- or cross-polarizing phase voltages are better for distant and/or high impedance faults.

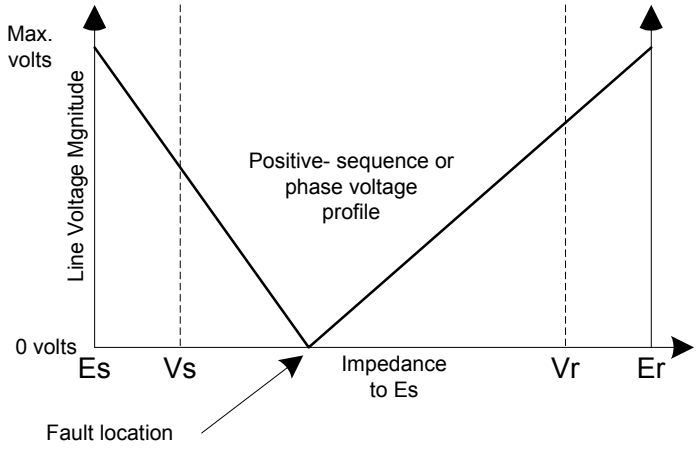


Figure 4.18: Phase Voltage Profile for Line-to-Ground Faults in a Two-Source System

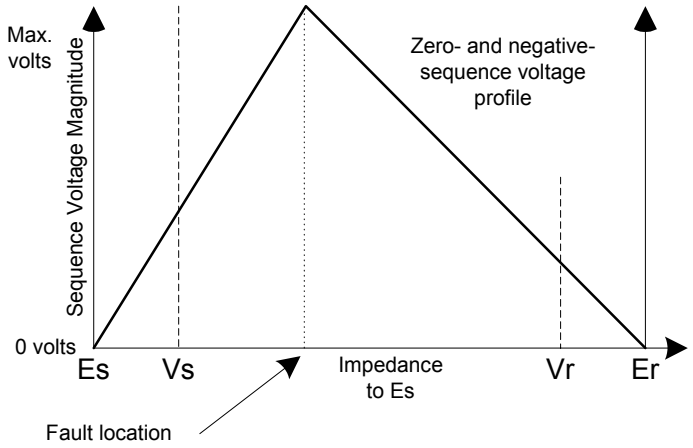


Figure 4.19: Zero- and Negative-Sequence Voltage Profile for Line-to-Ground Faults in a Two-Source System

Phase and symmetrical component currents do not change, regardless of fault location or source impedance, provided there are no other branches in the circuit. In other words, the representations of Figure 4.18 and Figure 4.19 are true as long as there is only one current. However, this is rarely the case. Even the mutual couplings by inductance and capacitance constitute additional paths that current can take. More commonly, tapped loads and parallel circuits provide alternate paths for the current to travel.

Self-Polarizing and Memory Circuits

Self-polarizing directional units do not work well for line-to-ground faults close to the point that the voltage is measured because it is difficult to determine the phase of low amplitude signals. Hence relays use a memory voltage. Electromechanical relays use a parallel LC circuit designed to resonate at 60 Hz. Computer-based relays use a digital filter that implements an algorithm similar to Equation 4.28, which produces a response to a loss of signal, as shown in Figure 4.20. The signal is sampled synchronously, which means that the sample rate is an integer multiple of the nominal frequency of the input signal. Such memory filters slowly track changes in amplitude and phase while providing sufficient signal for signal processing when a fault occurs. Figure 4.20 demonstrates that there are zero degrees of phase shift between the filter input and output. Since only the phase is important for polarizing signals, the amplitude of this signal is not critical provided there is enough signal to determine the phase. As Figure 4.20 shows, there are multiple cycles of signal after the input is set to zero. There is also a transient response once the signal is asserted again, so recapturing the phase of the signal takes time. Relay logic must compensate for the time lag between energizing the system and the availability of a valid polarizing signal. The closer a_1 is to unity, the longer the memory. Many popular relays using memory polarizing use a "fast charge" such that after the loss of potential, the coefficient a_1 is set to zero (hence no memory) for *N* samples as illustrated in Figure 4.21.

$$V_{MEM} = V_{IN} - a_1 V_{MEM}\, z^{-N/2}, \qquad \text{Equation 4.28}$$

N = number of samples per cycle of a synchronously

sampled signal, z^{-1}, is the unit delay operator, and $0 < a_1 < 1$

$$Hz = \frac{1}{1 + a_1 z^{-N/2}}$$ Equation 4.29

To further investigate this digital memory filter, take the frequency response of the transfer function Equation 4.29. Figure 4.22 shows that for a sampling rate of 16 times the fundamental, there are four resonance frequencies at the odd harmonics of 60 Hz. Therefore, it is important to use a signal that is free from odd harmonics for the input to this filter. Apart from the fundamental and the three harmonics, all other signals are well attenuated. Figure 4.22 also shows the net effect of the analog anti-aliasing filter, the cosine filter, and the memory filter, all of which operate on the input signal in a cascaded fashion.

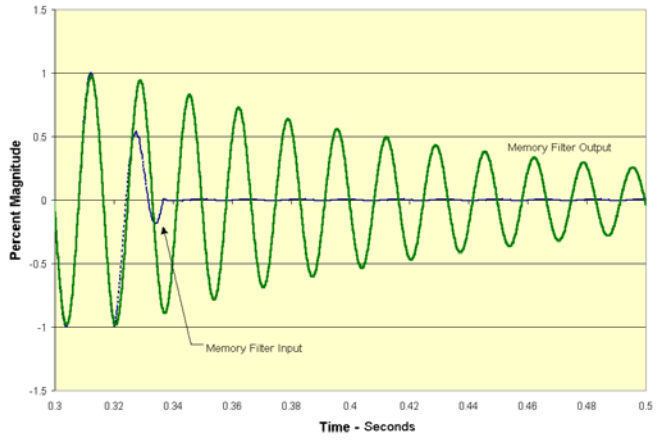


Figure 4.20: Response of a Digital Memory Filter to a Step-Loss of Input Signal

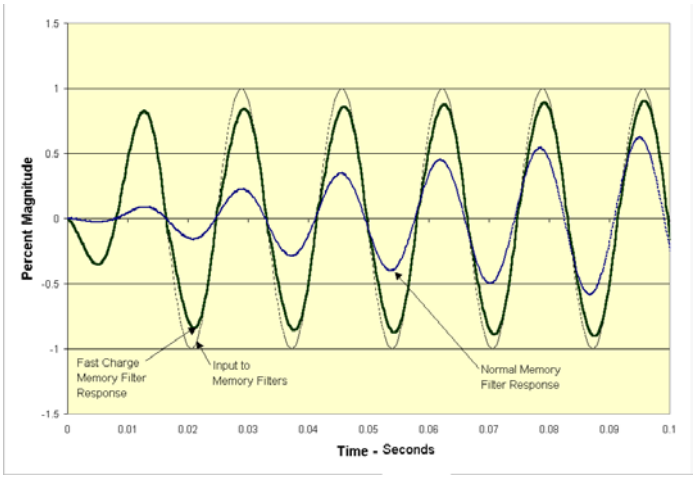


Figure 4.21: Effect of Fast-Charging Memory Filter

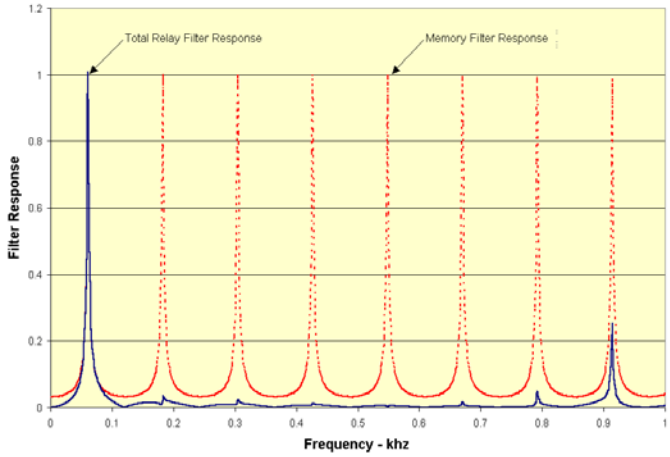


Figure 4.22: Memory Filter and System Total Frequency Response for a = 15/16

When the fault current is significantly greater than the load current, the current lags the source voltage in an inductive circuit. The relative direction of the source can be determined using the voltage as the directional or polarizing reference signal. This method is called self-polarizing; Schweitzer et al. have presented numerous conference papers on the subject. [33],[34] During a ground fault, load current can adversely affect the direction determined by a relay that uses a memorized polarizing voltage. Figure 4.23 illustrates how the line current phase angle shifts for a low current fault case when the load is in and out of the line relative to the relay. This plot also shows that the magnitude of the measured fault current Ia_{F2} is less than that of Ia_{F1}. As a result the relay underreaches when load current is in the bus and overreaches when load current is out of the bus.

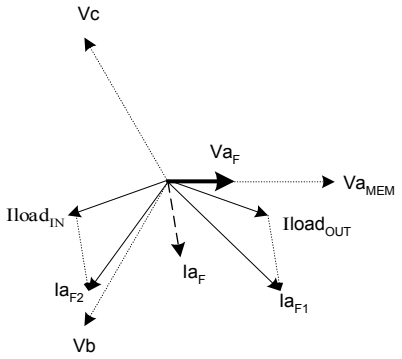


Figure 4.23: Effects of Load Current on High-Impedance Faults

4.2.4.1.1 Cross polarizing

Use cross-polarized signals to polarize ground-fault detecting elements for single-line-to-ground faults. These elements use the unaffected phases to form the polarizing reference. However, use special consideration when employing single-pole tripping because the reference phase may already be open when a second fault occurs that needs the reference of that particular phase. As with other polarizing

approaches, fault type identification is critical for proper operation. Roberts provides a comprehensive analysis of approaches to directional element implementations and provides the data shown in Table 4.3. [35]

Table 4.3: Cross-Polarized Fault Table

Faulted Phase	*Operating Quantity (Iop)*	*Polarizing Quantity (Vpol)*
A	Ia	Vpol=Va-Vb
B	Ib	Vpol=Vc-Va
C	Ic	Vpol=Va-Vb
AB	Iab	Vpol=-jVc
BC	Ibc	Vpol=-jVa
CA	Ica	Vpol=-jVb

To illustrate this polarizing approach, consider the lossless system for a configuration shown in Figure 4.17. Lossless systems contain only purely reactive impedances and are also called 90° systems because the phase current lags the phase voltage by 90°. For a single-line-to-ground fault on phase-C with zero fault impedance, the phase-C current measured by relay Rs, Isc, will lag the phase-C voltage of Vs by 90°. The resultant angle is 30°. The phase of the polarizing voltage is computed by subtracting the vectors Va-Vb using rectangular coordinates as shown in Equation 4.30 and illustrated by Figure 4.24. Torque computations similar to Equation 4.31 result in the largest positive torque value. Since the fault is between relays Rs and Rr, the results are identical except for the magnitude of the phase current. If a single-line-to-ground fault occurs at F2, then the current at relay Rs is 180° out of phase. This phase reversal produces a negative result in the torque computations. Using the corresponding Vpol listed in Table 4.3 produces similar results for single-line-to-ground faults for phases A and B.

$$\begin{aligned} \text{Vab} &= |\text{V}|\angle 0° - |\text{V}|\angle 240° \\ &= |\text{V}|(1 + \text{j}\,0 \;\; (-0.5\,\text{j}\,0.866) = |\text{V}|(1.5 + \text{j}\,0.866)) \\ &= |\text{V}|\angle 30° \end{aligned} \qquad \text{Equation 4.30}$$

$$Tabc = |Iabc| \cdot |Vpol| \cdot \cos(\angle Vpol - (\angle Iabc) + MTA) \qquad \text{Equation 4.31}$$

where *abc* denotes phase A, B, or C and MTA is the positive sequence line angle

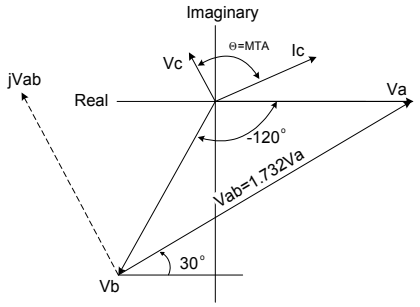


Figure 4.24: Vector Diagram for Phase-C-to-Ground Fault

4.2.4.1.2 Sequence polarizing

Other choices for polarizing quantities include symmetrical component voltages and currents as described by Equation 4.32Equation 4.32 through Equation 4.34. Symmetrical component currents are popular for polarizing quantities because they are relatively unaffected by load current. Because of unbalanced lines and/or loads, only positive-and negative-sequence currents are available during nonfaulted conditions. If a path exists to complete the circuit for the ground current, the relay generates zero-sequence voltages and currents for phase-to-ground faults.

Fault direction is computed using torque calculations where the results are positive for forward faults and negative for reverse faults. The magnitude can be perceived as a confidence factor where inputs with small magnitudes can produce unreliable results. Hence low magnitude torque values should be ignored or used only if no better information is available.

For balanced systems at steady state, the relay generates negative-sequence voltages and currents for all but balanced three-phase faults. Negative-sequence voltages can be weak to detect depending on the source impedance behind the relay and on impedance between the relay and the fault, as discussed in section 0 and illustrated in Figure 4.18 and Figure 4.19. A discussion of each sequence polarizing quantity follows. (See section 0 and Appendix 11.10 for additional details on symmetrical components.)

$I0 = Ia + Ib + Ic \text{ and } V0 = Va + Vb + Vc$	Zero	Equation 4.32
$I1 = Ia + a \cdot Ib + a^2 \cdot Ic \text{ and}$ $V1 = Va + a \cdot Vb + a^2 \cdot Vc \text{ where } a = 1\angle 120°$	Positive	Equation 4.33
$I2 = Ia + a^2 \cdot Ib + a \cdot Ic \text{ and } V1 = Va + a^2 \cdot Vb + a \cdot Vc$	Negative	Equation 4.34

4.2.4.1.2.1 Zero-sequence current polarizing

A polarizing current is available only if a zero-sequence source is available, such as the neutral current in a grounded wye transformer. The transformer need only supply only a portion of the ground current. Equation 4.35 and Equation 4.36 compute the

direction as torque quantity with both sign and magnitude. The phase of the polarizing current does not change for faults at positions Fault #1 and Fault #2, illustrated in Figure 4.25, but the phase angle of the residual current ($3I_0$) reverses by 180°.

$$32TV = |Ipol||Ires| \cos(\angle Ipol - \angle Ires) \text{ where} \qquad \text{Equation 4.35}$$

$$Ires = \vec{Ia} + \vec{Ib} + \vec{Ic} \qquad \text{Equation 4.36}$$

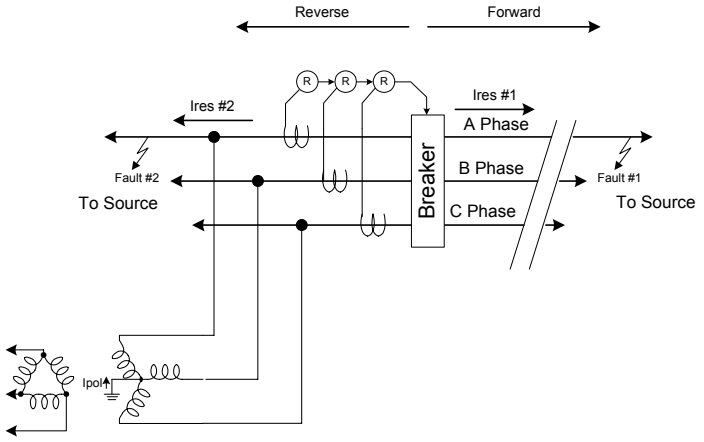


Figure 4.25: Polarizing Current Provided From a Delta-Grounded Wye Transformer

Table 4.4 and Table 4.5 show the phase angles for forward and reverse phase-to-ground faults. The exact angles computed are a function of the circuit and the power system angle. Table 4.4 shows that the difference between the polarizing and operating current results in angles close to zero. The cosine of this angular difference always produces a positive result with a multiplier close to unity. Table 4.5 shows that the difference is close to 180°, which produces a negative result with a multiplier that is also close to unity.

Table 4.4: Polarizing and Operating Current Phase Angles for Forward Phase-to-Ground and Two-Phase-to-Ground Faults Using *Ires* for *Ipol*

Fault type	*∠Ipol*	*Iop = ∠Ires*	*∠Ipol - ∠Ires*
AG	-82.4°	-81.2°	-1.2°
BG	157.7°	159.0°	-1.2°
CG	37.5°	38.7°	-1.2°
ABG	-143.6°	-143.2°	-1.4°
CBG	97.6°	98.7°	-1.1°
CAG	-23.0°	-21.8°	-1.2°

Table 4.5: Polarizing and Operating Current Phase Angles for Reverse Phase-to-Ground and Two-Phase-to-Ground Faults

Fault type	*∠Ipol*	*Iop=∠Ires*	*∠Ipol -∠Ires*
AG	-73.9°	115.5°	-189.4°
BG	166.5°	-4.7°	171.2°
CG	46.2°	124.6°	170.8°
ABG	-134.5°	56.1°	-190.6°
CBG	106.1°	-66.8°	172.9°
CAG	-14.0°	175.8°	-189.8°

Consider a fault at location F2 in the system shown in Figure 4.26. Relay Rs may detect the fault forward or reverse depending on the distance from Bus S to the fault on line #2. More positive direction torque for relay Rs results if the fault is on Line #2, closer to Bus R. Faults at Bus R immediately behind relay R are indistinguishable from faults at Bus R immediately in front of relay R. Depending on the fault impedance, line unbalance, and load, faults at 50 percent of Line #2 may produce positive torque. Relay systems using the transformer neutral current for the polarizing quantity may not perform satisfactorily for cases of multiple parallel lines.

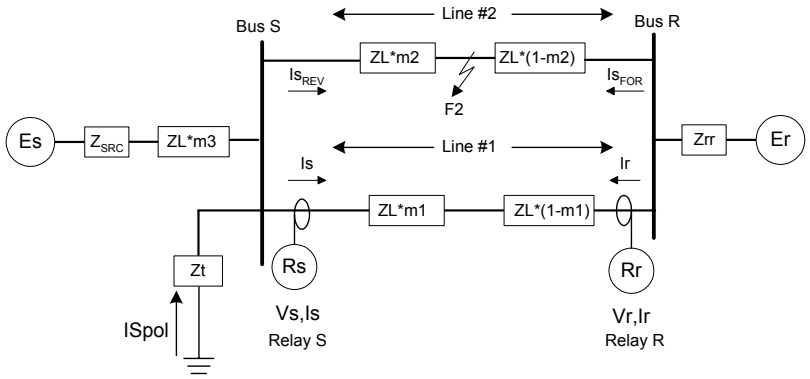


Figure 4.26: Single-Line Diagram of a System With Two Sources Connected by a Double-Circuit Transmission Line

4.2.4.1.2.2 Zero-sequence voltage polarizing

Equation 4.37 provides the torque expression for zero-sequence voltage polarizing using zero-sequence current for the operating quantity. Angle ZL_0 is the angle of the line zero-sequence impedance. The residual current seen by the relay is $3I_0$, which is equal to (Ia +Ib +Ic). Similarly, V_0 equals (Va +Vb +Vc). If the source behind the relay is too strong (low source impedance behind the relay), then a low torque value results from small values of V_0 because the voltage divides, as discussed in section 0.

$$T32V = |3V_0| \cdot \|3I_0\| \cdot \cos(\angle - V_0 - (\angle I_0 + \angle ZL_0)) ,$$ Equation 4.37

$\angle$-V0 is V0 shifted by 180°

Guzman, Roberts, and Hou, using Equation 4.38, present an alternate directional algorithm based on zero-sequence voltage current.[36] The result calculated for Z_0 is negative for forward faults and positive for reverse faults. For an explanation of this sign reversal from the torque equations, see a discussion of similar expressions for negative-sequence direction algorithms.[35] A threshold impedance can limit the reach for faults in the forward direction. A major advantage of using Equation 4.38 is that the result is not sensitive to the magnitude of V_0. This is because the quantity V_0/I_0 is a constant since the current is a linear function of the voltage. Another advantage of this algorithm over Equation 4.35 is that it doesn't require the polarizing current generated by the transformer grounded wye leg, which is not always available.

Equation 4.38

$$z_0 = \frac{\mathrm{Re}\left[3V_0 \cdot \overline{\left(\frac{ZL_0}{|ZL_0|} \cdot 3I_0 \right)} \right]}{|3I_0^2|}$$

Forward faults results in negative z_0 values

4.2.4.1.2.3 Negative-sequence voltage and impedance polarizing

Use Equation 4.40 for directional algorithms using negative-sequence voltage for polarizing. Phase-to-phase-to-ground and phase-to-ground faults generate negative-sequence quantities. This approach has the same limitations as using zero-sequence voltage for polarizing, except that it is not affected by zero-sequence mutual coupling of parallel lines. Computing the apparent negative sequence impedance between the relay and the fault as shown in Equation 4.43 overcomes the problem of a weak polarizing quantity caused by low source impedance behind the relay. [37] [36] [35]

$$T32Q = |3V_2| \cdot \overline{|3I_2|} \cdot \cos(\angle - V_2 - (\angle I_2 + \angle ZL_2)) ,$$ Equation 4.39

$\angle$-V_2 is V_2 shifted by 180°

When the negative-sequence source behind the relay terminal is very strong, the negative-sequence voltage (V_2) at the relay can be very low, especially for remote faults. To overcome low V_2 magnitude, we can add a compensating quantity that boosts V_2 by ($\underline{\alpha} \cdot ZL_2 \cdot I_2$). The constant, α, controls the amount of compensation.

Equation 4.40 shows the torque equation for a compensated negative-sequence directional element. The term ($\underline{\alpha} \cdot ZL_2 \cdot I_2$) adds with V_2 for forward faults and subtracts for reverse faults. Setting $\underline{\alpha}$ too high can make a reverse fault appear forward. This results when ($\underline{\alpha} \cdot ZL_2 \cdot I_2$) is greater, but 180° out of phase with, the measured V_2 for reverse faults.

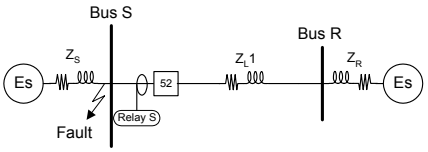
$$T32Q = \mathrm{Re}(V_2 \cdot \alpha\, ZL_2\, I_2) \cdot (ZL_2 \cdot I_2)$$ Equation 4.40

Figure 4.27 shows the sequence network for a ground fault at the relay bus. The relay measures IS_2 for forward faults and $-IR_2$ for reverse faults. Use Equation 4.41 to calculate the negative sequence impedance, Z_2, from V_2 and I_2 and Equation 4.42

to calculate this impedance for forward SLG faults. Figure 4.27 shows this relationship for a 90° (purely inductive) system.

$$Z_2 = {-V_2}/{IS_2} = -ZS_2 \qquad \text{Equation 4.41}$$

$$Z_2 = {-V_2}/{IR_2} = (ZL_2 + ZR_2) \qquad \text{Equation 4.42}$$



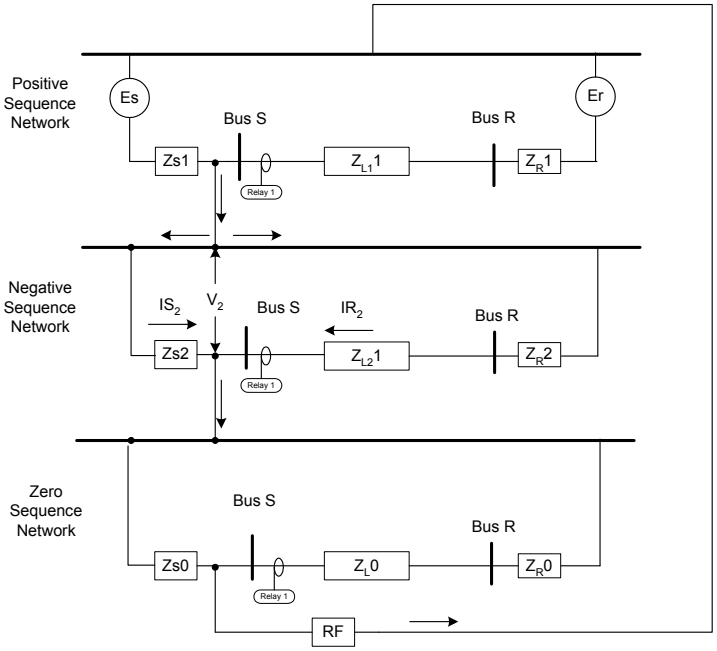


Figure 4.27: Sequence Network for a Reverse Single-Line-to-Ground (SLG) Fault

Determine the forward/reverse torque balance condition by setting the left side of Equation 4.40 equal to zero. Letting *z2* be equal to $(\underline{\alpha} \cdot ZL_2 \cdot I_2)$ and solving for z2 at zero torque results in Equation 4.43. Recall that the $(\underline{\alpha} \cdot ZL_2 \cdot I_2)$ term increases the amount of V_2 for directional calculations. This is equivalent to increasing the magnitude of the negative-sequence source behind the relay location. The same task is accomplished by increasing the forward z2 threshold.

$$z2 = \frac{\mathrm{Re}\left[3V_2 \cdot \overline{\left(\frac{ZL_2}{|ZL_2|} \cdot 3I_2\right)}\right]}{\left|3I_2^2\right|}$$

Equation 4.43

Forward faults result in negative z2 values

The z2 directional element has all the benefits of both the traditional and the compensated negative-sequence directional element. It also provides better visualization of how much compensation is secure and required. Set the forward and reverse impedance thresholds based on the strongest source conditions. Weak sources (high source impedances) actually enhance negative-sequence direction discrimination.

As Figure 4.28 illustrates, the negative-sequence directional element measures negative-sequence impedance at the relay location. The relay then compares this measurement to forward- and reverse-impedance thresholds, which are settings. The direction is forward (in front of the relay) if the measured negative-sequence impedance is less than the forward-impedance threshold setting. The direction is reverse (behind the relay) if the measured negative-sequence impedance is greater than the reverse-impedance threshold setting.

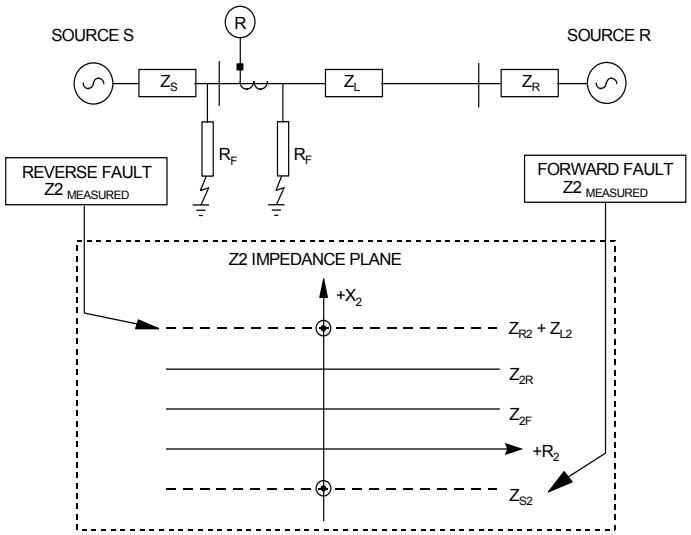


Figure 4.28: Measured Negative-Sequence Impedance Determines Direction

One advantage of the negative-sequence directional element is the ability to operate correctly for both phase-to-ground and phase-to-phase faults. However, like the directional element using zero-sequence voltage or current, it does not work well, if at all, with three-phase faults. The impedance-based directional element is more secure and reliable than a conventional negative-sequence directional element that calculates torque. The impedance-based directional element is better for faults at the end of long lines because they provide minimal negative-sequence voltage for systems with strong negative-sequence sources.

4.1.1 Distance Relays (ANSI type 21)

The example present in section 0 demonstrates one case where the 52 relay tripped incorrectly because of coordination problems under loaded conditions. The same scenario can be made for the 50 and 67 relays as well. Another problem with overcurrent relays is providing backup protection under widely varying source impedance conditions. Consider the system represented by Figure 4.29 that has a maximum five-amp secondary (from the CT) load current and a nominal 70 secondary (from the PT) at the source Es1 or Es2. For this system, assume that source impedance Zs1 is 1Ω and Zs2 is15Ω and either source must be capable of independently carrying the load. If the system has a three-phase fault with1Ω line impedance from Bus S to the fault, the fault current is equal to 70 V/1.9375 Ω or 36 A. If the source, Es1, is not connected, under the same faulted condition the fault current is 70 V/15 Ω or 4.67 A. Clearly the fault current is less than the load current and the relay will not trip. Distance relaying that measures the impedance to the fault is less sensitive to load current, yet provides the sensitivity needed for the problem cases just described.

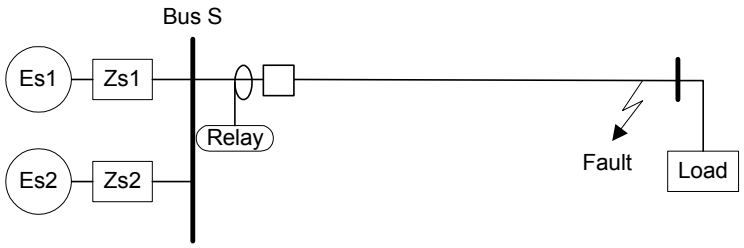


Figure 4.29: Fault Coverage Under Widely Varying Source Impedance Conditions

All lines have impedance that is proportional to the length of the line. The line angle is computed as the arctangent of the ratio of reactive to resistive impedance at 60 Hz. For overhead lines with 80 percent reactive and 20 percent resistive series impedance, this angle is nominally 77 degrees. Although the magnitude of the impedance increases with length, the line angle remains constant. Distance relays are called such because they compute the impedance to the fault, which is proportional to line length between the relay and the fault. Distance relays offer the following advantages over time-overcurrent relays:

- Greater instantaneous trip coverage
- Lower sensitivity to source impedance changes
- Better sensitivity to fault currents
- Reduced sensitivity to load
- Easier coordination with other distance relays

Electromechanical distance relays use torque-producing coils to make trip contacts open or close. Microprocessor-based relays calculate torque-like quantities based on torque equations.

Impedance Distance Relaying

Distance relays use current to create operating torque and voltage to generate restraining torque. When the operating torque exceeds the restraining torque, the trip contacts are closed. Equation 4.44 shows the part of the basic torque used for computing impedance for impedance-type relays. As Figure 4.30 shows, this operation can be perceived as a balanced beam system where voltage produces the restraining torque and current the operating torque. The balance point defines the fault/no fault boundary of the relay where there is zero torque. Equation 4.45 defines the voltage and current for a fault on the boundary.

$$T = K_1 I^2 - K_2 V^2 \qquad \text{Equation 4.44}$$

$$K_2 V^2 = K_1 I^2 \qquad \text{Equation 4.45}$$

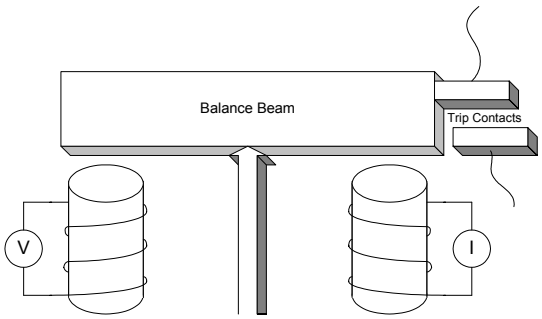


Figure 4.30: Balance Beam Torque Element

Since any positive nonzero torque produces a trip, equality between the voltage and current terms in Equation 4.45 determines the sensitivity limit, resulting in zero torque. As Equation 4.46 [38]and Equation 4.47 show, solving Equation 4.45 for the zero torque case provides the relationship for voltage and current as relates to impedance. If the balance impedance is a percentage of the line impedance, then that percentage is called the reach of the relay.

$$V/I = \sqrt{K_1/K_2} = Z \qquad \text{Equation 4.46}$$

$$T = K_2 \left(Z^2 I^2 - V^2 \right) \qquad \text{Equation 4.47}$$

Plotting of all possible values of voltage and current that produce zero torque on an R-X (real-imaginary) diagram forms a circle with the center at the origin and a radius of Z, assuming that K_2 is set to unity. The ratio of any voltage and current combination that results in a point inside the circle will produce torque, closing the trip contact.

Figure 4.31 illustrates the distance relay operation using an R-X diagram. This figure shows the line impedance as a line starting at the origin extending at the angle equal to the line angle. The reach of the relay is a fraction of the total line impedance (labeled “n” in Figure 4.31). The point where the circle-generated ratios of voltage

to current that produce zero torque and the line impedance vector is called the reach of the relay. Reach is usually denoted as a percent of the total line. Since the relay will trip for any fault inside the circle, a directional-sensing element must be added to restrict trips for faults in the reverse direction.

Impedance relays are inherently nondirectional. One means of making impedance relays directional is to provide directional control with a type 32 relay as discussed in section 0. Equation 4.48 provides another method of directional control where τ is the line angle and θ the angle between the line impedance vector and the difference between the voltage and current.. As long as positive torque is produced, then the direction contacts are closed, enabling the trip circuits. Assuming that K_1, the voltage, and the current are all nonzero, zero torque is produced whenever $(\theta-\tau)$ is $\pm$ 90°. The directional characteristic is shown in Figure 4.31 as the line orthogonal to the line angle.

$$T = K_1 \left|\mathrm{V}\right|\left|\mathrm{I}\right| \cos(\theta - \tau) \qquad \text{Equation 4.48}$$

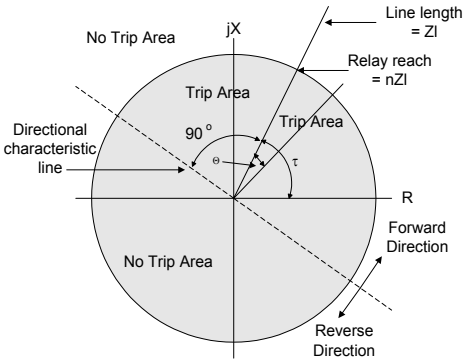


Figure 4.31: RX Diagram for Impedance-Based Distance Relay

Ohm distance relays are sensitive to fault resistance and infeed from remote sources. As Figure 4.31 illustrates, load into the source behind the relay makes relays underreach, while load current out of this source makes impedance relays overreach. Section 4.1.1.5, below, discusses the techniques for overcoming these sensitivities, where the relay operates on explicit values of fault resistance and line reactance.

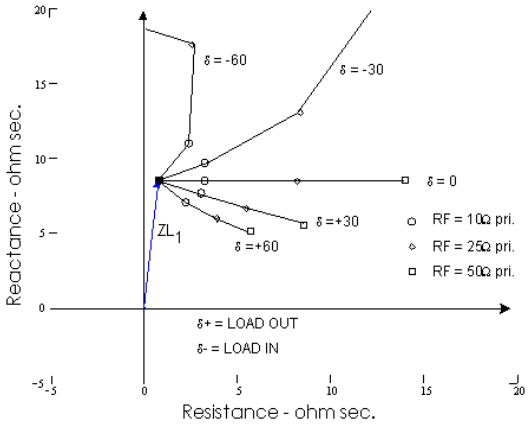


Figure 4.32: Effects of Load Flow and Fault Resistance on Apparent Impedance

4.1.1.1 Modified impedance relays

As previously shown, impedance relay sensitivity is uniform regardless of the direction of the derived impedance. Shifting the center of the characteristic circle along the line impedance vector reduces the sensitivity to load currents as well as to faults in the reverse direction. Equation 4.49 describes the modified torque equation. The constant C determines how far the center of the circle shifts from the origin of the RX diagram as shown in Equation 4.50.

$$T = K_1 I^2 - K_2 (V + CI)^2 \qquad \text{Equation 4.49}$$

$$Z = V/I = -C \pm \sqrt{K_1/K_2} \qquad \text{Equation 4.50}$$

4.1.1.2 Concepts of reactance distance relays

Figure 4.33 shows a reactance distance relay that combines an overcurrent element with a directional element, as expressed in Equation 4.51. K_4 represents a mechanical restraining spring and θ is the angle that the current lags the voltage. By solving for zero torque, we can rewrite Equation 4.51 as Equation 4.52. If we note that $|Z| \sin(\theta)$ is the reactive component of Z and ignore the spring constant, Equation 4.53 relates the reactance to constants K_1 and K_3 for zero torque. The relay uses only the reactive component of the fault impedance to make the trip/no trip decision. Adding the restraint from the mechanical spring moves the characteristic line toward the real axis.

$$T = K_1 I^2 - K_3 |V| |I| \sin(\theta) - K_4 \qquad \text{Equation 4.51}$$

$$\frac{|V|}{|I|} \sin(\theta) = |Z| \sin(\theta) = \frac{K_1}{K_3} - \frac{K_4}{K_2 I^2} \qquad \text{Equation 4.52}$$

$$|Z|\sin(\theta) = X = \frac{K_1}{K_3} \qquad \text{Equation 4.53}$$

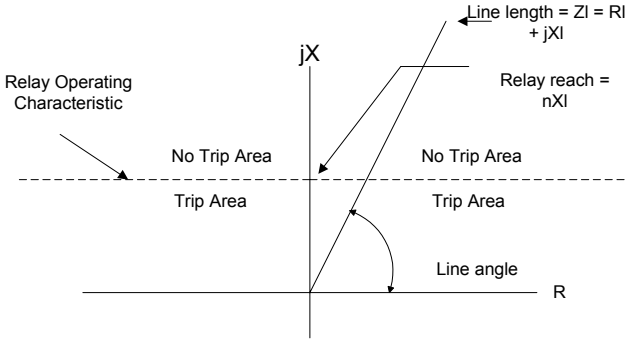


Figure 4.33: Characteristics of a Reactance Distance Relay

4.1.1.3 Starting units

Since the impedance relay could operate for large reactive loads, it requires a directional element that also rejects such loads. This directional element is often a voltage-restrained element. When used with a reactance distance relay, the characteristic torque equation becomes Equation 4.54, where θ is positive for lagging current and τ is the line impedance angle. Solving this equation for the balance point, where the torque equals zero, results in the expression shown in Equation 4.54. Ignoring the spring constant results in the expression for impedance characteristic shown in Equation 4.56.

$$T = K_3 V I \cos(\theta - \tau) - K_2 V^2 - K_4 \qquad \text{Equation 4.54}$$

$$\frac{V}{I} = Z = \frac{K_3}{K_2}\cos(\theta - \tau) - \frac{K_4}{K_2 V I} \qquad \text{Equation 4.55}$$

$$Z = \frac{K_3}{K_2}\cos(\theta - \tau) \qquad \text{Equation 4.56}$$

Figure 4.34 shows the results of combining a starting unit with a reactance relay. The trip area for this characteristic is defined as the region inside the starting characteristic circle, S, and below the reactance line marked X1. The starting unit provides both direction sensitivity and distance.

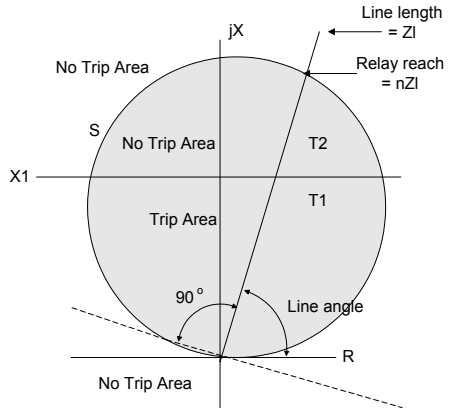


Figure 4.34: Reactance Distance Relay Characteristics With a Starting Unit

4.1.1.4 Mho distance relay

The characteristics of the mho distance relay are identical to the starting unit described above. When the mechanical spring constant are included, the diameter of the circle, S, in Figure 4.34 as described by Equation 4.56 is independent of voltage and current magnitude except for low levels of voltage or current. Low voltage levels are a problem when the fault is very close to the relay origin, causing the circle to collapse. In such cases, use a memory voltage to conserve the prefault voltage magnitude and phase.

It is much easier to set mho ground distance elements than quadrilateral ground distance elements. This is because mho elements require fewer settings and are less influenced by unequal source and line impedance angles.

A mho element using positive-sequence memory-polarization has a dynamic response that improves the resistive fault coverage offered by the relay. Under weak source conditions a mho element can offer better resistive fault coverage for close-in faults than a quadrilateral ground distance element.

4.1.1.4.1 Advantages of using mho ground distance elements

easy to set

less influenced by system nonhomogeneity than the quadrilateral element

capable of providing better resistive fault coverage than the quadrilateral element under certain system conditions

4.1.1.4.2 Disadvantages of using mho ground distance elements

provide limited resistive fault coverage for faults at the end of the element reach

provide limited resistive fault coverage for strong source conditions

are influenced by zero-sequence mutual coupling

Typically, six distance elements detect six of the seven possible types of faults as listed in Table 4.6. [33,39] The three phase-to-phase fault elements also detect the seventh fault type, three-phase-to-ground faults.

Table 4.6: Voltages and Currents for Six Mho Distance Elements

Fault Type	Voltage V	Current I	Polarization Vpol	Torque T
A to Gnd	Va	Ia + k0 Ir	Va1mem	Tag
B to Gnd	Vb	Ib + k0 Ir	Vb1mem	Tbg
C to Gnd	Vc	Ic + k0 Ir	Vc1mem	Tcg
A to B	Va – Vb	Ia – Ib	-j Vc1mem	Tab
B to C	Vb – Vc	Ib – Ic	-j Va1mem	Tbc
C to A	Vc – Va	Ic – Ia	-j Vb1mem	Tca
K0 = (Z0/Z1 – 1)/3 mem denotes memory voltage				

Depending on the type of fault, use Equation 4.1 or Equation 4.24 to compute the six torque values. The results are identical. [34] Both of these equations derive from Equation 4.48. In Equation 4.57 and Equation 4.59, m is the per-unit reach and ZL is the total line impedance. Table 4.6 defines variables V, I, and Vpol. As discussed in section 4.6.1.2, a voltage memory circuit generates the polarizing voltages described by Equation 4.60 through Equation 4.62. The unconventional shifting in these three equations results in the conventional shifts required for the positive-sequence component, but with better transient response. [33] Therefore, to shift by 240°, shift by 60° and negate the result (which is the same as adding 180° to the quantity already shifted by 60°).

$$T = \mathrm{Re}\left[\left(m \cdot ZL \cdot I - V\right) \cdot \overline{Vpol}\right] \quad \text{where} \qquad \text{Equation 4.57}$$

$$\overline{Vpol} = \textit{Vpol complex conjugate} \qquad \text{Equation 4.58}$$

$$T = \left|m \cdot ZL \cdot I - V\right| \left|Vpol\right| \cos\left(\angle\left(m \cdot ZL \cdot I - V\right) \angle Vpol\right) \qquad \text{Equation 4.59}$$

$$Va1 = \left[Va - (a-1)Vb - \left(a^2 - 1\right)Vc\right] \Big/ 3 \qquad \text{Equation 4.60}$$

$$Vb1 = \left[Vb - (a-1)Vc - \left(a^2 - 1\right)Va\right] \Big/ 3 \qquad \text{Equation 4.61}$$

$$Vc1 = \left[Vc - (a-1)Va - \left(a^2 - 1\right)Vb\right] \Big/ 3 \qquad \text{Equation 4.62}$$

4.1.1.4.3 Voltage Plane Representation

The impedance plane with resistance and reactance as coordinates is convenient for describing the operation of impedance relays.

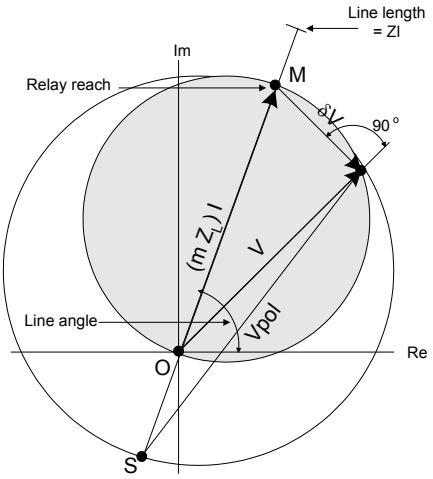


Figure 4.35: Mho Relay Operations Described Using the Voltage Plane

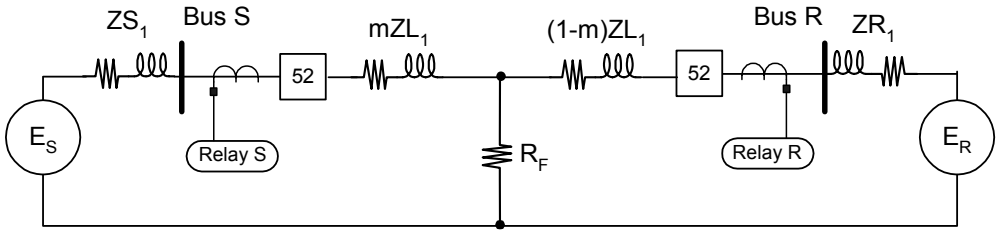


Figure 4.36: Circuit Loops of a Faulted Power System Network

4.1.1.5 Quadrilateral Distance Relay [6065] [39]

Although the distance relay is inherently directional provided the reach is limited (see section 4.3.2.1), it does have sensitivity problems, particularly in the presence of fault resistance. As Figure 4.37 shows, the quadrilateral relay has characteristics that form a parallelogram, defined by R1, R2, X, and 32Q. It is possible to work with zero- and/or negative-sequence voltages and currents so that the fault resistance results are less sensitive to positive-sequence load.

To provide greater fault resistance coverage for close-in faults or systems with strong sources, set the resistive reach to be far more sensitive than that of conventional mho elements. It is also important to set the resistive reach so that the negative-sequence voltages and currents that result from normal operations or for out-of-section faults will not trip the relay. There is no practical reason for extending R2 to the left of the line defined by the line angle, although R1 and R2 can be set to be equal, for convenience. The resistance reach lines are parallel to the line angle because, as we will show, the fault resistance is computed independently of the line resistance.

If instrumentation errors are small, we can usually set the upper reactance, X, to the same reactive reach as the mho element (see section 4.2.5.5.1.1). The directional element defines the bottom of the parallelogram.

Quadrilateral elements can detect both phase and ground faults but require different algorithms. They can stretch in all directions to provide the desired sensitivity and

can combine with conventional mho elements to generate the tripping region shown in Figure 4.37. The characteristics of this figure are reproducible where remote end infeed is not significant, such as for radial lines.

Small errors in voltage and current measurements can cause errors in the reactance measurement with extended resistive reach settings. Limiting the resistive reach with respect to the reactance setting ensures that the relay is measuring adequate signals for proper operation, as discussed in section 4.2.5.5.1.1. Differences in the source and line impedance angles can cause the reactance element to overreach or underreach. It is common to reduce the reactive reach to obtain good fault coverage for close-in faults with high fault resistance and use a mho characteristic to get good line reach coverage. Figure 4.38 shows this combination. The following sections will discuss methods for properly setting the quadrilateral for optimum restive and reactive reach.

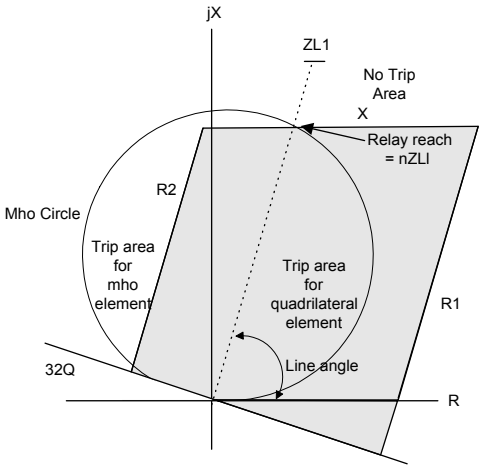


Figure 4.37: Quadrilateral Relay Characteristics Laid Over the Mho Relay Circle

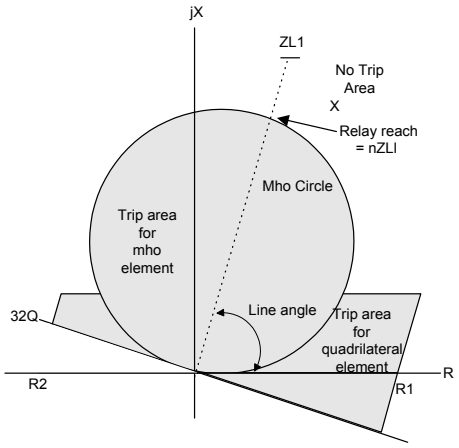


Figure 4.38: Combined Mho and Quadrilateral Characteristics

4.1.1.5.1 Ground Fault Quadrilateral Fault Detection

Ground fault protection using the quadrilateral element requires computing both the reactance to the fault and the fault resistance. For the sake of simplification at this point, assume that the relay measures the total fault current. We will relax this condition later in this section. Figure 4.39 provides the basis for the set of loop equations developed in Equation 4.63 through Equation 4.68. This mathematics relates the phase voltage and current seen by the relay to the positive-sequence line impedance that is usually provided for setting relays.

$$Va = Ia\, m(Zs) + V_M ba + V_M ca + Ia\, R_F,\ where \qquad \text{Equation 4.63}$$

$$V_M ba = m(Zm)\, Ib,\ V_M ca = m(Zm)\, Ic \qquad \text{Equation 4.64}$$

$$Va = m[\, Ia\,(Zs - Zm) + (Ia + Ib + Ic)\, Zm] + Ia\, R_F \qquad \text{Equation 4.65}$$

$$ZL_1 = (Zs - Zm),\ and\ Zm = (ZL_0 - ZL_1)/3 \qquad \text{Equation 4.66}$$

$$Va = m\left[ZL_1\ \ Ia + (Ia + Ib + Ic)\left(\frac{ZL_0 - ZL_1}{3} \right) \right] + Ia\, R_F \qquad \text{Equation 4.67}$$

$$\mathrm{Va} = \mathrm{m}\,\mathrm{ZL}_1\,(\mathrm{Ia} + \mathrm{k}_0\,\mathrm{Ir}) + \mathrm{Ia}\,\mathrm{R}_\mathrm{F},\ \mathrm{k}_0 = \frac{(\mathrm{ZL}_0 - \mathrm{ZL}_1)}{3 \cdot \mathrm{ZL}_1} \qquad \text{Equation 4.68}$$

$$\text{and } \mathrm{Ir} = \mathrm{Ia} + \mathrm{Ib} + \mathrm{Icl}$$

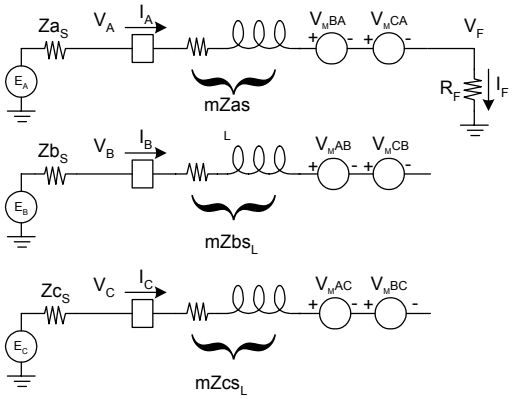


Figure 4.39: Single-Line-to-Ground Fault on a Three-Phase System

For quadrilateral elements, use two independent equations to determine both the reactance to the fault and the fault resistance. Derive both equations from the loop diagram shown in Figure 4.40. If either the switch at Bus R is open or the fault resistance is zero, the impedance is simply the voltage divided by the current. In this case neither the source impedance nor the impedance beyond the fault are of any consequence. Beginning with the result of Equation 4.68 we can use Equation 4.69 to solve for the fault resistance and Equation 4.70 for the reactance to the fault. Note that in both equations *Ia* is identical to the total fault current in both magnitude and

angle, with angle being the critical factor to make Equation 4.77 true. For this case alone, Z does equal V/I. [38]

$$R_F = \frac{\mathrm{Im}\left(\mathrm{Va}\cdot\overline{\left(\mathrm{ZL}_1\cdot\left(\mathrm{Ia}-\mathrm{k0\,Ir}\right)\right)}\right)}{\mathrm{Im}\left(\mathrm{Ia}\cdot\overline{\left(\mathrm{ZL}_1\cdot\left(\mathrm{Ia}-\mathrm{k0\,Ir}\right)\right)}\right)}, \text{where } \mathrm{k0}=\frac{\left(\mathrm{ZL}_0-\mathrm{ZL}_1\right)}{3\mathrm{ZL}_1} \qquad \text{Equation 4.69}$$

$$\text{and } \mathrm{Ir}=\mathrm{Ia}+\mathrm{Ib}+\mathrm{Ic}$$

$$X1=\frac{\mathrm{Im}\left(Va\,\overline{Ia}\right)}{\mathrm{Im}\left(\angle ZL_1\left(Ia-k0\,Ia0\right)\overline{Ia}\right)}, where\ \angle ZL_1=\frac{ZL_1}{\left|ZL_1\right|} \qquad \text{Equation 4.70}$$

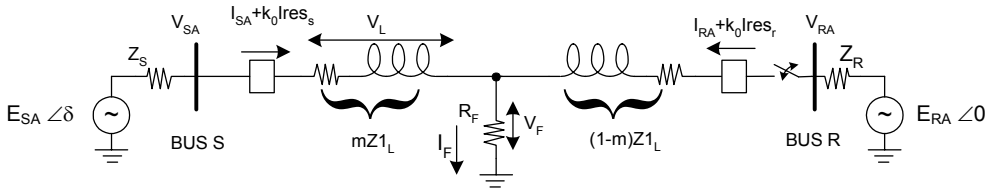


Figure 4.40: Loop Diagram for a Phase-to-Ground Fault

If the switch at V_{RA} is closed and R_F is not zero, then the relay at Bus S can no longer measure the total fault current and the phase angle of *Ia* is no longer co-linear with the phase angle of *If*. Without knowing the fault current from the remote end, we must approximate the fault current. A current distribution factor (CDF) relates the total fault current to the measured current, I_{SA}. The sequence component diagram in Figure 4.41 shows that the total fault current divides according to the zero-sequence impedance between the fault and the *S* and *R* ends of the line. For the zero-sequence CDF expressed in **Error! Reference source not found.** to be accurate, we must know the distance to the fault as well as the source impedances at both ends of the lines. If the system is co-linear (i.e. the phase angle of the source and line impedances are all equal) the CDF is a scalar quantity. This fault distance data is provided by Equation 4.88 in section 4.1.1.5.2.

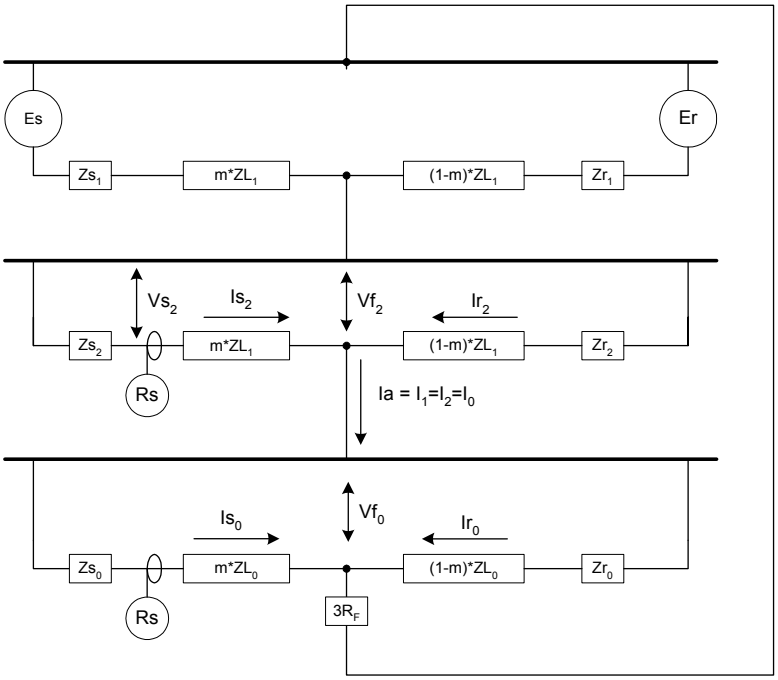


Figure 4.41: Symmetrical Component Diagram for a Single-Line-to-Ground Fault

$$CDF_0 = \frac{Zs_0 + (1-m)ZL_0 + Zr_0}{Zs_0 + ZL_0 + Zr_0} \qquad \text{Equation 4.71}$$

Where *m* is the per-unit distance to the fault

Load current also affects the accuracy of the results of Equation 4.69 and Equation 4.70. Reduce this problem by making the approximation that the faulted phase current, Ia, used to compute the fault current, is equal to two-thirds the sum of the faulted phase zero- and negative-sequence current as shown in Equation 4.72. Equation 4.73 shows the final result for calculating the fault resistance.

$$Ia = \left(\frac{3}{2}\right)\cdot\left(Ia_0 + Ia_2\right) \qquad \text{Equation 4.72}$$

$$R_F = \frac{\mathrm{Im}\left(Va \cdot \overline{\left(ZL1\cdot\left(Ia - k0\,Ir\right)\right)}\right)}{\mathrm{Im}\left(\left(\frac{2}{3}\right)\left(Ia_0 + Ia_2\right)\cdot CDF_0 \cdot \overline{\left(ZL1\cdot\left(Ia - k0\,Ir\right)\right)}\right)} \qquad \text{Equation 4.73}$$

Figure 4.41 shows that the negative-sequence fault current is equal to the zero-sequence current at the fault for single-line-to-ground faults. Equation 4.73 also shows that the CDF has a magnifying effect on the computed fault resistance. As the fault moves toward the remote end, the CDF becomes smaller. A decreasing CDF results in a larger R_F as computed by Equation 4.73. The net effect is that covering the same fault resistance for the entire length of the line requires increased resistive

fault coverage. It is easier to detect a one-ohm fault immediately in front of the relay than the same fault at the remote end of the line.

Only the phase of the polarizing quantity allows us to extract the variable we wish to solve for in Equation 4.68. This is done by making the coefficient of the variable that is to be isolated and removed real in the loop equation and taking only the imaginary part of the equation. Since the current is common for faults on radial lines, Equation 4.79 and Equation 4.80.

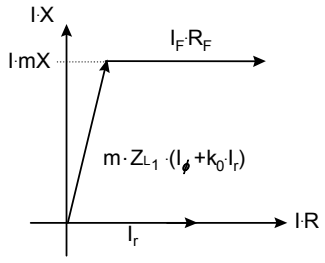
A system is completely homogeneous when the line and source angles are equal in all three sequence networks. The system is also considered homogeneous if the source and line impedances associated with the sequence current used by the reactance element for polarizing references have the same angle. For example, in a reactance element that uses zero-sequence current as a polarizing reference, consider only the zero-sequence network. In a reactance element that uses negative-sequence current as a polarizing reference, consider only the negative-sequence network. Here, we restrict the discussion to reactance elements that use zero-sequence polarization.

A system is nonhomogeneous when the source and line impedance angles are not the same. In a nonhomogeneous system, the angle of the total current in the fault is different from the angle of current measured at the relay. For this case, the CDF is no longer a scalar quantity but has a phase angle as well. For a bolted fault (a condition that assumes no resistance in the fault), a difference between the fault current angle and the current angle measured at the relay is not a problem. However, if there is fault resistance, the difference between the fault and relay current angles can cause a ground distance relay to severely underreach or overreach.

Figure 4.40 shows that we can represent the phase voltage measured by a relay at Bus S as the sum of two voltage drops: the voltage drop across the transmission line ground loop impedance and the voltage drop across the fault resistance. Equation 4.74 gives the sum and definitions of these two voltage drops with the various terms as defined by Equation 4.69.

$$\text{Va} = \text{V}_\text{L} + \text{V}_\text{F} \text{ where } \text{V}_\text{L} = \text{m} \cdot \text{ZL1} \cdot \left(\text{Ias} + \text{k}_0 \cdot \text{Ir}\right)$$
$$\text{and } \text{V}_\text{F} = \text{R}_\text{F} \cdot \text{I}_\text{F} \qquad \text{Equation 4.74}$$

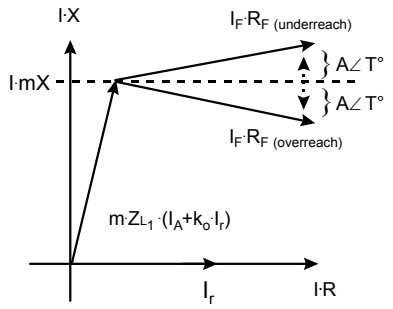
Figure 4.42 shows a voltage diagram for a resistive fault on a homogenous or radial system.



When the system is homogeneous or radial, the voltage drop across the fault resistance is purely resistive and in phase with the polarizing current I_r. The $R_F \bullet I_F$ term is effectively removed from the reactance element measurement.

Figure 4.42: Voltage Vector Diagram for a Resistive Fault in Homogeneous or Radial System

When the system is nonhomogeneous, the voltage drop across the fault resistance is no longer in phase with the polarizing quantity (in this case the zero-sequence current at Bus S in Figure 4.40). Figure 4.43 illustrates the voltage vectors for a resistive fault in a nonhomogeneous system.



In a nonhomogeneous system, the voltage drop across the fault resistance includes both real and imaginary terms. The imaginary part can cause the reactance element to overreach or underreach. The reactance element error is defined as A∠T°.

The reactance element will:

Underreach - If I_F leads I_r

Overreach - If I_F lags I_r

where I_r is the polarizing quantity for the reactance element.

Figure 4.43: Voltage Vector Diagram for a Resistive Fault in a Nonhomogeneous System

As Figure 4.41 illustrates, the total zero-sequence current in the fault is a function of the contributions from the source behind Bus S, the source behind Bus R, and the location of the fault on the line. Figure 4.43 shows that the tilt in the voltage drop across the fault resistance causes an error in the reactance element measurement. The difference of the fault current angle and reactance element polarizing referencing angle determines the degree to which the voltage across the fault resistance tilts. The reactance element measurement error is then a function of the ratio of the total zero-sequence fault current to the zero-sequence current measured in the relay. Equations 7 and 8 show two different methods for calculating the error term shown in Figure 4.43.

The error term calculated in Equation 4.75 is with respect to a relay at Bus S. Derive the expression in Equation 4.77 starting with Equation 4.74. Calculate the reactance measurement error using Equation 4.78, data available in a fault study, and the relay settings. Knowing the reactance measurement error caused by fault resistance allows the protection engineer to properly set the reach on a quadrilateral reactance element to prevent overreaching and underreaching.

$$A\angle T^\circ = \left[\frac{(Zs_0 + Zr_0 + ZL_0)}{((1-m)ZL_0 + Zr_0)}\right] = \frac{I_2 total}{I_2 local} \qquad \text{Equation 4.75}$$

$$A\angle T^\circ = \left[\frac{(If_0)}{(Is_0)}\right] \qquad \text{Equation 4.76}$$

$$\frac{Im\left(V\phi \cdot \overline{(Ir)}\right)}{Im\left(1\angle ZL_1 \cdot \overline{(I\phi_S + k_0 \cdot Ir)} \cdot \overline{Ir}\right)} = m \cdot |ZL_1| + R_F \cdot \frac{|Ir|^2 \cdot |A| \cdot \sin(T)}{Im\left(1\angle ZL_1 \cdot \overline{(I\phi_S + k_0 \cdot Ir)} \cdot \overline{Ir}\right)} \qquad \text{Equation 4.77}$$

$$\Delta X = R_F\left[\frac{|Ir|\cdot|A|\cdot\sin(T)}{\left(|I\phi\cdot\sin(\angle ZL_1+\angle I\phi-\angle Ir)+|k_0|\cdot Ir\sin(\angle ZL1+\angle k_0)\right)}\right] \quad \text{Equation 4.78}$$

A theoretical approach to calculating A∠T° is to use Equation 4.75. However, this method is more complex and requires calculating the zero-sequence source impedance at each end of the line. A simpler approach is to divide the total zero-sequence fault current by the zero-sequence current seen by the relay. It is easy to calculate the A∠T° term shown in Equation 4.76 from data available in a fault study. In some fault studies, the zero-sequence current is expressed in terms of $3\cdot I_0$. Calculate the error term shown in Equation 4.78 using $3\cdot I_0$ current, providing that the numerator and denominator terms are consistent.

The previous discussion provides the development of the term, e^{jT}, in Equation 4.79 through Equation 4.82. Compensate for nonhomogeneous systems with T defined in Equation 4.82. See section 4.3.3.4.1 for additional details on how to determine this compensation factor. For comparative purposes, Figure 4.44 plots the errors for RF from Equation 4.79 and X1 from Equation 4.80 as a function of per-unit fault distance from the relay.

$$R_F = \frac{\mathrm{Im}\left(Va\cdot\overline{\left(ZL_2\cdot Ia_2\cdot e^{jT}\right)}\right)}{\mathrm{Im}\left(Ia\cdot CDF_2\cdot\overline{\left(ZL_2\cdot Ia_2\cdot e^{jT}\right)}\right)} \quad \text{Equation 4.79}$$

where Ia_2 is the negative sequence current

$$X1 = \frac{\mathrm{Im}\left(Va\cdot\overline{\left(Ia_2\cdot e^{jT}\right)}\right)}{\mathrm{Im}\left(Ia\cdot\angle ZL_2\cdot\overline{\left(Ia_2\cdot e^{jT}\right)}\right)} \quad \text{Equation 4.80}$$

$$X1 = \frac{\mathrm{Im}\left(Va\cdot\overline{\left(Ir\cdot e^{jT}\right)}\right)}{\mathrm{Im}\left(Ia\cdot\angle ZL_2\cdot\overline{\left(Ir\cdot e^{jT}\right)}\right)}, where\ Ir = Ia + Ib + Ic \quad \text{Equation 4.81}$$

$$T = \arctan\left[1+\frac{\left(Zs_2\cdot m\cdot ZL_2\right)}{\left(Zs_2+(1-m)ZL_2+Zr_2\right)}\right] \quad \text{Equation 4.82}$$

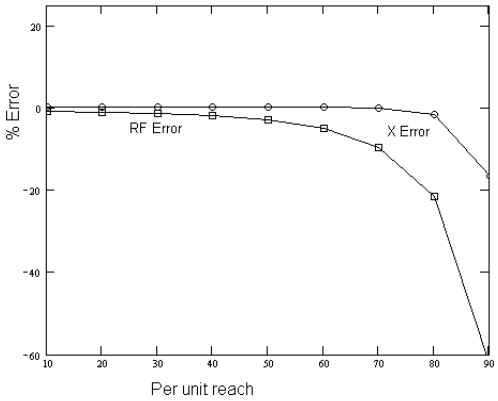


Figure 4.44: Error Sensitivity of Quadrilateral Apparent Reach, X and RF, as a Function of Reach for 20 Percent Phase Shift for the Source Impedances From the Line Impedance

Correcting the polarizing reference in the ground reactance calculation by the angle calculated in Equation 4.75 or Equation 4.76 can prevent overreach of Zone 1 elements. Adjusting the polarizing reference is equivalent to setting the variable 'T' in Equation 4.77 and Equation 4.78 to zero, thus removing the error introduced by the fault resistance voltage drop. Most relays with a quadrilateral element have a fixed angle; some relays provide a setting for adjusting the polarizing reference angle with respect to the system.

Reducing the Zone 1 reactance reach by the fault-resistance-induced error calculated in Equation 4.78 can also prevent overreach on external faults. The fault-resistance-induced error is a function of the magnitude of fault resistance in the fault. Use the Zone 1 resistance reach setting to calculate the worst-case fault-resistance-induced error. By limiting the Zone 1 resistive reach, the amount of reactance element overreach caused by fault-resistance-induced error is also reduced. Conversely, increasing the resistive reach allows the Zone 1 element to detect higher resistance faults and increases the potential of reactance element overreach for external faults.

4.2.5.5.1.1 Calculating Reactance Reach as a Function of Resistive Reach

The elements described by Equation 4.69 and Equation 4.70 are phase angle comparators. For the reactance element described by Equation 4.70, when the angle between the polarizing quantity (I_R) and the line-drop-compensated voltage $(Z_{1L} \bullet (I_A + k_0 \bullet I_R) - V)$ is 0°, the impedance is on the reactance element boundary. This element must measure line reactance without under- or overreaching from the affects of load flow or fault resistance. Hence, the element must use an appropriate polarizing current: negative- and zero-sequence currents are suitable choices. In some nonhomogeneous systems, the tip produced by the polarizing current may be insufficient to prevent overreach. To compensate for this nonhomogeneity, we introduce polarizing current angle bias (tip) or reduce the reach of the Zone 1 element.

Reducing the Zone 1 reach restricts that portion of the line protected by overlapping instantaneous Zone 1 protection. This overlapping zone is only achieved for low-resistance faults. A large resistive reach can limit the reactance element reach when

the instrumentation angle errors are considered. If the quadrilateral ground distance elements are the only Zone 1 protection, then we strike a balance between overlapping zones for midline faults, and large resistive coverage by one terminal for close-in faults.

Specifically, the instrumentation angle errors we consider are those caused by current transformers (CTs), voltage transformers (VTs), and the measuring relay. For this example, the values of these angles are: CT = 1°, VT = 2°, Relay Measurement = 0.2°

Assume that Relay R, shown in Figure 4.45, is a quadrilateral relay. For a ground fault outside of the protected zone with a reach *m* or *m XI* of Equation 4.70, the maximum secure reactive reach is a function of the expected resistive reach coverage for R_F of Equation 4.69. By observing Figure 4.45, we see that the two angles can be defined by Equation 4.83 and Equation 4.84.

Error! Objects cannot be created from editing field codes. Equation 4.83

Error! Objects cannot be created from editing field codes. Equation 4.84

To determine the maximum secure reach we must solve for m, as shown in Equation 4.85, using Equation 4.86.

$$\frac{m \cdot X_L}{R} = \tan(\theta_1 - \varepsilon) = \tan\left(\tan^{-1}\left(\frac{X_L}{R}\right) - \varepsilon\right) \quad \text{Equation 4.85}$$

$$m = \frac{R}{X_L} \cdot \tan\left(\tan^{-1}\left(\frac{X_L}{R}\right) - \varepsilon\right) \quad \text{Equation 4.86}$$

For $R >> X_L$, $\tan^{-1}(X_L/R)$ and $\tan(X_L/R) \cong X_L/R$. This approximation nets an error less than 5 percent for $X_L/R > 2.5$. Assuming the protected system is homogeneous (i.e, the only angular errors we must account for are those of the CT, VT, and relay), $\varepsilon = 3° \cong 1/20$ radians. These simplifications result in Equation 4.87.

$$m = \frac{R}{X_L}\left(\left(\frac{X_L}{R}\right) - \varepsilon\right) = \left(1 - \frac{R \cdot \varepsilon}{X_L}\right) = \left(1 - \frac{R}{X_L \cdot 20}\right) \quad \text{Equation 4.87}$$

Equation 4.87 shows that the lower the resistive reach, the greater the permissible reactance reach. Figure 4.46 shows a graph of allowable resistive to reactive reach ratio for $\varepsilon = 1/20$ radians (3°). The dashed line in this figure shows an example where an R/X_L ratio = 8 (for a 1-ohm line and an 8-ohm resistive reach) permits setting m = 0.6 per-unit of the line.

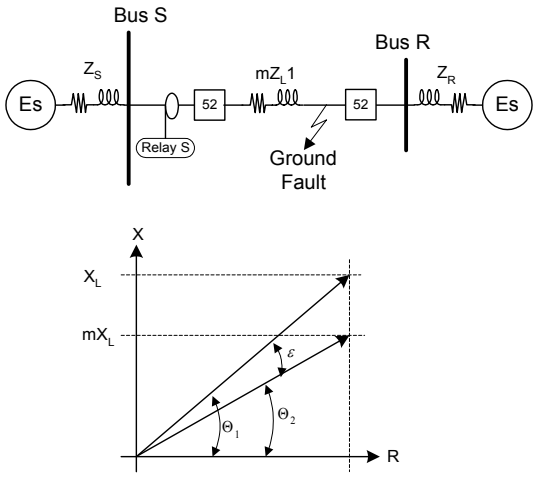


Figure 4.45: System Single-Line and First Quadrant of the Quadrilateral Distance Characteristics at Source S

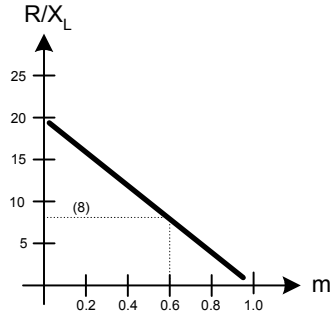


Figure 4.46: Increase Reactance Reach by Decreasing Resistive Reach for ε = 0.05

4.2.5.5.1.2 Advantages of quadrilateral ground distance elements

The advantages in using quadrilateral ground distance elements are:

- more fault resistance coverage than the mho element when properly designed [14]
- high-speed tripping of resistive faults when a pilot channel is not present
- fairly immune to in-line load switching
- good for cable protection

4.2.5.5.1.3 Complications of quadrilateral ground distance elements

The complications in using quadrilateral ground distance elements are:

- affected by errors in the current and voltage measurements when the resistive reach is much greater than the reactive reach

- affected by system non-homogeneity (i.e., unequal source and line impedance angles) [5,16]
- affected by zero-sequence mutual coupling in parallel lines

4.1.1.5.2 Phase Fault Quadrilateral Fault Detection

For cases when a quadrilateral relay is required on one segment, such as Bus S shown in Figure 4.47, and not on others, such as Bus R or T, it might be tempting to mix quadrilateral and mho distance relays. Doing so can lead to relay coordination problems. Even though the line may not be normally connected as a radial line, looped lines become radial from either operational switching or fault switching. Using a quadrilateral ground relay at Bus S may dictate that the phase element at Bus R be a quadrilateral element as well.

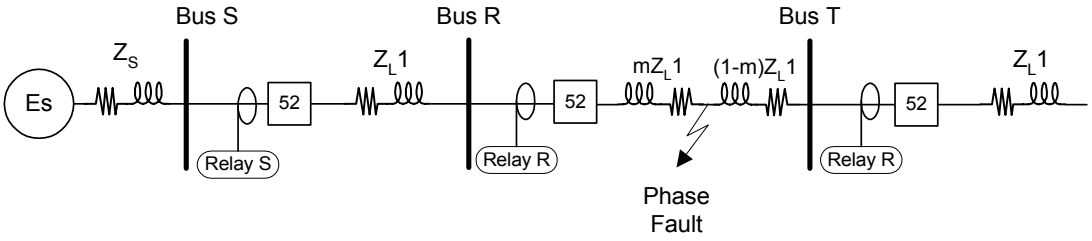


Figure 4.47: Radial System Employing Mho and Quadrilateral Distance Relays

The coordination problem arises when using Zone 2 of the Bus S relay to provide 100 percent coverage of the line and possibly backup protection for a portion of the line between Bus R and T as shown in Figure 4.48. For a fault in Bus R, Zone 2, the memory of the polarizing signal causes the zone coverage to expand back towards the source. Zone 2 delay causes the memory of the polarizing signal to diminish, which causes the Zone 2 coverage to shrink, as shown in Figure 4.48. After the memory has fully expired, a region in Zone 2 of the relay at Bus S has fault coverage that the relay at Bus R does not. Figure 4.48 shows this region as a dark shaded area at the upper right of Zone 2. One possible solution is to restrict the resistive reach at Bus S until that area disappears, but doing so adversely affects the desired Zone 2 coverage between Bus S and Bus R. Relay coordination is simplified if the shapes of the zones are similar, so the relay at Bus R should also be quadrilateral.

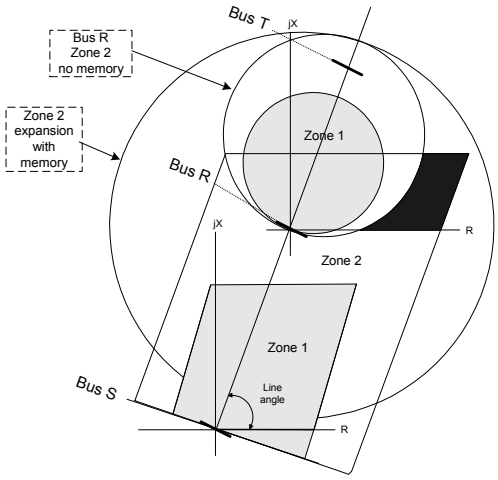


Figure 4.48: Overlapping Quadrilateral and Mho Relay Zones of Protection

Referring to Figure 4.49 and writing the two loop equations for a phase-B-to-C fault results in Equation 4.88 and Equation 4.92. Subtracting these two equations results in a single equation for the phase-to-phase voltage, Equation 4.90. Equation 4.91 is the simplified phase-to-phase voltage expression using phase domain impedances while Equation 4.92 uses symmetrical component impedances.

$$Vb = Ib\,m(Zs) - V_M ab - V_M cb + Vf^+, \text{ where } Vf^+ = Ib \cdot R_F/2 \qquad \text{Equation 4.88}$$

$$Vc = Ic\,m(Zs) - V_M bc - V_M ac + Vf^-, \text{ where } Vf^- = Ic \cdot R_F/2 \qquad \text{Equation 4.89}$$

$$Vbc = (Ib - Ic)mZs - m\,Zm\,Ic + m\,Zm\,Ib + \left(Vf^+ - Vf^-\right) \qquad \text{Equation 4.90}$$

$$Vbc = Ibc\,m(Zs - Zm) + Ibc\left(R_F/2\right), \text{ where } \frac{(Ibc\,R_F)}{2} = \left(Vf^+ - Vf^-\right) \qquad \text{Equation 4.91}$$

$$Vbc = Ibc\,m\,Z1 + Ibc\left(R_F/2\right), \text{ where } Z1 = Zs - Zm \qquad \text{Equation 4.92}$$

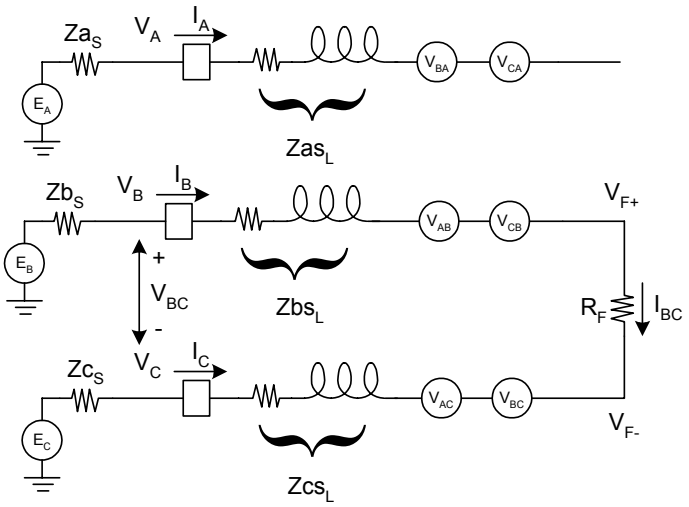


Figure 4.49: Phase-to-Phase Fault on a Radial Feed System

Extending the results of Equation 4.92 to the network shown in Figure 4.50, we can derive expressions for the fault resistance RF and the reactance X1, as shown in Equation 4.93 and Equation 4.94. These are valid for radial lines where the switches at V_{RB} and V_{RC} are open or the fault resistance is zero. If infeed from source R is possible and R_F is non-zero, a relay at Vs can no longer measure the total fault current, so the loop equation suggested in Equation 4.92 is no longer valid. For this case, the negative-sequence current provides both a means to approximate the total fault current and provide a high degree of immunity zone expansion and contraction caused by load current that is illustrated in Figure 4.32.

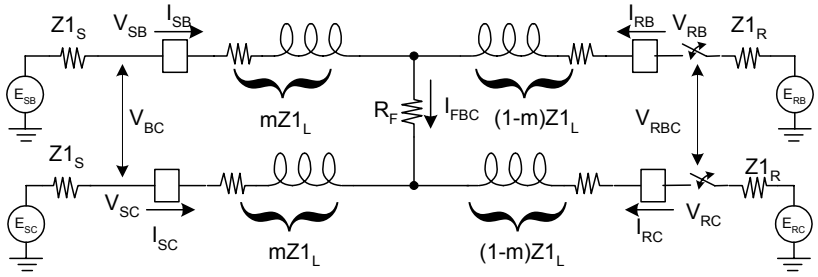


Figure 4.50: Loop Diagram for Phase-to-Phase Faults

$$R_{AB} = \frac{\mathrm{Im}\left(Vab \cdot \overline{(ZL1 \cdot Iab)}\right) \cdot 2}{\mathrm{Im}\left(Iab \cdot \overline{(ZL1 \cdot Iab)}\right)}$$ Equation 4.93

$$X1 = \frac{\mathrm{Im}\left(Vab \cdot \overline{(Iab)}\right)}{\mathrm{Im}\left(Iab \cdot \angle ZL1 \cdot \overline{Iab}\right)}$$ Equation 4.94

Using the techniques involving the negative-sequence impedance plane, we can derive equations for elements that provide a high degree of fault resistance coverage and immunity to load current in the presence of infeed. The results are shown in Equation 4.95 through Equation 4.101, which describe the three possible loops for phase faults, an equation for R_F and X for each loop. Formal derivation of the

negative-sequence currents used in these equations is provided in Appendix 11.8, Equations **Error! Reference source not found.** to **Error! Reference source not found.**.

$$R_{AB}=\frac{\mathrm{Im}\left(Vab\cdot\overline{(ZL1\cdot Iab)}\right)}{\mathrm{Im}\left(ja^2\sqrt{3}Ia_2\cdot CDF2\cdot\overline{(ZL1\cdot Iab)}\right)}$$ Equation 4.95

$$R_{BC}=\frac{\mathrm{Im}\left(Vbc\cdot\overline{(ZL1\cdot Ibc)}\right)}{\mathrm{Im}\left(j\sqrt{3}Ia_2\cdot CDF2\cdot\overline{(ZL1\cdot Ibc)}\right)}$$ Equation 4.96

$$R_{CA}=\frac{\mathrm{Im}\left(VcA\cdot\overline{(ZL1\cdot Ica)}\right)}{\mathrm{Im}\left(ja\sqrt{3}Ia_2\cdot CDF2\cdot\overline{(ZL1\cdot Ica)}\right)}$$ Equation 4.97

$$CDF2=\frac{(Zs_2+ZL1+Zr_2)}{((1-m)\cdot ZL1+Zr_2)}$$ Equation 4.98

$$X1_{AB}=\frac{\mathrm{Im}\left(Vab\cdot\overline{(ja^2Ia_2)}\right)}{\mathrm{Im}\left(Iab\cdot\angle ZL1\cdot\overline{(ja^2Ia_2)}\right)}$$ Equation 4.99

$$X1_{BC}=\frac{\mathrm{Im}\left(Vab\cdot\overline{(jIa_2)}\right)}{\mathrm{Im}\left(Ibc\cdot\angle ZL1\cdot\overline{(jIa_2)}\right)}$$ Equation 4.100

$$X1_{CA}=\frac{\mathrm{Im}\left(Vab\cdot\overline{(ja\cdot Ia_2)}\right)}{\mathrm{Im}\left(Ica\cdot\angle ZL1\cdot\overline{(ja\cdot Ia_2)}\right)}$$ Equation 4.101

4.1.1.6 Comparison of Relaying Schemes

The following comparisons provide some general application rules for deciding which relaying approach to use for different kinds of network configurations. Protection is rarely so simple and straightforward as to lend itself to a few rules of thumb but general guides can indicate the right direction.

4.1.1.6.1 Distance Versus Overcurrent [6065][40]

The major advantage of distance relays is that the zone of operation is a function of the protected line impedance, which is a constant, and is relatively independent of the current and voltage magnitudes. The distance relay has a fixed reach, unlike overcurrent relays for which the zone of protection varies with changes in the source impedance.

One difficulty with mho ground distance relays is their inability to detect high-resistance faults. The voltage measured by the relay is the sum of the line voltage drop to the fault and the voltage drop across the fault resistance. Current infeed from the other line terminal can change the voltage drop across the fault resistance. On a radial system (single source systems) there is no infeed from another line terminal and the distance relay measures the actual fault resistance. On looped transmission systems there is usually more than one source of current feeding the fault; therefore,

the infeed from another line terminal acts as a fault resistance amplifier. The amplifier effect is a function of total current in the fault and the current supplied from the relay terminal. As the total fault current increases with respect to the relay current, the apparent fault resistance also increases.

4.1.1.6.2 Mho Versus Quadrilateral

The mho characteristic is popular because it has a well-defined reach, is inherently directional within limited reach constraints, and can tolerate fault resistance quite well without serious overreaching errors from load or unequal source and line impedance angles. Under strong source conditions, a quadrilateral characteristic can provide greater fault resistance coverage than the dynamic characteristic of the mho element. Section 4.1.1.4 discusses this dynamic characteristic.

Mho distance relays have dynamic and/or variable characteristics that depend on the polarizing quantity, fault type, and system parameters. The mho ground relay offers a desirable balance between fault resistance accommodation on internal faults and security against misoperation on external faults. By comparison, the quadrilateral relay provides good fault resistance coverage, but experiences reduced security on remote faults because of unequal source and line impedance angles for these same resistive faults. We discussed the effect of unequal source and line angles on a quadrilateral element earlier in this chapter.

4.1.2 Pilot Protection

The protection zone concept is a compromise between overtripping and slow tripping. To keep relays from overreaching their primary zone of protection, faults are discriminated on the basis of current or impedance. This discrimination must account for inaccuracies in measurements and calculations. Hence, the primary zone only reaches 80 percent to 90 percent of the line being protected. The backup zone is responsible for clearing faults in the second zone of protection and must be delayed to allow coordination. This leaves 20 percent to 40 percent of the line that has faults cleared by Zone 2 delayed tripping. The importance of the line or the need to remove faults quickly justifies the expense for communications systems to allow tripping faster tripping than Zone 2 normally permits. The goal of pilot systems is to treat all terminals of the line as a single unit and to clear internal faults at Zone 1 speeds. This accelerated tripping is available if each terminal supplies a signal to all other terminals of the line. The advantages offered by pilot systems are as follows:

- Safeguard system stability by:
  - clearing a higher percentage of the faults at higher speeds
  - allowing the use of high-speed reclosers
- Improve power quality by:
  - reducing the duration of power sags
  - allowing longer coordination time intervals to reduce the number of out-of-zone trips
- Reduce damage to equipment by shortening the time that equipment must carry fault current

4.1.2.1 Classification of Pilot Systems

4.1.2.1.1 Channel Use

In general, the channels for communicating signals for relaying purposes are called pilot channels. Pilot systems that delay or inhibit tripping are called blocking systems. Pilot systems for tripping action are called tripping systems.

4.1.2.1.2 Fault Detectors

Fault detectors determine the presence or absence of a fault or otherwise abnormal system condition. Directional comparison schemes measure the fault or power flow direction. Each line-end relaying system sends a signal to the other line-end relaying systems to indicate the relative direction of the fault for that relay.

Another fault detection principle is phase comparison, where each relay detects faults by comparing the phase of the current. The polarization of currents at all terminals is such that positive current indicates current into the line. Summing the currents from all terminals results in zero unless the fault is internal to the zone of protection. Ideally, this summation of currents is zero but allowances are required for instrumentation inaccuracies and communications channel delays.

Traveling wave relays use yet another principle, transmission line theory, discussed in section 0, to detect faults. Faults generate high-speed signals that emanate away from the fault. Wide bandwidth communications is necessary to provide the ultra high-speed communications required by this approach. Section 4.2.8 further discusses this type of relaying.

4.1.2.1.3 Communications Media

Usually, relays are expected to operate autonomously and provide effective protection when needed without dependence on remote information. Added information provided by communications most often results in improved performance whether that is speed, reliability, security, or selectivity. The type of communications chosen for a particular relaying scheme depends on the degree of need for pilot relaying. Tripping pilot schemes require more dependable communications than do blocking schemes when reliability is more important than security. A paper by Schweitzer and Kumm provides an extensive review of statistical requirements for the various types of pilot relaying.[41]

Both direct analog signals and modulated signals communicate pilot signals. Direct signals are low voltage 50-60 Hz ac or dc voltages or currents and require direct electrical continuity between terminals. For ac signals, isolation transformers can block currents resulting from ground potential rise generated by faults at one of the terminals.

Modulated signals communicate information indirectly about the signals at each terminal. These modulated signals may be RF or audio depending on the media used for communications. Use audio tones to signal over any media than allows audio signals. The information is restricted to binary, which modulates the audio tones on and off (a type of amplitude modulation) or frequency shift keying (FSK a type of

FM). This requires wider bandwidths so discriminators can detect the presence or absence of a tone for key tone systems or to distinguish between two tones. If speed requirements permit, communications schemes use multiple tones on single audio channels. Modulation schemes can be digitally encoded and sent over fiber optics, digital and analog microwave, spread spectrum radio, or narrow band RF radio.

4.1.2.1.3.1 Pilot Wires

Pilot wire generally refers to a twisted pair of metallic conductors used for transmitting low voltage 50-60 Hz ac or dc signals between terminals. Typically, use privately-owned overhead or underground cables for security reasons, although you can also use public telephone circuits. The wire resistance restricts the distance between terminals.

4.1.2.1.3.2 Power Line Carrier (PLC)

The technology of using power lines for communications derives its name from the fact that the original signals were considered unmodulated RF carrier. As Figure 4.51 shows, a coupling capacitor that can also be used for potential metering (see section 0) couples the RF signal to one or more phases of the power line. Wave traps provide signal isolation and raise the terminal RF impedance in the presence of high bus capacitance.

Today, PLC communications can provide single or dual frequency keyed carrier or tones. Multiple audio channel systems use a broad spectrum for voice, and tone telemetry and relaying. Typically PLC communications operate using the frequency range of 30 to 300 KHz. Recently marketed industrial and home automation products use commercial and residential voltages at 120 to 480 volts ac. Narrow band phase shift keying (PSK) and spread spectrum technology are the two predominate types of modulation for these applications.

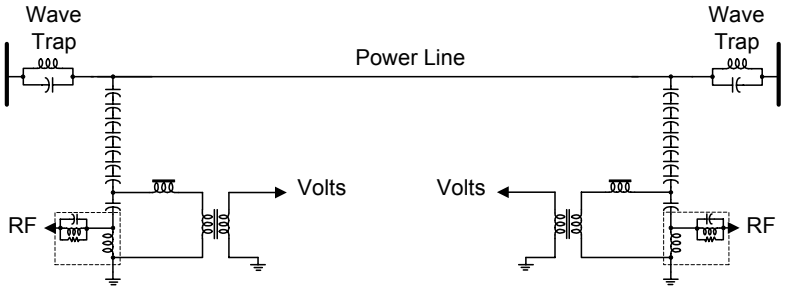


Figure 4.51: Typical RF Connection for PLC

4.1.2.1.3.3 Microwave

As early as the 1950s electric utilities began using microwave for voice, data telemetry, and relaying. The FCC allocated frequency bands for electric utilities that range from 1.9 to 6 GHz. Transmitter-receiver pairs must have unobstructed line of sight between them. Effective microwave path lengths are usually less than 100 miles because of attenuation and earth curvature. Active repeaters receive and retransmit the signals. Passive repeaters are like giant mirrors that bounce the microwave beams. Microwave communication is adversely affected by multipath

deflection because of thermal layers in the air, just like the mirages seen on hot pavement. Severe rain and snow showers can absorb the microwave energy and disrupt communication.

Microwave systems support multiple audio channels depending on the microwave frequency being used. The two microwave technologies in use today are digital and analog. Digital systems are replacing analog systems because digital systems can communicate more information using less microwave spectrum with greater noise immunity.

Microwave systems divide the bandwidth into 4 KHz analog audio channels or 8 KHz digital audio channels. The effective analog audio channels or equivalent digital channels have a usable voice band restricted to 300 to 3600 Hz. This allows the necessary filtering to provide good separation between adjacent audio channels. The spectrum beyond the voice band is used for signaling and in some instances for telemetry.

4.1.2.1.3.4 Fiber Optics

Fiber optic systems operate the same way as digital microwave except they use frequencies just under the visible light spectrum. The advantage they offer over microwave communication is broader spectrums, lower susceptibility to atmospheric disturbances, and no need for FCC licensing. Electric utilities today are capitalizing on existing right-of-way by installing fiber optic lines either in or wrapped around shield wires or phase conductors.

4.1.2.2 Directional Comparison Relaying

The most widely used pilot protection system is directional comparison. An IEEE survey published in 1988 [42] showed that about 80 percent of the important lines in 116 utilities have directional comparison protection. The main reasons for this wide acceptance are the low channel requirements and the inherent redundancy and backup of directional comparison systems. Directional comparison schemes measure the direction of a detected fault. If it is determined to be into a line between two relays, both relays will trip. The primary function of the directional unit in a relay is not to detect the presence of a fault, but to detect the direction of the fault relative to that relay without respect to fault distance or magnitude. This information is communicated to the relay at the opposite end of the line, which then makes decisions based on the directional information. As Figure 4.52 shows, the Zone 2 distance element typically detects forward faults not detected by underreaching as the Zone 1 element set underreaches the end of the line. Zone 3 distance elements detect reverse faults. It is important to remember that the sensitivity of the Zone 3 element for Relay 3 should be set to see further to the left of Bus A than does the Zone 2 element of Relay 4. Otherwise Relay 4 will trip unnecessarily for out-of-section faults.

The primary difference between the various directional comparison schemes is the way in which the relays use the information from the other terminal. Always remember that these schemes are rarely used alone, but are an application of protection overlaying conventional distance or time-overcurrent protection.

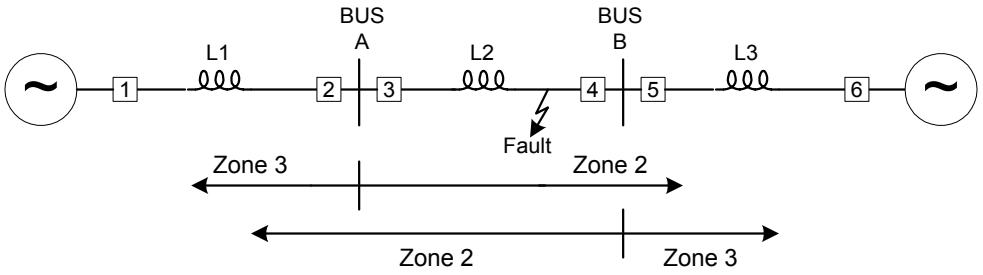


Figure 4.52: Example Single-Line Diagram for Relay Coordination

4.1.2.2.1 Permissive Overreaching Transfer Trip (POTT)

POTT schemes implement the logic shown in Figure 4.53. Each relay protecting the line has identical logic. Since the Zone 2 trip output requires an enable from a receiver output, the scheme is considered a tripping scheme. This improves performance speed for faults detected by Zone 2 elements because the relay operates as soon as an enabling signal is received for the remote terminal.

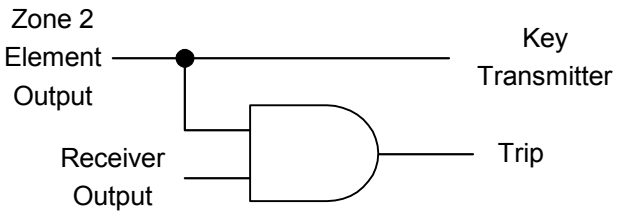


Figure 4.53: POTT Tripping Logic

There are, however, inherent reliability weaknesses in POTT. The line will not execute high-speed tripping for Zone 2 faults if the signal from the remote end is not received. Channel failure or relay failure to detect the fault at the remote end can cause this signal failure. This can also occur if the breaker is open at the remote terminal. If the source is weak behind the remote terminal, the local relay can fail to trip high speed or at all. Such applications require weak infeed logic to reliably detect in-section faults.

4.1.2.2.1.1 Current Reversals

If the line being protected is a parallel line, as shown in Figure 4.54, POTT schemes are subject to security problems. Consider a case where Line #1 has POTT and a fault occurs as shown. Initially, the directional elements correctly identify the fault direction. Breaker 3, which detects the fault in Zone 1, will open first and breaker 4 must wait for the communications-delayed signal. The relay at breaker 1 detects the fault in Zone 3 but is receiving an enable signal from terminal 2. After breaker 3 opens, the relay at terminal 1 may see the fault in Zone 2 depending on the strength of the source behind Bus B. If the delay time for the terminal 2, Zone 2 dropout plus the channel delay to terminal 1 is slower than the terminal 1, Zone 2 pickup, breaker 1 will trip incorrectly.

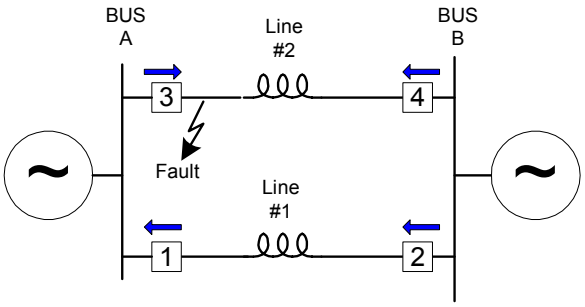


Figure 4.54: POTT Schemes Applied to Parallel Line Cases

Figure 4.34 shows the additional logic to prevent the current reversal problem just described. This logic blocks both the transmitter key and the trip output for a specified delay time after the Zone 3 element drops out. The keying and tripping are also inhibited for delay time, T1, if all three poles of the breaker are open. Figure 4.56 shows a time diagram describing this sequence.

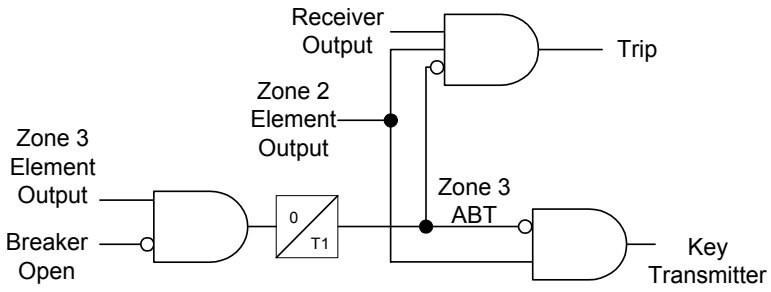


Figure 4.55: Current-Reversal Blocking Logic

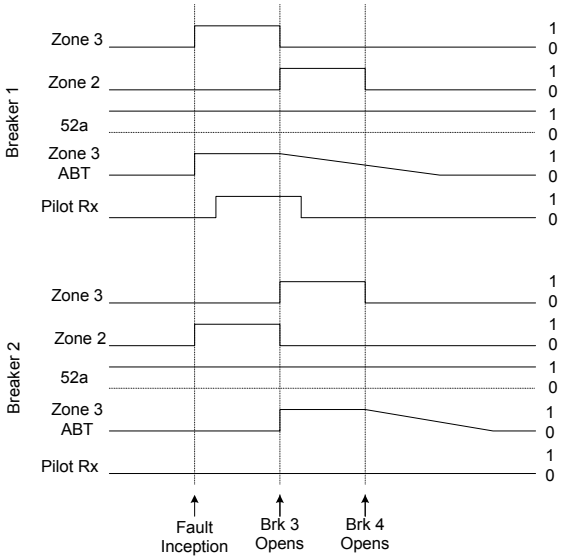


Figure 4.56: Current-Reversal Timing Sequence

4.1.2.2.1.2 Remote End Open

Sometimes the objective is to high-speed trip 100 percent of the line. Consider a case when the line is energized from the local end and the source behind the remote relay is very weak or the remote end is completely open. Without a source behind the relay at the remote end, the relay will never detect a fault no matter how close it is. However, you can still key the local relay to trip high-speed if the remote end immediately echoes the carrier. One method is to use the 52b contact to transmit continuous permission from the relay where the breaker is open. This approach will not work if the other end requires a guard before operating unless overridden by communications equipment logic.

Figure 4.57 shows logic that provides an alternate approach. This logic requires that the Zone 2 element have been dropped out at least as long as the delay specified by T1 and that the turnaround logic be enabled. If these conditions are met and a signal is received, then the next timer delays the receiver output by time T2 to ensure the relay has time to assert its Zone 3 if appropriate. The final timer guarantees a minimum persistence of T3 for the receiver output once the delay time T2 has been satisfied. The last AND gate provides that the transmitter is keyed back to the remote end only if the Zone 3 element is not picked up. Preventing channel lockup once the loop-back has been completed requires additional logic.[43]

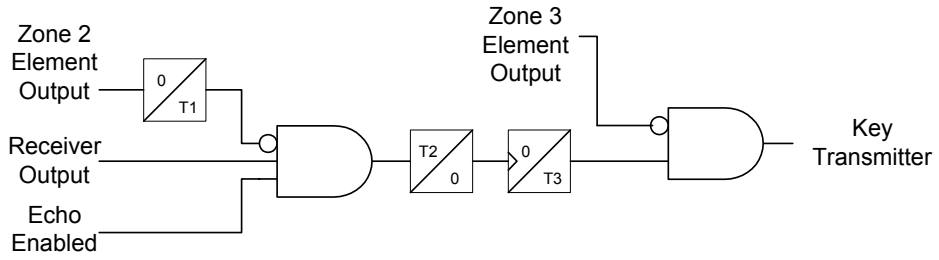


Figure 4.57: POTT Carrier Echo Logic

4.1.2.2.1.3 Weak Infeeds

If a strong infeed is radically weakened, the local relay may no longer detect a fault in Zone 1, if at all. The relay sensitivity can be improved using the logic shown in Figure 4.58 for weak infeed conditions. A phase voltage magnitude collapse or the presence of a large zero-sequence voltage indicates a possible fault condition. Figure 4.58 also shows that this logic must be enabled by a supervision input that set the relay to be sensitive to this condition. The requirement that all phases be closed prevents the relay from tripping from pole misalignment during normal breaker closing operations. Additional logic requires that the carrier signal has been present for time T2 and sustains the carrier output for time T3. The final requirement is that the relay Zone 3 element not be picked up. If all the conditions are satisfied, then the relay will trip high-speed even though other distance elements have not detected a fault.

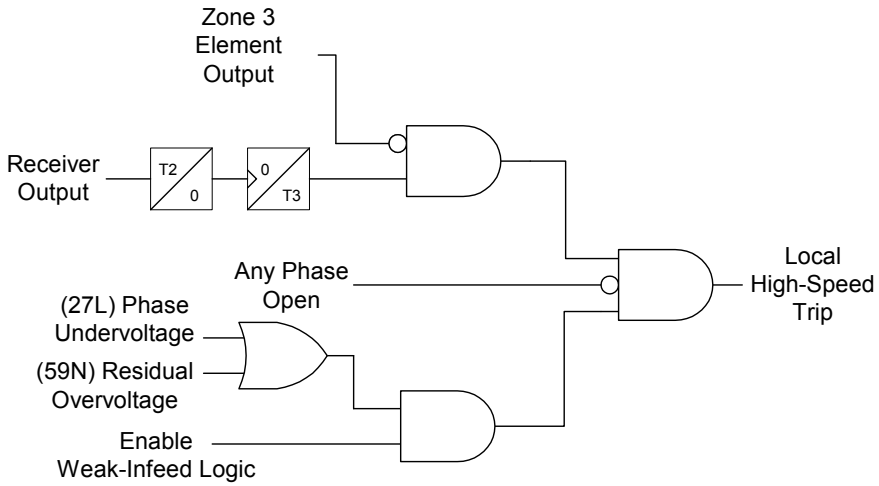


Figure 4.58: Weak Infeed Carrier Start Logic

4.1.2.2.1.4 Fault Tree for a Two-Terminal Line Protected by a POTT Scheme

Figure 4.59 shows a transmission line with a single circuit breaker and relay at each end. The two relays communicate through tone equipment and analog microwave gear to create a POTT scheme. Assume that the protection operates from a 125 Vdc battery, and the communications operate from a 48 Vdc battery.

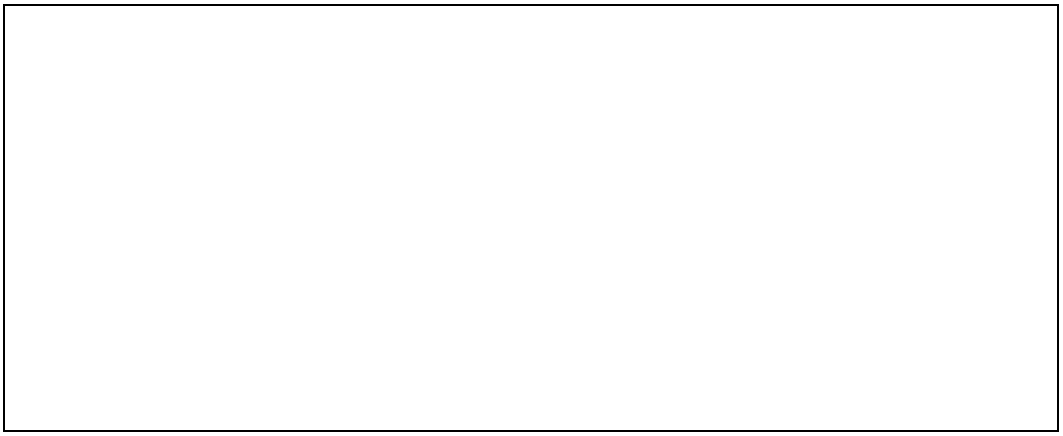


Figure 4.59: One-Line Diagram of a Tone/Microwave Based POTT Scheme

To construct a fault tree for this simple system, choose a top event of interest, such as "Protection Fails to Clear In-Section Fault in the Prescribed Time." We are interested in how each component contributes to the top event.

Figure 4.60 is a fault tree for the system in Figure 4.59 (see section 0). The fault tree contains only OR-gates, so we know that all devices must function properly to clear in-section faults. Later we will add some redundancy to reduce the number of single-point failures or devices that can singly cause the system to fail. We can use the fault tree to predict a system failure rate once we have some estimates of the device failure rates.

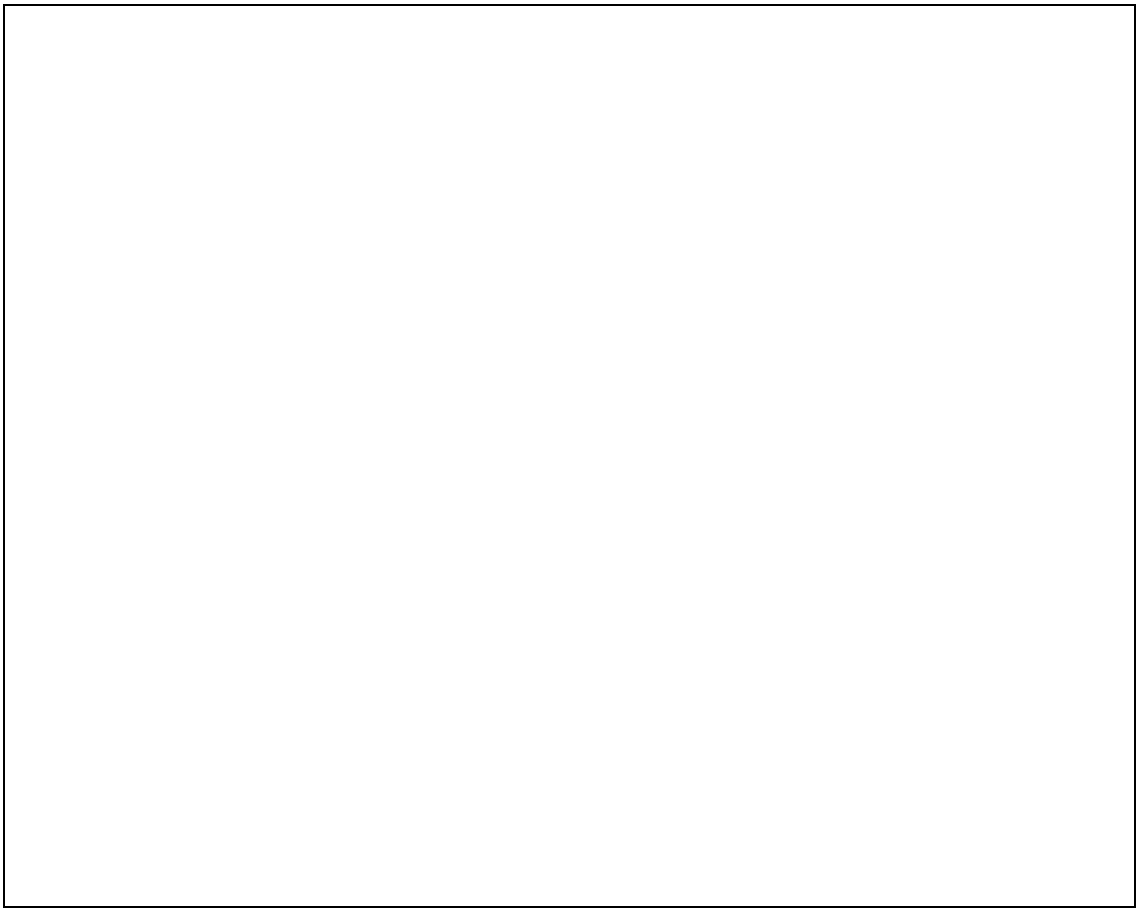


Figure 4.60: Fault Tree for System of Figure 4.59

4.1.2.2.2 Directional Comparison – Unblocking (DCUB)

The DCUB scheme can operate identically to the POTT schemes when the communications is functioning properly. This allows POTT schemes to be applied with communications system that can fail during faulted conditions such as power line carrier. This scheme assumes that the probability is extremely remote that a channel failure will occur simultaneously with external faults. The power line carrier is normally received to allow tripping. The only difference between the logic for the DCUB scheme shown in Figure 4.61 and the POTT scheme shown in Figure 4.53 is the addition of a delayed dropout on the received unblock signal. This delay allows tripping for time T1 after the signal is lost, allowing Zone 2 high-speed tripping during that interval.

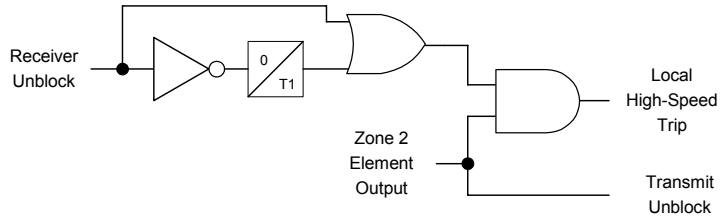


Figure 4.61: DCUB Tripping and Carrier Send Logic

When a communications media allows continuous transmission such as telephone lines or microwave, two separate signals are sent. One signal represents the blocking state and the other the unblocking state. This provides additional security because the relay knows when it is receiving a viable signal. The logic for this configuration, shown in Figure 4.62, has two timers associated with the loss of carrier signal. If the output from the time is low, then a valid carrier, either blocking or unblocking is present. Both delays provide a degree of noise immunity. For a loss of blocking signal without an unblocking signal, the scheme functions the same as the one shown in Figure 4.61. If an unblocking signal is received, then tripping is permitted for Zone 2 faults regardless of the condition of the blocking signal.

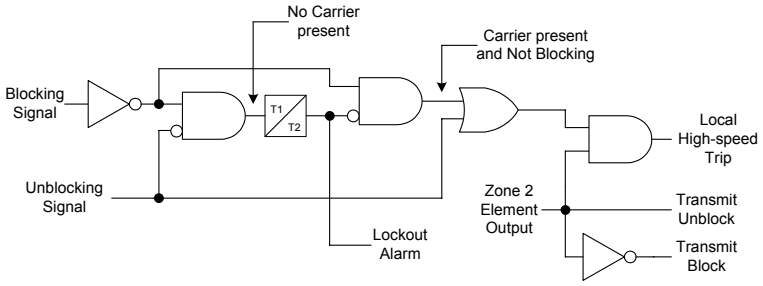


Figure 4.62: DCUB Logic With Carrier Supervision

4.1.2.2.3 Permissive Underreaching Transfer Trip – (PUTT)

Like POTT, PUTT is a tripping scheme. Figure 4.63 shows the logic for this scheme, which uses the Zone 1 element to key the transmitter. High-speed Zone 2 tripping only occurs if the fault is within the Zone 1 reach of the far terminal.

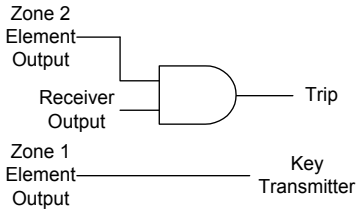


Figure 4.63: PUTT Logic

4.1.2.2.4 Directional Comparison Blocking – (DCB)

Blocking schemes rely on the absence of a blocking signal to inhibit tripping from the forward-reaching Zone 2 element. Delay the Zone 2 output, as shown in Figure 4.64, to allow time for the remote relay to generate the signal and the communications delays. Unblocking schemes favor reliability over security. If the remote end or the communications fails, tripping will still occur. The problem is that if the communications is slow or the remote end is long in sending the blocking signal, unnecessary Zone 2 operations may result.

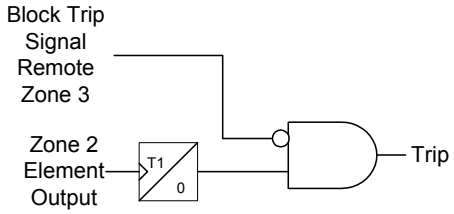


Figure 4.64: Delayed DCB Logic

4.1.2.2.5 Direct Transfer Trip

Transfer trip schemes provide high-speed tripping without condition and with little, if any, delay. Such schemes can maintain power system stability such as loss of generation far removed from larger quantities of concentrated load. An example of this is the Idaho Power system that had a single customer in eastern Idaho using as much as 250MW, yet the majority of power generation on the Idaho-Oregon border 350 miles to the west. If the power flow is east and a significant portion of the western Idaho generation is lost, then a signal is sent to trip the load and make up the lost generation. The difficulty with these load-shedding schemes is the logic to determine when the load tripping is advantageous, when it is a nuisance to the customer, and when it is detrimental to maintaining system stability.

Transfer tripping can also protect equipment. The scenario is similar in that the relay being tripped does not detect the fault, but the source of the transfer trip signal cannot otherwise clear the fault. The communications used with transfer tripping schemes must be both secure and reliable, with reliability being the greater of the two concerns. Some communications schemes provide for two independent paths where the probability of simultaneous communications failures is very remote.

4.2.6.2.6 Hybrid Communications-Aided Protection

A new communications-aided protection scheme might offer high-speed clearing of more faults while being as dependable and secure as each of the best of the existing communications schemes. Figure 4.65 shows the logic for this new protection scheme. While the channel is in service, the scheme can trip three different ways. The first way is when a fault is detected in Zone 2 for carrier coordination (CC) time if no Block Trip signal is received (traditional DCB). The second way is when a Permissive Trip signal is received, and the fault is not behind the terminal (DCB from perspective of remote end). And finally, a Direct Trip signal is received (saves 0.5 cycle for lower-resistance faults).

If the channel fails (Not Receive Okay, shown as Not Rx Okay in Figure 4.65), the relay logic blocks DCB logic (AND Gate 1) to maintain security. Relay logic then opens a 10-cycle tripping window (AND Gate 2) that allows tripping if the relay detects a forward fault. This improves dependability in instances where the channel fails as a result of the fault. A single reverse-blocking timer (RB) disables the permissive tripping logic and extends the Block Trip signal to provide security during current reversals.

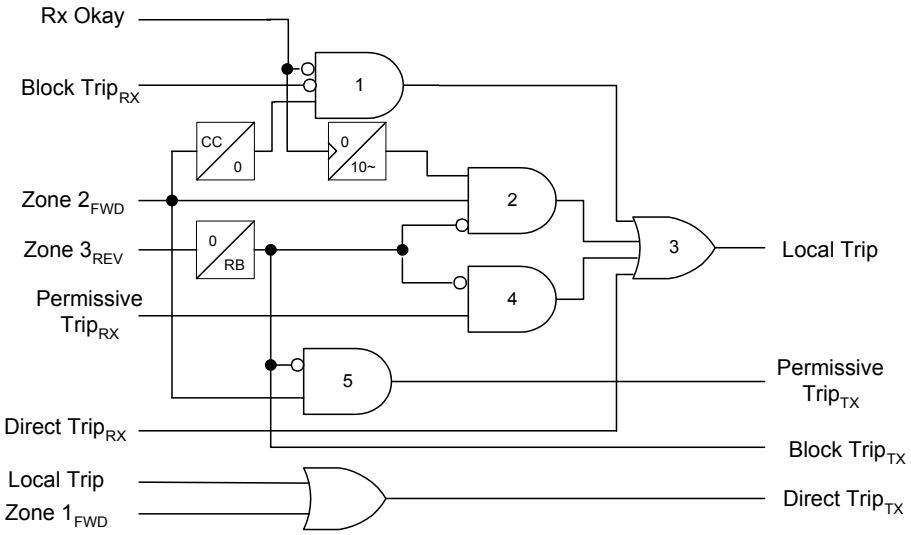


Figure 4.65: Hybrid Communications-Aided Protection Scheme

4.2.6.2.7 Comparison of Pilot Protection Schemes

Schweitzer presented a statistical comparison of four of the pilot protection schemes discussed in previous sections. Table 4.7 summarizes the performance of these communications-aided protection schemes on the criteria of overtrips per year and time-delayed trips per year (assuming a 100-line system), high-speed resistive-fault coverage, total resistive fault coverage, raw and normalized figures of merit, and complexity. The hybrid scheme offers marked advantages in terms of fault resistance coverage and operating speed, with no penalty on security or dependability. Scheme complexity is comparable to POTT schemes.

Table 4.7: Communications-Aided Protection Performance Summary, Long Lines

	Misoperations			**Rf Coverage, Operating Time Performance**					**Complexity**
Scheme	Over-trips per year	Time-Delayed Trips per year	Figure of Merit	High-Speed Rf Coverage Ω	Total Rf Coverage Ω	Fault Clearing Time, T_{ave} Cycles	Figure of Merit ρ_{TR}	Figure of Merit, Normalized ρ_{TRN}	Zones, Timers, & Logic
POTT	0.022	12.20	12.222	44	88	14.7	167 x 10^{-3}	3.1	5

DCB	0.380	0.33	0.710	44	88	7.4	84 x 10^{-3}	1.6	4
DCUB	0.022	0.33	0.352	44	88	14.7	167 x 10^{-3}	3.1	7
Hybrid	0.022	0.33	0.352	88	88	4.7	54 x 10^{-3}	1.0	5 (6)

Assumptions: Long Line, 1 percent probability of channel loss during a fault

4.1.2.3 Phase-Comparison Relaying

In spite of their popularity, directional comparison systems require voltage information, so they experience such problems as loss of potential for close-in faults or for blown fuses, ferro-resonance problems in voltage transformers, and transient response problems in capacitive-coupled voltage transformers. Phase-comparison schemes use analog information to convey direction of current flow alone. Current-only systems exhibit good performance in complex protection problems of transmission lines, such as evolving, intercircuit, and cross-country faults, mutual induction, power swings, and series impedance unbalance. Current-only systems are a good solution for series-compensated, three-terminal, and short transmission lines.

Synchronizing this information when it is received accounts for time delays in signal processing and communication. The information can be on a phase-by-phase basis, which requires three times the bandwidth, or a single composite representation of all three phases. It is not enough for communications channels to have the minimum band of the power system fundamental frequency for phase comparison schemes. If relay schemes are to have millisecond responses, then the bandwidths must be in the kilohertz range. Modern digital fiber-optic communications channels fulfill the requirements of current-only pilot protection systems. [44, 45]

Phase-comparison systems compare the phase of the currents at all line terminals. Early systems used a composite sequence network to form a single-phase voltage for phase comparison. [46, 47] Modern digital communications channels permit implementation of segregated phase-comparison systems that provide faulted phase identification and enhance the protection response to complex faults. [48, 49,50, 51]

Phase-comparison systems fail to detect internal faults with outfeed at one of the line terminals. Offset keying is an enhancement to phase comparison that adds magnitude information to the phase-comparison process in order to accommodate outfeed. However, offset-keying phase-comparison systems have sensitivity limitations for faults with low contributions at all line terminals. [52,53]

Current-differential protection combines phase and magnitude current information in a single comparison. Early line-differential protection systems used a pilot-wire channel to exchange analog information between the line terminals.[54] Modern systems typically exchange phasor current information on a digital channel or transmit the digitized raw samples.[55, 56] A basic limitation of traditional line current differential systems is the need to select the slope according to current transformer saturation. This single setting defines a relay characteristic having a given tolerance to channel time-delay asymmetry and outfeed. In other words, it is not possible to

address current transformer saturation, channel asymmetry, outfeed, and other problems with separate relay settings.

Charge comparison is an alternate form of current- differential line protection intended to reduce the communications channel requirements. Charge-comparison systems provide higher tolerance to channel asymmetry and outfeed than traditional current differential systems. However, the required zero-crossing detection introduces a half-cycle latency that penalizes speed and introduces additional time delay for internal faults with full dc offset. External faults with current transformer saturation that affect zero crossings may produce relay misoperations.

4.1.2.3.1 Pilot Wire Systems

Pilot-wire systems were some of the earliest pilot protection schemes working on the concept that the conductor is a single node where the summation of currents into that node must equal zero. If this is not the case, there must be a node between the two terminals that provides a path between conductors or to ground. As Figure 4.66 shows, pilot-wire systems use a single channel or pair of wires. The voltage produced by the sequence network is a function of the symmetrical component currents expressed by Equation 4.102 or Equation 4.103. Use these schemes for tripping or blocking, depending on the particular sequence network.

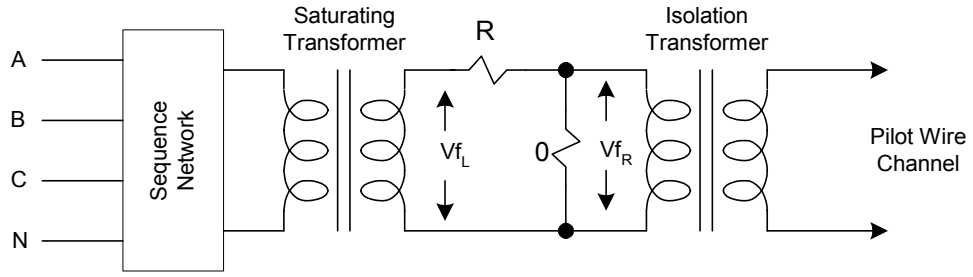


Figure 4.66: Schematic of a Pilot-Wire Channel for One Terminal

$$V_F = K_1 I_1 + K_0 I_0 \qquad \text{Equation 4.102}$$

$$V_F = K_1 I_1 + K_2 I_2 + K_0 I_0 \qquad \text{Equation 4.103}$$

A specific example of a tripping pilot-wire relay is the ABB LCB that implemented the algorithm expressed by Equation 4.28 through Equation 4.30.[57,] When V_{TRIP} exceeds 0.4242 volts the relay operates. Typical values for C0, C1 and C2 are 2.45, 0.1, and 0.22, respectively.

$$V_F = (14.14/\text{Tap})(-C_1 I_{A1} + C_2 I_{A2} + C_0 I_{A0}) \qquad \text{Equation 4.104}$$

$$V_O = \left| V_{FL} + V_{FL} \right| \qquad \text{Equation 4.105}$$

$$V_R = \left| V_{FL} \right| + \left| V_{FL} \right| \qquad \text{Equation 4.106}$$

$$V_{Trip} = V_O - 0.7 V_R \qquad \text{Equation 4.107}$$

The current phase contains all the necessary information to determine that is required by a current differential relay. If the saturating transformer shown in Figure 4.66 effectively converts the currents to a square wave, then the data can be transmitted using on-off keying or FSK audio tones.[58] Making the signal digital has significant advantages of electrical isolation, more options of types of communications and cast.

4.1.2.3.2 Single-Phase Comparison

Phase-comparison and current-differential systems use only current information. Figure 4.67 depicts a schematic diagram of current-only systems. Phase-comparison systems compare the phase of the currents at the line terminals. For internal faults these currents are approximately in phase. For external faults the currents are approximately 180 degrees out of phase.

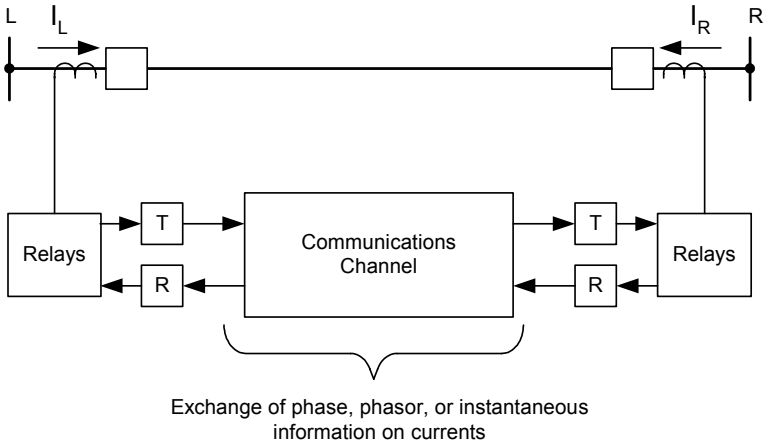


Figure 4.67: Schematic Diagram of Current-Only Pilot Systems

Figure 4.68 shows a simplified schematic diagram of one terminal for a phase comparator. Although the receive signal can be analog, as shown in Figure 4.69, it is more efficient to send only the discrete square wave shown as S_R. We must introduce a time delay, LD, in the local signal, S_L, to compensate for the channel time delay. The local end relay receives the remote-end square wave signal and compensates for the inherent channel time delay, CD. For no fault or an external fault, the square wave generated locally is 180° out of phase with the square wave received from the remote terminal. This causes the output of the AND gate to be low most of the time.

The integrator computes the average value of the AND gate output. When integrator output exceeds a threshold value set by V_{REF}, the relay trips. Both the saturating amplifier and the comparator use hysteresis for noise immunity. For digital integration, start a timer when the output of the AND gate goes high and reset the counter when the signal goes low. If the time exceeds a preset value, the relay trips.

The AND gate issues a logic 1 output signal when signals S_L and S_R are both positive. If LD = CD (exact compensation of the channel time delay), the AND gate behaves as a detector of the positive half-cycle coincidence of currents i_L and i_R. The coincidence timer issues an output tripping signal when the coincidence time of S_L and S_R is equal to or greater than the pickup time ΔT. The ΔT setting determines the

angular width of the phase comparator polar characteristic. For ΔT= one-quarter cycle the characteristic is 180° wide. The dropout timer setting △T′ is intended to latch the tripping signal. This setting should be greater than t–△T, where T is the fundamental frequency period. For internal faults (Figure 4.69 (a)) currents i_L and i_R are approximately in phase, the coincidence AND output signal lasts about half a cycle, and the coincidence timer times out and issues a tripping signal. For external faults (Figure 4.69 (b)) i_L and i_R are approximately 180° out of phase, the AND output is either zero or has very short logic 1 pulses, and the timer does not pick up.

Signals S_L and S_R are not exactly in phase for internal faults or 180° out of phase for external faults. The main sources of phase angle error for external faults are the transmission line charging current, current transformer saturation, and channel time delay compensation errors. For internal faults there is also a phase shift between the currents at both terminals because of the phase shift between the source voltages and the system impedance nonhomogeneity. Accurately measuring or estimating the channel time delay and compensating for it is very important in phase-comparison systems. A compensation error close to one-quarter cycle may cause a relay misoperation or a failure to trip.

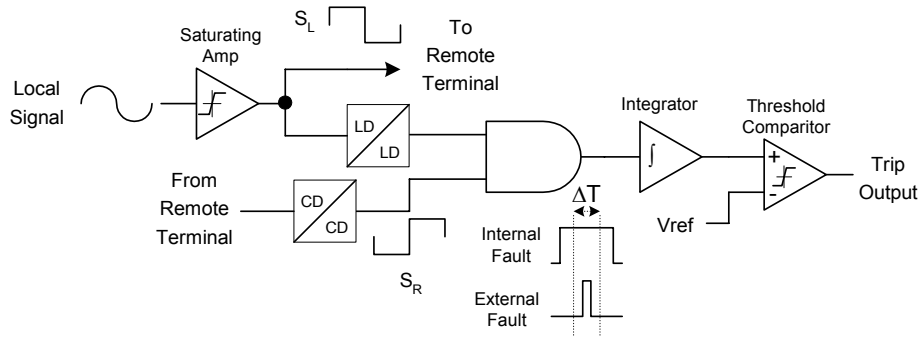


Figure 4.68: Phase-Comparison Schematic Diagram for One Terminal

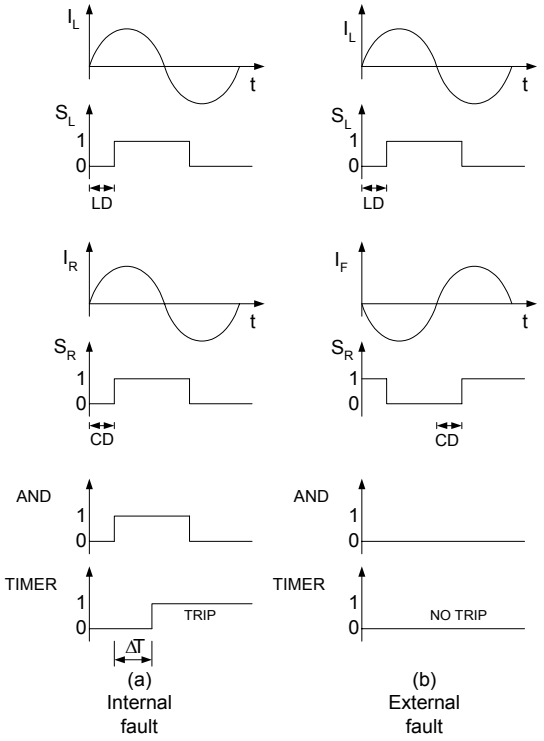


Figure 4.69: Time Diagrams of a Half-Wave Phase-Comparison Pilot Protection System

The operation principle described above corresponds to a transfer trip phase-comparison system. The scheme requires the presence of both signals before issuing the tripping signal. The system may fail to operate for an internal fault coinciding with a failure of the communications channel. In a blocking phase-comparison system we introduce a logic inversion in the square wave that we send to the other line terminal, and we invert again the received signal before the phase comparison. This logic produces tripping when there is no received signal and enhances dependability. The system may misoperate for an external fault coinciding with a communications channel failure.

4.1.2.3.3 Dual-Phase Comparison

Figure 4.68 depicts a half-wave or a single-phase-comparison scheme. The system fulfills the phase comparison for the positive current half-cycles only. This may introduce a half-cycle tripping delay using the full-wave or dual-phase-comparison system logic shown in c. We form two sets of square waves at each line terminal and compare them independently. In Figure 4.70, AND 1 forms the signal corresponding to the time coincidence of the positive – half-cycle square waves S_L^+ and S_R^+. AND 2 detects the time coincidence of the negative – half-cycle square waves S_L^- and S_R^-. The system may take a tripping decision at both half-cycles, thus providing higher operation speed. For simplicity, we do not represent the local and channel time delays in Figure 4.70 and Figure 4.71.

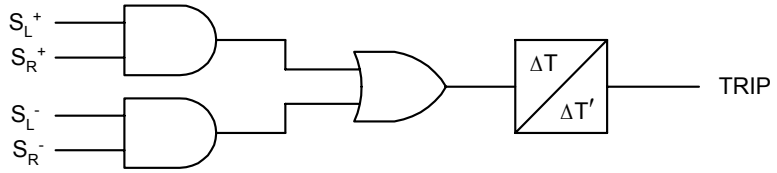


Figure 4.70: Simplified Logic Diagram of a Dual-Phase Comparison Scheme

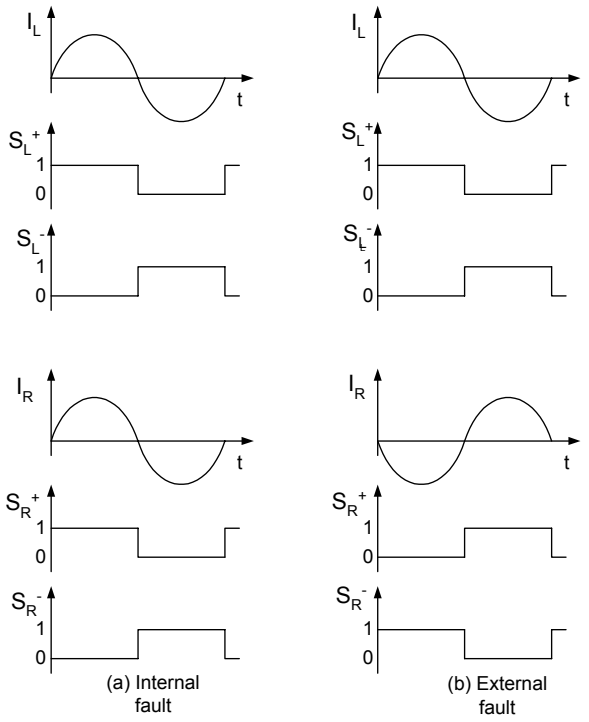


Figure 4.71: Time Diagrams of a Dual-Phase-Comparison Pilot Protection System

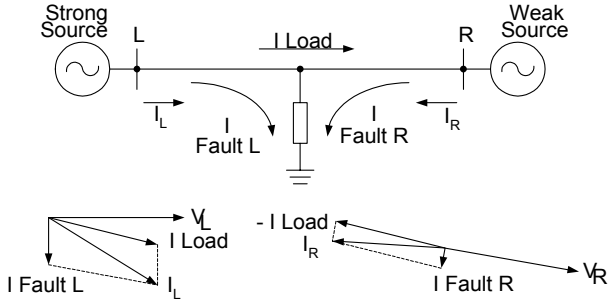
The most widely used phase comparison system is a nonsegregated scheme in which a composite sequence network at each line terminal combines the phase currents to form a unique single-phase voltage. This voltage is representative of the current phase angle for all types of faults. The voltage signals at both line terminals are the basis for phase comparison. A typical composite sequence network output signal, V_F, is a weighted combination of the current symmetrical components $\vec{I}_1, \vec{I}_2, \vec{I}_0$ discussed in section 4.1.2.3.1 and shown in Equation 4.108.

$$\vec{V}_F = k_1\vec{I}_1 + k_2\vec{I}_2 + k_0\vec{I}_0 \qquad \text{Equation 4.108}$$

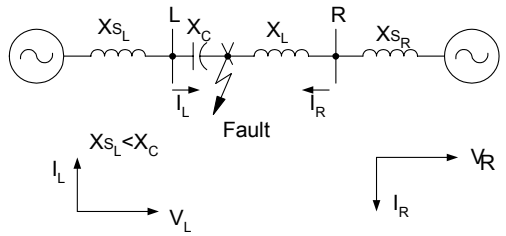
The high bandwidth of modern digital communications channels permits implementation of segregated phase comparison systems. These systems fulfill an independent phase comparison for each phase current. This is a more expensive scheme, but it provides faulted phase identification for single-pole tripping and enhances the protection behavior for evolving, cross-country and inter-circuit faults, and in series-compensated lines.

Phase-comparison systems include fault detectors to control signal transmission and to supervise tripping. Typical schemes use two overreaching overcurrent elements. A distance element may be necessary if the minimum internal fault current is close to the maximum load current.

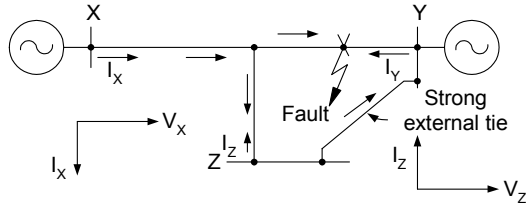
The basic phase-comparison principle exchanges only phase information between line terminals. This principle does not work for internal faults with outfeed, i.e., when one current flows in and the other current flows out of the line. Figure 4.72 shows three possible outfeed conditions for internal faults. A high-resistance internal fault, for which the load current is greater than the fault current (Figure 4.72 (a)), is a typical case of an outfeed situation. In series-compensated lines we have a current reversal when the net reactance from one of the sources to the fault point is capacitive (Figure 4.72 (b)). A three-terminal line having a strong external parallel tie between two terminals (Figure 4.72 (c)) may experience outfeed at one terminal for some internal faults.



(a) High-resistance internal fault



(b) Current reversal in a series-compensated line



(c) Three-terminal line with strong external tie

Figure 4.72: Possible Outfeed Conditions for Internal Faults

To accommodate outfeed, add magnitude information to the signal comparison process. Offset keying is an enhancement to phase comparison that uses both phase and magnitude information. Offset-keying phase comparison derives the square waves by comparing the currents with a given threshold value, which is greater than

the maximum expected outfeed current. Figure 4.73 depicts the square-wave signals obtained for different fault conditions. For internal faults without outfeed (Figure 4.73 (a)) and for external faults (Figure 4.73 (c)) the square waves adequately reflect the current phase angles and the scheme performs as required. Note that the threshold levels are equal in magnitude and have opposite signs at both line terminals. For internal faults with outfeed (Figure 4.73 (b)) signal S_R^- is a solid logic 1. The phase comparison of S_R^- with S_L^- results in a tripping signal. A basic limitation of offset-keying phase comparison is that the displaced threshold prevents tripping for internal faults with low infeed conditions at both line terminals.

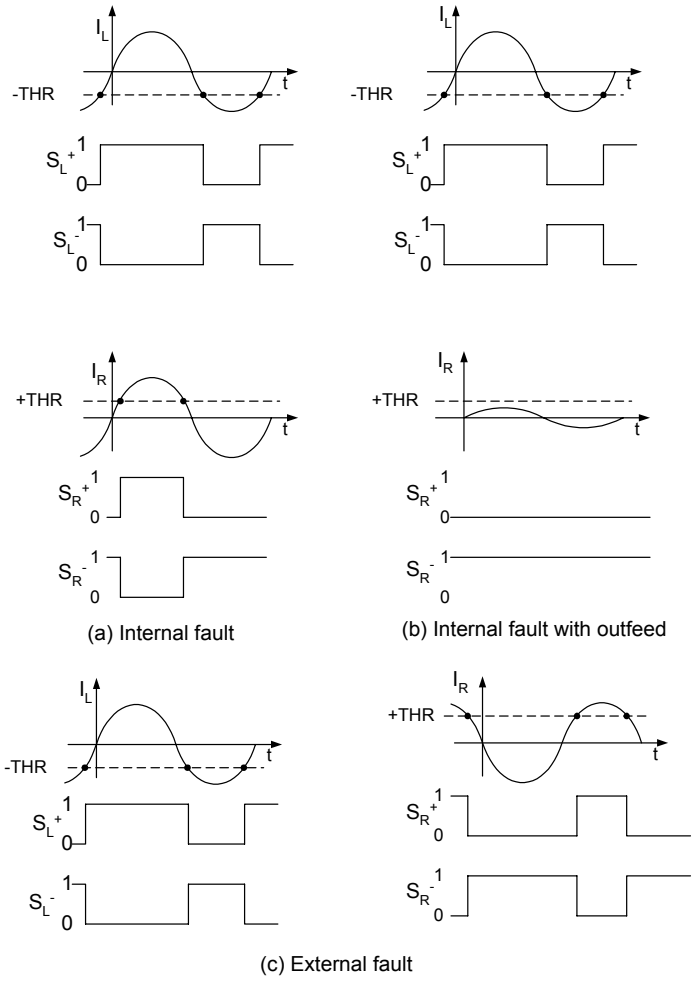


Figure 4.73: Time Diagrams of Offset-Keying Phase-Comparison Pilot Systems

4.1.2.3.4 Dual-Phase Comparison – Unblocking

4.1.2.3.5 Dual-Phase Comparison – Transfer Trip

4.1.2.3.6 Segregated Phase Comparison

Segregated phase comparison relaying operates under the premise that the vector sum of the currents into a line or conductor must equal zero. It is a type of line differential relaying scheme that requires communication of information on the magnitude and phase of the three phase currents to all terminals of the line. An alternate communications scheme sends $I_A - I_B$ over one channel and $3I_0$ over a second. This type of phase comparison is the scheme of choice for series-compensated lines. It is, however, susceptible to false trips in the presence of severe harmonics.

4.2.6.3.6.1 Advantages of phase-segregated current-only pilot systems

Segregated phase comparison relaying does not require voltage information, so avoids such problems as loss of potential for close-in faults, blown potential fuses, ferroresonance in VTs, and transients in CVTs. Phase comparison relays:

- are immune to effects of mutual induction, power swings, series impedance unbalance (open-pole conditions, unequal gap flashing on series-compensated lines, etc.), and current reversals in parallel-line configurations
- perform well for evolving, intercircuit, and cross-country faults
- are applicable to short transmission lines
- tolerate high line loading

Depending on the operating characteristic, current-only systems respond adequately to outfeed conditions during high-resistance faults and in series-compensated and three-terminal lines.

The basic limitations of current-only systems are that they require reliable, high-capacity communications channels. These limitations are rapidly disappearing with the increasing quality of modern digital fiber-optic communications channels. In addition, digital technology permits inclusion of many protection functions in a relay unit. It is then possible to combine a directional comparison and a current-only pilot system in the same relay. This diversity of operation principles in the same unit may enhance the overall performance without a significant increase in cost. In applications where reliability also demands duplicate hardware, we can install two such relay units and obtain four separate protection functions running on two separate hardware platforms.

4.1.3 Differential Relaying

Differential relays operate on the principle that the instantaneous algebraic sum of all currents into a node must equal zero. Figure 4.74 shows a typical application. The protected equipment can be any power device that can fail by an internal fault such as transformers, reactors, circuit breakers, and entire station buses. The current transformers act like constant current sources and as long as the secondary currents

are equal, no current flows through the differential relay element. Normally the differential relay element is an overcurrent relay, as discussed in sections 0 and 0.

The percentage-differential principle that was originally developed for the protection of transformers and generators, as discussed in section 0 and chapter 7, is extended to the protection of short transmission lines in the 1930s. The traditional system uses a telephone-type pilot wire channel to exchange analog information between the line terminals. Composite sequence networks form voltage signals (see Equation 4.108) that contain magnitude and phase information on the currents at the line terminals. Percentage-differential relays at each end respond to the currents derived from the comparison of these voltages through the pilot wire. This system operates as a percentage-differential relay at lower levels of fault current. At the higher currents it becomes a phase-comparison system because of the effect of a saturating transformer included in the scheme. The introduction of fiber-optic channels permits provision of the percentage-differential characteristic for all levels of fault current.

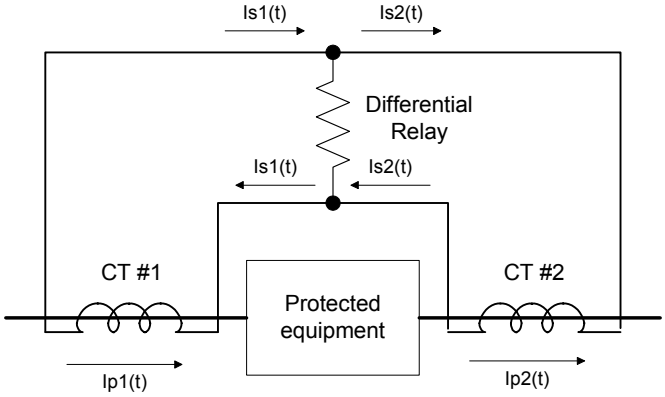


Figure 4.74: Differential Relaying Scheme

Differential relaying is fast and relatively simple to implement. However, false operations can occur from CT mismatches or unequal responses to transients generated by normal switching or external faults. The percentage-differential relay adds a restraint element, shown in Figure 4.75, to desensitize the relay at lower currents where mismatches are more pronounced.

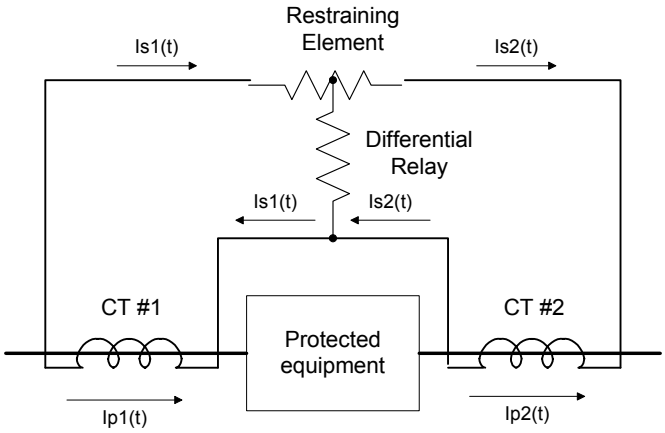


Figure 4.75: Percentage Differential Relaying Scheme

In digital current-differential pilot systems we use the communications channel to exchange digital information on the currents at the line terminals (see Figure 4.67). Systems exchange phasor information or digitized raw samples.

Percentage-differential elements compare an operating current (also called differential current) with a restraint current. In Equation 4.109 the operating current, I_{OP}, is the magnitude of the phasor sum of the currents entering the protected element.

$$I_{OP} = \left| \vec{I}_L + \vec{I}_R \right| \qquad \text{Equation 4.109}$$

I_{OP} is proportional to the fault current for internal faults and approaches zero for any other operating (ideal) conditions.

The most common alternatives for obtaining the restraint current, I_{RT}, are the following Equation 4.110 through Equation 4.113.

$$I_{RT} = k\left| \vec{I}_L - \vec{I}_R \right| \qquad \text{Equation 4.110}$$

$$I_{RT} = k\left(\left| \vec{I}_L \right| + \left| \vec{I}_R \right| \right) \qquad \text{Equation 4.111}$$

$$I_{RT} = \text{Max}\left(\left| \vec{I}_L \right|, \left| \vec{I}_R \right| \right) \qquad \text{Equation 4.112}$$

$$I_{RT} = \sqrt{\left| \vec{I}_L \right| \cdot \left| \vec{I}_R \right| \cos\theta} \qquad \text{Equation 4.113}$$

Here k is a constant coefficient, usually taken as 1 or 0.5, and θ is the angle between $\vec{I}_L$ and $\vec{I}_R$. Equation 4.111 and Equation 4.112 are applicable to differential relays with more than two restraint elements. For example, for a three-terminal line we may use the following quantities:

$$I_{OP} = \left| \vec{I}_X + \vec{I}_Y + \vec{I}_Z \right| \qquad \text{Equation 4.114}$$

$$I_{RT} = k\left(\left| \vec{I}_X \right| + \left| \vec{I}_Y \right| + \left| \vec{I}_Z \right| \right) \qquad \text{Equation 4.115}$$

where $\vec{I}_X$, $\vec{I}_Y$, and $\vec{I}_Z$ are the currents at the line terminals.

Equation 4.116 defines the operation condition of a percentage-differential relay as:

$$I_{OP} \geq K I_{RT} \qquad \text{Equation 4.116}$$

where K is a constant coefficient representing the slope of the relay characteristic. In order to provide the relay with a minimum pick-up current, K_0, we add the condition:

$$I_{OP} \geq K_0 \qquad \text{Equation 4.117}$$

Figure 4.76 (a) shows the relay operating characteristic resulting from the equality conditions of both Equation 4.116) and Equation 4.117).

Another possible definition of the differential relay operation condition is:

$$I_{OP} \geq KI_{RT} + K_0 \qquad \text{Equation 4.118}$$

Figure 4.76 (b) shows the relay characteristic corresponding to Equation 4.118. It is a straight line having a slope K and an intersect K_0 on the ordinate axis.

A variable-percentage or dual-slope characteristic (dotted lines in Figure 4.76) increases relay security.

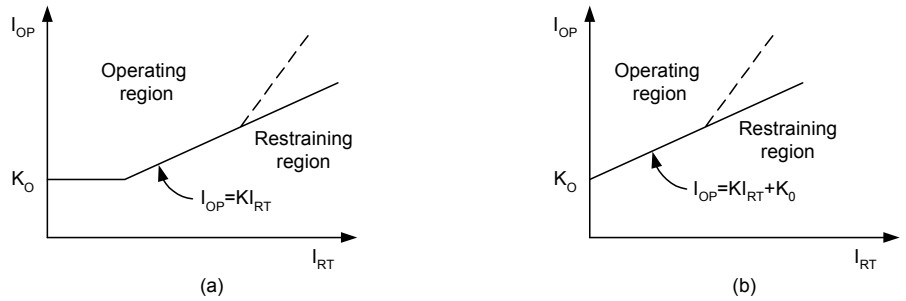


Figure 4.76: Differential Relay Operating Characteristics

The differential current is not exactly zero for external faults. The most common causes of false differential current in transmission line differential relays are the following are line charging current, tapped load, channel time-delay compensation errors, and current transformer saturation.

Line-charging current is significant in cable lines or long overhead lines. The false differential current created by tapped loads may be the result of load current or of low-side faults or inrush current in the tapped transformer. Using a negative or zero-sequence differential element eliminates the effect of line charging current and of the load current component of tapped loads. Channel time-delay compensation errors and current transformer saturation contribute to false differential current in all types of differential elements. To address these two sources of error we need to design carefully the operating characteristic of the differential element.

4.2.7.1 Charge Comparison

Charge comparison is an alternative form of current-differential transmission line protection intended to reduce the communications channel requirements. [59, 60, 61, 62] Charge comparison performs a numeric integration of samples of the phase and residual currents over half a cycle. The sample integration process takes place between current zero-crossings. The system stores the resulting ampere-seconds area in memory (converted into an rms current equivalent), along with polarity and start/finish time-tag information. Storage occurs only if the magnitude exceeds 0.5 A rms equivalent and the half-cycle pulse width is equal to or greater than 6 ms. The local system also sends information to the remote terminal every half-cycle.

Each line terminal performs a so-called nesting process to determine if a given received equivalent rms current value corresponds to the same semi-cycle as that of the stored local rms current value. Figure 4.77 depicts a time diagram of the nesting process for an internal fault. The local terminal receives the message from the remote terminal after the channel time delay, CD, and assigns a received time-tag to

the message. Then the local terminal subtracts a time interval from the received time-tag to form the adjusted received time-tag. This time interval includes the channel relay compensation, LD, plus a time adjustment in the received message, TA. A typical value of TA is one-quarter cycle. The local terminal compares the adjusted received time-tag with the local start and finish time-tags. A nesting operation is successful when the adjusted received time-tag is between the local start and finish time-tags.

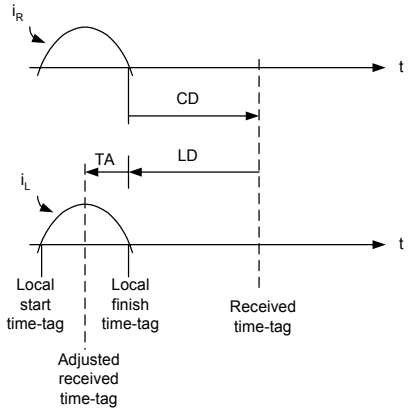


Figure 4.77: Time Diagram of the Nesting Process for an Internal Fault

When a nesting operation is successful, we use the local and remote current magnitudes to form the operating and restraining quantities of a dual-slope percentage-differential element. The restraining quantity is the sum of the absolute current magnitudes (scalar sum.) The operating quantity is the absolute value of the sum of the signed current magnitudes (arithmetic sum.)

4.2.7.2 Alpha-Plane Differential Relaying

Current-only line protection systems may compare phase or amplitude of quantities derived from the currents at the line terminals. It is customary to use a polar current diagram to represent the operation characteristic of phase-comparison systems. A scalar current diagram showing the operating current as a function of the restraint current is the typical way of representing the differential relay operating characteristics.

Taking into account that relay input signals are complex quantities, the most comprehensive way to represent relay characteristics is to use a complex plane defined by the ratio of the relay input signals. [63, 64] For relays having current and voltage input signals the complex plane could be an impedance or an admittance plane. For relays with only current or voltage inputs the complex plane is a current-ratio or a voltage-ratio plane, respectively.

4.2.7.2.1 Current-Ratio Plane

We may define a complex variable given by the ratio of the remote, $\vec{I}_R$, to the local, $\vec{I}_L$, currents:

$$\frac{\vec{I}_R}{\vec{I}_L} = a + jb = \vec{r} = re^{j\theta}$$ Equation 4.119

where

$$a = \frac{\left|\vec{I}_R\right|}{\left|\vec{I}_L\right|}\cos\theta = r\cos\theta$$ Equation 4.120

$$b = \frac{\left|\vec{I}_R\right|}{\left|\vec{I}_L\right|}\sin\theta = r\sin\theta$$ Equation 4.121

$$r = \sqrt{a^2 + b^2}$$ Equation 4.122

$$\theta = \arctan\frac{b}{a}$$ Equation 4.123

Equation 4.119 is the base for the Cartesian – or polar – coordinates versions of the current-ratio plane. Warrington [65, 66] introduced the term alpha-plane to designate the $\vec{I}_R / \vec{I}_L$ plane, and the term beta-plane for the $\vec{I}_L / \vec{I}_R$ plane. Both planes are equivalent in terms of the information they provide, so we will only use the alpha-plane.

4.2.7.2.2 Current-Differential Relay Characteristics

Let us obtain the current-ratio plane characteristic of a differential relay having Equation 4.116 as the operating equation and with a restraint quantity given by Equation 4.110, with k = 1 for simplicity. Substituting Equation 4.109 and Equation 4.110 in Equation 4.116 results in Equation 4.124.

$$\left|\vec{I}_L + \vec{I}_R\right| \geq K\left|\vec{I}_L - \vec{I}_R\right|$$

$$\left|1 + \frac{\vec{I}_R}{\vec{I}_L}\right| \geq K\left|1 - \frac{\vec{I}_R}{\vec{I}_L}\right|$$ Equation 4.124

Substituting Equation 4.119 results in Equation 4.124:

$$\left|1 + a + jb\right| \geq K\left|1 - a - jb\right|$$ Equation 4.125

After expanding the terms of the previous equation we get Equation 4.126. The equality condition in Equation 4.126 represents the relay threshold operation condition and describes the relay operation characteristic. It is the equation of a circle, with a radius, R_c, given by:

$$a^2 + b^2 + 2\frac{1+K^2}{1-K^2}a + 1 \geq 0 \qquad \text{Equation 4.126}$$

$$R_c = \frac{2K}{1-K^2} \qquad \text{Equation 4.127}$$

The location of the circle center in the complex plane is:

$$a_c + jb_c = -\frac{1+K^2}{1-K^2} + j0 \qquad \text{Equation 4.128}$$

Figure 4.78 shows a family of relay operation characteristics for different values of the slope, K. The operating region is the area out of the circle (see Equation 4.126) and the restraint region is inside the circle. Note that the –1 + j0 point corresponding to an ideal through-current condition is inside the relay restraint region.

Table 4.9 summarizes the types of operation characteristics of differential relays having Equation 4.116 or Equation 4.118 as the operating equation, and with different types of restraint quantities (Equation 4.110 to Equation 4.113). Table 4.9 also includes the characteristic of the unrestrained differential element, which corresponds to $I_{RT} = 0$ in Equation 4.118. Appendix 1 presents the derivation of the equations for all the differential relay characteristics.

In general, differential relays described by Equation 4.116 have circular characteristics (see Table 4.1). An exception is the frequent case in which the relay restraint quantity is of the type in Equation 4.111. Figure 4.79 depicts a family of relay characteristics for this case. Note that the value of the slope, K, determines not only the size, but also the shape of the relay characteristic. The relay with a restraint quantity of the type of Equation 4.112 has two different circular characteristics, depending upon the relative magnitudes of I_L and I_R (see Table 4.9).

Differential relays described by Equation 4.118 do not generally have circular characteristics (see Table 4.1). The only circular characteristics are those of the unrestrained differential element ($I_{RT} = 0$) and the relay having a restraint quantity of the type of Equation 4.112 (the characteristic is circular only for $I_L > I_R$). Note that in these two circular characteristics the radius depends not only on the parameters K and K_0, but also on the local current magnitude, I_L.

Dual-slope differential relays may have two different types of operating characteristics in the current-ratio plane. For example, if the first slope characteristic corresponds to Equation 4.116, the characteristic in the current-ratio plane is a circle (unless the restraint quantity is of the type shown in Equation 4.118). The second slope characteristic intersects the restraint current axis. It is of the type shown in Equation 4.118, which gives a noncircular operating characteristic in the current-ratio plane.

4.2.7.2.3 Charge-Comparison System Characteristic

In charge-comparison systems the nesting process basically determines whether the angle θ between the currents $\vec{I}_L$ and $\vec{I}_R$ is within ± 90 degrees with respect to 0 degrees, or is within ± 90 degrees with respect to 180°. The condition –90 degrees

$\leq \theta \leq 90$ degrees corresponds to the right semi-plane of the current-ratio plane; the condition 90 degrees $\leq \theta \leq 270$ degrees corresponds to the left semi-plane.

Table 4.8: Differential Relay Characteristics in the Current-Ratio Plane

Operation Equation	Restraint Quantity	Type of Characteristic	Center	Radius
$I_{OP} = KI_{RT}$	$I_{RT} = \left\vert \vec{I}_L - \vec{I}_R \right\vert$	Circular	$-\frac{1+K^2}{1-K^2} + j0$	$\frac{2K}{1-K^2}$
	$I_{RT} = \left\vert \vec{I}_L \right\vert + \left\vert \vec{I}_R \right\vert$	Not Circular	—	—
	$I_{RT} = \text{Max}\left(\left\vert \vec{I}_L \right\vert, \left\vert \vec{I}_R \right\vert \right)$	$\left\vert \vec{I}_L \right\vert > \left\vert \vec{I}_R \right\vert$ Circular	$-1 + j0$	K
		$\left\vert \vec{I}_L \right\vert < \left\vert \vec{I}_R \right\vert$ Circular	$-\frac{1}{1-K^2} + j0$	$\frac{K}{1-K^2}$
	$I_{RT} = \sqrt{\left\vert \vec{I}_L \right\vert \cdot \left\vert \vec{I}_R \right\vert \cos\theta}$	Circular	$-\left(1 - \frac{K^2}{2}\right) + j0$	$\frac{K}{2}\sqrt{K^2 - 4}$
$I_{OP} = KI_{RT} + K_0$	$I_{RT} = 0$	Circular	$-1 + j0$	$\sqrt{\frac{K_0}{\left\vert \vec{I}_L \right\vert}}$
	$I_{RT} = \left\vert \vec{I}_L - \vec{I}_R \right\vert$	Not Circular	—	—
	$I_{RT} = \left\vert \vec{I}_L \right\vert + \left\vert \vec{I}_R \right\vert$	Not Circular	—	—
	$I_{RT} = \text{Max}\left(\left\vert \vec{I}_L \right\vert, \left\vert \vec{I}_R \right\vert \right)$	$\left\vert \vec{I}_L \right\vert > \left\vert \vec{I}_R \right\vert$ Circular	$-1 + j0$	$\sqrt{1 + \left(K + \frac{K_0}{\left\vert \vec{I}_L \right\vert} \right)^2}$
		$\left\vert \vec{I}_L \right\vert < \left\vert \vec{I}_R \right\vert$ Not Circular	—	—
	$I_{RT} = \sqrt{\left\vert \vec{I}_L \right\vert \cdot \left\vert \vec{I}_R \right\vert \cos\theta}$	Not Circular	—	—

After qualifying the signals in the nesting process, we form the operating and the restraint quantities of the differential element. The restraint quantity, I_{RT}, is the sum of the absolute current magnitudes. Then, I_{RT} is of the type shown in Equation 4.111. The operating quantity, I_{OP}, is the absolute value of the arithmetic sum of the signed current magnitudes. Note that this is not a phasor sum. Then, there are two

expressions for I_{OP}, one for each semi-plane of the current-ratio plane expressed by Equation 4.129 and Equation 4.130.

$$I_{OP} = \left| \left| \vec{I}_L \right| - \left| \vec{I}_R \right| \right| \quad \text{(Left semi-plane)} \qquad \text{Equation 4.129}$$

$$I_{OP} = \left| \vec{I}_L \right| + \left| \vec{I}_R \right| \quad \text{(Right semi-plane)} \qquad \text{Equation 4.130}$$

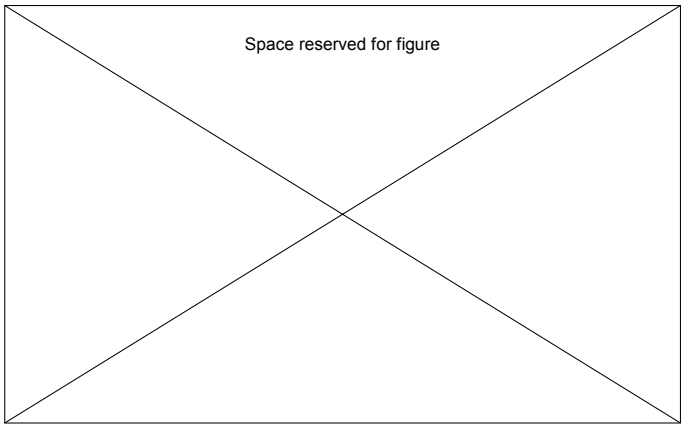


Figure 4.78: Operating Characteristics of a Differential Relay Described by Equation 4.116 and Equation 4.110

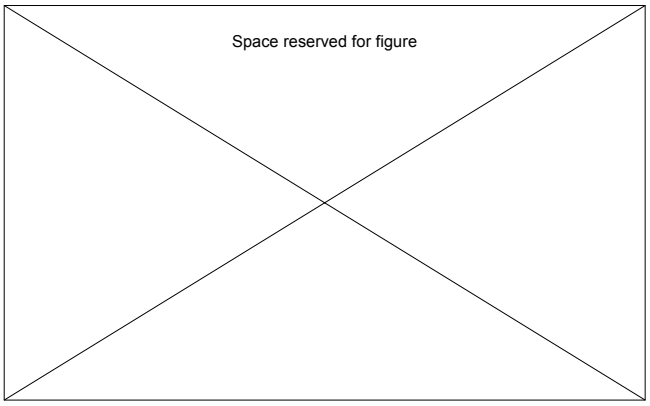


Figure 4.79: Operating Characteristics of a Differential Relay Described by Equation 4.116 and Equation 4.111

In charge-comparison systems the operation equation of the differential element is of the type shown in Equation 4.116. To obtain the operation characteristic corresponding to the left semi-plane of the current-ratio plane we substitute Equation 4.111 and Equation 4.129 in Equation 4.116, which results in Equation 4.131. Substituting Equation 4.119 in Equation 4.131 and expanding:

$$\left| \left| \vec{I}_L \right| - \left| \vec{I}_R \right| \right| \geq K \left(\left| \vec{I}_L \right| + \left| \vec{I}_R \right| \right) \qquad \text{Equation 4.131}$$

$$\left| 1 - \frac{\left| \vec{I}_R \right|}{\left| \vec{I}_L \right|} \right| \geq K \left(1 + \frac{\left| \vec{I}_R \right|}{\left| \vec{I}_L \right|} \right)$$

$$\left| 1 - \sqrt{a^2 + b^2} \right| \geq K \left| \left(1 + \sqrt{a^2 + b^2} \right) \right| \qquad \text{Equation 4.132}$$

Equation 4.132 has two solutions. The resulting operating characteristic in the left semi-plane consists of two semi-circles centered in the origin of coordinates. The operating region is outside the outer circle and inside the inner circle. The restraint region is between the two semi-circles. The radii of the two semi-circles are shown in Equation 4.162 and Equation 4.163.

$$R_1 = \frac{1 - K}{1 + K} \qquad \text{(Inner semi-circle)} \qquad \text{Equation 4.133}$$

$$R_2 = \frac{1 + K}{1 - K} \qquad \text{(Outer semi-circle)} \qquad \text{Equation 4.134}$$

To obtain the operation characteristic corresponding to the right semi-plane, we substitute Equation 4.111 and Equation 4.130 in Equation 4.131:

$$\left| \vec{I}_L \right| + \left| \vec{I}_R \right| \geq K \left(\left| \vec{I}_L \right| + \left| \vec{I}_R \right| \right) \qquad \text{Equation 4.135}$$

Equation 4.135 describes the case in which $K \leq 1$. Then, the right semi-plane of the current-ratio plane is an operating region for all cases in which $K \leq 1$. Figure 4.80 shows the operating characteristic of charge comparison systems in the current-ratio plane.

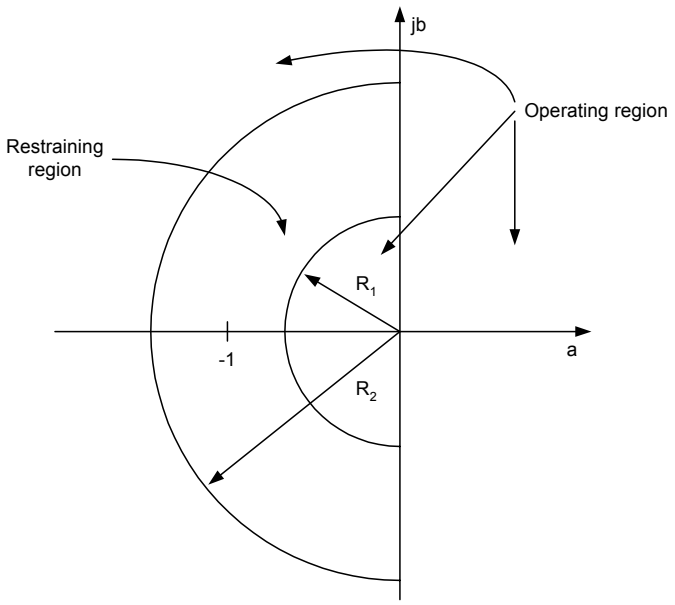


Figure 4.80: Operating Characteristics of Charge-Comparison Systems

4.2.7.2.4 Phase-Comparison System Characteristics

Figure 4.69 depicts the operation principle of phase-comparison systems. For exact compensation of the channel time delay, the angle between signals $\vec{S}_L$ and $\vec{S}_R$ equals the angle between $\vec{I}_L$ and $\vec{I}_R$, θ. The operation condition of the phase-comparison circuit (Figure 4.68) is:

$$-\beta \le \theta \le \beta \qquad \text{Equation 4.136}$$

where β is a constant parameter defining the angular limits of the phase comparator. β is equal to the value of θ for which the time coincidence of the signals equals ΔT. Then, β is the supplement of the coincidence angle $\omega\Delta T$:

$$\beta = \pi - \omega\Delta T = \pi - \frac{2\pi}{T}\Delta T = \pi\left(1 - \frac{2\Delta T}{T}\right) \quad (\text{radians}) \qquad \text{Equation 4.137}$$

where T is the fundamental frequency period.

Figure 4.81 depicts the operating characteristic of a phase-comparison system (Equation 4.136) in the current-ratio plane. Offset-keying phase-comparison systems add magnitude information to the comparison process in order to respond to internal faults with outfeed.

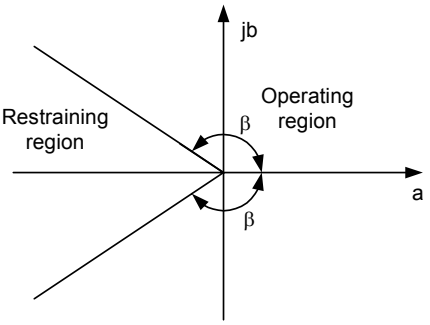


Figure 4.81: Operating Characteristic of a Phase-Comparison System

Figure 4.73 shows the basic operation principle of offset-keying phase-comparison systems. When the magnitudes of both currents exceed the threshold, THR, the offset-keying system behaves as a conventional comparison system (Figure 4.73 (a) Figure 4.73 (c)). When one current is below THR and the other one is above THR the system behaves as an overcurrent system (Figure 4.73 (b)). When both current magnitudes are below THR the system does not operate even for an internal fault. Let K_0 be the current value for which the system transitions from phase comparison to overcurrent protection. K_0 is an rms current expression of the threshold, THR. We may summarize the operation of the offset-keying phase-comparison system as follows:

For $\left|\vec{I}_L\right| > K_0$ and $\left|\vec{I}_R\right| > K_0$: Phase comparison

For $\left|\vec{I}_L\right| \le K_0$ and $\left|\vec{I}_R\right| \ge K_0$: Overcurrent protection

For $\left|\vec{I}_L\right| \geq K_0$ and $\left|\vec{I}_R\right| \leq K_0$: Overcurrent protection

For $\left|\vec{I}_L\right| < K_0$ and $\left|\vec{I}_R\right| < K_0$: No operation

The two operation conditions of the overcurrent protection function define two operating characteristics. For $\left|\vec{I}_L\right| \leq K_0$, the overcurrent operation condition is:

$$\left|\vec{I}_R\right| \geq K_0$$

$$\frac{\left|\vec{I}_R\right|}{\left|\vec{I}_L\right|} \geq \frac{K_0}{\left|\vec{I}_L\right|} \qquad \text{Equation 4.138}$$

$$\sqrt{a^2 + b^2} \geq \frac{K_0}{\left|\vec{I}_L\right|}$$

Equation 4.140 describes a circular operating characteristic centered in the origin of coordinates and with the operating region outside the circle. The radius is:

$$R_1 = \frac{K_0}{\left|\vec{I}_L\right|} \geq 1 \qquad \text{Equation 4.139}$$

For $\left|\vec{I}_R\right| \leq K_0$, the overcurrent operation condition is:

$$\left|\vec{I}_L\right| \geq K_0$$

$$\frac{1}{\left|\vec{I}_L\right|} \leq \frac{1}{K_0}$$

$$\frac{\left|\vec{I}_R\right|}{\left|\vec{I}_L\right|} \leq \frac{\left|\vec{I}_R\right|}{K_0} \qquad \text{Equation 4.140}$$

$$\sqrt{a^2 + b^2} \leq \frac{\left|\vec{I}_R\right|}{K_0}$$

The operating characteristic given by Equation 4.140 is a circle centered in the origin of coordinates with the operating region inside the circle. The radius is:

$$R_2 = \frac{\left|\vec{I}_R\right|}{K_0} \leq 1 \qquad \text{Equation 4.141}$$

Figure 4.82 shows the operating characteristic of the offset-keying phase-comparison system in the current-ratio plane. Note that the system operation as an overcurrent system (areas inside the inner circle and outside the outer circle) is conditioned: one of the currents needs to be above the threshold, K_0, for the system to operate. If both

current magnitudes are below K_0, the system does not operate. This may cause misoperation for internal faults with low current contributions from both line ends. Note also that the circle radii in Figure 4.82 are not constant, but depend on the current values.

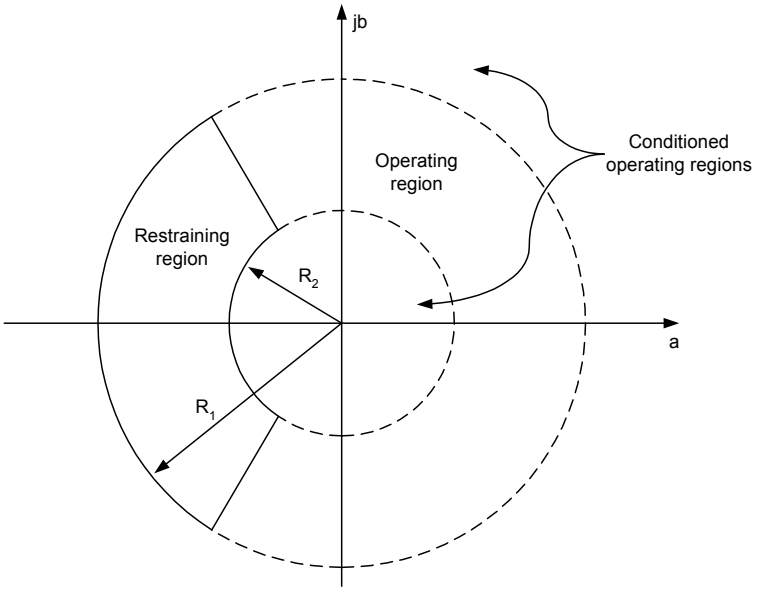


Figure 4.82: Operating Characteristic of an Offset-Keying Phase-Comparison System

4.2.7.3 Current-Ratio Trajectories

The current-ratio plane is an excellent tool for analyzing current-only protection system response to different power system conditions and to the signal corruption from the protection scheme elements. The method for analyzing relay operation is to superimpose on the same current-ratio plane the relay characteristic and the current-ratio trajectory resulting from the fault or abnormal condition in the power system. This method is equivalent to the operation analysis of distance relays in the impedance plane.

For power-system and protection-scheme steady-state conditions the current-ratio trajectory reduces to a point. Under transient conditions the trajectory converges to the final steady-state point in the current-ratio plane. Figure 4.83 shows current-ratio plane regions for steady-state fault and load conditions. Disregarding all possible sources of errors, the point representing the system condition will fall in the real, a, axis. For ideal through-current conditions (normal loads or external faults), a = –1. For internal faults with infeed from both line ends, then *a* is greater than zero. For internal faults with outfeed at one terminal, *a* is less than zero. Note that the relay characteristic should have $a = -1$ point in the restraint zone and all the fault regions in the operation zone.

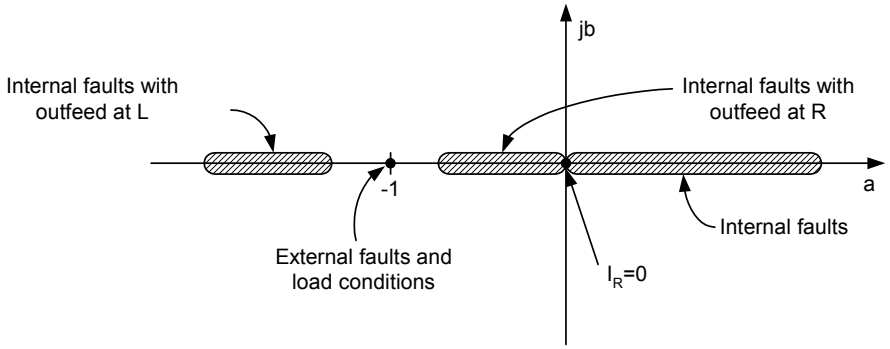


Figure 4.83: Current-Ratio Plane Regions for Ideal Fault and Load Conditions

4.2.7.3.1 System Power Angle And System Impedance Nonhomogeneity

For internal faults the angles of the phase currents $\vec{I}_L$ and $\vec{I}_R$ depend on the angles of the corresponding source voltages and on the angles of the impedances from the corresponding source to the fault point. In general, the currents at both line ends will not be exactly in phase for an internal fault. Figure 4.84 shows the modification of the fault regions when θ varies within ± 30° for internal faults. Note that the regions corresponding to load, external faults, and internal faults with outfeed remain unchanged. We may practically eliminate the phase-angle error by using the negative-or zero-sequence components of the line currents instead of the phase currents. The only source of error in this case is the system impedance nonhomogeneity, which typically represents a small part of the total angle error.

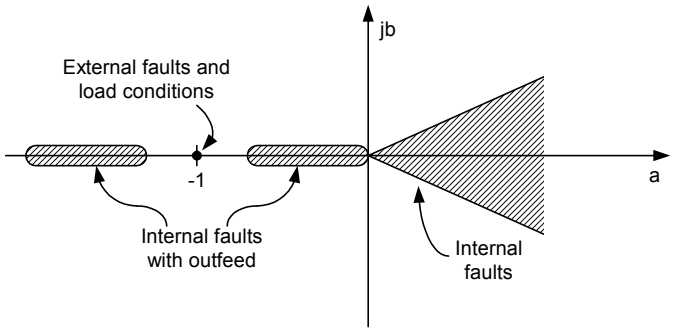


Figure 4.84: Effect of the System Power Angle and the System Impedance Nonhomogeneity

4.2.7.3.2 Line-Charging Current

Line-charging current flows into the line at both line terminals and creates a false differential current. Figure 4.85 (a) represents the current components that are in the line for a normal load condition. The currents at both line terminals are:

$$\vec{I}_L = \vec{I}_{LOAD} + \vec{I}_C$$
$$\vec{I}_R = -\vec{I}_{LOAD} + \vec{I}_C$$

Equation 4.142

where I_{LOAD} is the load current and I_C is the charging current at each line end. Then:

$$\frac{\vec{I}_R}{\vec{I}_L} = a + jb = \frac{-\vec{I}_{LOAD} + \vec{I}_C}{\vec{I}_{LOAD} + \vec{I}_C} \qquad \text{Equation 4.143}$$

Figure 4.85 (b) depicts the current-ratio locus () for different values of I_{LOAD}. The trajectory is not circular in the general case. Note that for small load currents the current-ratio value lies in the right semi-plane. The only way to avoid relay misoperation is to set the relay minimum pickup current greater than the line-charging current value. For differential elements responding to the phase currents this sensitivity limitation affects the relay fault resistance coverage for internal faults. The negative- or zero-sequence components of the charging current are very low compared to the positive-sequence or phase values. Then, set a negative-sequence or a zero-sequence differential element to be much more sensitive than a phase element. Appendix 2 presents two application examples that illustrate the large difference between phase- and negative-sequence charging current magnitudes.

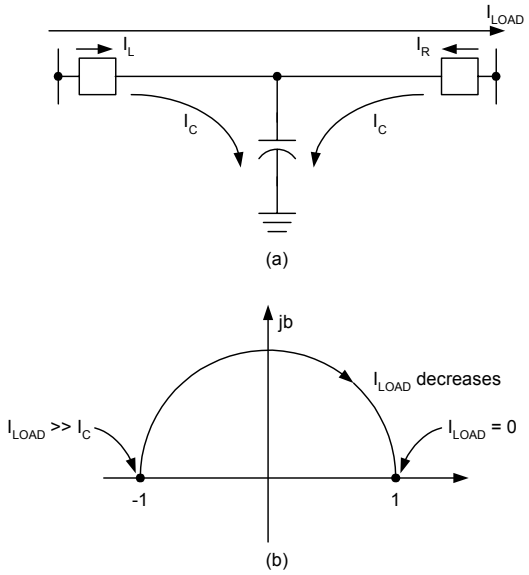


Figure 4.85: Effect of Line-Charging Current

4.2.7.3.3 Tapped Loads

A tapped load not included in the line differential measurements creates an operation current component in the differential scheme. Figure 4.86 shows the current distribution in a line with a tapped load. The tapped load current, I_T, may be load or fault current. Fault currents may correspond to internal or secondary-side faults in the tapped transformer.

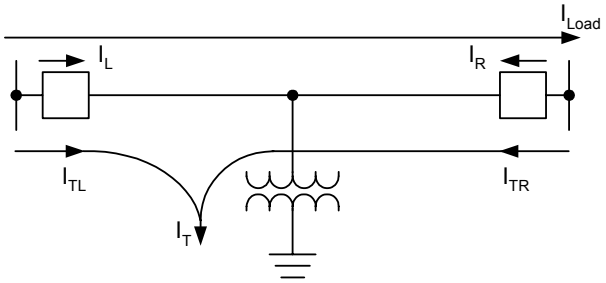


Figure 4.86: Transmission Line With Tapped Load

When $I_{TL} = I_{TR}$ (see Figure 4.86) the current-ratio locus has the general aspect of that of Figure 4.85 (b). It is only necessary to substitute I_C by I_T in Figure 4.85 (b). When $I_{TL} \neq I_{TR}$ the trajectory still begins at $a = -1$ (for $I_{LOAD} >> I_T$), and ends in the right part of the real axis. In general, $a \neq 1$ for $I_{LOAD} = 0$.

Set the differential relay pickup greater than the load current of the tapped load. Set negative- and zero-sequence differential elements to be more sensitive than the phase elements, because they only respond to load unbalance. Be sure to take the tapped load fault current into account. A possible solution is to desensitize the relay to the maximum tapped load fault current. The type of fault to consider depends on the differential element: three-phase fault for the phase elements, phase-to-phase or phase-to-phase-ground faults for the negative-sequence elements, and phase-ground faults for the zero-sequence elements. If one of the tapped transformer windings is connected in delta, a zero-sequence differential relay does not respond to secondary-side ground faults, but will still respond to internal transformer primary winding ground faults. A better solution is to coordinate the differential relay time with the tapped load overcurrent protection devices.

4.2.7.3.4 Channel Time-Delay Compensation Errors

Communications channel time delay produces a phase shift between the local current and the received remote current in current-only pilot protection systems. Using GPS signals to synchronize the sampling clocks of the relays at all line terminals is one solution to this problem. Synchronized sampling permits computation of phasors having the same angular reference. Assign a time tag or sampling index to the computed phasor and transmit this information to the other line terminal(s). Compare two phasors that have been acquired at exactly the same sampling instant by selecting those two phasors having the same sampling index. The basic limitation of synchronized sampling is the additional cost of the GPS receivers and clocks.

The most widely used solution is to estimate or measure the channel time delay and to compensate for it in the relay logic. In analog phase comparison pilot systems we introduce a time delay in the local square-wave signal to account for the channel time delay (see Figure 4.68).

Digital line differential protection systems typically use independent (nonsynchronized) sampling clocks and align the computed phasors. The universal technique to align the phasors, measuring the time delay between the sampling pulses at two different locations, is known as the ping-pong technique. Once the delay between the two sampling pulses has been established, the two phasors

corresponding to these two sampling pulses can be time aligned by applying a compensation rotation to one of the phasors. Appendix 3 describes the phasor alignment techniques for line differential protection systems.

The ping-pong technique assumes equal delay or symmetry in the communications channel. In some channels the transmit path has a different propagation delay than the receive path. This asymmetrical communications delay can exist, for example, on digital communications networks employing SONET self-healing-ring technology. The level of asymmetry depends on the architecture of the communications system. Delay differences are typically 1 to 2 ms. Delays of 3 to 5 ms are rare and only exist on systems with fiber lengths greater than 100 miles and with 20 or more nodes in the ring.

Communications channel asymmetries generate an error in the phase shift angle, θ, between phasors $\vec{I}_L$ and $\vec{I}_R$. Figure 4.87 shows the effect of this angle error in the current-ratio plane. Note that channel asymmetry creates an angular expansion of the ideal fault and load regions depicted in Figure 4.84.

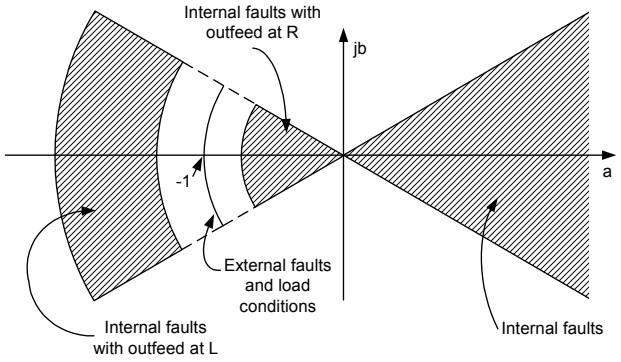


Figure 4.87: Effect of Channel Time-Delay Compensation Errors

4.2.7.3.5 Current Transformer Saturation

Different levels of saturation in the current transformers (CTs) for external faults produce a false operating current in a differential protection scheme. To avoid relay misoperation, desensitize the relay by selecting the appropriate value of the slope, K.

We use the current-ratio plane to visualize the effect of CT saturation and to determine the relay settings. Figure 4.88 shows the single-line diagram of the power system we use to obtain the current-ratio trajectory caused by CT saturation. As a worst-case scenario, assume that CTs associated with the relay terminal closest to the fault (terminal R) saturate while the local (L) terminal CTs do not. System and CT data are as follows:

X/R:	50 (system impedance angle equal to 89°)
CT ratio:	600/5
CT ANSI/IEEE Class:	C50
CT burden:	2Ω

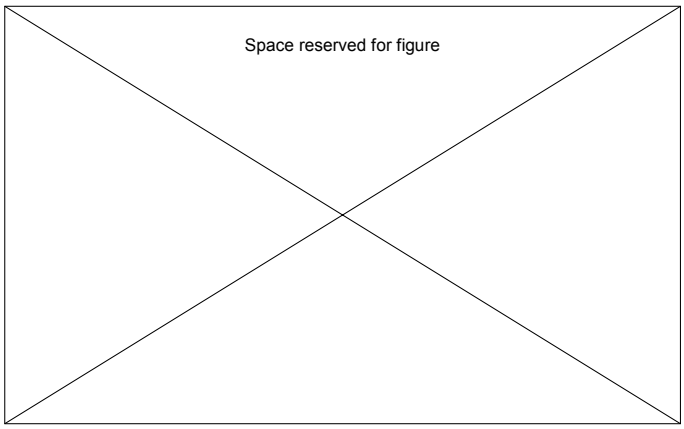


Figure 4.88: Example System Single-Line Diagram

Figure 4.89 shows the secondary CT currents and the resulting differential current for a fault with maximum dc offset that occurs at the location shown in Figure 4.88. Recall that the differential current should be zero for this external fault under ideal conditions. Figure 4.90 shows the resulting currents after analog and digital filtering in the microprocessor-based relay. Note the significant improvement in making the distorted waveforms sinusoidal. There is, however, a significant value of differential current that decreases as the saturated CT pulls out of saturation.

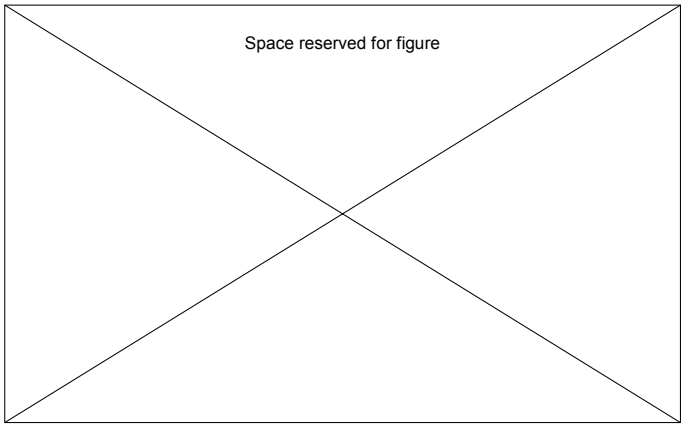


Figure 4.89: Raw Secondary Phase and Differential Currents for the Fault in the Figure 4.23 System

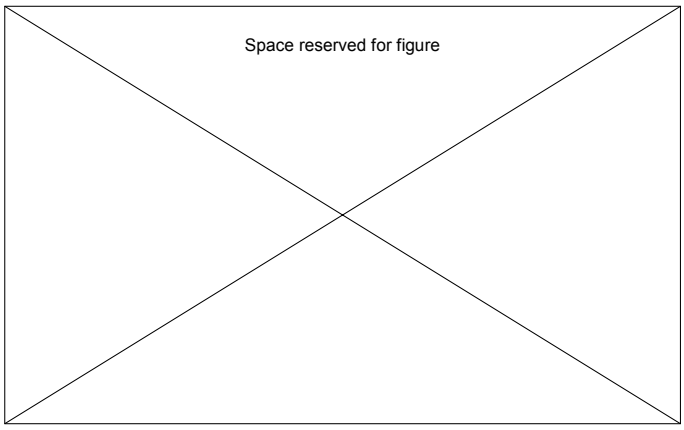


Figure 4.90: Filtered Phase and Differential Currents

Figure 4.91 depicts the current-ratio trajectory corresponding to the filtered currents shown in Figure 4.90. To obtain this figure calculate the fundamental phasor values of currents $\vec{I}_L$ and $\vec{I}_R$, using the output signals of the 16 samples-per-cycle cosine filters. Then determine the phasor $\vec{I}_R / \vec{I}_L$ ratio and plot the result on the complex plane. Select a slope value in the differential relay such that the relay characteristic encloses the entire cluster of points.

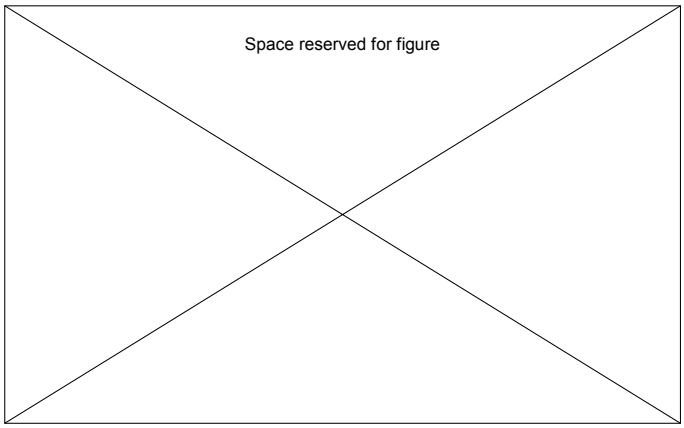


Figure 4.91: Effect of CT Saturation

4.2.7.3.6 Series-Compensated Lines

Series-compensated line protection is one of the most difficult tasks for relay manufacturers and utility protection engineers. Series capacitors introduce a capacitive reactance that changes the typical inductive behavior of the power system for some fault types and locations.

Typical steady-state problems caused by series capacitors are voltage reversals, current reversals, and distance relay reach errors. A voltage reversal occurs for a fault near a series capacitor when the impedance from the relay voltage measuring point to the fault is capacitive. As a result, the relay voltage shifts approximately 180° from its normal position in an inductive system. Voltage inversion causes a directional relay to see a fault on the protected line as being in a reverse direction. A

current reversal occurs when the net reactance from one of the sources to the fault point is capacitive. As a result, the current appears to be entering at one end of the line and leaving at the other for an internal fault (outfeed condition). Current reversals may affect the operation of current-only protection systems. The presence of the series capacitor between the relay voltage measuring point and the fault point also affects the reach estimation of distance relays.

In addition, series capacitors introduce transient effects in the power system. One of these problems is the decaying low-frequency oscillation caused by the LC circuit formed by the capacitor and the system inductance. This causes the impedance estimate of a distance relay to oscillate. As a result, the relay may over- or underreach or have directional discrimination problems. We use the current-ratio plane to show the effect of low-frequency oscillations on current-only systems. Figure 4.92 depicts the one-line diagram of the power system we use to obtain the current-ratio trajectories from the series capacitor.

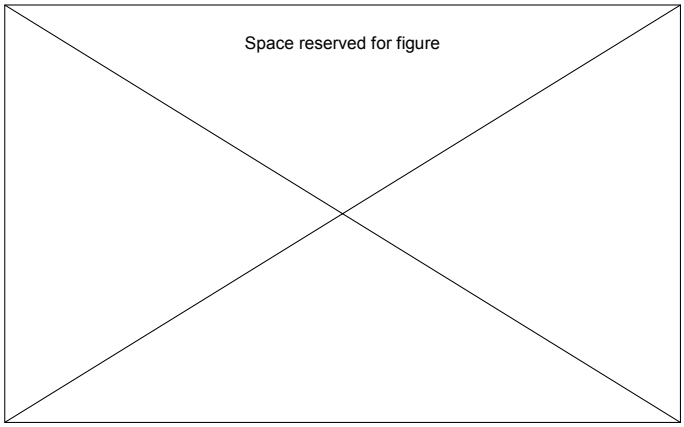


Figure 4.92: Model Power System With Series-Compensated Line

Figure 4.93 (a) shows a typical current-ratio trajectory for an internal fault in the series-compensated line. In general, the trajectory remains in the left semi-plane, but some points are close to the b axis. Figure 4.93 (b) shows the trajectory corresponding to an external fault.

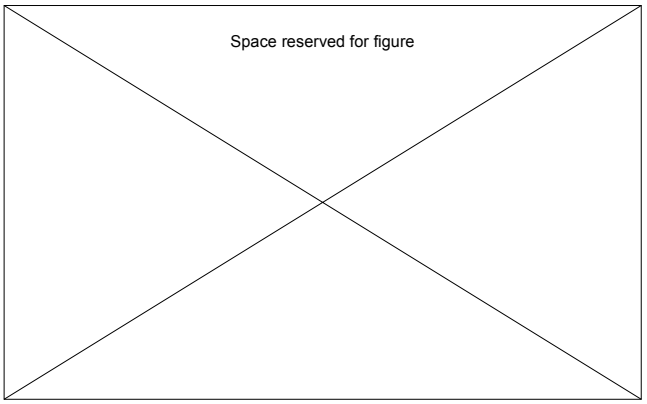


Figure 4.93: Effect of the Series Capacitor

4.2.7.3.7 Alpha-Plane Differential Element for Transmission Line Protection

The key factors to consider when defining the required shape of a line differential relay characteristic in the current-ratio plane are channel time-delay compensation errors, power system impedance nonhomogeneity, CT saturation, and low frequency oscillations in series-compensated lines. We can eliminate the effect of line-charging current and the system power angle using negative- or zero-sequence currents. Design solutions can address the tapped load problem. Then, it is not necessary to take these factors into account to define the shape of the relay characteristic.

The effect of channel time-delay compensation errors is to create a rotation of the ideal fault and load regions in the current-ratio plane (see Figure 4.87). The angle of that rotation equals the error in angle θ created by channel asymmetry. The effect of the system impedance nonhomogeneity is to produce a rotation of the ideal internal fault region in the current-ratio plane (see Figure 4.84). In a worst-case scenario this angle error adds to that produced by channel asymmetry. Figure 4.94 shows the combined effect of channel asymmetry and system impedance nonhomogeneity.

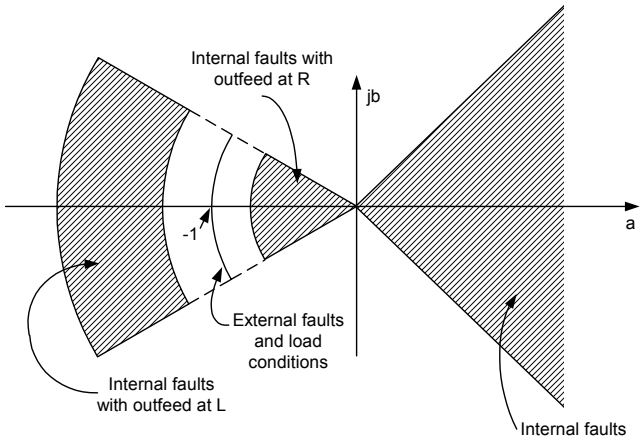


Figure 4.94: Combined Effect of Channel Asymmetry and System Impedance Nonhomogeneity

Figure 4.95 (a) depicts the proposed characteristic of a new differential element for transmission line protection. The relay restraining region in the current-ratio plane is the area between two circle arcs and two straight lines and includes the a = –1 point. We can create this characteristic by combining amplitude and phase comparison. Amplitude comparison provides the circular parts of the characteristic with independent settings R_1 and R_2 (circles radii). Phase comparison provides the linear parts of the characteristic and defines the angular settings α_1 and α_2. Note that we can set the characteristic to match perfectly with the different fault and load regions shown in Figure 4.94 and yet accommodate CT saturation and low-frequency oscillation effects in series-compensated lines. Figure 4.95 (b) shows a simplified version of the new relay characteristic that requires only two settings, R and α. The characteristic is symmetrical with respect to the a axis, and the radii of both circle arcs are reciprocal.

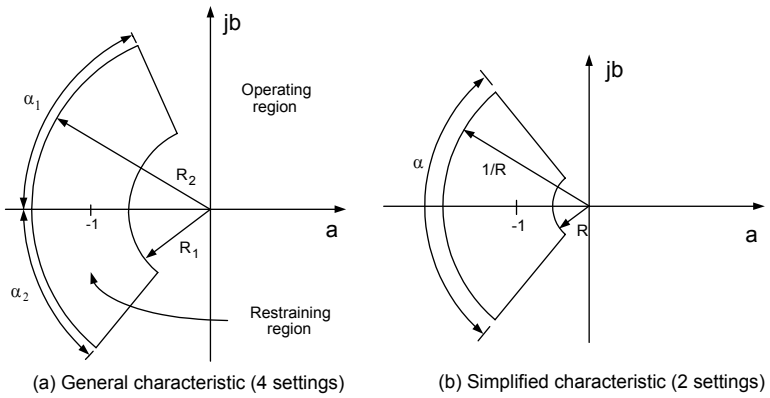


Figure 4.95: Characteristic of the New Differential Element in the Current-Ratio Plane

Figure 4.96 presents a comparison between the new characteristic and that of a traditional differential element (we assume a circular characteristic for simplicity). When we set both relays for the same level of tolerance to outfeed (Figure 4.96 (a)), the traditional differential relay has very low tolerance to channel asymmetry. If we increase the slope of the traditional relay to accommodate a high level of channel asymmetry (Figure 4.96 (b)), the relay loses sensitivity to internal faults with outfeed.

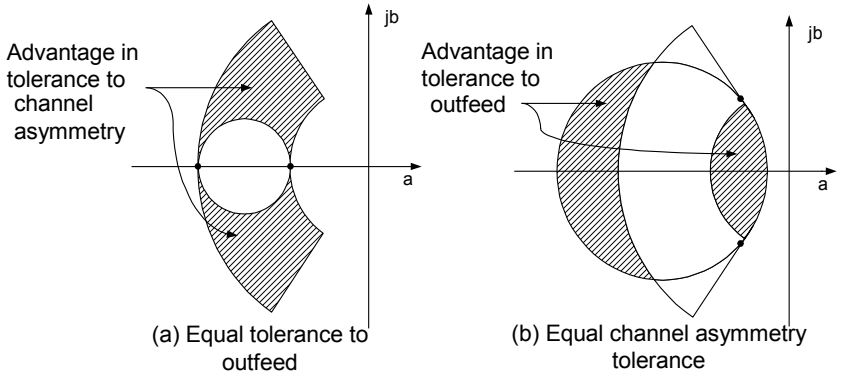


Figure 4.96: Advantages of Alpha-Plane-Based Relay Characteristic Over Traditional Differential Characteristic

Figure 4.97 shows the comparison of the new characteristic with that of charge-comparison systems (see Figure 4.80). For some internal faults in series-compensated lines the current-ratio trajectory may temporarily lie inside the shadowed areas shown in Figure 4.97. A proper selection of α in the new characteristic provides higher operation speed for these faults.

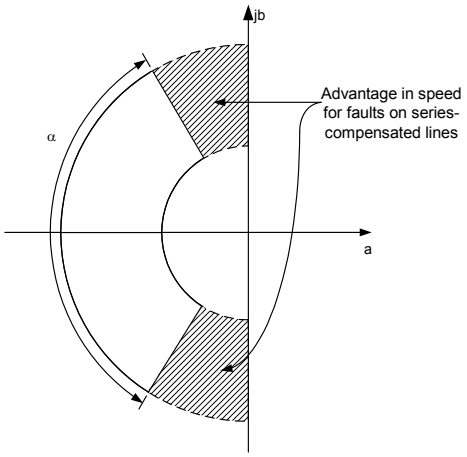


Figure 4.97: Advantage of the Alpha-Plane-Based Relay Characteristic 0ver the Characteristic

Figure 4.98 illustrates the comparison between the new differential element and offset-keying phase-comparison systems. Note that both characteristics look alike, but there are two significant differences between them.

In offset-keying phase-comparison systems the regions inside the inner circle and outside the outer circle represent conditioned operating regions (see Figure 4.82). The system behaves as an overcurrent system in these regions. For internal faults with low contribution at both line ends the phase comparison system fails to operate. In the new differential element the shadowed regions (Figure 4.98) are well-defined operation regions even for low contributions at both ends.

Another difference is that the circle radii are constant in the characteristic of the new differential element (Figure 4.95); in offset-keying system characteristics the circle radii depend on current values.

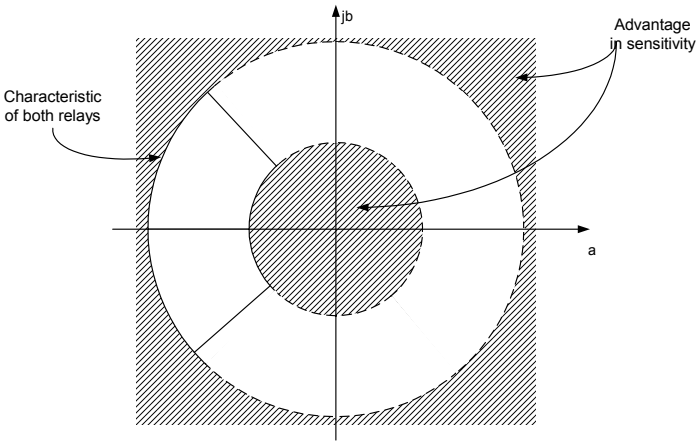


Figure 4.98: Advantage of the New Characteristic Over the Characteristic

Use the phase comparison to generate the linear sectors of the new differential relay characteristic. Equation 4.144 shows the general operation equation of a phase comparator.

$$\theta_1 \le \theta \le \theta_2$$ Equation 4.144

where θ is the angle between $\vec{I}_L$ and $\vec{I}_R$, and θ_1 and θ_2 are constant parameters defining the angular limits of the phase comparator. From Figure 4.95 (b) we may write Equation 4.145 and Equation 4.146.

$$\theta_1 = -\left(\pi - \frac{\alpha}{2}\right)$$ Equation 4.145

$$\theta_2 = \pi - \frac{\alpha}{2}$$ Equation 4.146

Substituting Equation 4.145 and Equation 4.146 into Equation 4.144:

$$-\left(\pi - \frac{\alpha}{2}\right) \le \theta \le \pi - \frac{\alpha}{2}$$ Equation 4.147

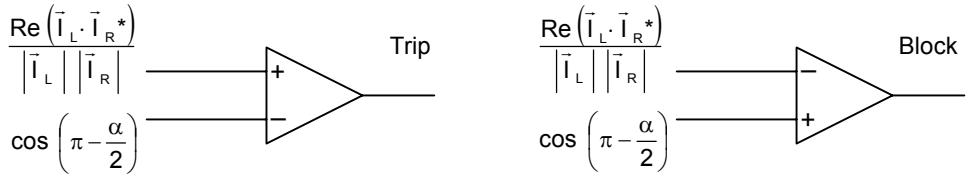
We may also write Equation 4.144 as:

$$\cos\theta \ge \cos\left(\pi - \frac{\alpha}{2}\right)$$ Equation 4.148

Then, we need to use a cosine type of phase comparator. Equation 4.148 takes the form:

$$\frac{\mathrm{Re}\left(\vec{I}_L \cdot \vec{I}_R{}^*\right)}{\left|\vec{I}_L\right| \cdot \left|\vec{I}_R\right|} \ge \cos\left(\pi - \frac{\alpha}{2}\right)$$ Equation 4.149

Figure 4.99 depicts the tripping and blocking logic versions of the phase comparator described by Equation 4.149.



a) Tripping logic b) Blocking logic

Figure 4.99: Logic Diagram of the Phase Comparator

We use amplitude comparison to generate the circle sectors of the relay characteristic. The operating conditions are (see Figure 4.95(a)):

$$\frac{\left|\vec{I}_R\right|}{\left|\vec{I}_L\right|} \le R_1$$ Equation 4.150

$$\frac{\left|\vec{I}_R\right|}{\left|\vec{I}_L\right|} \geq R_2 \qquad \text{Equation 4.151}$$

Figure 4.100 shows the amplitude comparison logic for both the tripping and logic versions of the amplitude comparator described by Equation 4.149 and Equation 4.150.

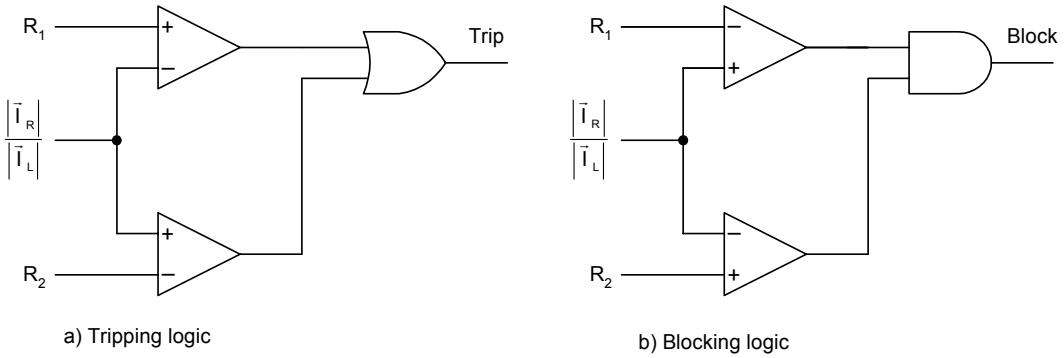


Figure 4.100: Logic Diagram of the Amplitude Comparator

Another alternative for amplitude comparison is:

$$\frac{\left|\vec{I}_L\right| - \left|\vec{I}_R\right|}{\left|\vec{I}_L\right|} \geq 1 - R_1 \qquad (0 \leq R_1 \leq 1) \qquad \text{Equation 4.152}$$

$$\frac{\left|\vec{I}_L\right| - \left|\vec{I}_R\right|}{\left|\vec{I}_L\right|} \leq 1 - R_2 \qquad (R_2 \geq 1) \qquad \text{Equation 4.153}$$

Figure 4.101 depicts the tripping and logic versions of the amplitude comparison given by Equation 4.152 and Equation 4.153.

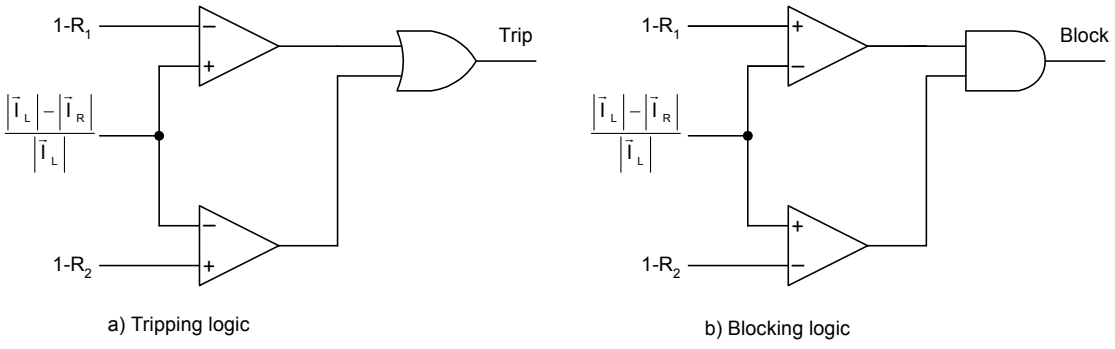


Figure 4.101: Another Alternative of Amplitude Comparison

4.2.8 The traveling wave relay

Whenever a fault occurs on a transmission line, the system transmits voltage and current waves in both directions down the transmission line, starting at the point of the fault, as shown in Figure 4.102. The system also generates a negative voltage step when the line voltage goes to zero. Simultaneously, it generates a current step with magnitude V/Zc where Zc is the characteristic impedance of the transmission line. Detectors at the line terminals mark the time that the first wave fronts are received and compare this time for the times recorded from the other line terminal. As Figure 4.102 shows, there are three fault location possibilities. For faults in Zone 1 and 3, the positive differences between the time recorded by terminals S and D will equal τd, which is the line length divided by the wave propagation velocity. For a fault in Zone 2, the difference will be less than τd. Since the wave propagation velocity is a constant, this approach serves equally well for fault locating as for fault detection.

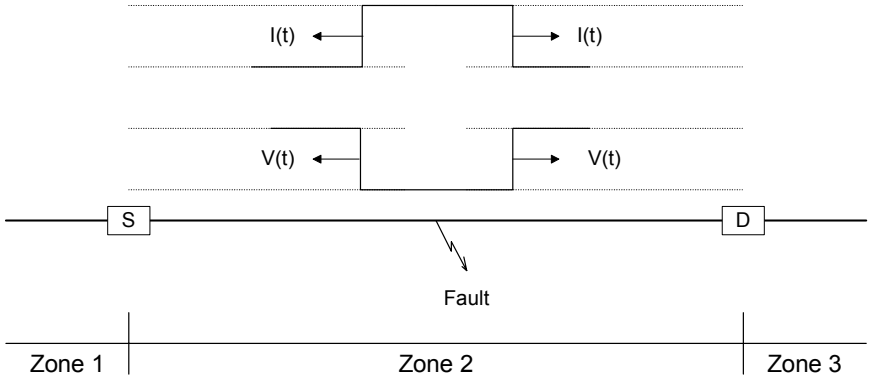


Figure 4.102: Traveling Waves Generated by a Fault

The simplified description above ignores many reality issues. Fault detection is not a simple matter. For multiphase systems such as three-phase power lines, we can break the traveling waves down into modes using transformations similar to symmetrical components. The transformation is selected such that the modal traveling waves are all independent. Fortunately, the propagation velocities for these modes are usually different but deterministic. Figure 4.102 and Figure 4.103 result from a transient simulation using a transient analysis program designed to model power systems. The negative transition at 2 ms is the time of the fault. The transition at 2.2 ms in Figure 4.102 marks the arrival time of the signal propagating in the line mode and the transition at 2.5 ms marks the arrival of the signal propagating in the ground mode.

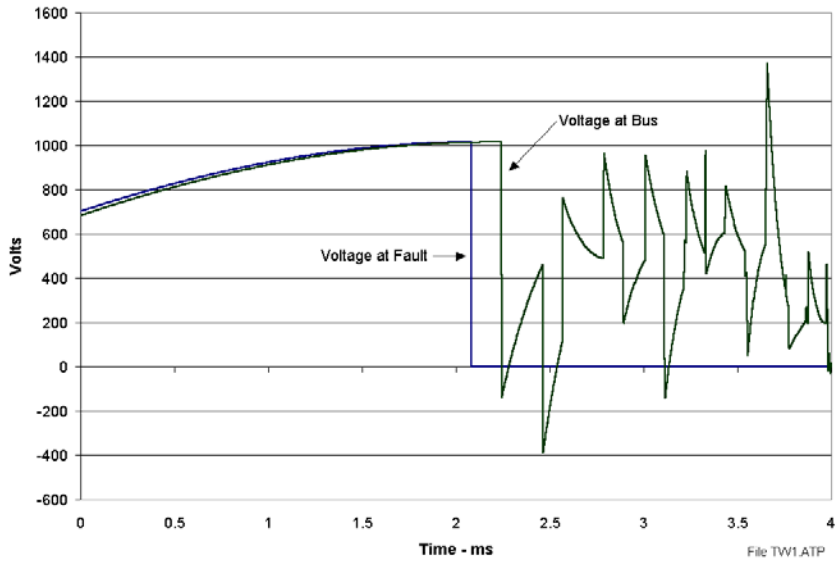


Figure 4.103: Voltage Transient at Terminal S for Simulated Phase-to-Ground Fault a 27 Percent Line Length From Terminal S

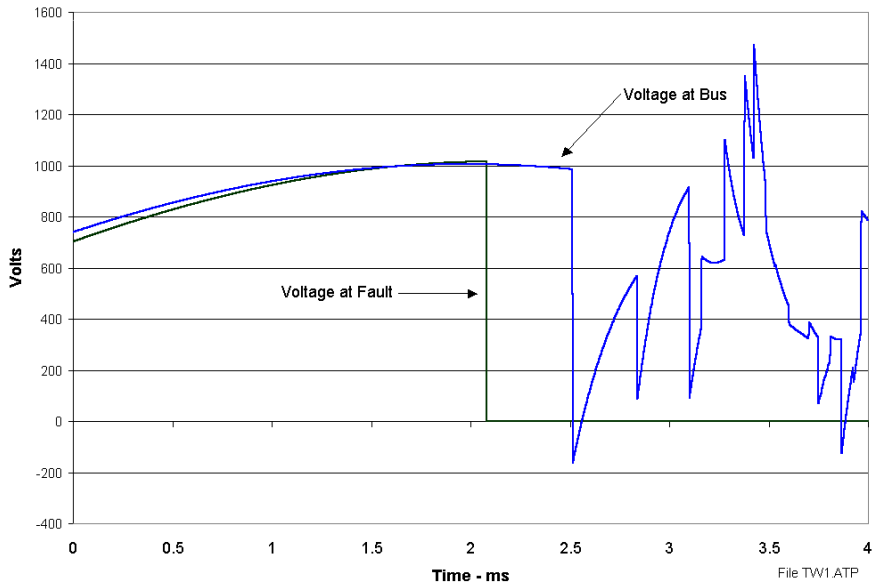


Figure 4.104: Voltage Transients at Terminal D for Simulated Phase-to-Ground Fault a 73 Percent Line Length From Terminal S

Figure 4.103 shows a similar situation. First, note the similarities of the shape of the waveforms up to the first positive transition. The difference is that the transient signals are stretched in Figure 4.103 because of the longer travel distance. The fault inception angle in this simulation generates an optimistic voltage transient.

Figure 4.104 and Figure 4.105 show the current transients generated for this fault simulation. The current at the fault makes a step until a reflection from the closest

terminal is received back at the fault location. These current transients, generated by arcing faults seen at the terminals, are not nearly as distinct as the voltage transients. Hence voltage-based detectors are normally used for traveling wave relays. Since lightning strikes produce a more pronounced current transient, some relays use both current and voltage wavefront detectors.

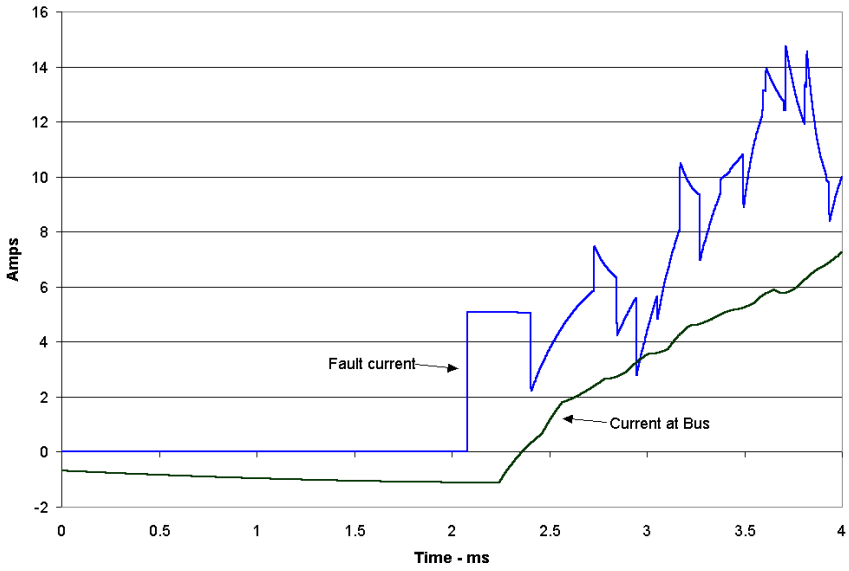


Figure 4.105: Current Transients at Terminal S for Simulated Phase-to-Ground Fault a 27 Percent Line Length From Terminal S

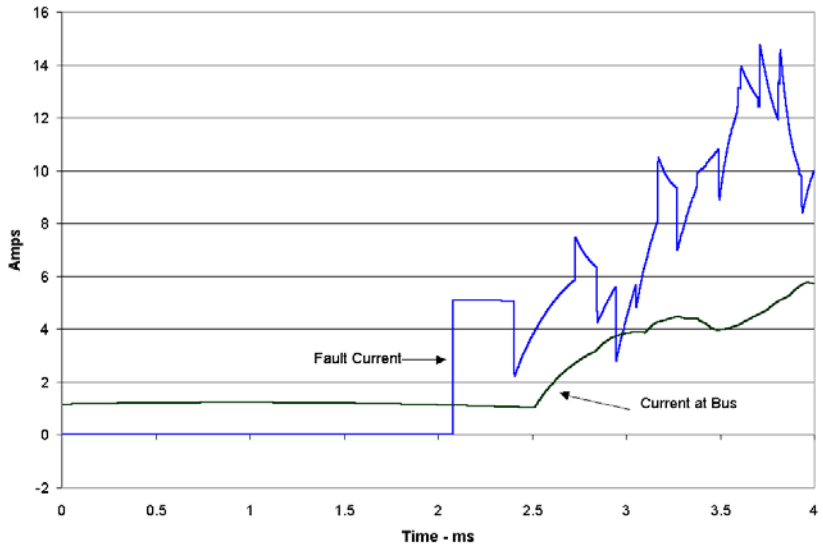


Figure 4.106: Current Transients at Terminal D for Simulated Phase-to-Ground Fault a 73 Percent Line Length From Terminal S

4.3 FAULT IDENTIFICATION

Fault identification is necessary for the protection zone concept to work correctly. Fault identification includes one or more of the following elements: direction, distance, type, and magnitude (or impedance). Fault identification functions are usually independent of the fault detection algorithms. Fault location is usually differentiated from distance to a fault in that the distance result, as it relates to a zone of protection, i.e. either in a particular zone or not, is usually a binary output indicating whether the fault is within a set percentage of the length of the line in Zone 1 or not. Fault locating is a background computing function for three reasons: to not interfere with the primary objective of line protection and to permit higher accuracy computations by allowing transients to dissipate and use algorithms that are more time consuming.

4.3.1 Transient response of directional algorithms

Microprocessor-based relays are subject to two types of transients, the algorithm transient and the network transient. These transients produce indeterminate results and may produce incorrect operations if remedial action is not taken to ensure the validity of the result.

The algorithm transient is generated by the finite response of the algorithm that converts the sampled data to RMS voltages and currents using either vector or complex notation. Relays that use a synchronously sampled cosine filter to determine both real and imaginary components require 5/4 cycles of the nominal frequency fundamental to reach steady state. (Relays frequently operate on levels detected before steady state is reached.) This means that for a step change on the input of the 60 Hz input, the filter requires 20.833 ms before the filter output achieves steady state. (See filtering section.) Figure 4.107 shows this characteristic for the time period 0 to 0.025 seconds of the simulation time. Assuming that all inputs are sampled simultaneously and assuming zero processing time for computations, the 20.833 ms transient delay is the best that a relay can theoretically achieve.

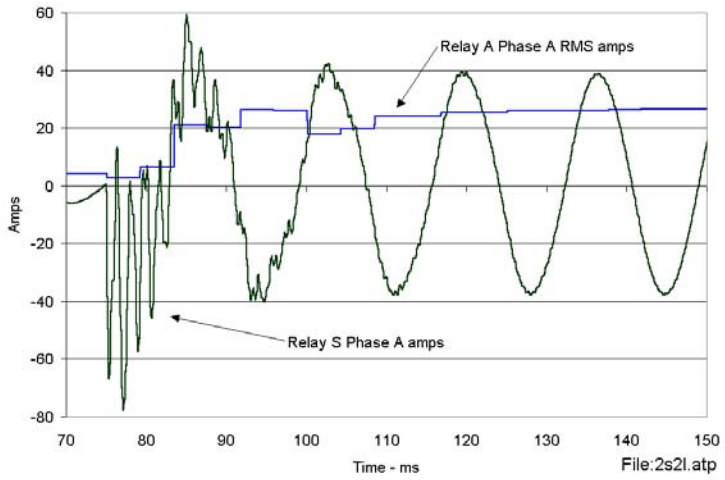


Figure 4.107: Phase-A Current Step Response

Practically speaking, most relays use fewer AD (analog to digital) converters than the number of analog channels to be sampled. This converter to channel mismatch can skew the input sampling. Also, the algorithm computational time is finite, significantly limiting the number of samples that can be processed in a given sampling interval. The interval between samples is generally controlled by processor interrupts, so phase errors generated by sample skew are reduced or eliminated by phase compensation in the computer program. Since the algorithms are closed form (requires a single pass with no decision branched in the computer code), the execution time is predictable to a high degree. A hardware solution to sample skew is to use a multichannel sample-and-hold IC that captures all analog inputs at the same instant. This solution eliminates sample skew if all processing is completed before the next set of samples are taken, so a single AD converter can then process the data in any order without being affected by skew.

Power system electrical network generated transients produce signals over a wide band of frequencies because the step change of the AC signal contains high frequencies and excites the natural modes of the network. Figure 4.107 depicts this phenomena starting at simulation time 0.075 ms. The RMS output from the cosine filter now requires much longer to achieve steady state. The filtering nature of the algorithms that converted the sampled data to RMS values reduces the effects on relay performance from transients generated by the network. Figure 4.108 is a normalized plot of the energy spectrum of phase A for a phase-A-to-ground fault. The majority of the energy is confined to the fundamental of the driving function from the power source. Figure 4.108 also shows the natural modes of the network.

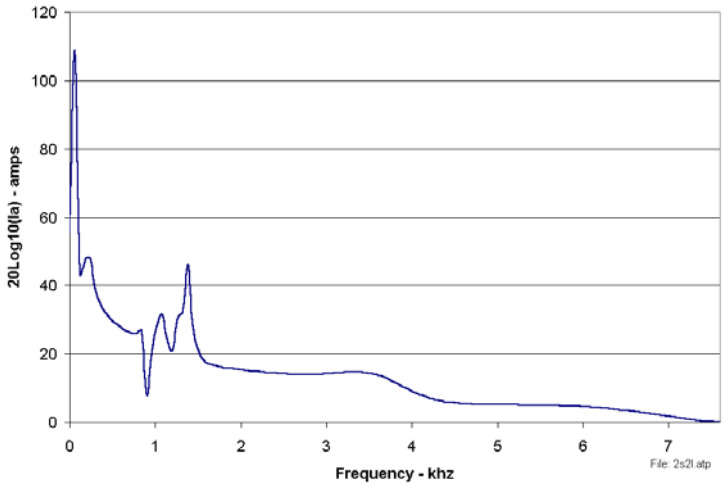


Figure 4.108: Frequency Spectrum for Phase-to-Ground Fault

Figure 4.110 through Figure 4.113 show the simulated results of a system for a fault at location F1 in Figure 4.109. The phase-A-to-ground fault is applied at a distance from bus V2 equal to 10 percent of the line length. For this simulation, sources Es and Er are in phase, so there is no prefault load current. The transmission line model was for an unbalanced line. The consequences of using this model are more evident by letting Es lead or lag Er to provide prefault loading. Plot the direction results for the relays at opposite ends of the same transmission line together. For these plots, results for relays at node V2 have the suffix S and those for node at V4 have a suffix of R. To provide a timing reference, the four plots include the phase-A current

leaving V2. To allow plotting torque with phase-A current, we normalize the torque plots to the maximum absolute value of the torque during the simulation. In reality, the torque magnitude can peak into the thousands depending on the fault location and source impedance.

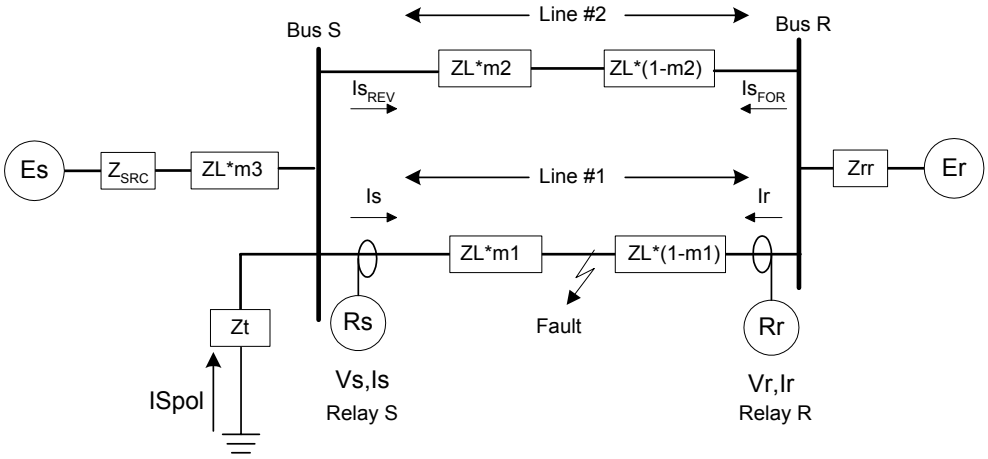


Figure 4.109: Single-Line Diagram of a System With Two Sources Connected by a Double Circuit

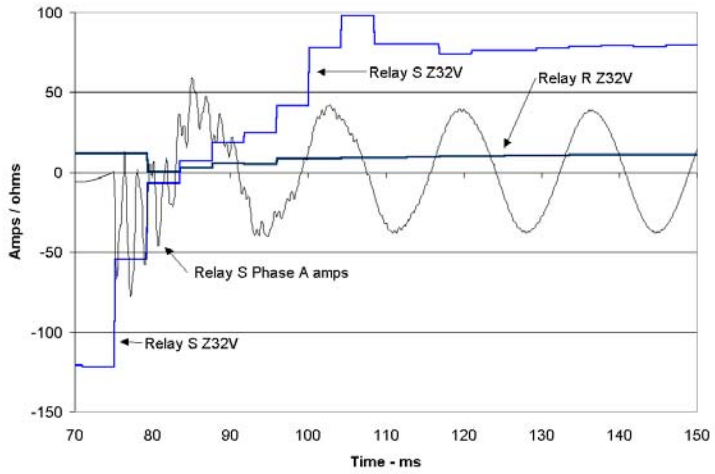


Figure 4.110: Transient Response of Zero-Sequence Torque Models for Relays at S and R (EMTP File: 2l2s.atp).

Algorithm transient response causes the initial transient. The torque and impedance transients after 0.75 ms reflect the results of processing the transient voltage and currents. Relay designers must investigate the direction algorithms used in their particular relays to inhibit the trip decision until there is a high probability that the direction results are valid. Figure 4.113 shows that the negative direction torque for node V4 briefly declared the direction in the reverse direction. This may have delayed tripping but would not have resulted in an incorrect operation.

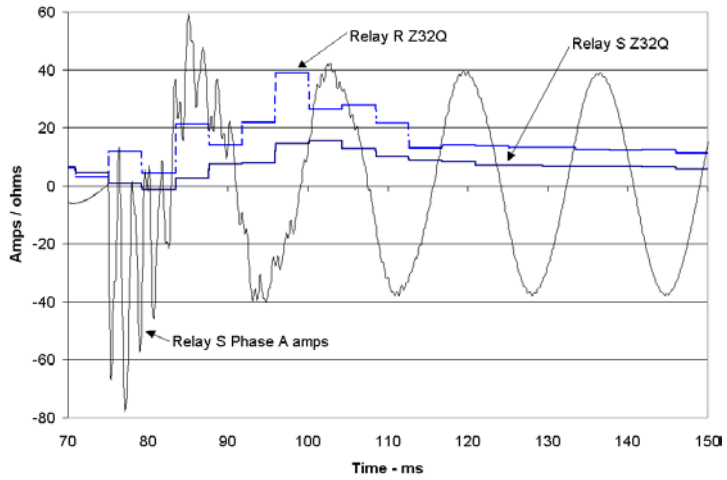


Figure 4.111: Direction by Negative-Sequence Impedance for Relays at V2 and V4

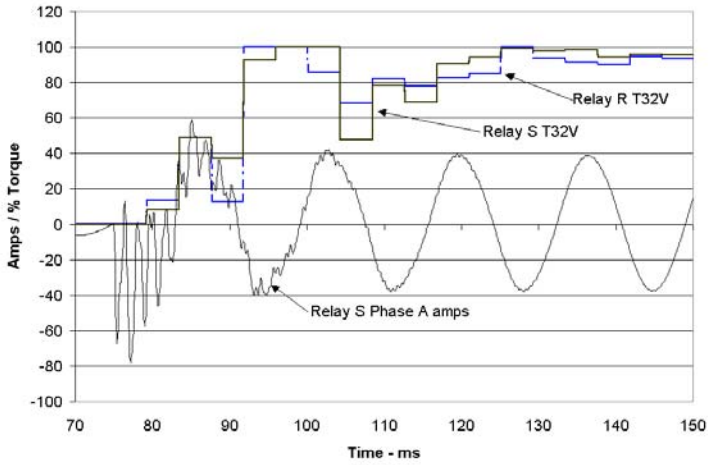


Figure 4.112: Direction by Zero-Sequence Torque for Relays at V2 and V4

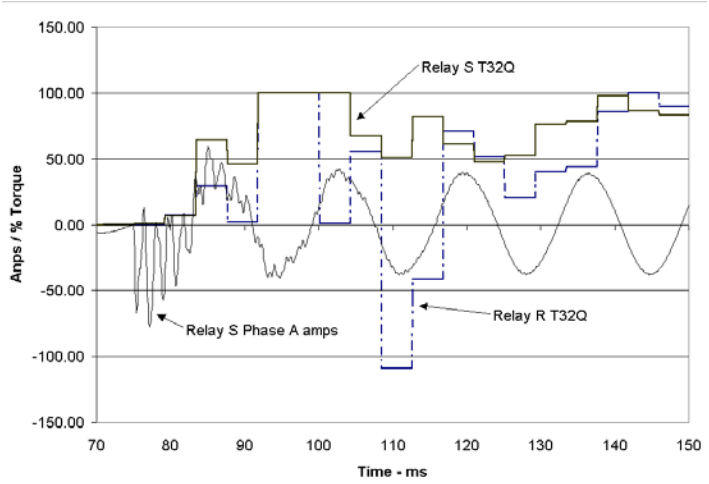


Figure 4.113: Direction by Negative Torque Impedance for Relays at V2 and V4

4.3.2 Fault type identification

Fault identification is important for two reasons, some distance elements tend to overreach due to load current and to identify the faulted phase for single phase tripping. In the presence of load flow and fault resistance, the ground distance elements associated with the faulted phases can exhibit severe overreaching tendencies. Fault type selection logic is needed to block selected ground distance elements for phase-to-phase-to-ground faults. In applications with strong sources behind the relay location, a forward direction close-in single-line-to-ground (SLG) fault can cause one or more phase-to-phase distance elements to assert. These same phase-to-phase distance elements assert for close-in phase-to-phase faults. If single-pole tripping is required, only the faulted phase requires interruption. Multiple phase faults require opening all three breaker poles. Assertion of the phase-to-phase distance elements for a SLG fault can cause an undesired three-pole trip.

Protective relaying schemes using distance elements to detect faults along the protected line must have logic that dependably distinguishes fault type for both simple and complex faults.

4.3.2.1 Fault selection using torque magnitude

Many microprocessor relays incorporate memory polarization for phase-to-phase and phase-to-ground distance elements, as described in section 4.5.2.4. Using a memory polarization approach, as in the methods discussed in section 4.6.1.2**,** expands the mho circle characteristics that allow the relays to operate correctly for higher resistive faults. While these expanded (and dynamic) mho elements give more coverage for resistive faults, they are also more likely to operate for unintended fault types than are self-polarized mho elements

The following exercise illustrates the phenomena described above. Consider an unloaded radial system with a close-in A-phase-to-ground fault as shown in Figure 4.114. For this case the reach of the relay as set by the parameter *m* in Equation 4.57 (see 4.1.1.4) is 300 percent. The apparent impedance and relay element torque quantities for overreaching Zone 3 distance elements for various values of fault

resistance are computed using Equation 4.154 and Equation 4.57 through Equation 4.62.

$$Zapt_{\text{fault type}} = V/I \qquad \text{Equation 4.154}$$

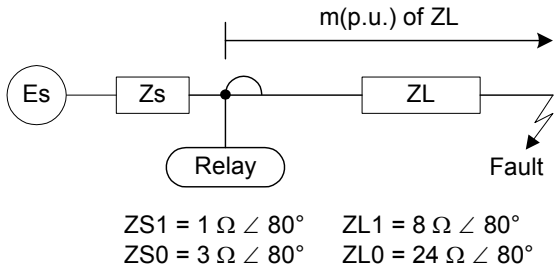


Figure 4.114: Example System Single-Line Diagram

The parameters, V and I, in Equation 4.154 are defined in Table 4.6 for the six types of fault. Table 4.9 lists the results of these computations. Figure 4.115 plots the apparent impedance on a R-X impedance plane diagram with the circle representing the 300 percent reach. The expanded circle shows the memory voltage effect on the characteristic. Note that the mho characteristic passes through the source impedance. Apparent impedances lying inside the mho circle are detected as faults.

Table 4.9: Results of Torque and Apparent Impedances Computations as Seen by the Relay for Fault Resistance, RF, Equal to 0, 2, 4, 6, and 8 Ohms for a Forward Fault Close to the Relay (ZL » 0)

R_F	T_{AG}	$\lvert Z_{AG}\rvert$	T_{BG}	$\lvert Z_{BG}\rvert$	T_{CG}	$\lvert Z_{CG}\rvert$	T_{AB}	$\lvert Z_{AB}\rvert$	T_{BC}	$\lvert Z_{BC}\rvert$	T_{CA}	$\lvert Z_{CA}\rvert$
0	118	0.0	-30	3.1	-29	3.1	56	2.1	0	∞	55	2.1
1	81	0.6	-38	4.1	-6	3.3	50	2.6	0	∞	22	3.2
2	46	1.2	-33	5.2	2.7	4.1	34	3.9	0	∞	3	4.7
3	28	1.8	-27	6.5	4.2	5.2	22	5.5	0	∞	-5	6.3
4	17	2.4	-23	7.9	4.0	6.5	15	7.1	0	∞	-8	8.0

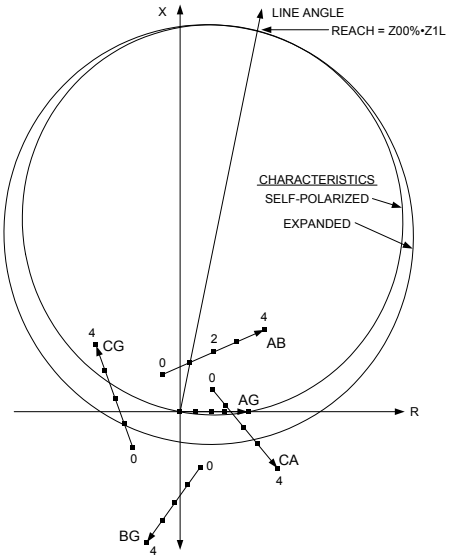


Figure 4.115: Apparent Impedances Seen by the Relay for Fault Resistance Values Listed in Table 4.14 for a Close-In Fault

From Table 4.9 and Figure 4.115, notice the following:

Multiple distance elements detect the A-phase ground fault when $R_F = 0$. In our example, the A, AB and CA elements all detect the fault. All of the noted elements use A-phase voltage and current quantities. This also emphasizes the need to block the AB and CA elements for single-pole trip applications.

With increasing fault resistance, the number of elements that detect the fault decreases.

With increasing fault resistance, the C-phase ground distance element develops positive operating torque.

Table 4.10 shows the results for torque and apparent impedances seen by each distance element for faults placed at 25 percent increments along the protected line section with the fault resistance set to zero. Figure 4.116 plots the apparent impedance on a R-X impedance plane diagram with the circle representing the 300 percent reach.

Table 4.10: Results of Torque and Apparent Impedance Computations as Seen by the Relay for Zero Fault Resistance and Fault Locations of 0, 25, 50, 75 and 100 Percent of the Line Length

m(%)	T_{AG}	$\|Z_{AG}\|$	T_{BG}	$\|Z_{BG}\|$	T_{CG}	$\|Z_{CG}\|$	T_{AB}	$\|Z_{AB}\|$	T_{BC}	$\|Z_{BC}\|$	T_{CA}	$\|Z_{CA}\|$
0	118	0.0	-30	3.1	-29	3.1	56	2.1	0	∞	55	2.1
25	36	2.0	-13	8.0	-13	8.0	13	7.8	0	∞	13	7.8
50	20	4.0	-9.9	13	-9.7	13	4.3	13	0	∞	4.1	13
75	13	6.0	-8.5	18	-8.3	18	0.7	19	0	∞	0.5	19
100	9	8.0	-7.7	23	-7.6	23	-1.4	25	0	∞	-1.5	25

Again, as expected, the distance elements involved with A-phase pickup for faults near the bus. As we move the fault placement away from the bus, the positive torque quantities produced by these elements decreases. For the A-phase ground fault placed at m = 1.0, only the A-phase ground distance element produces positive operating torque-like quantities. This shows that fault selection for remote faults without fault resistance is easily determined by reviewing which distance element loop elements are picked up. However, we cannot make this observation for close-in faults.

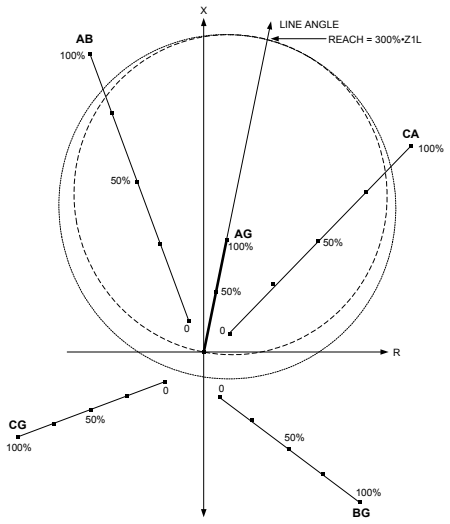


Figure 4.116: Apparent Impedances Seen by Varying Fault Location With Zero Fault Resistance

4.3.2.2 Fault selection using current phase relationships

Fault selection logic differentiates between single-line-to-ground faults and phase-to-phase-to-ground faults with resistance to ground under a wide range of system conditions. This method uses the angle between negative-sequence current (Ia2) and zero-sequence current (Ia0) to identify the fault type and faulted phase(s). It also

qualifies the ∠(Ia0 - Ia2) measurement with apparent fault resistance measurements described in the previous section.

The fault selection logic first compares the phase angle between Ia_0 and Ia_2. If the fault type is phase-A-to-ground (AG), the angle difference between Ia2 and Ia0 is ±30°. For a phase-B-to-ground (BG) fault, this angle difference is 120° ±30° and for a phase-C-to-ground (CG) fault this angle difference is -120° ±30°. Faults that result in angular differences of Ia0 and Ia2 outside of these sectors require additional evaluation to declare the fault type.

Figure 4.117 illustrates the phase vectors and phase angle relationship between Ia2 and Ia0 for the three possible single-line-to-ground faults. Figure 4.118 shows the phase relationship of Ia2 and Ia0 for a phase-B-to-C-to-ground (BCG) fault with differing amounts of fault resistance. The angle differences between Ia2 and Ia0 are zero degrees for both fault types as shown in Figure 4.117 (AG fault) and Figure 4.118 (BCG fault) for R_F equal to zero. This result is desirable because for the BCG fault the AG distance elements are enabled while the BG and CG distance elements are blocked. Since the distance element for the AG fault will not pickup, enabling the AG output by the fault selector logic does no harm. The angle difference for Ia0 and Ia2 between the AG and BCG faults becomes non-zero with increasing fault resistance, as shown in Figure 4.118.

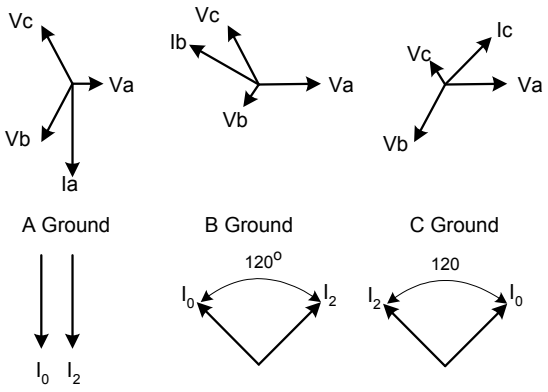


Figure 4.117: Angle Relationship of Ia2 and Ia0 for Ground Faults

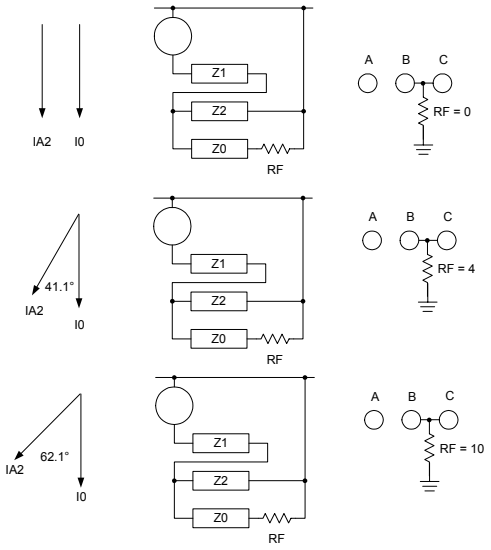


Figure 4.118: Phase Angle Relationship of Ia2 and Ia0 for BCG Faults and Symmetrical Component Networks That Represent the Faults

Three outputs are available from the fault selector logic, one for each of the three possible ±60° segments shown in Figure 4.119. The fault selection logic described by Equation 4.156 through Equation 4.161 enables or blocks phase-to-ground and phase-to-phase elements as listed in Table 4.11.

The phase-to-phase fault resistance can be developed using an approach similar to the phase-to-ground resistance. The circuit model present in section 4.6.3.3 results in Equation 4.74. Solving for Rbc_F in that equation results in Equation 4.55. Again, since the per-unit distance to the fault, m, is a scalar constant in both numerator and denominator, it can be eliminated as shown in Equation 4.56. This equation also substitutes the equivalent negative-sequence current on the assumption that the load and the line impedance are balanced pre-fault. Making this substitution minimizes the errors introduced by load current. Equation 4.157 and Equation 4.161 follow similar development for AB and CA phase-to-phase faults.

$$Rbc_F = \frac{\mathrm{Im}\left[Vbc\left(\overline{Ibc\ m\ Z1}\right)\right]}{\mathrm{Im}\left[Ibc\left(\overline{Ibc\ m\ Z1}\right)\right]} \qquad \text{Equation 4.155}$$

$$Rbc_F = \frac{\mathrm{Im}\left[Vbc\left(\overline{Ibc\ Z1}\right)\right]}{\mathrm{Im}\left[j\sqrt{3}Ia_2\left(\overline{Ibc\ Z1}\right)\right]} \qquad \text{Equation 4.156}$$

$$Rab_F = \frac{\mathrm{Im}\left[Vab\left(\overline{Iab\ Z1}\right)\right]}{\mathrm{Im}\left[ja^2\sqrt{3}Ia_2\left(\overline{Iab\ Z1}\right)\right]},\ a^2 = 1\angle 240° \qquad \text{Equation 4.157}$$

$$Rca_F = \frac{\mathrm{Im}\left[Vca\left(\overline{Ica\ Z1}\right)\right]}{\mathrm{Im}\left[ja\sqrt{3}Ia_2\left(\overline{Ica\ Z1}\right)\right]},\ a = 1\angle 120° \qquad \text{Equation 4.158}$$

The ground distance elements not associated with the identified phase are blocked. If the output from the fault selector logic is the fourth condition then all phase-to-ground distance elements are blocked.

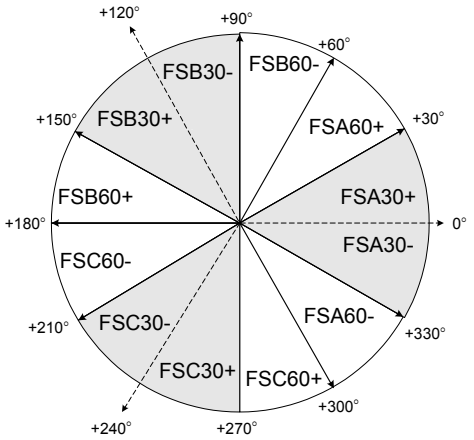


Figure 4.119: Regions of Angle Difference Between Negative- and Zero-Sequence Currents for Fault Selection

Table 4.11: I_0 - I_2 Phase-Comparison Fault Selection Logic

Fault Type	Enabled	Blocked
1	AG and BC	BG, CG, BC, and CA
2	BG and AC	AG, CG, AB, and BC
3	CG and AB	AG, BG, BC, and CA
4	AB, BC, CA	All but ABC-G

$$\text{Fault Type1} = \text{FSA30} + \text{FSA60} \bullet Z_{AB-MIN} \bullet \left(|R_{AG}| < |R_{AB}|\right) + \text{FSA60} \bullet Z_{BC-MIN} \bullet \left(|R_{AG}| < |R_{BC}|\right) + \text{FSA60} \bullet Z_{CA-MIN} \bullet \left(|R_{AG}| < |R_{AC}|\right) \quad \text{Equation 4.159}$$

$$\text{Fault Type2} = \text{FSB30} + \text{FSB60} \bullet Z_{AB-MIN} \bullet \left(|R_{BG}| < |R_{AB}|\right) + \text{FSB60} \bullet Z_{BC-MIN} \bullet \left(|R_{BG}| < |R_{BC}|\right) + \text{FSB60} \bullet Z_{CA-MIN} \bullet \left(|R_{BG}| < |R_{AC}|\right) \quad \text{Equation 4.160}$$

$$\begin{aligned}\text{Fault Type 3} &= \text{FSC30} \\ &+ \text{FSC60} \bullet Z_{AB-MIN} \bullet \left(|R_{CG}| < |R_{AB}|\right) \\ &+ \text{FSC60} \bullet Z_{BC-MIN} \bullet \left(|R_{CG}| < |R_{BC}|\right) \\ &+ \text{FSC60} \bullet Z_{CA-MIN} \bullet \left(|R_{CG}| < |R_{AC}|\right)\end{aligned}$$

Equation 4.161

$$Z_{AB-MIN} \Rightarrow mZ_{AB} < mZ_{BC} \text{ and } mZ_{AB} < mZ_{CA}$$

$$Z_{BC-MIN} \Rightarrow mZ_{BC} < mZ_{AB} \text{ and } mZ_{BC} < mZ_{CA}$$

Equation 4.162

$$Z_{CA-MIN} \Rightarrow mZ_{CA} < mZ_{BC} \text{ and } mZ_{CA} < mZ_{AB}$$

$$mZ_{AB,BC,CA} = \frac{\text{Im}\left(V_{AB} \cdot \overline{I_{AB,BC,CA}}\right)}{\text{Im}\left(\frac{ZL_1}{|ZL_1|} I_{AB,BC,CA} \cdot \overline{I_{AB,BC,CA}}\right)}$$

Equation 4.163

$$mZ_{A,B,C} = \frac{\text{Im}\left(V_{A,B,C} \cdot \left(\overline{I_{A,B,C}}\right)\right)}{\text{Im}\left(\frac{ZL_1}{|ZL_1|} \cdot \left(I_{A,B.C} + k_0 I_R\right)\left(\overline{I_{A,B,C}}\right)\right)}$$

Equation 4.164

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Equation 4.165

This method requires computation of the fault resistance. Do this by writing the loop equations for the various fault conditions. Equation 4.171 through Equation 4.175 provide the results, while sections 4.1.1.5.1 and 4.1.1.5.2 develop the fundamental approach. The difference is solving for the fault resistance instead of for the per-unit distance to the fault. For example, starting with Equation 4.176, both sides of the equation are multiplied by the complex conjugate of the expression shown in Equation 4.166, resulting in Equation 4.167. The first term on the right side of the equal sign is real, so can be eliminated by keeping only the imaginary part as shown in Equation 4.168. Note that both sides of Equation 4.168 are scaled by the per-unit distance to the fault, m, and may be divided out without altering the equality. This means that the algorithm is valid regardless of the distance to the fault. This conclusion is constrained by the caveats listed in 4.3.3. When the system and load is nearly balanced I_1, I_2. and I_0 are all approximately equal. This allows use of the approximation of Equation 4.170, resulting in Equation 4.171. Develop similar expressions for *Rbg* and *Rcg* simply by substituting the appropriate phase-to-ground voltage and phase current into Equation 4.171.

$$Va = Ia(mZL_1) + Ia \cdot Rag$$

Equation 4.166

$$\begin{aligned}&Va\ \overline{(m(Ia\ ZL_1))} \\ &= m(Ia\ ZL_1)\overline{(m(Ia\ ZL_1))} + (Ia\ Rag)\overline{(m(Ia\ ZL_1))}\end{aligned}$$

Equation 4.167

$$\text{Im}\left[Va\ \overline{(m(Ia\ ZL_1))}\right] = \text{Im}\left[(Ia\ Rag)\overline{(m(Ia\ ZL_1))}\right]$$

Equation 4.168

$$Rag = \frac{Im\left[Va\ \overline{(Ia\ ZL_1)}\right]}{Im\left[(Ia)\overline{(Ia\ ZL_1)}\right]} \qquad \text{Equation 4.169}$$

$$Ia \cong \frac{3}{2}(Ia_0 + Ia_2) \qquad \text{Equation 4.170}$$

$$Rag = \frac{Im\left[Va\ \overline{(Ia\ ZL_1)}\right]}{Im\left[\left(\frac{3}{2}(Ia_0 + Ia_2)\right)\overline{(Ia\ ZL_1)}\right]} \qquad \text{Equation 4.171}$$

Develop the phase-to-phase fault resistance using an approach similar to the phase-to-ground resistance. The circuit model in section 4.1.1.5.2 results in Equation 4.92. Solving for Rbc_F in that equation results in Equation 4.172. Again, since the per-unit distance to the fault, m, is a scalar constant in both numerator and denominator, you can eliminate it as shown in Equation 4.173. This equation also substitutes the equivalent negative-sequence current on the assumption that the load and the line impedance are balanced pre-fault. Making this substitution minimizes the errors introduced by load current. Equation 4.174 and Equation 4.175 follow similar development for AB and CA phase-to-phase faults.

$$Rbc_F = \frac{Im\left[Vbc\left(\overline{Ibc\ m\ ZL_1}\right)\right]}{Im\left[Ibc\left(\overline{Ibc\ m\ ZL_1}\right)\right]} \qquad \text{Equation 4.172}$$

$$Rbc_F = \frac{Im\left[Vbc\left(\overline{Ibc\ ZL_1}\right)\right]}{Im\left[j\sqrt{3}Ia_2\left(\overline{Ibc\ ZL_1}\right)\right]} \qquad \text{Equation 4.173}$$

$$Rab_F = \frac{Im\left[Vab\left(\overline{Iab\ ZL_1}\right)\right]}{Im\left[ja^2\sqrt{3}Ia_2\left(\overline{Iab\ ZL_1}\right)\right]},\ a^2 = 1\angle 240° \qquad \text{Equation 4.174}$$

$$Rca_F = \frac{Im\left[Vca\left(\overline{Ica\ ZL_1}\right)\right]}{Im\left[ja\sqrt{3}Ia_2\left(\overline{Ica\ ZL_1}\right)\right]},\ a = 1\angle 120° \qquad \text{Equation 4.175}$$

4.3.3 Fault Location (Contributing author - Jeff Roberts)????

Accurate fault location information is valuable to both operations personnel and protection engineers. Fault location is important to power system protection because it provides the feedback necessary to validate the performance of the protection system. The algorithms for determining fault location are very similar to the ones for distance relaying. However, since fault locating is performed off-line, the algorithm can be significantly more complex, requiring more time to achieve greater accuracy. Additionally, this time permits collecting information from other terminals of the protected line to further improve the accuracy of the computed fault location.

Single-ended, impedance-based fault location has become a standard feature in most of today's microprocessor-based protective relays.[67,68] In fact, many digital fault recorder manufacturers offer fault location as an option. Single-ended fault location is attractive because it is simple, fast, and does not require communications with

remote terminal devices. However, there are applications that can create undesirably large errors in fault location results.

Specifically these applications are those with:

- Strong zero-sequence mutual coupling
- Multiple remote terminals (most commonly three-terminal applications)
- Large angle differences between power system sources and the protected line
- Nontransposed transmission lines

Existing double-ended impedance-based fault locating methods can improve upon the accuracy of single-ended methods. Traditionally, these methods either require the phase alignment of data sets captured at both ends of a monitored line or communicate a significant amount of data. Advances in fault locating algorithms include: data sets do not rely on pre-fault data or require alignment, data volume communicated between relays is small enough that the data can easily be transmitted using a digital protection channel, and the system works well for three-terminal lines.

4.3.3.1 Fault location for single-phase single-terminal lines (Distance Mho)

If a single-phase line has a single source (shown in Figure 4.114), all the quantities can be measured at the relay to determine the impedance to the fault.[69] These quantities are the line-to-ground voltage and the phase current illustrated in Figure 4.120 and expressed in Equation 4.166. Z_L is the positive-sequence line impedance for the total line length and the *m* multiplier is the fraction of the total line length to the fault. R_F is the fault resistance and usually assumed to be purely resistive. The focus of fault locating is to determine the value of *m* in Equation 4.166. Rearranging Equation 4.166 into Equation 4.167 shows that the value computed for *m* is dependent on the fault resistance, which is not normally measurable. Eliminate the term involving fault resistance by first multiplying Equation 4.166 by the complex conjugate of the current *Ia* as shown in Equation 4.168. Since RF is assumed to be purely resistive, the term in Equation 4.168 has no imaginary component. As Equation 4.169 shows, we can take only the imaginary part of Equation 4.168 and solve for *m* without knowing the fault resistance. As subsequent derivations demonstrate, this procedure to eliminate an unwanted term (for whatever reason) is used extensively. The procedure is valid for this case because of the assumption that R_F is purely resistive.

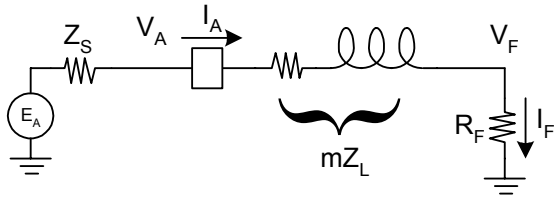


Figure 4.120: Single-Line-to-Ground Fault on a Radial Feed System

$$Va = Ia\,(mZl_L + R_F) = m\,(Ia\,Zl_L) + Ia\,R_F \qquad \text{Equation 4.176}$$

$$m = \frac{Va - Ia\,R_F}{Ia\,Zl_L}$$ Equation 4.177

$$Va\ \overline{Ia} = m\,(Ia\,Zl_L)\,\overline{Ia} + (Ia\,R_F)\,\overline{Ia}$$ Equation 4.178

$$m = \frac{Im\left[Va\ \overline{Ia}\right]}{Im\left[(Ia\,Zl_L)\,\overline{Ia}\right]}$$ Equation 4.179

4.3.3.2 Fault location for single-line-to-ground faults for multiphase lines

Zero-sequence coupling between phases requires compensation for accurate fault locating. The circuit now appears as the model shown in Figure 4.123, which includes the effects of the parallel conductors. For additional information on the multiphase line model refer to section 0). The faulted phase loop equation is expressed by Equation 4.63 and further clarified by Equation 4.64 as developed in section 4.1.1.5.1. The term, *m*, is the per-unit distance from the point of instrumentation for *Va* and *Ia* to the fault and *Zs* and *Zm* are the total line length self and mutual impedance. Equation 4.65 is generated by adding and subtracting the term *m(Zm) Ia*. Using the identities for the zero- and positive-sequence impedances for balance lines we can express Equation 4.165 in terms of Z0, Z1 as shown in Equation 4.167. Zocholl provides a derivation of Equation 4.167 that is an alternative to the one presented in section 4.1.1.5.1, but the results are the same.[70] From Equation 4.63, Equation 4.65, or Equation 4.68, the per-unit distance to the fault can be computed by applying techniques introduced in section 4.3.3.1. Equation 4.180 shows the results of applying this process to Equation 4.68. These results are subject to the sensitivities mentioned in section 4.3.3.

$$m = \frac{Im\left(Va\,\overline{Ia}\right)}{Im\left(ZL_1\left(Ia - k_0\,Ia_0\right)\overline{Ia}\right)}$$ Equation 4.180

4.3.3.3 Fault locating for phase-to-phase faults for multiphase lines

Following the procedure for solving for the per-unit distance, m, outlined in section 4.3.3.1 results in Equation 4.181, based on the development of Equation 4.88 through Equation 4.92 in section 4.1.1.5.2. As with the single-line-to-ground case, the assumptions are that the line is balanced and the fault impedance is purely resistive. The results are accurate when the four conditons described in section 4.3.3 do not apply. Note that this result, under the conditions specified, is independent of zero-sequence coupling.

$$m = \frac{Im\left[Vbc\ \overline{Ibc}\right]}{Im\left[(Ibc\,Z_L)\,\overline{Ibc}\right]}$$ Equation 4.181

This progression naturally extends to locating phase-to-phase-to-ground vaults such as the one shown in Figure 4.121. Computing the per-unit distance to the fault for each of the six circuits presented above will cover all 11 possible fault scenarios. Since fault resistance, load current, load unbalance, and line unbalance can introduce errors, select the correct phase using a faulted phase identification scheme.

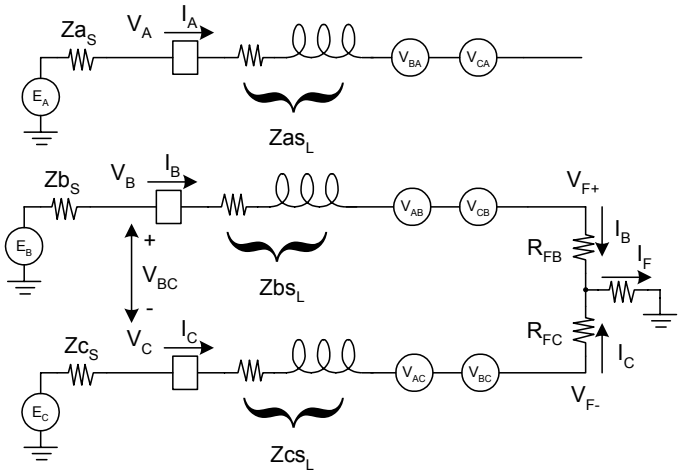


Figure 4.121: Phase-to-Phase-to-Ground Faults

4.3.3.4 Fault locating for multiterminal lines

The current through the fault resistance shown in Figure 4.122 and Figure 4.123 is the superposition sum of the currents supplied from the two sources. There are two approaches for fault locating on multiterminal lines, one using only available locally data and the other requiring information from all terminals. The advantage of the second approach is improved accuracy at the expense of communications equipment cost and the time to transmit the information.

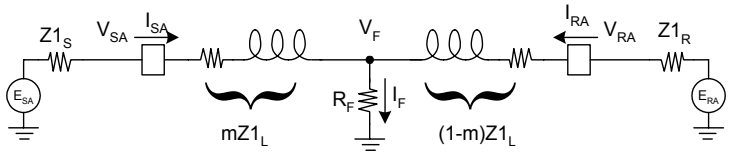


Figure 4.122: Single-Line-to-Ground Fault for Two-Source System

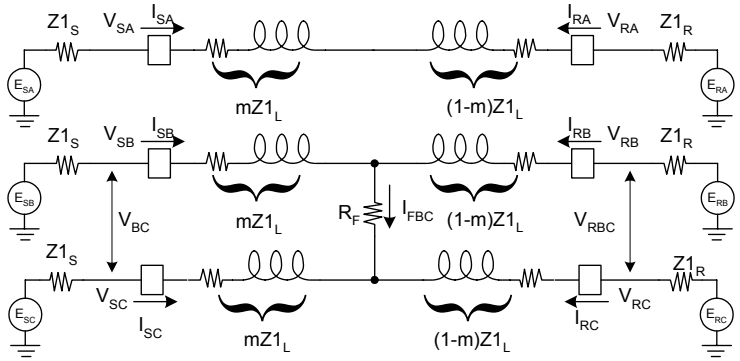


Figure 4.123: Phase-to-Phase-to-Ground Fault for Two-Source System

As with the single source case, loop equations for Va and Vab can be written for the phase-to-ground and phase-to-phase faults as shown in Equation 4.182 and Equation

4.183. In contrast to the single source cases, both R_F and I_F are unknown for the multisource case.

$$Va = m(Ia\,Zl_L) + I_F\,R_F, \text{ (see model in Figure 4.122)} \qquad \text{Equation 4.182}$$

$$Vbc = m(Iab\,Zl_L) + I_F\,R_F, \text{ (see model in Figure 4.123)} \qquad \text{Equation 4.183}$$

4.3.3.4.1 Single-ended fault calculations for multiterminal lines

There are two major types of single-ended fault locators: simple reactance and an algorithm based on work by Takagi.[71] The simple reactance method is well established in the protective relaying industry. With this method, the relay first measures the apparent impedance by using Equation 4.182, modified to include the voltage drop at the fault resistance. The voltage is the product of the fault resistance multiplied times the fault current from Bus S and Bus R, as shown in Equation 4.184. Simply ignoring the real component of Equation 4.180 and solving for the reactive impedance results in Equation 4.185. This assumes either that R_F is zero or that I_F is approximately equal to Ia. Computing the ratio of the reactance or imaginary part of the apparent impedance to the known reactance of the entire protected line produces a value for m, proportional to the distance, as shown in Equation 4.186. To put this proportion in terms a power system operator can use, the instrument often multiplies the resulting ratio by the total line length units.

$$Va_S = m\,ZL_1\left(Ia_S + Ia_0\,K_0\right) + (Ia_S + Ia_R)\,R_F \qquad \text{Equation 4.184}$$

$$X_L apt = Im\left[\frac{Va}{Ia}\right] \qquad \text{Equation 4.185}$$

$$m = \frac{X_L apt}{Im(Zl_L)} \qquad \text{Equation 4.186}$$

To illustrate the concept, consider a single-phase system having line impedance of $16\angle 80°\ \Omega$ and two sources, as shown in Figure 4.124. Assume a relay at bus S measures an apparent impedance $Z = 8\angle 80°\ \Omega$ (or $1.3892 + j7.8785\ \Omega$) for a single-line-to-ground fault, the imaginary part of Z then equals $7.8785\ \Omega$. If the total line reactance equals $15.7569\ \Omega$, the ratio described above equals 0.5. If the total line length equals 100 miles, the fault location indicated by this methodology is 50 miles. The simple reactance method works reasonably well for homogeneous systems when the ground fault does not involve significant fault resistance or load flow.

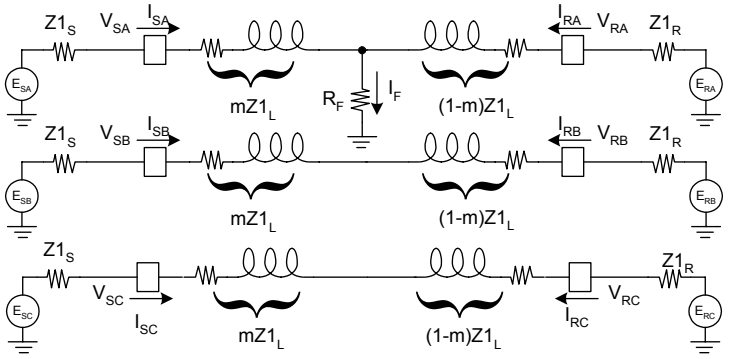


Figure 4.124: Single-Line-to-Ground Fault on Three-Phase Two-Terminal Line.

The following example demonstrates the accuracy of the calculated fault location to fault resistance. Assume that the system shown in Figure 4.124 experiences a phase-A-to-ground fault at *m* per-unit distance from Bus S. As viewed by the instrument (in this case a relay), the measured phase voltage separates into two parts: the voltage drop from the relay location to the fault, and the voltage across the ground fault resistance (R_F), as expressed in Equation 4.182. Applying Equation 4.169 results in an error for calculated *m* if I_F does not equal *Ia*. The amount of error is proportional to the magnitude of the fault resistance and the amount of current supplied to the fault from the remote source.

As shown in section 4.3.3.2, the influences of parallel conductors must be compensated for in multiphase systems. One approach is to use the single-source equations developed in section 4.3.3.1, which results in Equation 4.179. This method will work well if the $R_F \cdot (I_{AS} + I_{AR})$ term does not have an imaginary component as viewed from the Bus S relay.

With the simple reactance method, we simply ignored the $R_F \cdot (I_{AS} + I_{AR})$ term. Rather than ignore this term, we can use an alternate approach that derives a means of nullifying it. We can eliminate the $R_F \cdot (I_{AS} + I_{AR})$ term by multiplying all terms in Equation 4.184 by I_{A2}^*, the complex conjugate of the negative sequence current at bus S, or I_R^*, the complex conjugate of the zero sequence current at bus S, and then save only the imaginary components of all terms. I_{A2}^* or I_R^* is used here because it is a quantity measured at Bus S that has nearly the same phase angle as that of (I_{AS} + I_{AR}). If the angle of I_{A2} equals the angle of (I_{AS} + I_{AR}), the last term of Equation 4.184 is real. Extracting only the imaginary components of Equation 4.184 effectively eliminates the term involving the fault resistance, as shown in Equation 4.187.

$$m = \frac{\mathrm{Im}\left[\mathrm{Vas}\ \overline{\mathrm{Ias}_2}\right]}{\mathrm{Im}\left[\ ZL_1\left(\mathrm{Ias} + k_0\, 3 \cdot \mathrm{Ia}_0\right)\overline{\mathrm{Ias}_2}\right]} \qquad \text{Equation 4.187}$$

Other Takagi-based methods of fault location do not use I_{A2}^* or I_R^* in their fault location methodologies. Instead, these methods use the complex conjugate of a superposition term to multiply all terms in Equation 4.184. This superposition term is the difference of fault and pre-fault phase current (for the faulted phase). The Takagi paper uses the alpha component of the fault current since it is generally more uniform from line-end to line-end and is less affected by system grounding.[72]

Schweitzer further discusses Takagi-based methods. [71] The performance of these methods suffers if fault current contaminates the pre-fault current. For example, if the instrument performing fault location does not have accurate pre-fault data, the fault location result can be significantly affected, depending on the degree of pre-fault corruption.

In nonhomogeneous systems, I_{A2} or I_R may not be collinear (at the same phase angle) with I_F. Eliminating the R_F term by multiplying all terms in Equation 4.184 by I_{A2}^* assumes I_{A2} and I_F are nearly collinear. This simplification may introduce distance to fault reactance calculation errors in the presence of fault resistance and load flow. The amount of error depends on the difference in the system angles on either side of the fault, R_F magnitude, and the direction of load flow. These errors are most pronounced at high values of fault resistance.

To compensate for nonhomogeneous system error, using a compensation factor, ejT, can tilt the top of the line reactance characteristic calculation as shown in Figure 4.125. T is the angle of shift required for a particular fault location. The per-unit fault distance, m, calculation including this term is described in Equation 4.188 using Is_{A2} or Is_R , whichever sequence network is more homogeneous.

$$m = \frac{\mathrm{Im}\left[Va_S \left(\overline{Ias_2 \, e^{jT}} \right) \right]}{\mathrm{Im}\left[Zl_L \left(Ias + k_0 \, Ia_0 \right) \left(\overline{Ias_2 \, e^{jT}} \right) \right]} \qquad \text{Equation 4.188}$$

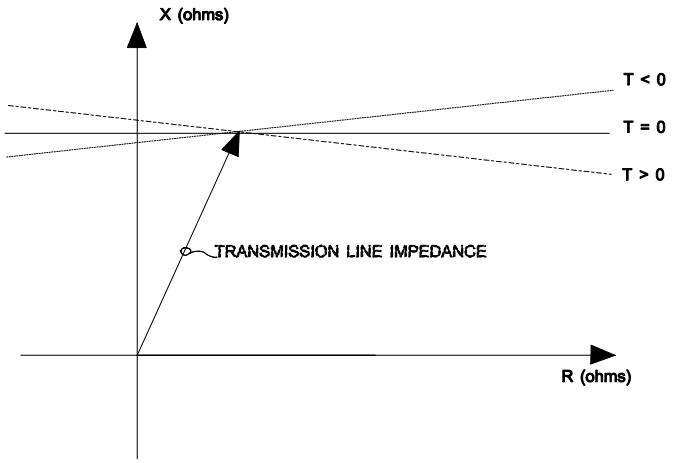


Figure 4.125: Ground Distance Reactance Characteristic Tilt

The value of T makes the distance to ground fault accurate for one point on the protected line. The result is that ground faults located at other points on the protected line do not have the precise T setting required to achieve an accurate fault location. For a given nonhomogeneous system, the ideal characteristic tilt angle, T, varies with fault location. Let us examine the sequence connection diagram of Figure 4.126 for an end-of-line fault. For this system we can represent Is_2 as shown in Equation 4.189. The result of solving Equation 4.189 for I_{TOTAL} is shown in Equation 4.190. The ideal T angle is thus the difference between the angle of I_{TOTAL} and the angle of I_2. Close observation of Equation 4.190 shows that neither relay measures all of the quantities necessary to calculate the ideal T.

Another method of obtaining this *T* angle would be to communicate the magnitude and angle of I_2 between relays. Once each relay received the remote relay I_2 measurement, it would simply sum the measured I_2 with the received I_2 to calculate the angle of I_{TOTAL}. The primary difficulty with this method is that it requires synchronizing the sampling clocks in the two relays: any single quantity angle measurement made by either relay is relative to its own internal sampling clock.

$$\mathrm{Ias_2} = \mathrm{I_{TOTAL}} \frac{\left[(1-\mathrm{m})\mathrm{ZL_2} + \mathrm{ZR_2}\right]}{\left[\mathrm{ZS_2} + \mathrm{ZL_2} + \mathrm{ZR_2}\right]} \qquad \text{Equation 4.189}$$

$$I_{TOTAL} = Ias_2 \frac{\left[ZS_2 + ZL_2 + ZR_2\right]}{\left[(1-m)ZL_2 + ZR_2\right]} \qquad \text{Equation 4.190}$$

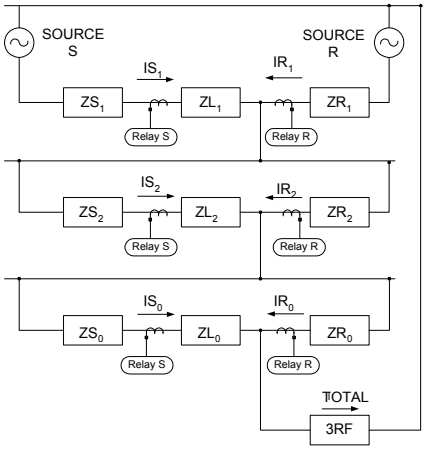


Figure 4.126: Sequence Connection Diagram for SLG Fault at Distance, m = 1.

4.3.3.4.2 Multi-ended fault calculations for multiterminal lines

The obvious difficulty with single-ended methods is that they must attempt to compensate for not knowing the total current flowing through the fault resistance. The most obvious solution is for all terminals of a line to communicate with one another. The relay sums the currents from each line terminal to derive the total fault current. The difficulty with this approach is time aligning data so that the proper magnitudes and phase angles are used in the computations.

One method of aligning data sets is requiring all relays to synchronize their sampling clocks with the same time source, such as Global Positioning Satellite. This time source, generated by a constellation of orbiting satellites, is very accurate but does require the installation of satellite receivers and associated equipment at each relay. For a two-terminal line, another method of aligning data is to collect event reports from all relay terminals on a line and use one terminal as the phase reference. Then calculate the angles necessary to align the data set of all the remote terminals with the reference terminal. Knowing that the measured positive-sequence pre-fault voltages and currents from the event reports and the positive-sequence line impedance must solve Equation 4.191. Solving for the remote positive-sequence voltage using

Equation 4.192, compute the adjustment angle from the positive-sequence voltage measured at the remote terminal, taken from Equation 4.193.

$$Vas_1 = Var_1 + Ias_1 \; ZL_1 \qquad \text{Equation 4.191}$$

$$\begin{aligned} \mathrm{Re}(Var_1) &= \mathrm{Re}\left(Vas_1\right) + \mathrm{Re}\left(Ias_1 \; ZL_1\right) \\ \mathrm{Im}(Var_1) &= \mathrm{Im}(Vas_1) + \mathrm{Im}(Ias_1 \; ZL_1) \end{aligned} \qquad \text{Equation 4.192}$$

$$\phi_{ADJUST} = \angle Vr_{MEASYURED} - \tan^{-1}\left(\frac{\mathrm{Im}(Var_1)}{\mathrm{Re}(Var_1)}\right) \qquad \text{Equation 4.193}$$

Once the data sets are aligned, there are numerous methods of calculating the distance to the fault.[73] One popular two-ended method is based on the theory that given a single fault on a power line, the voltage at the fault, as viewed by either end of the line, is equal. Thus, the two-ended algorithm recognizes that the voltage along the line from either end can be represented as a function of the distance to the fault. As Equation 4.194 through Equation 4.196 show, we can equate the fault voltage from both line ends, and solve the distance to the fault as follows for the system shown in Figure 4.124.

For relay at bus S $\quad V_F = Vs - m\,ZL\,Is$ $\quad$ Equation 4.194

For relay at bus R $\quad V_F = Vr - (1-m)\,ZL\,Ir$ $\quad$ Equation 4.195

Per-unit distance from bus S $\quad m = \dfrac{(Vs - Vr - Z\,Ir)}{Z(Is + Ir)}$ $\quad$ Equation 4.196

Using negative-sequence voltage and current terms in Equation 4.196 offers many advantages. For instance, we don't need to know the zero-sequence impedance of the line, a parameter that depends on varying factors and is difficult to determine. Using the terms in Equation 4.196 also avoids errors generated by zero-sequence current infeeds from tapped loads along the transmission line, as well as errors caused by zero-sequence mutual coupling with adjacent power lines.

4.3.3.4.2.1 Considerations for fault locating using zero-sequence parameters

Fault locating on systems with parallel lines must account for zero-sequence currents coupled to and from other lines, as shown in Figure 4.126. This is usually done by using mutual compensation for the residual current (I_{RM}) from the offending parallel line. This residual current must be routed to each relay that locates faults.

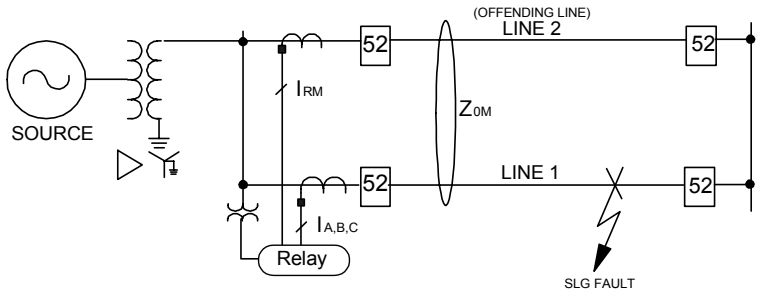


Figure 4.127: Mutually-Coupled Parallel Lines With a Single Source

Modify Equation 4.68 to include the coupled current. Equation 4.197 represents the voltage measured at the relay location. Compute the apparent impedance seen at bus S using Equation 4.198, which assumes that the fault resistance is zero.

$$Vsa = mZl_1\left(Isa + k_0\, Ia_0 + km_0\, Im_0\right) + I_F\, R_F \qquad \text{Equation 4.197}$$

$$Zapp = \frac{Vsa}{\left(Isa + k_0\, Ia_0 + km_0\, Im_0\right)} \qquad \text{Equation 4.198}$$

The (k_{0M}•I_{RM}) term in the denominator of Equation 4.198 is the error term if no corrections are made. For the system shown in Figure 4.126, the ground fault location reads long if the residual current in the offending line is in the same direction as the residual current in the faulted line (out-out). Moving the fault closer to the remote terminal makes the fault appear farther away than it actually is because of the k_{0M}•I_{RM} term.

To illustrate this point, Figure 4.127 shows a phase-A single-line-to-ground fault simulated at various places along Line 1. Table 4.12 lists the various calculated single-ended fault location results, I_R, and I_{RM} values.

Table 4.12: Relay Fault Locations Calculated for SLG Faults on the System of Figure 4.127

Fault Location	Calculated Fault Location	Ia_0	Im_0
m = 0.10	0.10	24.1∠-82.9°	1.27∠-82.9°
m = 0.20	0.21	15.7∠-82.9°	1.74∠-82.9°
m = 0.30	0.32	11.5∠-82.9°	2.03∠-82.9°
m = 0.50	0.55	7.30∠-82.9°	2.43∠-82.9°
m = 0.70	0.81	5.16∠-82.9°	2.78∠-82.9°
m = 0.90	1.12	3.83∠-82.9°	3.13∠-82.9°
m = 0.99	1.28	3.37∠-82.9°	3.30∠-82.9°

The line and system values used to calculate the values shown in Table 4.12 are:

$Z1S$ = Positive-sequence source impedance: (0.1 +j0.8) Ω secondary

$Z0S$ = Zero-sequence source impedance: (0.3 +j2.4) Ω secondary

Z_{1L1} = Line 1, positive-sequence line impedance: (1.0 +j8.0) Ω secondary

Z_{0L1} = Line 1, zero-sequence line impedance: (3.0 +j24.0) Ω secondary

$Z_{1L2} = Z_{1L1}$

$Z_{0L2} = Z_{0L1}$

$Z_{0M} = 0.5 \cdot Z_{0L1}$

As the data in Table 4.12 show, zero-sequence mutual coupling can have an appreciable affect on the ground fault location. Again, as the per-unit fault distance, m, increases the fault location error becomes more pronounced.

4.3.3.4.2.2 Errors caused by zero-sequence mutual coupling

In parallel line applications employing ground distance elements or requiring fault location, zero-sequence mutual coupling can cause under- and overreaching problems on both the faulted, and nonfaulted line relaying terminals. This can happen regardless of whether the parallel line in-service or out-of-service, provided it is grounded at both line ends. When the parallel line is grounded, the relay loses all current information from this offending line because the line grounding point is in front of the current transformers.

Errors are also introduced in applications where parallel lines are served from a single zero-sequence source as shown in Figure 4.127. Such is the case for a line that is connected to the grounded wye side of a transformer and a delta load or to the delta side of a transformer at the other. Such a condition can also occur when the load is being served at the remote bus yet the lines to the right of this remote bus are open for maintenance or out-of-service because of faults. In these cases, the percentage of under-/overreach is more pronounced than that of parallel lines where zero-sequence sources are present at both ends of the line, assuming equal sources on either end of the line.

For fault location using mutual compensation techniques, the residual current (I_{RM}) from the offending parallel line must be routed to the relay with the fault location feature. Determine relay settings carefully to avoid having some of the zero-sequence compensated fault location methods lead to incorrect operation of ground distance relays connected to the parallel nonfaulted line.

4.3.3.4.2.3 Discussion of compensating methods for zero-sequence mutual coupling

There are various methods, with varying degrees of success, for compensating for influences to zero-sequence current. One method measures Im_0 and uses the term, $Im_0 \cdot [Z_{0M}/(Z_{L1})]$, in the denominator of ground fault location calculations, however under- and overcompensation frequently occurs.

For example, assume a close-in fault on the offending line and a single zero-sequence source located behind the relaying terminal. In this case, Im_0 can be much larger than the residual current measured on the healthy line at the opposite end of the "lollipop loop," a system described by Figure 4.127, where Im_0 equals Ia_0 at both relaying terminals. Since the Im_0 term is used in the denominator, the resulting fault location is much reduced and positive at the terminal where $|Im_0|$ is greater than $|Ia_0|$ if Ia_0 and Im_0 flow in the same direction. If Im_0 and I_R are 180° out-of-phase, the fault location is correctly negative, but not correct in magnitude.

4.3.3.4.2.4 Switching the compensation factor, k_0

The switch decision depends on the magnitude of Im_0. If $|Im_0|/|Ia_0|$ is less than or equal to one within a degree of safety margin, the ground fault locator uses one km_0 factor. If $|Im_0|/|Ia_0| > 1$, the fault locator uses an alternate k_0 factor. The relay uses the Im_0 current as a simple switching indicator for the k_0 factor, but does not use it in the ground fault location calculations.

This method does not consider the direction of Im_0, which can cause undesirable overcompensation when the parallel faulted line trips sequentially. If the compensation method includes the direction of Im_0 flow in the offending parallel transmission line, then use the following characteristics of Im_0 in determining the amount of compensation required, if any.

Compensation is increased if Im0 is in the same direction and has less magnitude than IR measured in the relay. This feature reduces the underreaching fault location results.

Compensation is decreased if Im_0 is in the opposite direction and has less magnitude than I_R measured in the relay. This feature reduces the overreaching fault location results.

Compensation is decreased if the parallel line is tripped or if the parallel line is out-of-service and grounded at either end. If the line is floating, no Im_0 determination is possible and a new k_0 must be used.

4.3.3.4.2.5 Closed form negative-sequence nonpolarized techniques

Another method of locating ground faults uses negative-sequence quantities from all line ends. Using negative-sequence quantities overcomes the difficulties associated with zero-sequence mutual coupling. Further, this method of fault location for two-terminal lines does not require alignment of the data sets. This is because the algorithms at each line end use quantities from the remote terminal that do not require alignment, namely $|I_2|$ and the pre-calculated negative-sequence source impedance. Since both relays receive all of the necessary information, they calculate accurate fault location without iterations.

The concept is best illustrated by starting with a single-line-to-ground fault as illustrated in Figure 4.124 and the comparable sequence connection diagram shown in Figure 4.126. As discussed previously in section 4.3.3.4.2, we know that in double-ended fault location the zero- and negative-sequence fault voltages as viewed from all ends of the protected line are equal. This shows in Equation 4.194 and Equation 4.195 and can also be written as shown in Equation 4.199 and Equation

4.200. Using these two equations to solve for the negative-sequence current at the remote end results in Equation 4.201. This equation remains equal if we only consider the magnitudes of both sides of the equation. Multiplying both sides of Equation 4.201 by the respective complex conjugate results in Equation 4.202. Since phase is now eliminated, there is no need for data alignment.

For relay at bus S: Equation 4.199

$$V_F = Vs_2 - m\,ZL_2\,Is_2 = Is_2\left(Zs_2 + m\,ZL_2\right)$$

For relay at bus R: Equation 4.200

$$V_F = Vr_2 - (1-m)ZL_2\,Ir_2 = Ir_2\left(Zr_2 + (1-m)ZL_2\right)$$

$$Ir_2 = Is_2\left[\frac{Zs_2 + m\,ZL_2}{Zr_2 + (1-m)ZL_2}\right] \quad \text{Equation 4.201}$$

$$|Ir_2|^2 = \left|\left[\frac{Is_2\left(Zs_2 + m\,ZL_2\right)}{Zr_2 + (1-m)ZL_2}\right]\right|^2 \quad \text{Equation 4.202}$$

The computations required by Equation 4.202 result in a quadratic equation involving m, the per-unit distance to the fault, having the form $A{\cdot}m^2 + B{\cdot}m + C = 0$. As Equation 4.202 shows, there two possible solutions for m. Because of the ± operator, we have two possible fault locations: one realistic, the other not probable. From the above derivation, we show that each relay at each line terminal of the protected two-terminal line must transmit a minimal amount of information. Combining this information with negative-sequence quantities measured by each relay, we can solve for the fault location at each terminal without iterations. The minimal information sent by each relay for a two-terminal application is $|I_2|$ as well as the magnitude and angle of $Z_{2SOURCE}$

$$m = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A} \quad \text{Equation 4.203}$$

The methodology just described is attractive because, a reduced-time for computation of closed form solution for fault location. However it is not the only method that uses computed negative-sequence source information. The method described next has many of the same advantages with the obvious drawback that the time necessary to communicate the information between line terminals significantly increases the time for the scheme to compute a fault location.

4.3.3.4.2.6 Iterative negative-sequence nonpolarized techniques

This method of fault locating is an iterative approach that uses an initial estimate of m from one of the previous methods of fault locating and only the $|V_{2F}|$ need be repeatedly exchanged between line terminals. Each terminal solves Equation 4.194 and compares this result of $|V_{2F}|$ computed locally with the value for $|V_{2F}|$ communicated from the remote end. If the values are equal, then the value used for m is the final result. If only one of the terminals computes the fault location, then the newly calculated value for $|V_{2F}|$ must be communicated with the other end after each

computation. Each terminal computes a value for m as seen from its location. If ms is the value of m computed for terminal S then conversely mr is the value of m computed at terminal R. After convergence, the relationship ms = 1-mr is true.

One convergence algorithm uses successive approximation similar to the process used by R2R-SAR analog to digital converters. The procedure starts with each end assuming that the fault is at the middle of the line (m = 0.5). Each end computes the fault voltage using the current value for m and previous computed values for Zs and ZL2. The absolute value of this fault voltage is communicated to the other terminal. The relay compares the difference between $|V_{2F}|$ computed locally and the value computed remotely to ε, a convergence limit. If the difference is greater than ±ε, then m is adjusted by successively higher powers of 0.5, as demonstrated in Figure 4.128. Each successive iteration adds a power of 0.5 more precision until it achieves the desired accuracy.

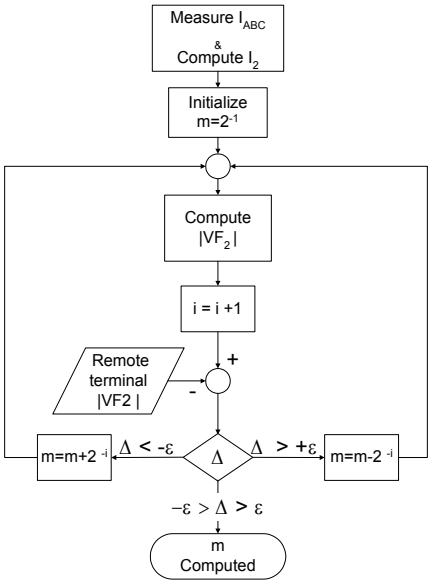


Figure 4.128: Flow Diagram for Fault Location Convergence

4.3.3.4.2.7 Fault Location Logic Extension for Three-Terminal Line Applications

Many times utilities connect another line with a source to an existing two-terminal line. This creates a three-terminal line, a line with three sources that can contribute to the energy of a fault. Utilities do this for many reasons, the most compelling are voltage support and increased operations flexibility. Such lines are much more complex to protect with conventional distance and directional protection schemes. These same lines are also more difficult to fault locate.

With single-ended fault locating devices at each line end, the most accurate fault location is provided by the relay whose line section is not in parallel with another line section during the fault. For example, for a single-line-to-ground fault on Line 1 in Figure 4.129, the fault location from Relay 1 is more accurate than those from Relay

2 or 5. Also note that the current from Lines 2 and 5 converge at Tap 1 before flowing to any fault on Line 1.

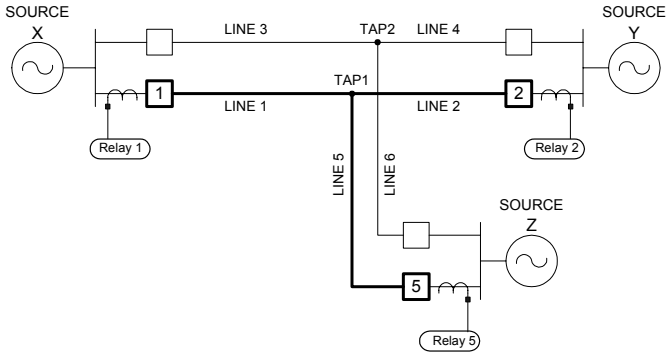


Figure 4.129: System Single-Line Diagram of Typical Parallel Three-Terminal Application

Use the following points, illustrated in the sequence connection diagram of Figure 4.130, to convert any three-terminal line to a two-terminal line in the negative-sequence network. We reduced the parallel portion of the three-terminal line to a single line to simplify the diagram and explanation without losing accuracy.

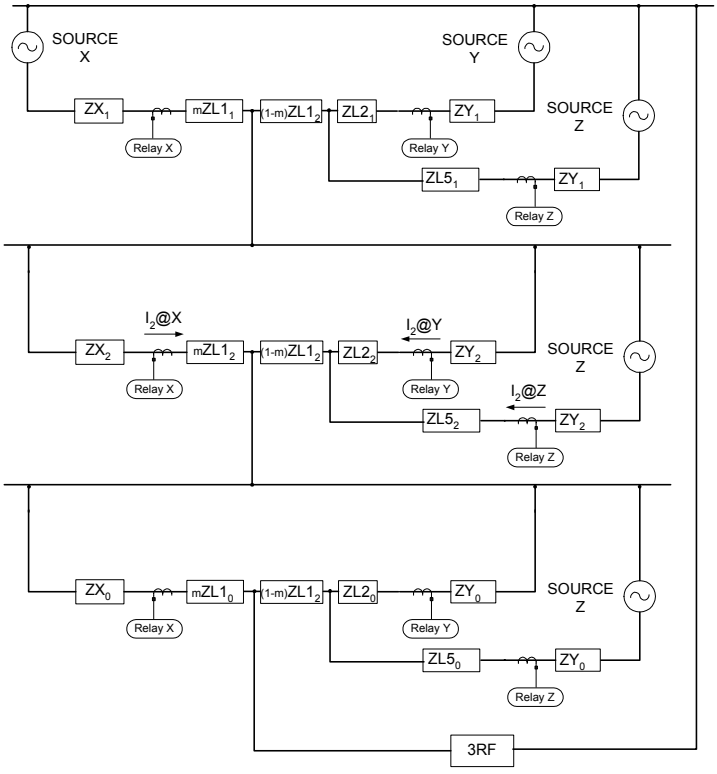


Figure 4.130: Sequence Connection Diagram for Example Three-Terminal Line

The sequence connection diagram in Figure 4.130 assumes a single-line-to-ground fault located m per-unit distance from Bus X. With this fault placement, there are two voltages that Relays 2 and 5 calculate the same: V_{F_2} and V_{TAP_2}. Relay 2 and 5 can accurately calculate V_{2TAP} without exact knowledge of the fault location on Line 1. They only need to know the positive-sequence line impedances and assume that the negative- and positive-sequence line impedances are equal. Each relay calculates V_{2TAP} as shown in Equation 4.204 through Equation 4.206.

@ Relay 1 $$Vx_{TAP2} = Vx_2 - ZL_2\, Ix_2$$ Equation 4.204

@ Relay 2 $$Vy_{TAP2} = Vy_2 - ZL_2\, Iy_2$$ Equation 4.205

@ Relay 5 $$Vz_{TAP2} = Vz_2 - ZL_2\, Iz_2$$ Equation 4.206

For faults on Line 1, $|Vy_{TAP_2}| = |Vz_{TAP_2}|$. Each relay calculates V_{TAP_2} and transmits it to the remote terminals. Once each relay receives the tap voltage, the V_{2TAP} that does not have a match indicates the faulted line section. In the example shown in Figure 4.129, $|Vy_{TAP_2}|$ and $|Vz_{TAP_2}|$ have the closest match. Once the faulted line section is identified, the parallel combination of $(ZL2_2 + ZY_2)$ and $(ZL5_2 + ZZ_2)$ must be converted to a single impedance. This conversion is simply $V_{TAP\,2}/(Iy_2 + Iz_2)$. We cannot simply add together currents I_2@Y and I_2@Z from Relays 2 and 5 because the sampling clocks at these terminals are not necessarily aligned. The phase of (Vy_{TAP_2}/Vz_{TAP_2}) equals the alignment angle between Relays 2 and 5. Once we know this angle, we can add the currents from Relays 2 and 5 to calculate an apparent negative-sequence source at the tap, as shown in Figure 4.131.

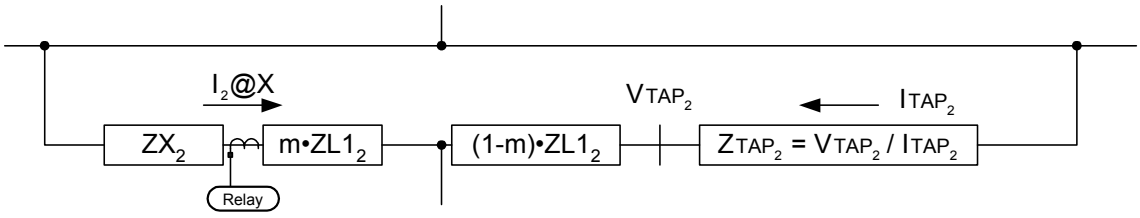


Figure 4.131: Equivalent Negative-Sequence Network Diagram

The negative-sequence magnitude and phase of both the current and the tap voltage are the minimal information that each relay must send to each of the other relays in the three-terminal application. From these transmitted quantities, each relay performs the following steps before calculating the fault location.

Compare the magnitudes of VTAP2. Those relays with approximately the same |VTAP2| are not associated with the faulted line section. Call these relays Remote 1 and 2.

From Remote 1 and 2 $\angle V_{2TAP}$ values, calculate the alignment angle between these relays. Use the relay with the $|I_{2RELAY}|$ as the reference relay.

Adjust the angle of the nonreference remote relay negative-sequence current by the alignment angle calculated in B, above.

Add the negative-sequence current of the reference remote relay with the angle adjusted negative-sequence current of the nonreference remote relay. Call this summation current I_{2TAP}.

Calculate Z_{TAP} as V_{TAP_2} / I_{TAP_2}.

With the network reduction described earlier, the algorithms previously developed for the two terminal lines are again applicable. Thus, for three-terminal lines we make the following substitutions:

$$\text{Three-terminal:} \qquad Z_{TAP_2} + ZL_2 = e + jf$$

$$IR_2 = I_{TAP_2}$$

Each relay has the necessary information to accurately locate the fault. Please note that because all relays have V_{2TAP} from the other relays, each relay then knows whether it can calculate m accurately. Note that an operator can then interrogate any relay for the protected line to determine the fault location. If we did not have such a feature, this same power system operator would have to interrogate each relay to determine the fault location. This interrogation adds undesirable time delay in system restoration.

4.4 SUPERIMPOSED QUANTITIES [74]

4.4.1 Theory of Superimposed Quantities Using Principles of Superposition

4.4.1.1 Fault Analysis Using the Superposition Principle

Consider the single-line diagram of Figure 4.132, where a fault is applied through a resistance Rf at a distance m per-unit line length from the relay at the left bus. The voltage Eb of the right-hand source is expressed by:

$$E_R = h \cdot e^{-j\theta} \cdot E_s \qquad \text{Equation 4.207}$$

where Θ is the angular difference between the left and right sources and h is a scalar. For negative values of Θ, load flows from left to right.

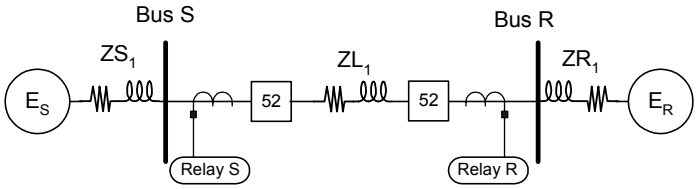


Figure 4.132: Example System Single-Line Diagram

We can use the superposition principle to determine the voltages and currents of the faulted circuit in the presence of the load flow. Figure 4.133(b) illustrates the pre-fault network. We define the pure-fault network (Figure 4.133 (c)) as:

pre-fault network voltage sources must be short-circuited

voltage source, Ef, must be applied at the fault point.

The magnitude of Ef is equal to the voltage level existing at the fault location before application of the fault. The source phase angle is opposite to the pre-fault voltage phase angle at the fault point.

Determine either a faulted circuit voltage (V) or a current (I) by summing two components, pre-fault plus pure-fault, as provided by the superposition principle shown in Equation 4.208 and Equation 4.209. In all equations, capital letters represent phasors; small letters are scalars.

$$V = V_{PRE-FLT} + \Delta V \qquad \text{Equation 4.208}$$

$$I = I_{PRE-FLT} + \Delta I \qquad \text{Equation 4.209}$$

The pure-fault network currents and voltages are zero before the fault. Therefore, any value they have from a fault condition represents a change or delta quantity. For this reason, they are called incremental or superimposed quantities and are represented with a prefix Δ to indicate the change with respect to the pre-fault circuit values.

4.4.1.2 Superimposed Quantities for Conventional Shunt Faults

Figure 4.133 a, b, and c shows circuits that represent a three-phase fault and cannot be used to analyze other conventional shunt faults. To investigate different faults, you must use the appropriate sequence network to represent the pure-fault network. Because the sequence network is used to represent the pure-fault network, all sequence quantities are represented as delta quantities.

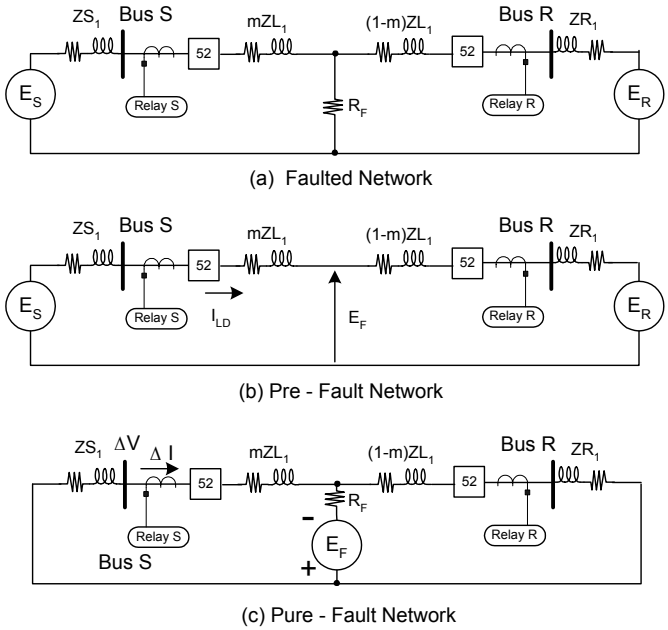


Figure 4.133: Superposition Networks

4.4.1.2.1 Analysis of a Phase-A-to-Ground Fault

Figure 4.132 (c) represents the pure-fault network of a phase-A-to-ground fault. Following the circuit of Figure 4.132, the phase-A pre-fault or load current is expressed as:

$$I_{LD} = \frac{E_a \bullet (1 - h \bullet e^{-j\theta})}{ZS1 + ZL1 + ZR1} \qquad \text{Equation 4.210}$$

The voltage E_F at the fault point before the fault is expressed by Equation 4.211 and the incremental phase-A current at the relay by Equation 4.212.

$$Ef = E_a - (ZS1 + m \bullet ZL1) \bullet I_{LD} \qquad \text{Equation 4.211}$$

$$\Delta I_{AR} = C1 \cdot \Delta I_{1F} + C2 \cdot \Delta I_{2F} + C0 \cdot \Delta I_{0F} \qquad \text{Equation 4.212}$$

Therefore, according to the superposition principle the total phase A current is:

$$I_{AR} = C1 \cdot \Delta I_{1F} + C2 \cdot \Delta I_{2F} + C0 \cdot \Delta I_{0F} + I_{LD} \qquad \text{Equation 4.213}$$

In these expressions, C1, C2, and C0 are the current distribution factors. [75]
Perform the same analysis to calculate the voltage at the relay. The phase-A pre-fault voltage is:

$$V_{AR(pre\_flt)} = m \bullet ZL1 \bullet I_{LD} + Ef \qquad \text{Equation 4.214}$$

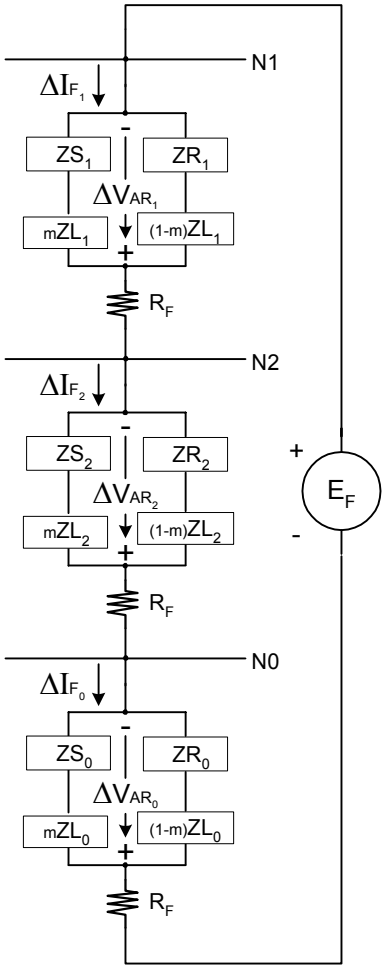


Figure 4.134: Pure-Fault Sequence Network for a Single-Line-to-Ground Fault

The incremental phase-A voltage at the relay is:

$$\Delta V_{AR} = -C1 \bullet \Delta I_{1F} \bullet ZS1 - C2 \bullet \Delta I_{2F} \bullet ZS1 - C0 \bullet \Delta I_{0F} \bullet ZS0 \qquad \text{Equation 4.215}$$

Using the superposition principle, the fault voltage at the relay is:

$$V_{AR} = -2C_1 \bullet \Delta I_{1F} \bullet ZS1 - C_0 \bullet \Delta I_{0F} \bullet ZS0 + Ef + m \bullet ZL1 \bullet I_{LD} \qquad \text{Equation 4.216}$$

We can easily extend the principles used in this analysis to other types of shunt faults, such as double-phase and double-phase-to-ground faults, by replacing the fault sequence network with the appropriate sequence network for the fault type of interest.

4.4.1.2.2 Incremental Impedance

Incremental impedance is the ratio of an incremental voltage phasor divided by an incremental current phasor. The incremental impedance can be single-phase A, B, or

C, or it can be a differential with the voltage (and current) being taken between two phases (AB, BC, or CA). Finally, it can be computed with incremental sequence quantities. As an example, the phase-A incremental impedance, as measured at the relay, for a phase-A-to-ground fault is given as:

$$\frac{\Delta \mathrm{Var}}{\Delta \mathrm{Iar}} = \Delta \mathrm{Zar} = \frac{-\left(\mathrm{C1}\cdot \mathrm{ZS}_1 \cdot \Delta \mathrm{I}_{1\mathrm{F}} + \mathrm{C2}\cdot \mathrm{ZS}_2 \cdot \Delta \mathrm{I}_{2\mathrm{F}} + \mathrm{C0}\cdot \mathrm{ZS}_0 \cdot \Delta \mathrm{I}_{0\mathrm{F}}\right)}{\mathrm{C1}\cdot \Delta \mathrm{I}_{1\mathrm{F}} + \mathrm{C2}\cdot \Delta \mathrm{I}_{2\mathrm{F}} + \mathrm{C0}\cdot \Delta \mathrm{I}_{0\mathrm{F}}} \qquad \text{Equation 4.217}$$

or

$$\frac{\Delta Var}{\Delta Iar} = \Delta Zar = \frac{-\left(2\cdot C1\cdot ZS_1 \cdot + C0\cdot ZS_0\right)}{C1 + C2 + C0} \qquad \text{Equation 4.218}$$

The positive-sequence impedance at the relay for a phase A-to-ground fault is provided by:

$$\Delta Zar_1 = \frac{\Delta Var_1}{\Delta Iar_1} = \frac{-\left(C1\cdot ZS_1 \cdot \Delta I_{1F}\right)}{C1\cdot \Delta I_{1F}} = -ZS_1 \qquad \text{Equation 4.219}$$

The incremental impedance across phases A and B is provided by:

$$\Delta Zabr = \frac{\Delta(Va - Vb)r}{\Delta(Ia - Ib)r} = \frac{-\left(2\cdot C1\cdot ZS_1 \cdot \Delta I_{1F}\right)\cdot\left(1 - a^2\right)}{2\cdot C1\cdot \Delta I_{1F}\cdot\left(1 - a^2\right)} = -ZS_1 \qquad \text{Equation 4.220}$$

In Equation 3.11, "*a*" is the operator equal to $1\angle 120°$. Note that the incremental impedance across two phases (one of them being phase-A) or using the positive-sequence quantities is equal to the negative of the source impedance behind the relay.

4.4.1.2.3 Incremental Impedances for Other Types of Shunt Faults

In the previous section, we showed that for a single-phase-to-ground fault, properly selected incremental impedances equaled the negative of the source impedance behind the relay. The same principle applies for the other types of shunt faults. Table 4.13 lists the incremental impedances equal to the negative of the source impedance for the four basic fault types.

Table 4.13: Incremental Impedances Equal to $-ZS_1$

Fault Type	Incremental Impedances
A-G	ΔZab, ΔZca, ΔZ_1
B-C	ΔZb, ΔZc, ΔZab, ΔZbc, ΔZca, ΔZ_1
BC-G	ΔZab, ΔZbc, ΔZca,ΔZ_1
ABC	ΔZa, ΔZb, ΔZc, ΔZab, ΔZbc, ΔZca, ΔZ_1

Note that the incremental impedances computed across two phases and the positive-sequence impedance are always equal to $-ZS_1$ for all fault types.

4.4.1.3 Relation Between Superimposed Quantities and Sequence Quantities

The pure-fault sequence network of Figure 4.132 represents all sequence voltages and currents as superimposed quantities. Normally, however, compute sequence quantities based on the measured fault voltages and currents. For instance, the pure-fault positive-sequence current at the fault is provided as:

$$\Delta I_{1F} = \Delta Ia + a \cdot \Delta Ib + a^2 \cdot \Delta Ic \qquad \text{Equation 4.221}$$

Normally we would compute the positive-sequence current as:

$$I_{1F} = Ia + a \cdot Ib + a^2 \cdot Ic \qquad \text{Equation 4.222}$$

Given that any phase current is equal to the pure-fault phase current plus the load:

$$I_{1F} = \Delta Ia_F + I_{LD} \qquad \text{Equation 4.223}$$

We end up with the relation that the computed positive-sequence current and the pure-fault positive-sequence current are different by a quantity equal to the load:

$$I_{1F} = \Delta I_{1F} + I_{LD} \qquad \text{Equation 4.224}$$

When we apply the same reasoning to both the negative- and zero-sequence currents, the load current vanishes if we assume it to be a balanced quantity. For these two-sequence fault types, the calculated sequence quantities are equal to the pure-fault quantities:

$$I_{2F} = \Delta I_{2F} \quad \text{and} \quad I_{0F} = \Delta I_{0F} \qquad \text{Equation 4.225}$$

In conclusion, the calculated sequence quantities, with the exception of positive-sequence quantities, are superimposed quantities.

4.4.1.4 Relation Between Superimposed Voltage and Superimposed Current

As we discussed above, selecting the proper quantities at the relay location for each forward fault-type yields an incremental impedance equal to the negative of the positive-sequence source impedance ZS_1:

$$\Delta Zr = \frac{(\text{post} - \text{fault Vr}) - (\text{pre} - \text{fault Vr})}{(\text{post} - \text{fault Ir}) - (\text{pre} - \text{fault Ir})} \quad \frac{\Delta Vr}{\Delta Ir} = -ZS_1 \qquad \text{Equation 4.226}$$

Alternatively, the same condition can be expressed as:

$$\frac{\Delta Vr}{\Delta Ir \cdot (-ZS_1)} = 1 \qquad \text{Equation 4.227}$$

Equation 4.227 indicates that during a fault the magnitude and phase of the incremental voltage waveform (or phasor) are equal to the magnitude and phase of the incremental current waveform (or phasor) multiplied by the negative of the

source impedance behind the relay. This principle has been exploited to define a directional element. If the scalar product between the incremental voltage phasor and the incremental current phasor, multiplied by the negative of the source impedance, is positive – a forward fault direction is declared:

$$\text{real}\left[\Delta Vr \cdot \left(\overline{\Delta Ir \cdot \left(-ZS_1\right)}\right)\right] = \Delta Vr \cdot \Delta Ir \cdot ZS_1 \cdot \cos(\theta) \qquad \text{Equation 4.228}$$

In this expression, θ represents any phase angle mismatch that could exist in the source phase angle representation. Normally θ is equal to zero. Because magnitude of the source impedance is always positive, we can set it to unity without affecting the basic principle:

$$\text{real}\left[\Delta Vr \cdot \left(\overline{\Delta Ir \cdot \left(\angle - ZS_1\right)}\right)\right] = \Delta Vr \cdot \Delta Ir \cdot \cos(\theta) \qquad \text{Equation 4.229}$$

If the result of Equation 4.229 is negative, the direction is reverse. Thus, for reverse faults the impedance presented to the relay is the sum of the line impedance plus the remote source impedance.

4.4.1.4.1 Impact of Parallel Lines on the Value of the Source Impedance

In more complex networks, like the double circuit shown in Figure 4.135, even the positive-sequence incremental impedance fails to exactly measure the source impedance behind the relay for three-phase faults. In this case, ΔZ1 is provided by:

$$\Delta Z_1 = \frac{-ZS_1}{1 + \dfrac{ZS_1}{ZL_1} - \dfrac{ZR_1}{ZL_1}\left(\dfrac{ZS_1 + \dfrac{m}{2}ZL_1}{ZR_1 + \dfrac{1-m}{2}ZL_1}\right)} \qquad \text{Equation 4.230}$$

For m equal to zero, Equation 4.230 reduces to Equation 4.231 and for m equal to one, to Equation 4.232, assuming that ZL_1 is identical for both line 1 and line 2.

$$\Delta Z_1 = \frac{-ZS_1}{ZS_1 + 2 \cdot ZR_1 + ZL_1} \qquad \text{Equation 4.231}$$

$$\Delta Z_1 = -2 \cdot ZS_1 \qquad \text{Equation 4.232}$$

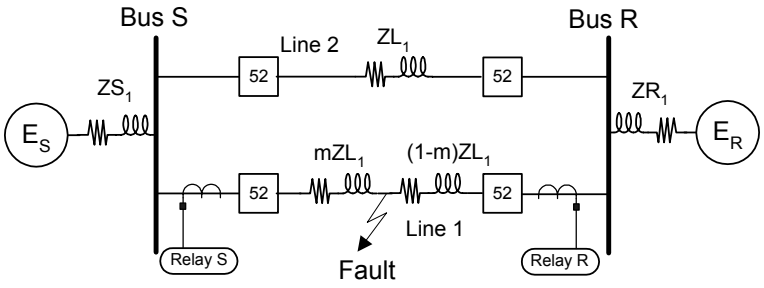
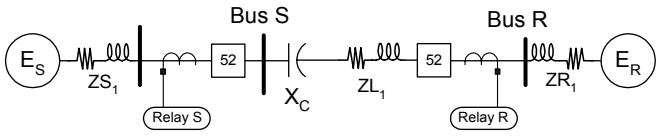


Figure 4.135: Single-Line Diagram of a Double Circuit Network

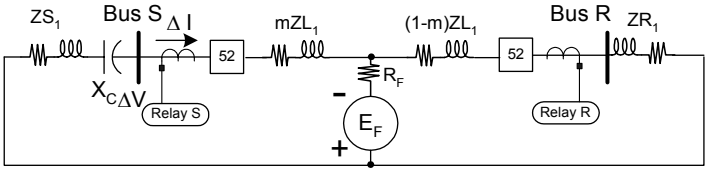
Equation 4.231 and Equation 4.232 indicate that the positive-sequence incremental impedance varies, depending on the location of the fault. The difference in amplitude varies from a small fraction to twice its nominal value. If the value of the local source impedance varies, it is important that the new value remains highly inductive to maintain directionality. Directionality, as provided by Equation 4.218, is still maintained if the mismatch θ remains acceptable. Note that source impedance magnitude variations are not important because source impedance can be set to unity. However, the source impedance magnitude must not be such that the measured current decreases below the sensitivity threshold of the measuring relay.

4.4.1.4.2 Conventional Networks and the Exception of Series-Compensated Networks

For conventional networks, the source impedance behind a relay is inductive, and applying Equation 4.218 for directionality is applicable without restriction. For series-compensated lines, as shown in Figure 4.136, an adverse situation might develop if the directional relay voltage is supplied from the line side of the capacitors. If the capacitor impedance becomes greater than the original source impedance (ZS_1), then the source impedance behind the relay is capacitive and the directional relay makes an incorrect directional declaration.



(a) Single-Line Diagram



(b) Pure - Fault Network

Figure 4.136: Single-Line Diagram and Pure-Fault Network Representing a Series-Compensated Line

4.4.1.5 Mimic Emulation of Source Impedance Behind the Relay

4.4.1.5.1 Definition of a Mimic Filter

In Equation 4.232, the negative of the unit source impedance behind the relay must multiply the incremental current phasor to get a compensated current. This can be accomplished in the time domain by processing the current waveform through a high-pass filter, or mimic, of the form:

$$K(1+\tau_1 s) \qquad \text{Equation 4.233}$$

In so doing, we fulfill two objectives: multiply the current phasor by the unit source impedance behind the relay and remove any dc offset present in the waveform. One

transformation that provides a digital form (using the z transform) of the analog high-pass filter expressed by Equation 4.223 is provided by:[83]

$$K\left[(1+\tau_1)-\tau_1 z^{-1}\right] \qquad \text{Equation 4.234}$$

where τ_1 is the filter time constant and K is chosen such that at 60 Hz, the gain is 1.

Figure 4.137 illustrates the removal of a dc offset added to a sine wave after it has been processed through a mimic filter in the time domain. Reference [12] shows that proper removal of any dc-offset effect occurs over a large interval of the network X/R ratio. Figure 4.138 shows the frequency response of the mimic filter. Note that the mimic filter is a high-pass filter. While the mimic filter does remove dc from the original waveform, the higher frequency components (if they exist) are amplified.

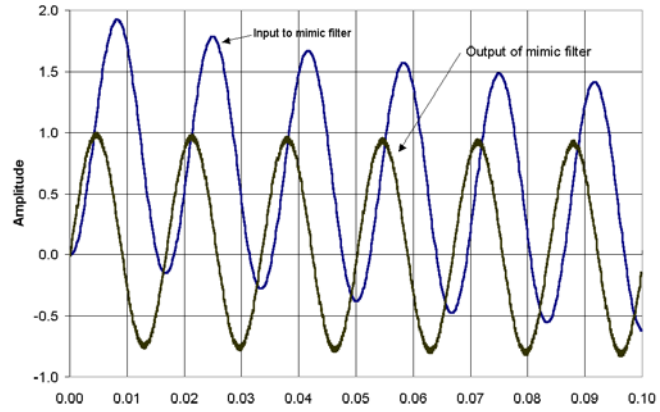


Figure 4.137: Mimic Filter Removes DC Offset

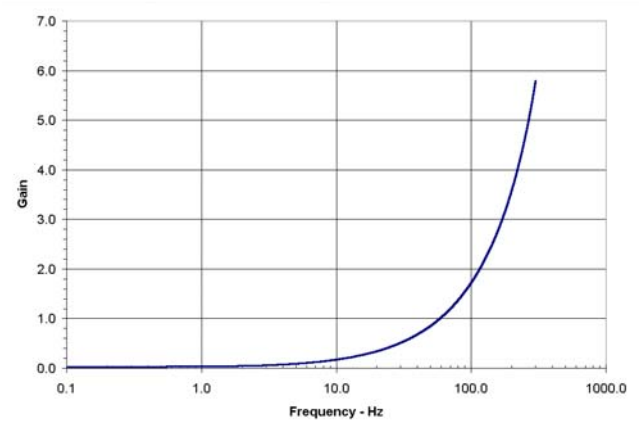


Figure 4.138: Mimic Filter Frequency Response Passes High Frequencies

When we implement the mho-type fault detector, we must compute two voltage phasors: the operating voltage and the polarizing voltage:

$$S_{OP} = I_r \cdot k \cdot ZL_1 - V_r \qquad \text{Equation 4.235}$$

$$S_{POL} = V_r \qquad \text{Equation 4.236}$$

where V_r is the particular loop voltage phasor, I_r is the particular loop current phasor, and $k\ (ZL_1)$ is the reach of the mho element.

In this example, we show the simpler case of a self-polarizing mho element. When computing the operating voltage, we must multiply the loop current by the positive-sequence line impedance scaled by the reach setting. We can do this in the frequency domain by multiplying two complex numbers, as shown in Equation 6.4. We can also do this in the time domain by equating the phase angle of the mimic of the preceding section to the phase angle of the line, then processing the current waveform through the high-pass filter. Next, multiply the phasor of the replica line impedance compensated current by the magnitude of the line reach. The advantage of this technique is that any dc offset is automatically removed. Equation 4.235 then becomes:

$$S_{OP} = I_r \cdot \left(1\angle\theta_{ZL_1}\right)k \cdot \left|ZL_1\right| - V_r \qquad \text{Equation 4.237}$$

From the angle of the positive-sequence line impedance, we can establish the constant τ_1 from:

$$\tau_1 = \frac{\tan\left(\theta_{ZL_1}\right)}{\omega} \qquad \text{Equation 4.238}$$

where $\omega = 2\ \pi\ 60$

Now use the same compensated current to compute the scalar product of Equation 5.4, necessary for assessing directionality of the fault. Doing this equates the local source phase angle to the line angle. If both the protected line and the source are inductive, even a large mismatch between these angles does not adversely affect the directionality. In theory, the mismatch θ could be as high as 90° before changing the sign of the scalar product.

In a practical digital relay design, the high-pass filter corresponding to Equation 6.2 processes all three-phase currents after the relay converts the currents to digital quantities. Then, the relay applies any algorithm for phasor computation and the compensated current phasors are available for any further processing.

4.4.1.6 Measurement of Superimposed Voltages and Currents

4.4.1.6.1 Definition of the Delta Filter

Figure 4.139 shows a delta filter, the conventional circuit used to extract a superimposed quantity. The basic delta filter subtracts from a time waveform the same waveform delayed by an integral number times the waveform period. In a delta filter, the delayed waveform is called the reference signal. The delay implemented in the filter is called the delta filter delay.

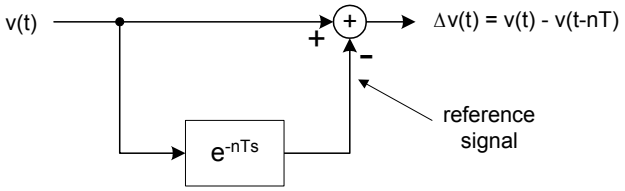


Figure 4.139: Delta Filter for a Time-Varying Waveform

4.4.1.2.2 Frequency Response and Time Response to Step-Function of a Delta Filter

A delta filter is a time-invariant linear filter. Figure 4.140 shows the frequency response of a delta filter with a delay corresponding to one 60-Hz period. This plot, however, is misleading because you might conclude that a delta filter rejects the 60-Hz fundamental component and the harmonics. The filter response to a unit-step 60-Hz sine wave is more revealing (see Figure 4.141). This figure shows that the filter output over an interval of time equal to one period is equal to the change impressed on the input waveform. In this case, the change is a unit 60-Hz period because the waveform originally did not exist.

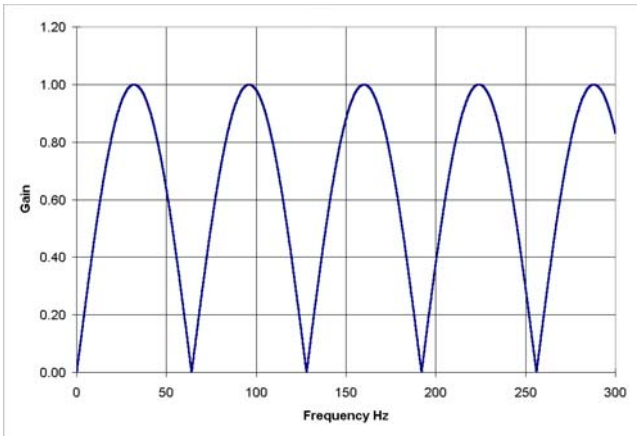


Figure 4.140: Frequency Response of a Delta Filter

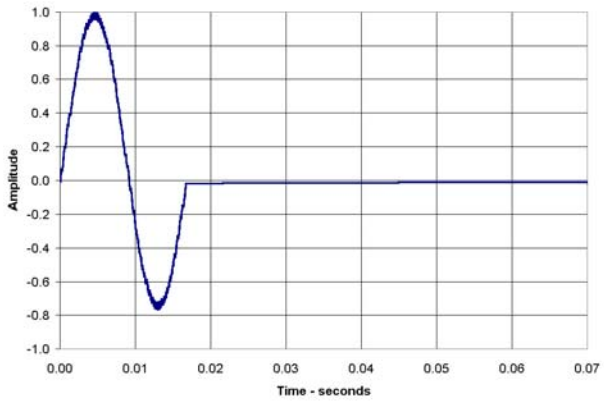


Figure 4.141: Time-Response to a Unit Step of the Mimic Filter Output

4.4.1.2.3 Adverse Effects on a Delta Filter

A delta filter should be tuned to a single frequency. Normally this is the rated network frequency: 50 or 60 Hz. Any change occurring after a fault on any frequency component other than the fundamental has an adverse effect on the delta filter output.

A second important issue with conventional delta filters is that the reference signal is constantly changing with time. Remember that we wish to subtract the waveform that existed before the fault. In a situation where we have a succession of network changes that last longer than the filter delay, the reference signal no longer satisfies this requirement.

A last issue concerns the fact that delta filters cannot handle some changes in a network topology. One example includes simultaneously energizing a line from both the local and remote terminals, such as a high-speed reclose. In this example, the delta filter does not produce relevant superimposed quantities. Do not assume that the pre-event line currents have zero magnitude because the line did not "exist" electrically before the line breakers were closed.

4.4.1.2.4 Application of Delta filters to Phasors

You can also apply delta filters to phasors. Figure 4.142 illustrates this concept. To accomplish this, you must have a time-invariant phasor or a phasor that remains still in the complex plane when no change occurs on the waveform. The delay implemented into the delta filter need not be equal any longer than an integral number times the waveform period.

When no change is taking place on a network, the incremental or superimposed quantities are zero. We can take advantage of this property and implement a change detector using the delta filter as shown in Figure 4.143. The relays compares the magnitude of the incremental phasor to a threshold INCR_TRH. When the change becomes greater than the threshold, a variable FREEZ indicating a change is set to 1. Because of the time-delay dropout, the variable remains asserted for a number of samples.

One of the shortcomings of the conventional delta filter is its difficulty in coping with a succession of changes that last an interval of time longer than the delta filter imbedded delay. This situation is easily handled if the reference phasor, as shown in Figure 4.142, is maintained during the evolving events. To achieve this, we introduce the concept of the "double-windowed" delta filter (patent pending) as represented in Figure 4.143. With this new principle, as soon as a change is detected, the value of the reference phasor is latched to a memory register. A second incremental quantity $\Delta V2$ is then generated using the memorized phasor as its reference. The main property of this second incremental quantity is that its reference phasor is fixed. If a series of changes occur on the network, the reference is always the same when computing the incremental value.

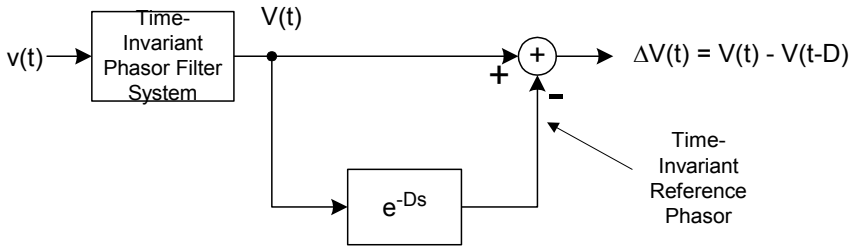


Figure 4.142: Concept of a Delta Filter Applied to a Time-Invariant Phasor

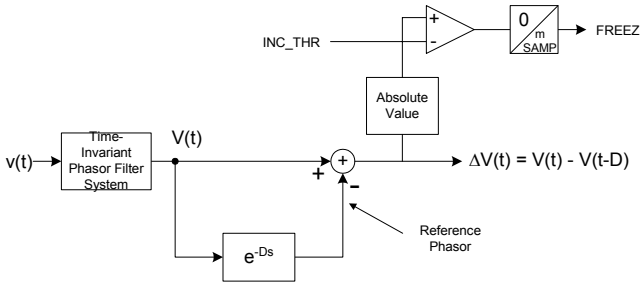


Figure 4.143: Concept of Delta Filter Applied With a Change Detector

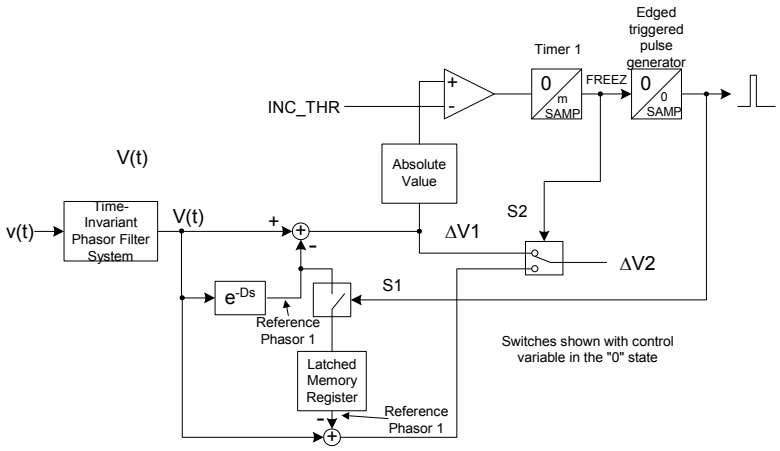


Figure 4.144: Concept of a "Double-Windowed" Delta Filter

4.4.2 Application to Relays

The idea of ultra-high-speed directional relays was first conceived in the late nineteen-seventies. There has been confusion between relays based on superimposed quantities and relays based on traveling waves. This is because relays based on traveling waves use the superimposed voltages and currents to assess the changes occurring on the line. Also, the initial research disclosed few details in the beginning about the practical aspects of the algorithms. More recently, superimposed quantities have been used to assess fault direction. For these applications, there was no strict timing requirement. This allowed using comparators processed in the frequency domain with the conventional use of phasors.

4.4.2.1 Implementation of Directional Elements

4.4.2.1.1 Implementation in the Time Domain

Using the scheme shown in Figure 4.145, we can implement a directional element that uses time-domain superimposed quantities. The combination of the integrator and threshold detector establishes a phase angle comparison. The phase angle comparison establishes the integrator output polarity: if the incremental voltage and the compensated incremental current waveforms are within ±90°, the integrator output is positive. The superimposed voltage and current are selected such that for a particular fault, the incremental impedance is equal to ($-ZS_1$). The superimposed quantities are normally zero if no change occurs on the network. If a forward fault occurs, assume for the sake of simplicity that the incremental voltage at the delta filter output is a sine wave as in:

$$\Delta vr(t) = \Delta v_R \cdot \sin(\omega t + \Psi) \qquad \text{Equation 4.239}$$

Using Equation 4.227 and accounting for any phase angle mismatch θ between the mimic and the source impedance, the incremental current after the mimic filter is provided by:

$$-\Delta irc(t) = \Delta v_R \cdot \sin(\omega t + \Psi + \theta) \qquad \text{Equation 4.240}$$

Integrating the product of the two incremental quantities results in the following equation:

$$COMP(t) = \Delta v_R \cdot \sin(\omega t + \Psi + \theta) \cdot \Delta i_R \cdot \sin(\omega t + \Psi + \theta)\, dt \qquad \text{Equation 4.241}$$

After an interval of time equal to one period, the integral has the value:

$$COMP(t) = \Delta v_R \cdot \Delta i_R \cdot \cos(\theta) \qquad \text{Equation 4.242}$$

The integral output at the end of the integration period corresponds to the scalar product of Equation 4.229.

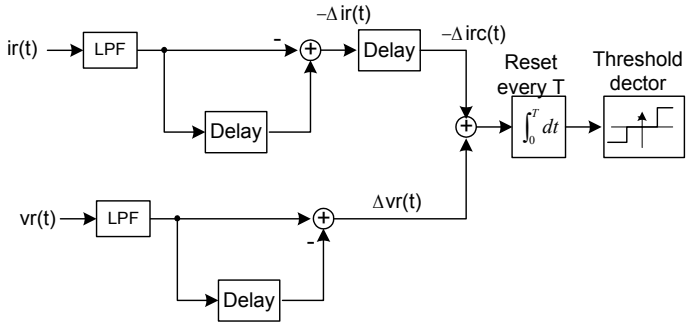


Figure 4.145: Time-Domain Generic Superimposed Quantities Directional Element

Figure 4.145 shows the integrator output *COMP(t)* for a forward fault with θ = 0° (perfect match between the mimic and the source impedance angles). Obviously the comparator output is positive from fault inception until time equals *T*. The basic

issue regarding this type of comparator is this: is the sign of the integrator output *COMP(t)* always the same as the sign of cos(θ) as time progresses from zero to *T* after fault inception?

To answer this question, look at the integrator output in Figure 4.147 for a reverse fault with θ= 0° and an impedance mismatch θ varying from 90 to 180°. With an ideal phase comparator, the output should always be negative. The normalized (with unit incremental voltage and current) maximum positive value calculated by the comparator is 0.16. The integrator output should be compared to this same threshold before declaring a forward fault. Using the 0.16 threshold results in the following comparison:

$$\mathrm{COMP}(t) = \Delta v_R \cdot \Delta i_R \cdot 0.16 \qquad \text{Equation 4.243}$$

Figure 4.145 shows this 0.16 threshold. Note the quick-response time indicated in Figure 4.145, better than one-quarter-cycle for a forward fault. There is, however, a shortcoming in this scheme. The threshold, to which the integrator output has to be compared, incorporates the product of the incremental voltage and incremental current magnitudes. Thus, these two values must then be user-entered settings in a comprehensive scheme. The directional element sensitivity is also impacted. If a fault occurs, such that the subsequent changes in the voltage and the current are smaller than the entered settings, the relay does not make a directional declaration.

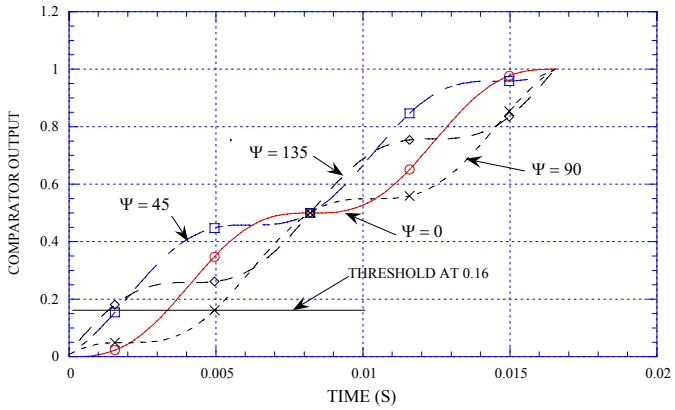


Figure 4.146: Comparator Output for a Forward Fault With θ = 0° and Ψ Varying

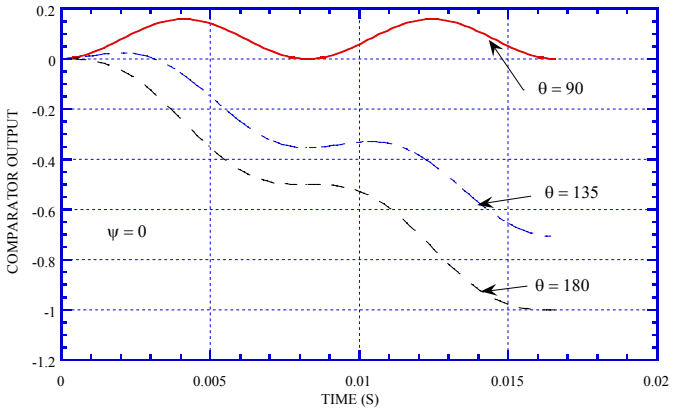


Figure 4.147: Comparator Output for a Forward Fault With ψ = 0° and θ = 90, 135, and 180°

4.4.2.1.2 Implementation in the Frequency Domain

The main advantage of implementing a superimposed directional element in the time domain is the speed (theoretically, less than one-quarter-cycle). There are two drawbacks; there is practically no filtering and the anticipated voltage and current changes have to be defined as settings. Overcome these two shortcomings by implementing the directional element using frequency domain input quantities. The implementation of Equation 4.229 (referenced below as Equation 4.244), representing the basic principle of a directional element in the frequency domain (using phasors), is shown as a straightforward design in Figure 4.147.

$$\text{real}\left(\Delta V_R \cdot \overline{\left(\Delta I_R \cdot 1\angle -ZS_1\right)}\right) = \Delta V_R \cdot \Delta I_R \cos(\theta) \qquad \text{Equation 4.244}$$

The speed of the directional element now depends on the data window of the selected filtering system. Direction assessment is still fast. For example, with a one-half-cycle Fourier filtering system for phasor evaluation, the response time is less than one-half-cycle. Schemes using filtering are then superior to schemes implemented in the time domain because there is no need to enter the anticipated changes as settings.

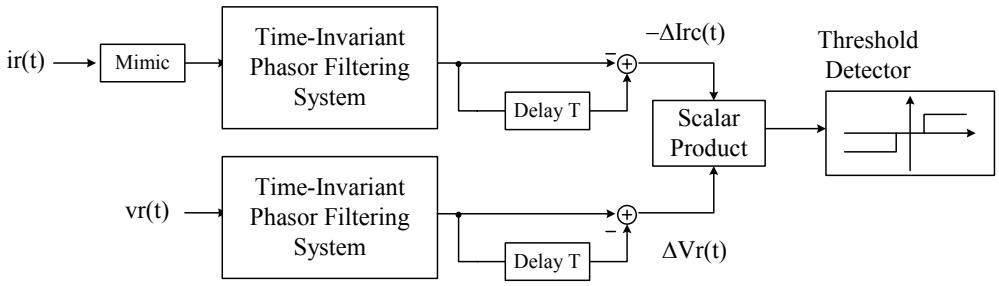


Figure 4.148: Frequency-Domain Generic Superimposed Quantities Directional Element

4.4.2.1.3 Implementation of Combined Phase-Selection and Directional Elements

Combine fast fault-type selection with directional assessment using the incremental impedances based on the differential (across two phases) superimposed voltages and currents. As shown in Table 4.14, for the single-line network (Figure 4.142), for any fault type, the incremental impedance is always equal to the negative of the source impedance behind the relay.

Table 4.14: Values of Differential Incremental Impedance

Fault Type	$\frac{\Delta V_{AB}}{\Delta I_{AB}}$	$\frac{\Delta V_{BC}}{\Delta I_{BC}}$	$\frac{\Delta V_{CA}}{\Delta I_{CA}}$
A-G	$-ZS_1$	0 / 0	$-ZS_1$
B-G	$-ZS_1$	$-ZS_1$	0 / 0
C-G	0 / 0	$-ZS_1$	$-ZS_1$
A-B, A-B-G	$-ZS_1$	$-ZS_1$	$-ZS_1$
B-C, B-C-G	$-ZS_1$	$-ZS_1$	$-ZS_1$
C-A, C-A-G	$-ZS_1$	$-ZS_1$	$-ZS_1$
A-B-C	$-ZS_1$	$-ZS_1$	$-ZS_1$

More useful and revealing information is obtained when the three incremental scalar products Δtab, Δtbc, and Δtca, corresponding to Equation 4.228 are performed. We define Δtab as:

$$\Delta tab = real\left(V_R \cdot \overline{\left(\Delta I_R \cdot 1\angle -ZS_1\right)}\right) \qquad \text{Equation 4.245}$$

In a practical application, the relay could assume that the local source impedance angle equals the angle of the positive-sequence line impedance. As described earlier, this can be done without changing the nature of the final results.

$$\angle ZS_1 = \angle ZL_1 \qquad \text{Equation 4.246}$$

With the incremental compensated current defined as:

$$\Delta I_{ABc} = \Delta I_{AB} \cdot \left(1 \cdot \angle ZL_1\right) \qquad \text{Equation 4.247}$$

When the current angular advance is provided by the mimic filter, we can now define the incremental scalar products as:

$$\Delta tab = real\left(V_{AB} \cdot \overline{\left(-\Delta I_{ABc}\right)}\right) \qquad \text{Equation 4.248}$$

$$\Delta tbc = real\left(V_{BC} \cdot \overline{\left(-\Delta I_{BCc}\right)}\right) \qquad \text{Equation 4.249}$$

$$\Delta tca = real\left(V_{CA} \cdot \overline{\left(-\Delta I_{CAc}\right)}\right) \qquad \text{Equation 4.250}$$

The relative values of the three incremental scalar products are shown in Table 4.15 for conventional shunt faults. As an example, for an A-phase-to-ground fault, Δtab

and Δtca are equal to some positive value and Δtbc equals zero. An A-phase-to-ground fault could unequivocally be inferred from the logic shown in Figure 4.149. In this diagram, CSTA is a constant number entered as a factory or user setting. To detect a reverse single-phase-to-ground fault, Δtab and Δtca must both be negative. In the case of a forward three-phase fault, all three scalar products are nearly equal and positive. The same logic applies to the other faults.

Table 4.15: Relation Between the Scalar Products

Fault Type	**Δtab**	**Δtbc**	**Δtca**
A-G	Δtab	0	tab
B-G	Δtab	Δtab	0
C-G	0	Δtbc	Δtbc
A-B, A-B-G	Δtab	0.25 Δtab	0.25 Δtab
B-C, B-C-G	0.25 Δtbc	Δtbc	0.25 Δtbc
C-A, C-A-G	0.25 Δtca	0.25 Δtca	Δtca
A-B-C	Δtab	Δtab	Δtab

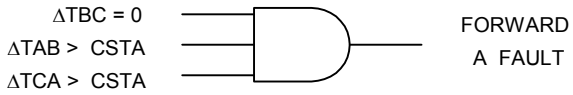


Figure 4.149: Logic to Establish a Forward Phase-A-to-Ground Fault

5 POWER LINES AND CABLES

LINE CLASSIFICATIONS

Power lines represent a large investment for utilities and incur the greatest number of faults by far. In the US the majority of transmission lines and distribution lines use overhead construction and are the most visible part of the power utility industry. Power lines are generally classified based upon operating voltage shown in Table 5.1 although no standard presently exists. Underground construction is also used for all power line classifications. (Need IEC's classification list – See Migners notes – not there????)

Table 5.1: Power Line Classifications

Classification	Operating voltage	Use or Function
Local Service	120V to 4kv	Circuits owned by the customer
Distribution	2.4kv to 34.5kv	Circuits from distribution stations to local service transformers
Subtransmission	13.8kv to 138kv	Circuits from generators to step-up / transmission stations and transmission stations to distribution stations
Transmission	115kv and higher	Circuits that carry large bulk power from points of generation to subtransmission and between utility systems

The customer generally owns local service circuits. Customers are classified based on voltage, load, and use, and are usually specified by the regulating body. Typical classifications include residential, agricultural, commercial, and industrial. Protection devices for residential circuits include fuses, circuit breakers, and ground fault interrupters (GFI). Large industrial customers may require the same protection devices that utilities use.

Line configuration, the potential for revenue, and the desired level of reliability and security dictate the relay equipment used in protection schemes for utility power lines. The differentiation between transmission and distribution relaying is becoming ever smaller as the cost of relaying equipment converges.

RADIAL LINE PROTECTION

Radial lines are those with a single positive sequence source and one or more loads, as illustrated in Figure 5.1. Historically, radial lines refer to distribution feeders. In the event that large commercial or industrial users assume responsibility for their own distribution, then subtransmission line can also be radial.

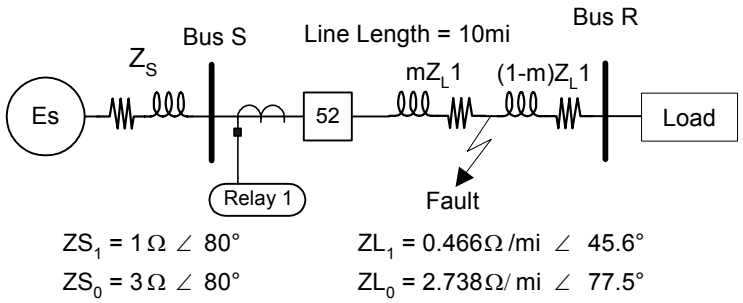


Figure 5.1: Protection for Radial Lines

It is a common misconception that radial lines do not require direction control. Consider the ground fault scenario illustrated by Figure 5.2. The symmetrical component network diagram for the fault shows that negative- and zero-sequence current will flow through Relay 2 even though Line 2 is not involved with the fault. One solution is to desensitize the relays that operate on negative- and zero-sequence current so they will not pickup for faults on adjacent radial lines. The closer the fault is to Bus S, the greater the current in the adjacent line. If the relays use direction control, then the reverse flowing current will block the operation of Relay 2. Therefore the sensitivities can be set according to the maximum negative- and/or zero-sequence current expected for normal operations.

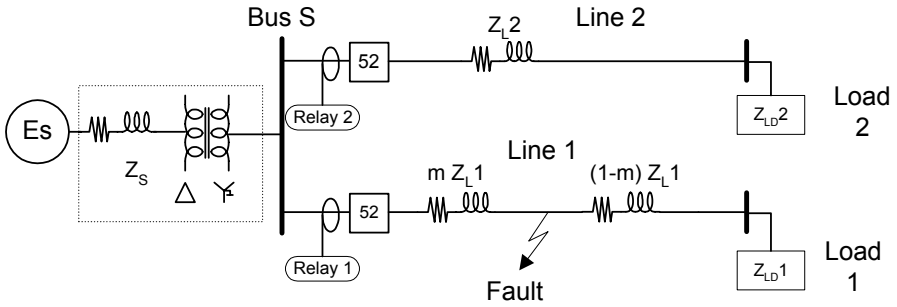


Figure 5.2: Influence of Loads on Parallel Radial Lines

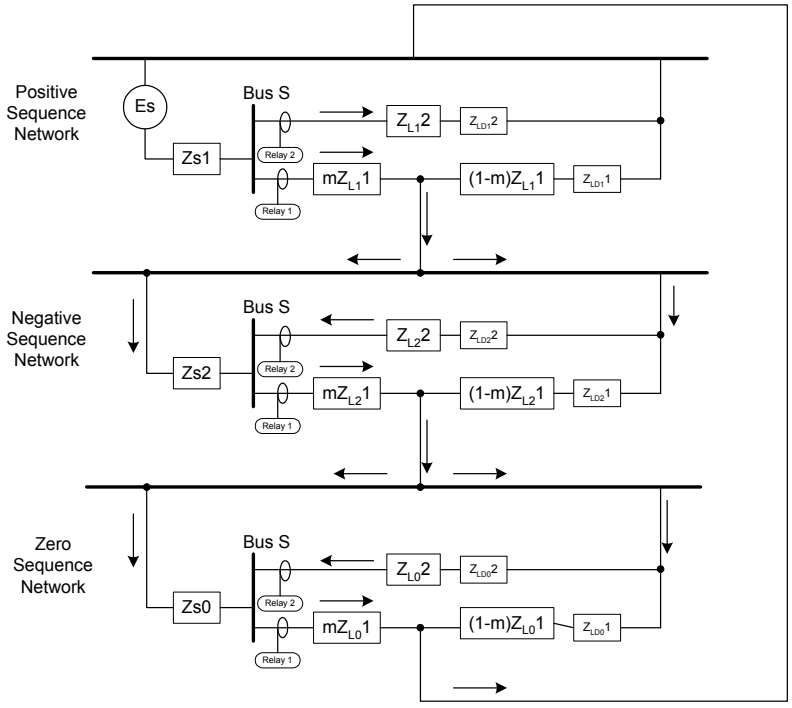


Figure 5.3: Sequence Configuration Diagram for Figure 5.2

Instantaneous Overcurrent Protection (50)

Instantaneous overcurrent protection provides fast operating time. The theory of operations for this type of relay is presented in section 0. As soon as the relay detects a current that is over a threshold setting, the relay will operate. Relays are set to see two different fault types, phase faults and ground faults.

Phase Fault Protection for Radial Lines

Usually instantaneous phase relays set the pickup current above 1.5 times the maximum expected load and below half the minimum fault current as shown in Figure 5.2. The maximum load current can be determined from billing records, knowledge of the customer's business, or load flow studies, all of which are subject to change without notice. Other factors to consider are maximum short time loads, asymmetrical offset, transformer magnetizing inrush, cold load pickup, and unusual operating conditions.

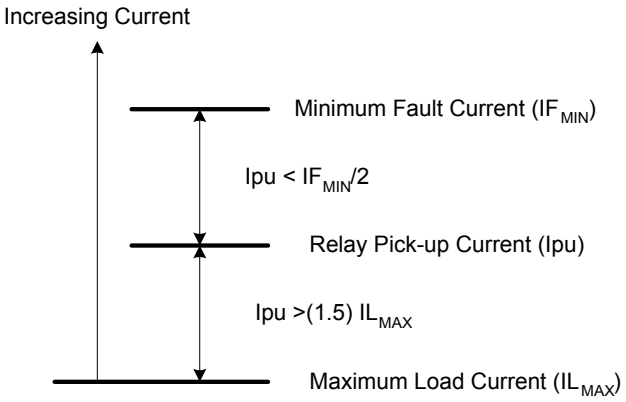


Figure 5.4: Relay Pickup Setting for Radial Lines

The minimum three-phase fault current is computed from the source voltage divided by the sum of the source and the total line impedance as shown in Figure 5.1. The loop circuit shown in Figure 5.5 shows that $I3\Phi_{MIN}$ can be computed using a single-line circuit model involving only the positive-sequence source and line impedances. The fault resistance for the three-phase case is the line-to-line fault resistance and is usually quite low since these types of faults are generally bolted faults. Hence R_f is set to zero in Figure 5.1. This is not the case for faults involving just two phases. Fault resistance must be included when applying Figure 5.1 to compute the minimum fault current making Figure 5.2 true only if R_f is zero. For arcing faults, the fault resistance can be determined from the model shown in Figure 5.3.

$$I3\Phi_{MIN} = \left| \frac{Vs_{LL}}{\sqrt{3}\left(m\,ZL1 + Zs + R_f\right)} \right|,$$

where

Equation 5.1

VS_{LL} = Source line to line voltage

Zs = Source impedance

ZL1 = Total line positive sequence impedance

m = per-unit distance from relay to fault

$$I\Phi\Phi_{MIN} = \left(\frac{\sqrt{3}}{2} \right) I3\Phi_{MAX}$$ Equation 5.2

$$R_f = \frac{440\ (\text{arc length})}{I}\Omega, \text{for } 70A < I < 20KA$$ [63] Equation 5.3

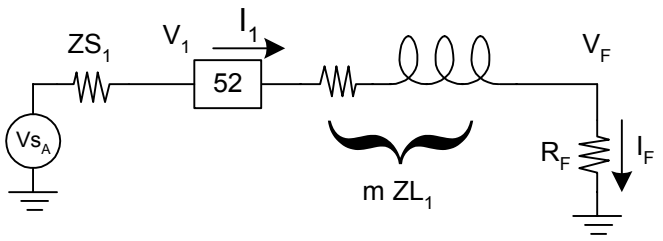


Figure 5.5: Circuit Loop for Three-Phase Faults

Use Figure 5.2 to compute the minimum phase-to-phase fault current for the case when R_f is zero. The model for the phase-to-phase fault as shown in Figure 5.7 sets R_{FG} to infinity. Although the line impedance is relatively predictable, the source impedance can vary greatly depending upon the power system configuration. For weak system, when the source impedance is high, you may not be able to find a pickup current that meets both criteria in Figure 5.4. For these cases, the load current can encroach into the pickup region and cause load induced trips. (These issues are discussed in greater detail in sections 0 and **weak infeed**)

Load can also influence the measured line current. The phasor diagram shown in Figure 5.6 shows that the load current is out of phase with the C phase fault current and in with the B phase fault current. If fault detection looks at only the phase currents, the C Phase relay may not detect a fault when it should where as B phase may detect a fault when it shouldn't. These overreaching and underreaching phenomena can be mitigated if the differences in the phase current are employed to detect phase faults.

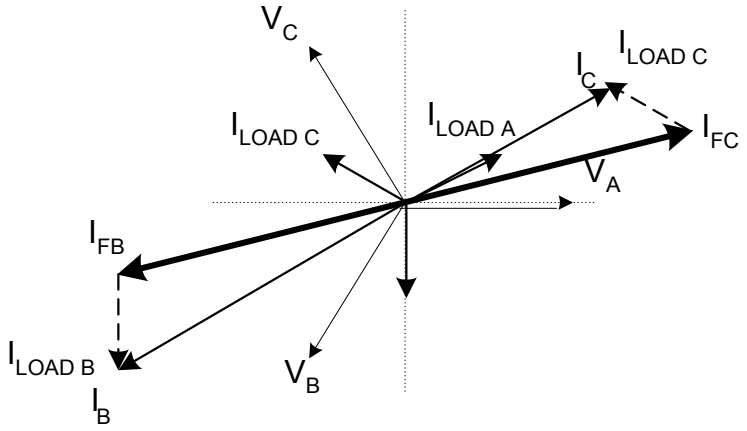


Figure 5.6: Phasor Diagram for a BC Fault

Mutual coupling also has effect but to a lesser degree than does load current. The amount of this effect depends on the degree of line unbalance and the distance from the relay to the fault. Line unbalance caused by to physical construction of the line and requires arranging the conductors so that the three self-impedances are equal and all six mutual impedances between conductors are equal. Figure 5.7 shows the correct polarity markings for the induced voltages. Roberts et. al. discuss the effects of line unbalance and the degree of unbalance for different tower configurations in a 1995 WPRC paper. [31]

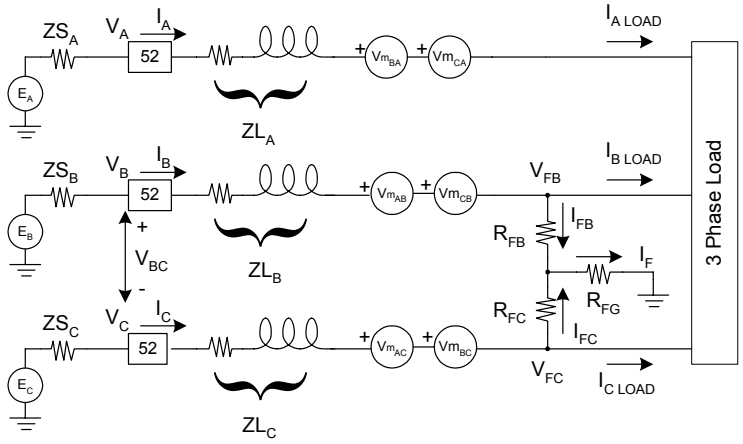


Figure 5.7: Circuit Loop for Phase-to-Phase and Phase-to-Phase-to-Ground Faults

Assuming the impedance values shown in Figure 5.1, for a 34.5 kV three-phase line, the minimum fault current for a three-phase fault with zero fault resistance is when m equal 1 and is predicted to be 3.61 kA. Using the same assumptions, the minimum fault current for the phase-to-phase fault is 3.13 kA.

Ground Fault Protection for Radial Lines

Ground faults may be modeled using the circuit shown in Figure 5.8. The difference between phase and ground fault models is that the phase impedance must be used for ground fault current calculations provided by Equation 5.4 and Equation 5.5 which result from Equation 2.53 through Equation 2.55. Zero-and negative-sequence currents are used to protect radial lines for ground faults. Figure 5.10 and Figure 5.11 show possible measuring sources of zero sequence current. The zero-sequence sources that are available for a relaying application depend on the construction and equipment for that particular line. Referring to Figure 5.10, the operating voltage restricts the use of the $3I_0$ derived from the sum of fluxes because of dielectric requirements for the three conductors in close proximity. Zero-sequence current derived from a transformer neutral requires a suitable transformer.

$$Zs = \frac{(Z0 + 2Z1)}{3} \qquad \text{Equation 5.4}$$

$$Zm = Z0 - Z1 \qquad \text{Equation 5.5}$$

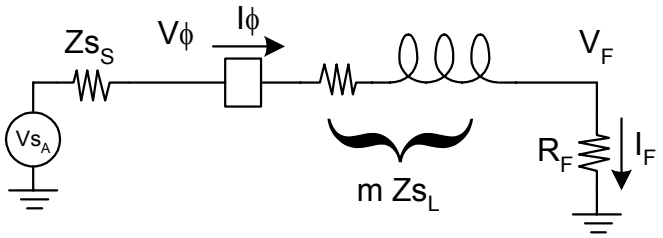


Figure 5.8: Circuit Loop for Single-Line-to-Ground Faults

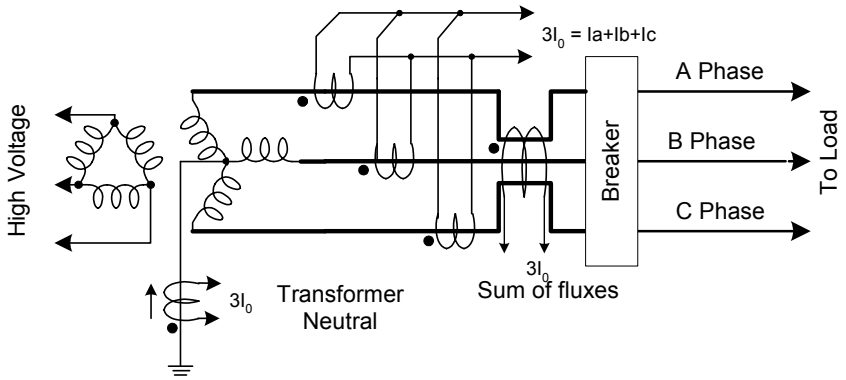


Figure 5.9: Possible Sources of Zero-Sequence Current for a Delta-Wye-Connected Transformer

The availability of the two $3I_0$ sources shown in Figure 5.9 also depends upon the transformer construction. To obtain $3I_0$ from the tertiary winding requires that the CT be internal transformer or that the broken-delta connections be brought out so that an external CT can be used. If summing the neutral currents to develop $3I_0$ as shown in Figure 5.10, the ratio of CTH to CTL must satisfy Equation 5.6 for the current ratio, I_H/I_L, equal to one. The currents of the two neutrals must be summed to include the current from the two possible paths. If the scaling provided by Equation 5.6 is not unity, relay sensitivity will be compromised.

$$\frac{I_H}{I_L} = \left(\frac{N_{WYE-L}}{N_{WYE-H}}\right)\left(\frac{N_{CTH}}{N_{CTL}}\right) \qquad \text{Equation 5.6}$$

Grounding transformers and grounded wye-delta transformers with no line connections on the delta side as provide measuring sources for I_0. In general, ground relays using $3I_0$ can be set to significantly more sensitive than phase relaying since loads usually generate little zero sequence current as compared to the phase current magnitude. Load unbalance from line to ground loads can have a more significant impact on the zero-sequence current that is generated under normal operating conditions. This unbalance can result from a poor distribution of single-phase loads on feeders or grounded wye loads. In these cases, using negative-sequence for detecting ground faults has better load rejection. However, for circuits made up of largely delta loads, zero-sequence currents have better load immunity.

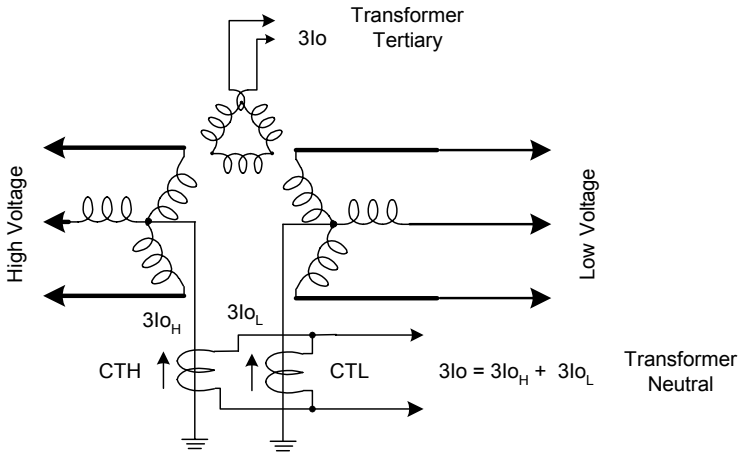


Figure 5.10: Additional Sources of Zero-Sequence Current From a Three-Winding Wye-Wye-Delta-Connected Transformer

Both the zero- and negative-sequence ground relay sensitivity is limited by the unbalance of the load and line in the circuit. However, the ground relay pickup needs to be set well above the sequence current expected from unfaulted operations. For example, if an unfaulted 30-mile 34.5KV line that is modeled using line parameters calculated in Appendix 11.3, is configured as shown in Figure 5.1, the symmetrical component currents shown in Table 5.2 result. A 407A balanced three-phase wye load generates nearly equal zero and negative sequence current. If the load is connected as a delta, for the same phase current, no zero sequence current is generated while 14A of negative-sequence current is produced. When the line is faulted at the load with a phase-A-to-ground fault, Table 5.2 supports the claim that the negative-sequence current is greater (thus more sensitive) for wye loads and zero-sequence is more sensitive for delta loads.

Table 5.2: Sequence Currents for a Phase-A-to-Ground Fault for Wye and Delta Loads

	Wye Load			**Delta Load**		
	$a0 = I_0/I_1$	I_1	$a2 = I_2/I_1$	$a0 = I_0/I_1$	I_1	$a2 = I_2/I_1$
No Fault	0.00733	407	0.00835	0.0	407	0.03439
AΦ - 3Ω	0.1538	572	0.3257	0.3146	445	0.2359

For an alternative demonstration, consider the sequence network for a single-line-to-ground fault as shown in Figure 5.11. For balanced wye loads, $Load_1$, $Load_2$ and $Load_3$ impedances are all equal. Higher the load (lower load impedance) results in reduced relay sensitivity. The positive sequence current measured by Relay S contains both load current and fault current. The negative and zero sequence current measured at the relay are reduced by the amount shunted through the load. More negative and zero sequence current is shunted through the load as the fault moves closer to the load make high resistance faults at the far end of the line more difficult to detect. Since the zero sequence line impedance is higher than the positive sequence impedance, more zero sequence current is shunted through the load than negative sequence current. Hence, relays operating on negative sequence current are

more sensitive for wye-connected loads than those operating on zero sequence current.

For delta-connected load, the impedance of $Load_0$ is infinite, meaning that the relay measures all the zero sequence current regardless of the load impedance. Negative-sequence current is shunted through the load as with the wye-connected load case while no zero-sequence current can flow through the load. The relay operating on zero-sequence current is sensitive to high resistance faults no matter where on the line they occur. Hence, relays operating on zero sequence current are more sensitive for delta-connected loads than relays operating on negative-sequence loads.

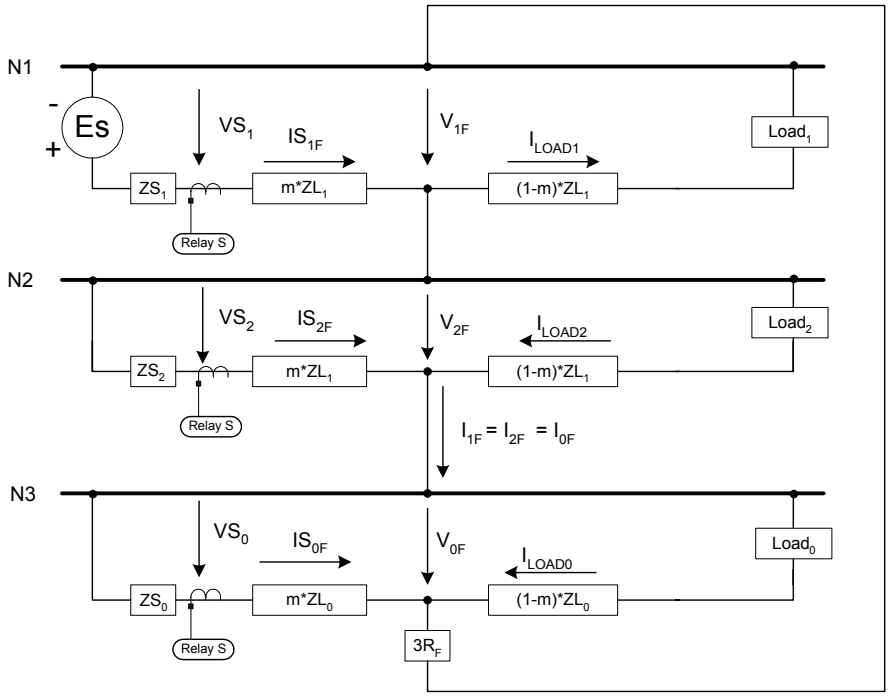


Figure 5.11: Sequence Network for a SLG-Faulted Radial Line

Since the relay sensitivity is limited by line and load unbalance when the load current is at maximum, greater sensitivity can be used when the system is operating at reduced loads. Relay sensitivity can be further improved by using the a2 ratio introduced in Table 5.2 to supervise the negative-sequence current relay as shown in Figure 5.12. The a2 ratio is established for the worse case that is usually at maximum load. Since all but three-phase faults generate negative sequence current, at full load, I_2 generated by the fault will in addition to that generated by the system unbalance. The output of Threshold Comparator #1 is asserted if the magnitude of the negative sequence is greater than the sensitivity limit set by the "a2|I1|" input. As load decreases, the "a2|I1|" threshold also decreases. For a no-load condition, the relay is set to its maximum sensitivity. The threshold setting for input to Threshold Comparator #2 can now be set for the desired reach of the relay. The logic shown in Figure 5.12 guarantees that the maximum sensitivity is used under all load conditions.

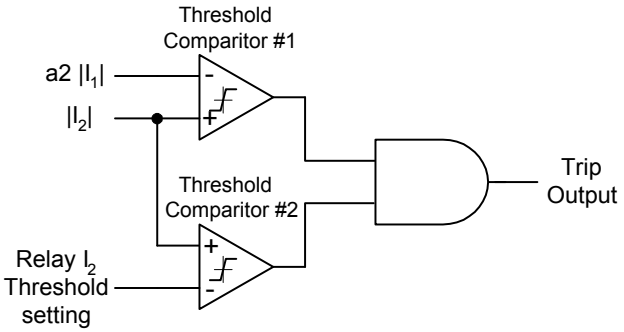


Figure 5.12: a2-Supervised Fault Detection Using Negative-Sequence Current

Time-Overcurrent Relaying - I2t (Type 51) Fault Protection for Radial Lines

In section 0, coordination is present as relates to load encroachment and line and/or load unbalance. If lines are configured as shown in either Figure 5.13 or Figure 5.14, then one or more relays must be coordinated with each other and/or with fuses. Time overcurrent relaying is frequently used for coordination of relays with fuses. The fundamental idea is that the higher the fault magnitude, the faster the relay will operate. Refer to the basic theory and concepts of time overcurrent relays discussed in Section 1 for more information on the relay operations.

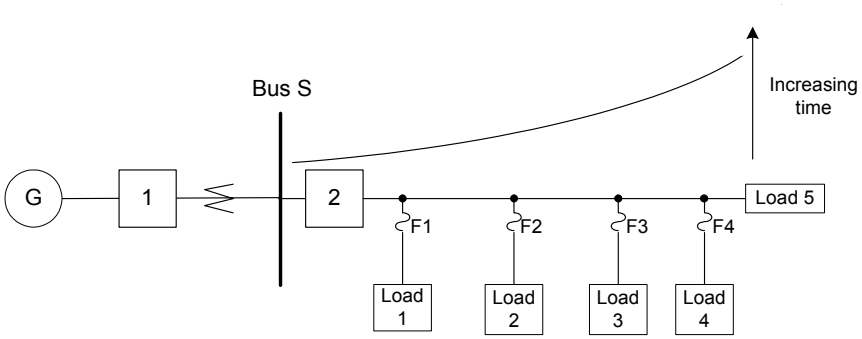


Figure 5.13: Radial System With Tapped Loads

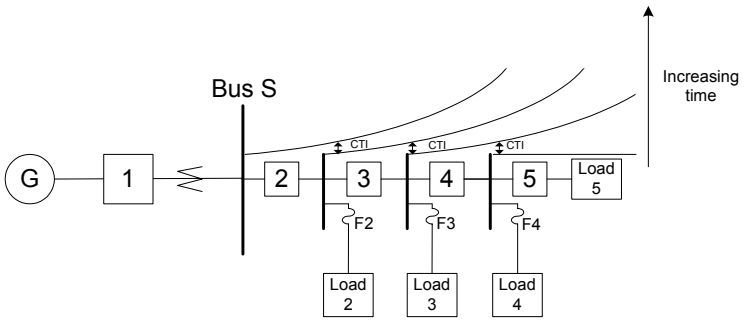


Figure 5.14: Multibreaker Radial System With Tapped Loads

Fuses, like time-overcurrent relays, are thermal tripping devices that clearing time is proportional to the current squared. They appear to be very basic devices but the proliferation of types and applications quickly reveals that they are highly complex.

A fuse consists of a resistive metallic conductor and is generally contained within an insulating container. The conductor is composed of one or more different metals depending upon the thermal characteristics desired. The list of metals includes bismuth, cadmium, lead, tin, silver, copper, and aluminum. The fuse characteristics that are shown in Appendix 11.4 plot three lines for the 65T fuse. The maximum clearing time is used for coordination of upstream fuses or relays. This time includes arc suppression and tolerance variances. The 75 percent of minimum melt curve shows the time until the temperature of fuse enters an area when the characteristics of the fuse are henceforth compromised and will no longer respond to currents in a predictable manner. The excessive heating of the metals in the fuse element makes the cold resistance higher causing the fuse to melt at a lower temperature.

Distribution systems generally use expulsion type fuses that confine the arc in a tube. The arc is extinguished by rapidly expanding gas resulting from an explosion direct toward one or both ends. Care must be exercise to direct the gas that is ionized away from other circuits to keep from inducing faults in unaffected circuits. The explosion creates considerable noise, which is an additional consideration when determining where the fuse is to be placed.

Most power fuses comply with the NEMA “E” rating and have time-current characteristics similar to those illustrated in Figure 4.6. Continuous carrying of rated current requires this type of fuse. For fuses rated less than 100A, the fuse must melt in less than 300 seconds for continuous currents between 200 percent and 240 percent of rated current. Fuses rated above 100A must melt within 600 seconds for this same current range. NEMA “N” rated fuses must melt from 300 to 600 seconds when the current is between 115 percent and 125 percent of rated current.

The fuse rating is determined by both the expected normal continuous current but also short-time overloads caused by energizing and switching surges as recommended by ANSI standard C57.92 – 1962. Severe overload conditions such as cold load pickup and transformer inrush situations require special considerations. Transformers can experience inrush currents 12 times the transform full time rating of to 0.1 seconds. Some dry-type transformers can experience inrush currents as high as 25 times the transformer rated current for as long as 10 ms. The voltage rating of a fuse must be equal to or greater than the phase-to-phase operating voltage to guarantee successful arc suppression. The fuse must also have a current interrupting capability greater than the maximum three-phase fault current. Only the source impedance to the fuse determines this.

Relays down stream of fuses must use the 75 percent melt time as the minimum upstream operate time. Hence these relays need to operate in less time than the fuse time plus breaker time.

Time-Current Coordination [6053][27]

Time that is controlled by current magnitude permits discriminating faults at one location from another. There are three variables available to discriminate faults, the time dial setting (TDS), the pickup current and the degree of curve inversness. Using the circuit shown in Figure 5.15, the following procedure can be used to determine these three time overcurrent settings for the type 51relay at Bus S. This example assumes that the relay is to provide backup protection for the fuse and hence must see the faults at the load under all conditions. Coordination is most difficult when the

source impedance is high compared to the line impedance and there is a large range of possible source impedance values.

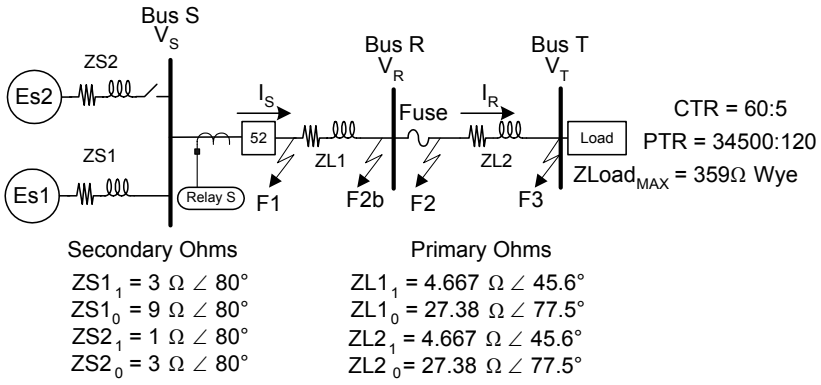


Figure 5.15: Single-Line Diagram for Fuse-TOC Relay Time Coordination

Step 1)

Determine the maximum and minimum three-phase, phase-to-phase and phase-to-ground fault currents for the fault locations identified in Figure 5.15. The minimum fault current is when source Es2 is not connected and the maximum fault current is when both Es1 and Es2 are connected. The results are presented in Table 5.3. Since the source impedance changes by a factor of four depending upon whether source Es2 is connected or not, it is not surprising to see the fault currents change by a factor of three to four as well. The data in Table 5.3 verifies that there is little difference in fault current for the three fault locations when the source impedance is high.

Table 5.3: Fault Currents for Coordinating System Shown in Figure 5.15 for Zero Fault Resistance

Fault Type	Source Z	F1 Amps Sec.	F2 Amps Sec.	F3 Amps Sec.
3Φ	Max	22.34	21.34	20.41
	Min	89	75	64
Φ-Φ	Max	19.35	18.48	17.68
	Min	77	65	55
Φ-G	Max	13.40	12.36	11.46
	Min	54	40	32

$Zload_{MAX}$ = 359Ω primary = 13.3Ω secondary

Step 2)

Plot the currents for faults at F2 and F3 on a fuse time-current chart to determine the minimum and maximum fuse operating times for faults at these locations. The currents listed in Table 5.3 have been normalized in Table 5.4 so that relay and fuse operate times are based on same multiples of pickup current Figure 5.16 and Figure 5.17 show the time current points for the four fault scenarios.

Table 5.4: Currents Listed in Table 5.3 Converted to Multiples of Pickup Current for the 60A Fuse

Fault Type	Source Z	F1 p.u. Amps	F2 p.u. Amps	F3 p.u. Amps
3Φ	Max	4.47	4.27	4.08
	Min	17.8	15	12.8
Φ-Φ	Max	3.87	3.69	3.54
	Min	15.4	13	11
Φ-G	Max	2.68	2.47	2.29
	Min	10.8	8	6.4

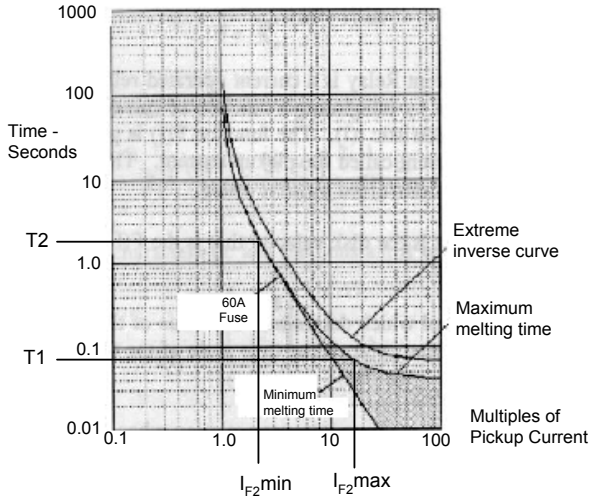


Figure 5.16: Minimum and Maximum Fuse Operate Times for a Fault at F2

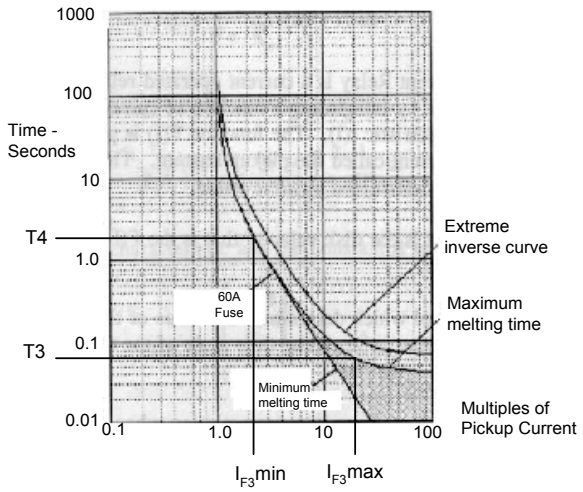


Figure 5.17: Minimum and Maximum Fuse Operate Times for a Fault at F3

Step 3)

Since the Type 51 relay at Bus S must see the entire length of the line based upon our assumption that the relay is to provide backup protection for the fuse, the relay pickup current must be set more sensitive (below) the minimum fault current for a fault at F3. For this example, the minimum pick is 2.29 p.u. or 137A.

Step 4)

Select a relay with a time-current curve that parallels the fuse time-current characteristics in the region below I_{F3}max.

Step 5)

Set the relay operate time to be above the fuse operate time plus the fixed CTI (Coordination Time Interval) for maximum faults at F2 using the TDS.

Only when the line impedance is significant when compared to the source impedance is discrimination possible. Since, for this example, the minimum currents at F1 and F2 are nearly the same, little time difference is available to discriminate faults on the upstream side of Bus R from faults to be cleared by the fuse. For the relay at Bus S, faults at F2 are indistinguishable from those at F2b. The penalty for the coordinated backup protection is slow operations the entire length of the Bus S to Bus R line. The constraint of the minimum current fuse operate time limits the maximum relay operate time to 2.7 seconds at F2, hence requires a TDS setting of 3. (See Appendix 11.1, Figure 11.4)

If the dynamic range of the source impedance is comparative small (less than perhaps two to one) and the line impedance is significant as compared to the source impedance, faults can be more easily discriminated. Hence, a type 50 relay could be used to protect the first 80 percent of the line between Bus S and Bus R with instantaneous operation and let the type 51 relay protect the last 20 percent and provide backup protection for the fuse.

Minimum TOC Pickup Settings

The protection objective is the set the relay pickup to be as sensitive as possible, so it operates as quickly as possible without violating coordination principles. Pickup settings of the most downstream fuse or relay are set in accordance with sections 0 and 0 with the aid of a load flow and fault study programs. The maximum and minimum fault currents are determined for each pickup setting protected by a relay or fuse from fault studies or traditional loading. In the absence of better information, the lesser of line rating or transformer rating can be used. The pickup relay value can be set by computing maximum relay fault current divided by the CTR times the minimum downstream fault current fuse or relay as was described in step three above.

For electromechanical relays, the relay had tap settings that acted as a secondary current transformer. These electromechanical relays restrict tap values to a discrete set while microprocessor relays allow fractional tap values.

The pickup value must be set sufficiently sensitive to see faults at the end of the protected line and yet not pick up for load. This is not always possible for systems with weak sources. In such cases, load encroachment blocking becomes necessary. (See section 0.)

Consider the time-current coordination of the system shown in Figure 5.13. Relay 5 requires only an instantaneous element set according to section 0 because there are no downstream devices to coordinate with. The minimum pickup is Relay 4 is also set according to section 0 with the difference being that Load 4 must now be considered.

TDS Setting

Time dials are set to create the necessary coordination time interval, CTI, to guarantee that the relay sees to the end of the next protected line segment but does not operate faster than the primary protection of the next line segment. Factors that influence an acceptable CTI are the maximum breaker fault clearing time, the relay disk over-travels (caused by inertia in electromechanical relays), and a safety margin to account for instrumentation errors, loads, and breaker-failure operate times. Typically the CTI of 0.3 seconds is used although this may vary from 0.2 to 0.5 seconds. This should be used unless there is justification otherwise.

Inverse Settings

Degrees of inverseness can also aid in discriminating faults by time. In general, use relays with similar inverse characteristics for easier coordination. Flatter inverse curves (weakly inverse, moderately inverse) are appropriate for the following conditions:

No coordination is required or the relay is the farthest downstream.

The line is short or there is little current difference for faults close to the relay and faults at the ends of the line.

Instantaneous operations provide good coverage.

Relays with inverse characteristics provide faster clearing times than relays with very or extreme inverse characteristics when the minimum fault current is significantly greater than the maximum load current. Relays with the latter two characteristics are used when:

The fault current is much greater when the fault is closer to the relay compared to when the fault is at the far end. This is the case when the line impedance is large compared to the source impedance.

When the short-term load is high or load encroachment is a potential problem.

When coordinating relays with downstream fuses and reclosers.

Modern relays permit implementing unique curves that follow no standards for applications where none of the standard curves provide the desired protection. However, doing so repeatedly without good justification can complicate relay coordination efforts in the future.

Time-Current Coordination Example #1

Consider the system illustrated in Figure 5.18 where the task is to coordinate a single time overcurrent relay with the fuse F1 that has characteristics similar to those shown in Figure 4.6 or Appendix 11.4 and the calculations for this example are included in Appendix 0. One must first determine the load and fault currents at the boundary conditions. For this example, the maximum relay current is three-phase fault at Bus S and the minimum relay current is a phase fault current at Bus T. The results of the fault current calculations are shown in Table 5.5.

The maximum per phase load current at Bus R is 50A; a 65E fuse is selected since that is the conventional size fuse greater than 125 percent of the maximum load current. The fault minimum fault current at Bus R and Bus T determines the basis for the coordination time needed for the phase and ground relay units. For a fault at Bus R, the maximum fault current occurs for a three phase-to-phase fault. Since the relay must be set sufficiently to see faults at Bus T which, for this example, is 9 secondary amps. According to the requirements set in section 0, the relay pickup current can be set as low 1.5 time the maximum load current or 3.125 secondary amps. Doing so makes the minimum fault current 2.88 multiples of the relay current and 216 primary amps for the fuse. From the fuse time current graph shown in Appendix 11.4, the fuse melt time is 8 seconds. Thus, to coordinate relay ground fault times with the fuse requires that the relay wait the 8 second fuse operate time. The CTI can be ignored for this case as there is no breaker-operate time to consider. Hence for the extremely inverse curve, the TDS must be set above 10.

The second point of the relay coordination, the relay can operate no faster that the fuse for three-phase faults at F2. The fuse current for is case is 3,340 primary amps and, according to the maximum melt time, is 0.04 seconds. 3340 amps primary is 44.5 multiples of the pickup current that was set to 3.125 secondary amps in the preceding paragraph. According to the extremely inverse time-current curve shown in Figure 11.4, the TDS could be set as low as 1.0. However, the constraint placed by the ground fault current at Bus T, the relay operate time for three-phase faults at Bus R is limited to 0.4 seconds.

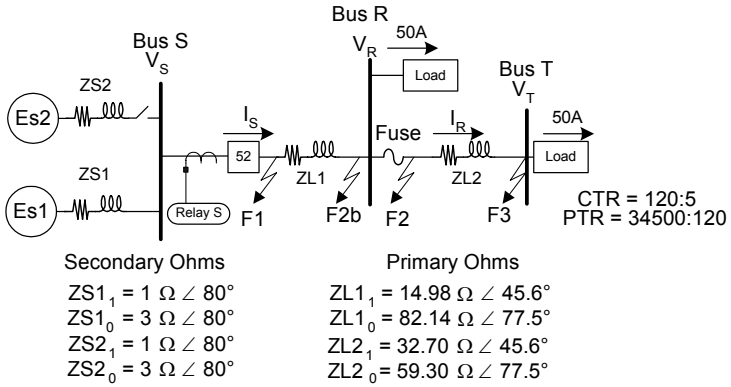


Figure 5.18: Single-Line Diagram for Time Coordination Example #1

Table 5.5: Relay Currents in Multiples of Secondary Full-Load Amps (5A) for System Shown in Figure 5.18 With No Load

Fault Type	Source Z	F1 sec. amps	F2 sec. amps	F3 sec. amps
3Φ	Max	139	41	24
	Min	69	32	21
Φ-Φ	Max	119	36	20
	Min	60	28	18
Φ-G	Max	83	18	10
	Min	42	15	9

The relay ground elements must be coordinated with the fuse as well. The coordination problems become significant when the ground fault current is on the same order of magnitude as the load current. Such is the case with this example where the phase current for a ground fault at Bus 3 is only 135A as compared to the load maximum current at Bus 1 of 100A. For a Bus 3 ground fault, the maximum fuse operate time is 2.5 seconds while for Bus 2 ground faults, the fuse operate time is still only 1.3 seconds. Even though the relay can be set to operate much faster, it must wait at least 1.6 seconds before clearing faults at Bus 2 on the source side of F1 in order to maintain the coordination. The problem is caused by fuse insensitivity to zero sequence currents. Solutions to this problem are presented in section 0. Aforementioned shortcomings of fuses not withstanding, in the correct application they can provide reliable and cost effective protection.

Distance Protection of Radial Lines

The problem presented at the end of the previous example is caused by the inability to discriminate between load current and fault current. Hence relays must wait for insensitive thermal elements to operate. The reasons for using distance relaying rather than time-overcurrent are listed in section 0. The two major advantages are increased fault sensitivity and reduced load sensitivity. Distance relays operate on the principle that the impedance is computed as the ratio of the phase voltage to the

line current. If the distance is computed using the negative-sequence impedance, the ratio of V_2 to I_2 is independent of both fault impedance and load current.

Delayed zone tripping where the reach is extended over a portion of the next protected line segment provides backup protection. A distance protection scheme for a radial line is shown in Figure 5.19. Relays 2, 3 and 4 require coordination of the backup Zone 2 protection with the faster primary Zone 1 protection. Take care to set the Zone 2 reach for Relays 2 and 3 so that it does not extend beyond the beginning of the Zone 2 of the next downstream relay. If, for example, the Zone 2 of Relay 2 extends beyond the start of Zone 2 for Relay 3, a fault in the overlapped section of line will cause both Relays 2 and 3 to operate. The constraint for setting the Zone 2 reach for Relay 4 is that it should avoid load encroachment. Relay 5 can be an instantaneous overcurrent relay as there are no relays for it to be coordinated with.

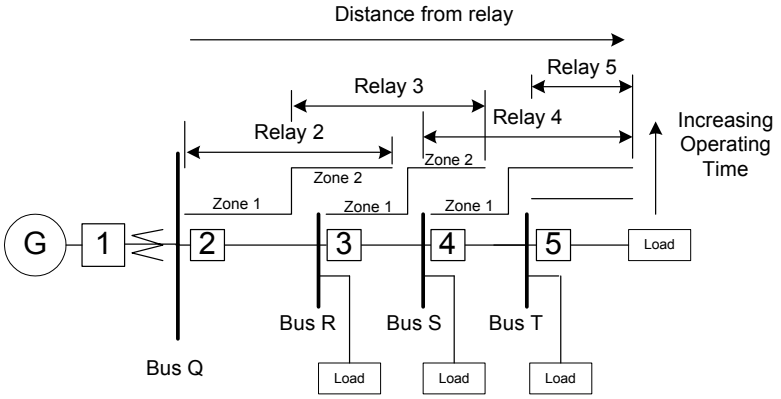


Figure 5.19: Distance-Protected Radial Line

Mho Versus Quadrilateral Elements

The mho element is recommended when the fault resistance coverage is sufficient for the application at hand. Shorter lines or those with low line impedance have mho circles that are small, resulting in limited fault resistance coverage. Since the fault resistance is independent of line impedance or distance to the fault, mho elements have very little fault resistance coverage for close-in faults. The resistive reach of the quadrilateral element is independent of the reactance reach of the relay and can be made to have considerable fault resistance coverage for close-in faults.

Increasing Sensitivity

Fuses can only work with current magnitude and must be set to carry full load. Relays, on the other hand, can be set to be more sensitive than fuses because they are able to use algorithms that are less affected by load. As discussed in section 4.2.4.1.2, negative- and zero-sequence currents are highly dependent on fault currents but affected little by load current. Consider the example shown in section 0 with the 50A load increased to 200A at Bus R. For this case, the minimum ground fault current at F3 is less than the total maximum total load current at Bus S (see Table 5.5). Hence the relay operating on phase current alone at Bus S will no longer be able

to distinguish between maximum load and fault current at maximum source impedance. Negative-sequence time overcurrent relaying provides a higher degree of sensitivity that is immune to load. A.F. Eleneweihi presents such an approach????. [76]

Ground fault resistance presents additional difficulties for fuses for reasons similar to those just described. Some utilities require fault ground fault detection in the presence of as much as 40 ohms-secondary fault resistances. For the example of section 0, 40 ohms secondary would be equivalent to 480 ohms primary, resulting in a maximum fault current of 40A. Hence the fuse will not clear the fault regardless of the fault location. Both zero- and negative-sequence ground overcurrent relaying are able to detect the fault but coordination with fuses is no longer possible. In the cases where a fuse is incapable of detecting faults, or at best clears faults very slowly, definite time-delayed zero- or negative-sequence overcurrent is used to provide faster backup protection.

Other methods of increasing sensitivity are presented in the following sections.

Instantaneous Overcurrent – the 50-51 solution

A frequent solution to the sensitivity problem discussed in section 0 is to use both instantaneous overcurrent and time-overcurrent elements in a relay. The reach of the instantaneous element is set to cover 80 percent of the line from the relay to the first fuse. This limits the probability that a fault will cause unnecessarily long operations.

Reclosers [????GLOVER and SARMA Section 10.5, pp. 394-397][77]

Reclosers are self-contained fault breakers with fault current interrupting capability. They can be used with instantaneous, time-overcurrent, and distance relay elements. Their autonomous operation allows them to be used anywhere along a radial line. They are typically used in the types of systems illustrated by Figure 5.20. Reclosers allow relays to see end-of-line faults more easily and reduce coordination complexity. As their name implies, reclosers automatically reenergize the line after a fault. This is based on the premise that over 80 percent of distribution faults are temporary and caused by such things as squirrels, birds, tree branches, and lightning shorting a conductor to ground or wind blowing two conductors together. Reclosers are programmed to generate a limited number of trip-close sequences in a specific interval of time. The feeder protection downstream and the equipment that must supply fault current on the source side of the recloser determine this number.

Coordinating reclosers with fuses overcomes the sensitivity problems presented in section 0. Typically type “T” fuses are used because their characteristics are well suited for time coordination with reclosers. Reclosers can use instantaneous and time-delay tripping to minimize fuse operations.

If the instantaneous element operates for faults also protected by fuses, the reclosers saves fuses at the expense of momentary outages for all loads on the feeder. If the instantaneous reach is set so that it does not cover sections protected by fuses, then recloser operations are reduced at the expense of necessitating maintenance and potentially longer times to clear faults. Such schemes are referred to as fuse-saving and trip-saving schemes, respectively.

Sectionalizers

These devices effectively replace fuses. They are placed along radial lines to restrict the outage area caused by a fault. Sectionalizers are not designed to interrupt current, neither fault nor load, and therefore must operate under their own power when the line is dead. Typically a battery that is charged when the line is energized provides this power. In Figure 5.20, the breakers numbered 3 through 5 are sectionalizer switches while breaker number 2 is a recloser-type breaker. The relaying controlling Breaker 2 senses the fault and continues to trip and reclose the breaker until either the fault is cleared or the number of operations causes the relay to go into a lockout condition.

The sectionalizer switches are programmed to operate after a specific number of line trip-close operations. The sectionalizer must also sense that the line was carrying fault current immediately preceding the last trip operation. The sequence of trip-close operations must occur within a limited period of time or the counter will reset. For example, sectionalizer number 3 would be programmed for three counts, number 4 for two and number 5 for one count. This provides the line segment nearest the load with one trip-close operation to reenergize that section in the event that the fault cleared when the line was deenergized. If a permanent fault is applied between sectionalizers numbers 3 and 4, number 3 would open after the third trip-close operation. Sectionalizers must be manually reset after they have gone to lockout and the fault has been cleared. Switches 4 and 5 do not need to be reset, because they saw no fault current.

Since the fault discrimination is not based upon time, the recloser at breaker number 2 can operate on overcurrent alone. This relay must be set with sufficient sensitivity to see faults all the way to load number 5 but not operate under normal operational conditions. If this cannot be achieved, then some sectionalizers will need to be replaced with recloser breakers.

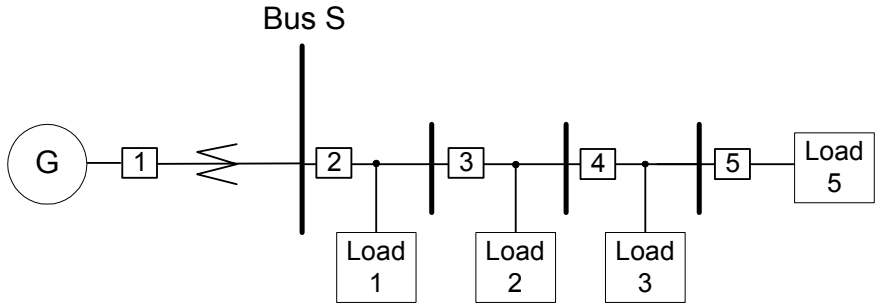


Figure 5.20: Radial Line Using Sectionalizers

Load Encroachment Blocking

The difficulty in relay coordination for lines with weak sources, whether for overcurrent or distance relaying, is to have sufficient sensitivity to provide the needed protection yet not trip for loads. Directional elements are necessary for looped lines, as discussed in section 0. Directional elements can help reduce the exposure to load-induced trips as shown in Figure 5.21 and Figure 5.22 but pockets

of exposure remain. Other options for improving load rejection include quadrilateral-based distance relaying and reactance relaying. (See section 4.1.1.2.) To inhibit tripping for load encroachment areas, those voltage and current relationships that define potential operation conditions must be identified before any fault detection begins. In order to achieve the objectives for both security and sensitivity, there must be sufficient separation to allow the sensitivity of the relay to discriminate between load and fault current or impedance. Thus the wider the angle between the line angle and the maximum load angle shown in Figure 5.21 and Figure 5.22, the better the security.

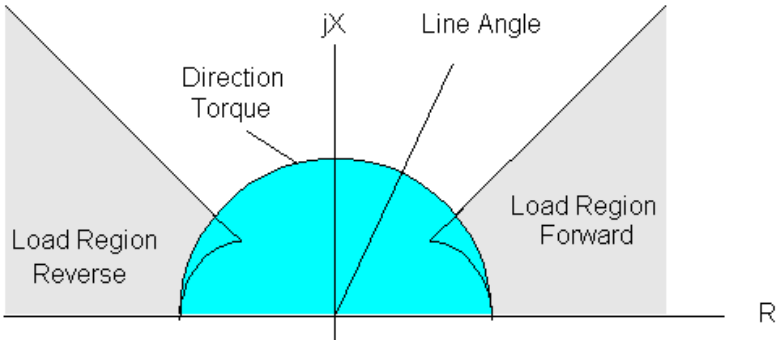


Figure 5.21: Directional Torque Applied to Overcurrent Relaying

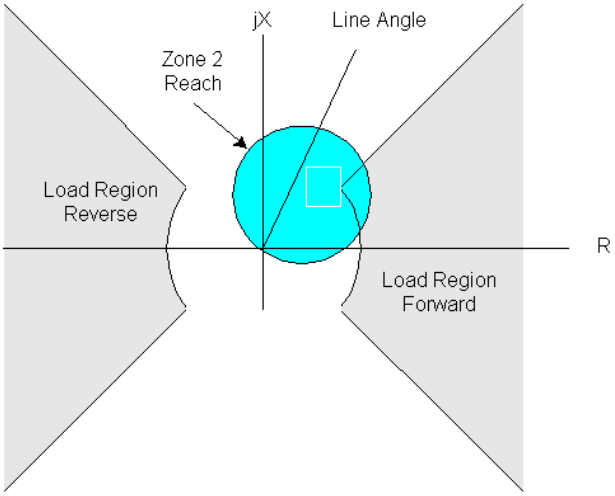


Figure 5.22: Load Encroachment Blocking for Distance Protected Lines

PROTECTION OF LOOPED SYSTEMS

Looped lines that are configured as shown in Figure 5.23 and Figure 5.24 result from a need for higher service reliability than is offered by simple radial lines. They may also result from lines that are normally operated from multiple sources but have become isolated because of normal or prior relay operations. Figure 5.23 shows a looped configuration for distribution feeders that increases reliability by decreasing exposure for critical loads. Only the load at Bus Z has dual sources and therefore

should be the critical load. The loads at all other buses will be lost when the fault on the adjacent line is cleared. For example, clearing a fault on the line connecting Bus U to Bus V will drop off the load at Bus 4. In this configuration, all relays are nondirectional except the relay at Breaker 5, so faults on the line between Bus Y and Bus Z can be distinguished from faults on the line between Bus V and Bus Z. Backup protection is provided by time coordination or by setting the reach of the Zone 2 element of distance relays.

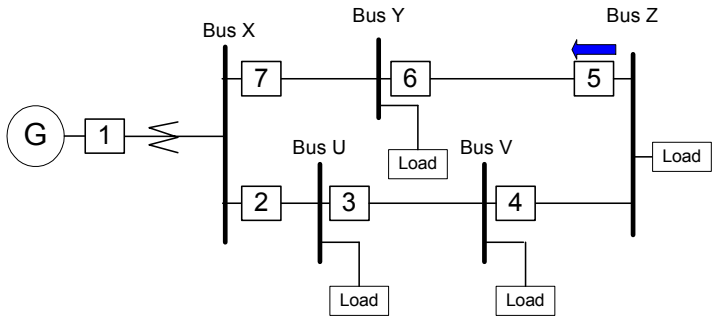


Figure 5.23: Looped Distribution Feeder

Figure 5.24 shows a looped system where all loads have dual sources. The cost of this additional service reliability is the added expense of an additional relay and breaker per bus, and also that the relays at all buses except Bus X must be directional. Only relays at Bus X can be nondirectional since current can only go one way through those lines.

Both distance and time-overcurrent relays can be used for fault detection. Using one of the pilot schemes discussed in section 4.1.1.5 achieves significant improvements in speed performance.

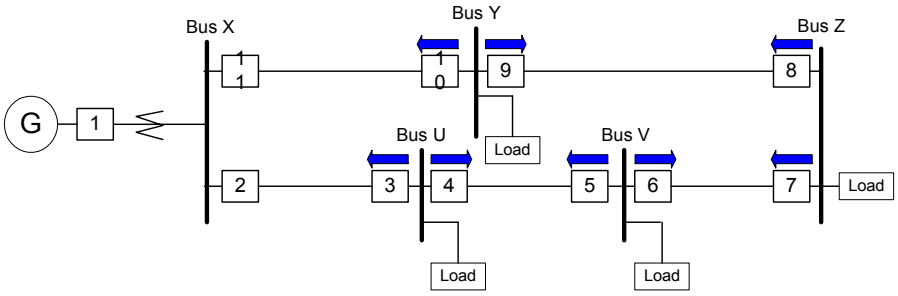


Figure 5.24: Looped Configuration

Sympathetic Tripping [6061][78]

The slow tripping of adjacent radial lines or out-of-zone faults on radial lines is called sympathetic tripping. This phenomenon is more of a power quality issue than an equipment protection issue. A ????paper by Roberts presents a detailed discussion of the nature of sympathetic tripping and classical and innovative solutions to the problem. [79]

One problem with slow fault clearing is that the longer the power sags to support the fault current, the greater the effect the low voltage has on equipment attached to the

unfaulted sections of the line. Figure 5.25 shows the dropout-time characteristics for various types of loads. ASD refers to industrial adjustable speed drives that are used with induction motors for variable speed control. Contactors are magnetically latched power switches and operate similarly to instantaneous undervoltage relays. The CBEMA curve is an industry standard for business machines and electronic equipment. The Information Technology Industry Council, which developed this curve, has recently adopted the curve shown in Appendix 511.6. For the example in preceding section, the voltage at Bus 2 will sag to 21 percent of nominal for phase-to-phase faults and 24 percent for phase to ground faults. According to the information shown in Figure 5.25, most, if not all, loads would drop out for faults on the fuse-protected section of the line.

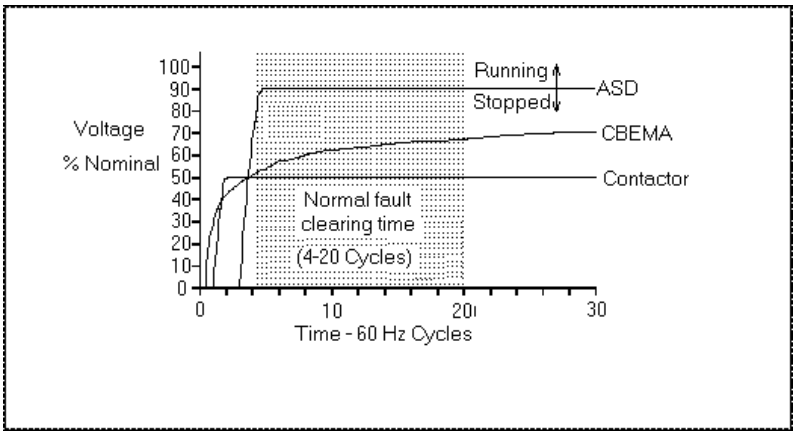


Figure 5.25: Dropout Times for Various Types of Voltage-Sensitive Loads

Voltage Drop Profile Example

Assume that a distribution line configured as shown in Figure 5.14 has the electrical characteristics shown in **Error! Reference source not found.**. Also assume that each tap has a fuse at 50 A per phase, resulting in a maximum load of 250 A per phase. To meet the criteria imposed by **Error! Reference source not found.**, the minimum fault current would need to be 875 A per phase. If the distribution line voltage is 34.5 kV, then the maximum positive-sequence line impedance is:

$$|ZL1_{MAX}| = \left(\frac{34{,}500\text{V}}{\sqrt{3}}\right) \Big/ 875\text{A} - 1\Omega = 21.75\Omega \qquad \text{Equation 5.7}$$

where the one ohm accounts for the source impedance

Since the positive-sequence impedance is 0.466 ohms per mile, the maximum line length is 46.7 miles. It is clear from this exercise that the higher the maximum source impedance, the shorter the line that can be reliably protected using a single time-overcurrent relay. The condition on the relay pickup setting is that it must satisfy Equation 5.1 and Equation 5.2 for the maximum impedance between the source and the fault. If the relay is to provide backup protection for the fused lines, then this includes the maximum of those impedances.

The relay time must be coordinated with the fuse such that the fuse will open before the relay trips. If we assume that the coordination must work for single fault scenarios, then the only time coordination constraint is that the relay operate time must be longer than the fuse operate time when the fault current through the relay is maximum and the fuse fault current is minimum. This will occur when the load is at a maximum and the fault is at the end of the highest impedance line.

Continuing on with the previous example, assume that the line from fuse F4 to the load meets the above criteria. The line voltage profile between the tap at fuse F4 and the source follows that shown in Figure 5.26 provided that the load current is independent of voltage. The fuse fault current is the voltage at fuse F4 divided by the impedance to the fault. The relay current is the sum of all load currents not connected to the faulted line (F4) plus the fault current.

Voltage Drop Equation	Value	Number
$V_{BUS-S} = Vs/\sqrt{3} - (I_{F4} + I_{L1} + I_{L2} + I_{L3} + I_{L5})Zs$	18.75KV	Equation 5.8
$V_{F1} = V_{BUS-S} - (I_{F4} + I_{L1} + I_{L2} + I_{L3} + I_{L5})ZL1_{BUS-S\,to\,F1}$	14.55KV	Equation 5.9
$V_{F2} = V_{F1} - (I_{F4} + I_{L2} + I_{L3} + I_{L5})ZL1_{F1\,to\,F2}$	10.72KV	Equation 5.10
$V_{F3} = V_{F2} - (I_{F4} + I_{L3} + I_{L5})ZL1_{F2\,to\,F3}$	6.97KV	Equation 5.11
$V_{F4} = V_{F3} - (I_{F4} + I_{L5})ZL1_{F3\,to\,F4}$	3.40KV	Equation 5.12
$I_{F4} = V_{F4}/ZL_{F4}$	973A	Equation 5.13
$I_{RELAY} = I_{F4} + I_{L1} + I_{L2} + I_{L3} + I_{L5}$	1173A	Equation 5.14

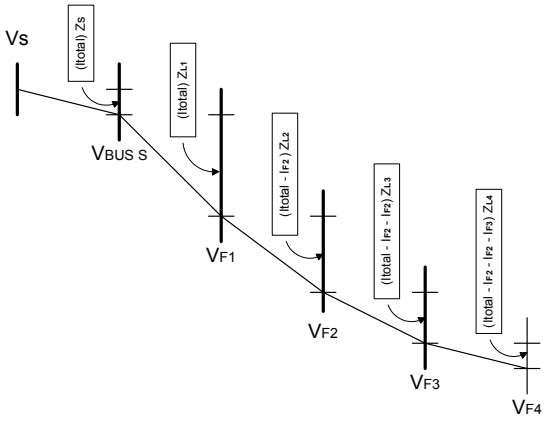


Figure 5.26: Voltage Profile for Three-Phase Fault on the Line Between F4 and F4 Load

TWO-TERMINAL LINE PROTECTION

The two-source line shown in Figure 5.27 most likely represents a single three-phase line between two substations. The radial line is a subset of this case generated by a disconnected source at Bus R and hence the protection of lines with sources at both ends must be operational for source *Er* in and out. Since the source, *Es*, and impedance, *ZS*, represent the equivalent of the power system behind the relay at Bus S, directional elements are required for overcurrent relays. The biggest concern for two-sourced lines is the effect on relay reach caused by infeed from the remote bus with non-zero fault resistance. Although the greatest effect is on ground relaying because of the propensity for high ground resistance, phase relaying can also be affected if the fault resistance is appreciable. Infeed is only a problem when the remote source is connected and the fault resistance is non-zero. Unfortunately, the probability of fault resistance is high.

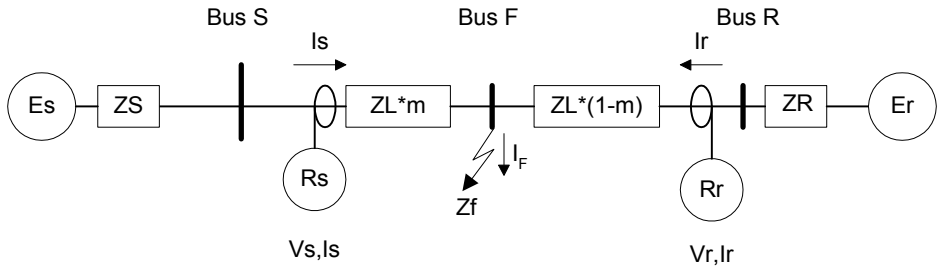


Figure 5.27: Two-Source Single-Line Diagram

Overcurrent Relaying

Time Overcurrent Relaying - I^2t (51)

The relay at Bus S must be coordinated with relays behind bus R as discussed earlier. For faults close to Bus R, the relay at Bus S has slower clearing times. The converse is true for the relay at Bus R when faults are close to Bus S. From a protection perspective, it is desirable for all faults to be cleared as quickly as possible without increasing the chances of tripping for out-of-section faults. Starting with A-phase-to-ground fault loop Equation 4.72, the remote infeed is included by letting I_F be the sum of the contributions from both sources as shown in Equation 5.15. Solving for Is_A, which is the measured current at Bus S, we can perform some simple sensitivity analysis. The first term on the right side of Equation 5.16 voltage derived current including the zero sequence compensation. The multiplier of this term is a scale factor that decreases the apparent fault current. This scale factor tends towards unity as R_F approaches zero, which is to be expected. It also shows that R_F has more effect the closer the fault is to Bus S, making the value of m small. The second term in Equation 5.16 is an error term involving both R_F and the infeed current from the remote end. This term also goes to zero as R_F tends towards zero as well as when Ir_A goes to zero.

$$Vs_A = mZL_1\left(Is_A + k_0\, Isr\right) + I_F R_F, \text{where} I_F = Is_A + Ir_A \qquad \text{Equation 5.15}$$

$$Is_A = \left[\frac{Vs_A}{m \cdot ZL_1} - k_0\, Isr\right] \cdot \left[\frac{1}{1+\left(\frac{R_F}{m \cdot ZL_1}\right)}\right] + \frac{Ir_A\, R_F}{m \cdot ZL_1 + R_F} \qquad \text{Equation 5.16}$$

Distance Relaying of Two-Source Lines

As discussed in previous sections, fault resistance and load current can affect the results of apparent impedance computations. As stated in section 0 on radial lines, mho elements are good for long lines but have poor resistive reach for short or low impedance lines.

Special Cases

Open Conductor

Not every power system line fault involves shorted or grounded conductors. A fault can also result when a two-source system such as that shown in Figure 5.27 has an open conductor. In this case, positive-sequence power can no longer be delivered to the load or transferred across the line. If, however, single-pole tripping is used, either the protection of open conductor should not be used or it should be disabled while in a single-pole open condition. The latter is possible with computer-based relays.

The symmetrical component diagram for this case is shown in **Error! Reference source not found.** of Appendix 11.12.2.5. Conventional overcurrent or distance relaying will not detect open-conductor faults as there is no fault current to start the relays. It is possible to protect for open conductors using negative sequence directional comparison with POTT pilot relaying. (See section 4.1.2.2 for additional information.) The negative sequence directional relay at Bus S sees the fault forward because the negative sequence current is out of the line as shown in **Error! Reference source not found.** but the voltage has the opposite direction to that shown in **Error! Reference source not found.**. The V2 and I2 phase relationship is shown in Figure 5.28. Since the current leads the voltage at both Bus S and Bus R, the fault is declared forward by both relays and the POTT scheme will cause a three-pole trip.

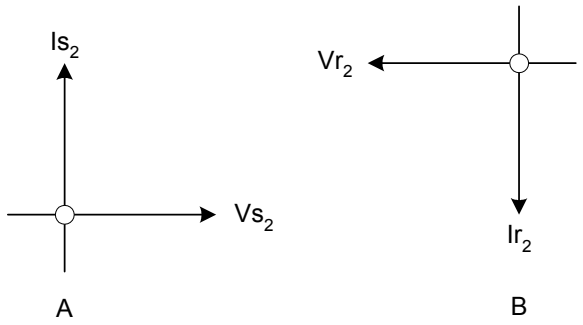


Figure 5.28: Negative-Sequence Voltage and Current Phase Relationship at (A.) Bus S and (B.) Bus R for Phase-A Open

Tapped Loads

Tapped loads are an inexpensive solution that complicates relaying and results in less than optimal relay performance. At best, relaying tapped lines is a compromise of poor options. Optimally, the line from Bus S to Bus R shown in Figure 5.29 would be split into two lines that terminate at Bus T. But such a solution is not always economically feasible because that requires an additional breaker and the construction of a second transmission line from Bus S to the tap.

When contemplating tapped loads, consider adding another source at the load bus. For this case, refer to 0.

Consider setting the Zone 1 ground distance reach from the relay at Bus S. Ideally, the reach should be 80 to 85 percent of the distance to Bus R and all the way to Bus T. If the relay at Bus S or R is set to be too sensitive, the relays will look past Bus T, past the transformer, and deep into the load that the transformer feeds. This can cause the relays at Bus S and R to operate for faults deep inside the customer's premises, which is highly undesirable.

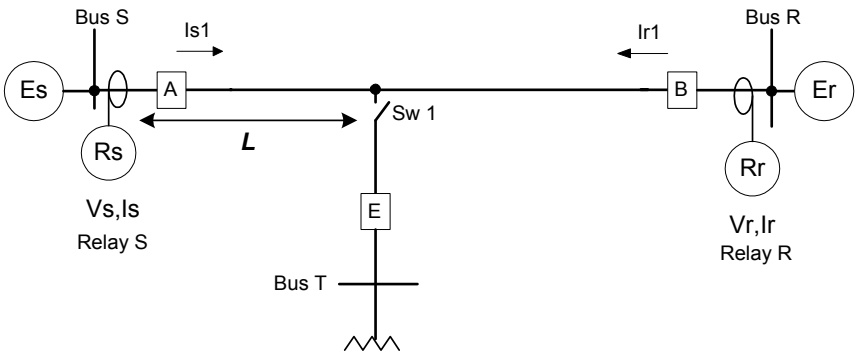


Figure 5.29: Single-Line Tapped Load

The Zone 2 elements for Relays A and B must both be able to see Bus T. In order to provide backup protection to the other source bus (Bus S or R in this example), each relay must also be able to see beyond the other source bus.

If the distance to the tap, which is shown as *L* in Figure 5.29 is too short, then it is not possible for the Zone 1 element to not reach into the load at Bus T. **DR suggestion**: **then the Zone 1 element is forced to reach into the load at Bus T.** In this case, an engineering decision is required. Either the Relay A zone will be permitted to reach into the Bus T load or it can be disabled altogether. In the event the first option is chosen, then Relay B is expected to be coordinated so that the Bus T remains energized while the customer's protection clears the fault or Relay B eventually trips out on Zone 2.

Depending on the transformer connection at Bus T, another problem can arise. Whether the relaying is overcurrent with the pickup based on Equation 5.16 or distance relaying based on Equation 4.58, resulting in Equation 5.17 for ground faults, the k_0 factor affects the results. As a rule of thumb, the ratio of ZL_0 to ZL_1 for transmission lines is three to one, resulting in k_0 of 0.67. If the transformer at Bus T is a grounded wye-grounded wye-delta bank, the transformer zero-sequence and positive-sequence impedance is equal. This makes k_0 for faults past the relay zero. The net effect is that the relays at Bus S and Bus R will underreach for all faults. This is undesirable for internal faults as well as external faults where A and B relays are expected to provide backup. transformer to be disconnected and Zone 2 to be able to look through the transformer for backup protection.

$$T = \mathrm{Re}\left[\left(m \cdot ZL_1 \cdot \left(I_\phi + k_0 \cdot I_{RES}\right) - V\right) \cdot \overline{Vpol}\right] \qquad \text{Equation 5.17}$$

Communications

As discussed in section 0 a POTT scheme needs communications to detect open conductors. System problems with tapped loads, discussed in 0, are exacerbated when the tap can be readily moved as shown in Figure 5.30. Since the optimal relay setting change depends on how the tap is connected, the relay setting must be changed to accommodate the network configuration. Microprocessor-based relays can be set with multiple group settings that can be remotely selected. This must be accomplished by an intentional operation by a responsible person or the changing of the group settings can be automated if communications is available from the tap to indicate which, if any, of the two switches is closed.

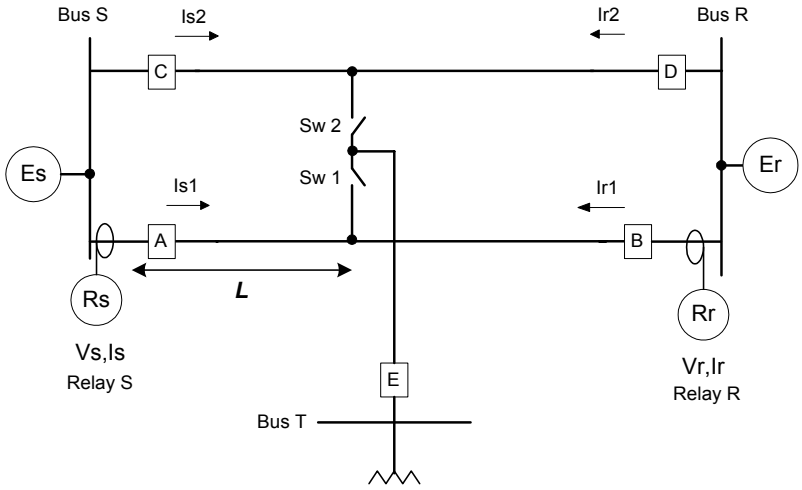


Figure 5.30: Parallel Lines With Tapped Loads

Another way of using communications to improve relay performance for tapped loads is to send a blocking signal from Bus T if faults are to be cleared by breaker E. Such a scheme is called DCUB and is described in 4.1.2.2.2.

THREE-TERMINAL LINE PROTECTION

Three-terminal lines are tapped two-terminal lines with an additional source. Any three-terminal line can degenerate into a two-terminal line and the relaying scheme must be capable of operating with one or two sources disconnected. If two sources are removed, then the three-terminal becomes a tapped radial line.

Special Cases????

Communication????

PROTECTION OF PARALLEL LINES

Zero-Sequence Mutual Coupling

Zero-sequence mutual coupling between parallel circuits can cause a ground distance relay to overreach or underreach. Zero-sequence overcurrent elements are also affected by zero-sequence mutual coupling. Numerous papers have been written that discuss the effects of zero-sequence mutual coupling on ground distance relays and others discuss the options available to address the problems associated with mutual coupling????. The intent of this text is to provide the protection engineer with the tools necessary to recognize that zero-sequence mutual coupling exists and to what extent the ground-fault protection is affected.

Effect of Zero-Sequence Mutual Coupling on Ground Distance Elements

If the transmission lines are relatively close to each other, some zero-sequence mutual coupling exists. The magnitude of the zero-sequence mutual coupling is a function of the spacing of the transmission lines and the voltage at which the lines are operating.

The ground distance measurement can appear to be greater than or less than the true distance to fault impedance when there is zero-sequence mutual coupling. Zero-sequence mutual coupling causes an increase or a decrease in the voltage and current measured at the relay that affects the ground distance measurement.

Figure 5.31 represents a system with parallel lines that are mutually coupled. For faults at the remote bus (Bus R), the ground distance elements underreach. Underreaching means that the impedance measured by the relay is greater than the actual distance-to-fault impedance. When a distance element underreaches, Zone 2 elements that are set to overreach the remote bus may not operate for faults at the remote end of the line. Failure of the Zone 2 element to operate can result in failure to trip or delayed tripping at one end of the line.

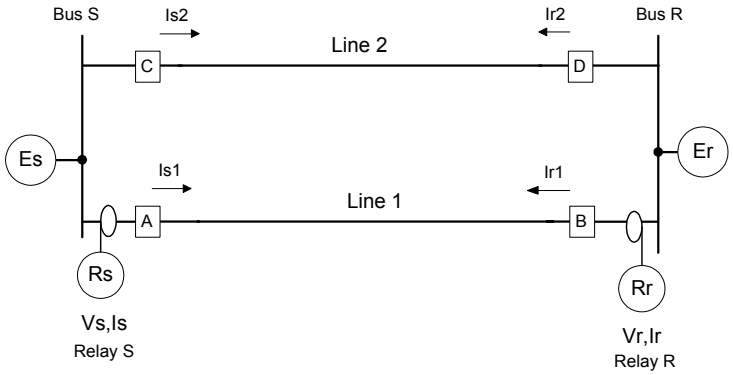


Figure 5.31: Single-Line Diagram Representing a Power System With Parallel Lines That Have Mutual Coupling

Ground distance relays can also overreach under certain conditions. Overreaching means that the measured impedance is less than the distance-to-fault impedance. Measuring line impedance less than the real distance to fault impedance can cause incorrect operation of underreaching Zone 1 relays.

As shown in Figure 5.31, a Zone 1 distance element can overreach if the parallel line is removed from service and grounded at both ends, and there is a close-in external ground fault. A ground distance relay can also overreach in cases where the zero-sequence current in the unfaulted line is a large percentage of the zero-sequence current in the faulted line. In both cases, the zero-sequence mutual coupling effect causes an increase in the current on the unfaulted line that results in Zone 1 overreach. Reference [41] provides methods for determining the amount of overreach for the conditions discussed in this paragraph.

Ground Distance Element Measurement Error Caused by Mutual Coupling

Reference [41] develops a method to determine the apparent impedance seen by a ground distance relay for a fault at the remote end of two parallel lines. Equation 5.18 can be used for setting overreaching Zone 2 distance elements. The extended reach required to accommodate mutual coupling may cause coordination problems with downstream time-delayed tripping relays when the parallel line is removed from service. However, if the distance element is used exclusively in a pilot protection scheme, there are no coordination concerns.

$$\frac{Z_{APP}}{Z_{L1}} = 1 + \frac{Z_{0M}/Z_{L1}}{[2K1/K0]} + p \quad \text{where}$$

Z_{APP} = apparent loop impedance

ZL_1 = positive − sequence line impedance

$K1 = I1_{RELAY}/I1_{FAULF}$

$K0 = I0_{RELAY}/I0_{FAULF}$

$p = ZL_0 / ZL_1$

Equation 5.18

The method described in Reference [3] works correctly and reliably for lines that are terminated at common buses and coupled with only one other circuit. When the lines are not terminated at common buses or the line is coupled with more than one circuit, use an apparent impedance calculation. Use Equation 5.19 to calculate the apparent impedance.

$$Z_{APP} = \frac{V\phi}{I\phi + k_0 \cdot Ir}$$

where

$V\phi$ = faulted phase voltage by the relay

$I\phi$ = faulted phase voltage by the relay

$Ir = Ia + Ib + Ic$ measured at the relay

$k_0 = (ZL_0 - ZL_1)/(3 \cdot ZL_1)$

Equation 5.19

The underreaching effect caused by zero-sequence mutual coupling can also be corrected by adjusting the zero-sequence compensation factor used for the overreaching distance elements. Many relays offered today allow separate zero-sequence compensation factor settings for the underreaching and overreaching distance zones. Calculate the overreaching zero-sequence compensation factor to accommodate mutual coupling as follows:

$$K_{0M} = \frac{ZL_0 - ZL_1 - Z_{0M}}{3 \cdot ZL_1}$$

where

ZL_0 = zero – sequence line impedance

ZL_1 = positive – sequence line impedance

Z_{0M} = zero – sequence mutual coupling impedance

Equation 5.20

Using Equation 5.20 for the ground distance calculation compensates the distance element reach such that faults at the end of the line are measured correctly (i.e., they represent the true line impedance). However, be cautious in using this method for correcting ground distance element underreach. When the parallel line is removed from service the ground distance element is over-compensated and can severely overreach the remote terminal.

The Effect of Zero-Sequence Mutual Coupling on Ground Overcurrent Elements

Zero-sequence mutual coupling also affects the performance of ground overcurrent elements that use zero-sequence current as an operating quantity. Mutual coupling can reduce the sensitivity of zero-sequence overcurrent elements in detecting faults at the remote end of the line.

Mutual coupling of the two circuits reduces the zero-sequence current in each line for remote faults. Faults at the remote end of the line are the worst case because this is where the effect is maximized.

Zero-sequence overcurrent elements can also overreach for sequentially cleared out-of-section faults. As illustrated in Figure 5.31, a phase-to-ground fault close to Breaker C will be cleared first by Breaker C and then by Breaker D. Once Breaker C opens, the zero-sequence mutual coupling between the two circuits causes an increase in the zero-sequence current flowing in the unfaulted line (Line A-B). Setting the direct tripping zero-sequence overcurrent elements above the maximum out-of-section fault current quantity (caused by mutual coupling) compensates for the increase in zero-sequence current flowing in the unfaulted line.

High-Resistance Fault Coverage and Remote Infeed

The amount of resistive fault coverage by any relay is influenced by a number of factors:

- Distance element reach
- Directional sensitivity
- Remote infeed and, thus, the source impedance behind the relay location
- Line length
- Normal system unbalance
- Load flow (in some distance relay designs)

References [80 and 41] ????discuss resistive fault coverage with respect to directional element sensitivity and pilot scheme selection. The two referenced papers show resistive fault coverage for a simple two-ended system with a single line. The system shown in Figure 5.27 is representative of the systems used for study in these two papers.

In Reference [80], the authors show how directional element sensitivity affects the ability of the relay to detect high-resistance faults and how to determine how much resistive fault coverage a particular directional element provides. The paper discusses current and voltage transformer accuracy and performance and how these devices can have a significant impact on directional element performance, especially for high-resistive faults. And finally, the paper explains how system unbalance, due primarily to the line conductor configuration and spacing, can have adverse affects on directional elements for faults other than ground faults (in particular, three-phase faults).

In Reference [41], the various pilot schemes are discussed and a method is presented for measuring the performance of these schemes. One of the measures of performance stated in the paper is how well the pilot scheme detects high-resistance faults. The evaluation is based on using directional ground overcurrent relays for high-resistance fault coverage in a pilot scheme and a channel-independent distance element. Plots are provided showing high-resistive fault coverage for a particular system with respect to the fault location on the line.

References [80 and 41] are excellent guides for evaluating directional element, distance element, and pilot scheme performance. The papers also provide detailed information concerning the limits of each element on a simple two-ended system.

The following discussion will focus on the distance and directional element performance on the example system shown in Figure 5.31. The plots provided demonstrate high-resistance fault coverage with respect to fault location and element type.

Directional Overcurrent and Distance Element Performance for High-Resistance Faults

Use the parameters listed in Table 5.6 to evaluate the directional and distance element fault-resistance coverage for the long line and short line system models shown in Figure 5.31. In both cases only the fault resistance coverage for ground faults is considered. The settings listed in Table 5.7 are used for distance elements, ground overcurrent elements, and negative-sequence elements. All settings are in secondary quantities.

Table 5.6: Line Parameters for Long and Short Line Examples

Long Line System Parameters	Short Line System Parameters
$Z_{1s} = 2\ \angle 88°\Omega$, $Z_{0s} = 2\ \angle 88°\Omega$	$Z_{1s} = 2\angle 88°\Omega$, $Z_{0s} = 2\ \angle 88°\Omega$
$ZL_1 = ZL_2 = 8\ \angle 84°\Omega$	$ZL_1 = ZL_2 = 0.5\ \angle 84°\Omega$
$ZL_0 = 24\ \angle 80°\Omega$	$ZL_0 = 1.5\ \angle 80°\Omega$

$ZL_{0M} = 16 \angle 78° \Omega$	$ZL_{0M} = 1 \angle 78° \Omega$
$Z_{1s} = 2 \angle 88° \Omega$, $Z_{0s} = 2 \angle 88° \Omega$	$Z_{1s} = 2 \angle 88° \Omega$, $Z_{0s} = 2 \angle 88° \Omega$

Table 5.7: Relay Settings Used in Overcurrent and Distance Element Performance Analysis in the Presence of High-Resistance Faults

*************NEED???? **********HEADING**************************	**NEED???? HEADING**************
Zero-Sequence Directional Overcurrent (67N)	0.5 amp (I_r current)
Negative-Sequence Directional Overcurrent (67Q)	0.5 amp ($3 \cdot I_2$ current)
Mho Ground Distance (21G)	$2 \cdot Z_{1L1}$ ohms
Quadrilateral Ground Distance (21X)	$2 \cdot Z_{1L1}$ ohms, reactance reach
Quadrilateral Ground Distance (21X)	50 ohms, resistance reach

THIS PARAGRAPH SEEMS CONFUSING, UNCLEAR:

The sensitivity of the directional overcurrent elements is limited by the specified pickup value, not the directional element operation. The operation of the ground distance elements is limited by the impedance settings, not the supervisory elements used with the distance elements. The quadrilateral reactance element is assumed to be corrected for system nonhomogeneity caused by a fault at the remote end of the line.

Figure 5.32 shows the resistive fault coverage using ground overcurrent and negative-sequence overcurrent elements on a long line. As the fault location moves away from the bus, the amount of fault resistance detected by the zero-sequence overcurrent element (67N) decreases, while the amount detected by negative-sequence overcurrent element (67Q) increases. The change in fault resistance coverage is caused by mutual coupling and differences in the line zero- and negative-sequence impedances [32]. Figure 5.32 shows the resistive fault coverage using mho and quadrilateral ground distance elements on a long line.

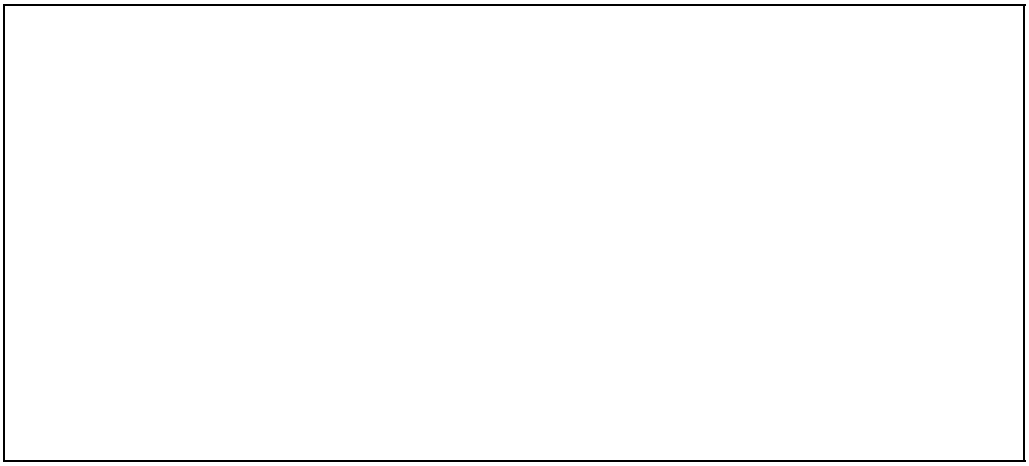


Figure 5.32: Long Line High Fault Resistance Detection Using 67N and 67Q Elements

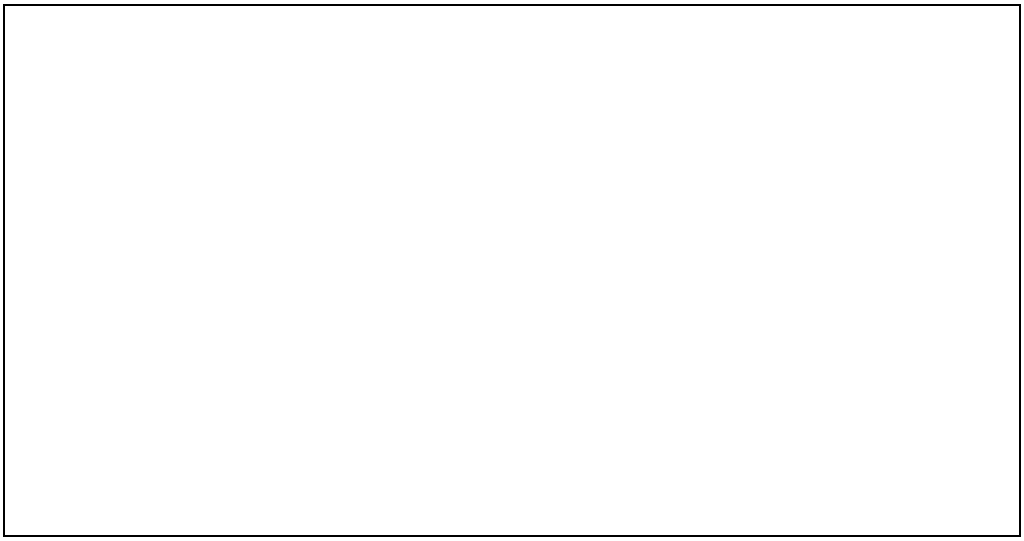


Figure 5.33: Long Line High Fault Resistance Detection Using 21G and 21X Elements

Figure 5.34 provides a comparison of the resistive fault coverage using only ground distance or ground overcurrent functions on a long line. In Figure 5.34 the ground distance and overcurrent functions are applied in a pilot scheme. The pilot scheme selected for the plot shown in Figure 5.34 is the pilot scheme developed in Reference [41]. This reference also provides additional information on pilot scheme comparisons with respect to fault-resistance coverage????.

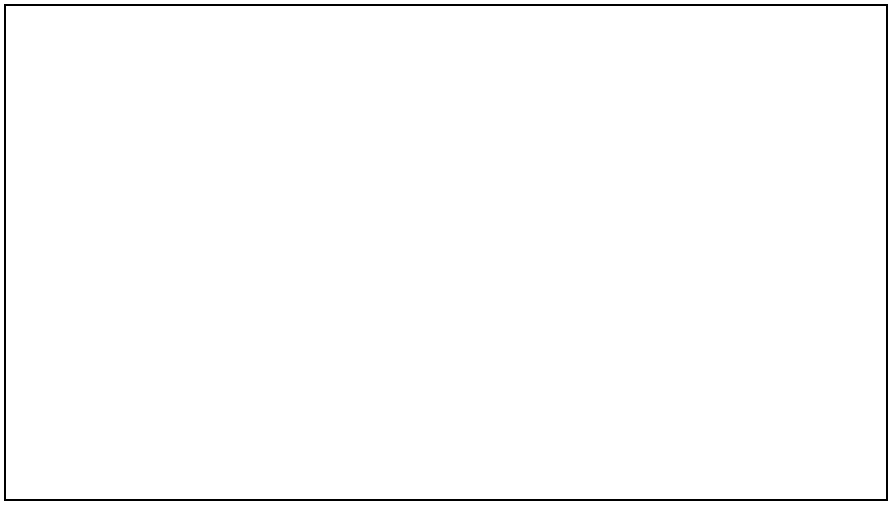


Figure 5.34: Long Line High Fault Resistance Detection 21 Versus 67 Elements

Figure 5.35 shows the resistive fault coverage using ground overcurrent and negative-sequence overcurrent elements for the short line case listed in Table 5.6. As in the long line fault coverage, when the fault location moves away from the bus, the zero-sequence sensitivity decreases and the negative-sequence sensitivity increases. Figure 5.36 shows the resistive fault coverage using mho and quadrilateral ground distance elements on a short line.

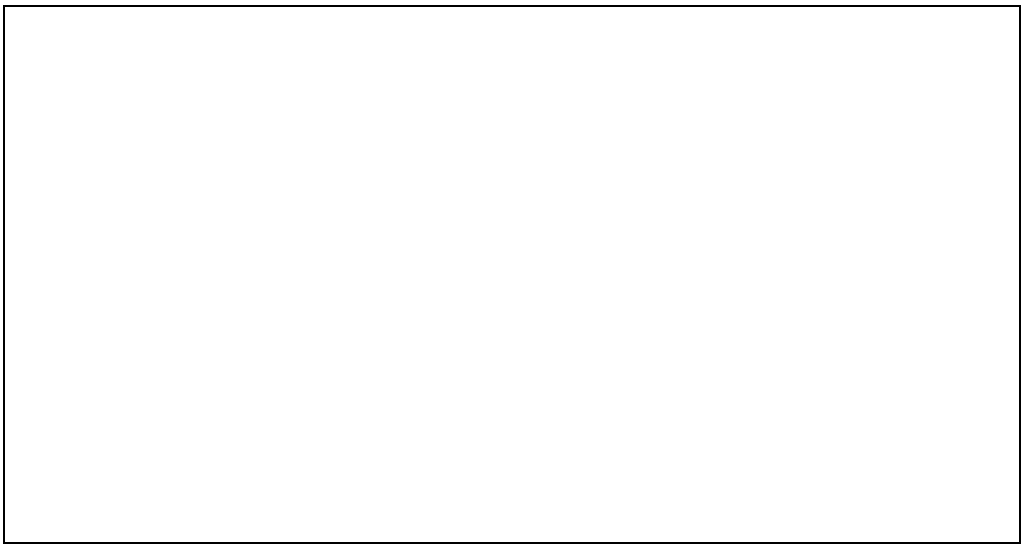


Figure 5.35: Short Line High Fault Resistance Detection Using 67N and 67Q Elements

Figure 5.36: Short Line High Fault Resistance Detection Using 21G and 21X Elements

Figure 5.37 allows the comparison of the resistive fault coverage using only ground distance or ground overcurrent functions on a short line. In Figure 18 the ground distance and overcurrent functions are applied in a pilot scheme. The pilot scheme selected for the plot shown in Figure 5.37 is a new pilot scheme developed in Reference???? [70].

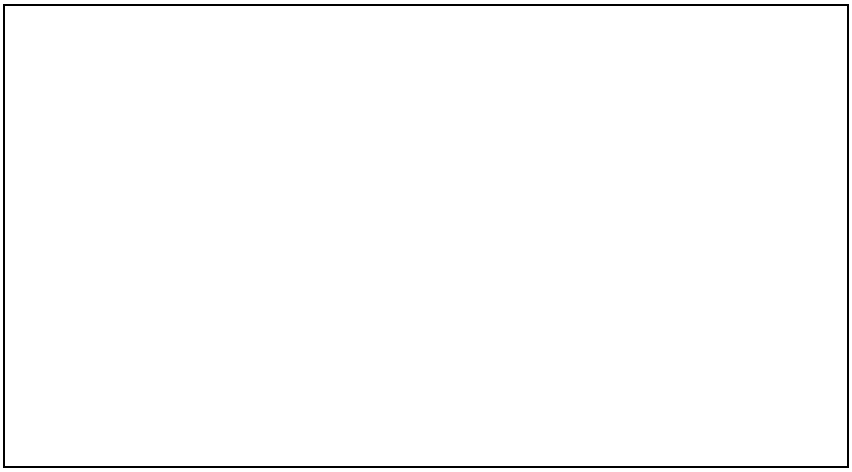


Figure 5.37: Short Line High Fault Resistance Detection 21 Versus 67 Elements

Figure 5.32, Figure 5.34, Figure 5.35, and Figure 5.36 show that as the fault moves away from the bus, the amount of fault resistance detected by the overcurrent and distance elements decreases. Current infeed from the other line terminal causes this decrease because current infeed from the other terminal acts as a fault resistance

amplifier. As the fault gets closer to the remote terminal, the amount of current contributed from the terminal nearest to the fault constitutes a greater portion of the total fault current. The terminal furthest away from the fault contributes a very small portion of the total fault current.

Dividing the total current in the fault by the current measured in the relay can approximate the measured fault resistance. To approximate the measured fault resistance for a remote fault (where the amplification for the fault resistance is at its greatest), apply a bolted fault at the remote bus and take the ratio of the total fault current to the fault current measured at the relay. Use the same currents in the ratio calculation as those the relay uses in the distance relay resistive measurement. Multiply the current ratio by the fault resistance value to evaluate the ability of the distance relay to detect the remote, high-resistance fault.

Reference???? [80] shows how to calculate the maximum fault resistance detected by a zero- or negative-sequence overcurrent element based upon the element setting.

System Unbalances Caused by Line Configuration or In-Line Load Switching

System unbalances caused by line configuration, in-line load switching, or unbalanced loads can affect the sensitivity of zero- and negative-sequence overcurrent elements. Ground distance elements are relatively immune to system unbalances, primarily because they cannot be set as sensitively as overcurrent elements.

????Roberts et. al. discuss in detail the limits of directional element performance for high-resistance faults, instrument transformer error, and transmission line configuration.[80] In this reference, Roberts also presents a method to determine the maximum resistive fault coverage based on directional element operating parameters and system impedances.

The pickup threshold for fault detecting elements should always be set greater than the normal unbalance on the power system. Given that high-resistance faults generate very low operating voltages and currents, any load-generated system unbalance can affect the sensitivity of a ground-fault detecting element, in particular, zero-sequence and negative-sequence elements. Setting these elements too sensitively can result in unwanted operations.

Load or in-line switching also generates system unbalances. Switching via a circuit breaker does not have a significant impact on sensitive fault-detecting elements because the breaker poles all open at nearly the same time. However, when load-break switches are used for switching, there could be a number of cycles between each phase interruption. This means that while the load-break switch is opening, unbalances are generated that could cause directional and overcurrent element operation. If no corrective action is taken, the relay scheme may misoperate and trip during the switching operation.

Open phase conductors also generate system unbalances and can be treated the same as in-line switching. For this case, assume that the conductor has opened, but has not made contact with ground. Appendix 11.12.2 provides details on the sequence networks for in-line load switching and open conductors.

SELECTING THE BEST GROUND-FAULT DETECTING ELEMENT

The data presented in this text and published in previous papers [2, 6, 11, 13] ???? clearly show that using zero-sequence and negative-sequence overcurrent elements in a pilot scheme provides the best protection with respect to security, dependability, and sensitivity (high-resistance fault coverage).

Using a combination of zero- and negative-sequence overcurrent elements provides the maximum fault resistance coverage for long or short lines, with and without mutual coupling. Zero- and negative-sequence overcurrent elements are likewise fairly immune to load flow and system nonhomogeneity. However, the sensitivity of zero- and negative-sequence overcurrent elements can be affected by system unbalance and in-line load switching as previously described.

Distance elements provide fair fault resistance coverage and are more tolerant to system unbalance and in-line load switching. However, mho elements provide little or no fault resistance coverage and can also be adversely affected by zero-sequence mutual coupling. The quadrilateral distance elements, while providing better fault resistance coverage than mho elements, are also affected by zero-sequence mutual coupling.

Quadrilateral distance elements are extremely sensitive to system nonhomogeneity if corrective measures are not taken. One relay has improved the quadrilateral reactance element design against overreaching caused by system nonhomogeneity. The improved design is compensating the polarizing reference based upon the system and not a factory-fixed correction factor.

The following tables highlight the benefits and application for each of the ground-fault detecting elements discussed in this paper. Table 5.8 compares the performance of the ground-fault detecting elements for specific applications. Table 5.9 should be used as a guide for selecting ground-fault detecting elements.

Table 5.8: Application Performance of Ground-Fault Detecting Elements

PERFORMANCE IN SPECIFIC APPLICATIONS	67N	67Q	21X	21G
Short Line Applications	☆☆☆	☆☆☆	☆	☆
Long Line Applications	☆☆☆	☆☆☆	+	☆
Parallel Line Applications	☆	☆☆☆	+	+
Channel Independent Direct Tripping - Instantaneous	☆	☆	☆☆☆	☆☆☆
Channel Independent Direct Tripping - Time Delay	☆	☆	☆☆☆	☆☆☆
Pilot Scheme	☆☆☆	☆☆☆	☆	☆

☆☆☆ = best selection
☆ = satisfactory
\+ = satisfactory but requires further study

67N = directional zero-sequence overcurrent element
67Q = directional negative-sequence overcurrent element

PERFORMANCE IN SPECIFIC APPLICATIONS	67N	67Q	21X	21G
21X = quadrilateral ground distance element 21G = mho ground distance element				

Table 5.9: Ground-Fault Detection Element Selection Guide????

PERFORMANCE IN THE PRESENCE OF:	67N	67Q	21X	21G
System nonhomogeneity *{pages 11-15}*	☆☆☆	☆☆☆	+	☆
High Fault Resistance (R_F) *{pages 18-23}*	☆☆☆	☆☆☆	☆	-
Strong Source *{pages 18-20}*	☆☆☆	☆☆☆	☆	☆
Weak Source *{pages 21-23}*	☆	☆	☆	☆
Zero-Sequence Mutual Coupling *{pages 15-17}*	☆	☆☆☆	+	+
Load Flow *{references 9,15}*	☆☆☆	☆☆☆	+	☆☆☆
In-Line Load Switching *{Appendix A}*	+	+	☆☆☆	☆☆☆
Nontransposed Transmission Lines *{reference 3}*	☆	+	☆☆☆	☆☆☆
Unbalanced Loading	☆	+	☆☆☆	☆☆☆

☆☆☆ = best selection
☆ = satisfactory
\+ = satisfactory but requires further study
\- = unsatisfactory

67N = directional zero-sequence overcurrent element
67Q = directional negative-sequence overcurrent element
21X = quadrilateral ground distance element
21G = mho ground distance element

Reference [15] provides one utility's perspective on selecting ground fault???? protection. The author states that the preferred method is ground overcurrent elements because they are simple and reliable. When the polarizing quantities available are inadequate for reliable relay operation, then ground distance is used. In addition, guidelines for determining adequate polarizing quantities are shown.

The ground fault protection selection criteria outlined in Reference [15] are valid for relays using directional elements that use conventional torque calculations. References [6, 9, and 14] show an improved directional element design using an impedance-based directional element. The impedance-based element design overcomes the limitations of conventional torque elements and expands the application of zero- and negative-sequence overcurrent elements.

SETTING GROUND FAULT DETECTING ELEMENTS

Direct-Tripping Overcurrent Elements (Instantaneous Elements)

Setting direct-tripping zero-sequence overcurrent elements

Set direct-tripping zero-sequence overcurrent elements greater than the maximum out-of-section fault current. In circumstances where the line is mutually coupled with other transmission lines, the maximum zero-sequence current may be for a fault at the end of a parallel line with the breaker closest to the fault open (sometimes referred to as end-of-line faults). The end-of-line fault current could result in the maximum external fault current because the mutual coupling between circuits is at its maximum. If the line is not mutually coupled, the maximum fault current is typically for faults at the remote bus.

Setting direct-tripping negative-sequence overcurrent elements

Set direct-tripping negative-sequence overcurrent elements greater than the maximum out-of-section fault current considering both phase and ground faults. Negative-sequence current is generated for all unbalanced faults. Zero-sequence mutual coupling does not affect the negative-sequence overcurrent element, so do not consider end-of-line faults. Evaluate the maximum out-of-section fault current for phase faults as well as ground faults, since negative-sequence current is generated for all unbalanced faults. Carefully evaluate the negative-sequence overcurrent element setting parameters since they may be in terms of I_2 or $3I_2$ current.

Setting direct-tripping elements

Use Equation 5.21 to set the direct-tripping element greater than the maximum external fault current plus some margin. Determine the margin based on the steady-state and transient overreach error of the protective relay, information that is available in the protective relay support documentation or through the relay manufacturer. The setting should include additional margin to account for fault study, line modeling, and current transformer errors (5 to 10 percent is usually adequate).

$$\text{Pickup} = I_F = \left(1 + \frac{\varepsilon_{SS}}{100} + \frac{\varepsilon_T}{100} + 0.05\right) \qquad \text{Equation 5.21}$$

where
I_F = maximum external fault current
ε_{SS} = percent steady-state error
ε_R = percent transient error
0.05 = additional margin for modeling and CT errors

Direct-Tripping Distance Elements (Zone 1)

Setting

Set direct-tripping distance elements to underreach faults at the remote bus, considering the steady-state and transient reach errors of the relay. Generally, you should also set direct-tripping distance elements based on the true line impedance, but without considering mutual coupling effects and remote infeed.

Consider capacitive voltage transformer (CVT) transient errors while determining the reach setting for direct-tripping distance elements. Capacitive voltage transformers (CVTs), have a transient response that may cause a distance element to overreach [8]. The overreach error caused by the CVT transient response is a function of the source impedance ratio (SIR, which is the source impedance divided by the distance element setting or line impedance), CVT ferroresonance circuit design, and distance relay design. Reduce or time-delay the direct-tripping element reach to avoid operation on external faults. ????***Refer to the protective relay support documentation or contact the relay manufacturer for information on CVT transient response.***

Calculating the CVT overreach error

Step 1) Calculate the positive-sequence source impedance

Calculate the positive-sequence source impedance behind the relay. The positive-sequence source impedance can be calculated using a fault study. One approach is to determine a Thevenin equivalent of the system with respect to the buses. The source impedance can also be calculated by applying a three-phase bus fault, removing the current contribution from the subject line, and dividing the line-to-neutral nominal system voltage by the adjusted total fault current. Calculate the source impedance under the weakest source condition.

Step 2) Calculate the source to line impedance ratio

Calculate the source to line impedance ratio (SIR) by dividing the calculated source impedance by the line positive-sequence impedance.

Step 3) Estimate the reach reduction

From the SIR calculated in Step 2, estimate the reach reduction from data provided by the relay manufacturer. Reference [6] provides a graph for reducing the Zone 1 reach based upon the CVT design. The graph presented in Reference [6] applies to one relay design. Contact the specific relay manufacturer for information concerning CVT transient overreach.

Calculating direct-tripping mho ground distance element settings

Step 1) Determine the minimum line impedance to the next line section or bus.

Step 2) CVT Compensation

If CVTs are not used, go to Step 3, below. If CVTs are used, reduce the impedance obtained in Step 1,above, by the factor determined from the CVT overreach calculations.

Step 3) Set the reach using Equation 5.22:

$$Z_R = Z1_{MIN}\left(1-\frac{\varepsilon_{SS}}{100}-\frac{\varepsilon_T}{100}-0.05\right)$$

where Equation 5.22

Z_R = distance relay reach setting
$Z1_{MIN}$ = minimum impedance from Step 1 or Step 2
ε_{SS} = percent steady-state error
ε_R = percent transient error
0.05 = additional margin for modeling and CT errors

Calculating direct-tripping quadrilateral ground distance element settings

Step 1) Setting

Quadrilateral distance elements must be set considering unequal source and line impedance angles. Unequal source and line impedance angles can cause a reactance element to over- or underreach when fault resistance is present. Calculate the reactance element over- or underreach using Equation 4.82. The error term calculated in Equation 4.82 assumes a zero-sequence polarized reactance element. Consider the nonhomogeneous system error when setting underreaching quadrilateral distance elements to prevent overreaching on external, high-resistance faults.

Step 2) Zone 1 Reactance reach

Adjust the polarizing reference or reduce the Zone 1 reach to accommodate unequal source and line impedance angles. Adjusting the polarizing quantity is sometimes shown as tilting the reactance characteristic. While adjusting the characteristic by a fixed angle helps improve the overreach error, it does not improve the reactance element performance for all systems.

Providing a settable adjustment works very well for a particular fault location and system condition. Cases where the system source angle can dramatically change because of changing operating conditions require further study.

Calculate the adjustment angle using Equation 7 or 8 for a zero-sequence polarized reactance element.

Step 3) Zone 1 Resistance reach

Using an extended Zone 1 resistance reach is problematic because it increases the chance that resistive faults will cause the Zone 1 reactance element to overreach. As Equation 4.82 shows, increasing the amount of fault resistance detected by the Zone 1 element can increase the fault-resistance-induced error. Limit the resistive reach of

the Zone 1 element to reduce the chance that resistive faults and unequal source and line impedance angles will cause overreach.

Determine the fault resistance coverage required by the Zone 1 element from historical fault data or tower footing resistance, or by calculating the arc resistance. Some relay manufacturers provide guidelines on limiting the resistive reach as a function of the reactance setting. Consult these guidelines when determining the Zone 1 resistive reach setting.

Selecting an arbitrary resistive setting is also valid if the fault-resistance-induced error in the reactance measurement is carefully evaluated.

Calculating the reach setting for a direct-tripping quadrilateral ground distance element:

Step 1)

Determine the minimum line impedance to the next line section or bus.

Step 2)

If CVTs are not used, go to Step 3. If CVTs are used, reduce the impedance obtained in Step 1 by the factor determined from the CVT overreach calculations shown earlier.

Step 3)

Calculate the nonhomogeneity adjustment factor (this factor has magnitude and angle) using Equation 4.79 or Equation 4.80 by applying a fault at the remote bus under normal operating conditions (set the "m" value in Equation 4.79 to equal 1.0).

Step 4)

In a relay that allows a settable adjustment to the polarizing reference, use the angle obtained from the nonhomogeneity adjustment factor calculated in Step 3. Continue with Step 5 using the nonhomogeneity adjustment factor angle as the fixed polarizing reference angle. Evaluate various system conditions that result in a change in the nonhomogeneity angle. Then select the worst-case change in the nonhomogeneity angle and use it in the following steps.

Step 5)

In relays with a fixed polarizing reference adjustment, calculate the resistance error by subtracting the fixed reactance line tilt from the angle calculated in Step 3 or 4. Subtract a negative angle for a downward fixed tilt. Subtract a positive angle for an upward fixed tilt.

Step 6)

This step is a data gathering procedure to obtain the data required for Step 7. Apply a bolted single-phase-to-ground fault at the remote bus under normal operating conditions. Obtain the fault currents (phase and ground currents) from the fault study.

Use the angle calculated in Step 5 for the "*T*" variable. Use the magnitude of the adjustment factor calculated in Step 3 for the "*A*" variable. Use the selected resistance setting used for the Zone 1 quadrilateral element for the "R_F" variable.

Step 7)

Calculate the reactance error using the data obtained in Step 6 and Equation 4.82.

Step 8)

Subtract the reactance error obtained in Step 7 from the impedance calculated in Step 2. If the reactance error calculated in Step 7 is negative, the relay will overreach for resistive faults. If the error term calculated in Step 7 is positive, it can be ignored since it will cause the relay to underreach for resistive faults.

Step 9)

If the result of Step 8 is less than zero, the reactance reach setting cannot be reduced to accommodate the fault-resistance-induced error. The resistive reach setting must be reduced and a new reactance error must be calculated starting at Step 7 to obtain the new resistive reach setting.

Step 10)

Set the resistive reach to the value determined from Step 7 or 9, which ever is less or gives the least reactance reach error.

Step 11)

Set the reactance reach using Equation 5.23:

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where
Z_R = distance relay reach setting
$Z1_{MIN}$ = minimum impedance from Step 8)
ε_{SS} = percent steady-state error
ε_R = percent transient error
0.05 = additional margin for modeling and CT errors

Equation 5.23

Overreaching Overcurrent Elements

Setting sensitive tripping elements

Set sensitive tripping elements above normal system load unbalance or the unbalance caused by line asymmetry under balanced fault conditions. Overreaching current elements used in pilot protection schemes can be set to be very sensitive to detect high-resistance ground faults. However, to maintain scheme security, the sensitive elements should be set above normal load unbalance.

It is difficult to theoretically determine the normal system load unbalance on the power system. ***Reference???? [80] presents methods for determining the load generated zero- and negative-sequence current caused by line asymmetry.***

It is also possible to take measurements at the time of relay installation, but setting adjustments may be required in the field to decrease the sensitivity of overcurrent elements.

A limiting factor to ground fault detection is the directional element sensitivity. Evaluate the directional element sensitivity when determining the amount of fault resistance coverage required for a particular application.

There is no advantage to setting overcurrent tripping elements to be more sensitive than the directional element sensitivity. [80] In fact, setting the overcurrent element to low (i.e., very sensitive) may cause the relay to overtrip for external faults. Set directional element supervisory elements to maximize sensitivity, but not at less than the load unbalance caused by line asymmetry.

Directional element sensitivity in some designs can be controlled by ratios of sequence currents typically referred to as restraint factors. The ratio of the negative-sequence current magnitude to the positive-sequence current magnitude, referred to as the *a2* ratio factor, can control the operation of the directional element. If high-resistance ground coverage is not required, set *a2* to no less than 0.15.

Reference [80] ????shows a2 ratio factors for vertical and horizontal line construction with different conductor phasing. These figures illustrate that an a2 ratio factor of 0.1 is adequate for the majority of phasing configurations. However, line configuration should be evaluated to determine the actual a2 ratio factor.

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Determine the *a2* ratio factor by measuring the phase currents on the line and calculating the *a2* ratio factor under load conditions. Assume that the a2 ratio factor remains constant for maximum load values. The *a2* ratio factor can be determined from the line impedance data. If it is not convenient to calculate the line impedance or to calculate the a2 ratio factor from the line impedance data, then set the *a2* ratio factor to 0.1.

The tripping elements should be set to provide maximum fault resistance coverage as well as maximum security under external fault conditions. Set tripping elements to no less than 0.5 amps secondary unless further study is performed. The lower limit of 0.5 amps applies to both zero-sequence and negative-sequence overcurrent elements. Set zero-sequence overcurrent elements in terms of $3 \cdot I_0$ (I_r) and negative-sequence overcurrent elements in terms of $3 \cdot I_2$.

Overreaching Ground Distance Elements

When using ground distance elements exclusively in a pilot scheme, set them to minimize operating time.

Traditionally, overreaching Zone 2 elements are set from 120 percent to 150 percent of the protected line impedance. The same Zone 2 element that is used in the pilot

scheme is typically also used as a time-delayed backup element. Newer relay designs allow separately set Zone 2 pilot and Zone 2 backup elements. The pilot zone can be set from 300 percent to 500 percent of the line impedance without coordination concerns, thus minimizing the element operating time. The backup zone can be set to the more traditional reaches.

When using extended pilot zone reaches, set the relay load encroachment logic to avoid operation under heavy load conditions. Set overreaching time-delayed backup distance relays less than the next line section Zone 1 element.

Setting the overreaching time-delayed backup zone less than the next line section Zone 1 element ensures proper coordination. If a long line is terminated into a substation with short lines, the time-delayed element reach or coordination margin may have to be reduced.

When heavy mutual coupling is present, it may be necessary to set the ground distance relay from 200 percent to 300 percent of the positive-sequence line impedance to overreach the remote terminal.

For cases with heavy mutual coupling, using a ground distance relay as a dedicated pilot zone does not present a problem. However, if the ground distance element is used for time-delayed backup, explore other options.

Relays that offer separate zero-sequence compensation for the underreaching and overreaching zones can compensate such that the ground distance element measures the correct impedance for faults at the end of the line.

Adjusting the zero-sequence compensation to correct for the effects of mutual coupling only works well when the line is coupled with one other line and both ends of the lines are terminated at the same buses. The zero-sequence compensation must be changed when the parallel line is out-of-service. Relays with multiple setting groups work very well for this application. The relay can be wired to change setting groups when the parallel line is removed from service, using a breaker auxiliary contact from the parallel line. The zero-sequence compensation factor used for the alternate setting group should be set based on the line impedance only.

Calculating the reach setting

Calculate the reach setting for an overreaching ground distance element:

Step 1)

Determine the maximum positive-sequence line impedance to the next line section or bus without considering infeed or mutual coupling (i.e., actual line impedance values).

Step 2)

If the circuit is not mutually coupled, go to Step 4. If the circuit is mutually coupled with one other parallel line, calculate the apparent impedance seen for a bolted single phase-to-ground fault at the remote bus using Equation 5.18, otherwise go to Step 3.

Step 3)

If the circuit is mutually coupled with more than one line or the mutually coupled lines are not terminated at the same substations, calculate the apparent impedance for a bolted fault at the remote bus using Equation 5.19.

Step 4)

If the overreaching ground distance element is used exclusively as a pilot tripping zone, set reach from **three** to **five** times the impedance calculated in Step 1, 2, or 3. When using the extended reach setting, always set the relay load encroachment logic to avoid operation under load conditions.

Step 5)

If the overreaching ground distance element is used for time-delayed backup as well as pilot protection, set the reach from 120 to 150 percent of the impedance calculated in Step 1, 2, or 3.

Calculating the True Quadrilateral Fault Resistance Coverage

A quadrilateral distance element cannot detect the fault resistance specified by the resistive element reach setting because of current infeed into the fault resistance from the other line terminal.

The amount of fault resistance detected by a quadrilateral element is not necessarily the resistance element setting. On a radial system, the fault resistance measured by the quadrilateral resistance element is the actual fault resistance because the relay measures the only current contribution to the fault. On a looped system, two or more sources can supply current. Multiple sources supplying current into a high-resistance fault amplify the actual fault resistance.

To calculate the approximate fault resistance detected by the quadrilateral distance element:

Step 1)

Apply a bolted fault at the remote bus. The measured resistance is maximum for a remote fault.

Step 2)

Divide the total fault current by the fault current measured in the relay. In the ratio calculation use the same currents the relay uses in the resistive element measurement.

Step 3)

Divide the resistive element setting by the current ratio calculated in Step 2. The result is an approximation of the true fault resistance detected by the resistance element.

SPECIAL CASES

Single-Pole / Three-Pole Tripping

Single-pole tripping is used on selected transmission lines to improve system stability. It is based on the premise that 80 percent of line faults are transient single-line-to-ground faults. Permanent single-line-to-ground and phase faults still require three-pole tripping. To operate correctly, the breakers used to clear the faults must be capable of tripping single pole and the relays must be able to detect and identify single-line-to-ground faults apart from all other types of potential faults. Single-pole tripping is a temporary solution requiring fast reclosing. If the single-line-to-ground fault persists after the first reclosing, the relay must conclude that the fault is permanent and initiate a three-pole trip.

Cross-Country and Simultaneous Faults

The probability of simultaneous faults increases when circuits are in close proximity to each other. Generally, two independent relays detect the faults and respond accordingly. As single-pole tripping becomes more widely spread, some simultaneous faults can be cleared by independent single-pole trips even though they involve different phases.

Consider the scenario of the system in Figure 5.31 where Line 1 and 2 share a common transmission line tower. Suppose that a lightning strike close to Bus R causes an A-phase-to-ground fault on Line 1 and a B-phase-to-ground fault on Line 2. Because a single event has become two independent faults, single-pole tripping will allow both faults to clear. Because the relays are directional, both D and B at Bus R will correctly identify the phase. However, the relays at A and C will see the fault as an A-to-B-to-ground fault and want to trip three pole.

The relays at A and C will probably see the fault in Zone 2, while B and D will see the fault in Zone 1. In this case, Relays B and D will operate first and A and C are delayed. After B and D are open, A and C may see the fault in Zone 1 and trip instantaneously without changing the fault type selection. If the relay is intelligent to change the fault identification before tripping, relays A and C can also operate single pole. However, this is rarely the case because the fault type selection logic is already setup and waits for the Zone 1 trip signal or the time-out for Zone 2.

Another solution that allows A and C to single-pole trip is if the fault type selection at Bus R is communicating with the respective relays at Bus S. Since relays A and C are already waiting for the Zone 2 time-out, there is time to communicate this information.

Outfeed

Some three-terminal configurations promote an outfeed condition for faults in some sections of the line. For the case with a fault at the location shown in Figure 5.38, the relays expect that fault current is supplied from Buses S, R, and T. If the sum of the line impedance for line segments 1d, 1c, and 2 is less than that of 1b, then the fault current through causes Relay C to see the fault in a reverse direction. In such an event, sequential tripping will eventually clear the fault. Initially, Relay B will open

and cause the current through Relay C to reverse and subsequently open for either a Zone 1 or Zone 2 fault. Relay A will also open but most probably for Zone 2 because of the distance to the fault. Relay C will most likely be the last to trip because it is the last to see the fault.

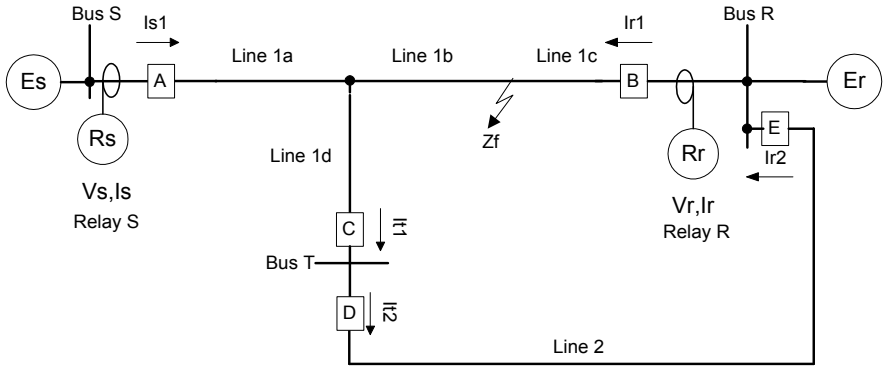


Figure 5.38: Network Configuration Promoting Outfeed

One way of overcoming the slow sequential tripping is to allow relays to communicate using direct transfer tripping for Zone 1 faults from Relays A, B, and C. (See section 4.1.2.2.5.)

DIFFERENTIAL LINE PROTECTION SCHEMES????

SPECIAL LINE RELAYING????

Protection of Compensated Lines????

UNIT PROTECTION (SEE GEC)????

UNDERGROUND CABLES (21GX)

Underground cables have three ground failure modes with radically different zero-sequence impedances. One mode is the fault-to-the-shield that is grounded on the cable terminations. Another other mode is a fault-to-the-earth at the point of failure. The third mode is a combination of the first two with varying degrees of fault resistance. Starting with Equation 4.72, the loop equation for a single-line-to-ground fault, the apparent impedance is expressed by Equation 5.24. For ground faults the magnitude of ZL_0 may vary as much as a factor of 10 and the angle may vary as much as 80°. Since the $k_0 + I_r$ term appears in all ground distance and direction equations, the sensitivity is propagated through these algorithms. Examination of Equation 5.16 shows that the coordination becomes difficult for overcurrent relaying and causes relay under- and overreach problems in distance relaying, as shown in Equation 5.24.

$$mZL_1 = \left[\frac{Vs_A}{(Is_A + k_0\, Isr) + I_A\, R_F} \right] \qquad \text{Equation 5.24}$$

$$\text{where} \; k_0 = \frac{ZL_0 - ZL_1}{3 \cdot ZL_1}$$

Line models????

Shielded phases????

Shielded cables????

Special considerations????

THERMAL PROTECTION OF POWER LINES AND CABLES

Heating of Overhead Lines

The heat balance equation for overhead conductors takes into account heat gain from the watt loss, convection loss from wind velocity, heat loss from radiation, and heat gain from solar radiation. These parameters are defined in subsequent equations with tables and polynomial equations provided to determine constants as explained in IEEE Std 738-1193 [4]:

$$q_c + q_r + mC_p \frac{dT_c}{dt} = q_s + I^2 \cdot R(T_c) \qquad \text{Equation 5.25}$$

where
q_c = Convected heat loss
q_r = Radiated heat loss
mC_p = Total conductor heat capacity
$R(T_c)$ = Conductor electrical resistance

Forced Convection Heat

Equation 5.26 gives the heat loss in a conductor for low-speed wind velocity. However, Equation 5.26 underestimates losses from high wind speeds. Use Equation 5.27 for high-speed wind velocity:

$$q_{c1} = \left[1.01 + 0.371 \left(\frac{D\rho_f V_w}{\mu_f} \right)^{0.52} \right] \cdot k_f \cdot (T_c - T_a) \qquad \text{Equation 5.26}$$

$$q_{c2} = 0.1695\left(\frac{D\rho_f V_w}{\mu_f}\right)^{0.6} \cdot k_f \cdot (T_c - T_a) \qquad \text{Equation 5.27}$$

where

D = Conductor diameter (in)ρ_f = Density of air (lb/ft^3)
μ_f = Absolute viscosity of air (lb/ft h)
V_W = Velocity of the air stream (ft/h)
T_c = Conductor temperature (°C)
T_a = Ambient temperature (°C)
k_f = Thermal conductivity of air, W/ft (°C)

The physics governing cooling caused by wind velocity, unfamiliar to many protection engineers, are given in tables or polynomials provided in IEEE Std 738-1193.

Radiated Heat Loss

Radiated loss depends on the emissivity, e, (0.23 to 0.91) which is a property of the surface and diameter of the conductor and is proportional to the 4th power of the absolute temperature:

$$q_r = 0.138 \cdot D \cdot \varepsilon \cdot \left[\left(\frac{T_c + 273^\circ}{100}\right)^4 - \left(\frac{T_a + 273^\circ}{100}\right)^4\right] \qquad \text{Equation 5.28}$$

Solar Gain

Heat gain in the conductor from the sun is given by **Error! Reference source not found.** with the angle defined as in Equation 5.30.

$$q_S = \alpha \cdot Q_S \cdot \sin(\theta)A \qquad \text{Equation 5.29}$$

$$\theta = \cos^{-1}\left[\cos(H_c)\cos(Z_c - Z_l)\right] \qquad \text{Equation 5.30}$$

where
Θ = Effective angle of incidence of the sun's rays (degrees)
α = Solar absorptivity (0.23 to 0.91)
Q_s = Total solar and sky radiated heat flux, (W/ft^2)
A = Projected area of the conductor, (ft^2/ft)
H_c = Altitude of sun (degrees)
Z_c = Azimuth of the sun (degrees)
Z_l = Azimuth in line degrees

Tables and polynomial equations for determining these constants are provided????.

Conductor Electrical Resistance

The values conductor resistance at high temperature T_{high} and low temperature T_{low} The resistance can then be determined by linear interpolation:

$$R(T_c) = \left[\frac{R(T_{high}) - R(T_{low})}{(T_{high} - T_{low})} \right] \cdot (T_{high} - T_{low}) + R(T_{low}) \qquad \text{Equation 5.31}$$

The heat loss equations reviewed above have been successfully implemented as the thermal element in a microprocessor-based line protection relay.

Power Cable Thermal Model

Figure 5.39, the thermal model of a cable, shows the thermal resistance and the distribution of the thermal capacitance for all layers of the cable. The model of a multilayered cable is characterized by complexity and the relative difficulty of determining parameters. Thermal capacitance and resistance for cables must be calculated using physical parameters [5].

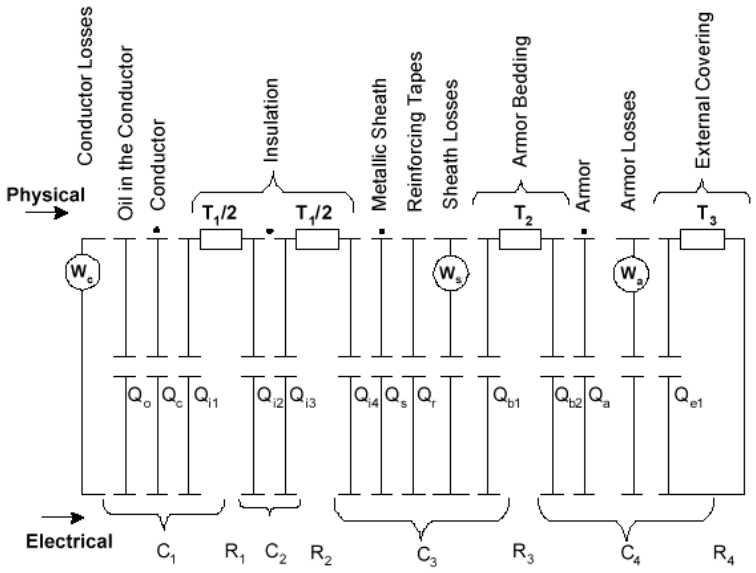


Figure 5.39: Thermal Model of a Cable

Thermal resistance of a cylindrical layer

Equation 5.33 is for a cylindrical layer of insulation. Thermal resistance must be calculated for each layer of insulation, and armor, and for the screen layers, sheath and/or oil layers that make up the cable. T is the IEC symbol for thermal resistance:

$$T = \frac{\rho_{th}}{2\pi} \cdot \ln\left(\frac{r_1}{r_2}\right) \qquad \text{Equation 5.32}$$

where
P_{th}= Thermal resistivity of the material K m/W
r_1= Inside radius (m)
r_2= Outside radius (m)

Thermal capacitance

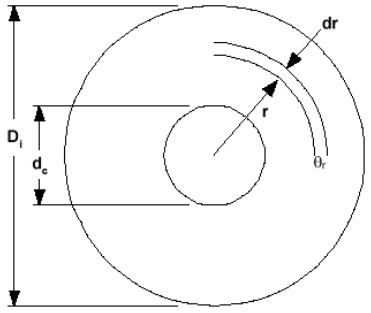
Calculate the thermal capacitance for each layer of insulation, armor, sheath, and/or oil that makes up the cable outer layers. Thermal capacitance is the volume of the material multiplied by its specific heat. Q is the IEC symbol for thermal capacitance.

$$Q_{th} = V \cdot c \cdot \frac{4}{\pi} \cdot \left(D_2^2 - D_1^2\right) \qquad \text{Equation 5.33}$$

where
V = Volume (m^3)
c = Specific heat ($J/(m^3 \cdot K)$)
D_1 = Inside diameter (m)
D_2 = Outside diameter (m)

As Anders describes [6], "The thermal capacity of the insulation is not a linear function of the thickness of the dielectric. To improve the accuracy of the approximate solution using lumped constants, Van Wormer, in 1955, proposed a simple method of allocating the thermal capacitance between the conductor and the sheath so that the total heat stored in the insulation is represented." The derivation shown in Figure 5.40 is based on the assumption that the temperature distribution in the insulation follows the steady-state logarithmic distribution during the transient. A three-node representation of the dielectric of a cable with thermal capacitance distributed using Van Wormer coefficients is shown in Figure 5.41.

The thermal model in Figure 5.39 may suggest that measured current can be used to calculate temperature in a cable. However, the density and resistivity of the soil backfill is crucial in determining the temperature rise. Therefore the backfill temperature must be monitored.



$$p = \frac{1}{2\ln\left(\frac{D_i}{d_c}\right)} - \frac{1}{\left(\frac{D_i}{d_c}\right)^2 - 1}$$

Figure 5.40: Logarithmic Distribution of Thermal Capacitance in Annular Insulation

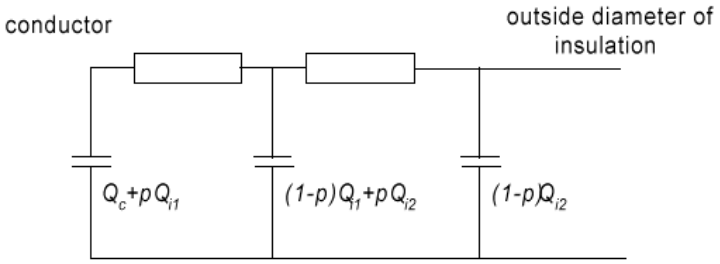


Figure 5.41: Three-Node Representation Using Van Wormer Coefficient

Summary of Thermal Protection of Lines and Cables

1. A long-time extremely-inverse overcurrent relay can emulate the shape of a thermal characteristic and can be coordinated to give thermal protection for a fixed initial condition. However, once heating occurs the overcurrent relay cannot prevent thermal damage for cyclic overloads.

2. An IEEE standard [3] defines thermal models for calculating transformer hottest-spot winding temperature, using top-oil temperature as the starting point and involving nonlinear time constants. The standard gives an alternate method using bottom-oil temperature that is more accurate but requires test data that is rarely available by specification.

3. A comprehensive IEEE standard gives the thermal model for overhead transmission lines. The heat balance equation includes convection and radiated heat loss and solar gain, as well as total conductor thermal capacity and watt loss. The standard provides polynomials for tabulated constants to aid computation. This thermal model has been integrated as an element in a line protection relay.

4. The thermal model for a multilayer cable is characterized by complexity and by the difficulty of determining thermal parameters. Although thermal capacitance and resistance values are available for transformers, motors, and overhead lines, for cables they must be calculated from physical parameters.

GENERAL RELAY APPLICATION CONCLUSIONS????

6 SUBSTATION PROTECTION

6.1 DATA RECORDING AND REPORTING [6080] [81]

Innovative developments within microprocessor-based relays have created new ways of collecting and reacting to data and then using this data to create useful information. Currently, power providers are dealing with demands to increase productivity and reduce costs that translate into the need to collect and act on decision-making information. Communicating information between protection components enables superior yet simple protection systems. This same information can supply other system needs such as automation, monitoring, and control.

Metering

Instrumentation Data

Power system conditions are emulated by creating digital representations of analog signals and discrete contacts. Various methods are used to instrument these values from physically interposed apparatus such as current and potential transformers, dc-wetted discrete contacts, and other sensors. There are many different methods for instrumenting different system values.

Instrumentation data are the result of the various instrumentation techniques used in the relay. The purpose of this data is to emulate the current status of the power system. With instrumentation data, we can protect, control, and analyze the power system using a virtual representation of power system characteristics. Instrumentation data are the source of all data and calculations in the relay and remote applications.

Protection Data

Protection decisions are based on the analysis of instrumentation data. Protection data can include currents, voltages, discrete digital inputs, physical location, and atmospheric conditions. The source of protection data may be local and/or remote. For local protection data, the relay making a specific protection decision instruments and/or calculates protection data. For remote protection data, another relay instruments and/or calculates protection data and communicates it to the relay making the specific protection decision. In this instance, the remote relay acts in part as distributed instrumentation and processing for the local relay and vice versa.

Protection analysis detects abnormal operating conditions resulting from disturbances on the system. The protection equipment must quickly determine the type and severity of the disturbance and decide if it needs to perform immediate action. This equipment must clear faults to protect people and equipment, then restore power quickly to minimize customer outage.

The local relay and remote relays coordinated within a protection scheme analyze protection data. Most protection decisions are mission critical and need to be made

in a sub-cycle time frame. The method of communicating this information must be dedicated, fast, reliable, and secure. The most secure method is a channel dedicated to this purpose alone.

Quickly communicating these data to several relays coordinated in a protection scheme enhances protection. Such coordinated protection is more robust and covers much greater distances when these data are communicated to remote relays via a single communications channel rather than the traditional method of a dedicated pair of copper conductors to sense every contact.

Metering Data

Traditionally, metering data are calculated analog values that emulate power system operating conditions. They are used for protection, monitoring, control, and revenue purposes. As mentioned above, the system operating conditions are calculated from the instrumentation data associated with the protection equipment. Metering data are calculated periodically to give a snapshot of the instantaneous state of the power system. Calculation examples include integration over time, scaling, and filtering. Some of the values necessary for metering already exist as a result of protection calculations and can be reused. Other system values are calculated specifically for the purpose of metering. Instantaneous and integrated values are archived periodically to provide peak and load profile historical characteristics of the system.

Metering data can be displayed locally and/or remotely to make power system conditions more visible to an operator. In this capacity, the metering data are a source of supervisory data. Local users traditionally view these data on a relay display, while remote users typically use a PC or other remote display with communications capabilities. Remote users view these data within a metering system, supervisory control and data acquisition (SCADA) system, energy management system (EMS), distribution automation (DA) system, or human machine interface (HMI).

Metering values such as demand and peak are archived within the relay to create historical information about the activity of the power system. These are discussed later in more detail as historical data.

Highly accurate metering data are useful for operations and revenue billing or validation purposes. These data can be the input to the revenue metering system within the enterprise and/or be used to validate calibration of other installed revenue metering devices. Revenue class metering at distributed locations within the power system allows operators to make accurate operational decisions. It also provides the most accurate information for protection equipment processes.

In the past, protection actions were initiated as a result of an electromechanical process passing through a threshold, such as an induction disc rotating to operate a contact. These processes were often adversely affected by environmental conditions. Now, decisions are made within microprocessors that operate uniformly through a wide range of environmental conditions. Metering data enhance protection because they are an accurate source for protection decisions, a source that is not affected by the passage of time or changes in the environment.

System Automation Data

System automation data are the result of logical decisions based on other types of data. These decisions often do not need to be made at the same frequency as protection decisions. Inputs to these algorithms can be derived locally or can be received from, or sent to, another device.

Results of these automated algorithms indicate that the relay needs to perform control, acquire and archive data, and generate event reports without intervention by an operator. These algorithms perform actions outside the scope of traditional protection algorithms at the device level and system level using protection data, metering data, extra contact inputs and outputs (I/O), and data communicated from other integration and control (I & C) components. The relay traditionally performs control of power system devices as a function of performing protection of the power system. System automation algorithms control the same, and additional, system components to perform ancillary actions like fault sectionalizing, restoration, and load shedding or transfer. Relays are an integral part of automatically controlling substations (substation automation) and feeders (distribution automation).

System automation data serve as another source for device-specific and station-wide custom protection decisions. System automation can be a combination of predefined processes and custom application-specific algorithms. Predefined system automation processes, such as reclosing, and user-defined custom logic can work in a coordinated manner with other relays to create application-specific system-wide protection.

System automation data are used locally by the relay and remotely by other I & C components performing system automation calculations. System automation data are an input to control and supervisory calculations. System automation decisions need to be made quickly and may result in mission-critical protection actions. Therefore, the method of communicating system automation data must be dedicated, fast, reliable, and secure.

These automation techniques enhance protection of individual power system components. More importantly, they better protect the entire power system as a whole. Automation techniques adapt protection methods as the power system configuration changes dynamically. Communicating these data via a single robust communications channel, rather than the traditional method of a dedicated pair of copper conductors, further enhances protection.

Control Data

Control data are the result of operator-initiated or processing-initiated functions that perform control actions. Control actions are initiated by local or remote protection algorithms or system automation algorithms or through the intervention of an operator. When the need for a relay to perform a control action is determined remotely, this function is initiated by passing a control message to the relay. Control actions can, therefore, be the result of disparate algorithms in many different devices with different execution time requirements.

These data allow the relay to influence the state of the power system through physical contact with power system devices. Control actions result in manipulating

the state of relay contact outputs, such as latching or pulsing discrete outputs, or changing the value of analog outputs. These actions in turn trigger when and how power system devices actuate. Remotely generated control messages can cause control actions or the manipulation of local relay logic. These different sources of control actions vary in speed of execution from subcycle to many seconds. Once the control function is initiated by the relay, or accepted from another relay, the control action speed is limited only by the relay ability to process and execute the result. The communications path for control messages that are initiated remotely determines any additional delay for the control action.

Control data enhance protection by initiating the operation of power system devices in accordance with protection and system automation decisions. Further, they allow remote operators and processing to change I & C system parameters and/or initiate the operation of power system devices as a result of system-wide protection considerations. Operators or equipment can send group-settings selection commands to relays to modify their processing to match changes in the power system characteristics, such as load variation or power system device failure. Finally, as mentioned earlier, communicating these data via a single robust communications channel, rather than the more traditional dedicated pair of copper conductors, enhances protection.

Supervisory Data

Supervisory data are any of the data types within the relay, or other I & C system components, that are used locally on an HMI or communicated to a remote device for the purpose of monitoring the power system. Much supervisory data are the result of other processing. Extra I/O points on the relay are often used to create additional supervisory data about power system components. The status of motor operated disconnects, load tap changer positions, and transformer fan status are examples of such data.

Often, contact inputs not used for protection instrument the status of system components. The results of some logical calculations in the relay can also provide supervisory data. Extra contact outputs can control additional power system devices. SCADA hosts, EMS hosts, DA hosts, HMIs, and other operator interfaces display system conditions and status. Operators can supervise the power system through these interfaces, which emulate its state, history, and reaction. The communications path for supervisory data influences the time discrepancy between when it is available in the relay and when it is visible to a remote operator or process.

The traditional data collection approach in the substation has been to build two separate I & C systems: one communications network and group of devices for protection and another separate communications network and group of devices for supervision and control. This adds complexity and cost yet reduces reliability. The relay is probably already collecting the data necessary for supervision as it is performing protection and other functions. If the supervisory system cannot acquire these data from the relay, a separate I & C device, such as a remote terminal unit (RTU), must be added simply to communicate system data that likely already exists in the relay.

Supervisory data enhance protection by allowing operators and equipment processes to make rapid, better informed decisions about system-wide, and device-specific protection.

Device Diagnostic Data

The relay stores information pertinent to analyzing the operation of power system devices. Examples include the total number of operations, frequency of use, duration of control actions, and interrupted current. Additionally, self-test processes internal to the relay create information about relay operation.

These diagnostic data provide information about the quality of both the power system and the I & C system. Any component failure is indicated immediately, which minimizes the unavailability of either system. With traditional periodic testing of relays, failures may not be noticed until the periodic test or a misoperation. In fact, during most traditional tests the device is out of service and some standard testing actually introduces modes of failure. System-wide device diagnostics allow operators and processing equipment to compensate for failed devices. In addition, analysis of diagnostic data to determine appropriate intervals for maintenance and upgrade can help prevent system and device failure.

The I & C system immediately detects device deterioration and alerts automatic equipment or operators to prevent or delay further deterioration. The system quickly alerts operators or equipment when these devices are unavailable to perform, enabling quick repair or replacement. Device diagnostic data enhance protection by maximizing the availability of the protection system.

Historical Data

The relay stores data to provide information about the reaction of the power system over time or to an event. This information includes system profiles, event reports, sequential event recorder (SER) reports, power quality reports, and protection quality reports. Locally, system disturbances, other events, or relay logic trigger report generation. Remotely, other I & C components or an operator trigger reports. A time synchronization command from a centralized source allows all devices in the system to use the same clock value for time stamps. Some system values are captured and archived periodically for trending analysis.

Historical report information allows forensic analysis of the power system and the I & C system so that decisions can be made to validate or improve system designs. Additionally, periodically stored values provide a profile of system characteristics over time. Archived performance data are used to trend device deterioration or improper configuration.

Event reports are collections of pre-trigger and post-trigger analog and digital values measured and captured in sequence and time stamped. This report captures the reaction of the system and the relay to a disturbance or other event in the power system.

SER reports are collections of data records stored as a result of user-defined changes of state. Each record contains time stamp and the present states of discrete digital inputs or digital logic values.

Power quality is a broad concept used in comparing the actual power system values to their ideal. Although there are many dedicated power quality measurement devices, relays are an effective measurement and storage device for some power quality data. Harmonics, frequency, voltage sag, voltage swell, and voltage interrupt are examples of power quality data captured by relays.

Most significant power quality problems are identifiable as power system voltage variations: complete interruption of voltage (<0.1 per unit), undervoltage (sag), and overvoltage (swell). A large percentage of these voltage variations are a result of power system faults. Recording and reporting voltage variation in the relay allows low cost correlation and validation of power consumer complaints. Monitoring the power quality allows the relay to react and compensate for power system variation or to alert users.

Protection quality data gauges the performance of the protection component of the I & C system. These data measure the ability of such items as instrument transformers, relays, batteries, and communications equipment to perform against stated benchmarks. Less testing is needed because the relay monitors element performance such as coordination margins, percent of settings reached, and other alarms and alerts an operator when the protection system deviates from nominal. In this manner, data are processed closest to the points measured, and protection quality answers are forwarded to operators.

Profile data, collections of archived metering data, provide an historical trend. At the pre-set profile acquisition interval, the relay adds a record to a profile report. This record contains a time stamp and the present value of each analog quantity being profiled. Remote users acquire these data and use them to analyze the load requirements and reactions of the power system. The data time stamp allows system-wide evaluation of the sequence-of-events from several devices. This facilitates system-wide operational and enhancement decisions such as connecting additional power sources and modifying protection settings.

The relay stores historical data in report format and communicates these reports to other devices automatically or on demand for additional remote processing. These reports can be quite large and take a lot of time to transmit. Fortunately, remote analysis is rarely appropriate immediately after it is recorded. Therefore, these reports can be communicated at a much slower rate than other data and need not reside on the same communications link as the other data types. Although it is convenient to transfer all data on a single channel, many integration protocols do not support file transfer.

Historical data enhance protection through dynamic system trend analysis, as well as being the source for remote operator and process forensic analysis. By continually monitoring the conditions of devices over time, operators and protection equipment develop a clearer picture of device performance.

Settings Data

Settings are the variables that configure relay software to function optimally in specific end-user applications. Additionally, settings initiate trigger conditions for event report and sequential event records and act as the parameters used to archive information.

Multifunction and multiapplication relays improve I & C system design. Settings allow the end user to coordinate the I & C system with power system and end-user protection practices. Power system parameters like conductor impedance and length influence each individual installation of a relay. Through settings, users can coordinate zones of protection, primary and backup schemes, and sectionalizing and restoration processes. Additionally, users can change settings dynamically to conform to changes in the power system. The relays stores several groups of settings and will change operation based on which group of settings is selected. Selecting predefined settings groups allows use of tested groups of settings for each selected condition.

This settings information is often calculated and stored remotely and then transmitted to the relay through a communications connection. Engineers, relying on their experience or expert software tools, can work remotely to create sophisticated, coordinated settings. Remote storage of the settings for each relay in the system allows a user to better maintain and review this data. This is particularly valuable in the event that an in-service relay needs to be replaced. Relay settings can be quickly retrieved from storage and transmitted to a replacement relay.

Many settings values interact in such a way that several settings must be changed simultaneously to change the operation of a relay. This results in a large amount of data being transferred during each transaction. However, using settings group selection commands for higher speed adaptation means these data are infrequently transferred to and from the relay. The path for communicating setting data must be secure but does not need to be high-speed nor does it need to reside on the same communications link as other data. As mentioned above, it is convenient to transfer all data on a single channel; however, many integration protocols do not support file transfer.

Settings data enhance protection by allowing the user to configure the relay to perform optimally in many unique applications. Settings groups allow the protection system to change dynamically to compensate for changes in the power system or I & C system. Finally, the ability to quickly configure replacement relays further reduces the unavailability of system protection.

Events monitoring [6002] [82]

Protection engineers are analyzing event reports of faults preserved by microprocessor relays to more clearly understand these faults and disturbances on transmission line systems. Their work frequently leads to better line parameters, more accurate locating of complex faults, and improved understanding of system operations. The event reports also help them determine fault resistance and explain otherwise unexplainable events.

Event Report Recording Equipment

Data stored before, during, and after a system disturbance or fault must provide protection engineers with sufficient information to investigate and/or recreate the event. The following data storage methods, some of which have existed for many years, are presently available.

Digital Oscillographs

These are typically installed in larger substations where a large number of lines are monitored. Data recorded from an event may be stored on disk or printed out on paper. An experienced operator must interpret the oscillograms. While this method shows the traditional sine waves on the printouts, accurately determining the phase angle relationships between the voltages and currents may be difficult. If large current magnitude differences exist between faults at the bus and the remote end of the line, scaling requirements may make it hard to unravel load from fault quantities.

Light Beam Oscillographs

These are typically applied the same way as the digital oscillographs. Data from an event are stored only on light-sensitive paper as traces that fade with time. A skilled operator must read the printouts. In older light beam oscillographs, the paper drum does not begin to move until after a start sensor detects the disturbance; thus, no prefault information is available.

Microprocessor Relays

Typically installed in single-terminal applications, these devices perform protective functions for the transmission line. All SEL relays produce and save event reports when faults or other triggering events occur. These relays report voltages, currents, relay elements and contact I/O in an easy-to-use and compact status format:

- Date and time of the fault or disturbance
- Prefault, fault, and post-fault voltages and currents
- Relay input and output contact status
- Relay element status
- Calculated fault location in miles or kilometers
- Relay settings at the time of the fault or disturbance

Reporting by relays has several advantages over oscillograph recordings:

- Relays are already in the station, whereas the additional expense of oscillographs rules them out in most stations.
- Relay event reports are more compact and easier to read, making retrieval and interpretation faster.
- At least one relay in a station will almost always be available for recording data. If the station relays on an oscillograph, however, data will be lost if the oscillograph is out of service.

Example 1: Incorrect AC Wiring????

Example 2. High-Impedance Ground Fault????

STATION BATTERIES AND DC CONTROL [6081]83

A protection system consists of circuit breaker(s), instrument transformers, protective relay(s), and a dc system. Every component of this system must perform properly for the system to work reliably. Measuring and improving the health of the dc portion of the protection system is vital.

The dc system consists of several parts:

- Power source including the battery and charger
- Wiring and connections
- DC system protection
- Switches, including protective relay contact outputs, auxiliary relay contacts, breaker auxiliary contacts, and isolation switches
- Loads, including protective relay contact inputs, auxiliary relay control coils, and circuit breaker trip and close coils

Battery Voltage Monitoring and DC Ground Detection

Figure 6.1 shows a small portion of a typical dc system. The batteries are usually series strings of lead-acid cells. Although the following discussion concerns 125 Vdc nominal battery systems, it applies equally well to other voltages.

Resistors R1 and R2 are sometimes replaced by lamps. The common connection of R1 and R2 is grounded. This references the battery to ground while still providing some isolation from ground. Isolation from ground is important, because inadvertent shorts from the dc system to ground do occur and the system must remain operative.

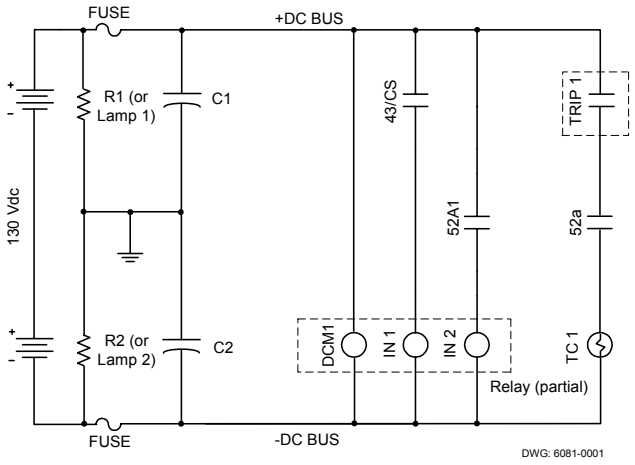


Figure 6.1: Portion of a Typical DC System

The definitions are as follows:

C1 and C2	Capacitance Caused by Wiring, Surge Protection, Power Supplies, etc.
R1 and R2	Battery Ground Centering Resistors
43/CS	Panel Mounted Feature Control Switch
TRIP1	Protective Relay Trip Output
52A1	Breaker Auxiliary Contact
IN1 and IN2	Protective Relay Contact Input
DCM1	DC Monitor
FUSE	Relay Panel Fuse
TC 1	Trip Coil 1
52a	Breaker Auxiliary

For example, consider an inadvertent short-circuit from the positive dc bus to ground. Before the inadvertent ground occurs, the current flowing through R1 and R2 is equal. Thus, under normal operation, R1 and R2 each support a voltage equal to half the total battery voltage. The inadvertent ground shorts out resistor R1. Therefore, the positive dc bus drops to ground potential, and the negative dc bus drops to the full battery voltage below ground potential. If Lamps 1 and 2 replace R1 and R2, respectively, Lamp 1 extinguishes during the positive dc ground, and Lamp 2 glows more brightly. Thus, the lamps detect and help locate the dc ground. However, lamps cannot notify remote personnel of a dc ground.

A single dc ground is not destructive. If a second short circuit is applied from the negative dc bus to ground, the dc protection system (panel fuses in Figure 6.1) operates to isolate the fault. It is important to isolate and remove dc grounds before this happens. Unfortunately, the method most often used to isolate dc grounds involves removing panel fuses or opening panel circuit breakers.

Figure 6.2 shows a dc ground detection and battery monitor circuit suitable for use in a protective relay (shown as DCM1 in Figure 6.1). The circuit connects to the positive dc and negative dc buses, and to ground. These connections are already present in the protective relay in the form of power supply connections and a surge ground connection. The circuit measures the voltage between the positive dc bus and ground and between the positive dc and negative dc buses. Resistors R3 and R6 are a very high value (22 MΩ) and are rated for high voltage (3 kV). For a 125 Vdc battery, they represent no more than a 3μ A leakage path from the positive dc and negative dc buses to ground.

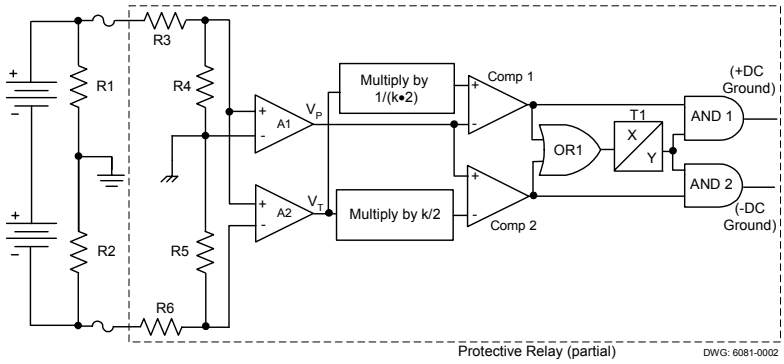


Figure 6.2: Battery Voltage Monitor and DC Ground Detector

The two instrumentation amplifiers (A1 and A2) sense the current flowing through R3 and R6 (via the voltage across R4 and R4 + R5, respectively). A1 produces a voltage, V_P, which is proportional to the voltage from the positive dc bus to ground. A2 produces a voltage, V_T, that is proportional to the total voltage from the positive dc bus to the negative dc bus. The value $V_T - V_P$ is proportional to the voltage from the negative dc bus to ground.

We use the values V_T and V_P to detect and help locate inadvertent grounds in the dc control wiring. We want to avoid any nuisance alarms. Nominally, V_P is approximately equal to ½•V_T. When $V_P > ½•V_T$, current is being shunted from the negative dc bus to ground. If $_P < ½•V_T$, current is being shunted from the positive dc bus to ground.

To avoid nuisance alarms, we create a dead band (see also **Error! Reference source not found.**)

$\frac{V_T}{2 \cdot k} \le V_P \le \frac{k \cdot V_T}{2}$, where $1 \le k \le 2$	Equation 6.1

When V_P is within this band, the dc system is in nominal operation and no alarm occurs. If $V_P \ge (k \cdot V_T)/2$, the relay alarms for a negative dc ground. The relay alarms for a positive dc ground when $V_P \le V_T/(2 \cdot k)$. Parameter k determines the sensitivity of the alarm conditions. Consider a value of 1.03 for k, which causes an alarm for $0.485 \cdot V_T \le V_P \le 0.515 \cdot V_T$. If the battery voltage $V_T = 130$ Vdc, then the relay alarms for 63.1 Vdc $\le V_P \le$ 66.95 Vdc.

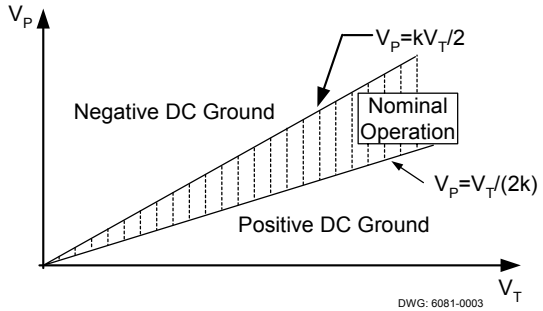


Figure 6.3: Alarm and Nominal Operation Regions for Circuit in Figure 6.2

Figure 6.2 also shows the logic for implementing the dead band detector described above. The output of comparator COMP1 asserts if $V_P \le V_T/(k \cdot 2)$. The output of comparator COMP2 asserts if $V_P \ge (k\ V_T)/2$. If either comparator output asserts for at least time X, the output of timer T1 asserts and the relay alarms for a dc ground.

The Effects of DC Grounds

One major West Coast utility reports measuring 100 - 400 μF of capacitance connected from ground to the positive dc and negative dc buses in its larger substations. This capacitance comes from dc surge capacitors in electronic equipment plus normal wiring capacitance. These capacitors store enough energy to energize some loads immediately following dc grounds. C1 and C2 in Figure 6.4 represent that capacitance. In the following cases, the 300 μF value illustrates a severe condition. Consider the effects of dc grounds applied at the points labeled 1 through 4 in Figure 6.4.

Case 1. Positive DC Bus Ground

An inadvertent ground on the positive dc bus shorts out R1. No equipment is affected for this circuit: the trip coil and relay inputs do not have a differential voltage across their terminals and the discharge/charge paths for C1/C2, respectively, are not through any of the dc equipment shown.

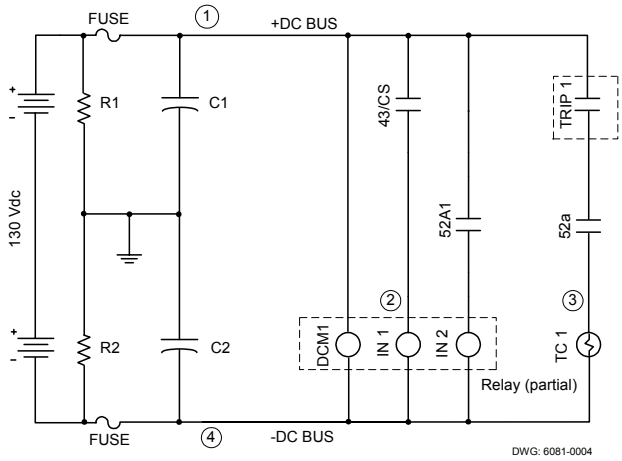


Figure 6.4: Portion of a DC System

Case 2. Ground Between the Open 43/CS Contact and IN1

Assume contact input IN1 has resistance much greater than R1 and R2. Typical values for R1 and R2 might be 3.3 kΩ. A typical value for the resistance of IN1 might be 30 kΩ. In this case, an inadvertent ground between the open 43/CS contacts and the relay input IN1 applies nearly half the total battery voltage to IN1 (see Figure 6.5). If IN1 asserts at less than half the battery voltage, a misoperation may occur.

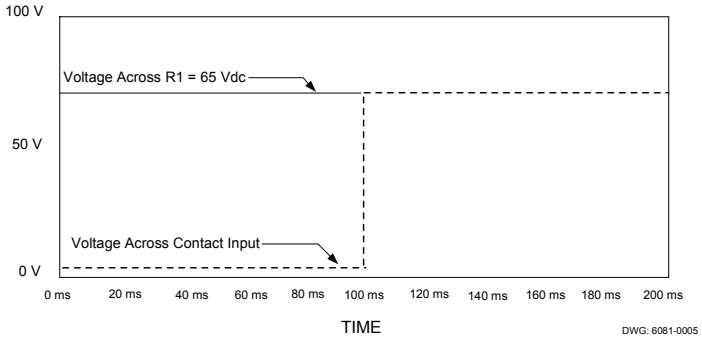


Figure 6.5: Contact Inputs Assert During a DC Ground if Pickup <1/2•VBATT

Case 3. Ground Between Trip Contact and Trip Coil

An inadvertent ground between the trip contact and the trip coil places the trip coil in parallel with R2 and C2. The trip coil resistance typically is much less than the value of R2. This causes the voltage across R2 and C2 to decrease and the voltage across R1 and C1 to increase for this dc ground. When the voltage across a capacitor changes, it discharges or charges. In this case, C2 discharges and C1 charges through the trip coil. The charge and discharge currents add constructively to nearly half the nominal trip current. Because both capacitors contribute to the problem, they appear in parallel. The time constant for the circuit is the product of the trip coil resistance and (C1 + C2). Assuming C1 = C2 = 300 μF, and a trip coil resistance of 13 Ω (10 A nominal), this trip coil is energized with a 4 A peak, 13 Ω•600 μF = 8 ms time-constant current spike (see Figure 6.6). This may be enough to operate the trip coil and trip the circuit breaker.

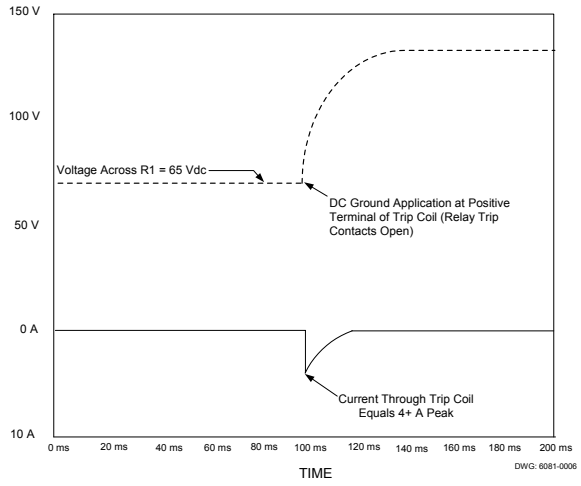


Figure 6.6: DC Ground at Trip Coil Input Terminals Operates Sensitive Trip Coils

Case 4. Negative DC Bus Ground

An inadvertent ground on the negative dc bus shorts out R2. No equipment is affected for the circuit shown: the trip coil and relay inputs do not have a differential voltage across their terminals, and the charge/discharge paths for C1/C2, respectively, are not through any of the dc equipment shown.

Cases 3 and 4 show that dc grounds on the positive terminals of loads are usually one of two cases:

- If the load resistance is an order of magnitude greater than the battery centering resistors, then a dc ground places up to half the battery voltage across the load indefinitely.
- If the load resistance is less than the battery centering resistors, then all of the surge capacitors connected to either dc bus charge/discharge through the load. The dc ground momentarily places up to half the battery voltage across the load.

Surge Capacitors on Loads or Contacts

In the cases considered above, grounds on the positive dc and negative dc buses had little or no effect on the dc equipment. However, adding surge capacitance to either contact input IN1 or to control switch 43/CS changes the situation. Figure 6.7 shows such surge capacitance (C3).

Reconsider Case 1, a dc ground applied to the positive dc bus. Before this dc ground, C3 is charged to -65 V. After the dc ground, C3 charges to -130 V. Thus, C3 discharged an additional 65 V because of the dc ground on the positive dc bus. Switch 43/CS is open, so the discharge current must pass through IN1. The voltage appearing across IN1 is limited to half the battery voltage. If IN1 only asserts for voltages greater than half the battery voltage, then it cannot assert falsely for this dc ground. (A similar situation exists for a negative dc ground.)

What if IN1 is allowed to assert for input voltages as low as one-fourth of the battery voltage? The circuit time constant is the product of the IN1 resistance and the surge capacitance. A typical surge capacitor on a contact input or output is 470 ρF. A typical resistance for a 125 V contact input is 30 kΩ. The time constant of this circuit is then 14.1 μ seconds (s). For the positive dc ground, the contact input voltage is greater than the minimum assertion voltage (one-fourth of the total battery voltage) for about 60 percent of a time constant, or about 9 μs. A protective relay that reads IN1 16 times per power system cycle or once every 1.04 ms, would probably have one false assertion of IN1 for every (1.04 ms/(9 μs)) = 116 dc grounds. This probability may be unacceptable, but is easily remedied by time-qualifying IN1 for two or more samples. A better solution might be to remove the surge capacitor. Properly designed contact inputs or outputs should not require surge capacitors.

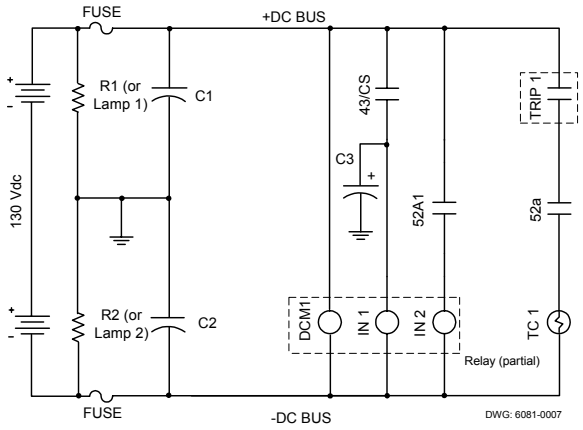


Figure 6.7: DC Control Circuit With Surge Capacitance

Negative Grounded DC Systems

The discussion above shows that dc grounds between contacts and loads place up to half the battery voltage on the load. If the contact or load has significant surge capacitance, then a dc ground on either dc bus can momentarily place up to half the battery voltage on the load. If the load is a contact input, we can solve these problems by ensuring the input does not assert for less than half the battery voltage or by time-qualifying the input. If the load is an auxiliary relay coil, or a circuit breaker trip or close coil, those solutions may be impractical. The case of a dc ground between a trip (close) contact and the trip (close) coil is particularly troublesome, because all surge capacitors or stray wiring capacitance connected to either dc bus charge or discharge through the coil.

Figure 6.8 shows a system that is less susceptible to the effects of dc grounds between trip (close) contacts and trip (close) coils. For this system to be effective, R3 must connect to the same dc bus as the trip/close coils. Switch SW2 is closed under normal operating conditions. In this example, R3 is much less than R1 or R2, but large enough to prevent a dc ground on the bus opposite SW2 from producing large currents when SW2 is closed. Assume R3 is 100 Ω. This value of R3 limits the current produced by a ground on the positive dc bus when SW2 is closed to less than 1.5 A.

Because R3 is a much lower impedance than R2, the negative dc bus and the positive terminal of trip or close coils are less than 5 V below ground potential with SW2 closed. A dc ground at the positive terminal of the coil creates less than 5 V across that coil, regardless of the coil resistance.

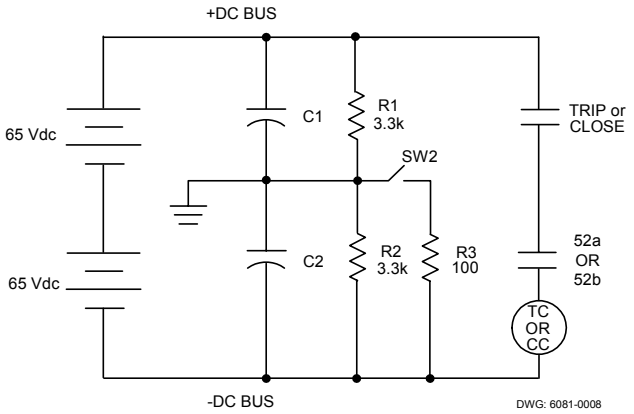


Figure 6.8: A System to Lessen Impact of DC Grounds on Trip and Close Circuits

One disadvantage of the circuit shown in Figure 6.8 is that it prevents detection of negative dc bus grounds while SW2 is closed. One major utility using this scheme opens SW2 routinely to check for negative dc bus grounds. In applications at this utility, SW2 is a manually controlled switch. In operator-occupied substations, an operator opens SW2 daily. In nonoccupied installations, operators open SW2 whenever they patrol the substation.

Control of SW2 can be automated. In a relay equipped with the dc-ground detection logic shown in Figure 6.2, the relay would open SW2 momentarily and check for dc grounds.

Switching SW2 is the same as applying and removing a negative dc ground. As discussed above, when contacts or contact inputs have significant surge capacitance, a dc ground on either dc bus can momentarily place up to half the battery voltage on the contact input. The situation is actually worse when SW2 is closed.

Consider Figure 6.9, which shows a contact output connected to a contact input with switch SW2 closed. Either the contact output or the contact input has 470 ρF of surge capacitance. Assume we place a ground on the positive dc bus in Figure 6.9 with SW2 closed. Before application of the positive dc ground, the surge capacitor is charged to approximately -5 V. After the dc ground, the surge capacitor is charged to -130 V. This means that the surge capacitor discharged 125V. Because the contact output is open, this discharge current must pass through the contact input. In fact, the dc ground places almost full battery voltage momentarily across the contact input. Therefore, all contact inputs used in this dc system must be secure to momentary application of the full battery voltage. Using two or more consecutive reads to time-qualify its output appears to be the only way to prevent the contact input from asserting in this situation (see Figure 6.10).

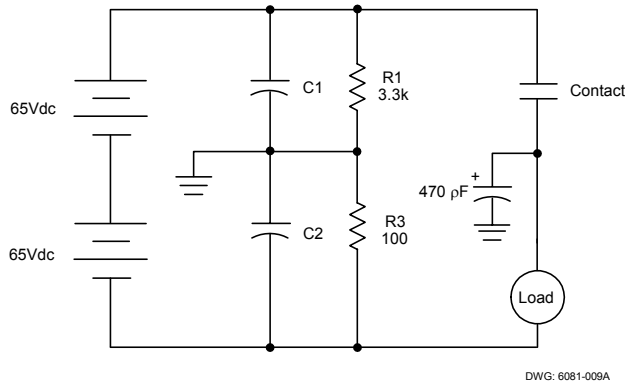


Figure 6.9: Negative DC Grounded System With Load Surge Capacitance

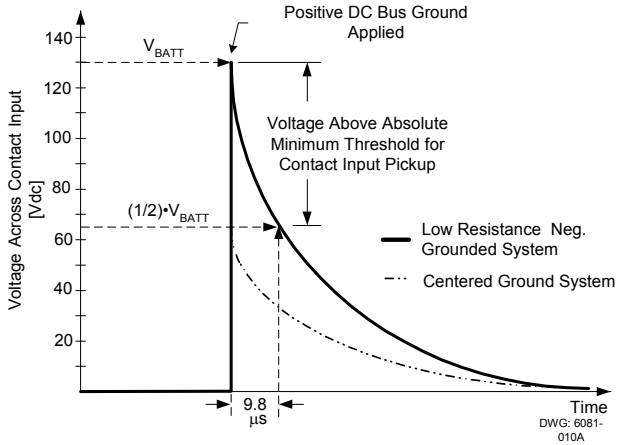


Figure 6.10: Plot of Voltage Presented to a Contact Input for positive dc Ground on a Negatively Grounded and Center Grounded DC System

In such a negativenegative dc-grounded system, the dc ground scenario of Case 3 is still troublesome because a second dc ground on the positive dc rail presents the trip coil with full battery voltage. Unless the application uses a target-indicating relay (which targets the fact that the trip coil drew current), all that anyone would know is that the breaker tripped.

The proposed inadvertent dc ground monitoring feature, when placed in a protective relay, can help the situation. This same relay also monitors breaker status, which is recorded in the relay event recording function. Given these recording and monitoring functions, engineers and operating personnel can access the relay event data to discover the sequence of events that led to the breaker opening:

- Initial inadvertent ground on or near the negative dc bus detected by the dc system monitor circuit of **Error! Reference source not found.**????.
- Simultaneous apparent removal of the negative dc ground and application of a positive dc ground.
- Breaker 52a status changes state from closed to open without the relay or control switch issuing a trip.

Improved Contact Input

The contact inputs of digital and static relays convert the open/close status of initiating contacts into a form recognizable by the relay electronics. In traditional relay designs, each contact input has two possible states: asserted when voltage is present across the input and deasserted when voltage is not present across the input. The previous discussion demonstrates that a good contact input should assert only when more than one-half the battery voltage is applied, and only if that voltage is applied for a sufficient time.

A contact input circuit that actually measures the applied voltage can help measure and improve the health of the dc system. Figure 6.11 shows the various proposed voltage thresholds of a contact input that measures the applied voltage. If the voltage applied to the contact input is between zero and half the nominal voltage, then it is deasserted. If the voltage is greater than half the nominal voltage, then it is asserted.

Figure 6.11 also shows alarm thresholds. If the measured contact voltage is between one-quarter and three-quarters of the nominal voltage, an abnormal condition exists: the contact input is malfunctioning, significant leakage exists around an open contact, significant resistance exists in a closed contact, or a dc ground exists somewhere between the initiating contact and the contact input. Of these, the latter is most likely. Detecting the existence of a dc ground between a contact output and contact input assists greatly in locating dc grounds.

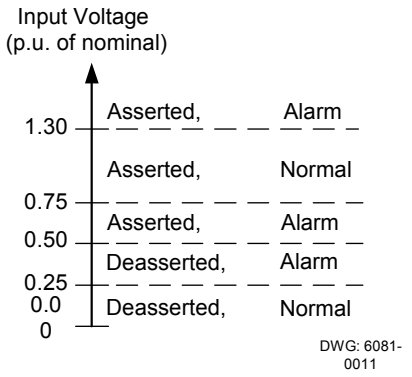


Figure 6.11: Assert/Deassert and Alarm/Normal Thresholds for a Contact Input

If the applied voltage is greater than 1.3 times the nominal voltage, the battery charger is malfunctioning or the contact input is defective, configured incorrectly, or not connected to the right battery.

Determining the correct values for the various thresholds can be problematic. Consider a protective relay housed in a circuit breaker cabinet. Table 9, "Rated Control Voltages and Their Ranges for Circuit Breakers," in *ANSI Standard C37.06 : 1987* requires that auxiliary equipment used as part of breaker control be subject to the same voltage limits as those used for the breaker trip and close coils. According to that standard, for a 125 Vdc nominal system, the operating voltage range for trip and close coils is 70 Vdc to 140 Vdc. The lower limit allows for drops in the control wiring and target coils that are part of the trip circuit. If the contact input were perfectly accurate, it would not assert because of a dc ground when the battery is

floating at 140 Vdc, even if programmed to assert at 70 Vdc. If the contact input is not perfectly accurate, then the requirement to operate at 70 Vdc conflicts with the requirement not to assert for a dc ground when the battery is at 140 Vdc.

Allowing the thresholds shown in Figure 6.11 to track different battery voltages resolve this conflict and decrease the number of false alarms in other applications. The circuit in Figure 6.2 measures the battery voltage. The vertical axis in Figure 6.11 would become "Input Voltage, (p.u. ≡ actual battery voltage)." Adaptive thresholds allow the contact input circuit to remain both secure and dependable, even given wide ranges in battery voltage.

For installations using two different voltage battery systems, 125 Vdc for the main control battery and 48 Vdc for the communications equipment, the relay must include two copies of the circuit in Figure 6.2. Each relay contact input is then assigned a dc monitor circuit and its threshold tracks the respective battery voltages.

Monitoring Coil Path Continuity

Monitoring trip and close path continuity allows users to know when either of these critical circuits experiences an open circuit condition. This is especially important for installations with a single trip coil. Two contact inputs and the programmable logic found in many microprocessor-based relays can monitor coil path continuity.

Traditional trip coil monitoring relays oversee trip coil path continuity with the breaker open or closed. To accomplish this same monitoring, connect two digital inputs of a protective relay as shown in **Error! Reference source not found.**????. Contact input IN2 monitors the continuity of the trip coil when the breaker is open or closed. When the breaker is open, contact input IN1 also checks the continuity of the wiring from the trip contact to the trip coil.

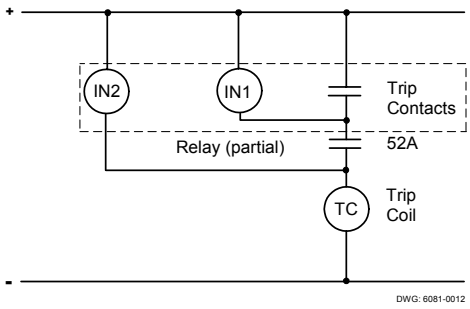


Figure 6.12: CD Connections for Trip Coil Path Monitoring Logic

Table 6.1 shows the logic required to monitor the trip coil path.

Table 6.1: Trip Coil Path Conditions and Relay Input Status

Breaker Position	IN1	IN2	Trip Path Condition
Open	0	0	Loss of Tripping DC or Coil Open
Open	0	1	Trip Path OK
Open	1	0	Monitor Circuit Malfunction
Open	1	1	Monitor Malfunction or 52a Failure
Closed	0	0	Loss of Tripping DC or Coil Open
Closed	0	1	Trip Coil OK, Trip Wiring Bad
Closed	1	0	Wiring Error or 52a Failure
Closed	1	1	Trip Path OK

Legend: 0 ≡ Input Deasserted 1 ≡ Input Asserted

There are only two combinations that do not indicate some sort of problem:

- Breaker open, IN1 Deasserted, IN2 Asserted
- Breaker closed, IN1 and IN2 Asserted

Using a separate contact input called 52a for verification of the breaker position results in the Boolean equation (where * ≡ Logical AND, + ≡ Logical OR, ! ≡ Logical Invert):

TRIP_ALARM = !(!52a * !IN1 * IN2 + 52a * IN1 * IN2)

To prevent erroneous pickup of the trip coil path logic, introduce a short time delay to allow the breaker auxiliaries to transfer state and the trip contact to open following a trip.

If contact inputs IN1 and IN2 are the voltage-measuring type discussed above, they can alarm for slowly degrading circuit continuity before the circuit becomes nonfunctional.

Contact Input Debouncing vs Filtering

SCADA systems and Sequence-of-Event Recorders (SERs) have different requirements for contact recognition than do protective relays. An SER should record the time when the contacts first touch, ignoring any subsequent contact bounces. This debounce function is the same as a dropout timer set longer than the maximum bounce-open duration.

As discussed above, a protective relay should consider a contact input asserted only after some time qualification. This filter function is the same as a pickup timer set longer than the maximum transient assertion duration.

Both functions can combine in a single device. The SER function can record the time of first contact closure if the protective relay function subsequently determines

that the contact input asserts. This avoids cluttering SER data buffers with erroneous contact input assertions caused by contact bounces, dc grounds, or other transients.

Use Relay Output Contacts To Replace Auxiliary Relays for DC Current Interruption

Simplifying dc systems increases their reliability. One easy means of simplifying dc systems is to eliminate components. The large number of available output contacts in modern digital relay designs makes it easy to eliminate external dc auxiliary relays by supplanting them with the contacts of the digital protection and control relay.

External dc auxiliary relays are used for two primary reasons: to separate dc sources and to increase interrupting duty. Using individual contacts from the protective relay meets the first requirement. The second requirement is only met if the contact from the protective relay has at least the same interrupting capability as the auxiliary relay.

How Metallic Contacts Interrupt DC Current

Metallic contacts in dc control circuits must interrupt dc current. The ability of the contact to interrupt dc current depends on a complex relationship of open circuit voltage, load current, load characteristics, environmental conditions, contact arrangement, and interrupting contact material. Inductive loads are particularly difficult to interrupt. Even when the intended load is resistive in nature, control wiring can exhibit enough inductance to present the contact with an effective load having significant inductance. Cobine [1] gives an excellent discussion of the interruption process from a circuit theory standpoint. However, we found that when the circuit current and capacitance are sufficiently small, the interruption process for some contact materials does not proceed as Cobine described.

Consider the circuit in Figure 6.13.

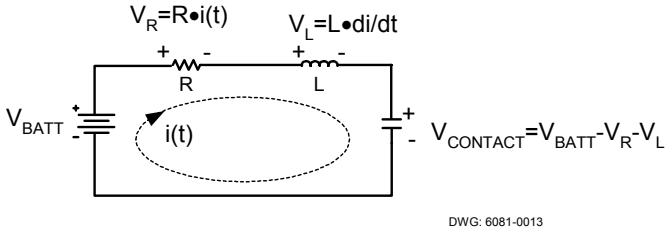


Figure 6.13: Typical Inductive DC Circuit

R and L represent the total lumped circuit resistance and inductance, respectively. When the contact closes, the current, i(t), increases gradually to a steady state value, i_{PK}. When the contact opens, i(t) does not instantly decrease to zero, because this implies an infinite di/dt and, therefore, an infinite V_L. The current, i(t), must eventually decrease to zero, or the contact will be destroyed.

To examine how small-gap metallic contacts interrupt dc current, we constructed the test circuit shown in Figure 6.13. Using this test setup, we tested several contacts suitable for use as protective relay output contacts. All contacts had 0.05 cm gaps. With these gaps, we expected an arcing voltage drop of about 15 V at 0.1 A. (Note that the arcing voltage drop is not the same as the flashover voltage. Theory predicts

and tests confirm that these contacts have an open-circuit flashover voltage between 2,500 and 3,000 V.) We fixed the battery voltage at 125 Vdc, and started with R = 1.25 kΩ and L = 75 H. This produced i_{PK} = 0.1 A, and a circuit time-constant L/R = 60 ms.

Refer to Figure 6.14. As the output contacts begin to part at time zero, current through the contacts abruptly chops to zero. However, current through the circuit inductance does not change appreciably. The inductor current rapidly charges the small stray capacitance appearing across the opening contacts. As the stray capacitance charges, the voltage across the contacts increases rapidly until it reaches the flashover voltage of the still parting contacts. At that point, the contacts flashover and begin to arc. As expected, the arcing voltage drop is low, so the contact voltage falls to around 15 V. A few microseconds after the flashover, current through the contacts again abruptly chops to zero, and the voltage again increases rapidly as the inductor charges the contact stray capacitance. However, the contacts have parted a bit more in the few microseconds since the last flashover, so the flashover voltage has increased. The voltage increases until it reaches this new, higher flashover voltage. The process repeats as the contacts separate, with the flashover voltage increasing as the contacts part.

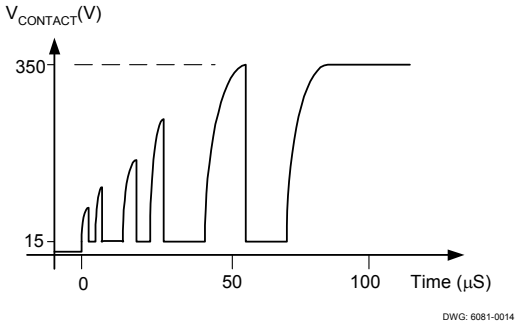


Figure 6.14: Typical Contact Voltage During Initial Separation

When the contacts separate sufficiently to support about 350 V, flashovers cease. The contact voltage then remains at approximately 350 V. The entire process, from first contact separation until the contact voltage stabilizes at 350 V, takes no more than about 100 μs for the contacts we tested. In that time the circuit current changed very little. At the instant the contact voltage stabilized at 350 V, the circuit current and voltages appeared as shown in Figure 6.15.

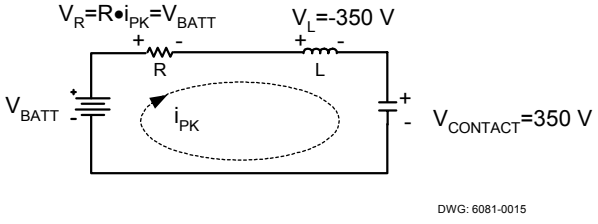


Figure 6.15: Circuit Voltages at Transition From Arcing to High-Voltage Conduction

Because the battery and resistor voltage cancel, a stable contact voltage of 350 V produces a voltage across the inductor of about -350 V. This causes current to begin decreasing through the inductor. Eventually, this current decreases to zero. As the circuit current nears zero, $V_{CONTACT}$ increases rapidly to about 350 V. This negative resistance region has negligible effect on the interruption process, because it occurs only near the end of the interruption. Figure 6.16 shows $V_{CONTACT}$ and i(t) during the interruption process.

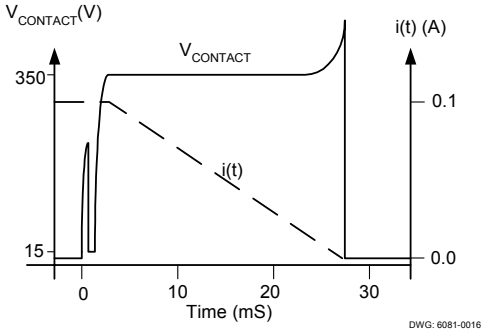


Figure 6.16: $V_{CONTACT}$ and i(t) During Interruption

If we increased $i_{PK} > 0.5$ A, the current chopping/arcing phenomenon shown in [redacted] (or a stable low-voltage arc) existed until the circuit current decreased below 0.5 A. When the circuit current decreased to less than about 0.5 A, the high-voltage negative-resistance conduction phenomenon occurred and the current again decreased to zero.

The current below which the conduction phenomenon changed from a low-voltage arc to the high-voltage conduction phenomenon varied with different contact materials. With AgCdO (Silver Cadmium Oxide) contacts, the transition occurred at 0.2 to 0.3 A. With gold-plated AgCdO contacts, it occurred at 0.6 to 0.7 A.

Initially we suspected that, as the gold plating burned off the contacts, the gold-plated contact performance would approach the AgCdO contacts. Surprisingly, we found the transition current increased significantly after the first few interruptions, then slowly decreased over many thousands of interruptions. After 10,000 interruptions, the gold-plated contacts still had a higher transition current than AgCdO contacts.

This discussion leaves a few questions unanswered. What is this high-voltage, negative-resistance conduction phenomenon? What roles do circuit voltage, inductance, and resistance have in determining contact damage during the interruption process? What effect does capacitance have on the interruption process?

To answer the first question, we again referenced Cobine. On pages 250 and 251 of [1], Cobine describes high-pressure glow discharge. High-pressure glow discharge is a low current-density, negative-resistance conduction phenomenon that creates a contact voltage of about 350 V. At one atmosphere in air, glow discharge transitions to a high-current-density arc at between 0.4 and 0.6 A. This description resembles closely the high-voltage conduction phenomenon described above. We believe the high-voltage conduction phenomenon is indeed high-pressure glow discharge.

$$E_{CONTACT} = V_C \frac{L}{R} i_{PK} \left[1 - \left(1 - \frac{V_C}{V_{BATT}} \right) \ln \left(1 - \frac{V_{BATT}}{V_C} \right) \right] \qquad \text{Equation 6.2}$$

where:

$E_{CONTACT}$ = energy dissipated in the contact
V_C = constant contact voltage during interruption
L/R = circuit time constant
i_{PK} = circuit current at the instant the contacts part
V_{BATT} = battery voltage
ln = natural logarithm

We could have approximated the energy dissipated in the contacts as the energy stored initially in the inductor. That approximation would be optimistic, because it would neglect the energy supplied by the battery during the interruption process.

From (1) we see that contact damage is proportional to circuit L/R and i_{PK}. The only variable of (1) without an obvious relation to contact damage is V_{BATT}. Figure 6.17 shows how $E_{CONTACT}$ varies with V_{BATT} for L/R = 40 ms and for several values of i_{PK}

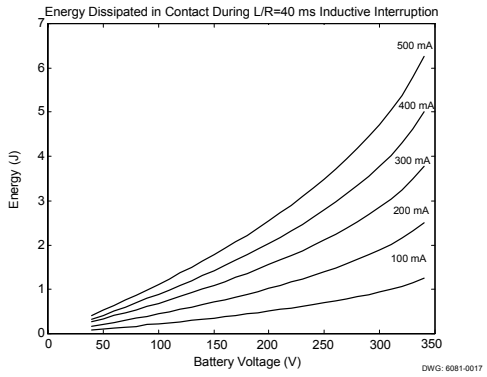


Figure 6.17: Graph of Equation 1????

Figure 6.17 helps relate known contact damage at one current/voltage combination to another current/voltage combination. For example, if we know the contact damage per interruption is acceptable at V_{BATT} = 125 V and i_{PK} = 0.4 A, then we would expect equal and, therefore, acceptable damage at 250 V and about 0.15 A.

If the circuit contains enough capacitance, the energy dissipated by the contacts changes because the waveforms of Figure 6.14 and Figure 6.16 change. In Figure 6.14, the time required for the circuit inductance to charge the capacitance to the flashover voltage increases. This gives more time for the contaminants introduced into the gap by the arc to dissipate, and for the contacts to cool. If the contaminants dissipate and the contacts cool sufficiently, glow discharge does not occur. Each time the arc extinguishes, the circuit inductance and capacitance begin to ring. If the peak of the ringing voltage is less than the flashover voltage of the contacts, then the

arc does not re-ignite. Interruption is complete after the ringing dies down. This reduces significantly the energy dissipated by the contacts. In this kind of interruption, the circuit resistance dissipates the vast majority of the energy stored in the inductor.

Interrupting Large Inductive DC Currents

To interrupt higher dc currents, we cannot rely on glow-discharge. We must either create a sufficiently large arc voltage by increasing the contact gap, or rely on the circuit capacitance to hold the peak ringing voltage to less than the open contact flashover voltage. We do not want to rely on circuit capacitance, and contacts with larger gaps tend to have slower operating speeds.

Error! Reference source not found.???? suggests another method of interrupting large inductive dc loads, while actually increasing the operating speed. The circuit of **Error! Reference source not found.**???? shunts current around the contacts (C) until they reach full separation, then clamps the ensuing inductive kick voltage to a level that the open contacts can withstand.

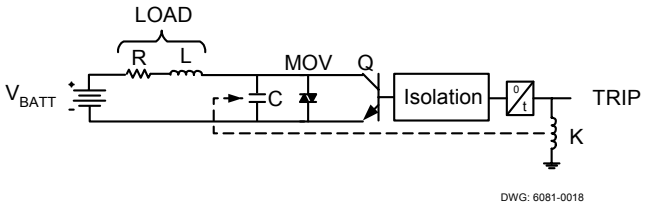


Figure 6.18: Application of High-Speed, High Interrupting Contact Output

In Figure 6.18, signal TRIP energizes the control coil K for the main metallic contacts. At the same time that TRIP energizes K, it also turns on transistor Q through the isolation device. Transistor Q turns on immediately and begins to conduct current through the load L and R. After some time the metallic contacts of K touch and begin to carry the load current. When properly designed, this circuit has a make-time of about 1 μs and the same continuous carry capacity as the metallic contacts.

A time-delay dropout timer keeps Q on for time t after TRIP turns K off. Time t allows the contacts of K to separate fully before Q turns off. When Q turns off, it forces the inductive current to flow through the MOV. Current flowing through the MOV causes it to break down and clamp at about 400 V. This creates negative voltage across the inductor, which forces the inductor current toward zero. Because the fully open contacts are capable of withstanding 400 V, no flashover, arcing, or glow discharge occurs. Also, the metallic contacts dissipate near zero energy. The MOV and circuit resistance absorb all of the energy stored in the inductor and produced by the battery. The contacts dissipate essentially zero energy, and therefore suffer negligible damage. In fact, this circuit has interrupted a 10 A, L/R = 40 ms inductive load at 125 V more than 10,000 times with no appreciable damage to the contacts.

Equation (1) gives the energy dissipated in the MOV for each interruption where V_C now is the MOV clamping voltage (400 V in this case). The energy is directly

proportional to L/R and i_{PK}. Figure 6.19 shows how much energy the MOV absorbs for a single interruption of a 40 ms inductive load.

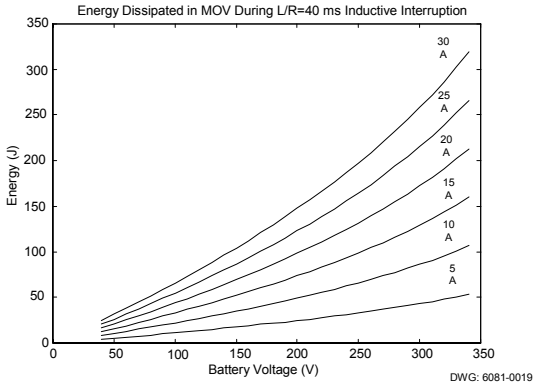


Figure 6.19: Graph of Equation Error! Reference source not found.???? for Circuit in Figure 6.6

The energy dissipated by the MOV is cumulative, if the MOV is not given time to cool. Such might be the case if the contact in question is interrupting trip or close coil current during a high-speed reclose sequence. For instance, given an MOV rated to dissipate 100 Joules, the circuit could interrupt a 10 A, 40 ms inductive load at 125 V four times in rapid succession (within one second). Following this sequence of high-current interruptions, the MOV must then be allowed to cool.

If the interruption is not repetitive, then the full energy rating of the MOV can be used for a single interruption. For example, if the MOV energy rating is 100 Joules, then the circuit can interrupt approximately 30 A of L/R = 40 ms inductive load at 125 V, or about 15 A at L/R = 40 ms inductive load at 250 V.

High-speed, high-interrupting output contacts have many uses.

Decrease Relay Operating Speeds (Trip Direct)

Relay operating time is the total time required to detect the fault and close the tripping output contacts. Open-to-close operating time for electromechanical output contacts is approximately 3 - 4 ms, or nearly a quarter cycle, at 60Hz. Use of the fast, high-current interrupting contacts described above avoids adding this one-quarter cycle to the tripping time. This increase in tripping speed occurs without loss of protection scheme security.

Increase Breaker Failure Margins (Relegate 86 to Hand-Reset Device)

From Figure 6.20, we see a cascade of events and the associated operating times of breaker failure relaying. All of these events must occur within the absolute maximum system fault clearing time. We can virtually eliminate the 86 (lockout) operating time by tripping each local breaker directly from the breaker failure relay using the high-speed, high-current interrupting output contacts described above. This saves approximately one cycle. Given this time savings, you can decrease the

absolute maximum fault clearing time. Alternatively, you may increase the breaker failure timer to increase security.

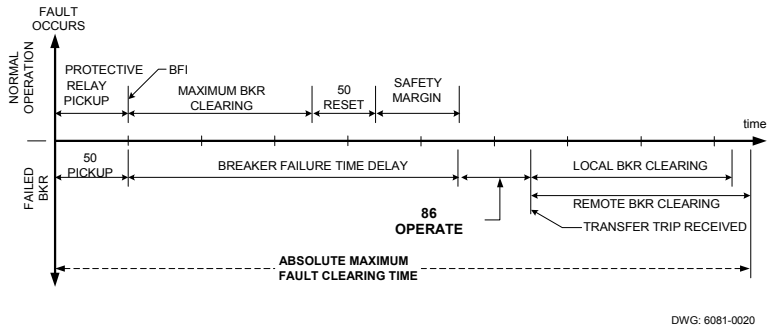


Figure 6.20: Basic Breaker Failure Scheme Timing

Figure 6.21 shows a typical dc schematic diagram where the breaker failure relay (or relay including breaker failure functionality) parallels its trip outputs with the existing 86 outputs. Notice that inclusion of the 86 device retains the mechanical hand-reset feature.

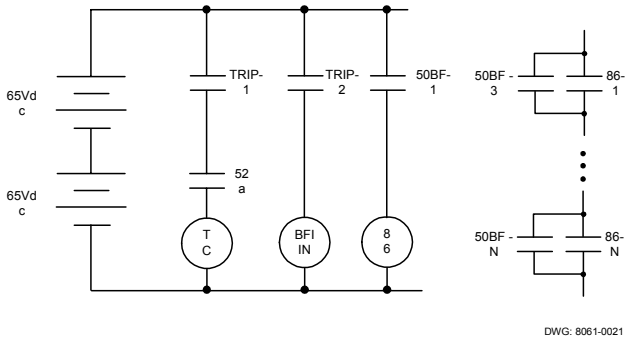


Figure 6.21: Typical Breaker Failure Schematic Using High-Speed Contacts

Stuck Breakers for Trip Direct Applications Should Not Destroy Output Contacts

In applications where the protective relay trips the breaker directly, the 52a contact normally interrupts the trip coil current. The exception to this is a mechanically stuck breaker. For such events, the 52a contact never opens. When the breaker failure scheme clears the bus, the protective relay senses removal of the fault and opens its tripping contacts. Because the 52a contact is still closed, the tripping contacts must interrupt the trip coil current. In such a case, the direct tripping contacts must be rated to interrupt trip coil current. An exception to this is where a "b" contact from the 86 is placed in series with the tripping contacts. For such applications, the 86 contacts perform the interruption, but only if the tripping contacts are guaranteed to drop out after the 86 operation.

Summary Remarks on DC Controls

1. An inadvertent dc ground must be detected; the second ground can operate the dc system protection and thus deenergize all connected loads. We discuss a simple means of including dc ground detection within a protective relay.

2. Contact inputs must have a minimum voltage threshold, for security during dc grounds. This minimum voltage threshold is at least half the battery voltage. We also introduce a new contact input circuit that measures the voltage applied to the contact input terminals. In addition to avoiding false contact input assertions during dc grounds, this measurement capability assists in locating the dc grounds.

3. DC system capacitance can operate auxiliary, trip, and close coils. In the cases we reviewed, stray and surge capacitors supplied the energy required to operate these coils. Capacitance in a dc control circuit may be necessary in some instances, but we strongly recommend removing capacitance where possible.

4. When loads connect directly to the negative dc bus, negative-grounding the dc system avoids the problem discussed in 3. above. We discuss means of automating the tests for inadvertent negative dc grounds in these systems.

5. The voltage presented to contact inputs can approach full battery voltage for positive dc grounds on negative-grounded systems. In such systems the contact inputs must be time-qualified to maintain security.

6. Monitoring the continuity of trip and close circuitry is important. We show a simple means of implementing this monitoring using contact inputs and simple programmable logic.

7. When interrupting highly inductive current, output contact damage is proportional to interrupted current and the L/R of the circuit. Properly designed metallic contacts reliably interrupt as much as 0.5 A of inductive current.

8. Combining a solid-state device with metallic contacts creates a hybrid output circuit. These hybrid relay contacts can reliably interrupt 30 A or more in very inductive circuits. This new capability simplifies the dc system by eliminating many dc auxiliary relays.

9. The nearly instantaneous operating speed (1 μs) of the high-current interrupting contacts increases protection speed without sacrificing security.

SUBSTATION RELAY DATA AND COMMUNICATIONS [6051] [84]

Multifunction digital relays have been available for over ten years and in popular use for nearly that long. Today, digital relays are by far the most popular choice for new protection and control installations, and they are widely applied to replace aging

electromechanical and solid-state electronic component-type relays and relay systems.

There are many reasons for the digital relay's popularity: price, reliability, functionality, and flexibility. But the feature that separates the digital relay from previous devices is information. Digital relays offer real-time and historical information about themselves, the power system, the protection and control system, and selected substation equipment. Such information includes:

- Fault location and fault type
- Prefault, fault, and post-fault currents and voltages
- Relay internal element status
- Relay control input and output status
- Instantaneous and demand metering
- Breaker operation data
- Relay self-test status

Traditional substation designs used separate devices to provide some of this information, such as metering and fault data. Other information, such as breaker operation data and relay self-test status, is not available in traditional substation installations.

Multifunction digital relays have opened a whole new world of information never before available and at virtually no additional cost -- in fact, at a reduced cost in many cases. Because of the widespread value of the relay's data, a variety of utility personnel, representing the interests of operating, maintenance, planning, engineering, and customer service, request the information they need in a format convenient for them to work with and in a time frame related to the response requirements of their job responsibilities. Accommodating these needs presents a challenge to the substation design team responsible for balancing functional and informational requirements of the substation design. Communication architecture and interface techniques play an important part in this process. But, the most important ingredient in the process is the imagination of the utility personnel who strive to minimize cost, increase efficiency, and improve power-system operation and reliability using the newfound tools available in today's integrated substations.

The Digital Relay Communication Interface - An Evolution

The digital relay communication interface has evolved over time to meet changing user needs. User needs have changed as utility personnel recognize the value of data provided by the digital relay and as new technology provided additional communication options.

Local Target Display

The mechanical flag or target was the first interface developed to communicate that the electromechanical relay had performed a function. As relays became more sophisticated, targeting systems evolved as well, to indicate which phase or zone of a particular relay's operating system had functioned. Solid-state relays carried on this

tradition through the use of electronic flags and light emitting diodes (LEDs). Some solid-state relay systems included LEDs to indicate the status of basic internal logic systems. It is not surprising that early digital relays incorporated LEDs to indicate, in basic function, what the relay had done. The conventional process of manual relay target collection, recording, resetting, and transcription is well established, so targets remain as a consistent part of even the newest relay designs. However, as communication and information processing techniques progress, the value of local relay targets will diminish and possibly disappear.

Local Display for Digital Data

As digital relay data became more sophisticated, the need arose to provide a more sophisticated medium to communicate this information. Fault information, such as current level, fault type, and fault location, required a local alphanumeric display for local interrogation by personnel dispatched to collect relay targets. Since faults occur rather infrequently, the local display was put to more continuous use to display real-time information, such as present voltage and current quantities. This, in essence, integrated the meter function into the relay. Many other functions followed, including relay element status, fault history, relay settings, line data, relay self-test status, and breaker operation data. With the addition of pushbuttons, the display also provides the ability to enter and change relay settings on some relays.

Communicate Locally with Terminal or PC

As digital relays progressed in both capability and information, the local targets and display capabilities quickly became inadequate. One or more communication ports became standard on digital relays to permit connection with a terminal or a PC with terminal emulation software. This greatly expanded the digital relay communication interface capability. Virtually all information in the digital relay could be accessed, and relay settings and other functions could be easily entered and changed.

Fortunately, the computer industry had developed some basic hardware interface standards for interconnecting computer equipment. One standard, EIA-232, became the initial defining communication interface that remains today, an almost universal constant among PCs, digital relays, and other IEDs.

Portable terminal and PC technology, and communication software capability, have developed along with the digital relay technology to meet a number of new requirements.

Interrogate Relay to Display and Capture Data/Reports

Communication and other support programs developed to permit easy interrogation of relays to display real-time and historical relay information and capture information to files for later analysis and reporting.

Remote Relay Settings

Proper relay settings, critical to the primary protection and control function of all types of relays, are most easily entered in the digital relay through a serial EIA-232 PC-to-relay communication interface. This interface also permits the user to confirm

relay settings and capture relay setting information to a PC file for documentation and record-keeping purposes. Techniques have developed to create, store, and modify relay setting files on the PC that are downloaded to the relay, easing the process of entering relay settings. Access to setting functions is typically restricted by passwords or pass-codes to provide relay setting security.

Remote Circuit Breaker Control via Relays

Some digital relays have control command functions that permit the user to open and close the power-system breaker through the existing control wiring between relay and breaker. This permits simple functional testing of the relay's output contacts and breaker control wiring. Access to breaker-control functions is typically restricted by security passwords or pass-codes.

Printed Output for Relay Messages

Some digital relays include a communication port that can be connected to a printer. Relay messages about faults, relay self-test status, and relay group setting changes are automatically sent to the printer to provide local documentation for operating and testing personnel.

Communicate Remotely with PC and Modem (Basic SCADA)

Digital relay interrogation and control functions that are performed locally can also be performed from remote locations with the use of PC, modems, and communication software. Communication media includes dial-up phone circuits, leased phone circuits, and user-owned microwave and/or fiber-optic communication networks. This remote communication capability allows engineering, operating, testing, maintenance, and planning personnel to directly access real-time and historical relay information that they need to perform their jobs.

Basic SCADA functions are performed by some utilities using these remote interrogation and control capabilities. Access to various setting and control functions is typically restricted by passwords or pass-codes, similar to local communication access security.

Multiple Relay Communication

The proliferation of digital relays and IEDs with local and remote communication capability requires communication concentrators that allow communication with multiple devices through a single communication channel. Two communication configurations, multidrop and point-to-point, are typically used in today's substations to interface with multiple relays and other IEDs. There are advantages and disadvantages to each of these configurations. For the purpose of this paper, the point-to-point configuration will be shown. Point-to-point communication typically uses the almost universal EIA-232 interface standard found on computer equipment and almost all digital relays and other IEDs. A port switch device is commonly used to transfer the communication connection from one IED to another.

Basic port switches allow communication between a master port and only one slave port at a time. This permits either local or remote communication with a single relay

or IED. Some basic port switches buffer messages automatically sent from attached relays. The port switch may also include a printer port to print these messages for the convenience of a local operator.

Multiple Relay Time and Clock Syncnchronizing

Digital relays and many other IEDs include a built-in clock to time-tag sampled data and events. This time-tagged information adds significant value to each individual device. However, all microprocessor based clocks, whether battery-backed or not, have some drift. Over time, differences develop between the time on each device that cause considerable confusion when comparing sampled data and event information from multiple devices.

The use of multiple digital relays and IEDs with built-in clocks requires a system to synchronize these clocks, either continuously or periodically. Continuous synchronization can be accomplished several ways, but the use of IRIG-B time-code synchronization is quite popular. The demodulated IRIG-B time code consists of a logic level (0 to +5 volts) pulse train encoded to provide day-of-year and time-of-day. Many digital relays and IEDs include a port designed to accept either a 1 kHz modulated or a demodulated IRIG-B signal.

Some devices that do not accept a synchronizing time-code input will accept a date and time command to update and correct their built-in clock/calendar. While not as accurate as a time-code input, the date and time command method, performed periodically, maintains date and time synchronization that satisfies most application requirements.

SCADA/RTU Interface

Real-time digital relay data is of particular value for system operating personnel. Real-time voltage, current, watt, and VAR data are needed to operate a system. Fault type and fault location, unavailable until the advent of fault locating digital relays, are now required by most operating and dispatch centers to guide system restoration. Economics and efficiency dictate that this information be transmitted to operating personnel through the same SCADA system interface from which they receive all other operating data.

Conventional SCADA RTUs accept only analog inputs (scaled current or voltage) and status inputs (dry or voltage wetted contacts). Digital relay data, therefore, are not directly compatible with these conventional RTUs. Although it seems somewhat inefficient to convert the digital relay data, which are originally analog and contact status, back to analog and contact status output to satisfy system operating personnel, in many cases, conversion is more cost effective than wiring separate devices to provide the same output.

Modern RTUs operate on digital principles that allow direct acquisition of digital data, permitting a direct interface between the RTU and digital relays or other IEDs. The same type of interface can be established with Programmable Logic Controllers (PLCs). Although communication protocol issues can complicate the use of this interface, many RTU and PLC vendors have developed simple and effective methods to establish this communication interface. Once in the RTU or PLC, these data are

polled from the SCADA central processor or passed to other IEDs like any other digital data.

Maintaining the digital relay data in digital format has the obvious advantage of security, maintained accuracy, and data handling efficiencies that produce better results at a lower cost. Other advantages accrue because more data are available from the digital relay than basic meter and fault data, including relay targets, relay elements, breaker interruption data, event history, relay self-test status, and settings.

Electromechanical Interface

Although it may not be considered on the same level as ASCII and binary digital relay communication, the digital relay electromechanical interface cannot be disregarded. This interface links the digital relay with the conventional inputs and outputs of the solid-state and electromechanical world. The status of these inputs and outputs is essential to a more complete understanding of operating states and sequence of events. In the solid-state and electromechanical world, the state of these interface points must be monitored by separate, external devices such as sequence of events recorders and oscillographs or fault recorders with status input points.

Most digital relays maintain the status of these points internally in a binary word format where the status of the input, off or on, and the status of the output, open or closed, is easily related to a binary state of 0 or 1. These binary words are updated and maintained in the digital relay and are available to interrogate or transmit through the communication interface.

Integrated Digital Relay Data Applications

Many utilities are examining their traditional practices in light of industry competition and renewed customer focus. As a result, utilities are focusing on ways to reduce both capital and operation/maintenance expenditures as well as ways to enhance revenue, while retaining or improving customer service reliability. One contribution toward these goals is the use of substation integration techniques.

Substation integration challenges traditional methods and opens the door to new and more effective methods of transforming, distributing, and controlling electric power. To a large extent, this new frontier exists because of the successful development and use of digital protective relays.

The key element in the digital relay is information. The key to successful substation integration is communicating and processing that information in the most efficient and economical method possible. This requires “open” network concepts that provide versatile options to satisfy multiple user needs.

Traditional Needs

Digital relays have evolved to include multiple interfaces, each designed to meet specific traditional data and control requirements. Integrated substation design offers the opportunity to meet these needs through a single digital interface, as shown in Table 6.2.

Table 6.2: Summary of Traditional Relay Data and Control Communication

Function ⇒ Interface ⇓	Real-Time Data	Historical Data	Local Control	Remote Control	Relay Set	Time Set/Sync.
Target Display		✔				
Relay HMI	✔	✔	✔		✔	✔
Printer Port		✔				
Local PC Port	✔	✔	✔		✔	✔
Modem Port	✔	✔		✔	✔	✔
Clock Port						✔
SCADA Interface	✔			✔		
Integrated SS Function	✔	✔	✔	✔	✔	✔

While integrated substation design accommodates and serves many traditional utility purposes, utility personnel use substation integration to go beyond traditional applications to achieve further cost efficiencies and system improvements.

Modern Use of Substation Relay Data and Communication

The demand for digital relay data seems insatiable. The reason for this stems from the innovative and creative applications of these data that digital relay users devise to solve long-standing problems that previously had no practical or economic solution. These new application techniques offer opportunities to improve protection, enhance control, speed outage restoration, improve operations analysis, automate maintenance functions, and improve planning and design data.

The following applications demonstrate improvements made feasible with substation digital relay data and communication.

Improve Protection

Use Digital Clock/Calendar to Change Protection

Some utilities have found that sensitive protection or fuse-saving coordination techniques result in nuisance outages that adversely affect reliability to critical customers. The ability to change protection based on time-of-day and day-of-week provides a compromise solution that avoids or reduces nuisance operations during hours when these critical customers are in operation. This also provides more sensitive protection and special coordination requirements when they are not in

operation. This is easily accomplished with digital relays by changing settings and logic through remote or local communication based on time-of-day and day-of-week.

Use Digital Relay Elements and Inputs to Change Protection

Protection requirements can change with system load and configuration. Conventional protection schemes must accommodate the worst-case operating scenario, compromising sensitivity and/or coordination under normal conditions. Optimize digital relay system protection based on the status of control inputs and internal relay elements.

One example using this technique alters distribution protection by changing distribution relay settings on each digital feeder relay when phase current demand or neutral current demand exceed specified levels. The original settings are highly sensitive. The new setting has less sensitive phase and residual overcurrent settings that tolerate higher loading but have reduced, but adequate, sensitivity. Relay settings on all circuits are changed to a third level when any one of the distribution relays trip. The third level settings have a longer time delay to tolerate inrush and surges following the fault on any of the distribution circuits. The current inrush typically occurs on all circuits following a fault on one circuit because of short-term transformer magnetizing inrush and the longer-term effect of restarting air conditioner motors that stalled during the fault. When all conditions return to normal for a prescribed time, the digital relays change back to their original settings.

Another example is adaptive protection. Here, the alarm contact from each of the digital feeder relays is connected to permit the backup relay to directly trip the breaker for the alarmed feeder. At the same time, the settings on the backup relay are changed to provide additional sensitivity to permit the backup relay to adequately protect the alarmed feeder.

Protective relay settings may be adequate during normal source conditions, but alternate relay settings may be required under some contingency source conditions. In the example the normal relay settings use negative-sequence polarizing for ground fault protection. However, when the generator on the far side of the delta-wye transformer is out of service, the negative-sequence source may become too weak to adequately polarize the relay, making zero-sequence current the preferred polarizing input. Automatically change relay settings from negative-sequence polarizing to zero-sequence current polarizing when the generator breaker opens, and change back to negative-sequence polarizing when the generator is in service.

Basic zone distance transmission line protection requires Zone 2 time-delayed overreaching relay elements. System configuration changes for equipment maintenance can reduce or even disable protection. As this example shows, use the dial-out and dial-in capability to automatically change the overreaching Zone 2 settings on each remote relay based on breaker and bypass switch status to restore adequate protection.

Communications for Enhanced Control and Minimum Wiring

Conventional protection and control schemes require independent control wiring for protection, SCADA, and manual breaker control. Additional wiring and switches are often used to control auto-reclosing functions. The use of multifunction digital relays

with communication offers numerous opportunities to enhance control functions and, at the same time, reduce conventional control wiring and eliminate many control switches and lights.

Basic zone distance transmission line protection requires Zone 2 time-delayed overreaching relay elements. System configuration changes for equipment maintenance can reduce or even disable protection. As this example shows, use the dial-out and dial-in capability to automatically change the overreaching Zone 2 settings on each remote relay based on breaker and bypass switch status to restore adequate protection.

A recloser on-off control switch is often included in line and feeder protection schemes to disable auto-reclosing when crews are working on or near energized line conductors. To operate this switch, someone must visit the station to turn auto-reclosing off and return again after the line work is completed to turn auto-reclosing back on. With multifunction digital relays, a control bit or multiple settings can be used to control auto-reclosing through remote communication, saving the cost to travel to the substation twice. As an added bonus, the relay element status indicates the auto-reclosing state, off or on, confirming the control change to the remote operator.

Some utilities use this communication capability to control reclosing on a wide-area basis. During good weather, when the risk of weather-related faults and outages is low, auto-reclosing is turned off to minimize the risk of reclosing for faults that may have human involvement, such as car accidents and crane contact. During storms, when the risk of weather-related faults and outages increases dramatically, auto-reclosing is enabled to optimize service reliability.

Speed Outage Restoration

The traditional method to find power-system faults usually involves two steps. First, the operator tries to energize the faulted circuit until he/she is convinced the fault is permanent. Most operators will instinctively make at least one attempt, even though the circuit may have already gone through one or more automatic reclose operations. Once it is determined that the fault is permanent, the second step is to sectionalize the circuit and try to energize only part of the circuit. Relay targets may be of some help in determining the nature of the fault, but it takes time to collect conventional relay targets because they must be read by an operator at the substation. The sectionalizing process will eventually reduce the fault location to an area or length of circuit between sectionalizing switches. If a customer has not reported the exact location because of the explosive results of the unsuccessful reclose attempts, personnel must be dispatched to patrol the circuit in the suspected fault location area. Needless to say, this approach is time consuming, labor intensive, and potentially hazardous.

Digital relays with built-in fault locating algorithms offer a tremendous opportunity to speed outage restoration. The fault location information is used to direct operating personnel to the proximity of the fault in a very timely manner, without the need for numerous reclose attempts. The communication capability of the digital relay offers several ways to retrieve the fault data from the relay in a timely fashion. The quickest method is to transmit the fault information through the SCADA system back to the control and dispatching center.

For systems that do not have SCADA, or where locations other than the operations center must be notified about faults and sent fault data, the automatic dial-out process presents some very nice solutions. With this communication capability, a variety of personnel at various locations can be sent notification and fault information, even paged.

Improve Operations Analysis Efficiency

Digital relays offer considerable information to perform operations analysis better than ever before possible with solid-state and electromechanical relays. The fault data and relay event reports show directly the protective relay's performance for each successive sample of power-system fault data. The power system's response to various faults at known locations is now also available to perform comparison with fault study models. With the proliferation of digital relays at numerous substation locations, the new challenge is how to manage the collection of this information in a timely manner. Data can be made available in printed format and in PC file format. The latter format offers the advantage of further interrogation and analysis through special software programs. The printed report can always be created from the file format at a later date, so the file format tends to be preferred by most utility personnel.

Event report file collection from individual relays can be time consuming. New substation integration techniques offer data concentration and automated data transfer capabilities.

Use substation integration to concentrate the event reports from several digital relays at a single location to make data collection more efficient. This avoids the need to establish communication with each individual digital relay to collect event reports.

Another useful capability is having the event report data from the weekend or previous night waiting for you when you arrive at the office in the morning. Use substation integration logic to send the event reports at a specific time each day, on selected days of the week.

For those who cannot wait to get the latest digital relay event report data from the most recent system disturbances, have the reports sent to your office after each event occurrence. The digital relay automatic event summary triggers the automatic dial-out process to send the latest event report summary or full event report to a remote computer waiting to capture the event information.

Likewise, use the same trigger condition to send a phone number to your pager so you can call the substation from wherever you are to retrieve the event information.

Concentrate alarm data from several relays and IEDs into a single alarm point for SCADA, but capture the individual alarm on a local substation annunciator or operator interface. Apply filtering to pass only permanent alarms to SCADA, but capture all intermittent alarms on the local substation log, or initiate a call directly to maintenance personnel for specific alarms.

Automate Maintenance Functions

Several routine maintenance and data collection operations are easily performed by automated means with digital relays and substation integration techniques.

Pilot schemes, especially those using on-off type carrier, need to be checked periodically to determine that the communication equipment and channel are in good operating order. Some digital relays with programmable logic capability can be set to test the communication channel and alarm if there is a problem. Use substation integration techniques to periodically initiate this check process and pass the alarm message back to an operating or maintenance center when a problem is detected.

Some digital relays collect breaker operation data, such as the number of operations and current interrupted for each operation. Many utilities are considering just-in-time breaker maintenance using breaker operation data to determine the need for breaker maintenance. However, breaker manufacturers are divided about the data that best indicates the need for breaker maintenance. Some say accumulated current, some say current squared, and some itemize the number of operations at several current ranges.

Collect the interrupted current for each operation and store it as a unique record to provide data for any of the breaker maintenance methods. Use substation integration techniques to download these data to a simple analysis program that calculates the need for breaker maintenance based on the manufacturer's recommended method.

Use substation integration techniques to synchronize device clocks in digital relays and other IEDs. Distribute time code to devices that accept IRIG-B and periodically send date and time commands to those devices that do not accept time code.

Filter relay status alarm messages from other equipment alarms, and either send the message to a maintenance office computer, or initiate a pager message using the dial-out process.

Improve Planning and Design Data

Most SCADA system data retrieval is limited by communication or central database constraints. Transmission and subtransmission system data typically does not include per-phase currents and voltages, so system current and voltage unbalance cannot be measured. Many SCADA systems do not include distribution substations, so these utilities are forced to rely on manual meter reading for transformer and feeder load data. Millions of dollars are spent each year for system expansion and modification based on these data.

Utilities have found that there are tremendous economies in better managed distribution systems, but better system management requires more complete metering. Many of these utilities have also found that adding distribution substation data and collecting per-phase currents, voltages, watts, and VARs create expense and problems. The addition or expansion of substation RTUs, addition of transducers and RTU analog input points, and added wiring are a tremendous expense. The additional data creates a tremendous burden on the SCADA system that slows response time and overloads central processing and database capability. Operating personnel and planning personnel become adversaries in the attempt to control SCADA system design and operation.

Data integration at the substation level offers a solution that satisfies both concerns. The minimum real-time data essential for system operation are passed to the SCADA system; more complete real-time and historical data are archived in substation files for periodic bulk transfer. The archived data can be accessed on demand, retrieved, or automatically offloaded at a convenient time, locally to a floppy disk or PC, or via modem to a remote site.

The substation database is a prime candidate to include in a Wide Area Network communication system that can share data and provide access from virtually any communication point within the system.

Complete data, including individual phase currents, voltages, watts, and VARs, and sequence currents and voltages are required to better understand the condition of a power system. A better understanding is the first step toward better management and efficient operation.

Use relay instantaneous phase, negative-sequence, and zero-sequence current and voltage quantities to monitor system unbalance.

Collect multiple data samples over time to monitor unbalance changes due to load and system changes. Check transmission system unbalance due to insufficient line transpositions. Adjust protection and control equipment settings to accommodate worst-case unbalance conditions, or use monitored quantities to adapt relay settings to system conditions.

Collect instantaneous and integrated demand data to create load profiles for planning analysis. Chart substation voltage profile versus load to check voltage regulation settings and capacitor bank switching schedules.

Time-tag integrated demand peak data, and chart high- and low-voltage excursions. Collect and correlate ambient and equipment temperature data from substation digital thermal devices.

Use substation data to monitor equipment operation and create data logs for reliability-based maintenance. Chart load tap changer positions and number of operations. Collect breaker and switch operation data.

TRANSFORMER PROTECTION [6025][85]

The following questions arise while applying a differential relay for transformer protection:

- What is the amount of fundamental and second-harmonic current that the relay sees while energizing the power transformer?
- What is the harmonic content of the excitation current under overvoltage conditions?
- Does zero-sequence current affect the performance of the differential element?
- What is the relay operating time?
- How secure is the relay for external fault conditions?
- How do I select the proper current transformers for my application?

- Are the current transformers going to saturate with high-fault currents?

Actual transformer testing is one of the options to answer these questions. The testing approach is time consuming and expensive. Transformer modeling is a more attractive and less expensive option to answer these questions. The transformer model simulates current signals for different operating and fault conditions. We apply these signals to the differential relay to analyze its performance. We validate modeling results with actual testing with a laboratory transformer.

In addition to transformer modeling and differential protection evaluation, we present a guide for selecting CTs (current transformers) to avoid misapplications of differential protection.

Current Differential Relay

The relay consists of three differential elements. Each differential element provides percentage restrained differential protection with harmonic blocking and unrestrained differential protection.

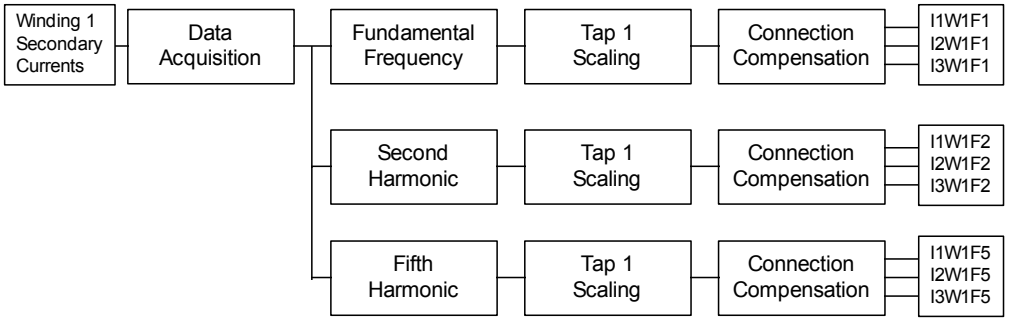


Figure 6.22: Data Acquisition and Filtering for Winding 1 Currents

Figure 6.22 shows the block diagram of the data acquisition and filtering sections for Winding 1 currents. The input currents are the CT secondary currents from Winding 1. The relay reduces the magnitude of these currents and converts them to voltage signals. Low-pass filters remove high-frequency components from the voltage signals. Digital filters extract the fundamental, second-, and fifth-harmonic quantities from the digital signals. The Tap 1 setting scales the signals in magnitude. After signal scaling, the relay removes the zero-sequence component of the input currents and compensates the transformer phase shift if required (Appendix 11.12.1 describes how the relay makes the transformer connection compensation). The Winding 1 compensated currents (I1W1F1, ..., I3W1F5) are the result of relay filtering, scaling, and connection compensation. The relay obtains the Winding 2 compensated currents (I2W2F1, ..., I3W2F5) in a similar way. The three differential elements use the compensated currents from Winding 1 and 2 as inputs to their logics. For example, the Differential Element 1 uses the compensated currents I1W1F1 and I1W2F1.

Figure 6.23 shows the block diagram of the differential and harmonic blocking elements. The relay provides percentage restrained differential protection with harmonic blocking. The harmonic blocking elements block the restrained differential elements when the settable harmonic percentage quantity is bigger than the operating quantity.

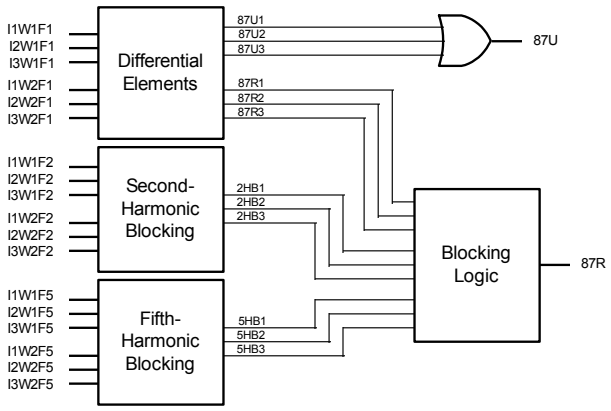


Figure 6.23: Differential and Blocking Elements

The magnitude of the vectorial sum of the compensated fundamental frequency currents determines the operating quantity of the restrained differential element. A settable percentage of the average of the magnitudes of the compensated currents determines the restraining quantity of this element. The relay compares the operating quantity to the restraining quantity. The percentage restrained differential element declares a tripping condition (87R element assertion) if the operating quantity is bigger than the restraining quantity and the minimum pickup level, and there is no harmonic blocking element asserted.

The relay calculates the second- and fifth-harmonic content of the differential current. It compares a settable percentage of the second- and fifth-harmonic magnitudes against the operating quantity. If the harmonic percentage is greater than the operating quantity, the harmonic blocking element asserts to block the percentage restrained differential element.

The blocking logic can operate in two ways: common harmonic blocking and independent harmonic blocking. In the common harmonic blocking mode, any harmonic blocking element (2HB1, ..., 5HB1) assertion blocks the three differential elements from operation. In the independent harmonic blocking mode, Harmonic Blocking Element 1 only blocks Differential Element 1. The first blocking mode gives higher security than the second blocking mode. In our applications, we selected the common harmonic blocking mode. The output (87BL) of the common harmonic blocking logic is the "or" combination of the harmonic blocking elements.

The unrestrained differential element compares the operating quantity against a settable threshold. If the operating quantity is bigger than the unrestrained element threshold, the relay declares a tripping condition (87U element assertion).

Differential Relay Performance

Differential Protection Performance While Energizing the Transformer

We tested the differential relay for different conditions upon transformer energization. We wanted to evaluate the performance of the differential elements. The transformer model simulated the input currents to the relay. Following is the relay performance for the no-fault, internal-fault, and external-fault conditions:

No-Fault Condition

Inrush currents compromise the security of differential relays. We do not want the differential relay to declare a trip condition while energizing an unfaulted transformer. The unrestrained and restrained differential elements respond to fundamental frequency only. The unrestrained differential element threshold must be set higher than the fundamental component of the highest expected inrush current. Otherwise, we must include a time delay to avoid unrestrained differential element (87U) misoperation under this condition. According to our testing results and harmonic analysis, the 87U threshold must be set above 9.0 sec. amps (71.9 pri. amps) to avoid 87U element assertion. The low-side CT ratio is 8. The typical setting for the 87U threshold is 8 times tap.

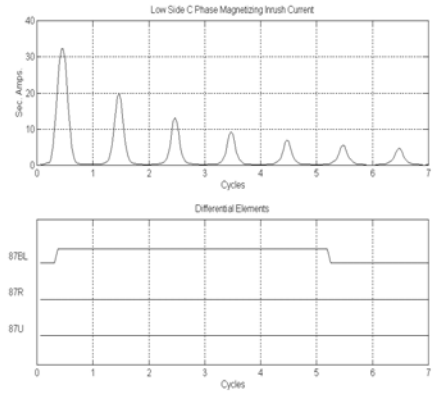


Figure 6.24: C-Phase Current While Energizing the 15 kVA Transformer Bank From the Low Side

The sensitivity of the restrained differential element (87R) is higher than the unrestrained differential element. The differential relay has to detect inrush currents and disable the 87R element. The differential relay uses a settable second harmonic to fundamental percentage to block the 87R element. This percentage must be set below 60% to detect the inrush current condition shown in Figure 6.24. This percentage can be smaller than 60% for other transformer applications or other energization conditions. From transformer modeling and utility experience, the typical setting is 15 percent. Figure 7 shows the second-harmonic content as percentage of fundamental of this inrush current.

The purpose of this test was to verify that the relay second-harmonic blocking element disables the restrained differential element, and the unrestrained differential element (87U) does not assert. The single-phase transformer bank connection was wye-wye. The CT connections were wye at both sides of the transformer bank. We used the same transformer and CT connections for all the performed tests. Figure 6.24 shows the inrush current shown in Figure 6 in sec. amps and the 87BL, 87R, and 87U elements. The 87BL element asserts to block the restrained differential element right after the transformer energization, and the unrestrained element does not assert. The 87BL element remains asserted until the operating quantity is below the relay pickup level.

Internal-Fault Condition

What is the relay operating time for internal faults? We simulated an internal C-phase-to-ground fault in the low side of the transformer bank upon transformer energization. Figure 6.25 shows high-side C-phase fault current in secondary amps and the 87R element assertion. The high-side CT ratio is 4. The 87R element asserts in approximately 1.5 cycles to clear the fault.

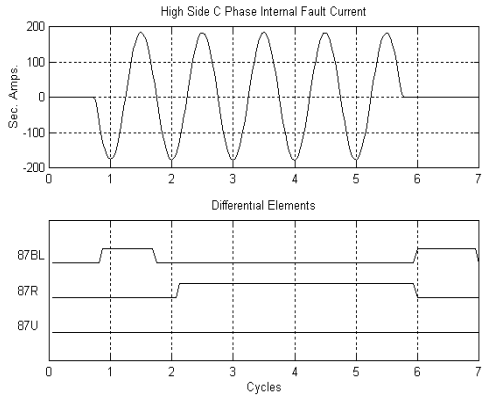


Figure 6.25: Restrained Differential Element Asserts in Less Than 1-1/2 Cycles to Clear the C-Phase-to-Ground Internal Fault

External-Fault Condition

How secure are the differential elements for out-of-section faults? We simulated an external C-phase-to-ground fault at the low side of the transformer bank upon transformer energization. Figure 6.26 shows high- and low-side C-phase secondary currents. The currents are 180° out of phase as expected for external fault conditions. The differential elements did not assert.

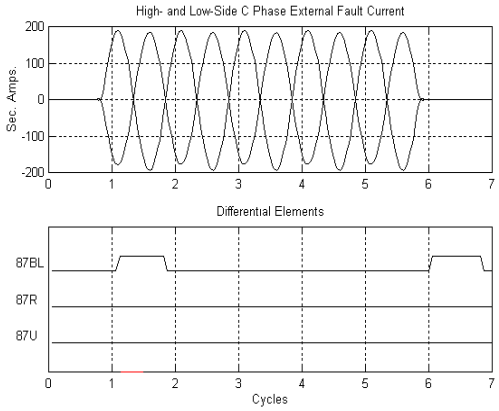


Figure 6.26: High- and Low-Side C-Phase Currents for an External C-Phase to Ground Fault. None of the Differential Elements Assert for the External-Fault Condition

Selecting CTs Used With Differential Relays

In transformer differential applications, CTs are selected to accommodate a maximum fault current and, at the same time, to preserve the low current sensitivity. As a minimum goal, CT saturation should be avoided for the maximum symmetrical external fault current. The CT ratio and burden capability should also permit operation of the differential instantaneous element for the maximum internal fault. The transformer application shown in Figure 6.27 presents a low external fault current but is complicated by the possibility of an extremely high internal fault current. The problems and solutions of this application will be made clear with simulations using CT models.

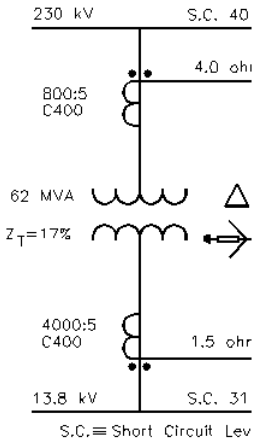


Figure 6.27: 62 MVA Transformer Protection Application. High-Side Short Circuit Level: 40 kA

High-Side CT Selection

A CT selection procedure is given in the forthcoming PSRC publication "Guide for the Application of Current Transformers Used for Protective Relaying Purposes." The following step-by-step procedure is given for selecting the high-side CT:

Step 1	Select the high-side CT ratio by considering the maximum high-side continuous current I_{HS}. The choice of the CT ratio should ensure that at maximum load the continuous thermal rating of the CT, leads, and connected relay burden is not exceeded. For delta connected CTs, the relay current is $\square$ times the CT current. Let this ratio be the nearest standard ratio higher than I_{HS}/I_N, where I_N (relay nominal current) is 5 A or a lower value determined by the relay tap setting.
Step 2	Determine the burden on the high-side CTs.
Step 3	For the high-side CT ratio, select the CT accuracy class voltage that will exceed twice the product of the total high-side CT secondary burden and the maximum symmetrical CT secondary current, which could be experienced due to an external fault. If necessary, select a higher ratio than that indicated in Step 1 to meet this requirement. For the maximum internal fault, the CT ratio and burden capability should permit operation

	of the differential relay instantaneous unit.

From Step 1, the load current I_{HS} is 156 amps and indicates a high-side CT ratio of 200:5 for wye-connected CTs to produce a suitable relay current of 3.9 amps. The 17 percent transformer impedance limits the external high-side fault current to 917 amps. From Step 3, the calculated burden voltage is (917 amps / 40) (4 ohms) = 92 volts. The CT accuracy class exceeding twice this voltage is C200. The excitation curve for the C200, 200:5 CT is plotted in Figure 16. The curve shows that the rated voltage (at 10 amps of excitation current) is typically twice the excitation of the maximum permeability (located by the 45° tangent to the curve). Consequently, the burden voltage for the maximum external symmetrical fault current operates the CT at a point of maximum permeability and least error.

Figure 6.28: C200, 200:5 CT Excitation Curve

The rating is aimed at preserving sine-wave operation for symmetrical faults. It also produces a significant degree of saturation during asymmetrical faults. The magnetizing current caused by CT saturation for external fault conditions appears as differential current in the relay. However, as shown in Figure 17????, the relay detects the second-harmonic content of the magnetizing current and restrains differential relay tripping.

Step 3 then states that for the maximum internal fault, the ratio and burden capabilities should permit operation of the differential instantaneous unit. With a 40,000 amp internal fault current, the 200:5 CT is inadequate by inspection, and a new selection criteria is needed. In this case, the CT model will be used in conjunction with a simulation of the microprocessor digital filter algorithm to verify the operation of the instantaneous element. To preserve the current sensitivity, the CT ratio is increased to 800:5 to provide approximately one amp of secondary current at full load. The simulation of the 40,000 amp internal fault is shown in Figure 18????. The simulation shows the fundamental content of the saturated

secondary current. With the instantaneous trip threshold set at 8 times tap, the trip level is reached in less than 1 cycle.

Low-Side CT Selection

A low-side CT ratio of 4000:5 provides an adequate current of 3.25 amps at full load. The burden voltage for the maximum internal fault of 16,000 amps is (16000 amps / 800)(1.5 ohms) = 30 volts. Avoiding CT saturation for the maximum asymmetrical fault requires a voltage rating of (1 + X/R) times the burden voltage for maximum symmetrical fault conditions, where X/R is the reactance-to-resistance ratio of the primary circuit. This criteria is met for an X/R ratio of 12 with a C400 rating as shown in the following calculation:

$$V_{rating} = \left(1 + \frac{X}{R}\right) V_{burden} = 13 \bullet 30 = 390 \qquad \text{Equation 6.3}$$

The CT ratings now provide adequate low-current sensitivity, prevent saturation on external faults, and ensure operation on extremely large internal fault currents.

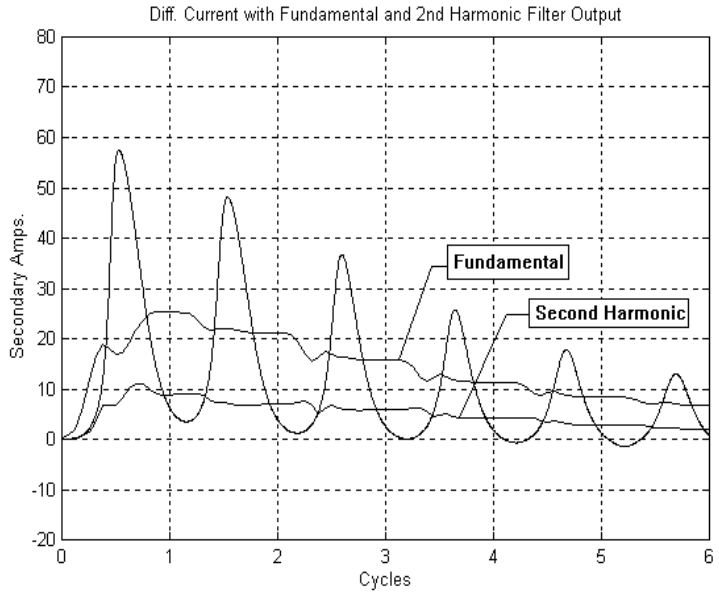


Figure 6.29: Difference Current Caused by Magnetizing Current

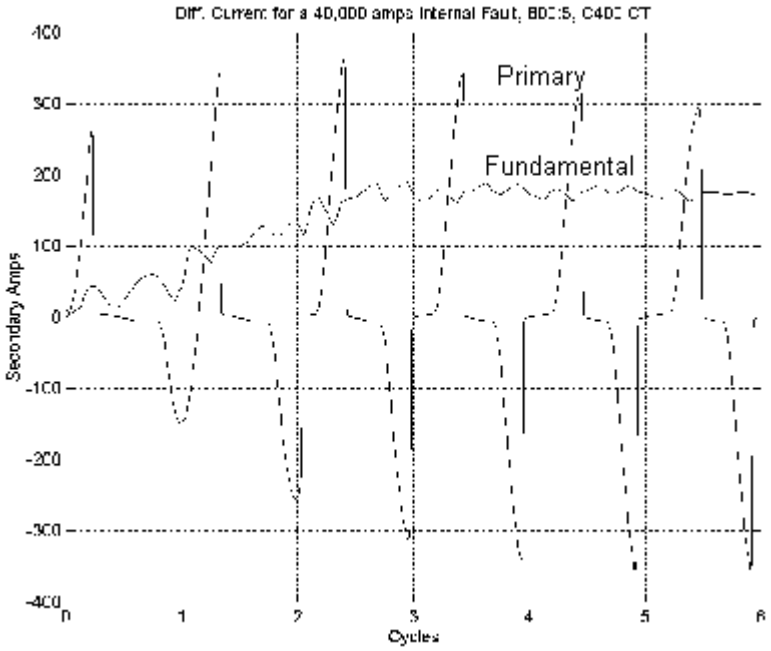


Figure 6.30: Secondary Current for a C400, 800:5 CT with 40,000 A

Transformer Differential Example

Figure 6.31 shows a 4160 volt power plant auxiliary bus supplied by a 5000 kVA delta-wye resistance grounded transformer. The transformer has a 4.95 percent impedance on a 5 MVA base and is fed by a standby and an emergency bus. The bus is protected by phase and ground directional overcurrent relays and the transformer is protected by percentage differential relays with harmonic restraint and a ground overcurrent relay fed by a CT in the transformer neutral.

A rating C-200, 1200:5 was selected for the low side cts and a C-200, 600:5 rating for the high-side CTs. The taps for the 87T relay were set at 2.9 amps for the high side winding and at 8.7 amps for the low-side winding leaving a ratio mismatch of 4.4 percent. The percentage differential for tripping was set at 25 percent.

The complication in this application is in the fact that the 600:5 CTs are located 1400 feet from the switchgear, requiring at least 2800 feet of leads. Only 25 feet of leads were required for the 1200:5 CTs mounted in the switchgear with the relay. The long run was installed with paralleled No. 10 gauge wire, which has a calculated resistance of 3.36 ohms, including the totally resistive relay burden. The 1200:5 CT was installed with a calculated total burden of 0.365 ohms. The maximum through-fault current was calculated as 12,312 amperes on the 4160 bus (3711 amperes at 13.8 kV) with an X/R ratio of 11.

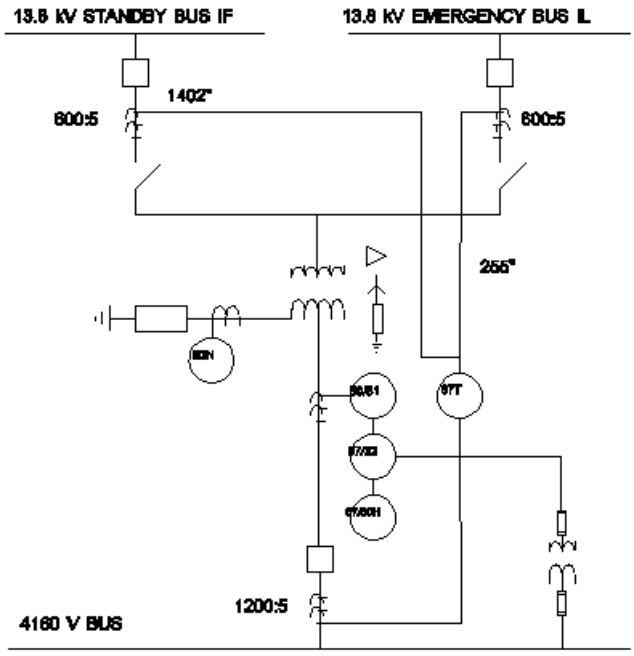


Figure 6.31: Power Plant Auxiliary

In the low side 1200:5 CT, the maximum symmetrical secondary fault current of 51.3 amperes flowing in the total burden of 0.365 produces 18.72 volts. This voltage multiplied by (X/R+1)=12 gives 225 volts. Consequently, the low-side CT can support undistorted asymmetrical ratio current in the secondary. In the 600:5 CTs, a maximum symmetrical fault current of 30.9 amperes flowing in the total circuit burden of 3.4 ohms produces 105 volts or about half the 200-volt accuracy rating. These CTs, therefore, are adequately rated by the accepted rules. However, their core will saturate with asymmetrical fault current. Since only one set of CTs will saturate, relay-operating current will persist for asymmetrical faults.

The implications of this arch-typical application are shown by the computer simulation of Figure 9????. The upper graph shows the time plot of saturated 600:5 CT secondary current with the unsaturated 1200:5 CT secondary current. This lower plot shows the large difference current that decays with the dc transient. The plot is literally the magnetizing current during saturation caused by the asymmetry. It has the same wave shape and is caused by the same phenomenon as the inrush current of the power transformer itself. Figure 10 is a plot of the harmonic content obtained from a Fast Fourier analysis of the difference current. The magnitudes of the harmonics are plotted in per unit of the fundamental. The analysis shows typical values of 173% dc component, 49% second harmonic, 62% fifth harmonic, and 153% sixth harmonic. As it turns out, the second and fifth harmonics are high enough during the offset that a differential relay with harmonic restraint units will restrain the relay from operating. Thus, the two times knee-point voltage rule-of-thumb is adequate for this application.

Concluding Remarks about Differential Current Transformer Protection

Power transformer modeling is an economical way to analyze transformers for different operating conditions. Using the Frolich Equation in the transformer model provides enough accuracy for differential protection evaluation purposes. Transformer models without hysteresis modeling reduce model complexity and minimize simulation time. Better understanding of the harmonic content in the inrush current leads to improved settings of the unrestrained differential element, second-harmonic blocking element, and overcurrent element.

A fifth-harmonic level detector can identify overexcitation conditions to block the differential element, to assert an alarm, or to trip a breaker. Adequate CT selection leads to proper transformer protection applications. Digital current differential relays provide fast and reliable transformer protection. These relays give feedback for the different transformer operating conditions, feedback that was not previously available to the relay user.

Transformer Thermal Protection

General Thermal Modeling Concepts

By definition, an overcurrent relay produces an inverse time-current characteristic by integrating a function of current F(I) with respect to time. The F(I) is positive above and negative below a predetermined input current called the pickup current. Pickup current is the current at which integration starts positively, and the relay produces an output when the integral reaches a predetermined set value. The F(I) represents the velocity of an induction disk and the integral represents its travel. Figure 6.32 shows the overcurrent relay represented as an analog circuit. The disk travel is represented by a voltage V. The function is $F(I) = I^2 - 1$ which produces an extremely-inverse characteristic where I is the input in per units of the pickup current.

Figure 6.33 shows a thermal model represented by an analog circuit. The voltage V in the thermal model represents the temperature rise in $I^2 t$ above an initial temperature V_t. In Figure 2, V has a steady state value for every value of input current and a trip is asserted only if V exceeds the trip threshold T_{hr}. The threshold is set at the limiting temperature of the protected element. By contrast, in Figure 1, the voltage V has no steady state and rises to exceed the trip threshold $k\Theta$ for any $I > 1$ and resets to zero for any current $I < 1$. The overcurrent trip time is set by means of a time dial that increases the travel by modifying factor k. The thermal model trip time is determined by the time constant $R_T C_T$, which is set to equal the thermal time-constant of the protected element.

Figure 6.34 shows that an overcurrent characteristic can emulate the shape of the thermal characteristic and can be closely coordinated with it. However, Figure 6.35 shows that the coordination is valid only for the initial temperature V_0 equal to 1 per unit. When a temporary overload raises the temperature, V_0 increases and the time to reach the damaging temperature decreases as shown in Figure 6.35. Therefore, during a recurring overload, the damaging temperature occurs before the overcurrent relay can operate. In addition, the coordination prevents the use of the added thermal capacity available when temperature V_0 is less than 1.0.

Consequently, only the thermal model can account for thermal history and accurately track the excursions of conductor temperatures.

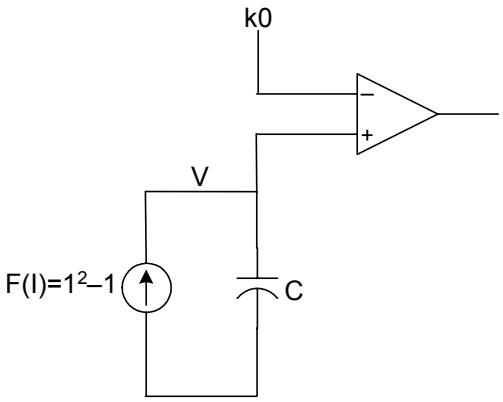


Figure 6.32: Analog of an Overcurrent Relay

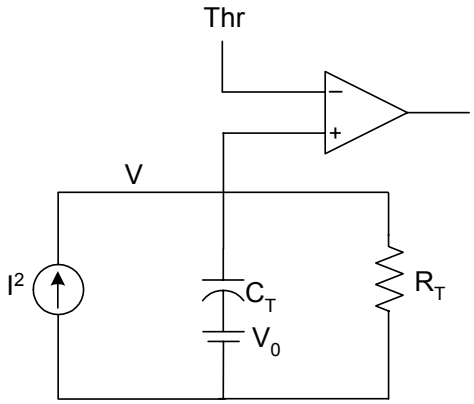


Figure 6.33: Analog of a Thermal Model

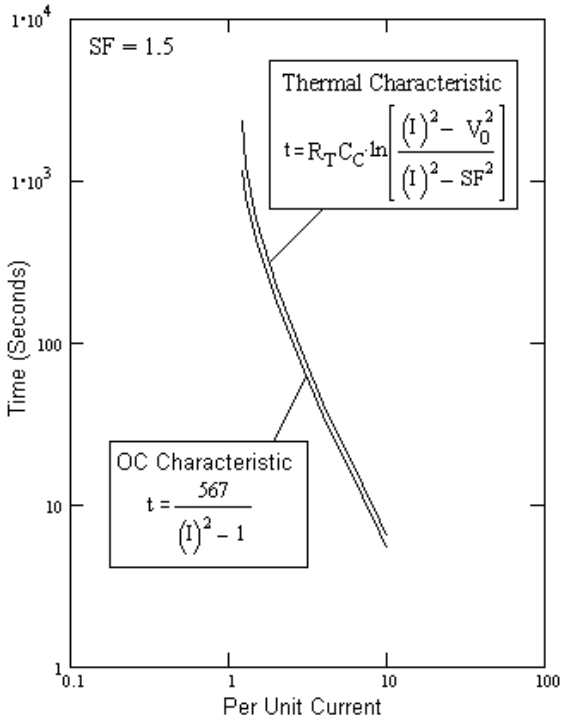


Figure 6.34: Overcurrent Coordination With a Thermal Characteristic

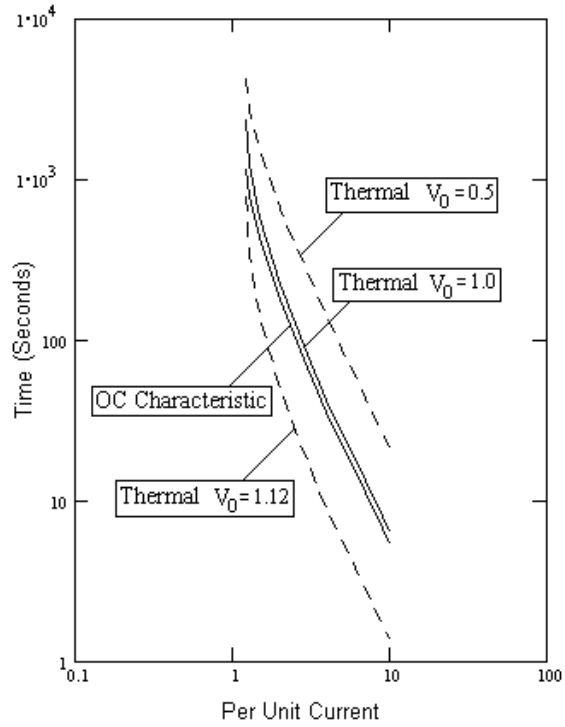


Figure 6.35: Thermal Characteristic Variation With Initial Condition V_0

Transformer Thermal Model

The transformer thermal model satisfies the requirements specified in ANSI standard C57.92- 1995 [3] to provide transformer overload protection. The model consists of two exponential equations and non-linear time-constants determined from transformer data. The thermal model calculates the following temperatures shown in Figure 6.36 for reference:

θ_o Top-oil rise over ambient temperature, °C

θ_g Hottest-spot conductor rise over top-oil temperature, °C

θ_{hs} Hottest-spot winding temperature, °C

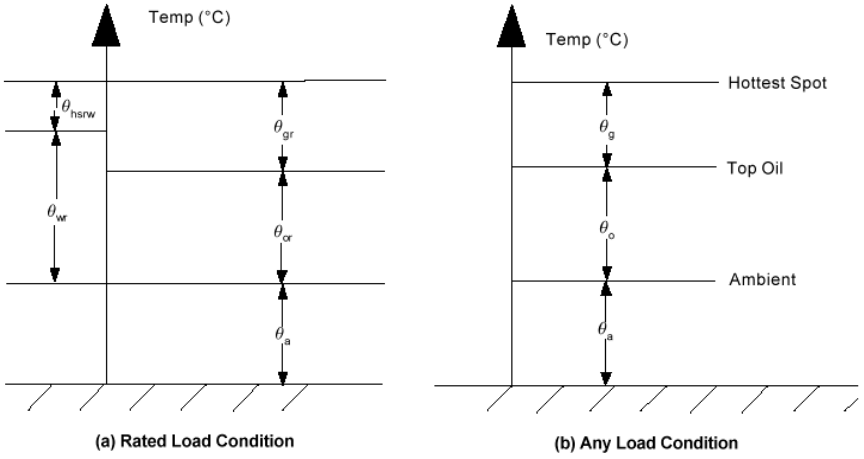


Figure 6.36: Transformer Temperatures for Different Load Conditions

Top-Oil Rise Over Ambient Temperature, θ_o

When a constant load is applied throughout the time interval Dt, the model calculates the top-oil rise over ambient temperature at the end of the interval, according to the following expression:

$$\theta_o = (\theta_{ou} - \theta_{oi}) \bullet \left[1 - e^{\frac{-\Delta t}{60 \bullet T_o}}\right] + \theta_{oi} \qquad \text{Equation 6.4}$$

where:

θ_{ou} Ultimate top-oil rise over ambient temperature for any load, °C

$\theta_{.oi}$ Initial top-oil rise over ambient temperature at start time of interval, °C

T_o Oil time constant of transformer, in hours

The increment Δt defines the time interval between calculations. The recommended interval is 10 minutes.

Ultimate Top-Oil Rise Over Ambient Temperature

The model calculates the ultimate top-oil rise over ambient temperature due to constant loads according to the following expression:

$$\theta_{ou} = \left[\frac{\left(K^2 \cdot R + 1\right)}{\left(R + 1\right)}\right]^n \cdot \theta_{or} \qquad \text{Equation 6.5}$$

where:

K Load expressed in per unit of transformer nameplate rating according to the cooling system in service (maximum phase current divided by the nominal current)

R Ratio of load loss at rated load to no-load loss

n An empirically derived oil exponent

θ_{or} Top-oil rise over ambient temperature at rated load, °C

The following expression determines the thermal top-oil time constant of the transformer for any n (oil exponent accounting for viscosity change with temperature) value and for any load value:

$$T_o = T_r \cdot \left[\frac{\frac{\theta_{ou}}{\theta_{or}} - \frac{\theta_{oi}}{\theta_{or}}}{\left(\frac{\theta_{ou}}{\theta_{or}}\right)^{\frac{1}{n}} - \left(\frac{\theta_{oi}}{\theta_{or}}\right)^{\frac{1}{n}}}\right] \qquad \text{Equation 6.6}$$

where:

T_R Thermal time constant at rated load with initial top-oil temperature equal to ambient temperature

If the T_R time constant is not known, the following expression determines the time constant:

$$T_r = C \cdot \left(\frac{\theta_{or}}{P_r}\right) \qquad \text{Equation 6.7}$$

where:

C Transformer thermal capacity (watt-hours/degree)

= 0.06×(weight of core and coil assembly in pounds)

+ 0.04×(weight of tank and fitting in pounds)

+ 1.33×(gallons of oil)

or

C Transformer thermal capacity (watt-hours/degree)

= 0.0272×(weight of core and coil assembly in kilograms)

+ 0.01814×(weight of tank and fitting in kilograms)

+ 5.034×(liters of oil)

PR Total loss at rated load (watts)

The model adds the ambient temperature, θ_a, to the top-oil rise over ambient temperature, θ_o, to obtain the top-oil temperature, θ_{ro}. The top-oil temperature at the end of the time interval, Δt, is:

$$\theta_g = \left(\theta_{gu} - \theta_{gi}\right) \cdot \left(1 - e^{\frac{-\Delta t}{60 \cdot T_{hs}}}\right) + \theta_{gi} \qquad \text{Equation 6.8}$$

where:

θ_{gu} Ultimate hottest-spot rise over top-oil temperature for any load K, °C

θ_{gi} Initial hottest-spot rise over top-oil temperature at start time of interval, °C

T_{hs} Winding time constant of hottest spot, in hours

Ultimate Hottest-Spot Rise Over Top-Oil Temperature

The model calculates the ultimate hottest-spot rise over top-oil temperature due to constant loads according to the following expression:

$$\theta_{gu} = K^{2m} \cdot \theta_{gr} \qquad \text{Equation 6.9}$$

where

m An empirically derived winding exponent

Θgr Hottest-spot conductor rise over top-oil at rated load, °C

Hottest-Spot Conductor Rise Over Top-Oil at Rated Load

When the transformer manufacturer does not provide the hottest-spot conductor rise over top-oil at rated load, you can calculate it as follows:

$$\theta_{gr} = \theta_{wr} + \theta_{hsrw} - \theta_{or} \qquad \text{Equation 6.10}$$

where:

θ_{wr} Average winding temperature rise over ambient temperature at rated load, °C

θ_{hsrw} Hottest-spot conductor rise over average winding rise, °C

Hottest-Spot Winding Temperature

When a constant load is applied throughout time interval Dt, the relay calculates the hottest-spot winding temperature at the end of the interval, according to the following expression:

$$\theta_{hs} = \theta_a + \theta_o + \theta_g \qquad \text{Equation 6.11}$$

Thus it takes two exponential expressions, thermal capacitance and times constants, calculated using transformer nameplate and test data, to determine the hottest-spot temperature under a specified load. The model is given in clause 7 of the standard and is based on top-oil temperature as a starting point. An alternative, more accurate, model is given in Annex G of the ANSI standard using bottom-oil temperature as a starting point. This model, although more accurate for large transient loads, presents a difficulty in that only top-oil temperature is available from most manufacturers. Annex G introduces duct oil temperature that may be higher than top-oil temperature, giving a true hottest-spot located in the duct.

Table 6.3: Exponents Used in Temperature Equations

Type of Cooling	m	n
OA	0.8	0.8
FA	0.8	0.9
Nondirected FOA or FOW	0.8	0.9
Directed FOA or FOW	1.0	1.0

BUS PROTECTION

Bus configurations

Ring bus

Breaker and a half

Main/Auxiliary

Double main

Fault types

Three-phase

Phase-to-ground

Phase-to-phase

Phase-to-phase-to-ground

Bus Protection Relays

Differential Relays

Low-Impedance Relays

High-Impedance Relays

Partial-Differential Directional

BREAKER PROTECTION

Malfunctioning of the mechanical system may prevent the PCB main contacts from following trip or close initiation, or a malfunction may move the main contacts into a partially open position, allowing the fault, load, or line charging current to flow through the preinsertion resistor. The development of new breaker failure relay was based on past experience with violent equipment failures since 1968, recent EMTP studies, and new capabilities offered by microprocessor based relays. The statistics for violent equipment failures of the 500 kV air blast PCB's were grouped into six general categories, as shown in Table 1 below.

Table 6.4: Violent Equipment Failure Summary for 500 kV Air Blast PCBs

Problems	Percentage of Failures
Operating mechanism malfunction during the close Cycle one interrupting head remains open.(Damage due to restrike occurs after the other poles on the same phase close. The other two poles close successfully.)	32%
Trip or close preinsertion resistor failure main contact in one pole remains partially open. (Current flows through the resistor until the resistor chamber explodes.)	28%
Operating mechanism malfunction during the trip-cycle one interrupting head remains closed. (Damage due to restrike occurs on the open poles of the same phase. The other two phases open successfully.)	16%
Violent CT/PT failure. (Can be detected to prevent failure.)	8%
Contamination of air/oil conduits. (Can be detected to prevent failure.)	8%
PCB air system violent failure. (Sudden pressure loss can be detected after the failure.)	8%

The table makes it clear that most of the disasters experienced were due to mechanism failures or malfunctions. A breaker failure relay should detect these failures, and others, and take corrective action.

Circuit Breaker Operation and Failure

Consider the operation of a power circuit breaker from the point of view of the state diagram of Figure 6.37. Circles represent "states" the breaker occupies throughout its operation. Lines represent the state transitions, or paths, by which the breaker changes state. States are assigned with physical significance to the breaker mechanisms. External stimuli (e.g. trip or close commands) or internal actions (e.g. successful close) cause the state of the breaker to change.

The breaker normally operates by moving around the state diagram in a counter clockwise direction. If the breaker is in the OPEN state, and its close coil is energized, the mechanism of the breaker begins to move. To accommodate the time taken by the physical processes of closing resistor operation and main contact operation, the CLOSING state is defined. A successful close leaves the breaker in the CLOSED state. If the trip coil is energized, then the mechanism begins to move again, opening the main contacts, and possibly opening one or more trip resistor contacts. This interruption process takes place in the OPENING state. A successful trip leaves the breaker in the OPEN state.

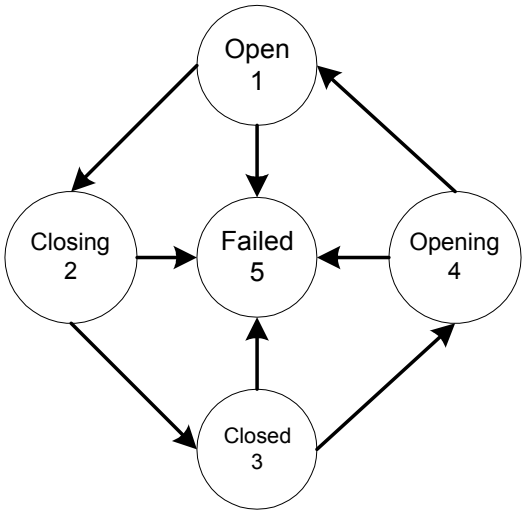


Figure 6.37: Circuit Break State Diagram

Breaker failure could occur in any state, leading to the FAILED state, shown in the center of the diagram. This diagram helps identify the ways a circuit breaker can fail. Once these are identified, we can find electrical means of detecting these failures. Since the means of protection are state dependent, it makes sense to design a breaker failure relay that determines the state of the circuit breaker from external features, and applies the protection appropriate to that state. Before discussing the means of detecting failures, we need to identify as many possible failures as we can.

Failure to Trip

Failures to trip can occur for fault conditions, load conditions, or no current conditions. Failures can occur in one or more main contacts, or in the resistor contacts. The failures can involve one, two, or all three poles.

Failure to Close

Close failures include one or more poles remaining open or partially open.

Failure while Open

Flashover across open contacts is a possible failure of an open circuit breaker.

Failure while Closed

A fully closed breaker is unlikely to fail.

Insulation Failures to Ground

Circuit breaker bushings, supports, and other related apparatus could fail, resulting in ground faults. These faults are detected by either the bus protection or the line protection, and need not be included in a breaker failure relay.

Other Failures

Failures may also occur in the control wiring, compressors, pressurization, and other auxiliary apparatus. Although many of such failures are handled by alarms or breaker control schemes, the breaker failure relay must tolerate these failures when possible.

Breaker Protection

Failure to Trip – Current Leads Trip (Mode A1)

Figure 6.38 shows a circuit breaker with four heads per pole, where two poles remain closed after tripping under fault conditions. The two open heads flashed over, thereby maintaining fault current through the circuit breaker of the failed pole.

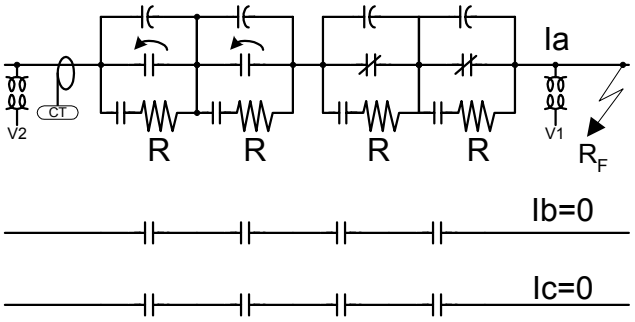


Figure 6.38: Failure to trip during Fault conditions (Mode A1 or A2)

Figure 6.39 shows the logic diagram for a scheme which is initiated when the fast pickup/dropout element A1:50 picks up, followed by the assertion of the TRIP input. After initiation, if the current does not allow the A1:50 to drop out, the timer A1:62 expires, and tripping results. Current is required to lead trip in this mode, to distinguish it from the A2 mode, which involves sequential clearing.

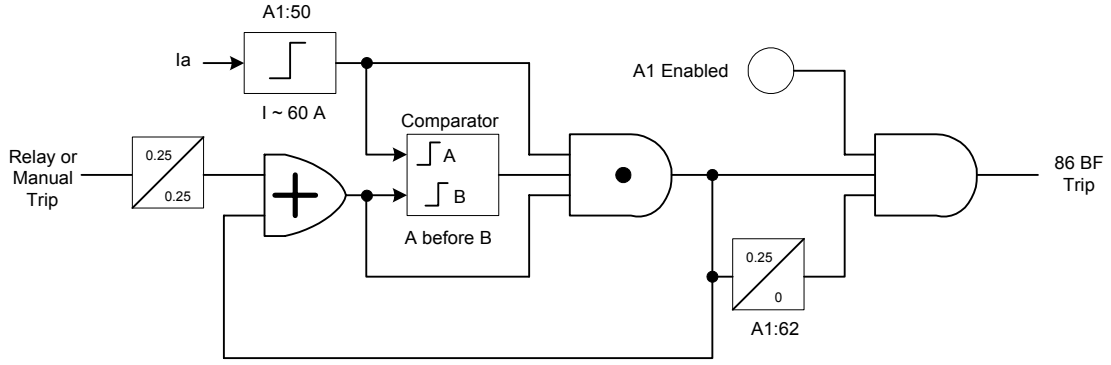


Figure 6.39: A1 Mode Breaker Failure Logic (failure to trip)

Failure to Trip – Trip Leads Current (Mode A2)

In a ring bus, for example, the current into the line passes through two breakers in parallel. The current division between the two breakers is not generally predictable. Therefore, enough fault current to pick up the A1:50 element may only begin to flow through one breaker when the other breaker opens, if the breakers share the current unevenly.

Suppose the breaker with the initially weak current fails to trip. The BFR first receives the trip signal. Next, the overcurrent element A1:50 picks up. The logic shown in Figure 6.40 detects this condition. It is identical to the A1 logic scheme, except for the B before A sense of the comparator.

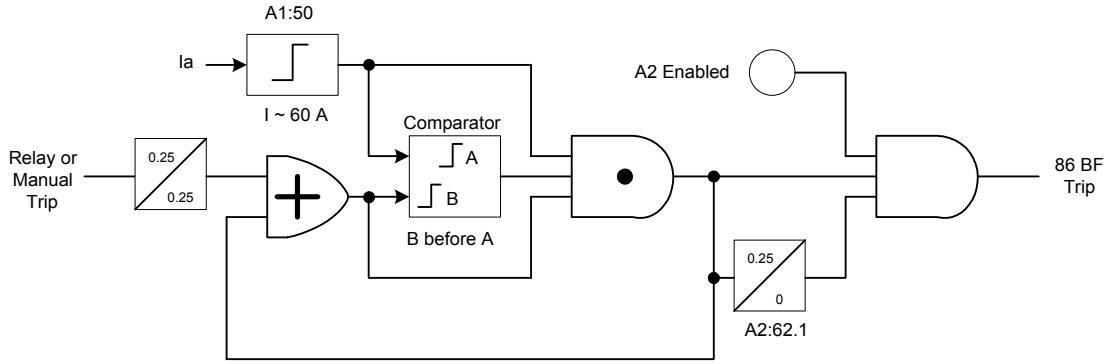


Figure 6.40: A2 Mode Breaker Failure Logic (sequential failure trip)

Timer A2:62:2 is common to both schemes, to ensure that A1 or A2 initiates for any fault causing the A1:50 to pick up. Timer A2:62:1 can be set shorter than the corresponding A1©scheme timer A1:62, since the sequence B before A indicates the relay is late in obtaining current. System stability benefits from the shorter time setting, as it reduces the fault duration for this type of breaker failure.

Failure to Trip – Resistors Stuck Closed (Mode A3)

When one or more resistors remains inserted following a trip, the fully open heads are not likely to withstand the added voltage stress, and will flash over. Current due to charging, load or a fault continues to flow, and the temperature of the resistors rises at a rate proportional to the power input to the resistors. Eventually, the resistors may be destroyed. Figure 6.41 shows one pole of a circuit breaker with two stuck resistors and two heads flashed over.

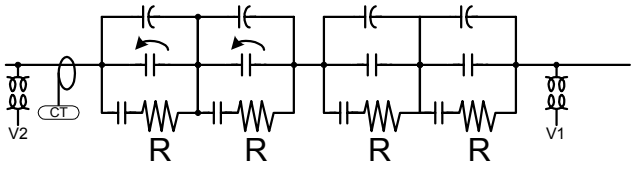


Figure 6.41: Trip Resistors Remain Inserted (Mode A3)

Figure 6.42 shows the logic of a scheme that detects this failure. The trip resistor thermal model accepts inputs of the current through the breaker and the voltage across the breaker and computes power into the trip resistor. The single node thermal model estimates the thermal energy stored in the resistor, and includes cooling to ambient with a settable time constant.

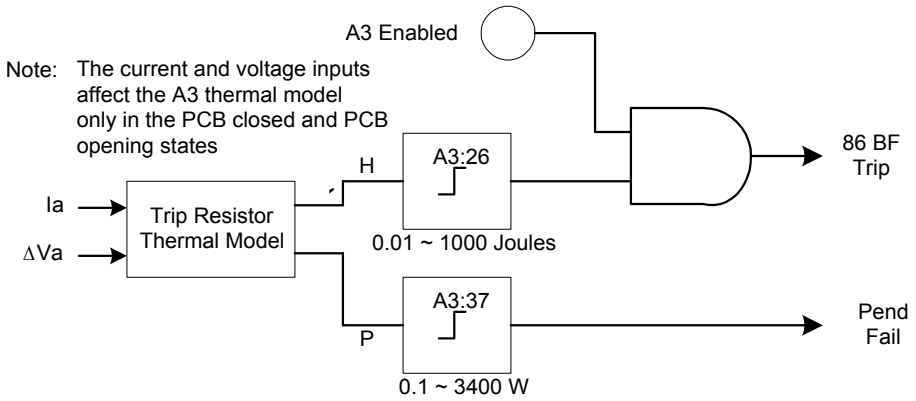


Figure 6.42: A3 Breaker Failure Logic (trip resistor failure)

Tripping occurs when the energy stored in the resistor exceeds the A3:26 setting. The scheme does not depend on any breaker failure initiate inputs. Security is enhanced by requiring the A3:59 overvoltage, A4:50, and A3:37 elements to all pick up before heating is allowed. The A3:37 pickup value is the product of the overvoltage and overcurrent elements.

A1 through A3 Failure Mode Relay Settings

Set the A3:59 overvoltage element to pick up for the product of the minimum resistance and minimum current. Minimum current may be chosen to be charging current. The setting should be maintained above the uncertainty in the differential voltage measurement across the breaker.

The A4:50 overcurrent element should be set to pick up for the minimum current expected.

The thermal limit for the tripping resistors is the basis for the setting of the A3:26 element. For example, if the maximum thermal stress of the ceramic resistors is 700 joules per cubic cm, and each disk has 225 cubic cm of ceramic material, and there are 44 disks per resistor, with two resistors per head, the maximum thermal stress per head is 13.86 MJ. A setting of about 12 MJ provides some derating.

The cooling time constant can be estimated as one-third the time to cool from maximum temperature to near ambient temperature. A time constant of one hour might be expected.

Note that the A3 scheme depends on the availability of voltage across the breaker, i.e. potential devices must be available on both sides of the breaker if the A3 scheme is to be used.

Failure to trip with charging Current Flowing (A4)

The trip failure shown in Figure 6.38 could occur when tripping for load or charging current, i.e. current insufficient to initiate the A1 or A2 schemes. Although such a trip failure probably does not pose much risk to the system, it indicates a potentially dangerous situation.

Figure 6.43 gives the logic for this sensitive scheme. It is initiated by trip in the presence of minimum current. A long time delay would normally be applied for security.

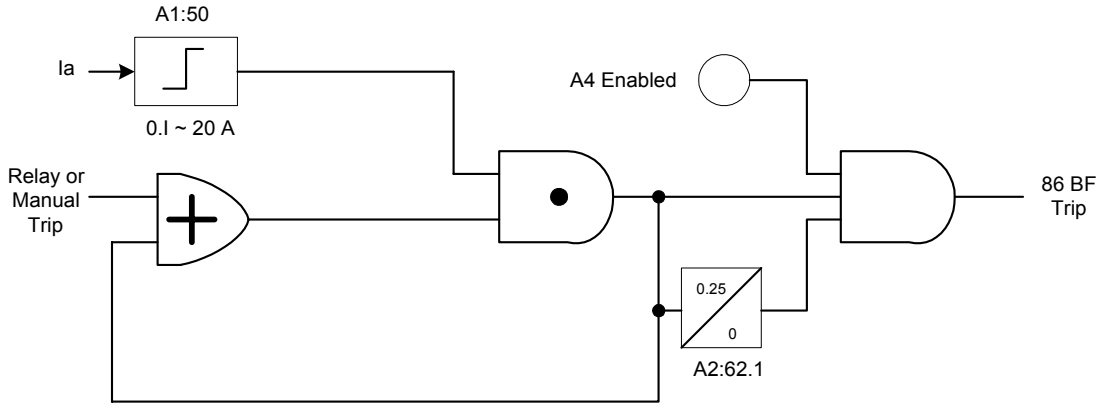


Figure 6.43: A4 Mode Breaker Failure Logic (sensitive failure to trip)

Charging current is about 3.5 A per mile at 500 kV. The A4:50 element may be set down as low as 0.1 A secondary. With 2000/5 CTs, this implies a line at least 12 miles long draws sufficient charging current to pick up this element.

Due to the relative magnitudes of the line-charging impedance and typical tripping resistors, stuck resistors have negligible effect on the charging current. Therefore, this scheme provides some backup to the stuck-resistor thermal scheme (A3), especially valuable when the differential-voltage measurement is not available. Two failure to-close schemes are required, one for heads stuck open and the other covers stuck closing resistors.

Failure to Close, Heads Stuck Open (B1)

Figure 6.44 shows one pole of a circuit breaker that has partially closed. Assuming that the open heads do not flash over, the condition can be detected by current unbalance, as shown in the block diagram of Figure 6.45 for pole A.

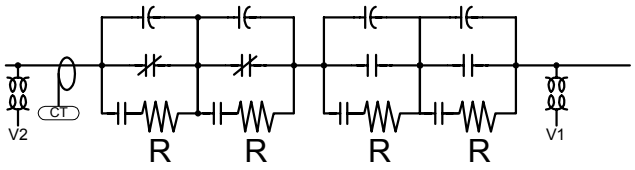


Figure 6.44: Failure to Close - Heads Stuck Open (Mode B1)

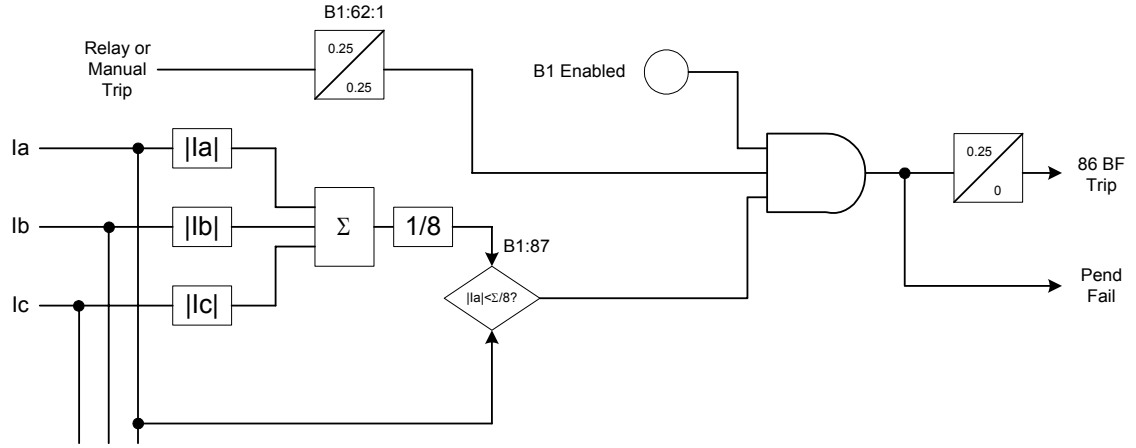


Figure 6.45: B1 Mode Breaker Failure Logic - Heads Stuck Open

Current unbalance is checked for during a time window defined by timer B1:62:1, initiated by any close signal. When the currents are balanced, the magnitude of each equals 1/3 of the magnitude sum of the three phases. If the current in any pole is less than 1/8 the magnitude-sum current (i.e. less than 3/8 of the expected value), then the currents are declared unbalanced. In the time window just after closing, one cause of this is an open pole. Another cause of current unbalance after closing is a fault. Thus the time window must be chosen, by the timer settings, to exclude switch-into-fault possibilities immediately after closing the breaker.

Failure to close – Heads Practically Stuck Open (B2)

A failure similar to Figure 6.44, where a closing resistor is switched in, but the main contact fails to short it out, leaves current flowing through the resistor. Figure 6.46 shows the logic for a thermal scheme which is identical to the A3 trip-resistor thermal scheme, except for its settings and when power into the breaker drives it.

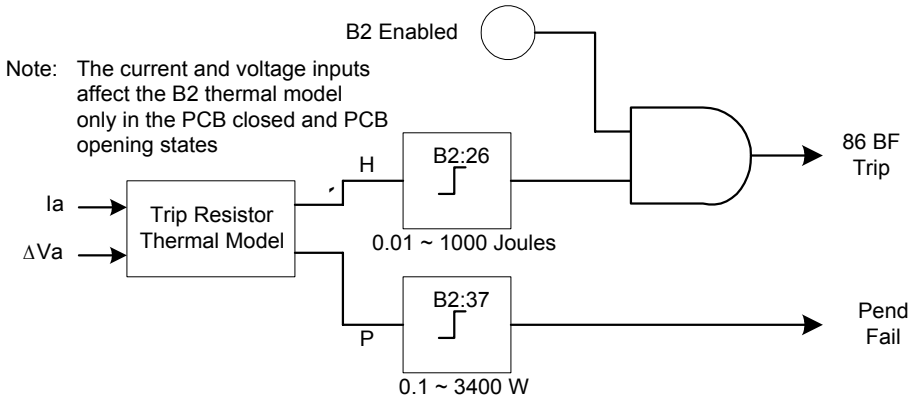


Figure 6.46: B2 Mode Breaker Failure Logic (close resistor failure)

The trip-resistor model is driven whenever the breaker is closed or opening, whereas the close-resistor model is driven whenever the breaker is open or closing. Thus the

relay has six resistor thermal models: one for tripping and one for closing in each of the three poles.

Current Flowing while Breaker is Open

When the circuit breaker is open, the flow of current in any pole indicates a failure. The E1 scheme detects this failure. For security, the scheme is only enabled when the voltage across the pole in question is above 67 volts per phase secondary, i.e. greater than one per-unit. RMS voltages greater than 1 pu occur during synchronizing and out-of-step events.

The N:50 element sets the sensitivity of the scheme. It is designed for sensitivity and security at the expense of speed, as pickup and dropout times are not critical. The remaining logic in Figure 6.47 ensures that the scheme is applied only when the breaker is truly open; not when it is opening or closing.

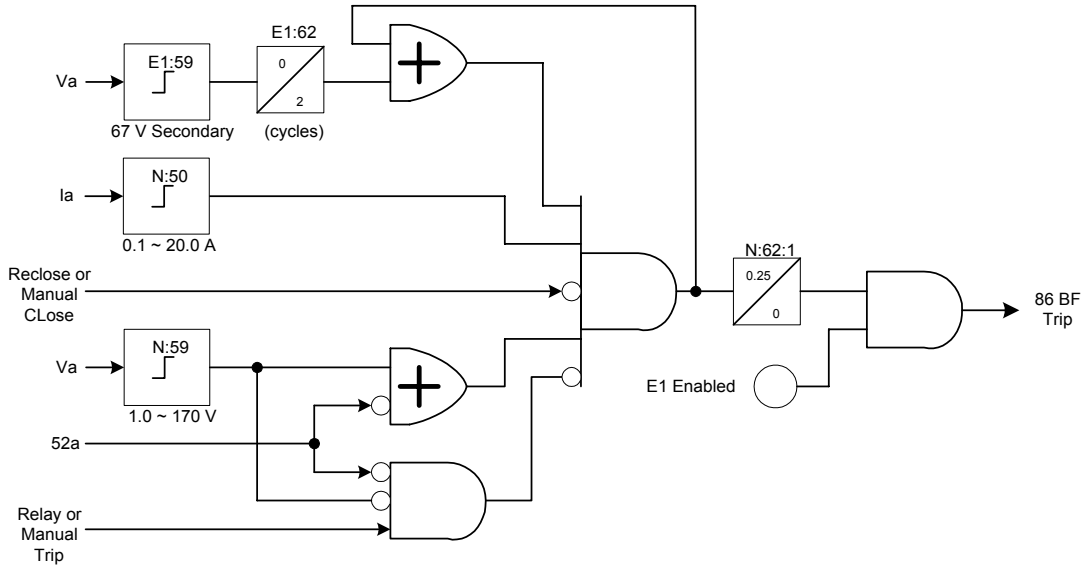


Figure 6.47: Failure Mode E1 (current while open) Logic

Control Logic

Logic is provided to trip the 86BF lockout relay, to trip motor-operated disconnect (MOD) switches after the failed breaker is successfully isolated, and to reset the 86BF lockout relay, readying the system for restoration. Figure 6.48 and Figure 6.49 are the block diagrams for this logic.

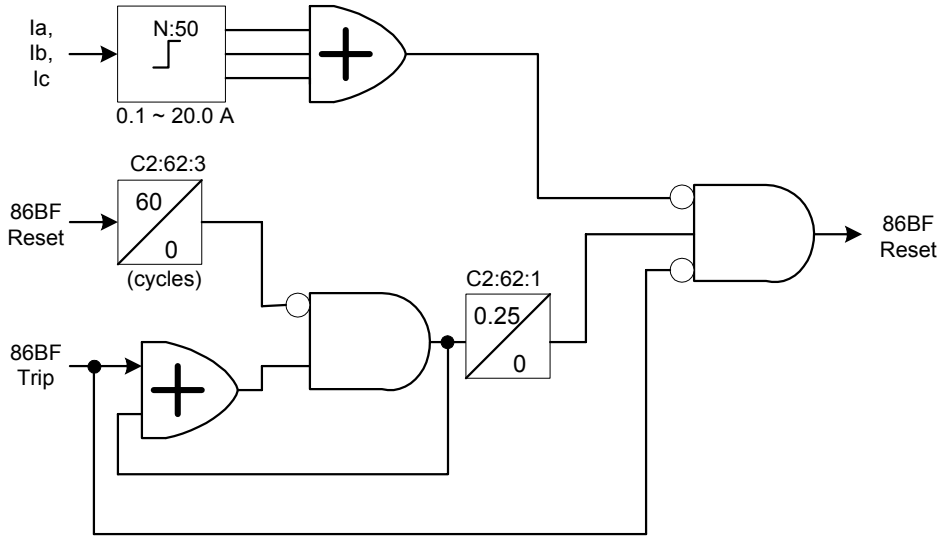


Figure 6.48: 86BF Reset Logic (C2 disabled)

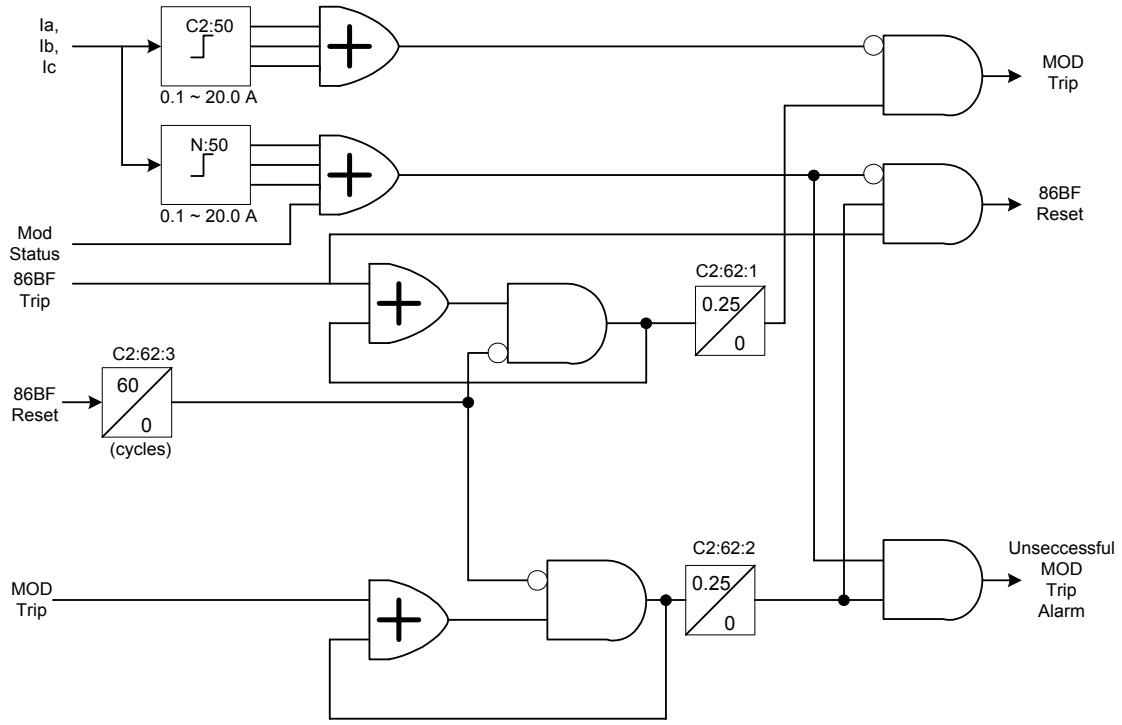


Figure 6.49: 86BF Reset and MOD Trip Logic (C2 enabled)

Two general courses of action are involved, depending on the setting for the C2 ENABLE. Figure 6.48 applies when C2 is disabled; Figure 6.49 applies when C2 is enabled. When the C2 scheme is disabled, the only control provided by the C2 scheme is automatic 86BF reset. The 86BF RESET output asserts when the following three conditions for the three-input AND gate in Figure 6.48 are met:

- No current is flowing (all three C2:50 elements are dropped out).

- The 86BF TRIP condition is expired.
- The 86BF TRIP timer (C2:62:1) expires, indicating that the set time has passed since the 86BF trip occurred.

The 86BF RESET output remains asserted until the C2:62:3 timer expires one second later. When the C2 scheme is enabled, Figure 6.49 applies, allowing automatic isolation by tripping the MODs. The 86BF RESET output is now controlled by the output of the three-input AND gate of Figure 6.49. The normal sequence of events for this logic is as follows:

- The MODs are tripped when little or no current flows (all three C2:50□ elements are dropped out), and the 86BF TRIP timer (C2:62:1) expires.
- The 86BF RESET output asserts when the MOD STATUS input indicates that the MODs have opened, as long as the currents stay below the N:50□ pickup setting, and the MOD TRIP timer is still running.

Breaker Failure Relay State Machine Design

Figure 6.50 is the breaker failure relay state diagram. Eight states and the associated protection are identified:

Table 6.5: Breaker Failure State Machine State Description

S	Name	Purpose	Protection
0	Restart	Determines breaker state at startup	Non required
1	Open	Monitors close and failure while open	B2, E1
2	Closing	Monitors closing process	B1, B2
3	Closed	Monitors trip and failure while closed	A3, A4
4	Opening	Monitors opening process	A1 - A4
5	Bus Clearing	Monitors successful bus clearing	C1
6	MODs Isolation	Monitors successful isolation by MODs	C2
7	PCB Isolated	Monitors MOD closure to allow restart	C3

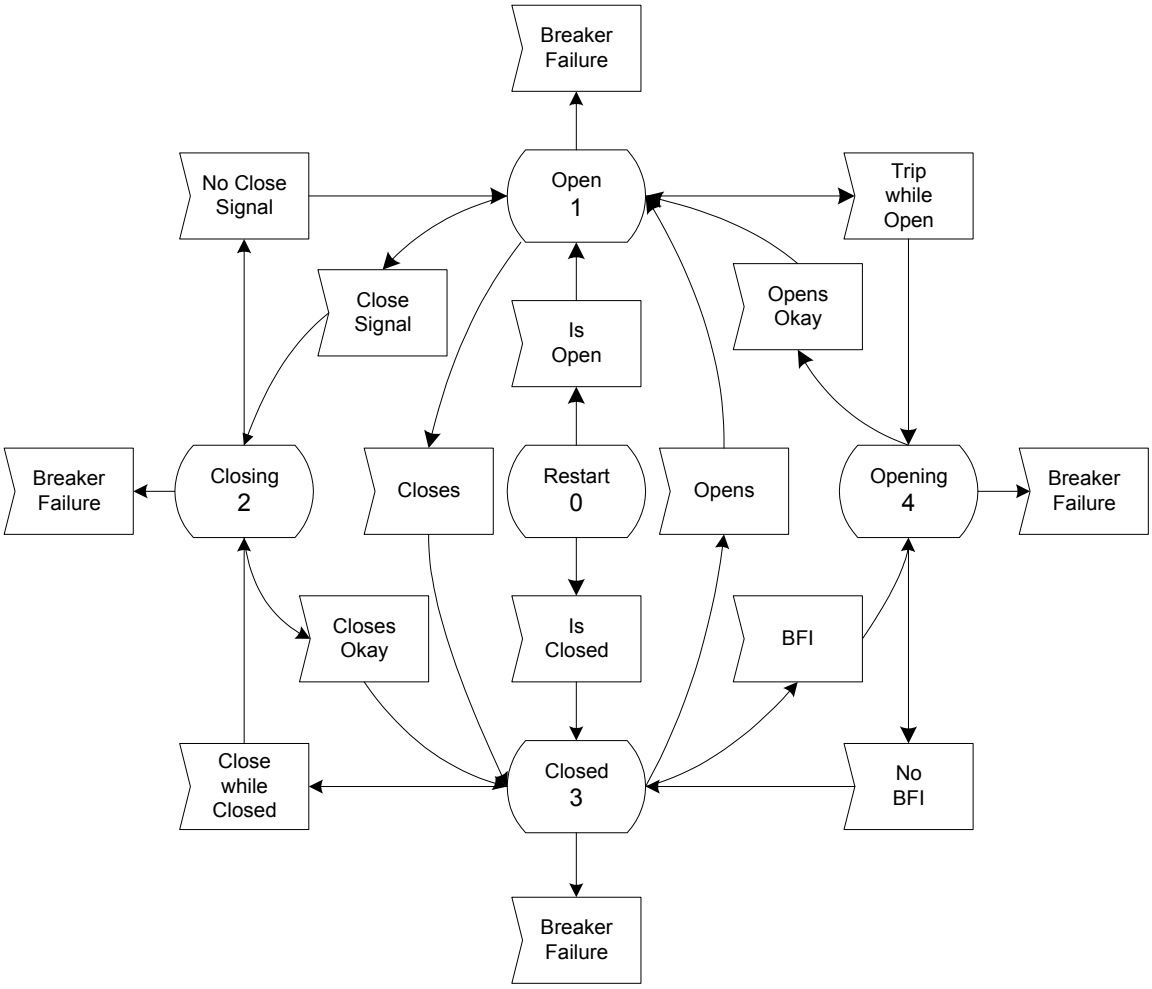


Figure 6.50: Breaker Failure Relay State Machine Diagram

The protection scheme notation is summarized below:

- A1: Current-leads-trip failure to trip scheme
- A2: Trip-leads current failure to trip scheme
- A3: Trip resistor thermal protection
- A4: Sensitive failure to trip scheme
- B1: Open-head failure to close scheme
- B2: Close resistor thermal protection
- C2: Control logic
- E1: Current-while-open protection

The protective relay elements are:

- A1:50 Fast pickup/dropout overcurrent element for A1, A2 fast schemes

- A3:59 Overvoltage element for trip and close resistor thermal protection
- A3:26 Trip resistor heat energy (temperature) detector, with settable cooling time constant (RTC)
- A4:50 Sensitive overcurrent element
- B2:26 Close resistor heat energy (temperature) detector, with settable cooling time constant (RTC)
- C2:50 MOD/86BF RESET sensitive overcurrent element
- N:50 86BF RESET and current-while-open sensitive overcurrent element (same as E1:50)
- E1:59 1 p.u. supervisory overvoltage element for current-while-open scheme
- 47Q Negative-sequence overvoltage unit for loss-of-potential scheme

More states are included in the relay than in the breaker itself (Figure 6.37), to accommodate startup and to control the lockout relay. The main counterclockwise loop shown in Figure 6.37, through states 1-2-3-4, remains. The relay has a transition directly linking CLOSED to OPEN to handle protection without fault-current trip initiation. The transition directly linking OPEN to CLOSED handles closing operations when the relay does not receive a close input.

Single-Pole Tripping

Proper Out-of-Step Blocking or Tripping (OSB/T) following a single-pole trip is extremely difficult. Out-of-Step (OOS) conditions are commonly generated after a single-pole trip in weak areas of the power system. The detection of a power swing during the single-pole open period is more difficult since unbalance is present during load flow through the two unfaulted phases. Some manufacturers choose to disable OSB during the single-pole open period. This paper demonstrates new techniques that properly detect a power swing during the single-pole open period.

Another common practice (typically when all three poles are closed) is to inhibit OSB upon detection of negative-sequence current; i.e., an unbalanced fault has occurred. Coordination with adjacent distance protection is compromised if OSB is halted immediately.

OSB should detect when a power swing evolves into a three-phase fault. This paper describes a technique that properly detects a three-phase fault after OSB has been asserted.

The trajectory of the impedance measured by a distance relay during a power swing does not have a constant velocity. However, many manufacturers use two distance characteristics (inner and outer) to measure the rate of the swing; i.e., the time measured for the trajectory to travel from the outer to the inner characteristic. Typically, constant velocity is assumed. This paper demonstrates a novel technique that accounts for acceleration.

Open-Pole Logic

Most manufacturers choose to inhibit power swing blocking during the open-pole period following a single-pole trip. This is due to the fact that detection of unbalance current is generally used to remove an OSB since this indicates a fault has occurred. Since an open pole generates unbalance current, this condition automatically disables power swing blocking. Unfortunately, power swings typically occur in weak areas of the power system due to the single-phase fault. Unwanted tripping of the remaining two phases due to a power swing (since OSB is inhibited) defeats the purpose of single-pole tripping. Therefore, if power swing blocking is disabled during an open-pole period, then the distance relay cannot distinguish between an actual swing and a fault on one of the two remaining phases.

An algorithm has been developed and fully tested that can distinguish between a power swing and a fault during the open-pole period following a single-pole trip. The phase and ground distance elements are blocked by the OOS logic during the open-pole period. The angular difference between the measured I_0 and I_{a2} is used to defeat OSB in case the fault occurs during the open-pole period.

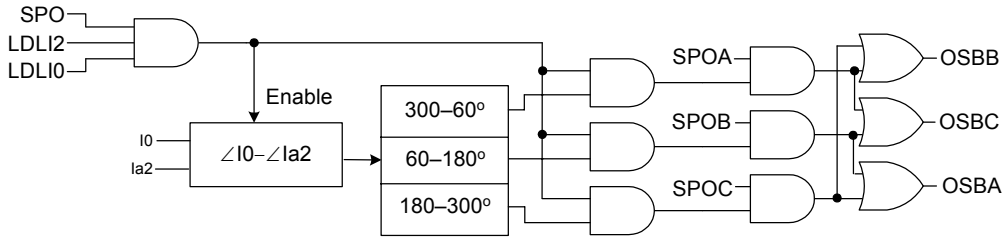


Figure 6.51: Open-Pole Ground Distance OSB Logic

SPO	Single Pole Open
SPOA	Single Pole Open, Phase A
SPOB	Single Pole Open, Phase B
SPOC	Single Pole Open, Phase C
LDLI2	Low-set negative-sequence current level detector
LDLI0	Low-set zero-sequence current level detector
OSBA	Assisted Out-of-Step Block, Phase B or C Open
OSBB	Assisted Out-of-Step Block, Phase C or A Open
OSBC	Assisted Out-of-Step Block, Phase A or B Open

Observe Figure 6.51. When a single-pole open condition is detected and unbalance current flows through the two unfaulted phases ($3I_0$ and $3I_{a2}$), then the Open-Pole OSB logic is enabled. Zero-sequence and negative-sequence current flowing due to load are in-phase, even during a power swing, when Phase A is open. The following equations show this relationship:

$$I_a = 0,\ Ib = 1\text{p.u.}\angle -120°,\ Ic = 1\text{p.u.}\angle -120°, \qquad \text{Equation 6.12}$$

$$I_{a0} = 0 + Ib + Ic = -1pu \angle 180° \quad \text{Equation 6.13}$$

$$I_{a2} = 0 + a^2 Ib + aIc = -1pu \angle 180° \quad \text{Equation 6.14}$$

$$\angle I_{a0} = \angle I_{a2} \quad \text{Equation 6.15}$$

This relationship ceases to exist when a fault occurs on one of the two remaining phases. A fault is detected when the angular difference falls outside the range 60° - 300° and Phase A is open (see Figure 6.52). The internal relay elements OSBB and OSBC are then deasserted.

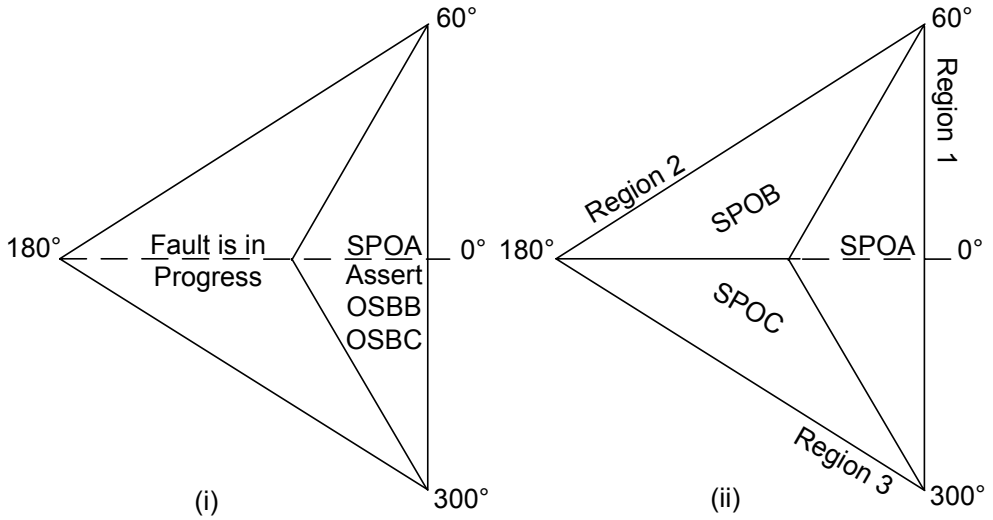


Figure 6.52: Open-Pole Ground Distance OSB Regions

Figure 6.53 illustrates how OSBA, OSBB, and OSBC are used to assist OSB during a single-pole open condition. OSB1 indicates Block Zone 1 during an OOS condition. When all three poles are closed, the normal OSB logic is executed. However, when a single-pole open condition is detected, then this additional logic is required. Should OSBA (because of SPOB or SPOC), OSBB (because of SPOA or SPOC), or OSBC (because of SPOA or SPOB) assert during the single-pole open condition, then the appropriate ground distance elements are blocked if an OSB is in progress. No settings are required for this logic.

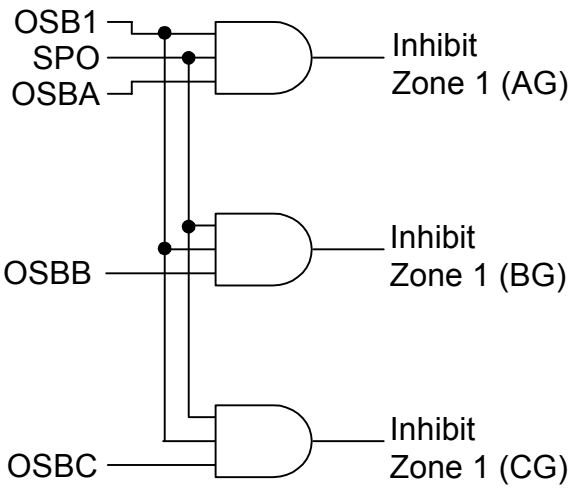


Figure 6.53: Open-Pole Ground Distance Unblock OSB Logic

6.3.1.1 Negative-Sequence Current Unblocking

Inhibiting OSB if negative-sequence current is detected during a power swing is a normal practice. This practice enables the affected phase distance elements to clear any phase fault that occurs during the OOS condition. Unfortunately, this presents a coordination problem with adjacent protection when the fault is out-of-section.

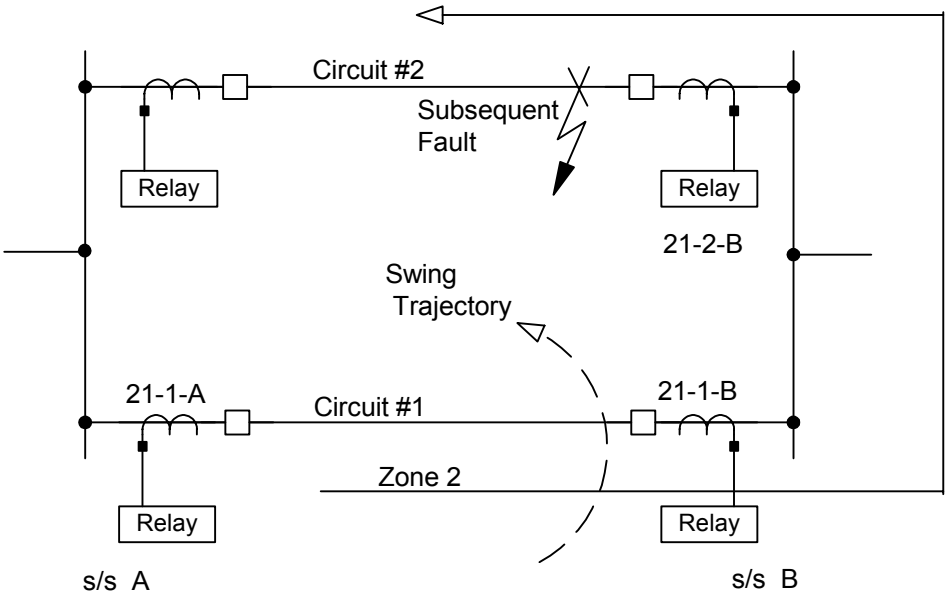


Figure 6.54: Out-of-Section Fault During OSB

Figure 6.54 shows a permissive overreaching transfer tripping scheme as the main protection for Circuit 1. Suppose that a power swing passes through the forward-looking zones of Distance Relay 21-1-B. Initially, the overreaching zone is inhibited by OSB. An unbalanced fault then occurs on Circuit 2. Distance Relay 21-1-A can overtrip since the OSB for Distance Relay 21-1-B is immediately unblocked by the presence of negative-sequence current; i.e., 21-1-A sees the fault on Circuit 2 before

the forward-looking zone of 21-1-B drops out. Figure 6.55 is a timing diagram that illustrates this race.

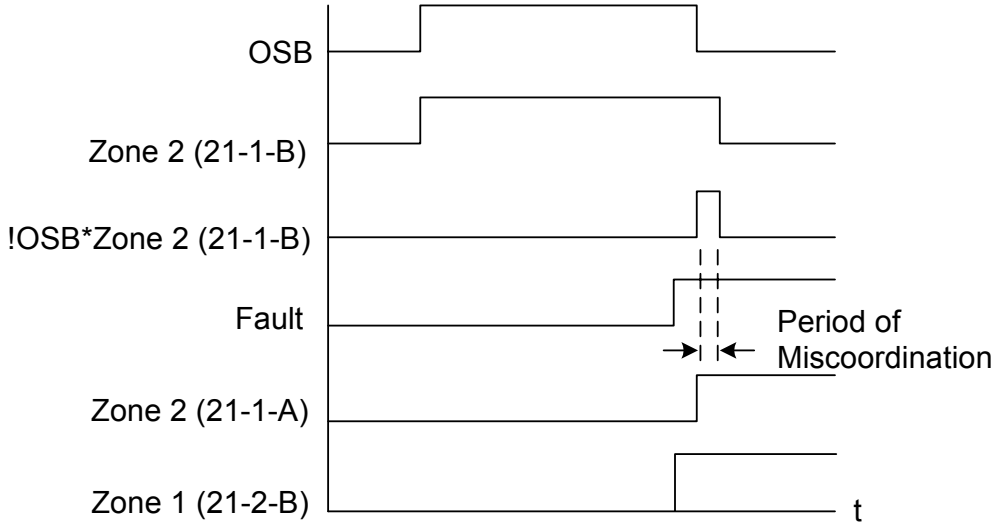


Figure 6.55: OOS Timing Diagram

Time delay on pickup prior to unblocking OSB allows Distance Relay 21-1-A to remain coordinated with the adjacent Distance Relay 21-2-B. Please refer to Figure 6.56. The unblock is delayed until after Zone 1 of Distance Relay 21-2-B has cleared the fault. UBD indicates a time delay on pickup prior to unblock.

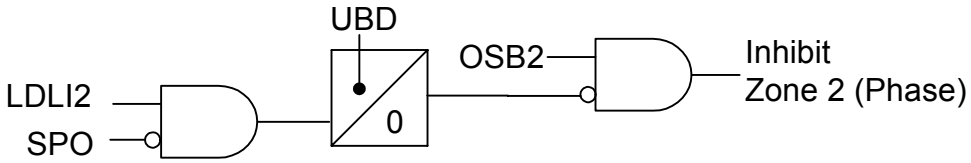


Figure 6.56: Negative-Sequence Unblocking Delay

6.3.1.2 Inner Blinders

Power swings and three-phase faults involve all three phases of the power system. The distance relay cannot simply use the measured impedance (e.g., positive-sequence impedance) alone to determine whether or not the phase distance protection should be inhibited or allowed to trip.

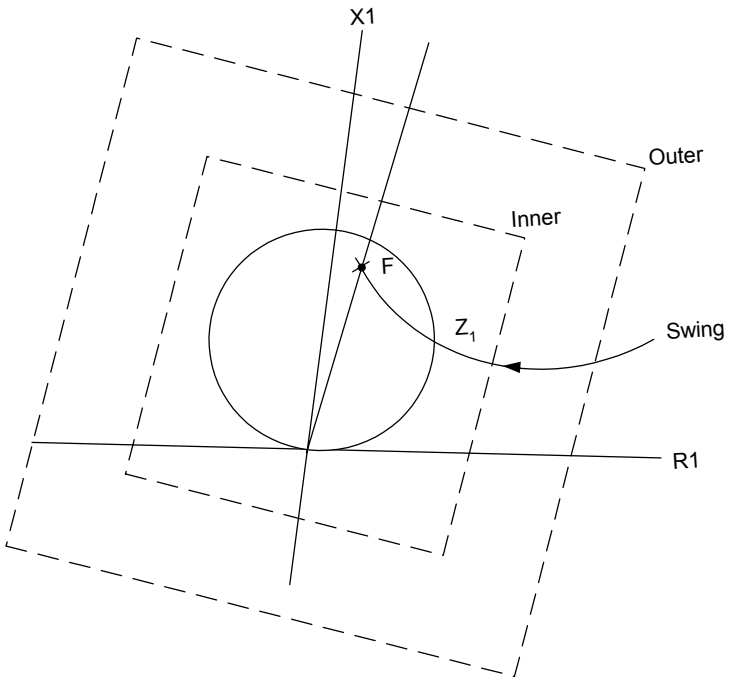


Figure 6.57: Power Swing Evolves into Three-Phase Fault

A critical distinction between three-phase faults and power swings is the rate-of-change of Z_1. The rate at which the measured Z_1 changes for a power swing is much slower than that of a three-phase fault. However, when concentric distance characteristics are used to detect a power swing, after OSB has been asserted, this logic cannot detect an evolving three-phase fault. See Figure 6.57.

When a three-phase fault occurs during a power swing, Z_1 moves to the line angle and remains there until the fault is cleared. By detecting that Z_1 remains static within a prescribed region during a measured amount of time (t_{RL}), the distance relay can detect that the power swing has evolved into a three-phase fault. The prescribed region is that area on either side of the line angle.

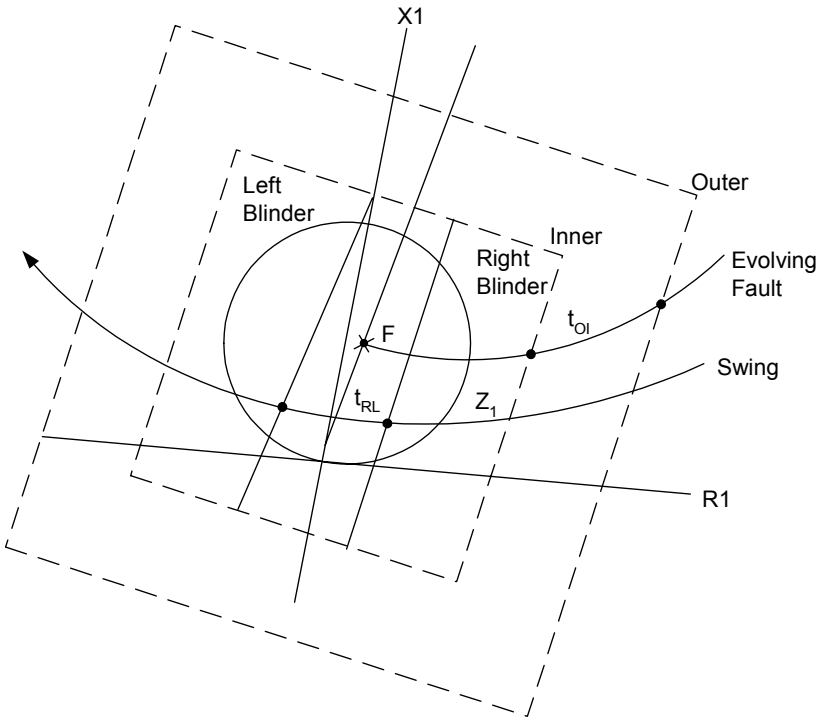


Figure 6.58: Inner Blinders

If Z_1 remains between the inner blinders and the inner characteristic for a certain amount of time (t_{RL}), then OSB is unblocked, and the phase distance protection trips.

6.3.1.3 Adaptive Timer

If indeed a three-phase fault has occurred, then the period of time required for Z_1 to pass through the inner blinders (t_{RL}) is slower than the time predicted after it passes through the concentric distance characteristics (t_{OI}). During a fast swing, a short delay is sufficient before OSB is unblocked, but a long delay is required for a slow swing! Therefore, the timer used to measure the period required for Z_1 to pass through the inner blinders (t_{RL}) should be adaptive.

The adaptive timer should always be long enough that when a slow swing passes through the inner blinders, the relay can distinguish that a three-phase fault has not occurred. However, a short delay provides quick clearance for an evolving three-phase fault following a fast swing.

The adaptive timer measures the period required for Z_1 to pass from the outer to inner distance characteristic (t_{OI}) in order to determine the time delay required before OSB is de-asserted. This period of time is directly proportional to the slip frequency of the power swing. A short time delay (t_{RL}) is possible for fast swings since it is proportional to the time required for Z_1 to pass from the outer to inner distance characteristic (t_{OI}).

Power swings generated by faults typically begin with a slow slip frequency that gradually increases. **Error! Reference source not found.** shows the current measured by a distance relay following a single-phase-to-ground fault.

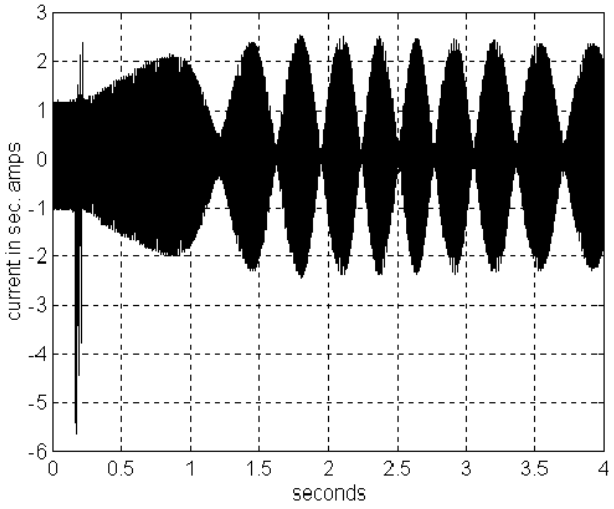


Figure 6.59: Slip Frequency for Single-Phase Fault

The fault occurs within the first half second of the captured event. The slip frequency of the ensuing power swing is superimposed on the fundamental (50 Hz) frequency of the current waveform following the disturbance. The swing is relatively slow up to the first second and then rapidly increases. If a fixed timer is set for a long time delay in order to accommodate the initial slow swing, then fast clearance is sacrificed if an evolving three-phase fault occurred later during the fast swing.

Error! Reference source not found. illustrates how an adaptive timer determines the time delay prior to unblocking for various rates of swing.

PER JEFF R THE PICTURE THAT WOULD BE HERE IF MSWORD HAD ITS ACT TOGETHER IS "JUST WRONG" AND NEEDS TO BE REDRAWN????

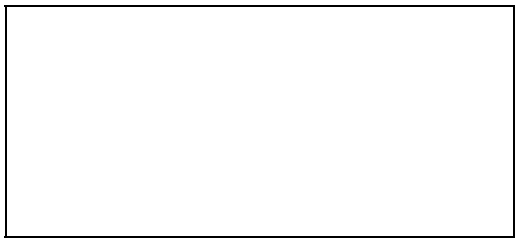


Figure 6.60: Adaptive Timer Measurement

ANOTHER ???? - - - THIS NEXT PART MAKES NO SENSE AND NEEDS TO BE REWRITTEN

$t_{RL} = \alpha \ t_{OI}$

where

α is a function of the inner and outer blinder settings, OSBD timer setting and the parameters of the protected line

6.3.1.4 Summary Remarks OOS Blocking during on Single-Pole Tripping

Single-pole tripping is typically employed at the EHV level to increase the power transfer level in weak areas of the power system. The ability to distinguish between a fault and a power swing during the open-pole period following a single-pole trip increases the power system stability.

The trajectory of the power swing is inside the inner characteristic of the power swing detection logic once an out-of-step block has been issued. Therefore, it is critical that this logic can detect if the swing evolves into a three-phase fault. Also, the unblocking logic must be able to distinguish between slow and fast swings, otherwise, the time delay required to unblock following a fast swing is too long.

6.4 CAPACITOR BANK PROTECTION????

6.4.1 Series Capacitors????

6.4.2 Shunt Capacitors [WPRC]???? [86]

Shunt capacitor banks are important in controlling and supporting the system voltage. In some areas, they may be required to prevent voltage collapse. Large capacitor banks that supply hundreds of megavars to the system are now in use. These banks consist of hundreds or even thousands of individual units interconnected to obtain the necessary voltage and VAR ratings. Large banks require sensitive protection to alarm and trip for faulted units.

Shunt bank protection must cover or consider:

- Failure of individual capacitor units
- Fuse failures and blown fuses
- Faults on the capacitor bank frames or structure
- Faults on the system external to the capacitor bank.

ANSI/IEEE C37.99-1980, the IEEE Guide for Protection of Shunt Capacitor Banks covers a very large range of fused bank configurations, protection requirements, and protection methods. More recently, fuseless banks have begun to appear. These have significant design, protection and operation advantages, made possible by film/foil capacitor units.

6.4.2.1 Shunt Capacitor Bank Description

Banks typically consist of series-parallel combinations of capacitor "cans" or "units". Each unit contains several smaller capacitors or sections, each having a typical nominal voltage rating of 1600 volts. Older capacitors are made of foil electrodes separated by dielectric layers and impregnated with oil. All new capacitors are made of foil electrodes separated by a dielectric of thin polypropylene sheets.

The referenced standard IEEE C37.99 states that capacitor units shall be capable of indefinite operation at 110% of the nameplate voltage rating. Virtually all high-

voltage banks are wye-connected. Although the neutral can be grounded or ungrounded, this paper concentrates on grounded wye-connected banks.

Fused banks consist of a series connection of numerous groups or layers. Each group contains a number of capacitor cans, or units, in parallel. Fuses protect each individual unit. Figure 6.61 shows one phase of a fused bank, with P units per group and S groups in series. The figure also shows two potential transformers. The bus PT is used for control and protection, while the tap PT is used for differential protection by comparing the bus and tap voltages.

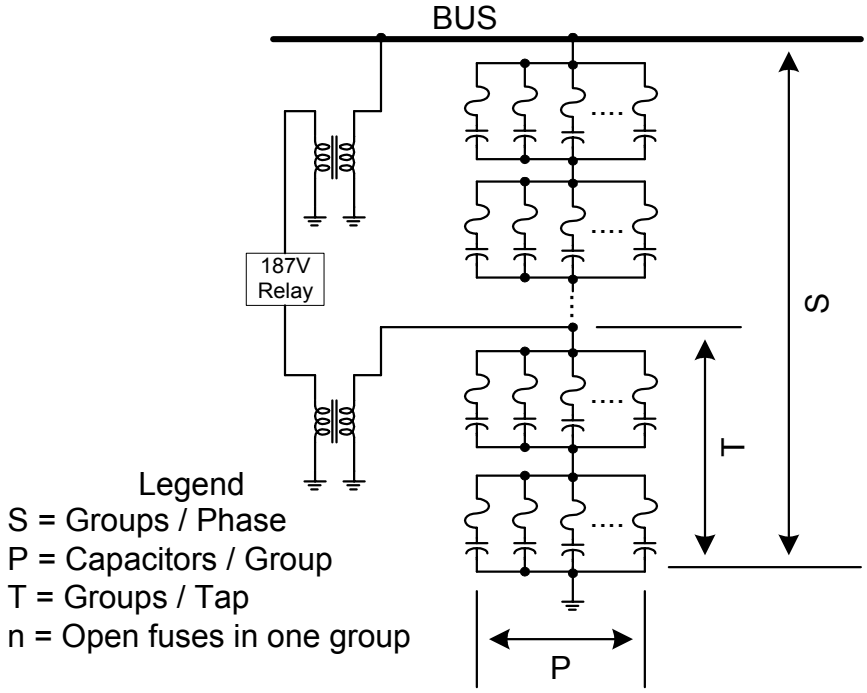


Figure 6.61: Fused Capacitor Bank With Voltage - Differential Protection

Fuseless banks consist of one or more series strings of units, per phase. If a section in a unit fails, the electrodes weld together solidly enough to safely carry rated current. Since there are no units in parallel, it is not necessary to isolate the failed unit.

6.4.2.2 Faults

A large variety of faults are possible. Many possibilities are mentioned below, along with the protective measures capable of handling them.

6.4.2.2.1 Shorted Unit in a Fused Bank

A unit normally fails at a point on wave where voltage is substantial. The system and the units in parallel with the shorted unit deliver energy to the fuse. The fuse in series with the shorted unit melts almost instantaneously.

In the less probable case where a unit is shorted upon energizing or otherwise shorts at a voltage zero, the fuse of the shorted unit carries P times the normal operating

current, where P is the number of units in parallel. In this case, fuse clearing can be expected in some fraction of a second.

The possibility of case rupture limits the number of units which can be safely paralleled. On the other hand, an open fuse increases the voltage across the remaining cans by approximately P/(P-1), so more than ten cans must be connected in parallel to ensure that one open fuse does not leave more than a 10% overvoltage on the remaining units in that group.

A differential voltage relay comparing the per-unit voltages at the bus and a tap point can detect a single open fuse in all but the largest banks.

6.4.2.2.2 Shorted Unit in an Unfused Bank

Unfused banks consist of series strings of units. There are no parallel combinations of units, so case rupture due to the energy delivered from parallel cans is not a concern. Differential voltage protection can again detect the unbalance produced by shorted units.

6.4.2.2.3 Shorted Group or Fuse Failure

Protection must cover failure of a fuse to clear and faults across any group. Fuses in the bank offer no protection for these events. The voltage across the remaining groups increases to S/(S-1), where S is the number of series-connected groups or layers. Fortunately, fuse failures and group faults are easily detected by differential protection, even in the largest banks.

A shorted group or fuse failure should be the first priority in protection. Fast tripping is desired to limit overvoltage on remaining groups and prevent the fault from becoming more serious.

6.4.2.2.4 Ground Fault in the Bank

A fault to ground could occur, which shorts out one to all of the groups in that phase. If a ground fault occurs near the bottom of the bank, the additional current produced may be very small. If the fault is near the top, the current can be large enough to quickly melt fuses. However, the fuses may not clear if the fault to ground is high enough up the bank to exceed recovery voltage capabilities of the fuses. Ground faults anywhere except at the top of the bank produce differential voltage signals.

If the fault is at the top, the bus and tap voltages remain equal, and no differential voltage develops. Phase overcurrent protection set to several multiples of rated bank current is sufficient to detect this fault.

6.4.2.2.5 Phase Fault in the Bank

Phase faults produce differential voltage, except if the fault is at the top. In the latter case, the overcurrent protection mentioned above must detect the fault.

A device with limited interrupting capacity, such as a circuit switcher, is often used to control the bank. It can be safely tripped for most faults in the bank. However,

overcurrent protection coordinated with the interrupting capacity of the circuit switcher should be considered to block tripping of the circuit switcher and operate devices capable of clearing the fault, for faults beyond the rating of the circuit switcher.

6.4.2.3 Voltage Differential Protection

Figure 6.61 shows one phase of a fused capacitor bank. Under normal conditions the groups of capacitor units have nearly identical impedances and the bus voltage divides evenly among all groups in series. Under most fault conditions, the voltage no longer divides evenly.

Table 6.6: General Equations for Grounded Wye Capacitor Banks

Condition	Equation	Equation Number
Tap voltage change (pu) for 10% group overvoltage	$dV10 = \frac{0.1}{S-1}$	Equation 6.16
Fuse operation (n) necessary to cause a 10% group overvoltage	$n = \frac{S \cdot P}{11 \cdot (S-1)}$	Equation 6.17
Tap voltage change (pu) when n fuses open in one group above the tap	$dV(n) = \frac{n}{S \cdot (P-n) + n}$	Equation 6.18
Tap voltage change (pu) when n fuses open in one group below the tap	$dVT(n) = \frac{n \cdot (1 - S/T)}{S \cdot (P-n) + n}$	Equation 6.19
Voltage (pu) across capacitors in group with n open fuses	$Vc(n) = \frac{S \cdot P}{S \cdot (P-n) + n}$	Equation 6.20

There are several ways to develop a differential voltage. The figure shows potential transformers measuring voltages at the bus and at an intermediate point in the bank. Table 6.6 gives equations for differential voltages and other conditions pertaining to a grounded fused shunt capacitor bank.

If the bank is divided into two or more series strings or otherwise split into sections, the voltages at intermediate points in the strings or sections can be compared. If there are only two strings, however, there are protection "holes": equal impedance changes above or below the taps cannot be detected. With more than two strings and tap voltages compared from string to string, only those faults which produced the same impedance changes in all three strings would be detected: this is probably an acceptable risk.

6.4.2.4 Unbalance Protection

Unbalance protection is a simpler alternative to differential protection. Where differential protection requires six inputs to cover a three-phase bank, an unbalance relay requires only one to three inputs.

One approach to unbalance protection monitors the neutral current for the bank. Unfortunately, natural system unbalance and faults produce neutral currents. Due to tolerances, differences in the net capacitance of the three phases also produce neutral currents.

Another approach is to compose a phasor sum of capacitor bank tap voltages. The idea is that when blown fuses produce unbalance, the phasor sum will deviate far enough from zero to be detected. Although the scaling factors for each of the three phases could be adjusted to null out system, measurement, and bank unbalance, the scheme still responds to system unbalance, because such unbalance is not static.

Unbalance elements respond to line and system faults, requiring long coordinating time delays. On the other hand, the differential elements emphasized in this paper do not respond to natural system unbalance or faults, and measurement unbalance can be nulled out.

6.4.2.5 Protective Relay Design

The development project had several objectives:

- Replace the differential protection previously provided by the MTY relay.
- Add instantaneous and definite-time overvoltage protection.
- Improve on the security, testability, and settability. In particular, make balancing the differential scheme easier.
- Include voltage control as well as bank protection to simplify installations.
- Provide versatility for broad voltage-relaying application through programmable mask logic and other tools.

6.4.2.5.1 Design Concepts

Three-phase differential protection requires six voltage inputs. Three-phase voltage control requires three voltage inputs. We designed one instrument with two sets of three-phase voltage inputs (X and Y) that could be used as two three-phase voltage relays and simultaneously as a differential relay. Each of the two voltage relays provides under-/overvoltage protection as well as voltage control.

This design approach yielded a relay that can control and protect a capacitor bank as well as a shunt reactor.

6.4.2.5.1.1 Relay Hardware

We chose to use field-proven digital relay hardware as the basis for the design. The hardware samples six voltage inputs four times per cycle and processes the samples in a microprocessor.

6.4.2.5.1.2 Voltage Reference and Temperature Dependence

Because the relay is intended for voltage control as well as capacitor bank protection, a precise voltage reference is required. The relay uses the internal buried-zener reference diode in the analog-to-digital converter as the reference.

We characterized the temperature dependence of voltage measurement by applying a constant voltage to the relay and reading its voltage measurement using the relay METER function while moving the temperature from -20 to +60° Celsius. We determined that the temperature dependence is about +6 mV/° Celsius at a nominal input voltage of 70 volts. A one percent change in the set point would require a temperature change of about 116° Celsius. This applies to all voltage elements, whether intended for voltage control or protection.

6.4.2.5.1.3 Elements for Voltage Control Measure the Average System Voltage

The relay contains two overvoltage and two undervoltage elements intended for voltage control. Each of these four elements responds to the magnitude-average three-phase voltage. Because of the filtering mentioned earlier, the relay measures and controls the three-phase average fundamental-frequency voltage.

6.4.2.5.1.4 Elements for Protection Measure the Individual Phases

There are overvoltage and undervoltage elements for each of the six voltage inputs. These respond to the fundamental-frequency component of the voltage applied to each input.

6.4.2.5.1.5 Differential Elements Respond to Magnitude Differences

A current differential element, if used for transformer protection, responds to the phasor sum of all currents into the zone of protection for that relay. In doing this, the current differential relay is performing Kirchoff's current law on the protected zone. Normally, high sensitivity is not a requirement.

Figure 6.62 reveals how the shunt capacitor differential protection problem is different. Minute changes in the performance of a string of capacitors acting as a voltage divider must be detected. The voltage measurement devices are of vastly different ratios and may have very different designs. For example, the bus voltage measurement may come from a CCVT, while the tap voltage measurement may come from a wound PT or potential device. Different phase shifts in the bus and tap PTs could produce error signals in a differential relay which responds to the phasor difference between the bus and tap voltages. For example, suppose that the bus and tap PTs produce 70 volts for the relay under normal balanced conditions, but there is a 0.5 degree difference between the phase shifts of the two voltage measurements. The differential voltage is about sin (0.5) = 0.009 pu or 0.6 volts. This is on the order of the differential signal that would result from a single blown fuse in a 100-unit bank!

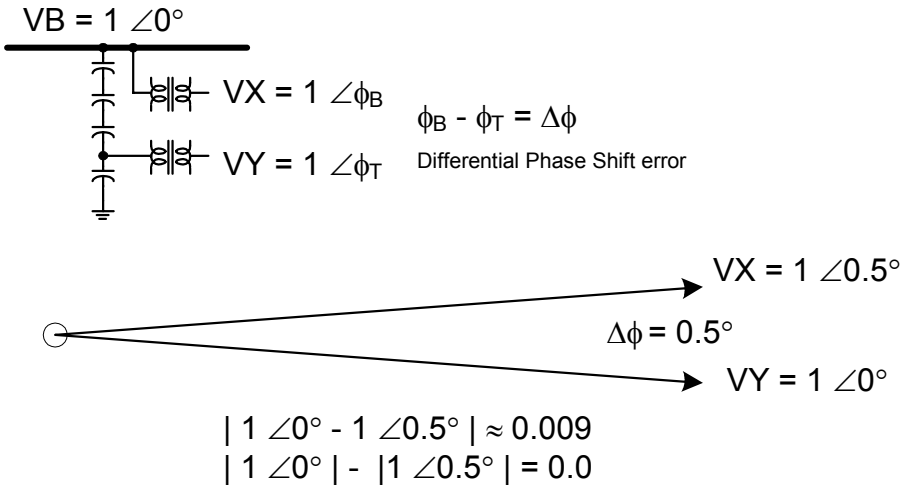


Figure 6.62: Differential Phase Shift Error Causes Significant Differential Voltage Signal Unless Magnitudes Are Used

A null adjustment for phase angle as well as for magnitude could overcome this limitation on sensitivity by providing. However, there is very little information that can be used in the phase angle, so it can be ignored. Short circuits and blown fuses in the bank move the magnitudes of the voltages, but the phase relationships stay generally constant. An exception is a phase-to-phase fault within the bank: it causes a significant phase shift between the bus and tap voltages. Fortunately this type of fault causes a significant magnitude shift.

For these reasons, the relay is designed to respond to the differences between the magnitudes of its inputs rather than the phasor differences.

The computer forms three magnitude-differential voltages. For example, for phase A, the differential voltage is:

$$dVA = |VAX| - KA \cdot |VAY| \qquad \text{Equation 6.21}$$

where:

dVA is the differential A-phase voltage

VAX is the A-phase input from the X set of potentials (e.g. bus)

VAY is the A-phase input from the Y set of potentials (e.g. tap)

kA is an adjustable proportionality constant.

The adjustments KA, KB and KC permit precise nulling of the differential voltages. In fact, the relay has a feature whereby it measures what values KA, KB and KC should have in order to null out the difference voltages.

Every attempt must be made to minimize the effects of quantization noise and scaling errors inside the relay. The relay should also accommodate noise and errors that occur outside the relay as much as possible. The difference voltage finally tested is the smoothed difference between two smoothed voltage measurements. The

smoothing does introduce some delay, but greatly adds to the security of the relay and reduces the minimum setting of the differential elements to under 0.2 volts.

6.4.2.5.2 Relay Logic

Figure 6.63 through Figure 6.67 illustrate the straightforward relay logic.

Figure 6.63 shows the instantaneous overvoltage and undervoltage elements and logic. Using the programmable-mask logic, an overvoltage condition on any combination of the six inputs could be programmed to cause a trip. In capacitor protection, these elements could be set to trip the bank for a severe overvoltage condition, e.g. 1.2 per unit.

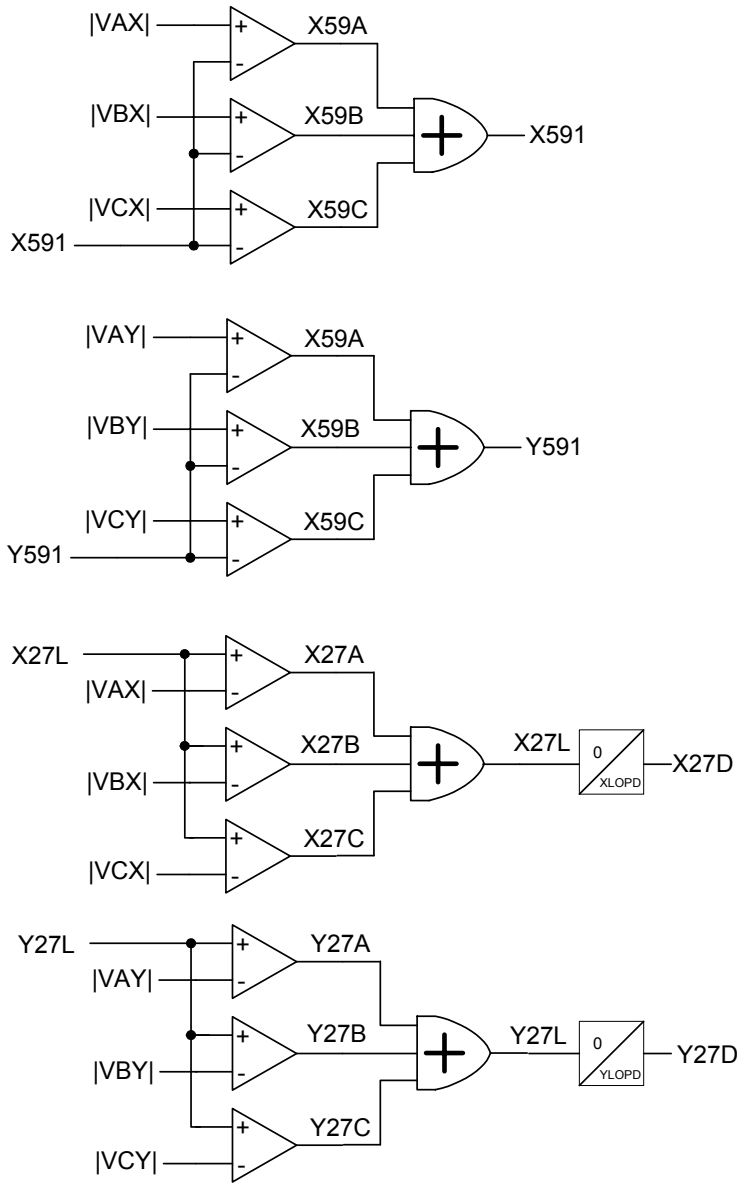


Figure 6.63 Overvoltage Elements / Undervoltage Elements and Logic

The undervoltage elements from the X-potentials are or'ed together and drive a time-delay dropout timer intended for loss-of-potential blocking of the differential elements. The Y-side "ands" the Y-undervoltage conditions together for a loss-of-potential condition. The OR of X-potentials versus AND of Y-potentials is the only difference between the X and Y sides of the relay. When the relay is applied to protect a capacitor bank, bus potentials should be applied to the X input and tap potentials to the Y input. Loss of a single phase of bus potential immediately blocks the differential relay logic; loss of three-phase tap potentials (as occurs every time control switches the bank off) is required to block the differential protection.

Definite-time overvoltage elements (Figure 6.64) can be used to initiate a trip for less-severe overvoltage conditions with the security of definite-time delay. Tripping might be set for several minutes at a voltage of 1.1 per unit (the upper limit of continuous operation of the capacitors.)

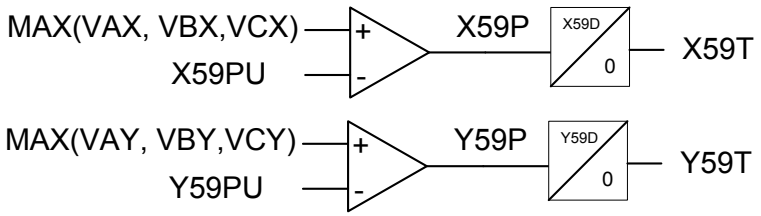


Figure 6.64: Definite-Time Overvoltage Logic

Figure 6.65 shows one phase of the voltage differential protection. The difference voltage is formed, considering a scale factor (KA for phase A) and tested against two thresholds (87AT, 87AA). Each phase has separate scale factors and thresholds. Loss-of-potential blocking disables the differential elements for single-phase losses of X-potentials or three-phase losses of Y-potentials. The time-delay dropout timers (LOPD, XLOPD and YLOPD) permit inclusion of sufficient time for voltages to settle down after energizing the bank or other restorations or applications of voltage. Keep in mind that the differential elements might need to be set quite sensitively (e.g. less than 0.01 pu in many cases), so ample settling time should be allowed for CCVT voltage measurements and the relay filtering.

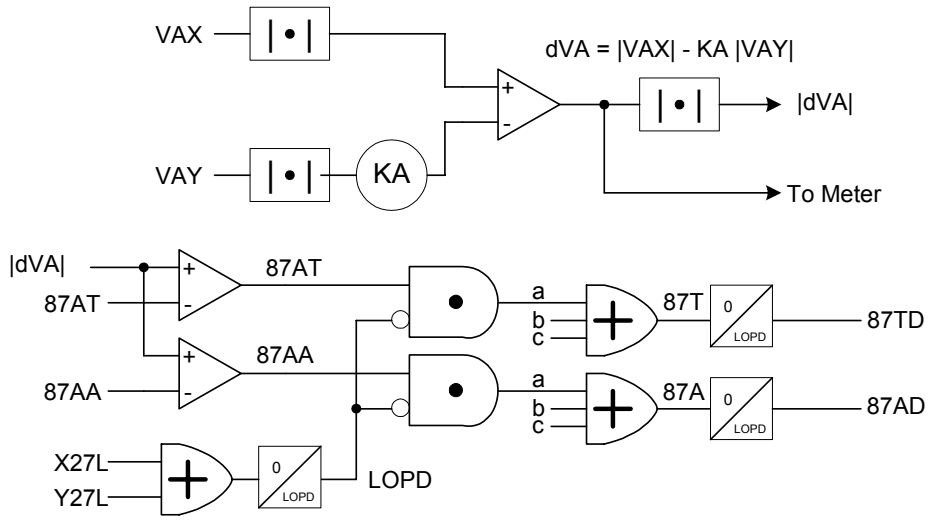


Figure 6.65: Voltage Differential Protection (Per Phase)

Differential signals exceeding their thresholds on any phase drive timers, which require minimum duration of the signals, and stretch the dropout time. The two outputs 87TD and 87AD can be used to trip and/or alarm on unbalanced conditions.

The signed difference voltages (dVA, dVB, dVC) are used by the METER command, so that we may inspect the difference voltage being sensed at any time.

Figure 6.66 shows the two voltage control logic schemes. Inputs V1 and V2 are taken from the X or Y side, depending on the voltage control setting selected.

When the differential functions are used, voltage control would normally use the X-potentials. The relay may be set so that V1 = V2 = VX. Both voltage control schemes then operate from the bus voltage, but provide independent levels and time delays.

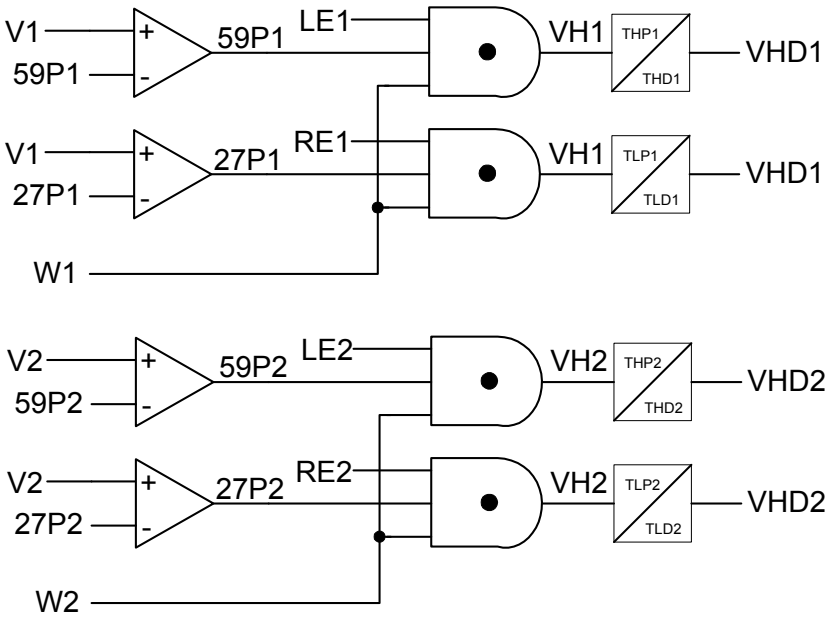


Figure 6.66: Voltage Control Logic

If the differential functions are not needed and the relay is to be used as two completely independent voltage relays, the instrument can be set so V1 = VX and V2 = VY, where VX and VY are the three-phase average voltages. Another option is that the relay automatically chooses VX or VY depending on loss-of-potential conditions.

The logic of Figure 6.67 can be used to prevent the voltage control scheme from oscillating. The logic detects voltage control instability by signaling a high voltage condition immediately after a voltage increase. For example, suppose the difference between the raise and lower voltage thresholds is 0.5 volt, but the insertion of the capacitor bank increases the voltage by one volt. If the voltage drops just below the raise-voltage threshold, then the bank is energized after a time delay. The signal to energize the bank is stretched with a time-delay dropout timer, providing an indication that the voltage "just raised." In our example, inserting the bank increases the voltage one volt, which brings it above the voltage-lower threshold. We assumed the voltage-lower threshold to be only 0.5 volt above the raise-voltage threshold. So, inserting the bank caused an overvoltage condition, and the lower-voltage threshold timer begins running.

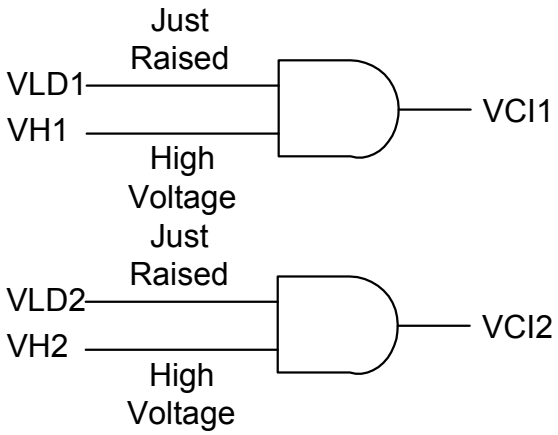


Figure 6.67: Voltage Control Instability Logic

6.4.3 Shunt Reactors????

6.4.4 Static VAR Compensation????

7 GENERATOR PROTECTION[87] (HECTOR ALTUVE) [6062][88], [6074][89]

Utility, industrial, and independent power producers (IPP) generation is subject to several adverse conditions for which protection must be considered. These conditions can be placed into one of categories. The first is for faults within the generator itself. The second category is for faults or abnormal operating conditions external to the generator but in some way involve the generator. The generation units for which the protection to be discussed in the following sections is limited to primarily synchronous machines but may include induction generation where appropriate. The protection systems for the various types of faults presented in this chapter should be viewed and layers of protection applied over each other as appropriated for the needs of the equipment. (See Figure 7.7.) Table 7.1 lists the types of problems that generators either need to be protected from.

Table 7.1: Potential Generation Protection Problems

Internal Faults	**Section**
Primary and backup phase and ground faults in the stator	7.3.1,7.3.2
Rotor ground faults and loss of field	7.3.3
System Disturbances and hazardous operational conditions	7.4
Generator motoring: Insufficient or loss of prime mover	????
Overvoltage and undervoltage	7.4.1,7.4.2
Inadvertent energizing resulting in nonsynchronous connection	????
Unbalanced current: pole disagreement or pole flashover	????
Overload and over temperature operation (loss of cooling)	7.5
Under and over-frequency operations	????
Loss of synchronism (Out of Step)	7.7, 7.7
Subsynchronous resonance	????

There are two common scenarios for connecting generators to loads. Generators can be directly bussed together through separate breakers as illustrated in Figure 7.1. The optional step-up transformer is not required if the power system voltage is the same as the generator voltage. This can be the case if the connection to the power system is through the distribution system. Generators are rarely operated above 20KV line to ground because of insulation requirements. For directly connected generators, the transformers, generators and buses are individually protected but coordinated with overlapping zones of protection as discussed in section 0. The auxiliary power is critical to the power plant for powering local loads necessary to service the generators. In the event of a cold isolated start, on-site diesel power generators must provide the minimal local power to start the first generator. The step-up transformer and/or the amp capacity of the distribution line limit amount of generation.

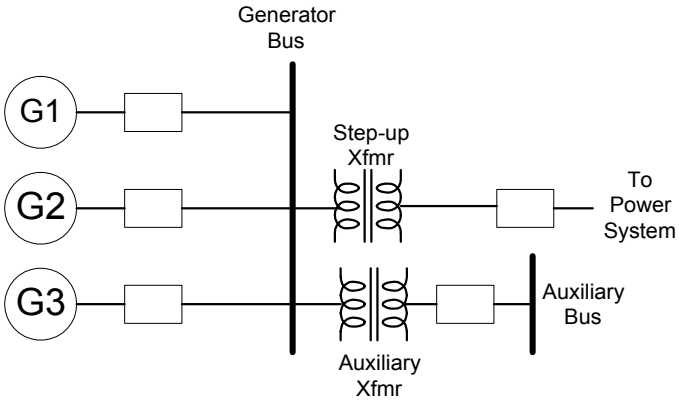


Figure 7.1: Direct-Connected Generator Scheme

Figure 7.2 illustrates unit-connected generators. In this configuration, the generator, transformer, and breaker are considered as autonomous units and may be protected as a single entity. Such a configuration offers additional reliability and flexibility at the expense of additional equipment. Configurations for connection the power and auxiliary bus must be designed carefully provide the expected redundancy of service.

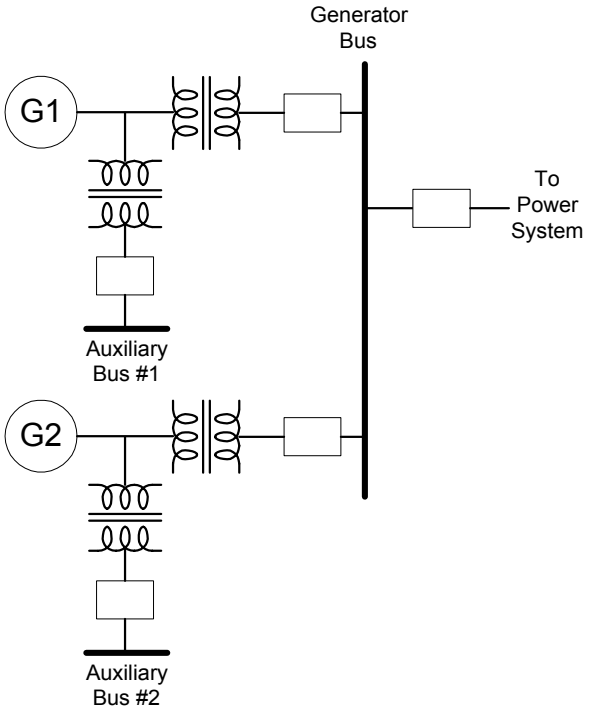


Figure 7.2: Unit-Connected Generators

When generation protection includes step-up transformers and interconnecting lines, this is considered unit protection. In this case, careful consideration must be paid to the availability of instrumentation for adequate protection and if necessary, fault identification.

7.3 INTERNAL GENERATOR FAULTS

Internal faults must be detected by sensing lines that enter or leave the generator to make external connections. In the following sections, method for sensing internal faults will be discussed.

7.3.1 Stator Phase Faults

Stator ground faults occur when the insulation around the stator breaks down and allows current to flow the ground or directly to another phase. Faults involving multiple phases are most easily detected using differential relaying. (See section 4.1.3) Figure 7.3 and Figure 7.4 show the connections required for percentage differential relaying. The differential relay will operate whenever the current in the stator winding CTs is different than the current in the line CTs. For wye-connected generators, the relationship is one to one. The winding CTs in delta-connected generators must be connected to convert delta currents to line currents as shown in Figure 7.4.

Type 87 percentage differential relays offer immunity to false tripping due to high currents for load or external faults. This accounts for variations in CTs and effects of CT saturation. It is recommended that CTs with similar characteristics be used on differential schemes to minimize unbalance due to instrumentation.

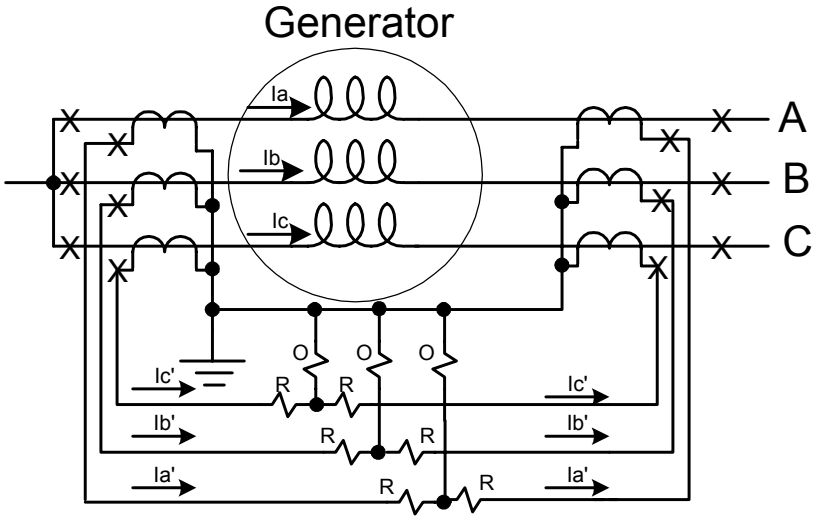


Figure 7.3: Percentage Differential Relaying Configuration for Wye-Connected Generators

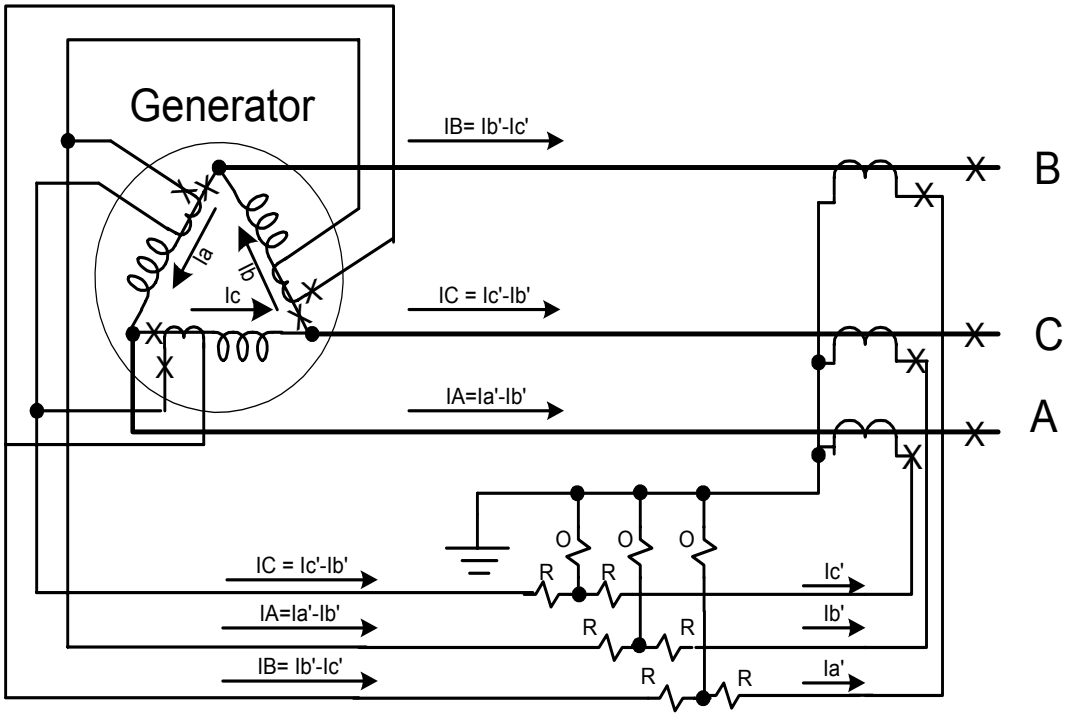


Figure 7.4: Percentage Differential Relaying Configuration for Delta-Connected Generators

7.3.2 Stator Ground Faults

If the stator is ungrounded, as is the case of a delta-connected generator, then the first fault will cause no problem, because there is no path for the ground current. The second ground fault now becomes either a phase-to-phase fault or a turn-to-turn fault. If the capacitance to ground is nearly equal for all three phases, ground faults can be detected by monitoring the line-to-ground voltage for each phase.

Stator faults for wye connected generators (need to fill in here)????

7.3.3 Rotor Faults

DC exciter currents are applied to the rotors winds that are isolated from ground. Rotor ground faults are detected by applying a type 67F relay supplied from either a separated source or the exciter as shown in Figure 7.5 and Figure 7.6. Either way, one side of the relay must be referenced to ground. Frequently, grounding brushes are required to solidly ground the rotor otherwise the ground path is through the bearings. The electrical path through the bearings usually has high impedance because of the insulation resulting from the oil film that the bearings rotate on. The first ground fault does not impair the rotor as only the current through the 67F relay goes to ground, which is negligible compared to the nominal field current. Hence the 67F relay serves more as an alarming function than protection.

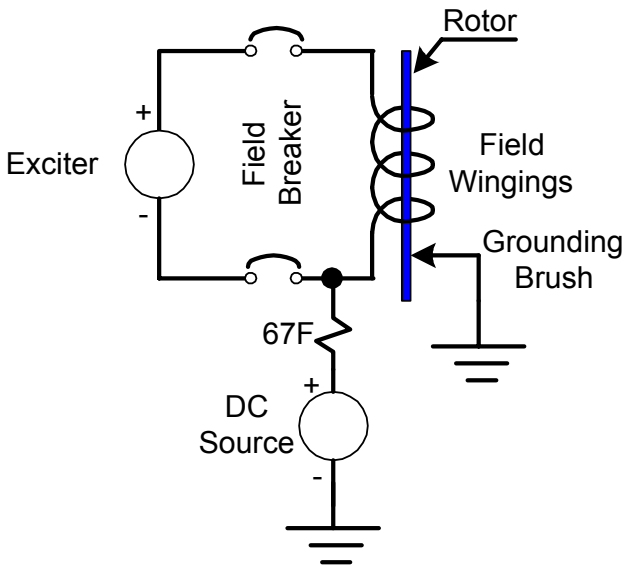


Figure 7.5: Stator Ground Detector With External Relay Source

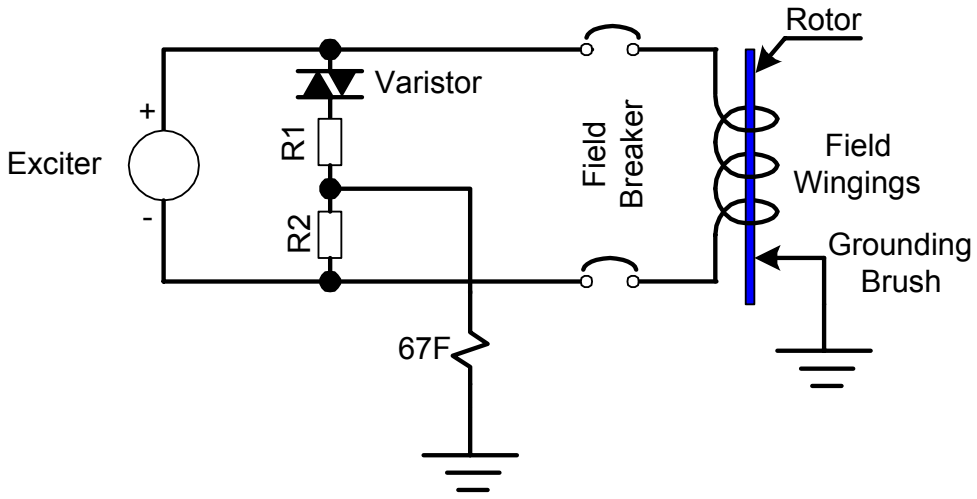


Figure 7.6: Stator Ground Detector Without External Relay Source

A subsequent second ground fault in the rotor has two serious affects. High currents are now conducted through the iron that can result in physical damage to the rotor. Secondly, a number of field windings are now shorted out resulting in an uneven distribution of magnetic field.

Although generators can continue to operate following an initial field-ground event, prudence dictates that the problem be resolved as quickly as possible. If the 67F relay is used for tripping, time delays of one to three seconds is recommended to avoid transients that are coupled from the stator winding into the rotor due to faults external to the generator. If the detection scheme shown in Figure 7.6 the maximum relay sensitivity is for faults at either end of the field. If the voltage divider equally splits the exciter voltage, the voltage on the 67F relay is nominally zero. The relay has

poor sensitivity for faults near the center of the rotor windings. The dynamic resistance characteristics of the varistor move the null point when the voltage across it changes to improve the relay sensitivity.

7.4 External Generator Faults

External faults are those that can occur independently to the generator condition. The conservative design of generators requires that fault currents be quickly removed or significantly limited.

7.4.1 Ground Fault Protection

Synchronous generators are rarely solidly grounded at the neutral point because of the risk of generating phase to ground fault currents that can also cause mechanical damage to the generator structure or stator stacks of iron. Usually, generators use a neutral impedance to limit these ground fault currents. To reduce the physical size of the resistor, a single-phase distribution transformer is used similar to T1 in Figure 7.7. As a consequence of the high ground impedance, the potential at the generator's neutral point can shift to line to ground potential for ground faults close to the high voltage terminals. Therefore, the primary voltage rating of transformer T1 must be at least as great as the generator line to ground potential.

Figure 7.7 also demonstrates the concept of multiple layers of protection suggested previously with the ground protection laid over the phase protection. The ground differential relay, 87GD, operates for internal stator ground faults but not for external ground faults. For internal stator ground faults, the $3I_0$ current to the right of the 87GD relay reverse direction. When this happens, the currents in the 87GD relay are additive instead of canceling with the current from the generator neutral CT. The 51G relay shown in Figure 7.7 provides backup ground relaying but is normally set for slow trips to avoid inadvertent operation for external faults or transients generated from normal operations.

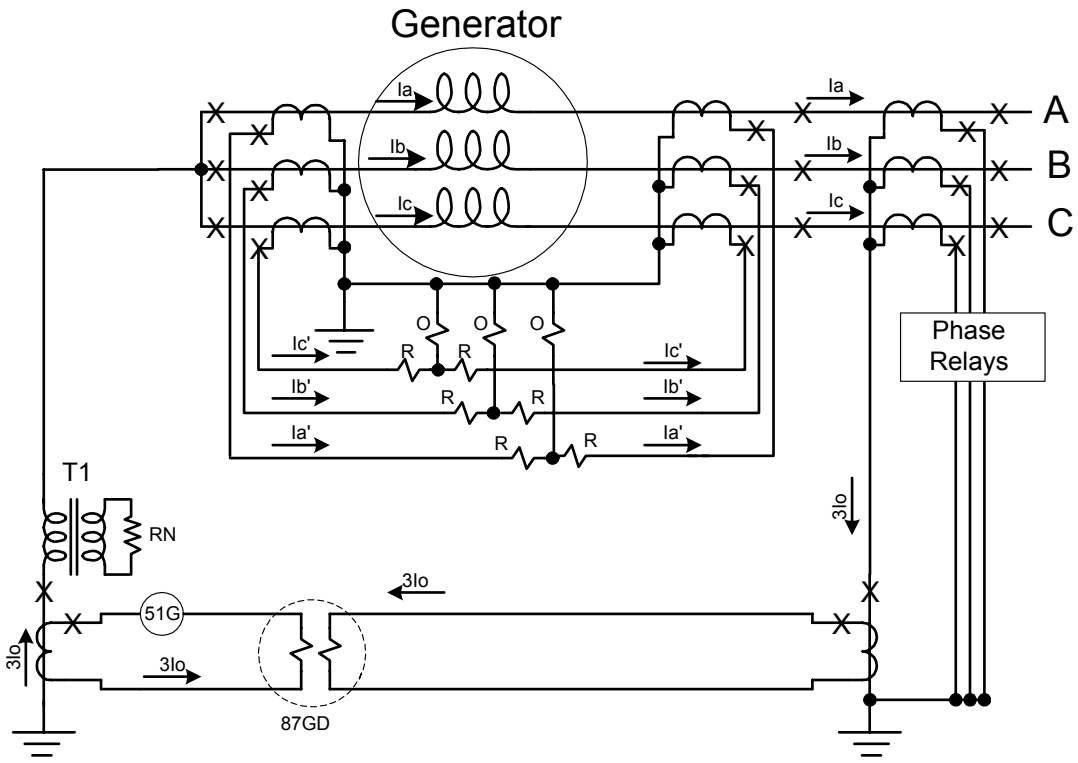


Figure 7.7: Generator Protection for External Faults

7.4.2 External Phase Fault Protection

Load unbalance, phase and ground faults all generate negative sequence currents that are couple back into the rotor inducing AC currents at double the nominal system frequency. Skin effect forces these currents to concentrate in the surface windings and generate heat in the rotor. The time that this heating can be tolerated is determined from equation **Error! Reference source not found.**. The K factor in represents a generator constant determined by unit construction. This constant may be as high as 40 for salient pole machines that are typical of hydroelectric generators. For cylindrical rotor machines, a K of 20 or less is to be expected.

$$t = \left(K \Big/ I_2^2 \right)$$ Equation 7.1

The phase relays shown in Figure 7.7 are expected to detect negative sequence faults and provide the proper protection. (This is a good place to introduce the SEL300G relay).????

7.5 Overload Protection

Generator ratings are based upon the expectation of an nominal range of operating and environments conditions. Generators can operate out side these limits intermittently provided that this operation does cause the stator windings to become

so hot that the insulation is damaged. Relays connected to restive temperature devices (RTD) can monitor the generator temperature and trip the unit if necessary. The RTDs are usually mounted in the stator iron as physically close to the stator windings as possible.

7.6 Loss of Excitation

The rotor field is the electromagnetic force that holds the rotor in synchronism with the field rotating in the stator at the power system frequency. A loss of this field causes the generator to speed up quickly because the power into the generator from the prime mover can now only transferred to energy stored in the rotor's angular velocity. Without removing the power input from the prime mover, the generator will soon self-destruct. The effects a loss of field can have on the power system include:

- Loss of reactive support
- Substantial reactive drain
- Area voltage collapse
- Power swings
- Excessive reactive power flows
- Transmission line tripping

When a loaded generator looses its field current, the generator becomes an induction generator until the prime mover is removed after which it may become an induction motor. Table 7.2 lists some of the methods used to detect a loss of rotor excitation. Whichever method is chosen, it should be immune to responding to normal system operations or system faults that are in the process of being cleared by other protection devices. Failing to do so may result further system instability.

Table 7.2: Methods for Detecting Loss of excitation

Method	Comments
Directly measure field current	Does not detect rotor shorts that result is loss of effective excitation.
Measuring generator reactive current	See section 7.7
Offset Mho Relay	Insensitive to power swings, system faults and stable transients.[3]

7.7 Out-of-Step

When a generator is operating at a frequency different than the power system, the generator is considered to running out-of-sep. The phase angle of the current between the generator terminals and the current at a location that is separated by impedance such as a transformer or transmission line is always changing. The rate

[3] *"IEEE Tutorial on the Protection of Synchronous Generators", pg. 43*[87]

that this angle changes is proportional to the frequency mismatch. If the generator is running faster than nominal system frequency, the generator will continue to speed up unless the input from the prime mover is removed. Just prior to the generator going out-of-step, the generator input and output power was in a balanced state. If the generator pulls out of synchronism due to a momentary loss of rotor field or an disturbance on the system, the generator will operate as a motor absorbing energy from the system when the current phase angle is between 90° and 270° with respect to the system. The electrical power from the system combined with the power from the prime mover will accelerate the generator and it will not be able to slow down during the time it is generating power back into the system.

One method of detecting an out of step conditions is monitor the phase between the terminal voltage and phase current. Whether electrical power delivered to or absorbed from the system modeled as shown in Figure 7.8 is determined by the angle θ, the angle between the voltage and current in Equation 7.2 that can be related back to the armature voltage to become Equation 7.3. The sine of the angle difference is positive to power delivered to the system and negative for power absorbed by from the system. Figure 7.9 illustrates this concept graphically, which, for the simplified system shown in Figure 7.8, makes the angles θ and δ the same. A fact learned from power system theory[4], is that once the power angle has gone beyond 90°, the system will not recover unless remedial action is taken. This action usually requires the two sources be electrically isolated until synchronous speed can be reestablished. Therefore, detecting the angle crossing this 90° boundary only once should be sufficient to indicate an out-of-step condition. Usually, the relays are set so the boundary, either at 90° or 270° has to be crossed multiple times in a specific time before tripping.

$$P_1 = (Vt \cdot Ia)\cos(\theta),\ \theta = \angle Vt - \angle Ia \qquad \text{Equation 7.2}$$

$$P_1 = \left(\frac{Ea_1\ V_{sys}}{Xa_1 + Zs + Xa_2}\right)\sin(\delta), \delta = \angle Ea_1 - \angle Ea_2 \qquad \text{Equation 7.3}$$

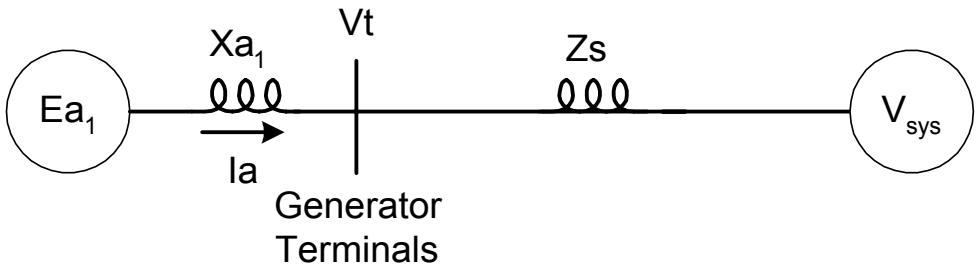


Figure 7.8: Two-Source Power System

[4] *Power System Analysis and Design, Chapter 13.3, pg. 543*[77]

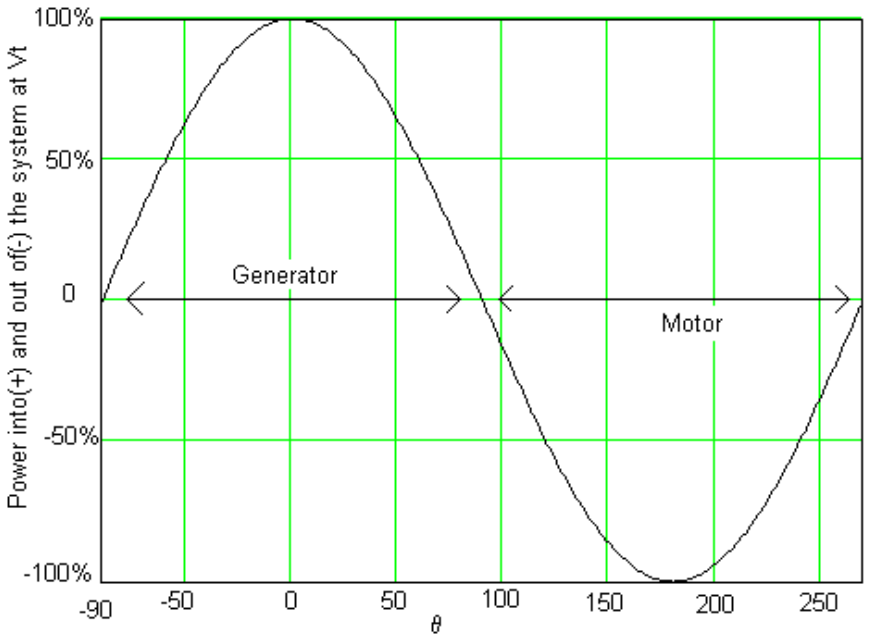


Figure 7.9: Generator Power Curve

7.8 OVER-SPEED

See loss of excitation section 7.6.

8 MOTOR PROTECTION

The fact that motor protection has many similarities to generation protection should be of no surprise since most motors can operate in the generating mode and vice versa. Like generators, motors need protection for internal winding and ground faults and thermal overload. Motors also need protection for single-phase failure and, in some cases, for loss of load. For synchronous machines, the protection possibilities are the same as generators. Induction motors offer a new set of protection challenges.

Since motors are electro-mechanical devices, there both electrical and mechanical failures. Statistics show that 40-50% of motor failures are due to rotor bearings, 25-35% due to stator faults and approximately 10% due to rotor electrical faults.

Fuses are the most widely used protection devices for motors. They must be sized to handle starting current but also clear sustained winding and ground faults. On larger motors, Time overcurrent relays are used for both phase and ground faults. Residual or zero sequence time over-current ground fault protection is possible if the motor is wye connected with a grounded neutral. Residual time-overcurrent is also available using window CTs. (See Figure 5.9, chapter 5.) The ground fault current can be limited using transformers with the secondary connected delta. A neutral resistor can be used if the secondary is connected grounded wye.

For phase failure, motors already running may continue to run but with a much reduce efficiency that leads to thermal over loading. If the motor is not running, there may be insufficient torque to start or the motor may run in the opposite direction. Since ground is not involved in phase failure faults, ground relays will not detect this situation. Also, the increase in phase current, if any, may be well below the phase overcurrent relay pickup setting or below the fuse melting current. Negative sequence overcurrent is one way of detecting phase failure. Negative sequence voltage relays can also be used to detect motors running in the opposite direction to the positive sequence voltage.

Excessive or elevated temperature operation can be caused by repeated starting, stalling because of excessive load, normal operating under-/overloading, running in an unbalanced electrical condition, or simply loss of cooling.

8.3 INDUCTION MACHINES – MOTORS [6003][90] [6023][91] , [6034][92]

The characteristics of the motor application are shown in Figure 8.1 with the starting current of an induction motor. In the motor application, definite-time and instantaneous elements provide protection for faults in the motor leads and internal faults in the motor itself. A definite-time setting of about 6 cycles allows the pickup to be set to 1.2 to 1.5 times locked rotor current to avoid tripping on the initial X_d" inrush current (shown magnified). The instantaneous can then be set at twice the locked rotor current for fast clearing of high fault currents.

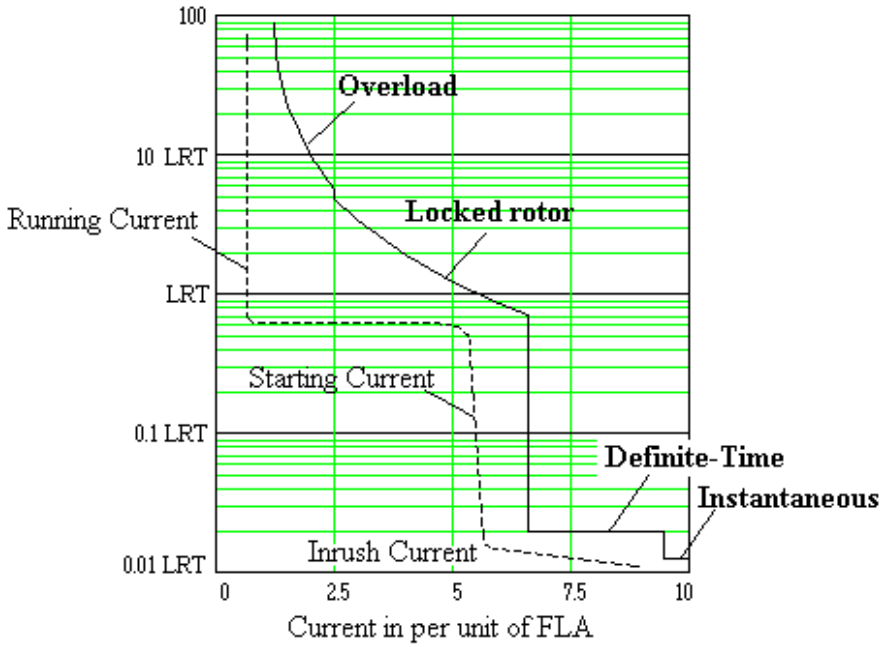


Figure 8.1: Motor Characteristics Plotted With Motor-Starting Current

An inverse-time phase overcurrent element and a separate negative-sequence overcurrent element could be applied to prevent the overheating caused by a locked rotor or an unbalance current condition. However, neither of these elements can account for thermal history nor track the excursions of temperature. Instead, an element is used that accounts for the I^2r heating effect of both positive- and negative-sequence current. The element is a thermal model, defined by motor nameplate and thermal limit data, that estimates motor temperature. The temperature is then compared to thermal limit trip and alarm thresholds to prevent overheating for the abnormal conditions of overload, locked rotor, too frequent or prolonged starts, and unbalanced current.

8.3.1 Defining the Thermal Model

The I^2r heat source and two trip thresholds can be discerned from a motor characteristic of torque, current, and rotor resistance versus slip shown in Figure 8.2. The plot shows the characteristic of the induction motor to draw excessively high current until the peak torque develops near full speed. Also, the skin effect of the slip frequency causes the rotor resistance to exhibit a high locked rotor value labeled R_1 which decreases to a low running value at rated slip labeled R_0.

Using a typical starting current of six times the rated current and a locked rotor resistance R_1 of three times value of R_0, the I^2r heating is estimated at 6^2 x 3 or 108 times normal. Consequently, an extreme temperature must be tolerated for a limited time to start the motor. Where an emergency I^2t threshold is specified by the locked rotor limit during a start, a threshold for the normal running condition is specified by the service factor. Therefore, the thermal model requires a trip threshold when

starting, indicated by the locked rotor thermal limit, and a trip threshold when running, indicated by the service factor.

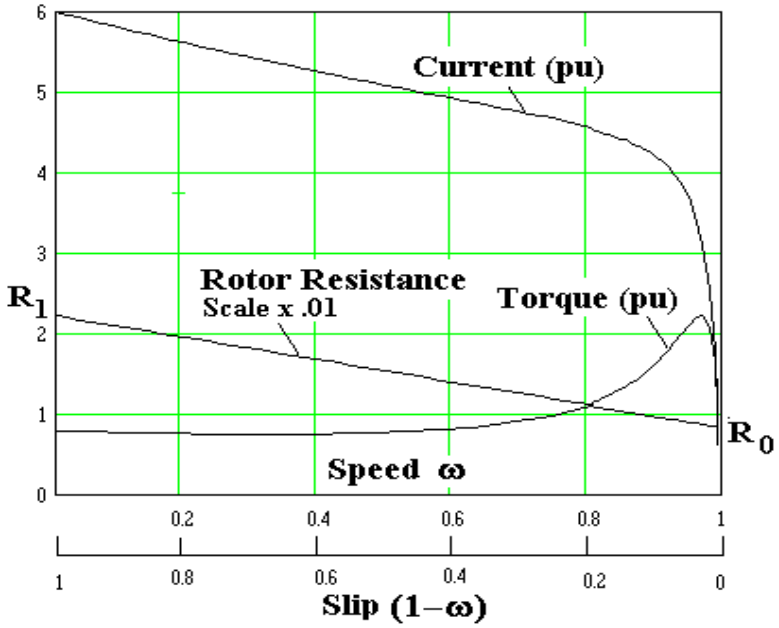


Figure 8.2: Current, Torque, and Rotor Resistance of an Induction Motor Versus Speed

The slip dependent heating effect of positive- and negative-sequence currents is derived as follows. The positive-sequence rotor resistance plotted in Figure 8.2 is calculated using current, torque, and slip in the following equation:

$$R_r = \frac{Q_M}{I^2} S \qquad \text{Equation 8.1}$$

and can be represented as a linear function of slip. The positive-sequence resistance R_{r+} is a function of the slip S:

$$R_{r+} = (R_1 - R_0)S + R_0 \qquad \text{Equation 8.2}$$

The negative-sequence resistance R_{r-} is obtained when S is replaced with the negative-sequence slip (2-S):

$$R_{r-} = (R_1 - R_0)(2 - S) + R_0 \qquad \text{Equation 8.3}$$

Factors expressing the relative heating effect of positive- and negative-sequence current are obtained by dividing **Error! Reference source not found.** and Equation 8.3 by the running resistance, R_0. Consequently, for the locked rotor case, and where R_1 is typically three times R_0, the heating effect for both positive- and negative-sequence current is three times that caused by the normal running current.

$$\frac{R_{r+}}{R_0}\Big|_{S=1} = \frac{R_{r-}}{R_0}\Big|_{S=1} = \frac{R_1}{R_0} = 3 \qquad \text{Equation 8.4}$$

For the running case, the positive-sequence heating factor returns to one and the negative-sequence heating factor increases to 5:

$$\frac{R_{r+}}{R_0}\Big|_{S=0} = 1 \quad \frac{R_{r-}}{R_0}\Big|_{S=0} = 2\left(\frac{R_1}{R_0}\right) - 1 = 5 \qquad \text{Equation 8.5}$$

These factors are the coefficients of the positive and negative currents of the heat source in the thermal model.

8.3.2 States of the thermal model

Because of its torque characteristic, the motor must operate in either a high-current starting state or be driven to a low-current running state by the peak torque occurring at about 2.5 per unit current. The thermal model protects the motor in either state by using the trip threshold and heating factors indicated by the current magnitude. The two states of the thermal model are shown in Figure 8.3. The thermal model is actually a difference equation executed by the microprocessor. However, it can be represented by the electrical analog circuit shown in Figure 8.3. In this analogy, the heat source is represented by a current generator, the temperature is represented by voltage, and thermal resistance and capacitance are represented by electrical resistance and capacitance. The parameters of the thermal model are defined as follows:

R_1 = Locked rotor electrical resistance (per unit ohms)

R_0 = Running rotor electrical resistance also rated slip (per unit ohms)

I_L = Locked rotor current in per unit of full load current

T_a = Locked rotor time with motor initially at ambient

T_o = Locked rotor time with motor initially at operating temperature

The starting state is shown in Figure 8.3a and is declared whenever the current exceeds 2.5 per unit of the rated full load current and uses the threshold and heating factors derived for the locked rotor case. Thermal resistance is not shown because the start calculation assumes adiabatic heating. The running state, shown in Figure 8.3b, is declared when the current falls below 2.5 per unit current and uses the heating factors derived for the running condition. In this state the trip threshold "cools" exponentially from a locked rotor threshold to the appropriate threshold for the running condition using the motor thermal time constant. This emulates the motor temperature, which cools to the steady-state running condition.

In the model, the thermal limit $I_L^2 T_a$ represents the locked rotor hot spot limit temperature and $I_L^2(T_a - T_o)$ represents the operating temperature with full load current. The locked rotor time, T_a, is not usually specified, but may be calculated by using a hot spot temperature of six times the operating temperature in the following relation:

$$\frac{I_L^2 T_a}{I_L^2 (T_a - T_o)} = 6 \;\therefore\; \frac{T_a}{T_o} = 1.2 \qquad \text{Equation 8.6}$$

There are two reasons for using the rotor model in the running state. The first is that, despite a difference in thresholds, it is industry practice to publish the overload and locked-rotor thermal limits as one continuous curve, as illustrated in Figure 8.1. The second is that the rotor model accounts for the heating of both the positive-sequence and the negative-sequence current. As a final refinement, assigning standard values of 3 and 1.2 to the ratios R_1/R_0 and T_a/T_o respectively, allows the model parameters to be determined from five fundamental settings:

FLA Rated full-load motor current in secondary amps

LRA Rated locked-rotor current in secondary amps

LRT Thermal-limit time at rated locked-rotor current

TD Time dial to trip temperature in per unit of LRT

SF Motor rated service factor

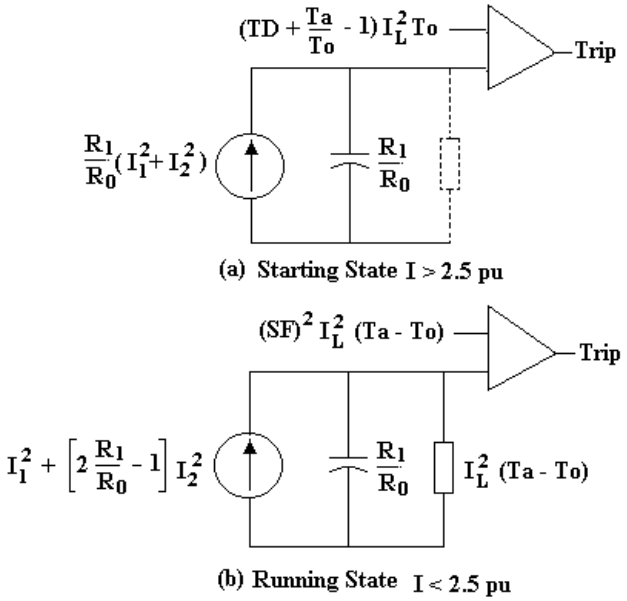


Figure 8.3: States of the Thermal Model

9 HOW PROTECTION EFFECTS POWER QUALITY

9.3 DEFINING POWER QUALITY????

9.4 OUTAGES ????

9.5 Over- and Undervoltages????

9.5.1 Voltage Drop and Regulation [Bosela Ch. 8, Pg. 239-286]????

9.5.2 Voltage Support with VAR Compensation [Bosela Ch. 9, Pg. 287-331]????

9.6 FLICKER????

9.7 POWER SYSTEM HARMONICS [BOSELA CH. 13, PG. 457-485]????

10 POWER SYSTEM INTEGRATION AND AUTOMATION

10.3 TRENDS IN POWER SYSTEM PROTECTION[93]

10.4 SUBSTATION AUTOMATION [94,95]

11 APPENDIX

11.1 APPENDIX I STANDARD TIME OVERCURRENT CHARACTERISTIC CURVES

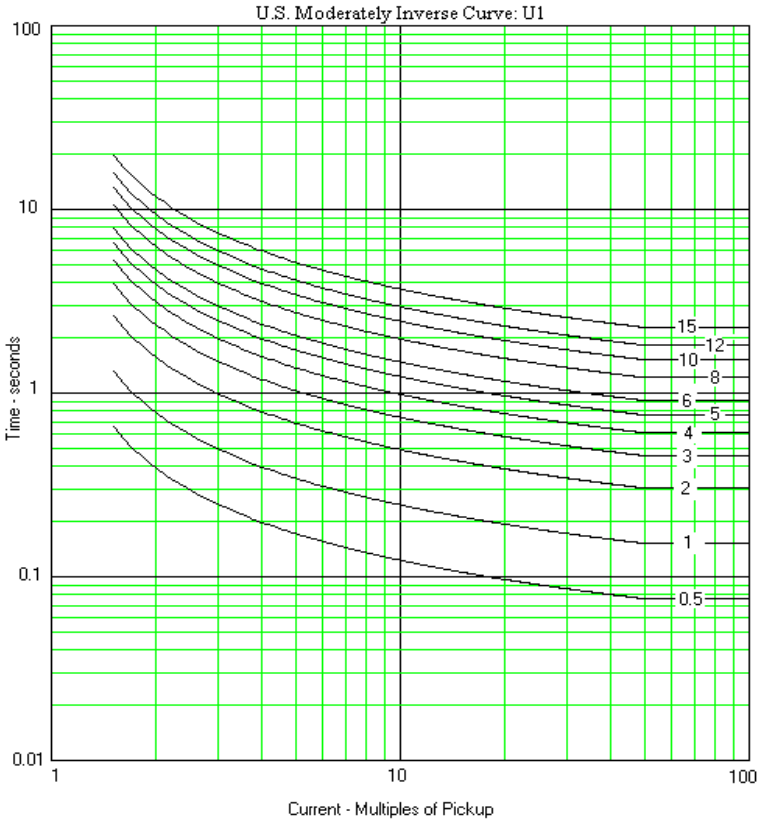


Figure 11.1: Family of Time-Overcurrent Curves for Various Time-Dial Settings for Type U.S. Moderately Inverse Curve U1

$$Tt = TD\left(0.0226 + \frac{0.014}{M^{0.02} - 1}\right) \qquad \text{Equation 11.1}$$

$$Tr = TD\left(\frac{1.108}{1 - M^{2}}\right) \qquad \text{Equation 11.2}$$

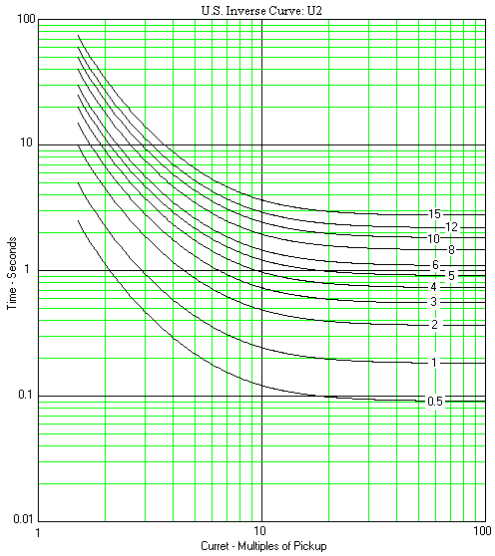


Figure 11.2: Family of Time Overcurrent Curves for Various Time-Dial Settings for U.S. Inverse Curve U2

$$Tt = TD\left(0.180 + \frac{5.95}{M^2 - 1}\right) \qquad \text{Equation 11.3}$$

$$Tr = TD\left(\frac{5.95}{1 - M^2}\right) \qquad \text{Equation 11.4}$$

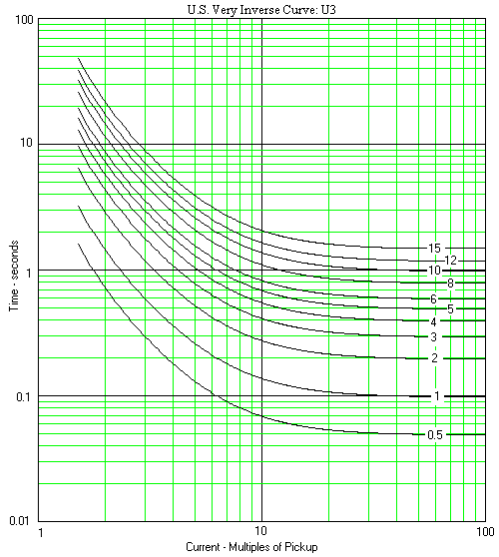


Figure 11.3: Family of Time Overcurrent Curves for Various Time-Dial Settings for U.S. Very Inverse Curve U3

$$Tt = TD\left(0.0963 + \frac{3.88}{M^2 - 1}\right) \qquad \text{Equation 11.5}$$

$$Tr = TD\left(\frac{3.88}{1 - M^2}\right) \qquad \text{Equation 11.6}$$

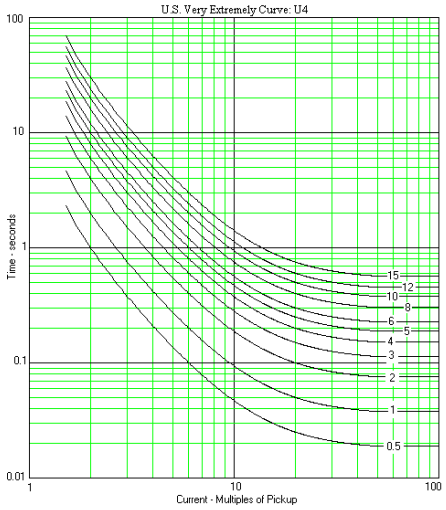


Figure 11.4: Family of Time Overcurrent Curves for Various Time-Dial Settings for U.S. Extremely Inverse Curve U4

$$Tt = TD\left(0.0352 + \frac{5.67}{M^2 - 1}\right) \qquad \text{Equation 11.7}$$

$$Tr = TD\left(\frac{5.67}{1 - M^2}\right) \qquad \text{Equation 11.8}$$

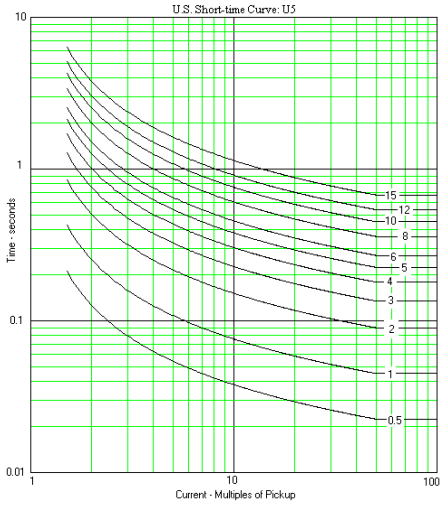


Figure 11.5: Family of Time Overcurrent Curves for Various Time-Dial Settings for U.S. Short-Time Inverse Curve U5

$$Tt = TD\left(0.00262 + \frac{0.00342}{M^{0.02} - 1}\right) \qquad \text{Equation 11.9}$$

$$Tr = TD\left(\frac{0.323}{1 - M^{2}}\right) \qquad \text{Equation 11.10}$$

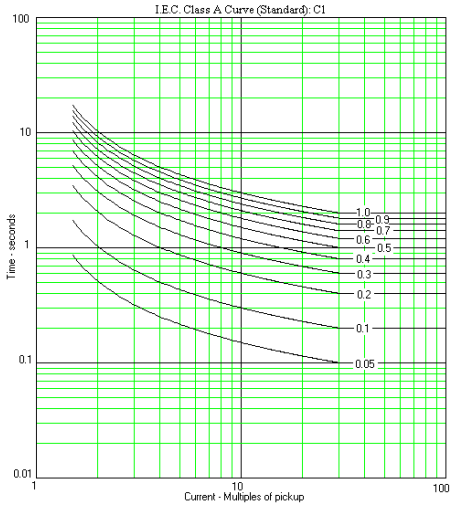


Figure 11.6: Family of Time Overcurrent Curves for Various Time-Dial Settings for I.E.C. Class A Curve (Standard Inverse) C1

$$Tt = TD\left(\frac{0.14}{M^{0.02} - 1}\right) \qquad \text{Equation 11.11}$$

$$Tr = TD\left(\frac{13.5}{1-M^2}\right) \qquad \text{Equation 11.12}$$

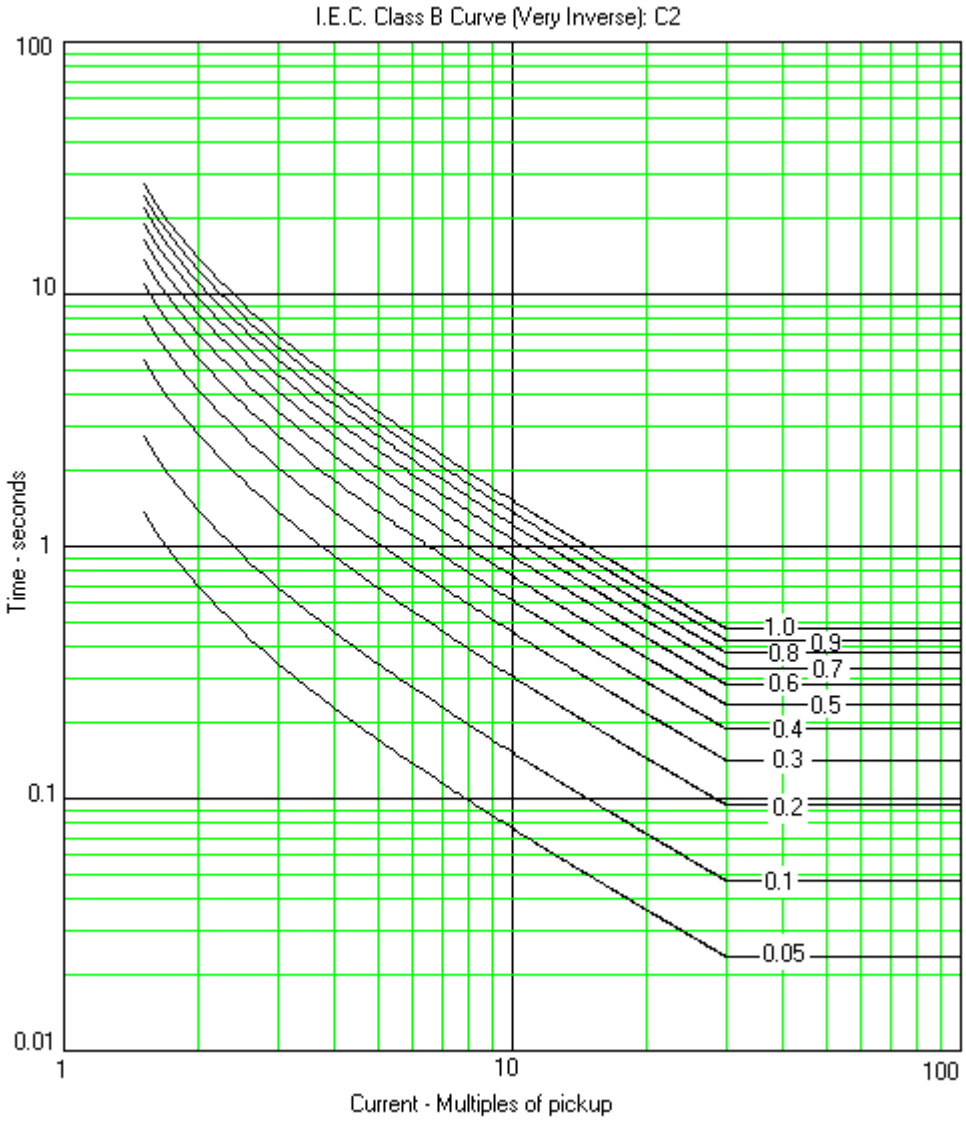


Figure 11.7 Family of Time Overcurrent Curves for Various Time-Dial Settings for I.E.C. Class B Curve (Very Inverse) C2

$$Tt = TD\left(\frac{13.5}{M^2-1}\right) \qquad \text{Equation 11.13}$$

$$Tr = TD\left(\frac{47.3}{1-M^2}\right) \qquad \text{Equation 11.14}$$

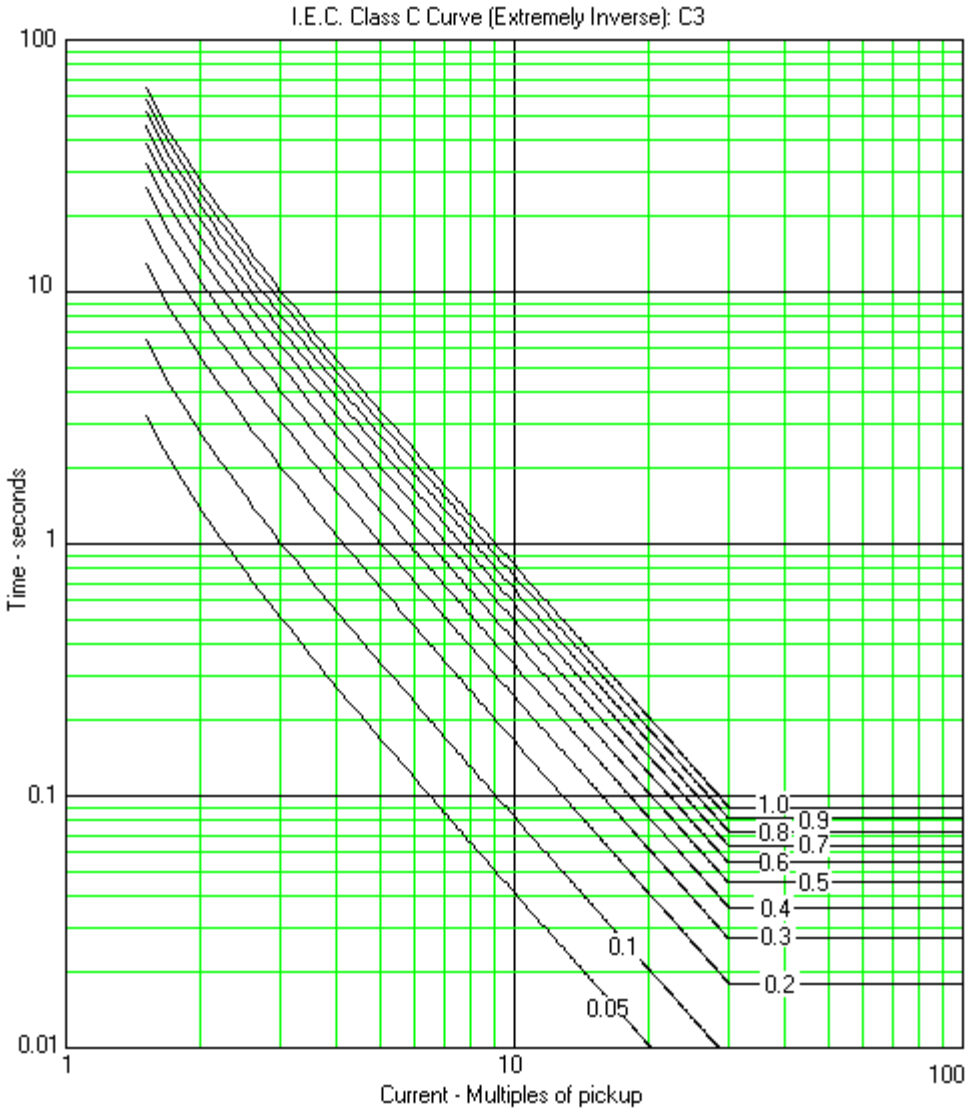


Figure 11.8: Family of time overcurrent curves for various time-dial settings for type I.E.C. Class C curve (extremely inverse) C3.

$$Tt = TD\left(\frac{80.0}{M^2 - 1}\right) \qquad \text{Equation 11.15}$$

$$Tr = TD\left(\frac{80.0}{1 - M^2}\right) \qquad \text{Equation 11.16}$$

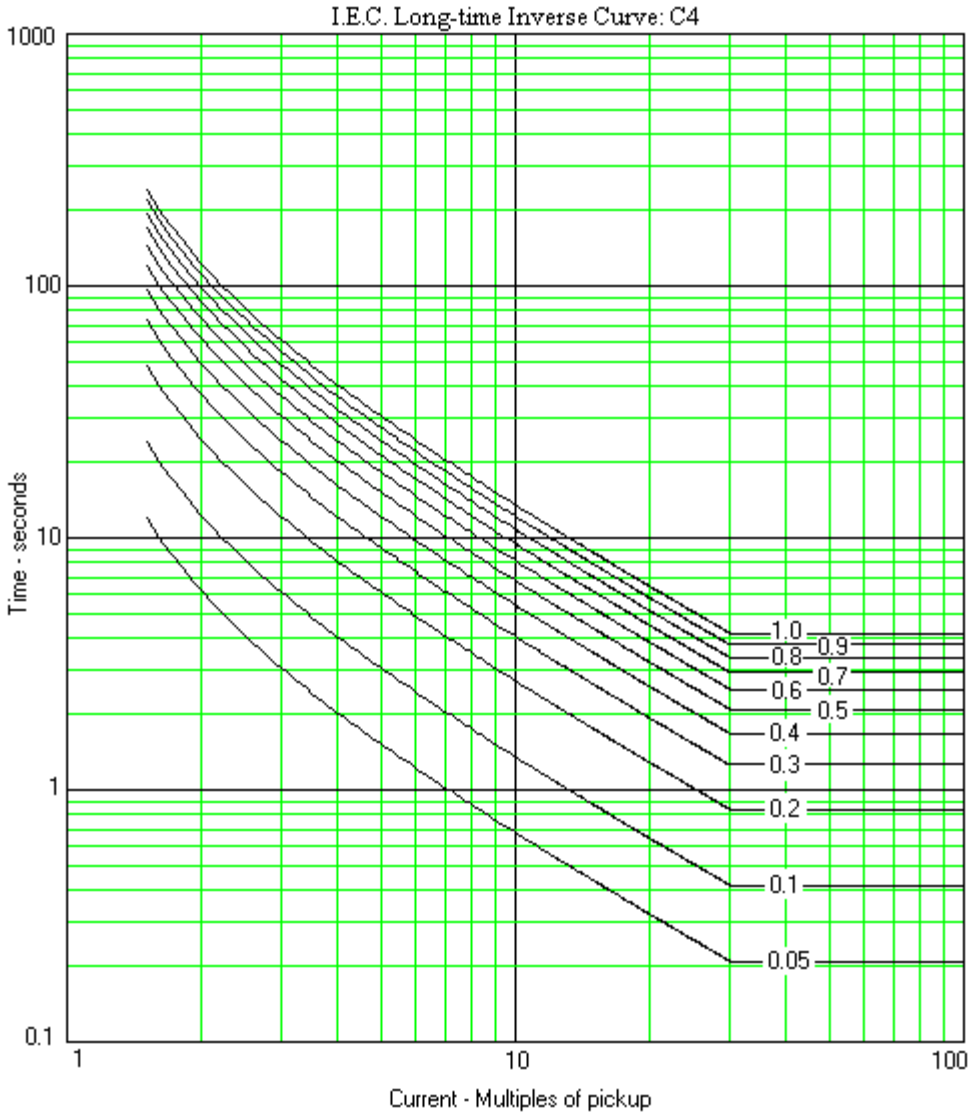


Figure 11.9: Family of Time Overcurrent Curves for Various Time-Dial Settings for I.E.C. Class C Curve (Long-Time Inverse) C4

$$Tt = TD\left(\frac{120.0}{M^2 - 1}\right) \qquad \text{Equation 11.17}$$

$$Tr = TD\left(\frac{120.0}{1 - M^2}\right) \qquad \text{Equation 11.18}$$

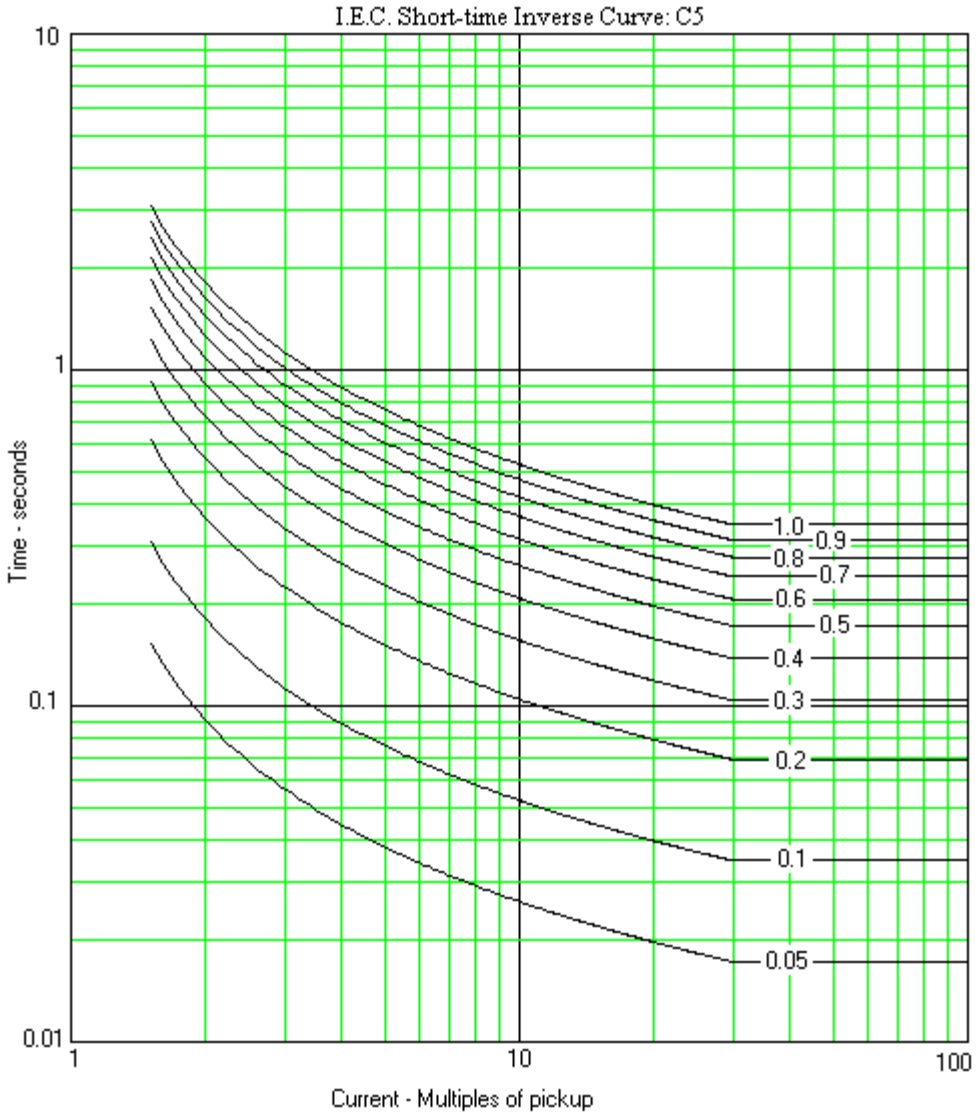


Figure 11.10: Family of Time Overcurrent Curves for Various Time-Dial Settings for I.E.C. Class C Curve (Short-Time Inverse) C5.

$$Tt = TD\left(\frac{0.05}{M^{-0.04}-1}\right) \qquad \text{Equation 11.19}$$

$$Tr = TD\left(\frac{4.85}{1-M^{2}}\right) \qquad \text{Equation 11.20}$$

11.2 APPENDIX II. TRANSMISSION LINE PARAMETERS CALCULATIONS

File name: XLine.prm

Description: 440 KV Transmission Line

Number of Phases	Operating Frequency	Ground Restivity	Number of Conductors in Bundle	Bundle Diameter (in)
3	60.0	1000	4	15.73

Phase Conductor and tower information

Conductor Number	Conductor Diameter (inches)	Conductor Resistance Ω/mile	GMR (1 foot spacing)	Conductor Height (feet)	Mid-span Sag (feet)	Horizontal Position (feet)
1	0.990	0.147	0.0329	78.89	44.02	-30.38
2	0.990	0.147	0.0329	90.96	44.02	0.0
3	0.990	0.147	0.0329	78.89	44.02	30.38

Ground Conductor and tower information

Conductor Number	Conductor Diameter (inches)	Conductor Resistance Ω/mile	GMR (1 foot spacing)	Conductor Height (feet)	Mid-span Sag (feet)	Horizontal Position (feet)
S1	0.375	3.5	0.01195	118.0	20.98	-24.7
S2	0.375	3.5	0.01195	118.0	20.98	24.7

Unbalanced lumped and Π parameter line model

Line Resistance and Induction Matrix					
Resistance (Ω/mile)			Inductance (mH/mile)		
0.419458	0.0931581	0.0931575	3.01367	2.20603	1.98293
0.0931581	0.419458	0.0931581	2.20603	3.01367	2.20603
0.0931575	0.0931581	0.419458	1.98293	2.20603	3.01367

Capacitance Matrix (μF/mile)		
0.0143964	-0.00467317	-0.00251761
-0.00467317	0.0154731	-0.00467317
-0.00251761	-0.00467317	0.0143964

Balanced lumped and Π parameter line model

Phase parameters: R,L, and C		
Rs = 0. 245702 Ω/mile	Ls = 3.01367 mH/mile	Cs = 0.014014200 μF/mile
Rm = 0.208563 Ω/mile	Lm = 2.13167 mH/mile	Cm = 0.00165198 μF/mile

Sequence parameters: R,L, and C		
R0 = 0. 662828 Ω/mile	L0 = 6.06001 mH/mile	C0 = 0.0107102 μF/mile
R1 = 0.0371397 Ω/mile	L1 = 1.89554 mH/mile	C1 = 0.0156662 μF/mile

Balanced Line Sequence parameters, Surge impedance and travel time	
Z0 = 767.559 Ω/mile	τ0 = 8.05632 μs/mile
Z1 = 348.078 Ω/mile	τ1 = 5.44938 μs/mile

11.3 APPENDIX III. FEEDER LINE PARAMETERS CALCULATIONS

File name: Feeder.prm

Description: 34.5 KV Feeder

Number of Phases	Operating Frequency	Ground Restivity	Number of Conductors in Bundle	Bundle Diameter (in)

3	60.0	100	1	0

Conductor and tower information

Conductor Number	Conductor Diameter (inches)	Conductor Resistance Ω/mile	GMR (1 foot spacing)	Conductor Height (feet)	Mid-span Sag (feet)	Horizontal Position (feet)
1	0.72	0.3263	0.244	35.0	8.0	-3.0
2	0.72	0.3263	0.244	35.0	8.0	0.0
3	0.72	0.3263	0.244	35.0	8.0	3.0

Unbalanced lumped and Π parameter line model

Line Resistance and Induction Matrix					
Resistance (Ω/mile)			Inductance (mH/mile)		
0.419458	0.0931581	0.0931575	3.01367	2.20603	1.98293
0.0931581	0.419458	0.0931581	2.20603	3.01367	2.20603
0.0931575	0.0931581	0.419458	1.98293	2.20603	3.01367

Capacitance Matrix (μF/mile)		
0.0143964	-0.00467317	-0.00251761
-0.00467317	0.0154731	-0.00467317
-0.00251761	-0.00467317	0.0143964

Balanced lumped and Π parameter line model

Phase parameters: R,L, and C		
Rs = 0.419458 Ω/mile	Ls = 3.01367 mH/mile	Cs = 0.0147553 μF/mile

Rm = 0.0931579 Ω/mile	Lm = 2.13167 mH/mile	Cm = 0.00395465 μF/mile

Sequence parameters: R,L, and C		
R0 = 0.605774 Ω/mile	L0 = 7.27700 mH/mile	C0 = 0.00684598 μF/mile
R1 = 0.326300 Ω/mile	L1 = 8.82000 mH/mile	C1 = 0.0187099 μF/mile

Balanced distributed parameter line model

Balanced Line Sequence parameters, Surge impedance and travel time	
Z0 = 1043.34 Ω/mile	τ0 = 7.0597 μs/mile
Z1 = 256.998 Ω/mile	τ1 = 4.06228 μs/mile

11.4 APPENDIX IV – TIME-CURRENT FOR T TYPE FUSES

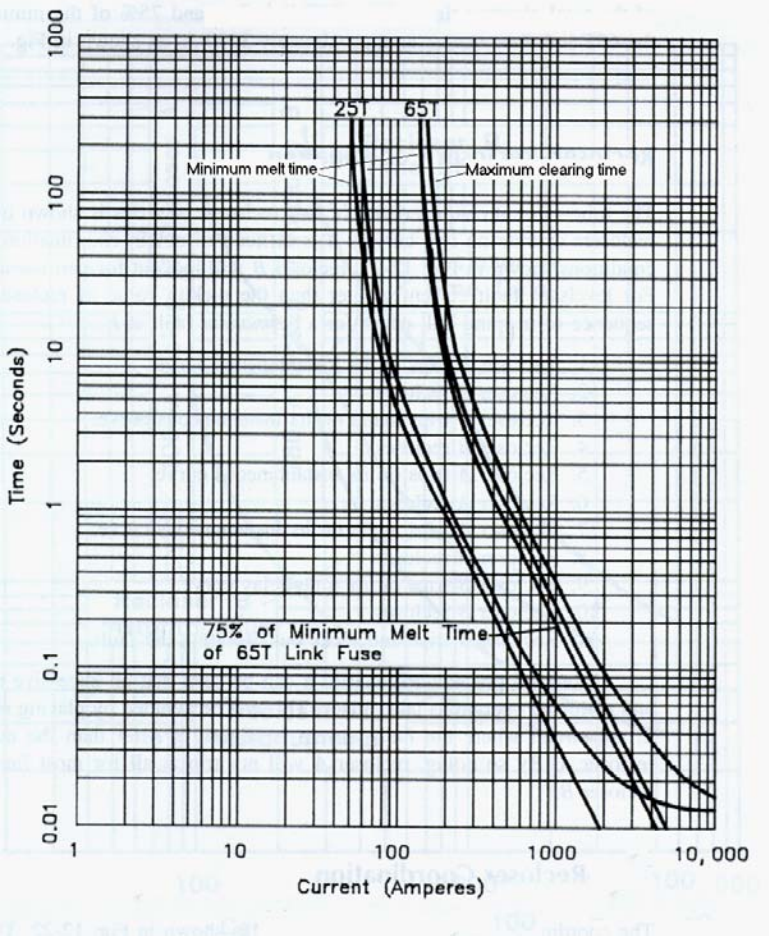


Figure 11.11: Time Current Characteristics for 25T and 65T Fuses

APPENDIX V - FAULT CALCULATIONS FOR COORDINATION EXAMPLE #1 MATHCAD PROGRAM TO COMPUTE OVERCURRENT TIME COORDINATION

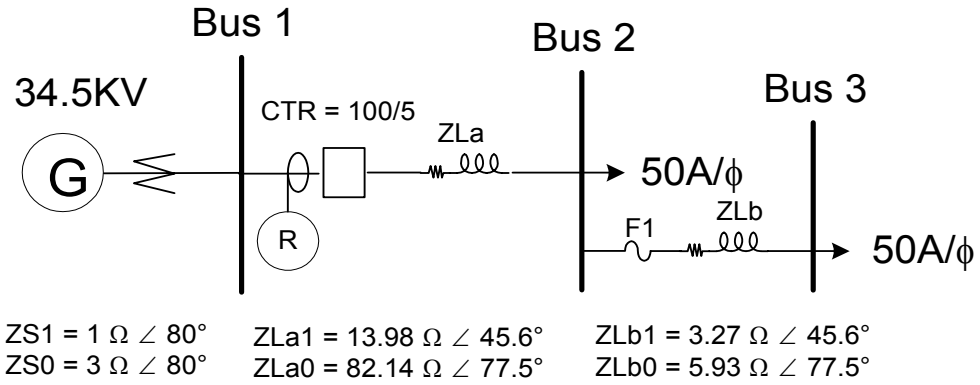


Figure 11.12: Radial Line Single-Line Diagram (1)

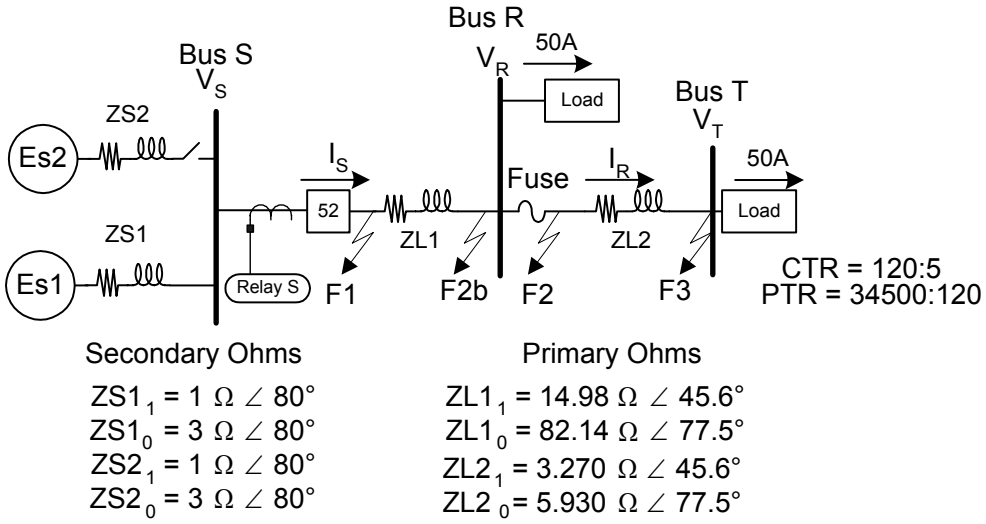


Figure 11.13: Radial Line Single-Line Diagram (2)

System Constants

$Vs := 34500$ $\quad CTR := \frac{100}{5}$ $\quad CTI := 0.3$ $\quad a := \cos\left(2\frac{\pi}{3}\right) + \sin\left(2\frac{\pi}{3}\right) i$

Phase Faults
Fault Current at Bus 2

Three-phase $If3\phi\ 2 := \dfrac{\left(\dfrac{Vs}{\sqrt{3}}\right)}{(Zs1 + ZLa1)}$ $|If3\phi\ 2| = 1.345 \cdot 10^3$ $\arg(If3\phi\ 2) = -47.788 \cdot deg$

Phase-to-phase $If\phi\phi\ 2 := \left(\dfrac{\sqrt{3}}{2}\right) \cdot If3\phi\ 2$ $|If\phi\phi\ 2| = 1.164 \cdot 10^3$ $\arg(If\phi\phi\ 2) = -47.788 \cdot deg$

Phase Faults
Fault current at Bus 3

Three-phase $If3\phi\ 3 := \dfrac{\left(\dfrac{Vs}{\sqrt{3}}\right)}{(Zs1 + ZLa1 + ZLb1)}$ $|If3\phi\ 3| = 1.023 \cdot 10^3$ $\arg(If3\phi\ 3) = -47.288 \cdot deg$

Phase-to-phase $If\phi\phi\ 3 := \left(\dfrac{\sqrt{3}}{2}\right) \cdot If3\phi\ 3$ $|If\phi\phi\ 3| = 886.184$ $\arg(If\phi\phi\ 3) = -47.288 \cdot deg$

Fuse Calculations

Fuse Clearing Times Determined From 60E Fuse Chart $Fuse := 60$

Faults at Bus 2

$Mfmax := \dfrac{|If3\phi\ 2|}{Fuse}$

$Mfmax = 22.409$

$Tf2 := 0.06$

Faults at Bus 3

$Mfmin := \dfrac{|If\phi\phi\ 3|}{Fuse}$

$Mfmin = 14.77$

$Tf3 := 0.09$

Relay Calculations for Phase Faults

Faults at Bus 2

$Tap := \left(\dfrac{|If\phi\phi\ 3|}{CTR \cdot Mfmin}\right)$

Round tap to next highest integer.

Faults at Bus 3

$Tap = 3$

$Tap := 3$

Calculate M for relay at Bus 2 and Bus 3 - no load.

Faults at Bus 2

$MRB2 := \dfrac{|If\phi\phi\ 2| + 0}{CTR \cdot Tap}$

Faults at Bus 3

$MRB3 := \dfrac{|If\phi\phi\ 3|}{CTR \cdot Tap}$

$MRB2 = 19.406$ $MRB3 = 14.77$

Phase Faults
Calculate TDS for relay type U4 at Bus 2 and Bus 3 - no load.

Faults at Bus 2

$Tt2 := Tf2 + CTI$

$Tt2 = 0.36$

$$TDS2 := \frac{Tt2}{\left[0.0352 + \left(\frac{5.67}{MRB2^2 - 1}\right)\right]}$$

$TDS2 = 7.158$

Faults at Bus 3

$Tt3 := Tf3 + CTI$

$Tt3 = 0.39$

$$TDS3 := \frac{Tt3}{\left[0.0352 + \left(\frac{5.67}{MRB3^2 - 1}\right)\right]}$$

$TDS3 = 6.361$

Calculate CTI margin at full load.

$$Tt2 := TDS2 \cdot \left[0.0352 + \left[\frac{5.67}{(MRB2 + 50)^2 - 1}\right]\right]$$

$Tt2 - CTI = -0.04$

$$Tt3 := TDS2 \cdot \left[0.0352 + \left[\frac{5.67}{(MRB3 + 50)^2 - 1}\right]\right]$$ [5]

$Tt3 - CTI = -0.038$

Calculate TDS for relay type U4 - full load.

$$MRB2 := \frac{|If\phi\phi\ 2| + 50}{CTR \cdot Tap}$$

Time to trip at full load

$$TDS2 := \frac{Tt2}{\left[0.0352 + \left(\frac{5.67}{MRB2^2 - 1}\right)\right]}$$

Error! Objects cannot be created from editing field codes.

$Tt2 := Tf2 + CTI$

$Tt2 = 0.36$

TDS including full load

$TDS2 = 7.336$

Ground Faults
Compute phase impedances.

$Zss := (Zs0 + 2 \cdot Zs1)$ $ZLas := (ZLa0 + 2 \cdot ZLa1)$ $ZLbs := (ZLb0 + 2 \cdot ZLb1)$

[5] *Relay tripping times at full load TDS2 is used here because only the maximum is chosen.*

Bus 2

$$If\phi g2 := \frac{\left(\frac{Vs}{\sqrt{3}}\right)}{(Zss + ZLas)} \qquad |If\phi g2| = 178.13 \qquad \arg(If\phi g2) = -70.02 \cdot deg$$

Bus 3

$$If\phi g3 := \frac{\left(\frac{Vs}{\sqrt{3}}\right)}{(Zss + ZLas + ZLbs)} \qquad |If\phi g3| = 135.089 \qquad \arg(If\phi g3) = -69.914 \cdot deg$$

Fuse Calculations

Fuse clearing times determined from 60E fuse chart $Fuse := 60$

Faults at Bus 2	**Faults at Bus 3**
$Mgfmax := \frac{\lvert If\phi g2 \rvert}{Fuse}$	$Mgfmin := \frac{\lvert If\phi g3 \rvert}{Fuse}$
$Mgfmax = 2.969$	$Mgfmin = 2.251$
$Tf2 := 1$	$Tf3 := 1.3$

Relay calculations for ground faults at no load

Faults at Bus 2	**Faults at Bus 3**
$Io2 := 1 \cdot If\phi g2$	$Io3 := 1 \cdot If\phi g3$
$\lvert Io2 \rvert = 178.13$	$\lvert Io3 \rvert = 135.089$
$Tap := \left(\frac{\lvert Io2 \rvert}{CTR \cdot Mgfmin}\right)$	$Tap = 3.956$
Round tap to next highest integer.	$Tap := 4$

Calculate M for relay at Bus 2 and Bus 3 - no load.

Faults at Bus 2	**Faults at Bus 3**
$MRB2 := \frac{\lvert Io2 \rvert}{CTR \cdot Tap}$	$MRB3 := \frac{\lvert Io3 \rvert}{CTR \cdot Tap}$
$MRB2 = 2.227$	$MRB3 = 1.689$

Calculate TDS for relay type U4 - no load.

$Tt2 := Tf2 + CTI$	$Tt3 := Tf3 + CTI$

$Tt2 = 1.3$

$$TDS2 := \frac{Tt2}{\left[0.0352 + \left(\frac{5.67}{MRB2^2 - 1}\right)\right]}$$

$TDS2 = 0.886$

$Tt3 = 1.6$

$$TDS3 := \frac{Tt3}{\left[0.0352 + \left(\frac{5.67}{MRB3^2 - 1}\right)\right]}$$

$TDS3 = 0.517$

Relay calculations for ground faults at no load.

Faults at Bus 2

$$Io2 := 1 \cdot \left(If_{\phi}\, g2 + 50 \cdot a + 50 \cdot a^2\right)$$

$|Io2| = 167.761$

Faults at Bus 3

$$Io3 := 1 \cdot \left(If_{\phi}\, g3 + 50\, a + 50 \cdot a^2\right)$$

$|Io3| = 126.924$

Calculate M for relay at Bus 2 and Bus 3 - full load.

$$MRB2 := \frac{|Io2|}{CTR \cdot Tap}$$

$MRB2 = 2.097$

$$MRB3 := \frac{|Io3|}{CTR \cdot Tap}$$

$MRB3 = 1.587$

Verify relay tripping times at full load.

$$Tt2 := TDS2 \cdot \left[0.0352 + \left[\frac{5.67}{(MRB2 + 50)^2 - 1}\right]\right]$$

$Tt2 - CTI = -0.267$

$Tt2 = 0.033$

$$Tt3 := TDS2 \cdot \left[0.0352 + \left[\frac{5.67}{(MRB3 + 50)^2 - 1}\right]\right]$$

$Tt3 - CTI = -0.267$

$Tt3 = 0.033$

11.6 APPENDIX VI CBEMA CURVE

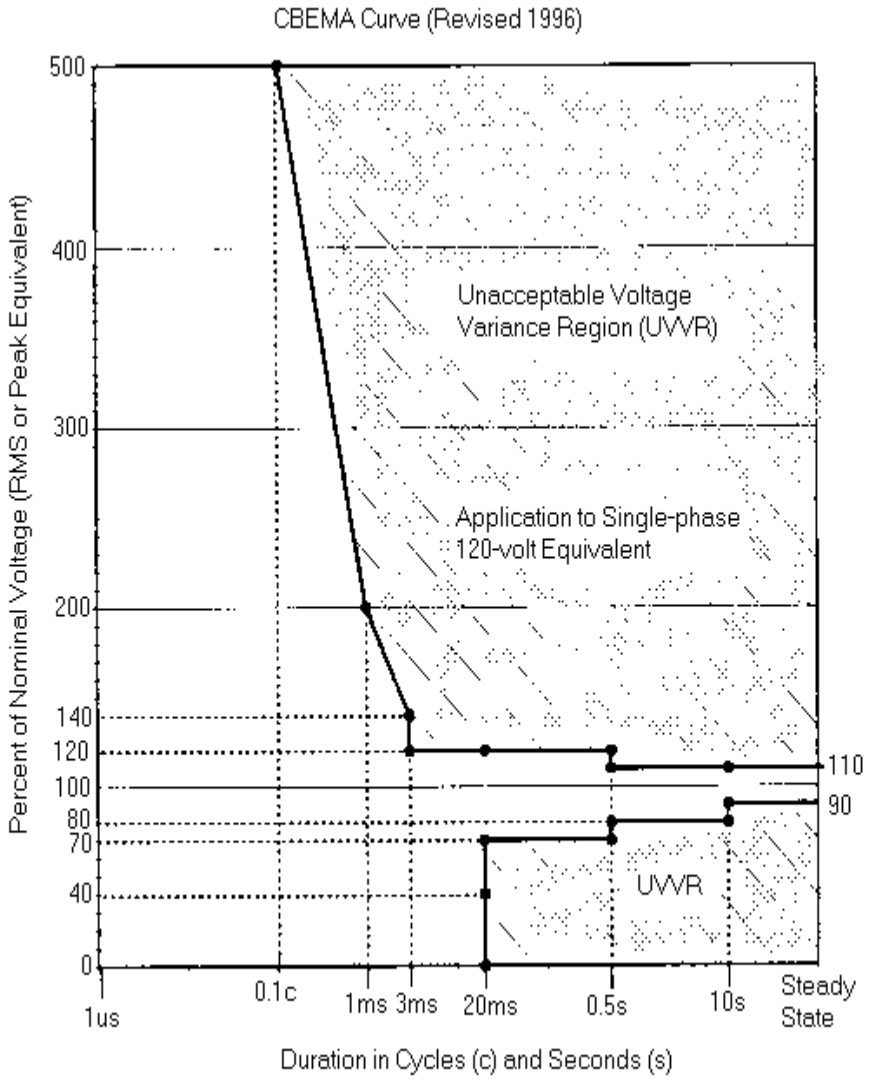


Figure 11.14: CMEMA Curve

11.7 APPENDIX VII. NETWORK THEORY - METHODS FOR GENERATING A SIMPLE FAULT STUDY USING MATHCAD

11.7.1 Introduction

The understanding of relay operations begins with a thorough knowledge of the power system it is designed to protect. Before the days of personal computers and engineering mathematics programs such as Matlab, Mathcad, Solver Q engineers relied on “back of the envelope” calculations to provide ballpark estimates. These

estimates are important to verify that data is being used properly in more complex and detailed programs for calculating system load flow and fault studies. The following discussion describes the process of generating a simple Mathcad program to analyze faults on the two-source system shown in Figure 11.15.

The general approach for modeling an electrical network is to first build an admittance matrix representing the branches between nodes in the system. Next, dividing the voltage sources by the respective source impedance generates a current vector. The inverse of the admittance matrix is multiplied times the current vector to compute all the node voltages. Individual branch currents are then computed as the voltage difference between two nodes divided by the impedance between them.

The reason the computer is handy is that the programs are extremely efficient when trying to solve a large number of simultaneous equations. Even for the simple system shown in Figure 11.15, 12 simultaneous equations must be solved to compute the four three-phase nodes. Inverting a matrix larger than three by three should only be done once in any ones lifetime.

In the process that follows, note that only node increase the size of the system matrix and additional branches between existing nodes to not. Consequently, a parallel line between nodes two and four can be simply added as well as additional loads at any existing bus.

11.7.2 System Considerations and the Single line diagram

The single line diagram is critical to knowing where the desired mathematical reside in the solution vectors. The order that data is entered into the current vector and admittance matrix is completely arbitrary but consistency is required. For the system considered here, we have chosen to number the nodes from right to left simply for convenience. For the system shown in Figure 11.15 eventually, the 12 simultaneous equations shown in Figure 11.16 will need to be solved. Fortunately for us today, the engineering programs previously mentioned handle matrices and vectors with almost the same degree of ease as scalar mathematics. If the admittance for each node is grouped as a 3 by 3 matrix, then the mathematics can be viewed as the four by four matrix shown in Figure 11.17. The engineering program still must solve all 12 equations shown in Figure 11.16. The methodologies for generating the three by three matrices and grouping them to form the 12 by 12 matrix will be presented in the following sections.

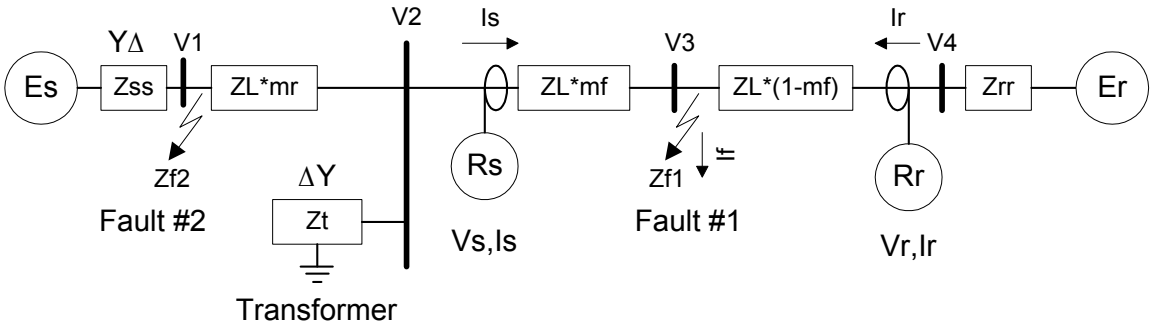


Figure 11.15: Single Line Diagram for Simplified Fault Analysis Study

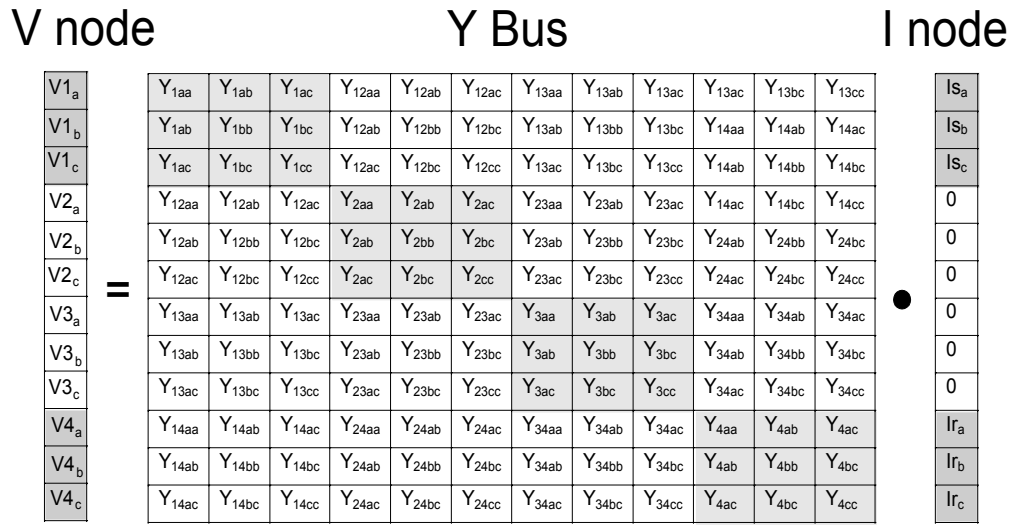


Figure 11.16: The12 Simultaneous Equations for Solving Node Voltages

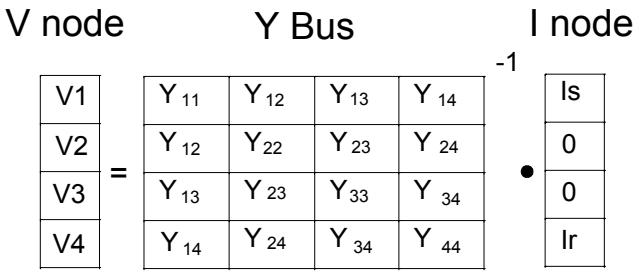


Figure 11.17: Simultaneous Equations for Solving Node Voltages on a Three-Phase Basis

With each block in Figure 11.15 now representing a three by three matrix of complex impedances, the task at hand now becomes that of determining what data should be used. This information may be gathered from other engineering studies or from manufacturers data. In any event, the results cannot be any more accurate than the accuracy of the data used in the model. The many simplifying assumptions will also affect the validity of the results and care is required to know what level of detail is sufficient for the desired results. On approach is to start with the most simple system possible that is made with the most relaxed assumptions possible. The results from this model are saved for later comparison. Next add a degree of additional detail to the element of the model that, in your judgment, represents the most egregious of assumptions. Compare those results with that of the more simplified model. If the differences in results are significant then additional detail may be requires for this model. This process represents a sensitivity analysis and leads to understanding of what kind of issues or detail that most affect the validity of the model.

For example, assume that initially the transmission lines are modeled as balanced inductors. The next level of detail is to add the line resistance. A further level of

detail is to insist that the lines be modeled as unbalanced lines. Finally, the line capacitance may be added to the model.

11.7.3 Building the impedance models

Although we will discuss methods of building impedance models using symmetrical component theory, the network admittance matrix must be in the phase domain.

11.7.3.1 Source Impedance

Source impedances represent the entire electrical network between the ideal generators and point that your model begins. This includes generators and transformers as well as line impedance and compensation. This impedance is usually obtained from a more complete fault study. Without such information you may make assumptions based upon the perceived strength of the source. Strong sources have impedances that are significantly lower than the modeled network impedance. Rarely is capacitive reactance included in the equivalent source impedance unless there is a good basis for doing so.

Frequently, the source impedance must include a wye-delta transformer, which precludes that source from supplying zero sequence current. In this case, it is convenient if the source impedance is specified as positive and negative sequence components. One assumption that is usually viable is that the positive and negative sequence impedances are equal.

Let us assume that we want to model the *Zss* in Figure 11.15. Since the delta side of the transformer blocks zero sequence current, the zero sequence impedance is set very large. For this example we will also assume that the positive and negative impedance are equal. At this point we have two methods of getting the phase domain impedance matrix. One way is the use the formal definition described by Equation 2.77 in section 0. Since we are assuming balanced source impedance, we can also use equations Equation 11.21 and Equation 11.22. Either way results in the balanced matrix, Equation 11.23.

$$Zs = \left(Z0 + 2\,Z1\right)\Big/_{3} \qquad \text{Equation 11.21}$$

$$Zm = \left(Z0 - Z1\right)\Big/_{3} \qquad \text{Equation 11.22}$$

$$Zss = \begin{bmatrix} Zs & Zm & Zm \\ Zm & Zs & Zm \\ Zm & Zm & Zs \end{bmatrix} \qquad \text{Equation 11.23}$$

11.7.3.2 Transformer Impedance

The purpose of the delta-ground wye transformer at Bus 2 is to provide a source for polarizing zero sequence current that will be used in some relay studies. The approach to generating the matrix is almost identical as that for the source impedance. Since the residual current is used for polarizing the magnitude is not critical as long as it is of sufficient magnitude that it does not lead to numerical

inaccuracies. Both the positive and negative impedance can be made to be the same. High positive and negative impedance represents a high impedance load on the secondary side. The zero sequence impedance can be made represent impedance in the neutral ground connection. This impedance can be complex or purely resistive and should be kept small, even zero.

11.7.3.3 Line Impedance

Line impedance data generally comes form a line constant parameter program that converts tower construction data and conductor dimensions to impedance matrices. (See section 0). If a balanced line model is to be used but only data for an unbalanced line is available, simply make the mutual impedance term equal to the average of the off-diagonal terms and the self-impedance equal to the average of the diagonal terms. Since the line impedance is linear with respect to length, the position of the fault bus is arbitrarily set by the per unit multiplier, *m*. As shown in **Error! Reference source not found.**, the line length between *V2* and *V4* remains constant while the relative location of bus V3 varies as the multiplier *mf* varies. The length of the line between *V1* and *V2* is set by the multiplier *mr*.

11.7.3.4 Fault Impedance

The fault matrix shown in **Error! Reference source not found.** represents the ten types of possible faults. The six impedances are all kept very large (on the order of 1 mega ohm) for open circuit elements. **Error! Reference source not found.** shows the combinations for generating the various fault types. Values for fields labeled "small" are set to represent the fault impedance. These values should be positive and greater than a micro ohm to avoid computational errors. Other combinations not listed in **Error! Reference source not found.** are also possible. For example, to model a phase A to phase B to ground fault with different impedances, one needs to specify *Zaa*, *Zbb*, and *Zab*. Faults represented by this matrix do not need to be symmetrical.

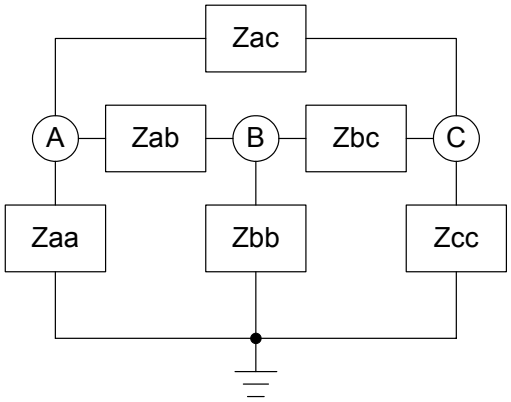


Figure 11.18: Fault Matrix Diagram

Table 11.1: Fault Types

Fault type	Zaa	Zbb	Zcc	Zab	Zbc	Zac
AG	Small					
BG		Small				
CG			Small			
AB				Small		
BC					Small	
CA						Small
ABG	Small	Small				
BCG		Small	Small			
CAG	Small		Small			
ABC	Small	Small	Small			

The fault matrix is computed according to Equation 11.24. It is constructed by applying common nodal analysis techniques. The diagonal terms are the sum of all admittances connecting that node with any other node including the reference (or ground) node. The off diagonal terms are the negative of the admittances between node under consideration and the connected node. For realizable passive networks, the admittance matrix (and subsequently the resulting impedance matrix) is symmetrical. Applying these rules, admittance matrices can be written from inspection of the electrical network diagram. Inverting the fault admittance matrix generates the fault impedance.

$$Zf = \begin{bmatrix} \left(Zaa^{-1} + Zab^{-1} + Zac^{-1}\right) & -Zab^{-1} & -Zac^{-1} \\ -Zab^{-1} & \left(Zbb^{-1} + Zab^{-1} + Zbc^{-1}\right) & -Zcb^{-1} \\ -Zac^{-1} & -Zcb^{-1} & \left(Zcc^{-1} + Zac^{-1} + Zcb^{-1}\right) \end{bmatrix}^{-1} \quad \text{Equation 11.24}$$

According to the circuit in Figure 11.15, there are two fault buses, *V1* and *V3*. The distance from *V2* to *V1* and *V3* to is set by constants *mr* and *mf* respectively. The larger *mf* is set, the greater the impedance between *V1* and *V2* regardless of the fault matrix values for either *F1* or *F2*.

11.7.4 Building the source models

As suggested in earlier discussions, the known sources are modeled as ideal current sources. This is accomplished by dividing the source voltage by the source impedance. Applying Kirchhoff's current law to node *V1* shown in Figure 11.19 results in Equation 11.25. Rearranging these terms to group coefficients of the node voltages generates equation Equation 11.26 that has six unknowns: three phase

voltages for *V1* and *V2*. The reason admittances are explicitly expressed as the inverse of the impedance is to remind us that these involve matrix operations. As such, for multiplication, the order is important and for addition and subtraction, the matrix dimensions must be the same.

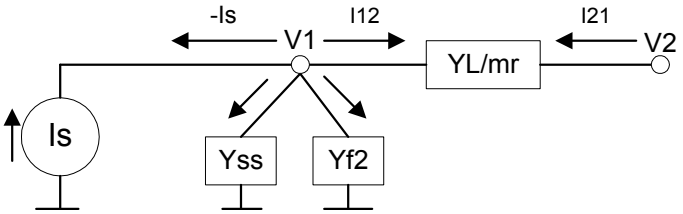


Figure 11.19: Sum of Currents for Node V1

$$(Yss + Yf2)\cdot V1 + (YL/mr)\cdot(V1 - V2) - Is = 0 \qquad \text{Equation 11.25}$$

where:

$Is = Yss \cdot Es$

$Yss = Zss^{-1}$

$Yf2 = Zf2^{-1}$

$YL = ZL^{-1}$

$$(Yss + Yf2 + (YL/mr))\cdot V1 - (YL/mr)\cdot V2 = Is \qquad \text{Equation 11.26}$$

11.7.5 Generating the system admittance matrix

Up to this point, procedures for generating all the impedance models needed for the circuit shown in Figure 11.15 have been discussed. The first three simultaneous equations are presented in section 11.7.4 above. Using the same procedure that resulted in Equation 11.26, the remaining nine simultaneous equations, Equation 11.27through Equation 11.29, can be written from inspection of the node single line drawings.

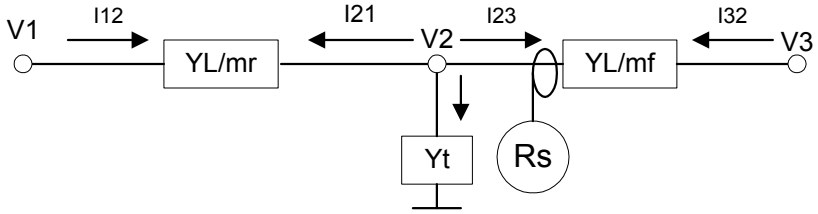


Figure 11.20: Sum of Currents for Node V2

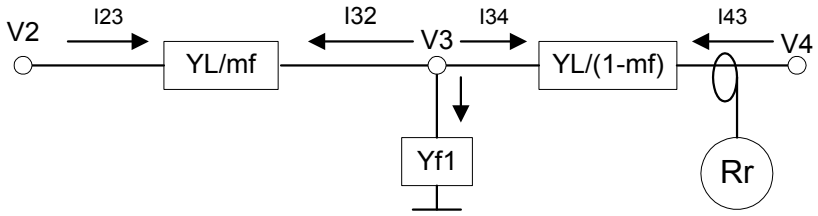


Figure 11.21: Sum of currents for node V3

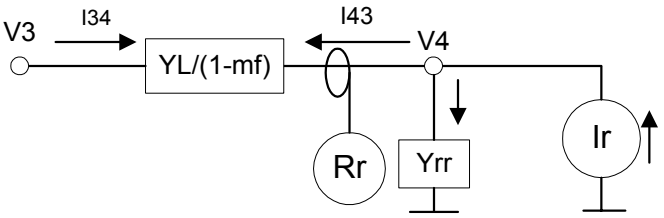


Figure 11.22: Sum of Currents for Node V4

$$-\left(YL/_{mr}\right)\cdot V1+\left[\left(YL/_{mr}\right)+Yt+\left(YL/_{mf}\right)\right]\cdot V2-\left(YL/_{mf}\right)\cdot V3=0 \qquad \text{Equation 11.27}$$

where:

$Yt=Zt^{-1}$

$YL=ZL^{-1}$

$$-\left(YL/_{mf}\right)\cdot V2+\left[\left(YL/_{mf}\right)+Yf1+\left(YL/_{(1-mf)}\right)\right]\cdot V3 -\left(YL/_{(1-mf)}\right)\cdot V4=0 \qquad \text{Equation 11.28}$$

where:

$Yf1=Zf1^{-1}$

$$-\left(YL/_{(1-mf)}\right)\cdot V3+\left[Yrr+\left(YL/_{(1-mf)}\right)\right]\cdot V4=Ir \qquad \text{Equation 11.29}$$

where:

$Ir=Yrr\cdot Er$

$Yrr=Zrr^{-1}$

Equation 11.26 through Equation 11.29 now represent 12 simultaneous equations. These four equations can be arranged to make single linear equation Equation 11.30 required for the simultaneous solution of all 12 unknown node voltages. Each of the elements in the admittance matrix, which are themselves three by three matrices, corresponds to the coefficients of the respective node voltages in Equation 11.26 through Equation 11.29. Some elements are null three by three matrices signifying that there are no connections between those three-phase nodes as is the case for Y_{13},

Y_{14}, and Y_{24}. By their very nature, many of the off-diagonal terms of the admittance matrix representing power systems are zero showing that most nodes are connected to relatively few other nodes. In these cases, sparse matrix inversion techniques can be employed to invert the admittance matrix for greater computational efficiency.

$$\begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{12} & Y_{22} & Y_{23} & Y_{24} \\ Y_{13} & Y_{23} & Y_{33} & Y_{34} \\ Y_{14} & Y_{24} & Y_{34} & Y_{44} \end{bmatrix} \cdot \begin{bmatrix} V1 \\ V2 \\ V3 \\ V4 \end{bmatrix} = \begin{bmatrix} Is \\ 0 \\ 0 \\ Ir \end{bmatrix} \qquad \text{Equation 11.30}$$

11.7.6 Solution of Node voltages

Multiplying both sides of Equation 11.30 by the inverse of the admittance matrix results in Figure 11.17. The final results are the 12 node voltages expressed by the node voltage vector shown in Figure 11.16.

11.7.7 Extracting branch currents

The line current of interest for this relay study is the current between node *V2* and *V1*, *V2* and *V3*, and *V4* and *V3*. Understanding the development of Equation 11.27 through Equation 11.29 show that they provide the basis for determining these currents. The three sets of three-phase current are calculated by Equation 11.31 through Equation 11.33.

$$I_{21} = \left(YL/_{mr}\right) \cdot (V2 - V1) \qquad \text{Equation 11.31}$$

$$I_{23} = \left(YL/_{mf}\right) \cdot (V2 - V3) \qquad \text{Equation 11.32}$$

$$I_{43} = \left(YL/_{(1-mf)}\right) \cdot (V4 - V3) \qquad \text{Equation 11.33}$$

11.8 APPENDIX VIII. DERIVATION OF PHASE FAULT DETECTION USING THE NEGATIVE SEQUENCE IMPEDANCE PLANE

Relating the symmetrical component current to the phase currents.

$$\begin{aligned} Ia &= I_1 + I_2 + I_0 \\ Ib &= a^2 \cdot I_1 + a \cdot I_2 + I_0 \\ Ic &= a \cdot I_1 + a^2 \cdot I_2 + I_0 \end{aligned} \qquad \text{Equation 11.34}$$

Assume I_0 is zero for phase-to-phase faults. Compute the phase-to-phase currents as the difference between any two of the three phase currents in Equation 11.34 through Equation 11.37.

$$\begin{aligned} Iab &= Ia - Ib = (I_1 + I_2 + I_0) - (a^2 \cdot I_1 + a \cdot I_2 + I_0), \\ Iab &= (1 - a^2) \cdot I_1 + (1 - a) \cdot I_2 \\ Iab &= \sqrt{3} \angle 30° \cdot 1 \angle -60° \cdot I_1 \angle 60° \; + \; \sqrt{3} \angle -30° I_2 \\ Iab &= 2 \cdot \sqrt{3} \angle -30° I_2 \end{aligned} \qquad \text{Equation 11.35}$$

where:

$I_2 = I_1 \cdot 1 \angle 60°$ for AB faults

$Iab = 2 \cdot \sqrt{3} \angle 330° I_2 = 2j \cdot \sqrt{3} \cdot a^2 I_2$

$$\begin{aligned} Ibc &= Ib - Ic = (a^2 \cdot I_1 + a \cdot I_2 + I_0) - (a \cdot I_1 + a^2 \cdot I_2 + I_0) \\ Ibc &= (a^2 - a) \cdot I_1 + (a - a^2) \cdot I_2 \end{aligned} \qquad \text{Equation 11.36}$$

where:

$I_1 = -I_2$ for BC faults

$Ibc = (a^2 - a) \cdot (I_1 - I_2) = 2j\sqrt{3} \cdot I_2$

where:

$(a^2 - a) = j\sqrt{3}$

$$\begin{aligned} Ica &= Ic - Ia = (a \cdot I_1 + a^2 \cdot I_2 + I_0) - (I_1 + I_2 + I_0) \\ Ica &= (a - 1) \cdot I_1 + (a^2 - 1) \cdot I_2 \\ Ica &= \sqrt{3} \angle 150° \cdot 1 \angle 60° \cdot I_1 \angle -60° \; + \; \sqrt{3} \angle 210° I_2 \\ Ica &= 2 \cdot \sqrt{3} \angle -30° I_2 \end{aligned} \qquad \text{Equation 11.37}$$

where:

$I_2 = I_1 \cdot 1\angle -60°$ for CA faults

$Ica = 2 \cdot \sqrt{3}\angle 210° I_2 = 2j \cdot \sqrt{3} \cdot a\, I_2$

Substitute the following identities into Equation 11.35 through Equation 11.37.

11.9 APPENDIX IX. IEEE C37.2 DEVICE NUMBERS AND DEFINITIONS

1 Master switch normally used for manually operated devices

2 Time delay starting or closing relay. Does not include 48, 62 and 79 devices

3 Checking or interlocking relay

4 Master contactor

5 Stopping device

6 Starting circuit breaker

7 Rate of rise relay

8 Control power-disconnection device

9 Reversing device

10 Unit sequence switch

11 Multifunction device

12 Overspeed device

13 Synchronous-speed device

14 Underspeed device

15 Speed- or frequency-matching device

17 Shunting or discharge switch

18 Accelerating or decelerating device

19 Starting-to-running transition detector

20 Electrically operated valve

21 Distance relay

22 Equalizer circuit breaker

23 Temperature control device

24 Volts per hertz relay

25 Synchronizing or synchronism-check device

26 Apparatus thermal device

27 Undervoltage device

28 Flame detector

29 Isolating contactor

30 Annunciator relay

31 Separate excitation device

32 Directional power relay

33 Position switch

34 Master sequence device

36 Polarity or polarizing voltage device

37 Undercurrent or underpower relay

38 Bearing protective device

39 Mechanical conduction device

40 Field relay

41 Field circuit breaker

42 Running circuit breaker

43 Manual transfer or selector device

44 Unit/sequence starting relay

45 Atmospheric condition monitor

46 Reverse-phase or phase-balance relay

47 Phase-sequence voltage relay

48 Incomplete-sequence relay

49 Machine or transformer thermal relay

50 Instantaneous overcurrent relay

51 Ac time overcurrent relay

52 AC circuit breaker

52a and 52aa: Follows breaker contacts. Open when 52 contacts are open

52b and 52bb: Opposite of 52a contacts. Closed when 52 contacts are closed

53 Exciter or dc generator relay

55 Power factor relay

56 Field application relay

57 Short-circuiting or grounding relay

58 Rectification failure relay

59 Overvoltage relay

60 Voltage or current balance relay

62 Time-delay stopping or opening relay

63 Pressure switch

64 Ground detector relay

65 Governor

66 Notching or jogging device

67 Ac directional overcurrent relay

68 Blocking relay

69 Permissive control device

70 Rheostat

71 Level switch

72 Dc circuit breaker

73 Load-resistor contactor

74 Alarm relay

76 Dc overcurrent relay

77 Telemetering device

78 Phase-angle measuring or out-of-step protection relay

79 Ac-reclosing relay

80 Flow switch

81 Frequency relay

82 Dc-reclosing relay

83 Automatic selective control or transfer relay

84 Operating mechanism

85 Carrier or pilot wire-receiver relay

87 Differential protective relay

88 Auxiliary motor or motor-generator

89 Line switch

90 Regulating device

91 Voltage directional relay

92 Voltage and power directional relay

93 Field-changing contactor

94 Tripping or trip-free relay

11.10 APPENDIX X. TUTORIAL ON SYMMETRICAL COMPONENTS

by Dave Angell, Idaho Power Company

11.10.1 Introduction

Relay manufacturers make use of symmetrical components to detect power system unbalanced fault conditions. Their literature, both manuals and application notes, will include symmetrical component network diagrams of the power system. This advanced course in symmetrical components is intended to build on the basic course. In this course we will focus on the symmetrical component networks.

11.10.2 Common Symmetrical Component Equations

The symmetrical component equations were introduced in the Basic Symmetrical Components Course. These equations will be used to gain further insight into the operation of the power system and relays that are designed to operate on symmetrical component principles.

The following equations were defined or developed:

Per-Phase Symmetrical Component Equations:

$$V_A = V_{A0} + V_{B1} + V_{A2} \quad (11.11.38)$$

$$V_B = V_{B0} + V_{B1} + V_{B2} \quad (11.11.39)$$

$$V_C = V_{C0} + V_{C1} + V_{C2} \quad (11.11.40)$$

Synthesis Equations:

$$V_A = V_{A0} + V_{B1} + V_{A2} \quad (11.11.41)$$

$$V_B = V_{A0} + a^2 \cdot V_{A1} + a \cdot V_{A2} \quad (11.11.42)$$

$$V_C = V_{A0} + a \cdot V_{A1} + a^2 \cdot V_{C2} \quad (11.11.43)$$

Analysis Equations:

$$V_{A0} = \left(V_A + V_B + V_C\right)/3 \quad (11.11.44)$$

$$V_{A1} = \left(V_A + a \cdot V_B + a^2 \cdot V_C\right)/3 \quad (11.11.45)$$

$$V_{A2} = \left(V_A + a^2 \cdot V_B + a \cdot V_C\right)/3 \quad (11.11.46)$$

11.10.3 The Sequence Networks

For the three-phase power system to be analyzed with symmetrical components, the power system network must be represented by symmetrical component elements. These elements are referred to as sequence elements. Each network only contains voltage and impedance elements of that particular sequence.

The zero-sequence network contains only impedance connections between the reference bus, shown at the top, and the fault bus, shown at the bottom. The positive-sequence network consists of the driving system voltage and positive sequence system impedance. This source represents the system generators producing their nominal balanced three-phase voltage. The negative sequence network simply includes impedances between the reference bus and the fault bus. Although the three networks are illustrated in Figure 11.1 show the sequence impedance as purely reactive, the impedance can be any combination of resistance, inductance and capacitive reactance. An explanation of the positive, negative and zero sequence impedances is discussed below.

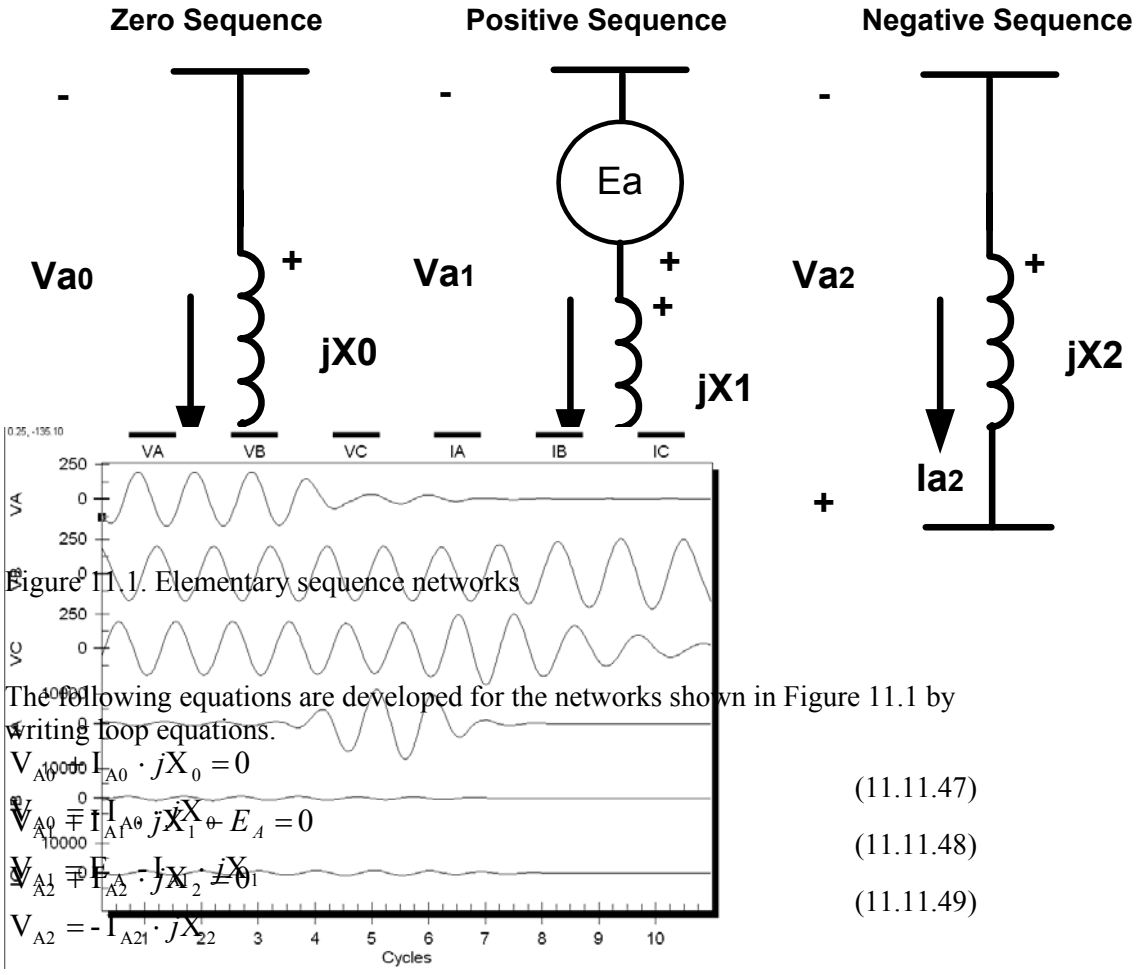


Figure 11.1. Elementary sequence networks

The following equations are developed for the networks shown in Figure 11.1 by writing loop equations.

$$V_{A0} + I_{A0} \cdot jX_0 = 0 \tag{11.11.47}$$

$$V_{A1} + I_{A1} \cdot jX_1 - E_A = 0 \tag{11.11.48}$$

$$V_{A2} + I_{A2} \cdot jX_2 = 0 \tag{11.11.49}$$

$$V_{A2} = -I_{A2} \cdot jX_2$$

11.10.4 Connection of sequence networks for unsymmetrical faults

We will use the example A-phase to ground fault to develop the sequence network connections.

11.10.4.1 Single line - to - ground (SLG) fault

To simplify analysis, we will assume these traces are representative of the voltages and currents at the fault point with a bolted fault, such that $Z_f = 0$.

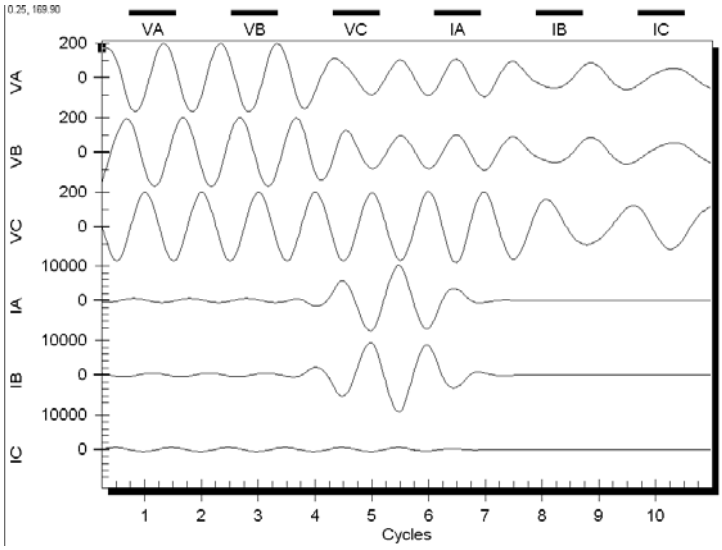
The conditions at the point of fault are:

$V_a = 0, \qquad I_b = 0, I_c = 0$

+ Ia0

From the phase fault voltage, Va =0, and the synthesis equation for phase A, we find the sequence voltages to be:

$V_a = V_{a0} + V_{a1} + V_{a2} = 0$



ve find the

We will use the example A to B phase fault from the Basic Course to develop the sequence network connections.

The voltages and currents are:

$V_a = V_b, \qquad I_c = 0, I_a = -I_b$

Again to simplify analysis, we will assume the voltage and currents at the point of fault are similar to found at the substation and that it is a bolted fault, $Z_f = 0$. Additionally, we will convert the fault to a phase B to C, so that a-phase symmetrical components may be used,

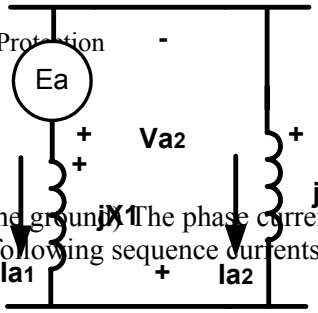
$V_b = V_c, \qquad I_a = 0, I_b = -I_c$

From the phase fault voltage, Vb = Vc, and the analysis equations, we find the sequence voltages to be:

$V_{a0} = \frac{1}{3} (V_a + V_b + V_b)$

$$V_{a1} = \frac{1}{3}(V_a + a\,V_b + a^2\,V_b) = \frac{1}{3}(V_a - V_b)$$

$$V_{a2} = \frac{1}{3}(V_a + a^2\,V_b + a\,V_b) = \frac{1}{3}(V_a - V_b)$$



Thus, $V_{a1} = V_{a2}$, and $V_{a0} = 0$ (no connection to the ground). The phase currents Ia = 0, Ib = -Ic and the analysis equations produce the following sequence currents:

$$I_{a0} = \frac{1}{3}(0 + I_b - I_b)$$

$$I_{a1} = \frac{1}{3}(0 + a\,I_b - a^2\,I_b) = \frac{1}{3}(I_b \angle 90°)$$

$$I_{a2} = \frac{1}{3}(0 + a^2\,I_b - a\,I_b) = \frac{1}{3}(I_b \angle -90°)$$

Thus, $I_{a1} = -I_{a2}$

Connecting the positive and negative networks to satisfy $V_{a1} = V_{a2}$ and $I_{a1} = -I_{a2}$ results in a parallel connection of the positive and negative sequence network:

The per unit system is used in power system analysis to simplify the calculation of voltage, current, impedance and power flow in the system. The advantage mostly comes from avoidance of the multiplication and division by the transformer turns ratio (n) when calculating voltage and current magnitudes across transformers. Other benefits include:

The per unit system gives one a "feel" for the relative magnitude of voltage and current. The per unit voltage applies to both phase-to-phase and phase-to-ground. For example: 1.2 per unit voltage is too much but 276 kV depends on the voltage level and whether the value is phase-to-phase or phase-to-ground.

Transformers and machines have typical ranges of per unit impedances, which are 5 to 10% for transformers and 30% for generators. These per unit values are referenced to the transformer or generator base VA.

The per unit equivalent impedance of a transformer is constant but the ohmic impedance values change by n^2 from primary to secondary.

11.10.4.3 Development of the Per Unit Equations

The per unit voltage is fixed at the nominal operating voltage, 13.8KV, 138,KV 230KV, 345KV, etc. A fixed voltage and current produce a certain power flow (S = VI). Therefore, we set the apparent power base, typically 100 MVA. Once the voltage and power base are set, the current and impedance bases may be calculated. The base calculations are:

Single phase: S = VI: $I_{base1\phi} = \frac{S}{V} = \frac{VA}{V} = \frac{MVA \times 1000}{kV}$

Three phase: $S = \sqrt{3}VI$ $I_{base3\phi} = \frac{S}{\sqrt{3}V} = \frac{VA}{\sqrt{3}kV} = \frac{MVA \times 1000}{\sqrt{3}kV}$

$S = \frac{V^2}{Z}$ $Z_{base} = \frac{V^2}{S} = \frac{V^2}{VA} = \frac{kV^2}{MVA}$, for both single and three phase

To convert from amps to pu: $I_{PU} = \frac{I(A)}{I_{base}}$, and back to amps: $I(A) = I_{PU} I_{base}$

To convert from ohms to pu: $Z_{PU} = \frac{Z(\Omega)}{Z_{base}}$, and back to ohms: $Z(\Omega) = Z_{PU} Z_{base}$

The impedance of transformers and machines is given in percentage on the device's VA rating. These impedances must be converted to the system base using the following equation:

$$Z_{SYSTEM} = \frac{(Z_{PU_{DEVICE}})(Z_{base_{DEVICE}})}{Z_{base_{SYSTEM}}} = \frac{Z_{PU_{DEVICE}} \left(\frac{kV^2_{DEVICE}}{MVA_{DEVICE}} \right)}{\left(\frac{kV^2_{SYSTEM}}{MVA_{SYSTEM}} \right)}$$

$$= Z_{PU_{DEVICE}} \left(\frac{kV_{DEVICE}}{kV_{SYSTEM}} \right)^2 \left(\frac{MVA_{SYSTEM}}{MVA_{DEVICE}} \right)$$

11.10.4.3.1 Example of Per Unit Calculations

Given the an example generator, step-up transformer and transmission line:

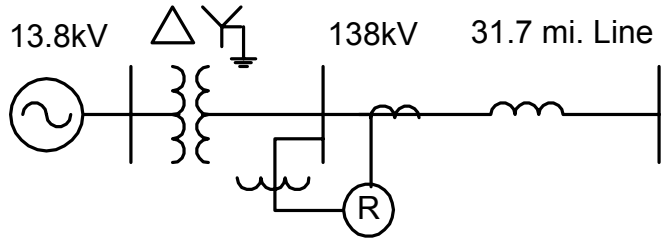


Figure 11.2. Example power system

Generator	Transformer	Line
$X_{d'} = 0.35$ @ 50 MVA	$X_t = 10\%$ @ 50 MVA	$Z_1 = 0.6$ ohms per mile
$X_0 = 0.2$ @ 50 MVA		$Z_0 = 1.8$ ohms per mile

11.10.4.3.2 Generator impedance

Convert the generator and transformer to per unit on 100 MVA base:

$$X_1 = X_{d'} \times \left(\frac{MVA_{base}}{MVA_{gen}} \right) \qquad X_1 = 0.35 \times \left(\frac{100}{50} \right) = 0.7 \text{ PU @ 100 MVA}$$

$$X_0 = X_0 \times \left(\frac{MVA_{base}}{MVA_{gen}} \right)$$

11.10.4.3.3 Transformer impedance

10% is equal to 0.1 per unit

$$X_1 = X_t \times \left(\frac{MVA_{base}}{MVA_{xfmr}} \right) \qquad X_1 = 0.10 \times \left(\frac{100}{50} \right) = 0.2 \text{ PU @ 100 MVA}$$

11.10.4.3.4 Line impedance

Multiply the line ohms per mile by the line length.

$$Z_{line} = 31.7 \times 0.6 = 19.0 \text{ ohms} \qquad Z_{base} = \frac{kV^2}{MVA} = \frac{138^2}{100} = 190.4 \text{ ohms}$$

$$Z_{line} = \frac{19.0}{190} = 0.1 \text{ per unit}$$

Now, we can also calculate the base current at 138 and 13.8 kV

$$I_{base138} = \frac{MVA}{\sqrt{3}kV} \times 1000 = \frac{100000}{\sqrt{3}(138)} = 418.4A \qquad I_{base13.8} = 4184A$$

11.10.4.4 Example Two source two-line systems

Below is the example system with two sources to gain some insight to the effect of multiple sources. This has an additional benefit in relating the zero and negative sequence quantities at a bus to determine fault direction. In order to simplify the math, let us make the second source impedance match the original. Then the current should divide equally between the sequence network branches.

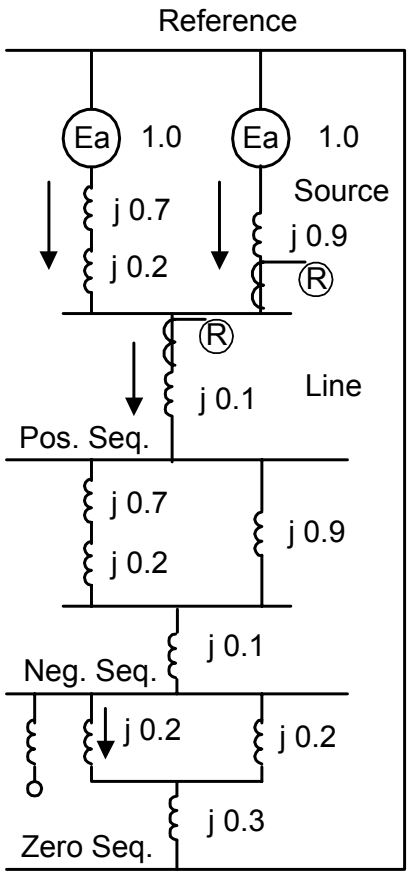


Figure 11.3. Sequence diagram for system in Figure 11.4

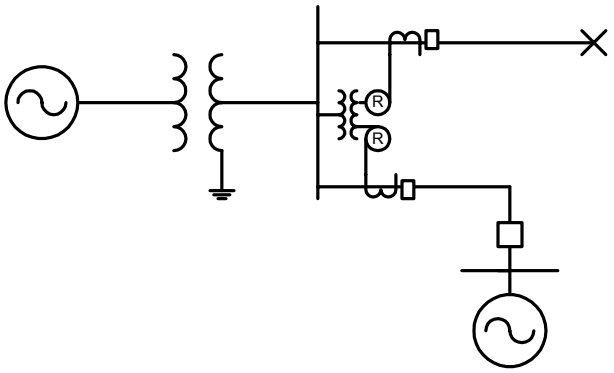


Figure 11.4. Faulted two-source, two-line system

Calculation of fault current:

$Ia_0 = Ia_1 = 1a_2$

$$Ia_0 = \frac{1}{Z_1 + Z_2 + Z_0}$$

$$Ia_0 = \frac{1}{j0.55 + j0.55 + j0.4}$$

$$Ia_0 = \frac{1}{j1.5}$$

$$Ia_0 = -j0.67$$

$$I_a = Ia_0 + Ia_1 + Ia_2 = 3I_0 = -j2.0$$

This is the current at the fault point and the faulted line. The current in the in the non-faulted line is half this value because the sources are equal. Now to calculate the voltage at the 138 kV bus for comparison with the original system.

$$V_a = 0.33$$

$$V_b = -0.067 + 0.70a^2 - 0.30a$$

$$V_b = 0.91\angle -107^o$$

$$V_c = -0.067 + 0.70a - 0.30a^2$$

$$V_c = 0.91\angle 107^o$$

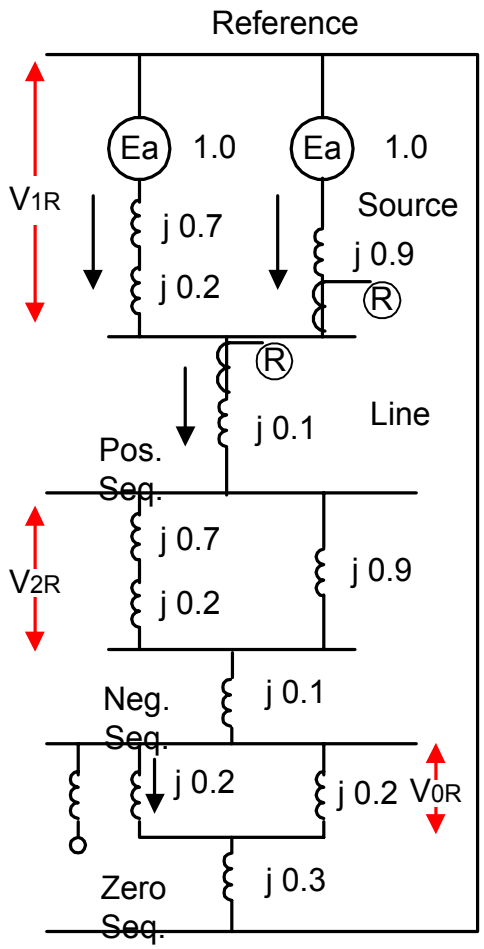


Figure 11.5, Sequence diagram for faulted system

Notice the magnitude and polarity of the zero and negative sequence voltages in Figure 11.5.

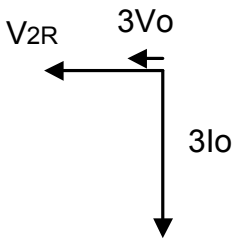


Figure 11.6. Faulted line relay quantities

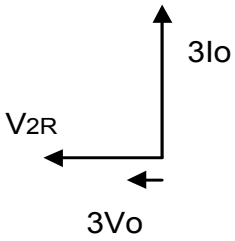


Figure 11.7, Unfaulted line relay quantities

Below is the example line with two sources to gain some insight to the effect of multiple sources. This has an additional benefit in relating the zero and negative sequence quantities at line ends.

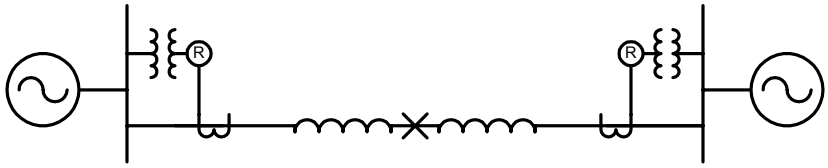


Figure 11.8.A single-line to ground fault has the following network connections

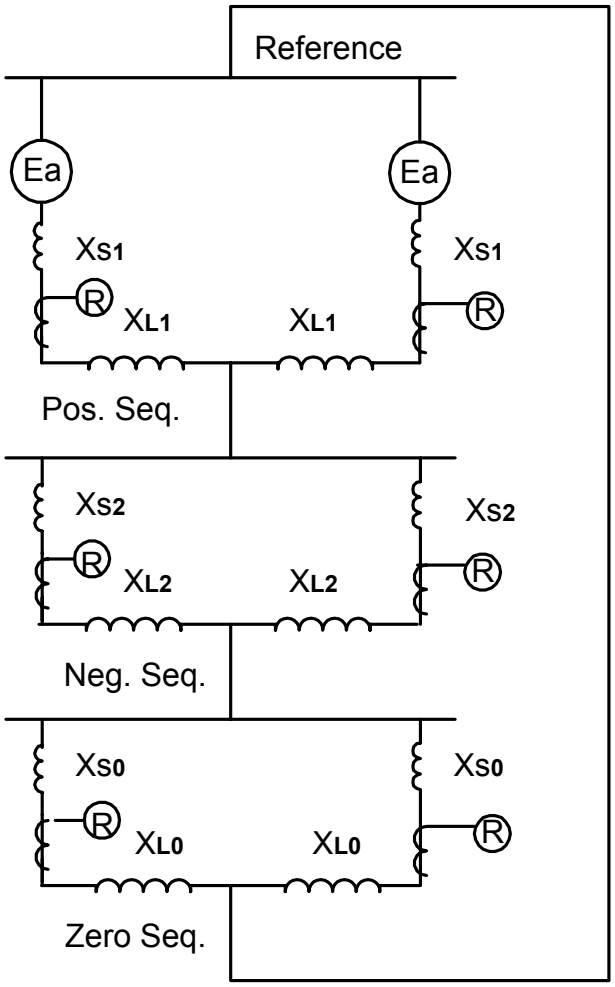


Figure 11.9. Sequence network showing relay instrumentation points for the faulted system shown in Figure 11.4

Notes:

11.10.4.4.1 Phase to phase faulted networks connections:

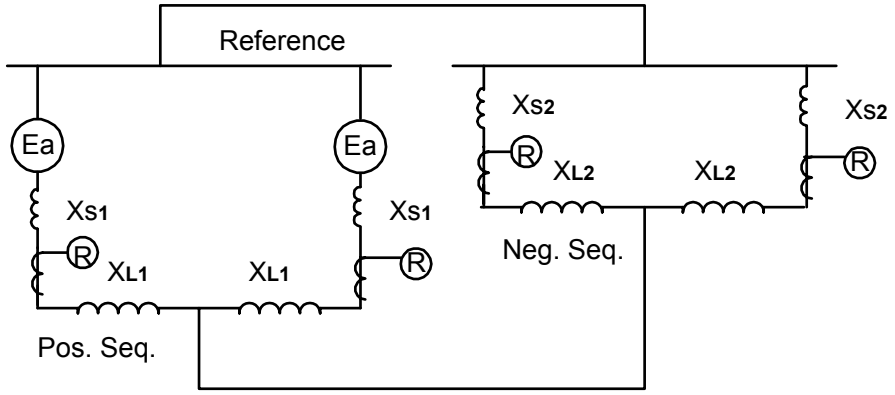


Figure 11.10. Phase to phase fault has positive and negative sequence networks connections

11.10.5 Element modeling

11.10.5.1 Transformers

Not all the flux produced in an electro-magnetic device stays in the iron core. A portion escapes and is known as leakage flux. This leakage flux produces a voltage drop by Faraday's Law: $e = -N\frac{d\varnothing}{dt}$, and can be related to an inductance by $L = \frac{N\varnothing}{i}$, $\varnothing = \frac{Li}{N}$ such that $e = -L\frac{di}{dt}$. From this we can produce a circuit model as shown:

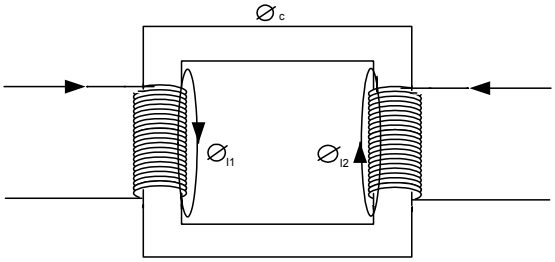
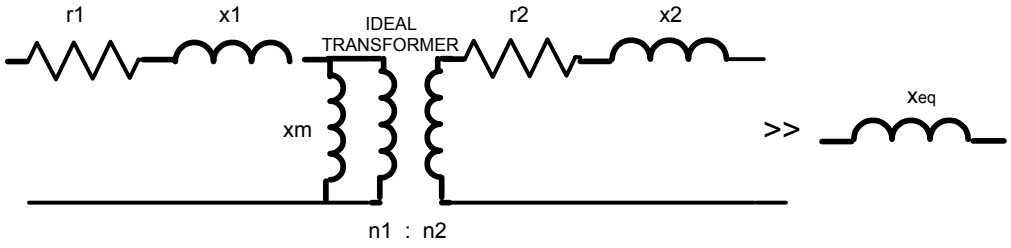


Figure 11. 11 Two winding transformer

$$\frac{E_1}{E_2} = \frac{n_1}{n_2} = n$$

$$E_1 = nE_2$$

$$I_1 = \frac{1}{n} I_2$$



The resistance will be ignored again to simplify calculations $r \approx 0.1\,X$. The reactance x_2 may be referred to the primary by the square of the turns ratio, $x_{eq} = x_1 + a^2 x_2$. The manufacturer on the transformer nameplate provides this equivalent reactance. A typical value is 7% on the transformer base impedance. This value is the phase, positive and negative sequence impedance because all three produce a balanced core flux and result in a net external flux of zero.

The zero sequence reactance is dependent upon transformer construction. Three single-phase and shell-form *3Ø* transformers have *Xo = X1*. Core-form *3Ø* transformers have an *Xo < X1* because the entire zero sequence flux is forced out of the transformer core. Now the excitation branch, previously neglected (high

impedance path for phase and positive sequence current), becomes significant because zero sequence magnetizing flux is forced out of the core. This leakage flux travels trough the oil and transformer tank. Oil and tank steel have a high reluctance and low inductance producing the low exciting branch inductance.

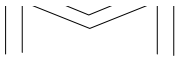


Figure 11.12. Diagram of a synchronous machine

11.10.5.2 Synchronous Generators

A synchronous machine has three positive sequence reactances, one negative reactance and one zero sequence reactance. These sequence reactances are produced by leakage inductance and armature reaction. The leakage reactance is similar to transformer leakage reactance and occurs due to leakage flux in the slot, end runs, and non-linking flux across the air gap (smaller portion).

The armature reaction results from current flow in the stator winding (larger portion)

Figure 11. 13. Diagram of a synchronous reactor

11.10.5.2.1 Sequence Reactances

11.10.5.2.1.1 Positive

Direct axis x_d:	Figure (a, b) If the rotor axis (d - axis) is in line with stator MMF peak, then the flux wave has a high permeance path, resulting in maximum flux. Small air gap results in highest inductance. $x_d = x_{ar} + x_l$. When a fault occurs, the load on the system changes from high impedance to low impedance (internal reactance) and results in large current flow. A synchronous machine responds to this change with a time varying reactance, the x_d' and x_d''.
Transient x_d' axis:	Figure (c, d) Assume an initially unloaded synchronous machine. An abrupt change in armature current causes a sudden appearance of a MMF opposite the field pole establishing a flux through it. This flux links the field winding

	which produces field current and opposes the flux change. The flux is forced out of the pole (path of high permeance) and into the air gap between poles. This results in a low reactance $x_d' < x_d$.
Sub-transient x_d'':	Figure (e, f) Synchronous machines typically have damper, amortisseur windings These windings force the flux out of the rotor and into the air gap. They limit the flux path through the rotor and thus increase the reluctance, resulting in a small reactance where $x_d'' < x_d' < x_d$.

Time-constants of the positive sequence reactances: The sub-transient reactance developed by the amortisseur windings are copper bars with relatively high resistance, resulting in a short time constant of about three cycles. The transient reactance is a result of the low resistance field windings that produce about a one second time constant.

11.10.5.2.1.2 Negative

Negative sequence currents create a MMF that rotates backwards at twice the machines synchronous speed as seen from the rotor. This induces currents of twice the synchronous frequency in the rotor circuits (field and amortisseur windings). The flux is then forced into paths of high reluctance because of its rotation. Its peak occurs along the q - axis as well as the d - axis.

$x_2 = \frac{x_d'' + x_q''}{2}$, x'' is usually slightly greater than x_d'' (11.11.50)

11.10.5.2.1.3 Zero

Zero sequence current flowing in the stator winding produces zero sequence flux in each phase. Each phase flux is equal in magnitude and phase. Each phase is mechanically separated by 120 electrical degrees, balanced. Thus, no flux flows across the air gap. The result is $x_0 = x_1$ only. Thus $x_0 < x_d''$.

11.10.5.3 Transmission Lines

The resistance of power lines is significant due to the power loss associated with power transfer (I^2R). The inductance of the transmission line is significant because it limits the power transfer across a line. The transmission line resistance is small compared to the inductance for typical construction and can be ignored. The inductance of the transmission line is dependent upon the magnetic flux linking it. A sinusoidal current causes the magnetic flux to be constantly changing. This change of flux creates a voltage $e = -N\frac{d\varnothing}{dt}$. This voltage is presented in a polarity

opposing the change. Inductance is the quantity that relates this voltage to the changing current, $e = -L\frac{di}{dt}$.

In terms of phasor quantities:

$V = j\omega LI$, self inductance of circuit

If two circuits exist then:

$V_1 = j\omega M_{12} I_2$, represents the voltage induced into circuit 1 from I_2 flowing in circuit 2.

The inductance of a three-phase line is the sum of internal and external inductances. The external inductance is a function of both self and mutual terms.

$$L_{\text{int}} = \frac{1}{2} \times 10^{-7} \frac{H}{m}$$

$$L = 2 \times 10^{-7} In \frac{D}{r_1}$$

As the conductor separation, D, increases, L increases (D fixed by voltage / air dielectric strength)

As the conductor radius, r_1, increases, L decreases (the advantage of bundled conductors)

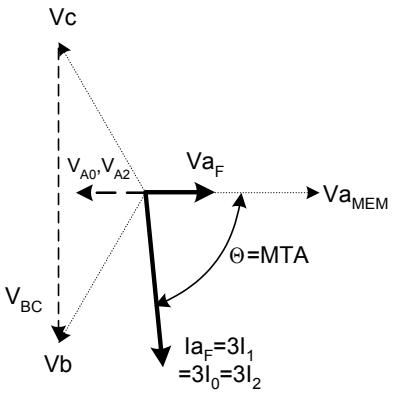
The inductance of each phase is identical, thus the positive and negative sequence reactances (x_1) are equal to the phase reactance. Typical value of x_1 is 0.6 Ω/mi. Typical construction does not result in equilateral spacing so transpositions are required to balance phase reactances.

Zero sequence current flows in all three phases and returns in the ground.

$$L = 2 \times 10^{-7} In \frac{D}{r}$$

Because the current flows in the phase and returns in the ground, the xo is at least two times x_1 and ranges from 2.5 to 6 times x_1, typical value is 3 times x_1.

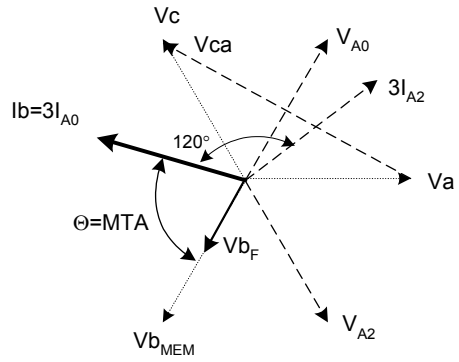
11.11 APPENDIX XI. DIRECTIONAL POLARIZING QUANTITIES FOR FAULTED NETWORKS



Phase A to Ground Fault	
Polarization	**Torque Equation**
Memory	$T32=\lvert Ia\rVert Va_{MEM}\rvert\cos(\angle Va_{MEM}-(\angle Ia+\theta))$
Cross	$T32=\lvert Ia\rVert Vab\rvert\cos(\angle jVab-(\angle Ia+\theta))$
Negative Sequence	$T32=\lvert Ia\rVert 3V_{A2}\rvert\cos(\angle -3V_{A2}-(\angle Ia+\theta))$
Zero Sequence	$T32=\lvert Ia\rVert 3V_{A0}\rvert\cos(\angle -3V_{A0}-(\angle Ia+\theta))$
Polarizing Current – I	$T32=\lvert 3I_{A0}\rVert Ipol\rvert\cos(\angle Ipol-\angle 3I_{A0})$

Θ = MTA = Positive Sequence Impedance Line Angle

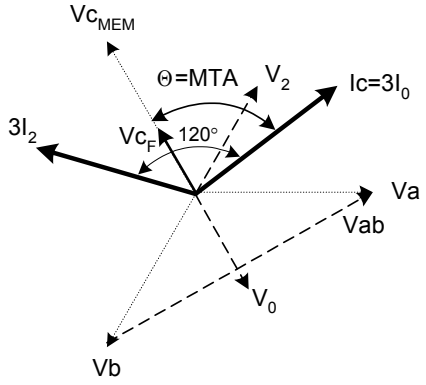
Figure 11.23: Polarizing Quantities for Phase-A-to-Ground Faults



Phase B to Ground Fault	
Polarization	**Torque Equation**
Memory	$T32 = \lvert Ib \rVert Vb_{MEM} \rvert \cos(\angle Vb_{MEM} - (\angle Ib + \theta))$
Cross	$T32 = \lvert Ib \rVert Vca \rvert \cos(\angle jVca - (\angle Ib + \theta))$
Negative Sequence – V	$T32 = \lvert Ib \rVert 3V_{A2} \rvert \cos(\angle a(-3V_{A2}) - (\angle Ib + \theta))$
Zero Sequence – V	$T32 = \lvert Ib \rVert 3V_{A0} \rvert \cos(\angle -3V_{A0} - (\angle Ib + \theta))$
Polarizing Current – I	$T32 = \lvert 3I_{A0} \rVert Ipol \rvert \cos(\angle Ipol - \angle I_{A0})$

Θ = MTA = Positive Sequence Impedance Line Angle

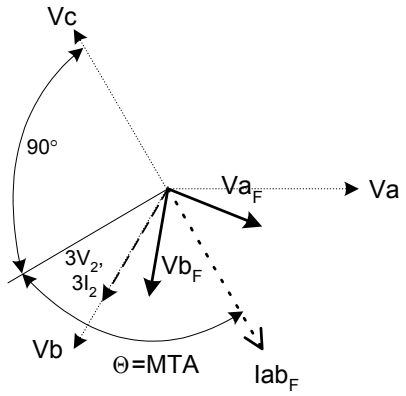
Figure 11.24: Polarizing Quantities for Phase-B-to-Ground Faults



Phase C to Ground Fault	
Polarization	**Torque Equation**
Memory	$T32 = \lvert Ic \rVert Vc_{MEM} \rvert \cos(\angle Vc_{MEM} - (\angle Ic + \theta))$
Cross	$T32 = \lvert Ic \rVert Vab \rvert \cos(\angle jVca - (\angle Ic + \theta))$
Negative Sequence – V	$T32 = \lvert Ic \rVert 3V_{A2} \rvert \cos(\angle a^2(-3V_{A2}) - (\angle Ic + \theta))$
Zero Sequence – V	$T32 = \lvert Ic \rVert 3V_{A0} \rvert \cos(\angle -3V_{A0} - (\angle Ic + \theta))$
Polarizing Current – I	$T32 = \lvert 3I_{A0} \rVert Ipol \rvert \cos(\angle Ipol - \angle 3I_{A0})$

Θ = MTA = Positive Sequence Impedance Line Angle

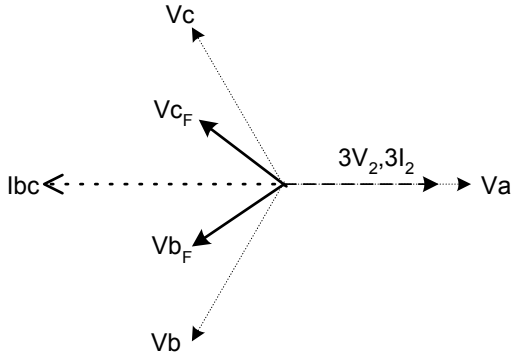
Figure 11.25: Polarizing Quantities for Phase-C-to-Ground Faults



Phase AB and AB to Ground Fault	
Polarization	**Torque Equation**
Memory	$T32 = \lvert Iab \rVert jVc_{MEM} \rvert \cos(\angle jVc_{MEM} - (\angle Iab - \theta))$
Cross	$T32 = \lvert Iab \rVert Vc \rvert \cos(\angle jVc - (\angle Iab - \theta))$
Negative Sequence – V	$T32 = \lvert Iab \rVert 3V_{A2} \rvert \cos(-3a^2 V_{A2} - \angle Ibc)$
Zero Sequence – V	*None*
Polarizing Current – I	*None*

Θ = MTA = Positive Sequence Impedance Line Angle

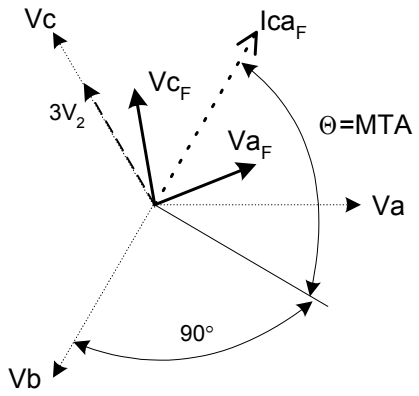
Figure 11.26: Polarizing Quantities for Phase-AB and AB-to-Ground Faults



Phase BC and BC to Ground Fault	
Polarization	**Torque Equation**
Memory	$T32 = \lvert Ibc \rVert jVa_{MEM} \rvert \cos(\angle jVa_{MEM} - (\angle Ibc + \theta))$
Cross	$T32 = \lvert Ibc \rVert Va \rvert \cos(\angle jV_{A1} - (\angle Ibc - \theta))$
Negative Sequence – V	$T32 = \lvert Ibc \rVert 3V_{A2} \rvert \cos(-3V_{A2} - \angle Ibc)$
Zero Sequence – V	*None*
Polarizing Current – I	*None*

Θ = MTA = Positive Sequence Impedance Line Angle

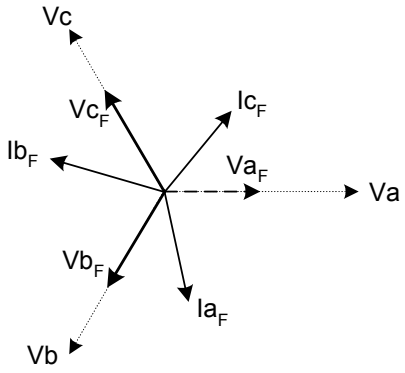
Figure 11.27: Polarizing Quantities for Phase-BC and BC-to-Ground Faults



Phase CA and CA to Ground Fault	
Polarization	**Torque Equation**
Memory	$T32 = \lvert Ica \rVert jVb_{MEM} \rvert \cos(\angle jVb_{MEM} - (\angle Ica + \theta))$
Cross	$T32 = \lvert Ica \rVert Vb \rvert \cos(\angle jV_{B1} - (\angle Ica - \theta))$
Negative Sequence – V	$T32 = \lvert Ica \rVert 3V_{A2} \rvert \cos(-3aV_{A2} - \angle Ica)$
Zero Sequence – V	*None*
Polarizing Current – I	*None*

Θ = MTA = Positive Sequence Impedance Line Angle

Figure 11.28: Polarizing Quantities for Phase-BC and BC-to-Ground Faults



Phase ABC and ABC to Ground Fault	
Polarization	**Torque Equation**
Memory – any of one of three equations	$T32 = \lvert Iab \rVert jVc_{MEM} \rvert \cos(\angle jVc_{MEM} - (\angle Iab + \theta))$
	$T32 = \lvert Ibc \rVert jVa_{MEM} \rvert \cos(\angle jVa_{MEM} - (\angle Ibc + \theta))$
	$T32 = \lvert Ica \rVert jVb_{MEM} \rvert \cos(\angle jVb_{MEM} - (\angle Ica + \theta))$
Cross	*None*
Negative Sequence – V	*None*
Zero Sequence – V	*None*
Polarizing Current – I	*None*

Θ = MTA = Positive Sequence Impedance Line Angle

Figure 11.29: Polarizing Quantities for Phase-ABC and ABC-to-Ground Faults

11.12 APPENDIX XII. TRANSFORMER CONNECTION SYMMETRICAL COMPONENT NETWORKS

11.12.1 Transformer Configuration Impedance Network Diagrams

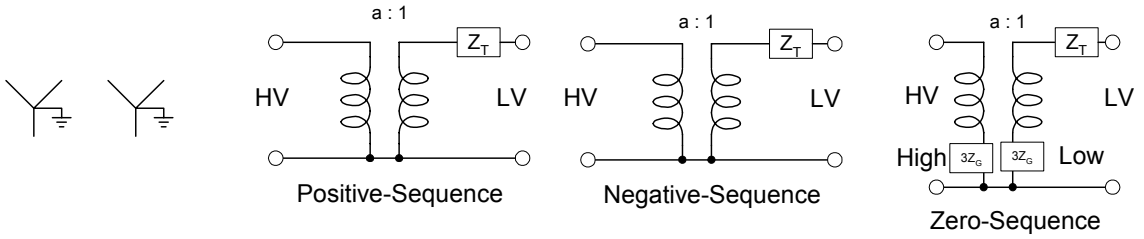


Figure 11.30: Wye-Grounded.–Wye-Grounded Transformer Sequence Impedance Networks

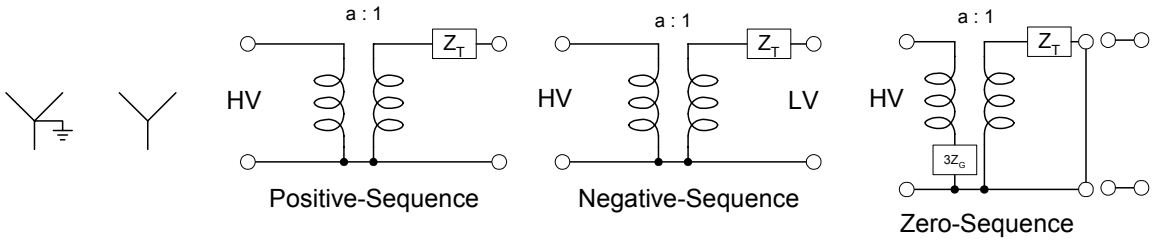


Figure 11.31: Wye Grounded–Wye Transformer Sequence Impedance Networks

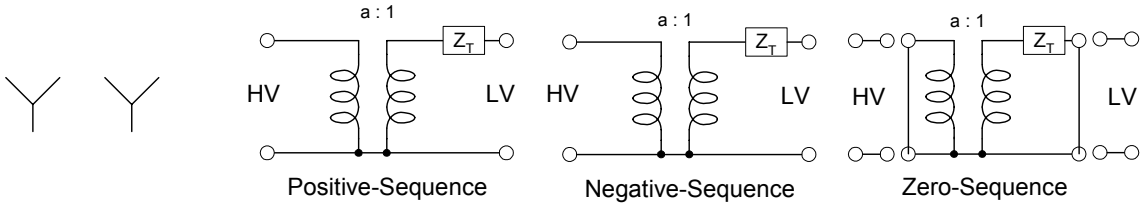


Figure 11.32: Wye–Wye Transformer Sequence Impedance Networks

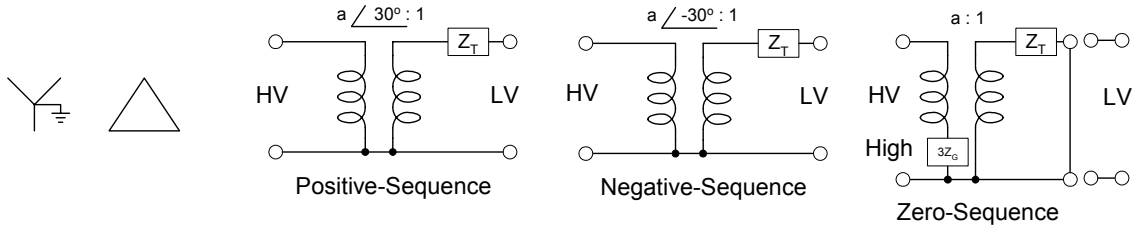


Figure 11.33: Wye-Grounded–Delta Transformer Sequence Impedance Networks

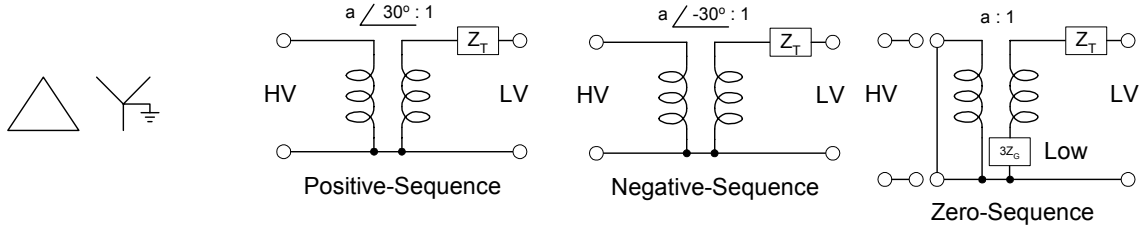


Figure 11.34: Delta–Wye-Grounded Transformer Sequence Impedance Networks

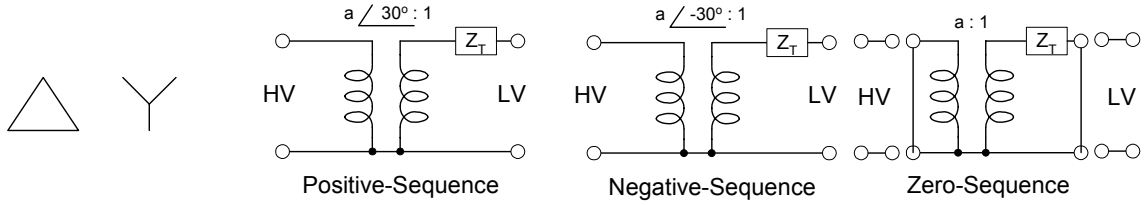


Figure 11.35: Delta–Wye Transformer Sequence Impedance Networks

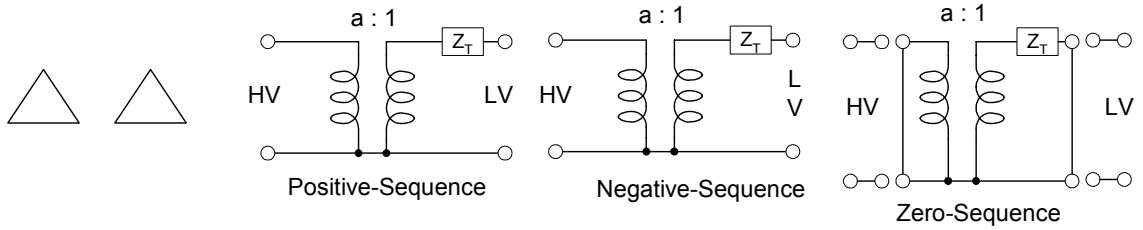


Figure 11.36: Delta-Delta Transformer Sequence Impedance Networks

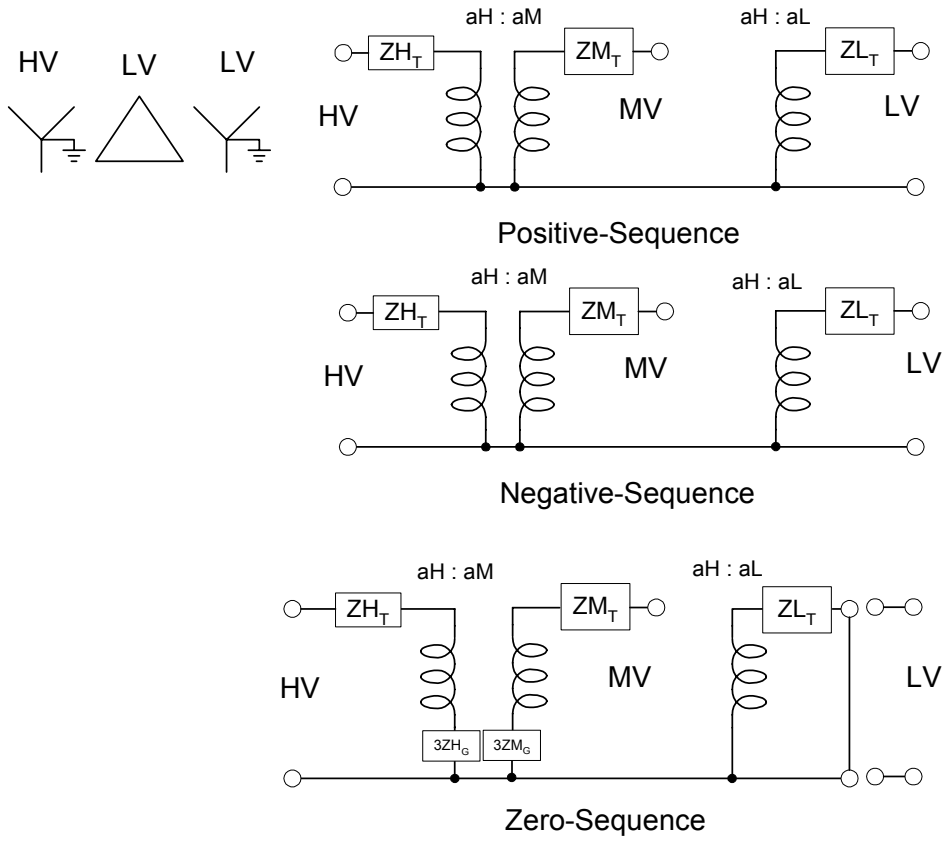


Figure 11.37: Wye-Grounded–Wye-Grounded–Delta Tertiary Transformer Sequence Impedance Networks

11.12.2 Two-Source Faulted Networks Symmetrical Component Impedance Network Diagrams

11.12.2.1 Single-Line-to-Ground Faults

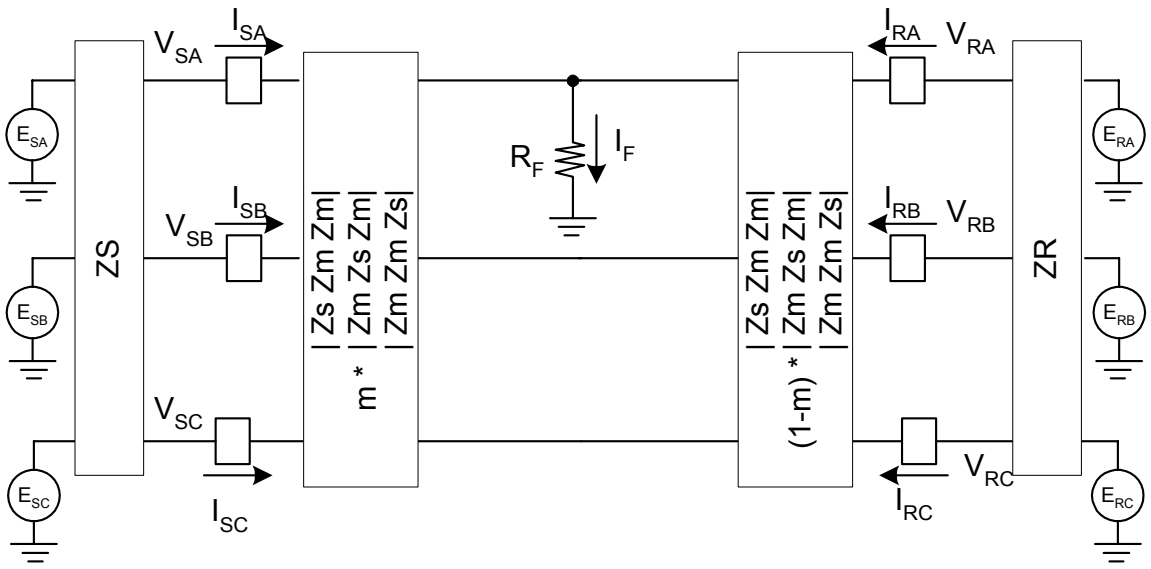


Figure 11.38: Single-Line-to-Ground Fault Three-Line Diagram

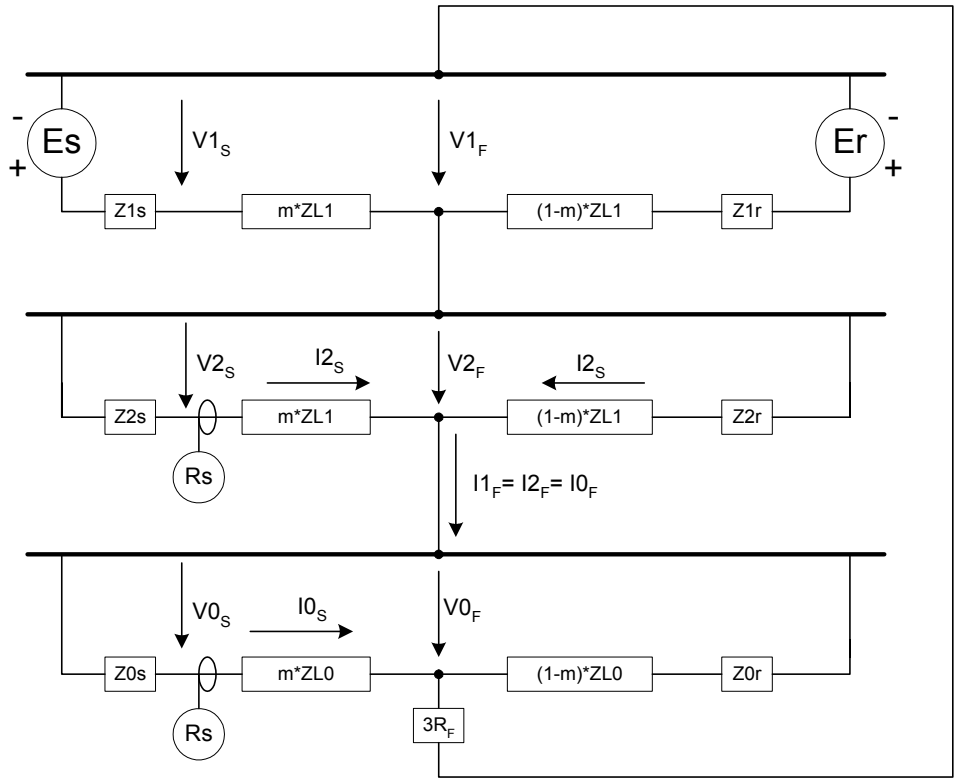


Figure 11.39: Single-Line-to-Ground Fault Symmetrical Component Diagram

11.12.2.2 Line-to-Line Faults

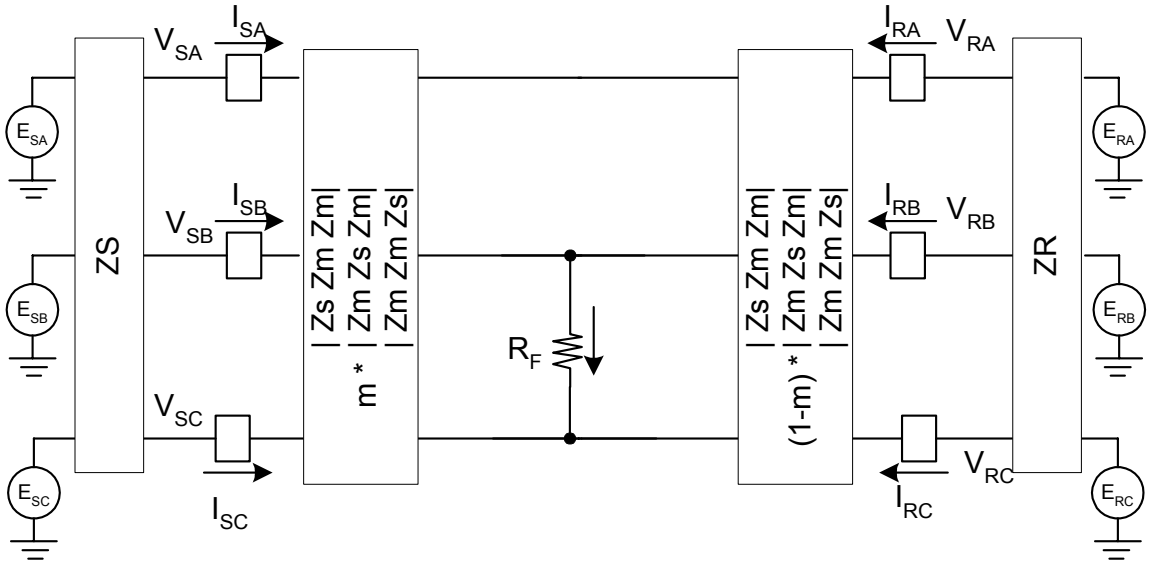


Figure 11.40: Line-to-Line Fault Three-Line Diagram

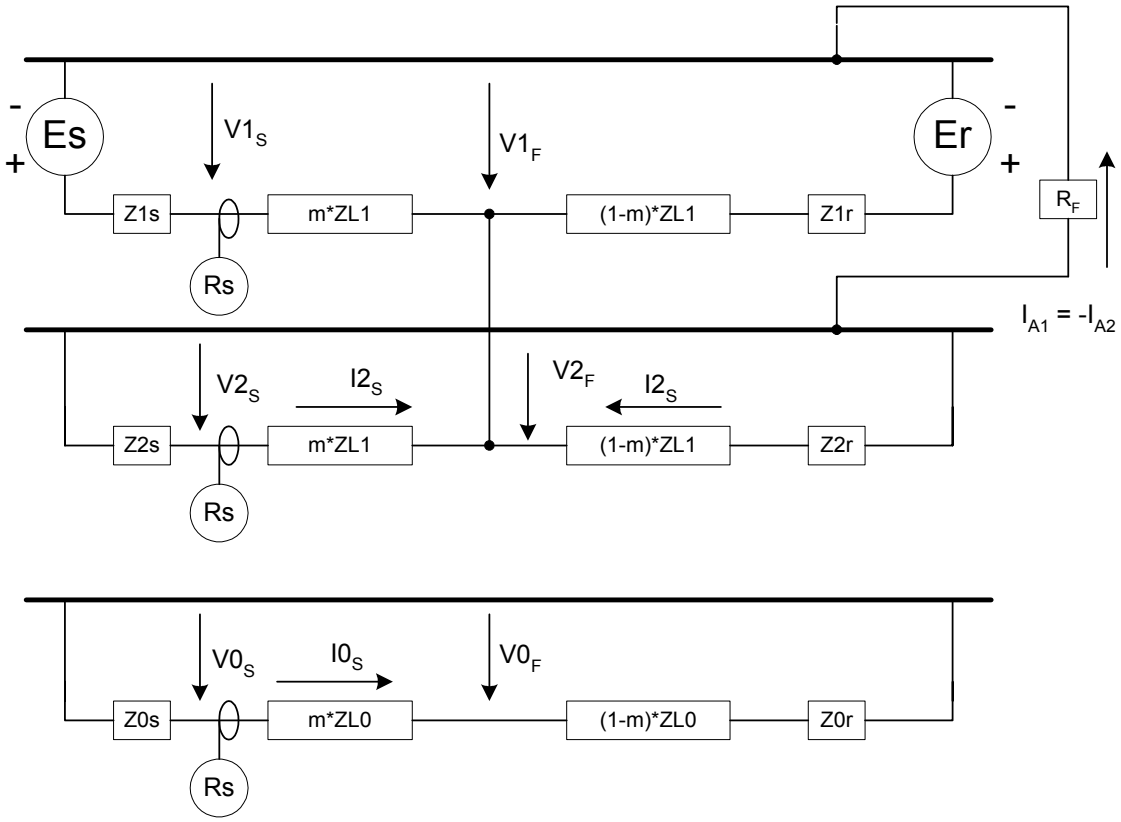


Figure 11.41: Line-to-Line Fault Symmetrical Component Diagram

11.12.2.3 Line-to-Line-to-Ground Faults

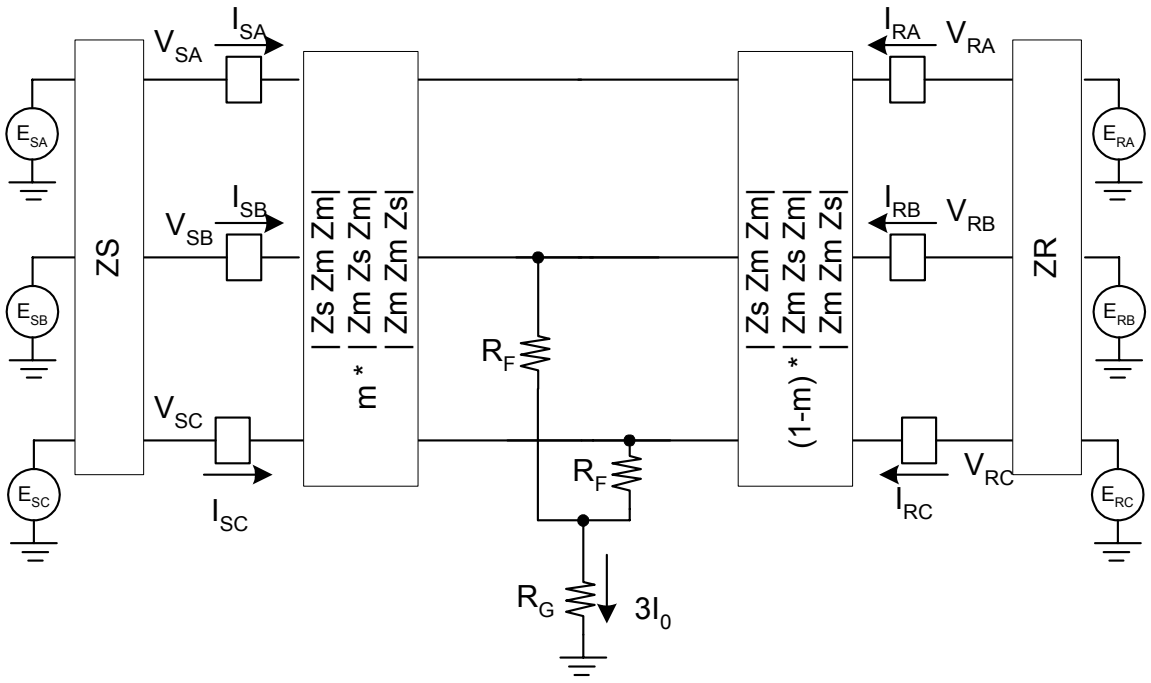


Figure 11.42: Line-to-Line-to-Ground Fault Three-Line Diagram

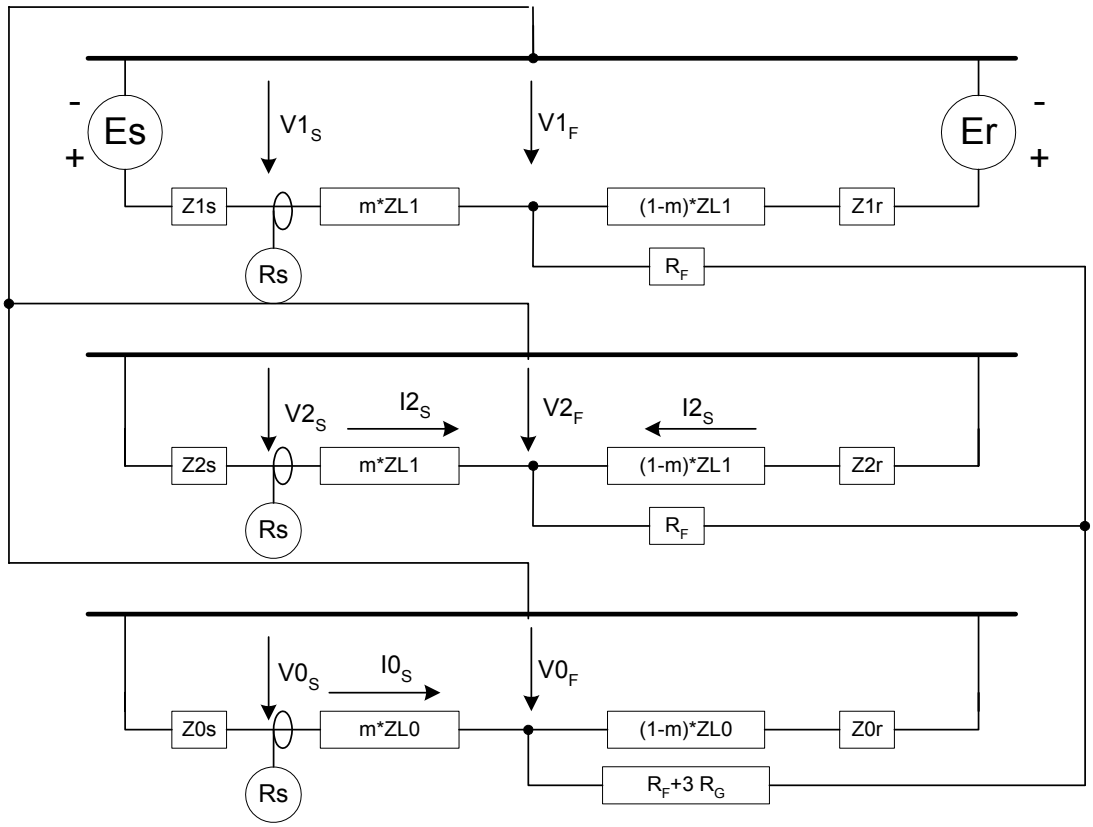


Figure 11.43: Line-to-Line-to-Ground Fault Symmetrical Component Diagram

11.12.2.4 Three-Line-to-Ground Faults

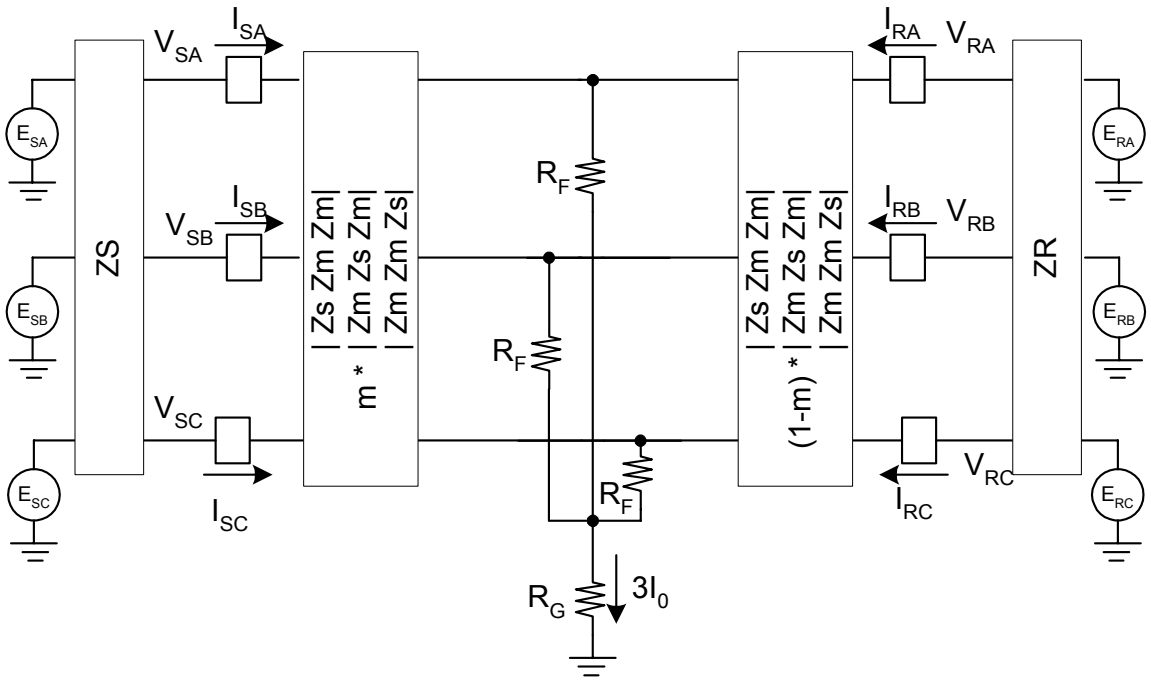


Figure 11.44: Three-Line-to-Ground Fault Three-Line Diagram

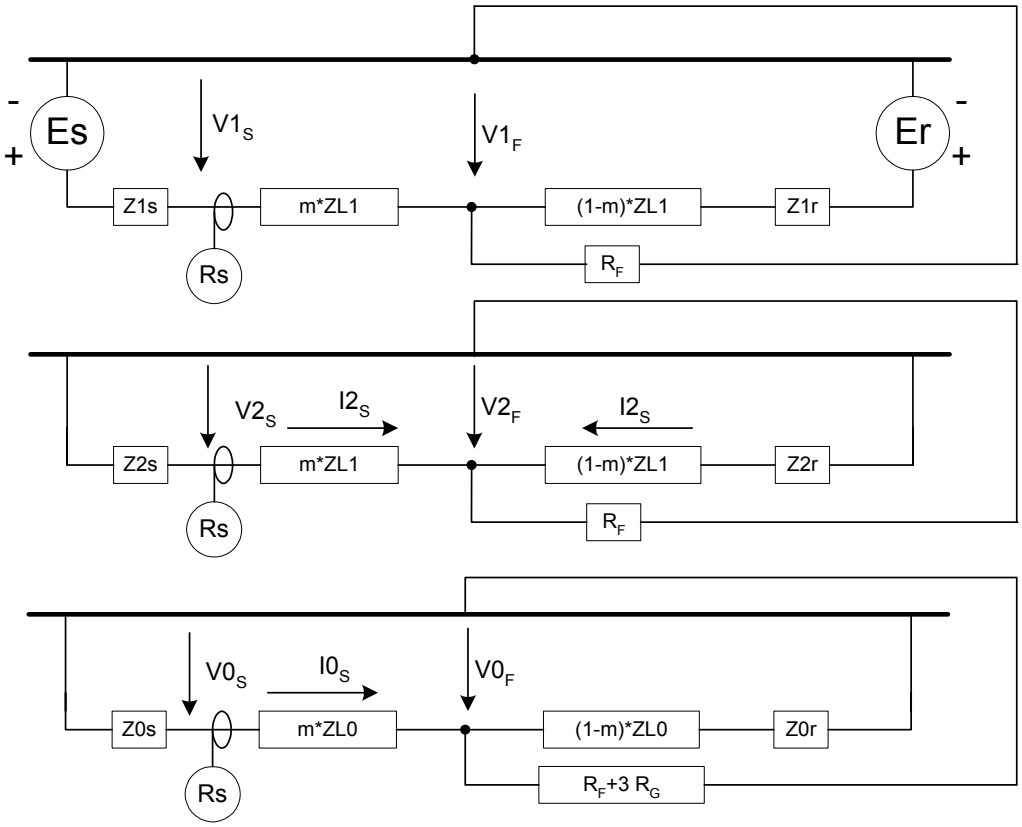


Figure 11.45: Three-Line-to-Ground Fault Symmetrical Component Diagram

11.12.2.5 Single-Line Open

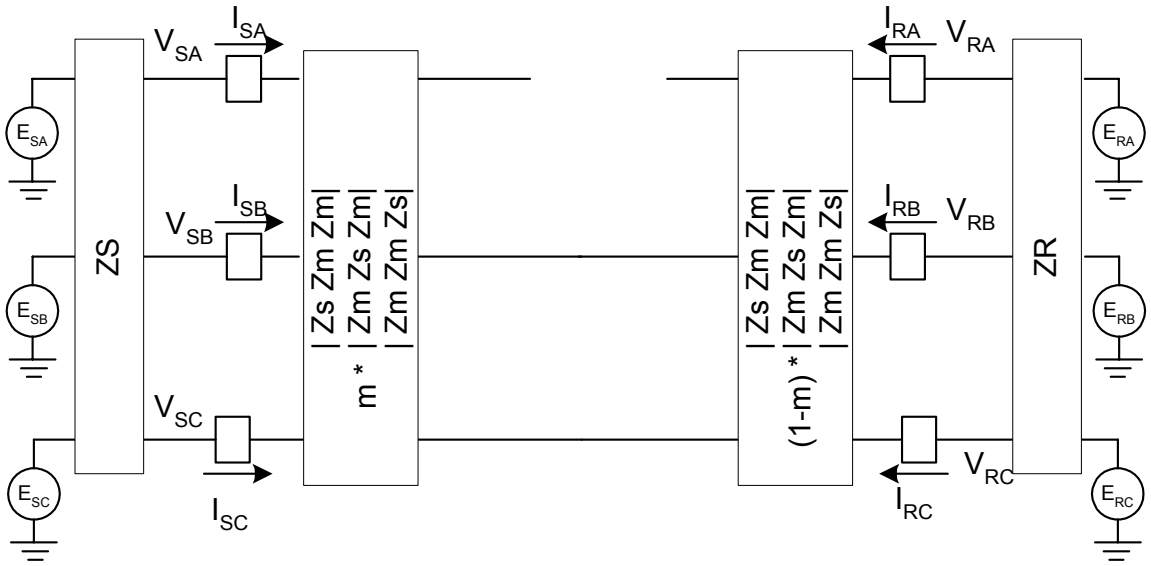


Figure 11.46: Single-Line Open Three-Line Diagram

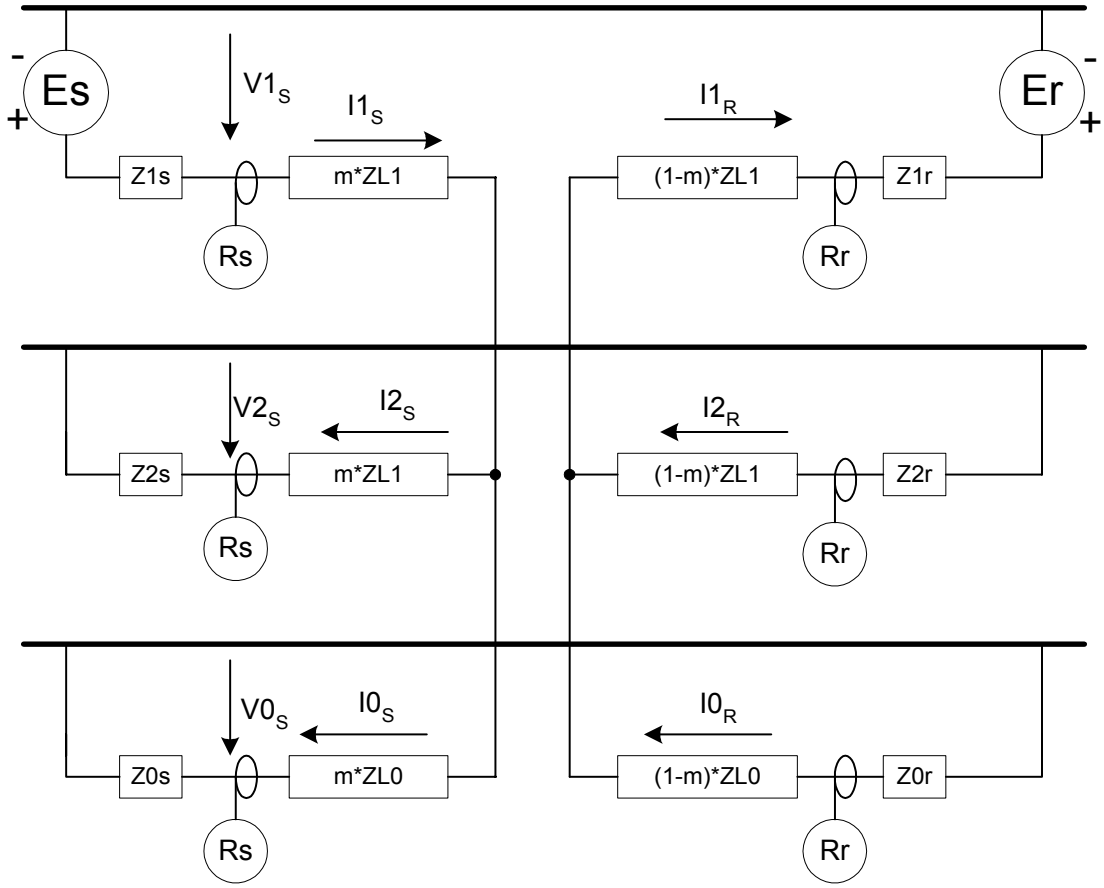


Figure 11.47: Single-Line Open Symmetrical Component Diagram

11.13 APPENDIX XII. TRANSFORMER MODELING

11.12.1 Basic Transformer Model

Figure 11.48 shows a simple single-phase shell-type transformer with two windings. We used a transformer bank with three single-phase transformers for testing and modeling purposes. The total flux in Winding 1 is the sum of the mutual flux (Φ) plus the Winding 1 leakage flux (ϕ_{11}). The sum of the mutual flux (Φ) plus the Winding 2 leakage flux (ϕ_{22}) determines the total flux in Winding 2.

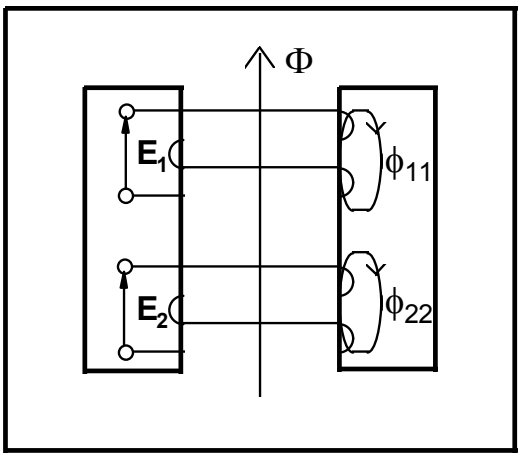


Figure 11.48: Single-Phase Two-Winding Transformer

The following expressions determine the relationship between voltages, currents, and mutual flux in the transformer core:

$$E_1 = R_1 \cdot I_1 + L_1 \cdot \frac{\Delta I_1}{\Delta T} + N_1 \cdot \frac{\Delta \Phi}{\Delta T}$$ Equation 11.51

$$E_2 = R_2 \cdot I_2 + L_2 \cdot \frac{\Delta I_2}{\Delta T} + N_2 \cdot \frac{\Delta \Phi}{\Delta T}$$ Equation 11.52

$$\Delta \Phi = P \cdot N_1 \cdot \Delta I_1 + P \cdot N_2 \cdot \Delta I_2$$ Equation 11.53

where:

E1	Winding 1 input voltage, volts
E2	Winding 2 input voltage, volts
I1	Winding 1 current, amps
I2	Winding 2 current, amps
R1	Winding 1 resistance, Ω
R2	Winding 2 resistance, Ω
P	Core permeance, Wb/(amp-turn)
L1	Winding 1 leakage inductance, H
L_2	Winding 2 leakage inductance, H
N_1	Winding 1 number of turns, turns
N_2	Winding 2 number of turns, turns
ΔI	Incremental current, amps
Δ□	Incremental magnetic flux, Wb
ΔT	Incremental time, seconds

The ratio $\Delta\phi/\Delta I$ times N determines the leakage inductance (for example, $\Delta\phi_{11}/\Delta I_1$ times N_1 determines the Winding 1 leakage inductance L_1). Equation 11.54 shows the matrix representation of Equation 11.51 through Equation 11.53.

$$\begin{bmatrix} E_1 - R_1 \cdot I_1 \\ E_2 - R_2 \cdot I_2 \\ 0 \end{bmatrix} = \begin{bmatrix} L_1 & 0 & N_1 \\ 0 & L_2 & N_2 \\ P \cdot N_1 & P \cdot N_2 & -1 \end{bmatrix} \cdot \begin{bmatrix} \frac{\Delta I_1}{\Delta T} \\ \frac{\Delta I_2}{\Delta T} \\ \frac{\Delta \Phi}{\Delta T} \end{bmatrix} \qquad \text{Equation 11.54}$$

Winding 1 and 2 voltages are the input quantities to the transformer model. We want to determine the current values for different transformer operating conditions. The first matrix in the right term of Equation 4 is the Coefficient Matrix. Equation 5 is the matrix representation of the incremental values of Winding 1 and Winding 2 currents and the incremental value of the mutual flux.

$$\begin{bmatrix} \frac{\Delta I_1}{\Delta T} \\ \frac{\Delta I_2}{\Delta T} \\ \frac{\Delta \Phi}{\Delta T} \end{bmatrix} = \begin{bmatrix} L_1 & 0 & N_1 \\ 0 & L_2 & N_2 \\ P \cdot N_1 & P \cdot N_2 & -1 \end{bmatrix}^{-1} \cdot \begin{bmatrix} E_1 - R_1 \cdot I_1 \\ E_2 - R_2 \cdot I_2 \\ 0 \end{bmatrix} \qquad \text{Equation 11.55}$$

All terms in the Coefficient Matrix have fixed values except the permeance P. The following expression determines the permeance of a given transformer core:

$$P = \frac{\mu \cdot A}{\ell} \qquad \text{Equation 11.56}$$

where

μ Permeability, H/m

A Transformer core area, m^2

ℓ Mean core length, m

The ratio of the incremental value of the flux density to the incremental value of the magnetic field intensity determines the permeability μ.

$$\mu = \frac{\Delta B}{\Delta H} \qquad \text{Equation 11.57}$$

where

ΔB Incremental magnetic flux density, Wb/m^2 (Tesla)

ΔH Incremental magnetic field intensity, amp-turn/m

Figure 11.49 shows the well-known anhysteretic B-H curve for ferromagnetic materials with initial relative permeability $\mu_i = 15000$ and saturation flux density $B_{SAT} = 1.8$ Wb/m^2. As we can see, the permeability μ is a nonlinear function of the magnetic flux density and magnetic field intensity. The main problem when modeling transformers with an iron core is a mathematical problem. In this case, we

have to solve three differential equations. We solve these equations with the fifth-order Runge-Kutta numerical method.

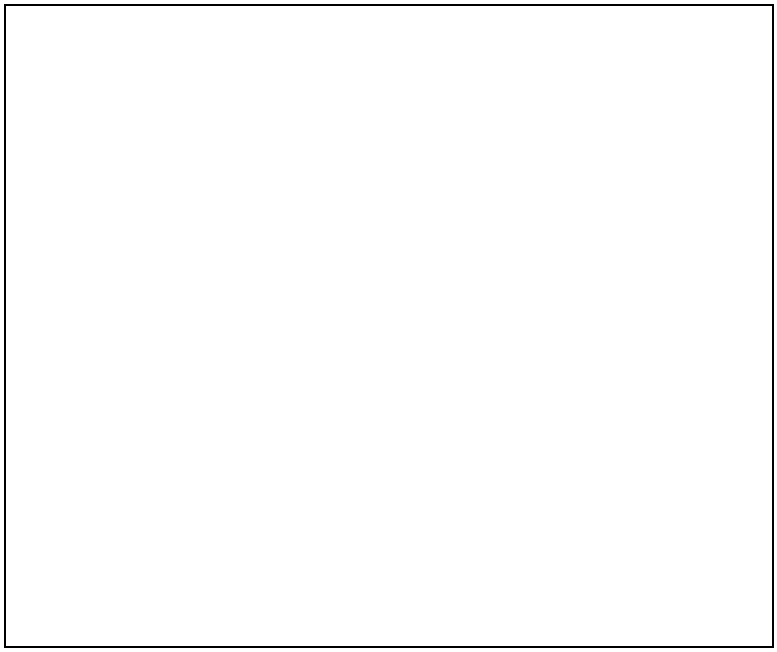


Figure 11.49: Anhysteretic B-H Curve of Ferromagnetic Materials With mi = 15000 and BSAT = 1.8 Wb/m2

The empirical Frolich Equation 11.58 models the S shape of the anhysteretic B-H curve [2].

$$B = \frac{H}{c + b \cdot |H|}$$

where Equation 11.58

B Magnetic flux density, Wb/m^2

H Magnetic field intensity, (amp-turn)/m

The following equations determine the empirical b and c constants:

$$c = \frac{1}{\mu_i \cdot \mu_0}$$

and

$$b = \frac{1 - \frac{1}{\sqrt{\mu_i}}}{B_{SAT}}$$ Equation 11.59

μ_i Initial relative permeability

μ_0 Free space permeability

B_{SAT} Saturation flux density

We use the anhysteretic curve modeled by the Frolich Equation to determine the permeability values for the different magnetic flux conditions presented in transformer operation.

We can model the iron core hysteresis loops using the Jiles and Atherton [3]this is reference 3 in tech paper 6025 and is not listed in text references Method. We use the Frolich Equation 11.58 to model the anhysteretic B-H curve instead of the Langevin Expression proposed in the original paper. Figure 11.50 shows the hysteresis loops using this approach. From our initial modeling studies, we found that modeling hysteresis does not improve the transformer model significantly for relay performance evaluation. We did not model hysteresis in most of our cases. Without taking into account hysteresis, the transformer model is less complex and uses less simulation time. We can model Eddy currents with an additional third winding.

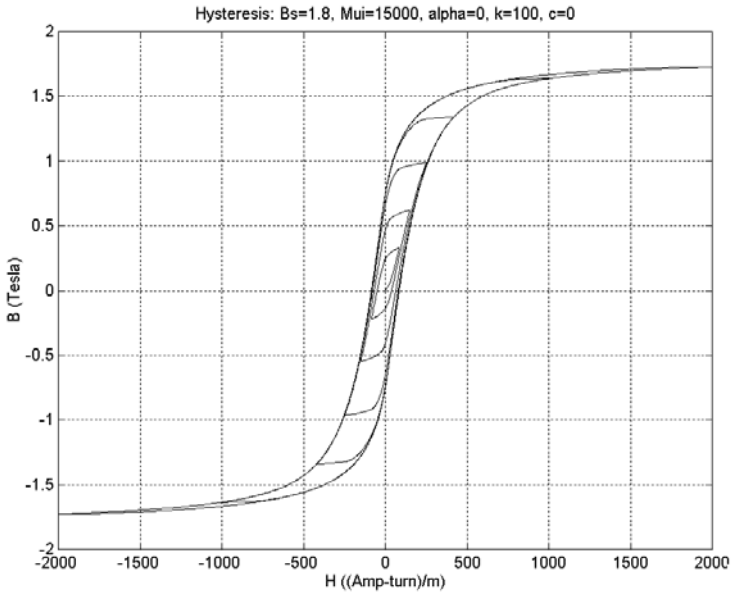


Figure 11.50: Hysteresis Loops Using the Jiles and Atherton Model

Figure 11.51 shows the basic algorithm of the transformer-modeling program. We use this program to model power and current transformers. Because the primary current is known in the current transformer model, we only need to calculate the mutual flux and the secondary current. We solve two equations instead of solving Equation 11.51 through Equation 11.53.

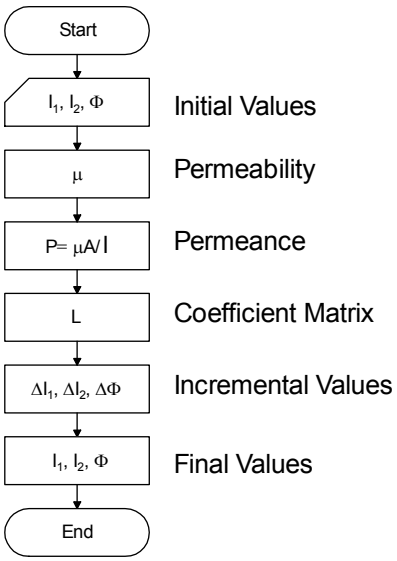


Figure 11.51: Transformer Model Algorithm

11.12.2 Transformer Model Evaluation

We recorded the current signals while energizing and overexciting a laboratory transformer. Appendix A shows the laboratory transformer and power system source data that we used in the transformer model. We compared the recorded signals with the modeled signals to validate the model.

11.12.2.1 Transformer Energization

Figure 11.52 shows the C-phase inrush current while energizing the 15 kVA transformer bank (three 5 kVA single-phase transformers). We applied 121.24 volts to the low-voltage side of each of the single-phase transformers. The high side of the transformer was open circuited. The C-phase voltage incidence angle was zero at the time of transformer energization. The instantaneous value of the first peak of the inrush current was approximately 260 amps. The transformer nominal current is 43.5 amp rms (61.5 amp peak). The inrush peak current is approximately 4.2 times the nominal peak current. How well does the transformer model simulate this condition?

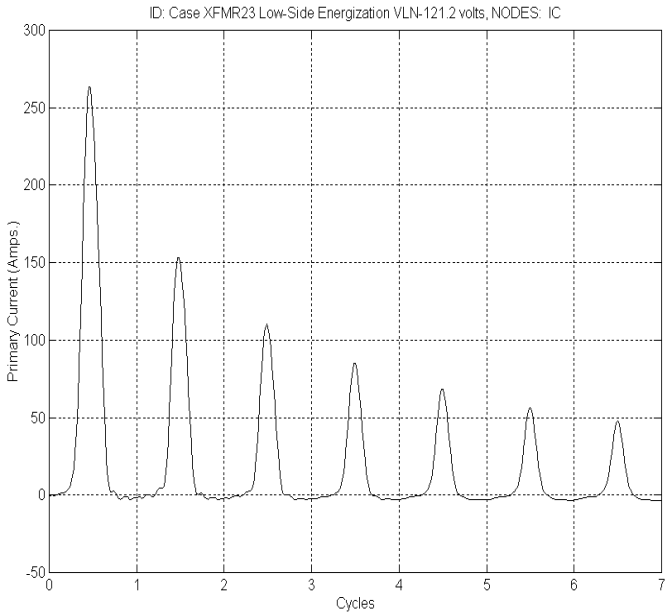


Figure 11.52: C-Phase Inrush Current Obtained from Transformer Testing

Figure 11.53 shows the C-phase inrush current obtained with the transformer model for the same conditions. As we can observe from both graphs, the current waves are similar in magnitude and in shape. The first two peaks of the inrush current are 260 and 155 amps spaced 1 cycle from each other.

The voltage incidence angle and the residual flux are main factors to determine the first peak value of the inrush current. The residual flux was zero for this energization condition. The system time constant (L/R) determines how fast the inrush current diminishes. From 11.12.3, the system time constant is 6.6 ms for this condition.

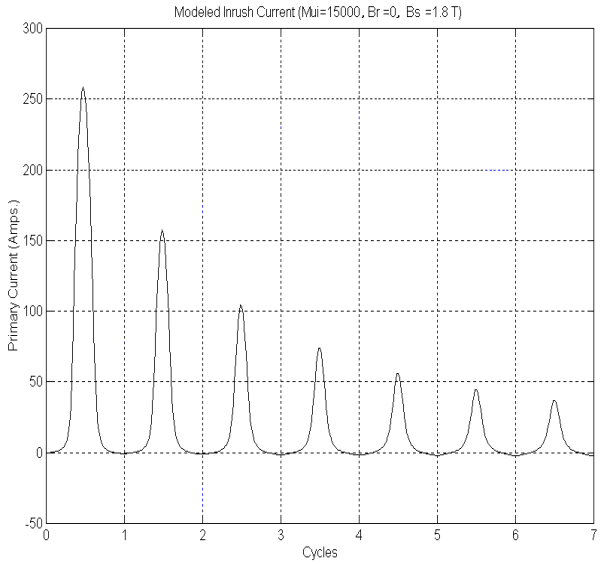


Figure 11.53: C-Phase Inrush Current Obtained from Transformer Modeling

11.12.2.2 Fundamental Frequency and Second-Harmonic Content of the Inrush Current

Figure 11.54 shows the fundamental frequency and second-harmonic content of the C-phase inrush current shown in Figure 11.53. The maximum fundamental frequency current magnitude is 71.9 amps, and the maximum second-harmonic magnitude is 48.0 amps. Both magnitudes decrease as the inrush current diminishes. Figure 11.54 also shows the second harmonic as percentage of the fundamental frequency current. This percentage is above 60% for this energization condition.

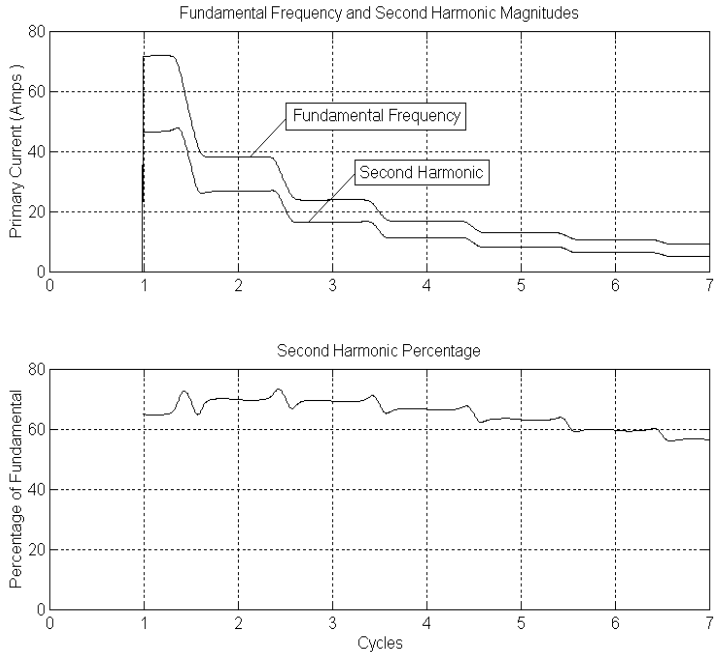


Figure 11.54: Fundamental Frequency and Second-Harmonic Content of the Inrush Current

11.12.2.3 Transformer Overexcitation

Figure 11.55 shows the A-phase excitation current that we recorded when we applied 150% overvoltage to the low-side windings of the single-phase transformer bank.

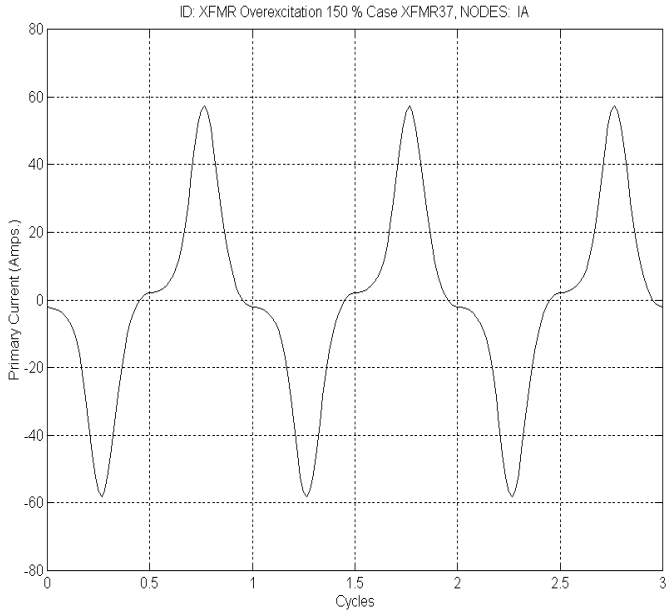


Figure 11.55: A-Phase Current Obtained from Transformer Testing. 150 Percent Overvoltage on the Low Side of the Transformer

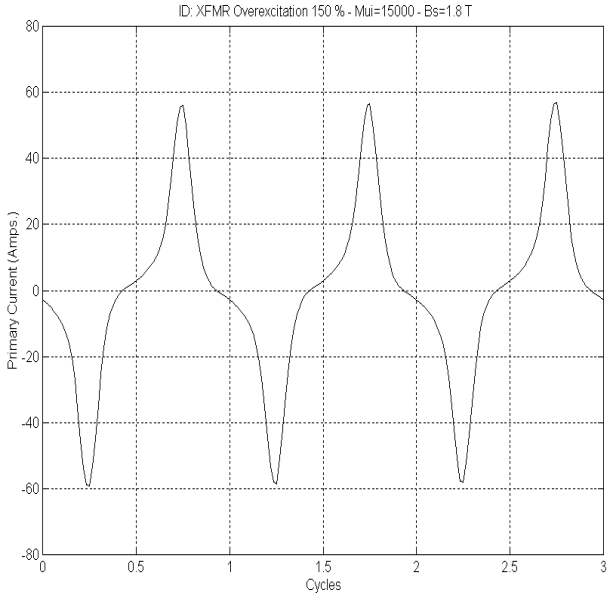


Figure 11.56: A-Phase Current Obtained from Transformer Modeling. 150 Percent Overvoltage on the Low Side of the Transformer

Figure 11.56 shows the A-phase current obtained with the transformer model for the same overvoltage condition. The peak value of the excitation current is approximately 57 amps in the actual current and in the modeled current. The two current waves are similar in magnitude and in shape. To properly simulate the

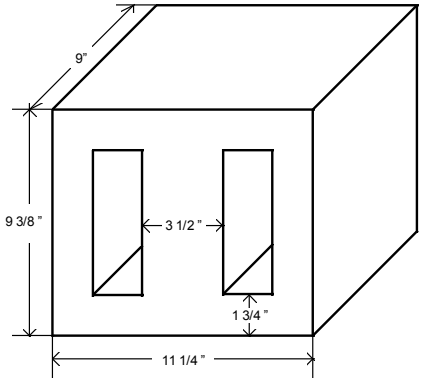
excitation current zero crossings, we modeled the hysteresis loops for this overexcitation condition.

Table 11.2 shows the odd-harmonic content of the current signal shown in Figure 11.57**Error! Reference source not found.**. The third and fifth harmonics provide reliable quantities to detect overexcitation conditions. The third harmonic is filtered out with the delta [96]connection compensation of the differential relay or the delta connection of the CTs. A fifth-harmonic level detector can identify overexcitation conditions.

Table 11.2: Harmonic Content of the Excitation Current While Overexciting the Transformer Bank

Frequency Component	Magnitude (Primary Amps)	Percentage of Fundamental
Fundamental	22.5	100.0
Third	11.1	49.2
Fifth	4.9	21.7
Seventh	1.8	8.1

11.12.3 Transformer and Source Data



5 kVA
230/115 V
60 Hz

Figure 11.57: Single-Phase Shell-Type Transformer Core

Transformer data:

N1	= 36	turns
N2	= 18	turns
	= 0.02	m2
	= 0.58	m
L_1	= 0.24	mH
R_1	= 1.5	mΩ
L_2	= 0.06	mH
R_2	= 0.38	mΩ

Source Data:

L_S= 0.7 mH
RS= 115 mΩ

Note: The transformer model adds the source impedance to the winding impedance.

11.12.1 Zero-Sequence Removal and Connection Compensation

In some power transformer connections, the low-side currents are not in phase with the high-side currents. For example, Figure 20 shows a transformer with delta connection in the high side and wye connection in the low side. The current in the high-side I_A-I_B leads the current in the low-side I_a by 30 ^{o}. The normal way to compensate the phase shift between the high- and low-side current is to connect the low-side CTs in delta and the high-side CTs in wye as shown in **Error! Reference source not found.**.

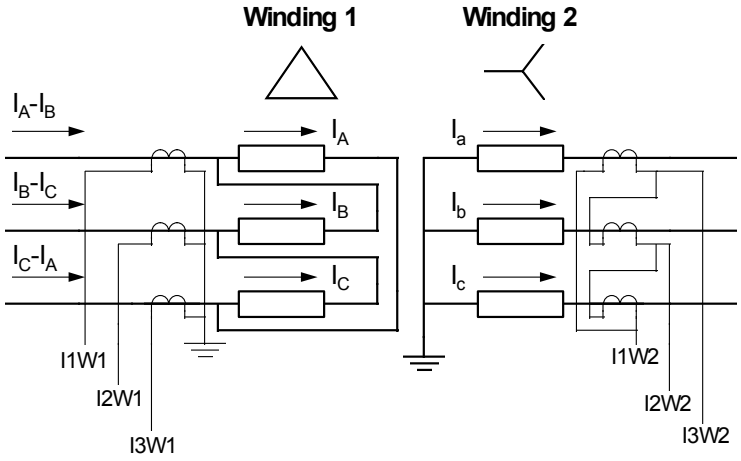
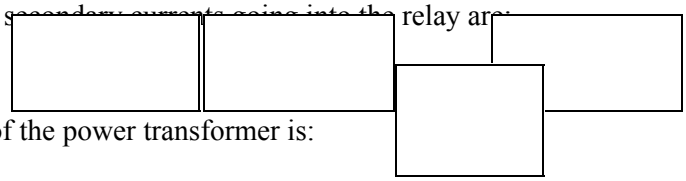


Figure 11.58: Delta-Wye Transformer Connection With Traditional CT Connections

The Winding 1 secondary currents going into the relay are:



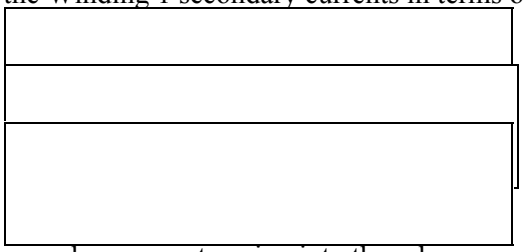
The turn ratio of the power transformer is:

where:

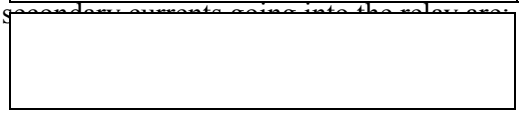
V_H - High-Side Voltage

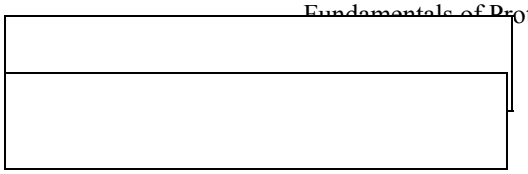
V_L - Low-Side Voltage

We can express the Winding 1 secondary currents in terms of Winding 2 primary currents:



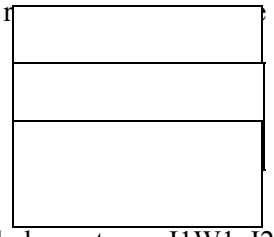
The Winding 2 secondary currents going into the relay are:





The CT delta connection in Winding 2 compensates the phase shift in the power transformer and filters out the zero-sequence current component. One phase current minus the adjacent phase current (I_a - I_b) filters out zero-sequence currents.

In applications where the CTs are wye connected at the low side of the power transformer, the following current combinations compensate the power transformer phase shift and r[illegible] currents:



The differential elements use I1W1, I2W1, I3W1, I1W2, I2W2, and I3W2 as input currents. The input currents to the differential elements do not have zero-sequence current component.

12 GLOSSARY

A-Symbol for Ampere

AC-In text, use lower case: ac. Abbreviation for Alternating Current

AC Brownout-The condition that exists when the ac line voltage drops below some specified value.

AC Line-The set of conductors that route ac voltage from one point to another.

AC Line Filter-A circuit filter placed in the ac line to condition or smooth out variations that are higher in frequency than the line frequency.

AC Loss Detector-A power-fail detector circuit that monitors the status of the ac lines.

Ah-Abbreviation for Ampere-Hour

ANSI-Abbreviation for American National Standards Institute

AWG-Abbreviation for American Wire Gauge

Abnormal Failure-The failure of a component resulting from an induced condition that causes a malfunction of the device.

Absolute Accuracy-The correctness of the indicated value in terms of its deviation from the true or absolute value.

Accumulator-See Secondary Battery

Accuracy Limits-See Total Regulation Band

Activated Stand Life-The period of time, at a specified temperature, that a cell can be stored in the charged condition before its capacity falls below a specified level.

Activation-The process of making a reserve cell functional, either by introducing an electrolyte, by immersing the cell into an electrolyte, or by other means.

Activation Polarization-Polarization resulting from the rate-determining step of the electrode reaction.

See also Polarization

Active Cell-A cell containing all components and in a charged state ready for discharge (as distinct from Reserve Cell).

Active Material-The material n the electrodes of a cell or battery that takes part in the electrochemical reactions of charge or discharge.

Air Gap-The separation between magnetic materials used to lower the permeability and increase the ampere turns before the core saturates. The gap is usually filled with a non-magnetic material other than air.

Alive (Live)-Electrically connected to a source of voltage difference or electrically charged so as to have a voltage different from that of earth; the term may be used in place of 'current-carrying' where the intent is clear, to avoid repetition of the longer term.

Alternating Current (ac)-A periodic current the average value of which over a period is zero. Unless distinctly specified otherwise, the term refers to a current that reverses at regularly recurring intervals of time and which has alternately positive and negative values.

Ambient Temperature-The average temperature of the environment immediately surrounding the power supply. For forced air-cooled units, the ambient temperature is measured at the air intake. See also Operating Temperature, Storage Temperature, Temperature Coefficient

American National Standards Institute (ANSI)-United States standards agency located in New York.

American Wire Gauge (AWG)-A standard for sizing cross-sectional areas of wire, and for measuring sheet-metal thickness.

Ampacity-Current carrying capacity of electric conductors expressed in amperes.

Ampere (A)-Electron or current flow representing the flow of one coulomb per second past a given point in a circuit.

Ampere-Hour (Ah)-A measurement of quantity of electricity computed as the product of current (in amperes) and time (in hours).

Ampere-Hour Capacity-The quantity of electricity measured in ampere-hours (Ah) which may be delivered by a cell or battery under specified conditions.

Ampere-Hour Efficiency-The ratio of the number of ampere-hours delivered during the discharge of a secondary cell or battery to the number of ampere-hours necessary to restore the initial state of charge under specified conditions.

Ampere-Turn-The SI unit of electromagnetic force defined as the field produced by the flow of one ampere in a single turn of wire in a coil.

Amplifier-A circuit or element that provides gain.

Amplifier, DC -A direct coupled amplifier that can provide gain for zero-frequency signals.

Amplifier, Differential-An amplifier which has available both an inverting and a noninverting input, and which amplifies the difference between the two inputs.

Amplifier, Inverting-An amplifier whose output is 180 degrees out of phase with its input. Such an amplifier can be used with degenerative feedback for stabilization purposes.

Amplifier, Noninverting-An amplifier whose output is in phase with its input.

Amplifier, Operational-A dc amplifier whose gain is sufficiently large that its characteristics and behavior are substantially determined by its input and feedback elements. Operational amplifiers are widely used for signal processing and computational work.

Anion-Particles in the electrolyte carrying a negative charge and moving toward the anode during operation of the cell.

Anode-The electrode at which an oxidation reaction occurs. During discharge, the negative electrode of the cell is the anode. During charge, the situation reverses and the positive electrode of the cell is the anode.

Anode Terminal-In semiconductors, the terminal by which current enters the device. The positive terminal, such as the plate in an electron tube.

Anolyte-The portion of the electrolyte in a galvanic cell adjacent to the anode; if a diaphragm is present, the electrolyte on the anode side of the diaphragm.

Anti-Saturation Circuit-A circuit designed to prevent saturation of a bipolar switch transistor. See also Baker Clamp

Apparent Power-Power value obtained in an ac circuit as the product of current times voltage. See VA.

Aprotic Solvent-A nonaqueous solvent that does not contain a reactive proton although it may contain hydrogen in the molecule.

Asymmetrical Waveform-A current or voltage waveform that has unequal excursions above and below the horizontal axis.

ATE-automatic test equipment

ATG-automatic test generation

Attenuation-Decrease in amplitude or intensity of a signal.

Authorized Person-A qualified person who, by nature of his duties or occupation, is obliged to approach or handle electrical equipment or, a person who, having been warned of the hazards involved, has been instructed or authorized to do so by someone in authority.

Autoranging Input. An input voltage sensing circuit in the power supply that automatically switches to the appropriate input voltage range (90-132 VAC or 180-264 VAC). Sometimes known as Auto-select input. See also Universal Input.

Auto-Transformer-A single winding transformer with one or more taps. A transformer in which at least two windings have a common section.

Automatic Crossover-The characteristic of a power supply having the capability of switching its operating mode automatically as a function of load or setting from the

stabilization of voltage to the stabilization of current. The term automatic crossover power supply is reserved for those units having substantially equal stabilization for both voltage and current. Not used for voltage-limited current stabilizers or current-limited voltage stabilizers. See also Crossover Point

Auxiliary Supply-A power source supplying power other than load power as required for the proper functioning of a device.

Available Capacity-The total capacity, Ah or Wh, that will be obtained from a cell or battery at defined discharge rates and other specified discharge or operating conditions.

Average Drain-The average current withdrawn from a cell or battery during discharge.

Average Value-The value of alternating current or voltage of sine wave form that is found by dividing the area under one alternation by the distance along the X axis between 0 and 180 deg.

Eavg = .637 Emax

Eavg = 2/T e(t)dt

Averaging Filter-See L-C Filter

Backup Power Supply-A power supply used to provide alternate system power in the event the primary power source fails or is unable to continue providing adequate system power.

Baker Clamp-A circuit used in the base drive of a bipolar power switch to prevent the transistor from going into deep saturation. By reducing excess charge in the base emitter junction, it allows faster turn off of the transistor.

Balun- "Balanced to unbalanced" A differential wound choke used as an EMI filter component. Presents a high impedance to common-mode signals and a low impedance to differential mode signals.

Bandwidth-Based on the assumption that a power supply can be modeled as an amplifier, the bandwidth is that frequency at which the voltage gain has fallen off by 3 dB. Bandwidth is an important determinant of transient response and output impedance.

Baseplate-Mounting platform for power supply components.

Baseplate Temperature-The temperature at the hottest spot on the mounting platform of the supply.

Basic Insulation-The insulation applied to live parts to provide basic protection against electric shock.

See also Insulation

Battery-Two or more electrochemical cells electrically interconnected in an appropriate series/parallel arrangement to provide the required operating voltage and

current levels. Under common usage, the term 'battery" is often also applied to a single cell.

Battery Back-up-Battery support to maintain function of selected components or devices.

Battery Charger-Electrical equipment designed to restore capacity to secondary batteries.

Battery Crate-A container with frame walls for holding several groups of cells or batteries. Usually used in railroad applications.

Battery Rack-A rigid support of one or more levels for stationary cells. Also called a battery stand.

Battery Voltage-The total voltage between the positive and negative terminals of the battery. See also Nominal Voltage, Voltage, Working Voltage

Bead-A small ferrite normally used as a high frequency inductor core.

Bench Power Supply-A power source fitted with output controls, meters, terminals and displays for experimental bench-top use in a laboratory.

Bifilar Winding-Two conductors wound in parallel.

Bipolar-Having two poles, polarities or directions.

Bipolar Plate-An electrode construction where positive and negative active materials are on opposite sides of an electronically conductive plate.

Bipolar Power Supply-A special power supply which responds to the sense as well as the magnitude of a control instruction and is able to linearly pass through zero to produce outputs of either positive or negative polarity.

Bipolar Switch-A bipolar transistor used as a switch.

Bipolar Transistor-A junction transistor having both majority and minority charge carriers.

Bit-A binary unit of digital information having a value of "0" or "1". See also Byte

Black Box-Element in a system specified by its function, or operating characteristics.

Bleed-A low current drain from a power source.

Bleeder Resistor-A resistor that allows a small current drain on a power source to discharge filter capacitors or to stabilize an output.

Bobbin-1) A non-conductive material used to support windings. 2) A cylindrical electrode (usually the positive) pressed from a mixture of the active material, a conductive material, such as carbon black, the electrolyte and/or binder with a centrally located conductive rod or other means for a current collector.

Bode Plot-A plot of gain versus frequency for a control loop. It usually has a second plot of phase versus frequency.

Bonding-A low impedance path obtained by permanently joining all non-current-carrying metal parts to assure electrical continuity and having the capacity to conduct safely any current likely to be imposed on it.

Boost Charge-A charge, generally at high-rate, far a limited period to restore capacity in all cells of a battery.

Boost Regulator-One of several basic families of switching power supply topologies. Energy is stored in an inductor during the pulse then released after the pulse.

Boundary Layer-The volume of electrolyte solution immediately adjacent to the electrode surface in which concentration changes occur due to the effects of the electrode process.

Bounding-The process of providing a boundary or limit to various output quantities. Fuses, circuit breakers and current limiters, as well as overvoltage crowbars, spark gaps and voltage limiters, are all examples of bounding circuits.

Branch-The current path between two voltage nodes in a circuit.

Branch Circuit-That portion of the wiring installation between the final overcurrent device protecting the circuit and the line connection.

Branch Circuit Protection-An overcurrent protection circuit or device that protects the branch circuit.

Break Frequency-A frequency at which two asymptotes of a bode plot intersect.

Breakdown Voltage-1) The voltage level which causes insulation failure. 2) The reverse voltage at which a semiconductor device changes its conductance characteristics.

Bridge Circuit-Circuit with series-parallel groups of components.

Bridge Converter-A power conversion circuit with the active elements connected in a bridge configuration.

Bridge Rectifier-Full-wave rectifier circuit employing two or more rectifiers in a bridge configuration.

Bridge, Wheatstone-A bridge circuit for determining the value of an unknown component by comparison to one of known value.

Brown and Sharp Wire Gauge-A standard for sizing non-ferrous conductors and non-ferrous sheet metal.

Brownout-The condition created during peak usage periods when electric utility companies intentionally reduce their Tine voltage by approximately 10 to 15 percent to counter excessive demand.

Brute-Force Supply-A basic form of power supply that delivers relatively unfiltered, unregulated power.

Buck Regulator-One of several switching power supply topologies where a series of pulses are applied by a switching device to an averaging L-C filter and then applied to a load.

Built-in Test-The capability of a power supply to monitor its own vital functions and to identify potential or actual failures.

Bulk Capacitor-The energy storage capacitor at the front end of a regulator.

Bulk Voltage-The voltage across a bulk capacitor.

Burn In-The operation of a newly fabricated device or system prior to application with the intent to stabilize the device, detect defects, and expose infant mortality. In power supplies, a period during which a supply is energized and loaded to peak output, with the intent of finding potentially weak components. Typical burn-in tests can include temperature cycling, input cycling, and/or load cycling

Bus-The common primary conductor of power from a power source to two or more separate circuits.

Bysyn-Trade name for a symmetrical bipolar transistor designed for synchronous rectification.

Byte-A sequence of binary digits, frequently comprised of eight (8) bits, addressed as a unit. See also Bit

C-Variously, the abbreviation for capacitance, capacitor, Celsius, centigrade and coulomb.

C_5-Symbol for ampere-hour capacity at the five-hour discharge rate to an end voltage.

CCV-Abbreviation for Closed-Circuit Voltage

CE - A mark applied to an end-use product certifying that the product meets "applicable directives" and can be sold in Europe. "Certified Europe" is the result of the "harmonization" or unification of European safety and other standards. Each type of end-use equipment has "applicable directives" which must be met in order to display the CE mark. Power supplies intended for use within an end-use system are not required to have a CE mark. However, many power supply manufacturers offer CE-certified power supplies which have been tested to the applicable directives which the power supply manufacturer believes will be necessary for the anticipated end-use equipment.

CEMF-Abbreviation for Counter Electromagnetic Force

CGS Unit-Abbreviation for the Centimeter-Gram-Second Unit of measurement.

C Rate-1) Discharge or charge current, in amperes, expressed in multiples of the rated capacity. A cell's capacity is not the same at all discharge rates and usually increases with a decreasing rate of discharge. See Hourly Rate. 2) C/X Rate-The current which would be necessary to discharge or charge a cell of a given rated capacity (C) in X hours if the cell maintained the same rated capacity at all discharge rates. For example, a 2.5 ampere-hour cell, rated at the 10-hour rate, will provide 250 milliamps for 10 hours. In the real world, however, a cell does not maintain the same rated capacity at all discharge rates.

CSA-Abbreviation for Canadian Standards Association

CW-Abbreviation for Continuous Wave

Canadian Standards Association (CSA)-An organization chartered to test and evaluate products and to set applicable safety standards in Canada.

Capacitance-Inherent property of an electric circuit or device that opposes change in voltage. Property of circuit whereby energy may be stored in an electrostatic field.

Capacitance, Distributed-The capacitance in a circuit resulting from adjacent turns on coils, parallel leads and connections.

Capacitive Coupling-Coupling resulting from the capacitive effect between circuit elements.

Capacitive Effect Leakage Current-The current flow between segregated conductive metal parts; voltage and frequency dependent.

Capacitive Reactance (XC)-Opposition to ac as a result of capacitance.

Capacitor-A device that stores a charge. A simple capacitor consists of two conductors separated by a dielectric.

Capacitor Input Filter-Filter employing capacitor as its input.

Capacity-The ability of a component, battery or other device to store and discharge a given quantity of current (A) or power (W) over a specified period of time (Ah or Wh).

Capacity Current-The fraction of the cell current consumed in charging the electrical double layer.

Capacity Retention-The fraction of the full capacity available from a battery under specified conditions of discharge after it has been stored for a period of time. See Charge Retention

Carbon-Zinc-A generic term for primary dry batteries of the LeClanche or Zinc Chloride system.

Carbonization-The formation of carbonate ions in an alkaline electrolyte owing to absorption of carbon dioxide from the air or from the topping-up water or to oxidation of carbonaceous matter within the cell. The carbonation can be expressed in % or in grams of potassium carbonate per liter of electrolyte.

Card Edge Connector-See Edge Connector

Carry-Over-See Holdup Time

Catch Diode-See Free Wheel Diode

Cathode-The electrode in an electrochemical cell where reduction takes place. During discharge, the positive electrode of the cell is the cathode. During charge, the situation reverses, and the negative electrode of the cell is the cathode.

Catholyte-The portion of an electrolyte in a galvanic cell adjacent to a cathode; if a diaphragm is present, the electrolyte on the cathode side of the diaphragm.

Cation-Particle, in the electrolyte, carrying a positive charge and moving toward the cathode during operation of the cell.

Cell-1) The basic electrochemical unit used to generate or store electrical energy. A cell consists of two electrodes of dissimilar material isolated from one another electronically, in a common ionically conductive electrolyte. 2) An electrochemical system which converts chemical energy into electrical energy and also the reverse for rechargeable units.

Cell Oil-A pure mineral type of oil used on top of the electrolyte in large, non-sealed alkaline cells to minimize electrolyte creepage and eliminate certain self-discharge reactions.

Cell Polarization-See Polarization

Cell Reversal-Reversal of polarity of a cell due to over discharge or forced discharge.

Cell Voltage-The dc voltage potential between the individual positive and negative terminals of a cell in a battery. See also Nominal Voltage, Voltage, Working Voltage

Center Tap-Connection made to center of an electronic device.

Centering-See Tolerance

Centimeter-Gram-Second Unit (CGS Unit)-An absolute unit based on the centimeter, gram and second as fundamental units.

Charge-1) The conversion of electrical energy, provided in the form of a current from an external source, into chemical energy within a cell or battery. 2) The potential energy stored in a capacitive electrical device.

Charge Acceptance-The ability of a battery to accept charge under specified conditions.

Charge Coefficient-The factor by which the quantity of electricity delivered during discharge is multiplied to determine the amount necessary for recharge.

Charge/Discharge Cycle-A sequence of a charge and subsequent discharge under specified conditions.

Charge Equalization-Bringing all of the cells in a rechargeable battery to the same state of charge.

Charge Rate-The current applied to a secondary cell or battery to restore its capacity. This rate is commonly expressed as a multiple of the rated capacity of the cell or battery. For example, the C/10 charge rate of a 500-Ah cell or battery is expressed as:

C/10 rate = 500 Ah/10 = 50 A

Charge Retention-The ability of a battery to retain capacity on open circuit under specified conditions of temperature. See Capacity Retention

Charge, State of-Condition of cell in terms of the rated capacity remaining in the cell at a given point in time.

Charge Voltage-The voltage applied to a cell during charge.

Charger-Device used to charge a cell or battery.

Charging-Process of restoring electrical energy into a rechargeable cell or battery. See also Charge

Charging Temperature Coefficient-The factor by which the charge voltage must be adjusted for a given change in temperature.

Chassis-The structure supporting or enclosing the power supply.

Chassis Ground-The voltage potential of the chassis.

Choke Coil-An Inductor

Choke, RF-A choke coil with a high impedance at radio frequencies.

Circuit Input Filter-A filter employing an inductor (L) or an inductor/capacitor (LIC) as its input.

Circular Mil-Cross-sectional area of a conductor one mil in diameter.

Circulating Current-See Ground Loop

Clamp Circuit-A circuit that biases a voltage waveform to a different voltage level.

Clamp Diode-A diode in either a clipper or clamp circuit.

Clearance Distance-The shortest path separating two conductors or two circuit components.

Clipper Circuit-A circuit that blocks or removes the portion of a voltage waveform above some threshold voltage.

Clock-An oscillator producing timing pulses to synchronize various elements of a system. In switching mode power supplies, a clock is used to produce the power pulses that are modulated to control power transfer. In digital interfaces that communicate on a bus (such as the IEEE-488) a clock is used to synchronize the data transfer and commands.

Closed-Circuit Voltage (CCV)-The potential or voltage at the terminals of an electrical device when current is flowing.

Closed Loop Buck Converter-A circuit where energy is pulsed to an averaging LIC filter and delivered to a load.

Closed Loop Gain-In a feedback control circuit, the increase in value of an output signal due to the effects on it of various other components or signals in the circuit. See also Gain

Coefficient of Coupling (K)-Percentage of mutual inductance, unless specified otherwise, between circuit elements expressed as a decimal.

Collector-1) Electronic connection between the electrochemical cell electrode and the external circuit. 2) In a transistor, the semiconductor section which collects the majority carriers.

Common Choke-See Integrated Magnetics

Common-Mode Noise-The component of noise voltage that appears equally and in phase on conductors relative to a common reference.

Common-Mode Output-That electrical output supplied to an impedance connected between the terminals of the ungrounded floating output of a power supply, amplifier, or line-operated device, and the ground point to which the source power is returned.

Common Point-With respect to operationally programmable power supplies one output/sense terminal is designated "common to which load, reference and external programming signal all return.

Common Return-A return conductor common to two or more circuits.

Communications Port-A standard communications interface, such as an IEEE 488 or RS-232, that provides information flow from a processor to a peripheral device, such as a power supply.

Commutation-Transfer of unidirectional current between circuit elements.

Comparison Amplifier-A dc amplifier which compares one signal to a stable reference, and amplifies the difference to regulate the power supply power-control elements.

Compensation-The addition of circuit elements to assist in stabilization of a control loop.

Complementary Tracking-A system of interconnection of two voltage stabilizers by which one voltage (the slave) tracks the other (the master).

Compliance-Agency certification that a product meets its standards. See also Safety Compliance

Compliance Voltage-The maximum dc output voltage of a constant current supply.

Compliance Range-Range of voltage needed to sustain a given constant current throughout a range of load resistance.

Component-An element in an electrical circuit.

Concentration Polarization-Polarization caused by the depletion of ions in the electrolyte at the surface of the electrode. See also Polarization

Conductance (G)-The ability to conduct current. It is equal to amperes per volt, or the reciprocal of resistance, and is measured in siemens (metric) or mhos (English). $G = 1/R$

Conductor-Material which permits free motion of large number of electrons.

Conformal Coating-An insulating layer often applied by spraying or dipping that covers and protects the components on a circuit board.

Conformance- Manufacturer's commitment that product meets specified standards.

Connector-A mechanical device used to link conductors.

Constant Current Charge-A charge during which the current is maintained at a steady state value.

Constant Current Limiting Circuit-Current-limiting circuit that holds output current at some maximum value whenever an overload of any magnitude is experienced.

Constant Current Load-An electronic load with a control loop to regulate the current drawn from the power supply.

Constant Current Power Supply-A power supply that regulates its output current, within specified limits, against changes in line, load, ambient temperature and time. Constant current supplies are sometimes used to drive certain types of loads (such as large incandescent lamps) or in certain applications where very long output leads can result in significant induced noise and resistive losses (such as industrial environments).

Constant Voltage Charge-A charge during which the voltage across the battery terminals is maintained at a steady state.

Constant Voltage Power Supply-A power supply that regulates its output voltage within specified limits, against changes in line, load, ambient temperature and time.

Constant Voltage Transformer-Maintains approximately constant voltage ratio over the range from zero to rated output.

Continuous Duty-A requirement of service that demands operation at a substantially constant load for an indefinitely long time. See also Intermittent Duty

Continuous Test-A test in which a cell or battery is discharged to a prescribed end-point voltage without interruption.

Continuous Wave (CW)-Uninterrupted sinusoidal rf wave radiated into space, with all wave peaks equal in amplitude and evenly spaced along time axis.

Control-The means of regulating the operation of a piece of equipment.

Control Circuit-The circuit that carries the electric signals directing the performance of a control device, but that does not carry the power which the device controls.

Control Coefficient-A ratio of an incremental change in a stabilized output signal to the incremental change in the control signal that causes it.

Control Deviation-The difference between the actual value of a controlled output quantity and the control quantity, divided by the control coefficient. The control deviation includes nonlinearity, calibration error and offsets.

Control Loop-A feedback circuit used to control an output signal. See also Loop

Control Range-The parameter over which the controlled signal may be adjusted and still meet the unit specifications.

Control Rate-The maximum rate at which the stabilized output can be varied as a result of control signal changes without exceeding the control deviation.

Control, Remote-Control over the stabilized output signal by means located outside or away from the power supply. May or may not be calibrated.

Control, Resolution-The smallest increment of the stabilized output signal that can be reliably repeated.

Convection-The transfer of thermal energy in a gas or liquid by currents resulting from unequal temperatures.

Convection-Cooled Power Supply-A power supply cooled exclusively from the natural motion of a gas or a liquid over the surfaces of heat dissipating elements.

Converter-A device that changes the value of a signal or quantity. Examples: DC-DC; a device that delivers dc power when energized from a dc source. Fly-Back; a type of switching power supply circuit. See also Flyback Converter. Forward; A type of switching supply circuit. See also Forward Converter

Cooling-The process of removing heat dissipated by a power supply during transformation and regulation.

Cooling: Forced air

Forced air cooling ratings may be specified in either linear feet per minute (LFM), cubic feet per minute (CFM), or pound mass per minute (lb/mm). Linear feet per minute ratings are a more valid measure of the air flow because they specify exactly where the air flows and directly relate to heat transfer. However, CFM values are usually specified. Flow measured in lb/mm is most useful when dealing with varying air densities or high altitude, and is calculated by CFM and density (lb/w). This application note explains the relationship between forced air specifications in linear feet per minute and in cubic feet per minute. This application note applies to all Astec power supplies requiring forced air cooling. To Convert from CFM to LFM and LFM to CFM given the cross sectional area: To convert from CFM to LFM and vice-versa, we need the cross section area of the power supply. This would be the actual area that the air is being blown through. The formula is CFM LFM x cross sectional area. A popular selection is 2.5" x 5.0". This corresponds to 0.0868 square feet. For any fixed cross sectional area, the relationship is linear and can be shown with a graph.

Copper Loss-Heat loss in motors, generators and transformers as the result of wire resistance. Joule's Law mathematically describes the heating effect of the flow of current as a result of losses. Sometimes called 1^2R loss.

Cord Set-An assembly of a suitable length of flexible cord provided with an attachment plug at one end and a second connector at the other.

Core-Magnetic material serving as a path for magnetic flux.

Core Loss-Power dissipated by a magnetic core due to hysteresis and eddy currents.

Core Saturation-The tendency of molecules in an iron core to orient in one direction due to the application of direct current.

Coulomb-The quantity of electricity when one ampere flows for one second, representing 6.24 x 1018 electrons. See also Current, Faraday

Coulombic Efficiency-See Ampere-Hour Efficiency

Counter EMF (CEMF)-Voltage induced in conductor moving through magnetic field which opposes source voltage. See also Electromagnetic Force (EMF)

Counter EMF Cell-A very low capacity cell used to oppose the voltage of the main battery.

Coupled Choke-See Integrated Magnetics

Coupling-The characteristic of isolated circuit elements to interact with one another. See also Coefficient of Coupling

Creepage-The movement of electrolyte onto surfaces of electrodes or other components of a cell with which it is not normally in contact.

Creepage Distance-The shortest distance separating two conductors as measured along a surface touching both conductors.

Crest Value-Maximum value of a waveform excluding transients.

Cross-Regulation-In a multiple output power supply, the percent voltage change at one output caused by the load change on another output.

Crossover Frequency-The frequency on a bode plot at which the loop gain drops to zero decibels.

Crossover Point-That point on the operating locus of a voltage/current automatic crossover power supply formed by the intersection of the voltage- stabilized and current-stabilized output lines. The resistance value (E/I) defined by this intersection is the matching impedance for the power supply, which will draw the maximum output power. See also Automatic Crossover

Crossover, Voltage/Current-Voltage/current crossover is that characteristic of a power supply that automatically converts the mode of operation from voltage regulation to current regulation (or vice versa) as required by preset limits.

Crowbar-An overvoltage protection circuit which rapidly places a low resistance shunt across the power supply output terminals if a predetermined voltage is exceeded.

Cuk Converter-A variation of the buck/boost topologies.

Current (I)-The rate of transfer of electrical energy measured in amperes. (One 'international" ampere will deposit silver from a specified silver nitrate solution at the rate of 0.00111800 grams per second. An "international" ampere, in turn, is defined as 0.99985 "absolute" amperes, one coulomb per second.)

Current Collector-An inert member of high electrical conductivity used to conduct current from or to an electrode during discharge or charge. See also Collector

Current Control-See Current Stabilization

Current Density-The current per unit active area of the surface of an electrode.

Current Fed Supply-A buck regulator with a choke in the primary.

Current Foldback-See Foldback Current Limiting

Current Limit Knee-The point on the plot of current vs. voltage of a supply at which the current starts to foldback, or limit.

Current Limiting-An electronic overload protection circuit which limits the maximum output current to a preset value. See also Output Current Limiting

Current Mode-The functioning of a power supply so as to produce a stabilized output current.

Current Sensing Resistor-A resistor placed in series with the load to develop a voltage proportional to load current.

Current Source-A power source that tends to deliver constant current.

Current Transformer-1) Instrument Transformer: Intended to have its primary winding connected in series with the conductor carrying the current to be measured or controlled. 2) Metering: Designed for use in the measurement or control of current. Its primary winding may be single turn or bus bar, and is connected in series with the load. 3) Power and Distribution Transformer: Intended to have its primary winding connected in series with the conductor carrying the current to be measured or controlled. (In window-type current transformers, the primary winding is provided by the line conductor and is not an integral part of the transformer.)

Current Stabilization-The process of controlling an output current.

Cutoff Voltage-The cell or battery voltage at which the discharge is terminated. The cutoff voltage is specified by the cell manufacturer and is generally a function of discharge rate.

Cycle-A period of time in which recurring events are completed.

Cycle Life-The number of cycles under specified conditions before a device tails to meet specified performance criteria.

Cycle Service-A duty cycle characterized by frequent and usually deep discharge-charge sequences, such as motive power applications.

Cylindrical Cell-A cell whose height is greater than its diameter. The term cylindrical is also used to describe batteries made up of cylindrical cells.

D-Variously, the symbol for diameter, drain and deuterium.

DB-Abbreviation for Decibel

DC-In text, use lower case: dc, Abbreviation for Direct Current

DC Component -The dc value of an ac wave that has an axis other than zero.

DC/DC Converter - A circuit or device that changes a dc input signal value to a different dc output signal value.

Debug - The process of detecting and correcting errors.

Decay Time - See Fall Time

Decibel - The numerical expression of the relative loudness of two signals, such as sound. The difference in decibels between two signals is ten times the common logarithm of the ratio of their powers.

Dedicated - Set aside for a special purpose.

Deep Discharge-1) Withdrawal of at least 80% of the rated capacity of a cell or battery. 2) Discharge of a battery to below the specified voltage cutoff before the battery is replaced or recharged.

Delta Connection - So connected that the windings of a three-phase transformer (or the windings for the same rated voltage of single-phase transformers associated in a three- phase bank) are connected in series to form a closed circuit.

Density-1) The ratio of mass of material to its own volume. 2) Number per unit.

Depolarization - A reduction in the polarization of an electrode.

Depolarizer - A substance or means used to prevent or decrease polarization. The term "depolarizer" is often used, albeit incorrectly, to describe the positive electrode of a primary cell.

Depth of Discharge - The ratio of the quantity of electricity (usually in ampere-hours) removed from a cell or battery on discharge to its rated capacity.

Derating - Practice of applying components or devices at a lower stress level than specified capabilities in order to reduce the occurrence of stress-related failures. Generally for power supplies, it is the reduction in output power at elevated temperatures.

Design Life - Expected length of time of acceptable performance under specified conditions.

Destructive Testing - A test to determine the point at which a device catastrophically fails.

Diaphragm - A porous or permeable means for separating the positive and negative electrode compartments of a galvanic cell and preventing admixture of catholyte and anolyte.

Dielectric - An insulating material between conductors.

Dielectric Constant (K) - For a given dielectric material, the ratio of the value of a capacitor using that material to the value of an equivalent capacitor using a standard dielectric such as dry air or a vacuum.

Dielectric Withstand Voltage - Voltage an insulating material will withstand before flashover or puncture. See also Hi-Pot Test, Isolation

Differential Mode Noise - The component of noise, excluding common-mode noise, that is measured between two lines with respect to a common reference point. The value is the difference of the noise components on the two lines.

Differential Voltage - The difference in voltages at two points as measured with respect to a common reference.

Diffusion - The movement of species under the influence of a concentration gradient.

Diode - A two-element device containing a cathode and an anode that permits flow in one direction and blocks flow from the other.

Direct Current (DC) - Flow of electrons in one direction. In text, use lower case: dc.

Direct Plug-In - A device that engages a receptacle without a cord.

Discharge - The conversion of the chemical energy of a cell or battery into electrical energy and withdrawal of the electrical energy into a load.

Discharge Rate - The rate, usually expressed in amperes, at which electrical current is taken from the cell or battery.

Distortion, Output - See Harmonic Distortion

Distortion, Source - The departure of the source ac waveform from sinusoidal form. Some types of power supplies induce distortion in their source by imposing a nonlinear load impedance on the nonzero impedance of the source line.

Domain Theory - Theory concerning magnetism, assuming that atomic magnets produced by movement of planetary electrons around a nucleus have a strong tendency to line up together in groups. These groups are called domains.

Double Cell - See Twin Cell

Double Insulation - An insulation system comprised of basic insulation and supplementary insulation, with the two insulations physically separated and so arranged that they are not simultaneously subjected to the same deteriorating influences (temperature, contaminants, and the like) to the same degree.

Double Layer - The region in the vicinity of an electrode-electrolyte interface where the concentration of mobile ionic species has been changed to values differing from the bulk equilibrium value by the potential difference across the interface.

Double-Layer Capacitance - The capacitance of the double layer.

Double Plate - A pocket plate design where the plate consists of two plate blanks clamped together in the same frame.

Drain - With regard to cells or batteries, the withdrawal of current.

Drift - A change in output over a period of time independent of input, environment or load. For power supplies, the change in DC output as a function of time at constant line voltage, load, and ambient temperature. Normally specified for an eight hour period after a half hour warm-up.

Driver - A current amplifier used for control of another device or circuit.

Droop - The decrease in amplitude of a flat top square pulse; a form of square pulse distortion.

Dry Battery - A battery in which the electrolyte is immobilized, being either in the form of a paste or gel or absorbed in the separator material. See Dry-Charged Battery

Dry Cell - A cell with immobilized electrolyte. The term "dry cell" is often used to describe the Leclanche cell.

Dry-Charged Battery - A battery in which the electrodes are in a charged state, ready to be activated by the addition of the electrolyte.

Duplex Electrode or Plate - See Bipolar Plate

Duration - The time interval between the first and last instants at which the instantaneous amplitude reaches a stated fraction of the peak pulse amplitude.

Duty Cycle 1) The ratio of time on to time off in a recurring event. 2) The operating regime of a cell or battery including factors such as charge and discharge rates, depth of discharge, cycle length a length of time in the standby mode.

Dynamic Load - A load that rapidly changes from one level to another. To be properly specified, both the total change and the rate of change must be stated.

E-The symbol for Voltage (electrode potential).

E°-Variously, symbol for Electrode Potential, Standard Electrode Potential

e? - Symbol for Electron

E/I-Resistance value. See Crossover Point

EIA-Abbreviation for Electronic Industries Association

EMF-Abbreviation for Electromotive Force

EMI-Abbreviation for Electromagnetic Interference

EMI Filter-A circuit composed of reactive and resistive components for the attenuation of radio frequency components being emitted from a power supply. See also EMI

EMI Filtering-Process or network of circuit elements to reduce electromagnetic interference emitted from or received by an electronic device. See also EMI

ESD-Abbreviation for Electrostatic Discharge

ESL-Abbreviation for Equivalent Series Inductance

ESR-Abbreviation for Equivalent Series Resistance

Earth-An electrical connection to the earth frequently using a grid or rod(s). See also Ground

Eddy Currents-A circulating current induced in a conducting material by a varying magnetic field.

Eddy Current Loss-Energy loss resulting from eddy currents circulating in a magnetic material.

Edge Connector-Female receptacle that mates with contacts on the edge of a printed circuit board.

Edge Insulator-Material that insulates the plate edges from each other and/or from the container sidewalls of a cell or battery.

Effective Value-The value of a waveform that has the equivalent heating effect of a direct current. For sine waves, the value is .707 x Peak Value; for non-sinusoidal waveforms, the Effective Value = RMS (Root Mean Square) Value.

Efficiency-1) The ratio of total output power to total input power, expressed as a percentage, under specified conditions. For power supplies efficiency is generally measured at full load with nominal line conditions. 2) The ratio of the output of a secondary cell or battery on discharge to the input required to restore it to the initial state of charge under specified conditions. See also Ampere-Hour Efficiency, Voltage Efficiency and Watt-hour Efficiency

Electrical Double Layer-See Double Layer

Electricity-Property of fundamental particles of matter that have a force field associated with them to gain or lose electrons.

Electrochemical Couple-The system of active materials within a cell that provides electrical energy through an electrochemical reaction.

Electrochemical Equivalent-Weight of a substance that is deposited at an electrode when the quantity of electricity which is passed is one coulomb. See also Faraday

Electrochemical Series-A classification of the elements according to the values of the standard potentials of specified electrochemical reactions.

Electrode-1) The site, area, location or material at which electrochemical processes take place. 2) A conducting element that performs one or more of the functions of emitting, collecting or controlling the movements of electrons, holes or ions in an electron tube or semiconductor device.

Electrode Potential (Eo)-The voltage between an electrode and its surrounding elements. See also Standard Electrode Potential

Electrolysis-The electrochemical decomposition of water or other materials from the electrolyte.

Electrolyte-The ion-conducting medium within an electrochemical cell that provides the ion transport mechanism between positive and negative electrodes.

Electrolytic Capacitor-A device that contains two electrodes separated by an electrolyte.

Electrolytic Cell-A cell in which electrochemical reactions are caused by supplying electrical energy or which supplies electrical energy as a result of electrochemical reactions; if the first case only is applicable, the cell is an electrolysis cell; if the second case only, the cell is a galvanic cell.

Electromagnet-A device consisting of a ferromagnetic core and a coil that produces appreciable magnetic effects only when an electric current exists in the coil.

Electromagnetic Interference (EMI) 1)-Any electronic disturbance that interrupts, obstructs, or otherwise impairs the performance of electronic equipment. For power supplies, unwanted energy, generally emitted from switching power supplies, which may be conducted or radiated.

Electromotive Force (EMF)-1) Force that causes free electrons to move in a conductor. Unit of measurement is the volt. 2) The standard potential of a specified electrochemical action.

Electromotive Series-See Electrochemical Series

Electron (e?)-Negatively charged particle.

Electron Volt-A measure of energy. The energy acquired by an electron passing through a potential of one volt.

Electronic Industries Association (EIA)-Trade group headquartered in Washington, DC.

Electronic Load-A test instrument designed to draw various and specified amounts of current or power from a power source.

Electrostatic Discharge (ESD)-The flow of current that results when objects having a static charge come into a close enough proximity to discharge.

Electrostatic Field-Electric field around a charged body.

Electrostatic Shield-A conductive screen that shunts induced electrical energy to ground. See also Faraday Shield.

Element-1) A distinct functioning device in an electrical circuit. 2) The negative and positive electrodes together with the separators of single cell. It is used almost exclusively in describing lead-acid cell and batteries.

Enclosure-A housing for an electronic device designed to separate and protect both the internal componentry and the outside environment.

End Voltage-The prescribed voltage at which the discharge (or charge, if end-of-charge voltage) of a cell or battery may be considered complete. See also Cutoff Voltage

Energy-Power output capability in a closed circuit as a function of time.

Energy Density-The ratio of the energy available from a cell or battery to its volume (WhIL) or weight (Wh/kg).

Equalization-The process of restoring all cells in a battery to an equal state of charge. Also referred to as Equalization Charge

Equalization Charge-See Equalization

Equalizing Connector-A device which connects points of the same theoretical potential in a battery to ensure that there will be no potential difference between these points.

Equivalent Circuit-An electrical circuit that models the fundamental properties of a device or circuit.

Equivalent Load-An electrical circuit that models the fundamental properties of a load.

Equivalent Series Inductance (ESL)-The amount of inductance in series with an ideal capacitor which exactly duplicates the performance of a real capacitor.

Equivalent Series Resistance (ESR)-The amount of resistance in series with an ideal capacitor which exactly duplicates the performance of a real capacitor.

Equilibrium Electrode Potential-The difference in potential between an electrode and an electrolyte when they are in equilibrium for the electrode reaction which determines the electrode potential.

Error Amplifier-An operational amplifier, or differential amplifier, in a control loop that produces an error signal whenever a sensed output differs from a reference voltage.

Error Signal-The output voltage of an error amplifier produced by the difference between the reference and the input signal times the gain of the amplifier.

Error Voltage-The output voltage of the error amplifier in a control loop.

ESR-equivalent series resistance

Exchange Current-Under equilibrium conditions, the forward and backward currents of an electrochemical process are equal. This equilibrium current is defined as the exchange current.

Excitation Current (No-Load Current) - The current which flows in any winding used to excite the transformer when all other windings are open-circuited.

Exciting Current-See Magnetizing Current

Explosion Proof-Encased in an enclosure capable of withstanding without damage, the explosion within it of a specified gas or vapor, and capable of preventing a specified gas or vapor surrounding the enclosure from ignition due to sparks, flashes or an explosion of the specified gas or vapor within it.

°F-Abbreviation for degrees Fahrenheit.

Fe-Symbol for iron.

FEP-Abbreviation for Functional End Point

FET-Abbreviation for Field Effect Transistor

FCC-Abbreviation for Federal Communications Commission

Failure Mode-The way in which a device has ceased to meet specified minimum requirements.

Fall Time-The time required for a pulse to decrease from 90 percent to 10 percent of its maximum positive (negative) amplitude.

Fan Cooled-A method of forced-air cooling used to maintain design temperatures.

Farad-Unit of measurement of capacitance. A capacitor has a capacitance of one farad when a charge of one coulomb raises its potential one volt: C = QIE

Faraday-One gram equivalent weight of matter is chemically altered at each electrode of a cell for (approximately) each 96,500 international coulombs, or one Faraday, of electricity passed through the electrolyte. See also Coulomb

Faraday Cage-A grounded metallic screen completely surrounding a space to protect it from external electrostatic influence.

Faraday Shield-An electrostatic shield between input and output windings of a transformer. This can be used to reduce coupling capacitance which in turn reduces output common mode noise. See also Electrostatic Shield

Fault Mode Input Current-Input current drawn by a power supply with the output short circuited.

Fault Tolerant-A high level of redundancy to provide continued operation following specified failure

Faure Plate-See Pasted Plate

Federal Communications Commission (FCC)-A board of commissioners appointed by the President having the power to regulate all interstate and foreign electrical communications Systems and emissions originating in the United States.

Feedback-The process of returning part of the output signal of a system to its input.

Feed Forward-A control technique whereby the line regulation of a power supply is improved by directly sensing the input voltage.

Feed Through-A plated-through hole in a printed circuit board which electrically connects a trace a top of the beard with a trace on the bottom side.

Ferrite-A ceramic material that exhibits low loss at high frequencies, and which contains iron oxide mixed (with oxides or carbonates of one or more metals such as manganese, zinc, nickel or magnesium.

Ferroresonance-The property of a transformer design in which the transformer contains two separate magnetic paths with limited coupling between them. The output contains a resonating tank circuit and draws power from the primary to replace power delivered to the load.

Ferroresonant Transformer-An AC regulator designed to operate at a given input frequency and which uses a resonant circuit to achieve regulation. Although the regulation is imprecise, the device itself is simple, very rugged and reliable. Typically operating at 50Hz or 60Hz, these "iron-core" (actually laminated silicon steel) transformers incorporate a capacitor in one of the secondaries that resonates with the inductance of the transformer. An excessively high input AC voltage which would otherwise result in excessive secondary voltage will cause the resonant circuit voltage to ring high enough to locally saturate the transformer core. Once saturated, the primary winding magnetic flux no longer links the secondary winding and the secondary voltage is limited.

Field Effect Transistor (FET)-Transistor in which the resistance of the current path from source to drain is modulated by applying a transverse electric field between two electrodes. See also Junction Field Effect Transistor, Metal Oxide, Semiconductor Field Effect Transistor

Filter-One or more discrete components positioned in a circuit to attenuate signal energy in a specified band of frequencies.

Final Charging Voltage-The voltage which a battery reaches at the end of a charging operation. In the case of constant voltage charging, this voltage is determined by the setting of the charging equipment.

Flag Signal-See Status Signals

Flame Arresting Vent-A special design of a wet cell vent which provides protection against internal explosion when the cell or battery is exposed to a naked flame or external spark.

Flash Current-See Short-Circuit Current

Flat Plate Cell-A cell fabricated with rectangular flat-plate electrodes. See also Pocket Plate

Float Charge-A method of maintaining a cell or battery in a charged condition by continuous, long-term, constant-voltage charging, at a level sufficient to balance self-discharge.

Float Voltage-The voltage required for retaining a charged battery in a fully charged condition. This is also known as float charging.

Floating Output-ungrounded output of a power supply where either output terminal may be referenced to another specified voltage.

Flooded Cell-A cell design which incorporates an excess amount of electrolyte.

Flux -Total number of lines of magnetic force.

Flux Density (B)-Number of lines of flux per cross-sectional area of a magnetic circuit expressed in Gauss.

Flyback Converter-A power supply switching circuit which normally uses a single transistor. During the first half of the switching cycle the transistor is on and energy is stored in a transformer primary; during the second half of the switching cycle this energy is transferred to the transformer secondary and the load.

Foldback Current Limiting-A power supply output protection circuit whereby the output current decreases with increasing overload, reaching a minimum at short circuit. This minimizes internal power dissipation under overload conditions. Foldback current limiting is normally used with linear regulators and is not necessary to protect switching regulators. However, many switchers incorporate foldback to protect the load form excessive current.

Forced Discharge-Discharging a cell or battery, with external battery or power source, below zero volts into voltage reversal.

Formation-Electrochemical processing of a battery plate or electrode between manufacture and first discharge which transforms the active materials into their usable form.

Forward Converter-A power supply switching circuit that transfers energy to the transformer secondary when the switching transistor is on

Free Wheel Diode-A diode in a pulse-width modulated switching power supply that provides a conduction path for the counter electromotive force of an output choke.

Frequency -Number of cycles per second measured in hertz.

Frequency Converter-Power conversion equipment that transforms ac electric power from one frequency to another. Frequency converters are often used to electronically convert a 60Hz source to a 50Hz source and vice versa for system testing.

Frequency Modulation-The variation in frequency about a specified value caused by a change in a control signal.

Frequency Response-Rating of a device indicating its ability to operate over a specified range of frequencies, e.g., gain-frequency characteristics of an amplifier.

Fuel Cell-A cell in which the active materials are continuously supplied and the reaction products continuously removed.

Full-Bridge Converter-A power switching circuit in which four power switching devices are connected in a bridge configuration to drive a transformer primary.

Full-Bridge Rectifier-A rectifier circuit that employs four diodes per phase.

Full-Wave Rectifier-Rectifier circuit that produces a dc output for each half cycle of applied alternating current.

Functional End Point (FEP)-Voltage below which battery-operated equipment will not function properly.

Fuse-Safety protective device that permanently opens an electric circuit when overloaded. See also Over-current Device, Overcurrent Protective Device

G-Variously, the symbol for gram conductance

Gain-Ratio of an output signal to an input signal. See also Closed Loop Gain, Gain Margin, Open Loop Gain

Gain Margin-The gain of a control loop at the frequency for which there is 360 degrees of phase shift around the control loop.

Galvanic-Pertaining to the flow of electrons due to chemical action.

Galvanic Cell-An electrolytic cell that converts chemical energy into electrical energy by electrochemical action.

Gap-A non-magnetic segment in the magnetic path in a transformer or choke.

Gassing-The evolution of gas from one or more of the electrodes in a cell. Gassing commonly results from local action (self-discharge) or from the electrolysis of water in the electrolyte during charging.

Gate-1) A device or element that has the ability to block or pass a signal. 2) A device having one output channel and two or more input channels that performs a logic function. 3) A control electrode in a semiconductor device such as a triac, or FET.

Gauss-Measure of flux density in Maxwells per square centimeter of cross- sectional area. One gauss is iC-^{4} Tesla.

Gilbert-The centimeter-gram-second unit of magnetomotive force.

Glitch-1) An undesired transient voltage spike occurring on a signal. 2) A minor technical problem arising in electrical equipment.

Grid-1) In batteries, a framework for a plate or electrode which supports or retains the active materials and acts as a current collector. 2) In vacuum tubes, an element used to control the flow of electrons. 3) A network of equally spaced parallel lines, one set spaced perpendicular to the other. See also Power Grid

Ground-A conducting connection, whether intentional or accidental, by which an electric circuit or equipment is connected to earth, or to some conducting body that serves in place of earth. (National Electric Code)

Ground Bus-A bus to which individual grounds in a system are attached and that in turn is grounded at one or more points

Ground Grid-Interconnected bare conductors arranged in a pattern over a specified area, laid out on or below the earth's surface.

Ground Loop-A condition that causes undesirable voltage levels when two or more circuits share a common electrical return or ground lines.

Ground Rod-A metallic rod, commonly copper clad, driven into the earth to serve as a ground terminal.

Grounded-Connected to or in contact with earth or connected to some extended conductive body which serves instead of the earth.

Grounding-A permanent and continuous conductive path to earth with sufficient ampacity to carry any fault current liable to be imposed on it, and of a sufficiently low impedance to limit the voltage rise above ground.

h-Variously the abbreviation for height, hour

H-Variously, the symbol *for* Henry, Magnetic Field Strength, or Magnetomotive Force.

Hz-Abbreviation for Hertz

Half-Bridge Converter-A switching power supply design in which two power switching devices are used to drive the transformer primary. See also Bridge Rectifier

Half-Cell-An electrode (either the anode or cathode) immersed in a suitable electrolyte.

Half-Wave Rectifier-A circuit element, such as a diode, that rectifies only one-half the input ac wave to produce a pulsating dc output.

Harmonic Distortion-The distortion of a sinusoidal wave characterized by the presence of harmonics of the fundamental frequency. Percent Harmonic Distortion is an appropriate figure of merit and is defined as the ratio (in percent) of the square root of the sum of the squares of all rms harmonic voltages (or currents) to the fundamental.

Headroom-The difference between the bulk voltage and the output voltage in a linear series pass regulator. See also Differential Voltage

Heat Pipe-A device using a fluid in a sealed capillary network to conduct thermal energy away from a heat source.

Heat Sink-The medium through which thermal energy is dissipated.

Henry (H)-Unit of measurement of inductance. A coil has one henry of inductance if an EMF of one volt is induced when current through an inductor is changing at rate of one ampere per second.

Hertz (Hz)-The SI unit of measurement for frequency, named in honor of Heinrich Hertz who discovered radio waves. One hertz equals one cycle per second.

Hexfet-Trade name of International Rectifier Corporation for a power Mosfet having an hexagonal geometry.

Hipot Test (High Potential Test)-A test performed by applying a high voltage for a specified time to two isolated points in a device to determine adequacy of insulating materials. For power supplies, it is often a test to determine if the breakdown voltage of a transformer or power supply exceeds the minimum requirement.

Hiccup-A transient condition that momentarily confuses a control loop.

Hiccup mode - A protection mode used in some switching power supplies that shuts down the supply and then attempts a periodic restart. When the fault is cleared, the supply will automatically start. The sound resulting from the fault sounds like a hiccup.

High Line-Highest specified input operating voltage.

High Voltage Power Supply - A power supply with an output voltage of 100V or more. High Voltage power supplies often use air as the primary dielectric medium, avoiding the weight and serviceability problems associated with other dielectrics. Most high voltage supplies are of two types. The first type is simply a step-up power transformer with rectified and filtered (but otherwise unregulated) high voltage secondary. This is the most straightforward, efficient, and lowest cost power supply because of its simplicity. The second basic type is essentially a switcher with a string of voltage doublers that provide the high voltage output. As a switcher, the second type enjoys heat, weight and size advantages over the first type. By employing pulse width modulation, the switcher's output can be regulated. On the negative side, the

switcher includes an input energy storage cap that sustains the high voltage output even if the AC power is cut off. This can result in a safety hazard. Product selection requires extra attention to the design features and construction techniques that contribute to safety and protection against failures. Pulse-width modulation and full-wave/symmetrical cascade high voltage multipliers, with surge limiting resistors, contribute to high efficiency and reliability.

Holding Time-See Holdup Time

Holdup Time-The time under worst case conditions during which a power supply's output voltage remains within specified limits following the loss or removal of input power. Sometimes called Holding Time or Ride-Through.

Holy Point Ground-See Single Point Ground

Hourly Rate-A discharge rate, in amperes, of a cell or battery which will deliver the specified hours of service to a given end voltage. See also C Rate

Hum-Audible noise from a magnetic device due to magnetostrictive activity of the core at twice line frequency.

Hybrid-The combination of different component technologies on a single substrate.

Hybrid Supplies-A power supply that combines two or more different regulation techniques, such as ferroresonant and linear or switching and linear, or one that takes advantage of hybrid technology. See also Hybrid

Hydrogen Electrode-An electrode of platinized platinum saturated by a stream of pure hydrogen.

Hydrogen Overvoltage-The activation overvoltage for hydrogen discharge.

Hysteresis-1) The property of a magnetic substance that causes magnetization to lag behind the force that produces it. 2) A variable input voltage threshold determined by the logic state of the output of the circuit.

Hysteresis Loop-A closed curve that shows, for each value of magnetizing force, two values of the magnetic flux density in a cyclically magnetized material: one when the magnetizing force is increasing, the other when it is decreasing.

Hysteresis Loss-Energy dissipated due to molecular friction as domains move through cycles of magnetization.

I-Symbol for electric Current

IC-Abbreviation for Integrated Circuit

IEC-Abbreviation for International Electrotechnical Commission.

IEEE-Abbreviation for Institute of Electrical and Electronics Engineers.

IR Drop-See Voltage Drop

I2R Loss-See Copper Loss

ISO9000 - The International Standards Organization quality assurance system is gaining popularity around the world. ISO9000 is the overall standard. ISO9001 is the most stringent standard, which requires a complete quality system including engineering and design, resource planning, documentation, installation and service. ISO9002 contains quality requirements for product production and installation. ISO9003 pertains only to inspection and testing. ISO9004 gives detailed directions for implementing each of the ISO9000 standards.

Impedance (Z)-Total resistance to flow of an alternating current as a result of resistance and reactance. Also the ratio of voltage to current in AC circuits, containing both resistance and reactance terms, usually expressed as ohms.

Impedance Matching (Z Match)-The connection across a source impedance of a matching impedance to allow optimum undistorted energy transfer.

Induced Current-Current that flows as a result of an Induced EMF (Electromotive Force).

Induced EMF-Voltage induced in a conductor in a varying magnetic field.

Inductance (L) - inherent reactive property, measured in henrys, of an electric circuit or circuit element that opposes a change in current flow. Hence, inductance causes current changes to lag behind voltage changes. See also Henry

Inductive Circuit-Circuit in which an EMF is produced by a changing current.

Inductive Reactance (XL)-Opposition to a changing current as a result of inductance:

XL= 2(pi)FL

Inductor-A coil or component with the properties of inductance.

Initial (Closed-Circuit) Voltage-The on-load voltage at the beginning of a discharge.

Inner Helmholtz Plane-The plane of closest approach of ions in solution. It corresponds to the plane which contains the contact-absorbed ions and the innermost layer of water molecules.

Input AC - The sinewave input voltage normally specified in volts RMS. An input waveform that is not sinusoidal, such as a square wave or distorted sinewave wave (from a UPS) can affect power supply operation and must be defined. Contact Professor Power for information on derating of standard catalog power supplies for voltage, frequency, and wave shape variations beyond those specified in the catalog.

Input DC - The DC level normally specified in volts. Lower DC voltages can cause heating and limit output power. Contact Professor Power for information on derating at low input voltage.

Input Reflected Ripple Current - (DC/DC converters) The AC ripple current measured at the input and generated by the switching action of the converter. Low ESR (Effective Series Resistance) input capacitors are used to reduce the input ripple voltage caused by the ripple current.

Input Impedance-The impedance of the input terminals of a circuit or device with the input disconnected.

Input Line Filter-A low-pass or band-reject filter at the input of a power supply which reduces line noise fed to the supply or fed onto the input power lines. This filter may be external to the power supply.

Input Pi Filter-See Pi Filter

Input Surge-See Inrush Current

Input Voltage Range-The range of input voltage values for which a power supply or device operates within specified limits.

Inrush Current-The peak instantaneous input current drawn at turn on by a power supply.

Inrush Current Limiting-The characteristic of a circuit that limits inrush current when a power supply is turned on.

Instantaneous Value-The measured value of a signal at a given moment in time.

Institute of Electrical and Electronics Engineers (IEEE)-A professional organization. The IEEE develops standards on definitions, test methods, symbols, units and safety in the field of electrical science and engineering.

Insulation-Non-conductive materials used to separate electric circuits.

Insulation Resistance-The resistance of an insulating material to the flow of current resulting from an impressed dc voltage. Usually measured in megohms.

Integrated Circuit (IC)-A combination of active and passive circuit elements contained on a single semiconductor substrate.

Integrated Magnetics-A magnetic component in which separate circuit elements share a common core segment.

Interleaved Transformer Windings-The segmentation of portions of the same winding by another to improve or control inductive coupling.

Intermittent Duty-A requirement of service that demands operation for definitely specified alternate intervals of: a) Load and no load; b) Load and rest; or c) Load, no load and rest. See also Continuous Duty

Intermittent Test-A test during which a power source is subjected to specified alternate periods of loading and rest.

Internal Impedance-The impedance exhibited by a circuit element or component.

Internal Resistance-1) The resistance exhibited by a circuit element or component. 2) The opposition or resistance to the flow of an electric current within a cell or battery; the sum of the ionic and electronic resistances of the cell components.

Internal Resistance (Apparent)-Quotient of the difference of voltage across battery terminals to the corresponding difference of current. It should be observed that the internal resistance is not constant but varies with state of charge, temperature and the testing method.

International Electrotechnical Commission (IEC)-Headquartered in Geneva, Switzerland, writes and distributes recommended standards on electrical products and components. The recommendations include references to safety and performance. The IEC does not perform any testing; this function is left to the national testing agencies. National standards are frequently based on IEC publications.

Inverter-1) A device that changes dc power into ac power. 2) A circuit, circuit element or device that inverts the input signal.

Iron Core-A general class of cores that contain iron. Sometimes used to refer to cores made only from steel laminations. See also Core, Ferrite, Powdered Iron Core

Iron Poisoning-In nickel alkaline cells a process by which the nickel electrode performance is impaired owing to the presence of excessive amounts of iron species in the nickel active material.

Isolation The electrical separation between input and output of a power supply by means of the power transformer. The isolation resistance (normally in megaohms) and the isolation capacitance (normally in picofarads) are generally specified and are a function of materials and spacings employed throughout the power supply.

Isolation Transformer-A transformer with a one-to-one turns ratio. See also Step-Down Transformer, Step-Up Transformer, Transformer

Isolation Voltage-The maximum ac or dc specified voltage that may be continuously applied between isolated circuits.

J-Symbol for Joule

JDEC-Abbreviation for Joint Electronic Device Engineering Council

JFET-Abbreviation for Junction Field Effect Transistor. See also Field Effect Transistor

Joint Electronic Device Engineering Council (JDEC)-A group within the Electronic Industries Association, originally formed in conjunction with NEMA. No longer affiliated with NEMA, the EIA group has retained the JDEC acronym.

Joule (J)-Unit of energy equal to one watt-second.

Junction Field Effect Transistor (JFET)-A low power semiconductor having a conductive channel whose resistance is controlled by the reverse voltage on the gate channel junction.

K-Variously, the symbol for coefficient of coupling, potassium, and Kelvin.

kW-Symbol for kilowatt

kWh-Symbol for kilowatt-hour.

Kelvin (K)-1) Unit of temperature in the International System of Units (SI) equal to the fraction 1/273.16 of the thermodynamic temperature of the triple point of water. The Kelvin temperature scale uses Celsius degrees with the scale shifted so 0 K is at

absolute zero. Add 273.16 to any Celsius value to obtain the corresponding value in Kelvins. 2) A technique using 4 terminals to isolate current carrying leads from voltage measuring leads.

Kirchoff's Current Law-At any junction of conductors in a circuit, the algebraic sum of the currents is zero.

Kirchoff's Voltage Law-In a circuit, the algebraic sum of voltages around the circuit is equal to zero.

L-Variously, the symbol for Inductance and length, and the abbreviation for liter.

L-C Filter-A low pass filter that consists of an inductance (L) and a capacitance (C). Also known as an averaging filter/

Li-Symbol for lithium.

LED-Symbol for Light-Emitting Diode

L-Section-Filter consisting of at least two components, one of which is reactive (inductive or capacitate) connected in an "L" configuration.

Lag Network-Resistance- reactance components arranged to control phase-gain roll-off versus frequency The main effect is to reduce gain at low frequencies so the slope of the remaining rolloff can be relatively more gentle.

Lagging Angle- The angle that current lags voltage in inductive circuit.

Laminations -Thin sheets of coated steel or alloys used in cores of transformers, motors and generators.

Land-A terminal point on a printed circuit board.

Latch-A logic circuit that, once set, maintains the output at some fixed state until reset.

Latch Up-A part of the control circuit for a power supply that goes into a latched condition. Latching Relay-A relay that mechanically latches until mechanically or electrically reset.

Layer Winding-The method of winding a transformer or choke whereby conductors are layered one top of another, commonly separated by an insulating layer.

Lead-Acid Cell-Secondary cell which uses lead peroxide and sponge lead for plates, and sulfuric acid water for electrolyte.

Lead Network-Resistance-reactance components arranged to control phase-gain roll-off versus frequency, typically used to assure the dynamic stability of a power-supply's comparison amplifier. The effect is to introduce a phase lead at higher frequencies, near unity gain frequency.

Lead Resistance-DC resistance in the leads of a circuit element or device.

Leading Angle-Angle current leads voltage in capacitive circuit.

Leakage Current-1) The ac or dc current flowing from input to output and/or chassis of an isolated device at a specified voltage. 2) The reverse current in semiconductor junctions.

Leakage Flux-Magnetic lines of force that go beyond their intended path and do not serve their intended purpose.

Leakage Inductance-Self inductance in a transformer caused by leakage flux.

Leclanche-A Carbon Zinc battery with a slightly acidic electrolyte consisting of ammonium chloride and zinc chloride in water.

Light-Emitting Diode (LED)-A semiconductor device that radiates in the visible spectrum when energized by an electric current. Color is determined by the electroluminescent characteristics of the materials used in fabricating the devices, and by the addition of various dopants. For example, copper-doped zinc sulphide emits light in the 555 nanometer (green) range, the area of peak sensitivity of the human eye.

Life Test-A test in which a device is subjected to actual or accelerated use to obtain an estimate of life expectancy.

Line-1) Medium for transmission of electricity between circuits or devices. 2) The voltage across a power transmission line. See also High Line, Low Line

Line Conditioner-A circuit or device designed to improve the quality of an ac line.

Line Effect-See Line Regulation

Line Regulation . The change in value of DC output voltage resulting from a change in AC input voltage over a specified range, or from low line to high line or from high line to low line. Normally specified as the + or - change from the nominal DC output voltage.

Line Frequency Regulation-The percentage change in output for a specified change in the line frequency at specified load values, with all other factors constant.

Line Regulator-Power conversion equipment that regulates and/or changes the voltage of incoming power.

Linear-1) In a straight line. 2) A mathematical relationship in which quantities vary in direct proportion to one another, the result of which, when plotted, forms a straight line.

Linear Pass-See Series Pass

Linear Regulation-A regulation technique wherein the control device, such as a transistor, is placed in series or parallel with the load. The output voltage is regulated by varying the effective resistance of the control device to dissipate the power resulting from the difference between input and output voltage time the current. See also Linear Power Supply

Linear Regulator-A power transistor or device connected in series with the load of a constant voltage power supply in such a way that the feedback to the series regulator changes its voltage drop as required to maintain a constant dc output.

Linear Power Supply-An electronic power supply employing linear regulation techniques. "Linears" can provide fast transient response, very precise output regulation, very low output PARD (noise), and excellent isolation from the source voltage. They are also larger (about 10X) heavier (about 10X) and generate more heat (about 5X) compared to an equivalent switcher. Linear supplies typically utilize a 50Hz - 60Hz transformer to provide an isolated lower unregulated secondary voltage that is then regulated with a "linear pass device". The pass device is usually a transistor controlled with a local feedback loop.

Linearity-1) The ideal property wherein the change in the value of one quantity is directly proportional to the change in the value of another quantity, the result of which, when plotted on graph, forms a straight line. 2) Commonly used in reference to Linearity Error

Linearity Error-The deviation of the output quantity from a specified reference line.

Line Transient-A perturbation outside the specified operating range of an input or supply voltage.

Litz Wire-Wire that consists of a number of separately insulated strands woven together so each strand successively takes up all possible positions in the cross section of the entire conductor to reduce skin effect and thereby reduce RF resistance.

Load-Capacitance, resistance, inductance or any combination thereof, which, when connected across a circuit determines current flow and power used.

Load Decoupling-The practice of placing filter components at the load to attentuate noise.

Load Effect-See Load Regulation

Load Impedance-The complex resistance to the flow of current posed by a load that exhibits both the reactive and resistive characteristics.

Load Line Shaper-See Snubber

Load Regulation-1) Static: The change in output voltage as the load is changed from specified minimum to maximum and maximum to minimum, with all other factors held constant. 2) Dynamic: The change in output voltage expressed as a percent for a given step change in load current. Initial and final current values and the rates of change must be specified. The rate of change shall be expressed as current/unit of time, e.g., 20 amperes A/u second. The dynamic regulation is expressed as a +/- percent for a worst case peak-to-peak deviation for dc supplies, and worst case rms deviation for ac supplies.

Load-Tap-Changing Transformer: A transformer used to vary the voltage, or phase angle, or both, or a regulated circuit in steps by means of a device that connects different taps of tapped winding(s) without interrupting the load.

Load Transient Overshoot-See Overshoot

Load Transient Response Time-See Transient Recovery Time

Local Action-Chemical reactions within a cell that convert the active materials to a discharged state without supplying energy through the battery terminals (self-discharge).

Local Control-Control over the stabilized output signal by means located within or on the power supply. May or may not be calibrated.

Local Sensing-Using the power supply output voltage terminals as the error-sensing points to provide feedback to the voltage regulator.

Logic Ground-Common return or reference point for logic signals.

Logic High-A voltage representing a logic value of one (1) in positive logic.

Logic Inhibit/Enable-A referenced or isolated logic signal that turns a power supply output off or on.

Logic Low-A voltage representing a logic value of zero (0) in positive logic.

Long-term Stability-The output voltage change of a power supply, in percent, due to time only, with all other factors held constant. Long-term stability is a function of component aging.

Loop-The path used to circulate a signal. See also Closed Loop, Control Loop, Open Loop

Loop Gain-The ratio of the values of a given signal from one point to another in a loop. See also Gain

Loop Response-The speed with which a loop corrects for specified changes in line or load.

Loop Stability-A term referencing the stability of a loop as measured against some criteria, e.g., phase margin and gain margin.

Low Line-Lowest specified input operating voltage.

Luggin Capillary-The salt bridge from a reference electrode to a cell solution often has a restricted (capillary) junction between the bridge and the cell solution. The restriction, which is often situated close to the working electrode, is called a Luggin capillary.

M-Symbol tar Mutual Inductance

MHO-Unit of measurement of Conductance.

MOSFET-Abbreviation for Metal Oxide Semiconductor Field Effect Transistor

MPP-Abbreviation for Molypermalloy Powder

MTBF-Abbreviation for Mean Time Between Failure

MTTR--Abbreviation for Mean Time to Repair

MX-Abbreviation for Maxwell

Magnetic Amplifier-Transformer type device employing a control circuit to vary the magnetic core saturation, thus varying the output voltage of the amplifier.

Magnetic Field Strength (H)-See Magnetomotive Force

Magnetic Flux -Total number of lines of magnetic force. See also Flux

Magnetic Flux Density-The number of lines of flux per cross-sectional area of a magnetic circuit expressed in Gauss or Tesla. Sometimes referred to as Magnetic Induction.

Magnetic Gap-See Air Gap

Magnetic Induction-The use of a magnetic field to generate currents or voltages in a conductor sometimes referred to as Magnetic Flux Density.

Magnetizing Current-The no-load current in the transformer primary winding that is required to magnetize the core. Sometimes called exciting or excitation current.

Magnetomotive Force (H)-The magnetizing force around a magnetic circuit. When electrically induced, magnetomotive force is proportional to (and can be measured in) ampere-turns (SI) or gilberts (cgs).

Sometimes known as Magnetic Field Strength.

Maintenance-Free Battery-A secondary battery which does not require periodic 'topping up" to maintain electrolyte volume.

Margining-The ability to temporarily shift output voltage by a specified amount (often +/- 5%) for system testing.

Master/Slave Operation - Interconnection of two or more regulated supplies in which one (the master) controls the others (the slaves).

Maximum Load-1) The highest allowable output rating specified for any or all outputs of a power supply under specified conditions including duty cycle, period and amplitude. 2) The highest specified output power rating of a supply specified under worst case conditions.

Maximum Power Transfer--Condition that exists when resistance of load equals internal resistance of source.

Maxwell (MX)-The cgs unit of magnetic flux equal to 1 G/cm^2, or to one line of magnetic force. The SI unit for magnetic flux, the weber, is preferred. One weber equals 108 maxwells.

Mean Time Between Failure (MTBF)-The average length of time between system failures, exclusive of infant mortality and rated end-of-life. An established method of calculating MTBF is described in Mil Handbook 217.

Mean Time to Repair (MTTR)-The average time required to repair a product.

Mechanical Recharging-Restoring the capacity of a cell by replacing a spent or discharged electrode with a fresh one.

Memory Effect-The tendency of a cell to adjust its electrical properties to a certain duty cycle to which it has been subjected for an extended period of time. For instance, if a battery has been cycled to a certain depth of discharge for a large number of cycles, then on a subsequent normal discharge the cell will not give more capacity than that corresponding to the applied cycling regime.

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)-See Field Effect Transistor

Midpoint Voltage-The voltage of a cell or battery midway in the discharge between the fully charged state and the end voltage.

Migration-The transportation of ionic species in the electrolyte due to the presence of an electric field.

Miniature Cell-A button- or coin-shaped cell whose diameter is greater than its height. The term "Miniature" is also used to describe batteries made up of miniature cells.

Minimum Load-1) The lowest specified current to be drawn on a constant voltage power supply for the voltage to be in a specified range. 2) For a constant current supply, the maximum value of load resistance.

Minimum Operating Temperature-The lowest ambient temperature at which the power supply will continuously operate safely and within specifications.

Minimum Starting Temperature-The lowest ambient temperature at which a power supply will turn on and operate safely.

Mismatch-Incorrect matching of load and source impedance.

Mobile Battery-A battery used in mobile applications.

Modified Constant Voltage Charge-A constant voltage charge where the initial current is limited.

Modular-1) A physically descriptive term used to describe a power supply made up of a number of separate subsections, such as an input module, power module, or filter module. 2) An individual power unit patterned on standard dimensions and capable of being integrated with other parts or units into a more complex and higher power system.

Modulator – the control element of a switching power supply.

Molypermalloy Powder (MPP) Core-A core material produced from a magnetic alloy containing nickel, iron and molybdenum that is processed to form a powder and pressed into a toroidal shape. It exhibits very low loss at relatively high ac flux density compared to powdered iron core material.

Monoblock Battery-A secondary battery in which the plate packs are fitted in a multi-compartment Container.

Monoblock Container-A container with several compartments each of which can hold one or more plate packs.

Multiple Power Battery-See Traction Battery

Multimeter-A meter capable of measuring current, voltage and resistance.

Multiple Output Power Supply-A power supply with two or more outputs.

Mutual Inductance (M)-A measure of the amount of inductive coupling between two coils.

Mylar-A registered trade mark of El Dupont De Nemours & Co. for polyethylene terephathalate. The polyester film is a common insulating material used in transformers, capacitors, etc.

Na-Symbol for sodium

NEMA-Abbreviation for National Electrical Manufacturers Association

Ni-Symbol for nickel

NiCad-Abbreviation for Nickel Cadmium Cell

National Electrical Manufacturers Association (NEMA)-Industry trade organization with headquarters in Washington, DC.

Negative Electrode-The Electrode acting as an anode when a cell or battery is discharging.

Negative-Limited-The operating characteristics (performance) of the cell is limited by the negative active material.

Negative Rail-The more negative of the two conductors at the output of a power supply.

Negative Regulator-A voltage regulator whose output voltage is negative compared to the voltage at the return.

Negative Temperature Coefficient-A decreasing function with increasing temperature. The function may be resistance, capacitance, voltage, etc.

Network-Two or more components connected in series, parallel or a combination thereof.

Neutral-The ac return somewhere connected to ground, but which should not be used for ground because it is a current-carrying path.

Nickel-Cadmium (NiCad) Cell-Alkaline cell using nickel and cadmium as active materials and an electrolyte.

No Load Voltage-Terminal voltage of battery or supply when no current is flowing in external circuit. See Off-Load, Open Circuit Voltage

Node-The junction of two or more branches in a circuit.

Noise-The aperiodic random component on the power source output that is unrelated to source and switching frequency. Unless specified otherwise, noise is expressed in peak-to-peak units over a specified bandwidth.

Nominal Value-The stated or objective value of a quantity or component, which may not be the actual value measured.

Nominal Voltage-The stated or objective value of a given voltage, which may not be the actual measured.

O-Symbol for oxygen

OCV-Abbreviation for Open-Circuit Voltage

OP-AMP-Abbreviation for Operational Amplifier

OVP-Abbreviation for Overvoltage Protection

Overreach - the propensity for a relay or fault locator to perceive a fault location further away than it actually is.

OEM-original equipment manufacturer

Oersted -Unit of magnetic intensity equal to one gilbert per centimeter.

Line Power Supply-1) A power supply in which the ac line voltage is rectified and filtered without using a line frequency isolation transformer. 2) A power supply switched into service upon line loss to provide power to the load without significant interruption. See also Uninterruptible Power Supply

Off-Load Voltage-See Open-Circuit Voltage

Offset Current-The direct current that appears as an error at either input terminal of a dc amplifier when the input current source is disconnected.

Offset Voltage-The dc voltage that remains between the input terminals of a dc amplifier when the output voltage is zero.

Ohm (Ω)-Unit of measure of Resistance.

Ohmic Overvoltage-Overvoltage caused by the ohmic drop at an electrode-electrolyte interface.

Ohm's Law-The fundamental mathematical relationship between current (I), voltage (E) and resistance (~ discovered by George Simon Ohm. The passage of one Ampere through one Ohm produces one

Volt.

On-Line Power Supply-A power supply that continuously provides output power to the load without any interruption. See also Uninterruptible Power Supply

On-Load Voltage-The difference in potential between the terminals of a cell or battery when it is discharging.

Open-Circuit Voltage (OCV)-The difference in potential between the terminals of a cell or voltage when the circuit is open (no-load condition). See No Load Voltage

Open-Frame Construction-A construction technique where the supply is not provided with an enclosure.

Open Loop-A signal path without feedback.

Open Loop Gain-Ratio of output signal to input signal without feedback.

Operating Temperature Range-The range of ambient base plate or case temperatures through which a power supply is specified to operate safely and to perform within specified limits. See also Ambient

Temperature, Storage Temperature

Operational Amplifier (OP-AMP)-A high gain differential input device that increases the magnitude of the applied signal to produce an error voltage.

Operational Power Supply-A power supply with a high open loop gain regulator which acts like an operational amplifier and can be programmed with passive components.

Opto-Coupler-A package that contains a light emitter and a photoreceptor used to transmit signals between electrically isolated circuits.

Opto-Isolator-See Opto-Coupler

Outgassing-1) The discharge of gas due to subjecting a material or component to abnormally high temperatures. 2) The release of gas from a cell during operation.

Output-The energy or information delivered from or through a circuit or device.

Output Choke-The inductor in the LC filter of the output.

Output Current Limiting-A protective feature that keeps the output current of a power supply within predetermined limits during overload to prevent damage to the supply or the load. Also see Current Limiting

Output Filter-One or more discrete components used to attenuate output ripple and noise.

Output Filter Capacitor-The capacitor(s) across the output terminals of a power supply.

Output Impedance-The impedance that a power supply appears to present to its output terminals.

Output Inductor-See Output Choke

Output LC Filter-The low pass filter in the secondary of a switching power supply that smooths the rectified output to its average value. Also called an averaging filter.

Output Range-The specified range over which the output voltage or current can be adjusted.

Output Rectifier -A diode(s) used to convert ac to dc in the secondary of the transformer.

Output Ripple and Noise-*Output ripple* is the periodic AC component imposed on the output voltage of a converter. *Output noise* refers to unwanted variations in the converter output that are unrelated to the switching frequency. Ripple and noise are

typically specified together as a peak-to-peak value over a specified bandwidth. Ripple and noise is sometimes referred to as Periodic And Random Deviation (PARD). Care must be taken when measuring output noise and ripple not to induce errors in the test instrumentation. Attach a twisted wire pair (about 1 foot in length) with three twists per/inch between the converter outputs and an appropriate load. Connect a 33 uF electrolytic capacitor across the load. Using an oscilloscope with a minimum bandwidth of 20 MHz and a probe with the ground clip disconnected, measure the ripple at the connection of the load and twisted pair wires. This method eliminates the 'common mode noise" that interferes with measurements made directly at the converter output pins.

Also see Periodic and Random Deviation

Output Voltage-The voltage measured at the output terminals of a power supply.

Output Voltage Accuracy - the maximum allowable deviation of the DC output from its ideal or nominal value. Output voltage accuracy is sometimes called "output voltage tolerance" or "output voltage setpoint" and is commonly given as a percentage of output voltage.

Overcharge-The forcing of current through a cell after all the active material has been convened to the charged state. In other words, charging in excess of that needed to return full capacity to the cell.

Overcurrent Device-A device capable of automatically opening an electric circuit, both under predetermined overload and short-circuit conditions, either by fusing of metal or by electro-mechanical means.

Overcurrent Protection-See Output Current Limiting

Overload Protection Power supply protection based on power supply input power. Many low cost switching power supplies have no method to control or limit output current. The easiest and least expensive protection method is sensing input power. If input power becomes excessive, you assume that one power supply output must have an excessive load. Some overload circuits permanently shut down the power supply; others will automatically recover when the fault is removed. Also see Output Current Limiting

Overshoot-A transient change in output voltage in excess of specified output regulation limits, which can occur when a power supply is turned on or off, or when there is a step change in line or load.

Overvoltage-1) The potential difference between the equilibrium of an electrode and that of the electrode under an imposed polarization current. 2) A voltage that exceeds specified limits.

Overvoltage Protection (OVP)- A power supply feature which shuts down the supply usually by firing a crowbar or clamping the output when an output voltage exceeds a preset level. See also Overvoltage, Crowbar

Oxygen Cycle-See Oxygen Recombination

Oxygen Recombination-The process by which oxygen generated at the positive plate during charge is reacted at the negative plate. Also known as Oxygen Cycle

P-Variously, the abbreviation for Power, pressure.

PARD-Abbreviation for Periodic and Random Deviation

Pb-Symbol for lead.

pH-Negative logarithm of the hydrogen ion concentration.

PIV-Abbreviation for Peak Inverse Voltage

PPM-Abbreviation for parts per million.

Psi-Abbreviation for pounds per square inch.

PWM-variously, the abbreviation for Pulse-Width Modulation, Pulse-Width Modulator

Pad-A conductive area on a printed circuit board used for connection to a component lead or terminal area, or as a test point.

Paper-Lined Cell-Construction of a cell where a layer of paper, wetted with electrolyte, acts as the separator.

Paralleling Connecting the output of two or more supplies together, either for the purpose of delivering additional current or creating redundancy. The reliability of a power system is critical to overall system performance. Indeed, the requirements for power systems are generally higher than those for the system overall. A cost effective way to provide very high levels of reliability is to connect a number of independent power supply units in parallel, such that if one power supply fails, the remaining power supplies will continue delivering sufficient current to supply the maximum system load without any interruption. This architecture is often referred to as an (n+x) redundant power supply. If any one of several paralleled supplies can fail without causing the entire system to fail, the power system is said to be (n+1) redundant. If any two of several paralleled supplies can fail without causing the entire system to fail, the power system is said to be (n+2) redundant.

By allowing the live removal or insertion of power supply boards to and from the system power bus, a "hot pluggable" redundant power supply system provides a practical way to achieve the zero down time required in critical applications such as mainframe computer systems and telecommunications systems.

In practice, (n+x) redundancy can be difficult to achieve. Connecting power supplies in parallel and ensuring that the failure of one parallel supply unit does not affect the remainder presents particular difficulties, ruling out paralleling schemes such as master-slave configurations entirely.

Parallelability-Common usage term to describe power sources that may be connected in parallel.

Pass Element-A controlled variable resistance device, either a vacuum tube or semiconductor, in series with the dc power source used to provide regulation.

Passivation-The phenomenon by which a metal, although in conditions of thermodynamic instability, remains indefinitely unattacked because of certain surface conditions.

Paste-Lined Cell-Leclanche cell constructed so that a layer of gelled paste acts as the separator.

Pasted Plate-A plate, usually for a lead-acid battery, manufactured by coating a grid or support strip with active materials.

Peak-Maximum value of a waveform reached during a particular cycle or operating time.

Peak Charging-A rise in voltage across a capacitor caused by the charging of the capacitor to the peak value of the input voltage.

Peak Inverse Voltage (PIV)-Maximum value of voltage applied in a reverse direction.

Peak Inverse Voltage Rating-The maximum rated voltage that can be applied in the reverse direction across a semiconductor.

Peak Output Current-The maximum current value delivered to a load under specified pulsed conditions.

Peak-To-Peak-The measured value of a waveform from peak in a positive direction to peak in a negative direction.

Periodic and Random Deviation (PARD)-The sum of all ripple and noise components measured over a specified bandwidth and stated, unless otherwise specified, in peak-to-peak values. See Output Ripple and Noise

Phase Angle -The angle that a voltage waveform leads or lags the current waveform.

Phase Controlled Modulation-A regulation technique where operating frequency is held constant (typically line frequency) and the phase angle at which the control elements are turned on is varied, controlling both line and load changes with minimal dissipation.

Phase Inverter-See Inverter

Phase Margin-The amount of phase shift subtracted from 1800 found in a feedback system at the frequency for which its gain reaches unity. The margin from 1800 represents a measure of dynamic stability.

Phase Shift-The difference between corresponding points on input and output signal wave forms (not affected by magnitude) expressed as degrees lead or lag.

Pi Filter-A filter consisting of two line-to-line capacitors and a series inductance in all configuration used to attenuate noise and ripple.

Pilot Cell-A representative cell of a battery utilized to assess the average state of the battery or a somewhat undersized cell that is used as an indicator of the depth of discharge.

Pin Out-The pin assignment of a device.

Plante Plate-A plate for a secondary battery in which active materials are formed directly from a lead substrate by electro-chemical processing.

Plate-1) An assembly for an electrochemical cell of active materials on a supporting framework grid, frame or support strip. 2) Frequently the anode of a cell, battery or electron tube.

Plate Group-An assembly of plates of the same polarity connected together.

Plate Pack-An assembly of the positive and negative plate groups with separators.

Plated Through Hole-A conductive material deposited on the walls of a hole in a printed circuit board is a plated through hole. Sometimes also called vias.

Pocket Plate-A plate for a secondary battery in which active materials are held in perforated metal pockets on a support strip.

Polarity-Property of device or circuit to have poles such as north and south or positive and negative.

Polarization-The change in potential of a cell or electrode from its equilibrium value caused by the passage of an electric current.

Pole-1) Downward break or change in slope on the gain plot of a Bode diagram. 2) The positive or negative terminal of a cell or battery.

Pole Frequency-The frequency associated with a downward break in the gain plot portion of a Bode plot.

Positive Electrode-The electrode acting as a cathode when a cell or battery is discharging.

Positive-Limited-The operating characteristics (performance) of the cell is limited by the positive active materials.

Positive Rail-The most positive of the two output conductors of a power supply.

Post Regulation-Refers to the use of a secondary regulator on a power supply output to improve line/load regulation and to attenuate ripple and noise.

Pot-Abbreviation for potentiometer. Also, name of plant grown in Mendicino County, California.

Potting-An insulating material for encapsulating one or more circuit elements.

Powdered Iron Core-Magnetic core material that contains iron particles held together with a high resistance binder to reduce eddy currents. See also Core, Ferrite, Iron Core

Power (P)-1) Measured in watts, P=EI, 1^2R or E^2/R: 1 watt = 1 joule/second, 1 joule = 1 watt-second 2) In a resistive circuit, power is the product of the in-phase components voltage and current (volt-amperes). See also Apparent Power, True Power

Power Density-1) The ratio of the power available from a power source to its weight, e.g., watts/pound. 2) The ratio of the power available from a power source to its volume, e.g., watts/inch.

Power Factor-The ratio of true to apparent power expressed as a decimal. It has been frequently specified as lead or lag of the current relative to voltage. However, switching power supplies have almost no phase shift but a significant difference between true and apparent power. Thus a switcher's power factor is measured with special equipment. Also see VA.

Power Factor Correction-1) Technique of forcing ac current draw to either approach being in-phase with the voltage waveform or approach a pure sinewave 2) Addition of capacitors to an inductive circuit to offset the reactance and subsequent phase shift. Also see VA.

Power Failure Signal-A logic signal from a power supply that provides advance notice that the output voltage is about to fall out of specifications due to loss of line voltage.

Power FET-Specialized field effect transistor designed for high current or high power applications.

Power Good Signal-A logic signal from a power supply that power is within predetermined specifications. Also called Power OK Signal

Power Grid-A distribution network connecting power generating systems and local utilities.

Power OK Signal-See Power Good Signal

Power Rating-Power available at the output terminals of a power source based on the manufacturers specifications.

Power Source-Any device that furnishes electrical power, including a generator, cell, battery, power pack, power supply, solar cell, etc.

Power Status Signals-See Status Signals

Power Supply-A device for the conversion of available power of one set of characteristics to another set of characteristics to meet specified requirements. Typical application of power supplies include to convert raw input power to a controlled or stabilized voltage and/or current for the operation of electronic equipment.

Power Supply Cord-An assembly of a suitable length of flexible cord provided with an attachment plug at one end. See also Cord Set

Preregulation-The initial regulation circuit in a system containing at least two cascade regulation loops.

Primary Cell or Battery-A cell or battery which is not intended to be recharged and is discarded when the cell or battery has delivered all its electrical energy.

Primary Circuit-A circuit electrically connected to the input or source of power to the device.

Primary Side Control-A name for an off-line switching power supply with the pulse-width modulator in the primary.

Primary Winding-A driven coil in a transformer

Programming-The control of a power supply parameter, such as output voltage, by means of a control element or signal.

Programmable Power Supply-A power supply with an output controlled by an applied voltage, current, resistance or digital code.

Programmable Coefficient-The required range in control resistance to produce a one volt change in output voltage. Expressed in ohms per volt. The ratio of change in a control parameter to induce a unit change in an output, e.g., 100 ohms/volt, or 100 ohms/ampere.

Programming Speed-Programming speed is a measure of a power supply's ability to respond to a varying command to change its output setting from one level to another. Programming speed can be measured in terms of a programming time constant and a slewing rate.

Programming Time-Elapsed time between the initiation of a programmed event and arrival within a specified range of the final value. In the absence of a specified range, 95% of the desired change shall be used.

Proportional Base Drive-A scheme for providing a base drive current in proportion to the transformer switching (emitter) current so the switch is driven into soft saturation to maintain rapid switching times.

Pulse-A step rise, a level, and a step fall of voltage or current. Characteristics of a pulse are: rise time, duration and fall time.

Pulse Discharge-A noncontinuous discharge.

Pulse Droop-See Droop

Pulse Duration-See Duration

Pulse Loading-A pulse load imposed on top of the normal output current from a power supply. See Peak Output Current

Pulse Modulation-Use of pulse code to modulate a transmitter.

Pulse Train-A continuous or discontinuous series of pulses.

Pulse-Width Modulation (PWM)-A method of regulating the output voltage of a switching power supply by varying the duration, but not the frequency, of a train of pulses that drives a power switch.

Pulse-Width Modulator (PWM)-An integrated discrete circuit used in switching-type power supplies, to control the conduction time of pulses produced by the clock.

Push-Pull Converter-A power switching circuit that uses two or more power switches driven alternately on and off.

Q-The energy-storing characteristic of an electronic circuit, system or device, equal to reactance divided by resistance. Q determines rate of decay of stored energy; the higher the 0, the longer it takes for the energy to be released.

Quiescent-At rest; inactive.

Quiet Ground-A low noise analog ground.

r-Variously, the symbol for radius, radio.

R-Symbol for Resistance

RC-Symbol for resistance-capacitance.

REL-Unit of measurement of reluctance equal to 1 ampere-turn per magnetic line of force.

RF-Abbreviation for radio frequency.

RFC-In text, use lower case: rfc. Abbreviation for Radio Frequency Choke

R^1-Abbreviation for Internal Resistance

RFI-Abbreviation for Radio Frequency Interference

RMS Value-In text, use lower case: rms. Abbreviation for Root Mean Square Value

Race Condition-An undesired state that exists when two inputs to a logic or control circuit are both changing, so as to produce an unpredictable output.

Radio Frequency Choke (RFC)-Coil with specified impedance to of currents.

Radio Frequency Interference-An undesired radiated or conducted signal in the radio frequency spectrum.

Rail-Either conductor of the output of a supply. See Positive Rail, Negative Rail

Rated Capacity-The number of ampere-hours a cell or battery can deliver under specific conditions (rate of discharge, end voltage, temperature); usually the manufacturer's rating.

Rated Output Current-The maximum continuous load current a power supply is designed to provide under specified operating conditions.

Rating Drain-The specified current withdrawn from a cell or battery to determine its rated capacity.

Reactance (X)-Opposition to alternating current as result of inductance or capacitance.

Reactive-A component that exhibits the property of either capacitance or inductance.

Real Power - the actual power consumed by a circuit irrespective of power factor, See VA.

Recharge-See Charge

Rechargeable-Capable of being recharged; refers to secondary cells or batteries.

Recombination-The mechanism whereby oxygen reacts with the negative active material to prevent loss of water from the system.

Recovery Time-The time required for the measured characteristic to return to within specified limits follow mg an abnormal event.

Rectification-The process of changing an alternating current to a unidirectional current. See Full-Wave Rectifier, Half-Wave Rectifier

Rectifier-A component that passes current only in one direction, e.g., a diode.

Redox Cell (Reduction-Oxidation Cell 1)-A secondary cell in which two reactant fluids, separated by a membrane, form the active materials.

Redundancy- Power supplies connected in parallel operation so that if one fails, the others will continue delivering enough current to supply the maximum load. This method is used in applications where power supply failure cannot be tolerated. See Paralleling.

Reference Electrode-A specially chosen electrode which has a reproducible potential against which other electrode potentials may be referred.

Reference Ground-Defined point in a circuit or system from which potential measurements shall be made.

Reference Voltage-The defined or specified voltage to which other voltages are compared.

Regulated Power Supply-A device that maintains within specified limits a constant output voltage or current for specified changes in line, load, temperature or time.

Regulation-The process of holding constant selected parameters, the extent of which is expressed as a percent.

Regulator-The power supply circuit that controls or stabilizes the output parameter at a specified value

Reinforced Insulation-As defined by Underwriters Laboratories, Inc., an improved basic insulation with such mechanical and electrical qualities that it, in itself, provides the same degree of protection against electrical shock as double insulation. It may consist of one or more layers of insulating material. It is acceptable in place of double insulation.

Relay-A magnetic component or solid state device that opens or closes an isolated switch(es) when a voltage is applied to the control terminals.

Reluctance-Resistance to flow of magnetic lines of force. Unit of measurement is the REL.

Remote Enable/Disable-A logic signal used to turn a power supply on or off.

Remote Margining-See Margining

Remote Programming-See Programming

Remote Sensing- A technique for regulating the output voltage of a power supply at the load by connecting the error-sensing leads to the load. Remote sensing compensates for voltage drops in cables and connectors between the power supply and the load. Since the remote sense leads usually directly control the power supply's

internal feedback loop, the system should not be operated with the remote sense leads disconnected. Also, when connecting remote sense leads, make sure the + lead goes to the + end of the load. A very common mistake is to reverse the leads, which can damage the system.

Remote Voltage Adjustment Adjustments of the output voltage made remotely over a limited range by a variable resistor. This type of control is often found on high density DC/DC converters.

Repeatability-The ability to duplicate results under identical operating conditions.

Required Headroom-The minimum voltage across a series regulator which results in a regulated output voltage.

Reserve Cell-A cell which may be stored in an inactive state and made ready for use by adding electrolyte (or another cell component) or, in the case of a thermal battery, melting a solidified electrolyte.

Reset Current-A current injected into the winding of a magnetic component to reset the core.

Reset Signal-A signal used to return a circuit to a desired state.

Residual Flux-The flux that exists in a magnetic core after the H field is returned to zero.

Resistance (R)-Property of a material that opposes the flow of current.

Resonance-1) The state in which the natural response frequency of a circuit coincides with the frequency of an applied signal, or vice versa, yielding intensified response. 2) The state in which the vibration frequency of a body coincides with an applied vibration force, or vice versa, yielding rein-forced vibration of the body.

Resonant Circuit-A circuit in which inductive and capacitive elements are in resonance at an operating frequency.

Resonant Converter-A class of converters that uses a resonant circuit as part of the regulation loop.

Resonant Frequency-The natural frequency at which a circuit oscillates or a device vibrates. In an L circuit, inductive and capacitive reactances are equal at the resonant frequency.

Response Time-The time required for the output of a power supply or circuit to reach a specified fraction of its new value after a step change or disturbance.

Return-The name for the common terminal of the output of a power supply; it carries the return currents for the outputs.

Reversal-The changing of the normal polarity of a cell or battery.

Reverse Current-See Leakage Current

Reverse Energy-The product of reverse voltage times reverse current in a diode integrated over specified time.

Reverse Polarity-A connection that is opposite to that which is specified or intended.

Reverse Recovery Time (Diode)-The time required to remove charge carriers from the junction of rectifier when reverse voltage is applied.

Reverse Voltage Protection-A circuit or circuit element that protects a power supply from damage by a voltage of reverse polarity applied at the input or output terminals.

Ride-Through-See Holdup Time

Ripple-The periodic ac component at the power source output harmonically related to source or switching frequencies. Unless specified otherwise, it is expressed in peak-to-peak units over a specified band width.

Ripple and Noise-See Periodic and Random Deviation (PARD)

Ripple Voltage-The periodic ac component of the dc output of a power supply.

Rise Time-The time required for a pulse to rise from 10 percent to 90 percent of its maximum amplitude

Root Mean Square (RMS) Value-The equivalent DC voltage that produces exactly the same amount of heating as the AC waveform in a simple (non-inductive) resistor. The RMS value of a sine wave is 0.707 x Peak Value.

s-Abbreviation for second.

S-Variously, the symbol for source, secondary winding. Abbreviation for Siemens

SCC-Abbreviation for Short-Circuit Current

SCR-Abbreviation for Silicon-Controlled Rectifier

SELV-Abbreviation for Safe Extra Low Voltage

SI-Abbreviation for Systeme International d'Unites

SLI-Abbreviation for starting, lighting, ignition.

SMD-Abbreviation for Surface Mounted Device

SMPS-Abbreviation for Switched Mode Power Supply

SOA-Abbreviation for Safe Operating Area

SOC-Abbreviation for State-of-Charge

SPS-Abbreviation for Standby Power Supply

Safe Extra Low Voltage (SELV)-International safety standards as described in IEC 380 and VDE 0806.

Safe Operating Area (SOA)-A manufacturer specified power/time relationship that must be observed to prevent damage to power bipolar semiconductors.

Safety Classes-Grouping of products by various safety agencies to conform to their unique standards.

Safety Compliance-Certification, recognition or approval by safety agencies such as Underwriters Laboratories Inc. (UL/U. S. A.), Canadian Standards Association (CSA), etc.

Safety Ground-A conductive path from a chassis, panel or case to earth to help prevent injury or damage to personnel and equipment.

Saturable Reactor-A magnetic component with a square loop hysteresis curve. The saturable reactor when driven in and out of saturation functions as a magnetic amplifier or switch.

Saturation (Magnetic)-A condition in a magnetic material in which an increase in (B) will no longer produce an appreciable increase in (H).

Saturation (Bipolar Transistor)-A condition when an increase in base current will not produce an appreciable change in the collector-emitter voltage.

Sawtooth Waveform-A serrated waveform resembling the teeth of a saw.

Schottky Diode-A diode device that exhibits a low forward voltage drop and fast recovery time relative to a standard silicon diode.

Sealed Cell-A cell which is sealed under normal conditions, but allows the escape of gas if the internal pressure exceeds a critical value.

Secondary-A cell or battery designed to be recharged. See also Secondary Output, Secondary Winding, Secondary Battery, Secondary Cell

Secondary Battery-A galvanic battery which, after discharge, may be restored to the fully charged state by the passage of an electric current through the cell in the opposite direction to that of discharge.

Secondary Breakdown-A failure mode that occurs when a bipolar transistor is operated outside its safe operating area.

Secondary Cell-A galvanic cell which, after discharge, can be brought back to its initial condition by passing a current through it in the reverse direction to that of discharge.

Secondary Circuit-A circuit electrically isolated from the input or source of power to the device.

Secondary Circuit protection-Overcurrent protection located in the secondary circuit.

Secondary Output-An output of a switching power supply that is not sensed by the control loop.

Secondary Protection-See Overload Device

Secondary Winding-A coil that receives energy from the primary winding by mutual induction and delivers energy to the load is the secondary winding.

Self-Discharge-The loss of useful capacity of a cell or battery on storage due to internal chemical action (local action).

Self-Discharge Rate-The rate at which a cell or battery loses rated capacity when standing idle.

Self-Inductance-Inductance that produces an induced voltage in itself as the result of a change in current flow.

Semiregulated Output-A subjective term indicating partial regulation.

Sense Line-The conductor which routes output voltage to the control loop. See also Remote Sensing

Sense Line Return-The conductor which routes the voltage on the output return to the control loop.

See also Remote Sensing

Separator-An ionic, permeable, electronically nonconductive spacer which prevents electronic contact between electrodes of opposite polarity in the same cell.

Sequencing-The process that forces the order of turn on and turn off of individual outputs of a multiple output power supply.

Series-1) The interconnection of two or more power sources such that alternate polarity terminals are connected so their voltages sum at a load. 2) The connection of circuit components end to end to form a single current path.

Series Pass-A controlled active element, such as a transistor, in series with a load that is used to regulate voltage.

Series Regulation-See Linear Regulation

Series Regulator-A regulator in which the active control element is in series with the dc source and the load.

Service Life-1) The period of useful life of a primary cell or battery before a predetermined end-point voltage is reached. 2) Period of useful life of a power supply before a predetermined end of life point is reached. Service life may be significantly increased by the replacement of select components.

Service Maintenance-The percent of rated capacity remaining after a specified period of time.

Setting Range-The range over which the value of the stabilized output quantity may be adjusted.

Settling Time-The time for a power supply to stabilize within specifications after an excursion outside the input/output design parameters. Related topic: Transient Response

Shape Change-Change in shape of an electrode due to migration of active material during charge/discharge cycling.

Shelf Life-The duration of storage under specified conditions at the end of which a component or device retains the ability to give a specified performance.

Shield-Partition or enclosure around components in a circuit to minimize the effects of stray magnetic and radio frequency fields. See also Enclosure, Electrostatic Shield, Faraday Shield

Shock and Vibration . A specification requirement for which a power supply is designed or tested to withstand, such as 20 G shock for 11 milliseconds and 5G random vibration for 2 hours over a 2 -2000 Hz bandwidth.

Shock Hazard-A potentially dangerous electrical condition that may be further defined by various industry or agency specifications.

Short-Circuit-A direct connection that provides a virtually zero resistance path for current.

Short-Circuit Current (SCC)-The initial value of the current obtained from a power source in a circuit of negligible resistance.

Short-Circuit Protection-A protective feature that limits the output current of a power supply to prevent damage.

Short-Circuit Test-A test in which the output is shorted to ensure that the short circuit current is within its specified limits.

Shunt-1) A parallel conducting path in a circuit. 2) A low value precision resistor used to monitor current.

Shunt Regulator-A linear regulator in which the control element is in parallel with the load, and in series with an impedance, to achieve constant voltage across the load.

Siemens (S)-SI unit of measurement of conductance (replaces cgs unit, mho).

Signal Ground-The common return or reference point for analog signals.

Silicon-Controlled Rectifier (SCR)-A uni-directional, four-layer (PNPN) junction device in which conduction is initiated by the application of a gate current. Conduction will continue until the current is reduced to some minimum value.

Sintered Electrode-An electrode construction in which active materials are deposited in the interstices of a porous metal matrix made by sintering metal powder. Also called sintered plate.

Sine Wave-A wave form of a single frequency alternating current whose displacement is the sine of an angle proportional to time or distance.

Single Point Ground-The one point in a system that connects multiple grounds and returns. Also known as star ground, or holy point ground.

Sinusoidal Frequency Response-The maximum sinusoidal frequency to which a fast-programmable power supply will respond with specified distortion in the output waveform.

SLI Battery-A battery designed to start internal combustion engines and to power the electrical systems in automobiles when the engine is not running (starting, lighting, ignition). Also called Starter Battery.

Slave-A power supply which uses the reference in another power supply, the master, as its reference.

Slewing Rate-The maximum rate of change a power supply output can produce when subjected to a large step response or specified step change.

Slow Start-A feature that ensures the smooth, controlled rise of the output voltage, and protects the switching transistors from transients when the power supply is turned on.

Snubber-An RC network used to reduce the rate of rise of voltage in switching applications.

Snubber Network-A circuit that uses a RC network and a diode in unipolar switching applications.

Soft Start A feature that lowers the peak inrush current during power supply turn-on.

Solidstate Switch-A switch that uses no moving parts.

Source-Origin of the input power, e.g., generator, utility lines, mains, batteries, etc.

Source Frequency Effect-The effect on the output of a change in source frequency; or the change in stabilized outputs produced by a specified primary source frequency change. (Note: Mainly affects ferroresonant-type power supplies.)

Source Voltage Effect-The change in stabilized output produced by a specified primary source voltage change.

Spacings-See Clearance Distance, Creepage Distance Specific Energy-See Energy Density

Specific Gravity-The specific gravity of a solution is the ratio of the weight of the solution to the weight an equal volume of water at a specified temperature.

Specific Power-See Power Density

Spiral Wound-The shape of the internal roll in a cylindrical device made by winding electrodes or conductors and separators or insulators into a spiral wound, jelly-roll-like construction.

Split Bobbin Winding-The method of winding a transformer whereby the primary and secondary are wound side-by-side on a bobbin with an insulation barrier between the two windings.

Stability-1) The percent change in output parameter as a function of time, with all other factors constant, following a specified warm-up period. 2) The ability to stay on a given frequency or in a given state without undesired variation.

Standard Electrode Potential (E^0)-The equilibrium value of an electrode potential when all the constituents taking part in the electrode reaction are in the standard state. See also Electrode Potential

Standby Battery-A battery designed for emergency use in the event of a main power failure.

Standby Current-The input current drawn by a power supply under no load conditions.

Standby Power Supply (SPS)-A power source designed to furnish power in periods of line loss.

Standoff-A mechanical support, which may be an insulator, used to connect and support a wire or device away from the mounting surface.

Star Ground-See Single Point Ground

Starter Battery-See SLI Battery

Starting Drain-See Initial Drain

Start-Up Delay-The time delay between either applying ac or a remote "on" and the time at which the outputs are in regulation.

Start-Up Sequence-The order of events that occur in a power supply during start up. For example, an active inrush limiting circuit may start first, followed by output voltages which must reach regulation in a particular sequence. Then a logic output signals the end of the start-up sequence and proper power supply operation.

Starved Electrolyte Cell-A cell containing little or no free fluid electrolyte. This enables gases to reach

electrode surfaces during charging and facilitates gas recombination.

State-of-Charge (SOC)-The available or remaining capacity in a cell or battery expressed as a percentage of rated capacity.

Static Load-A load that remains constant over a given time period.

Static Transfer Switch-A solid-state switch used in Standby Power Supply (SPS) and Uninterruptible Power Supply (UPS) systems for transferring the load between the ac power line and inverter output.

Stationary Battery-A secondary battery designed for use in a fixed location.

Status Signals-Logic signals that indicate normal or abnormal conditions of operation, including:

ac low dc low

ac ok dc ok

overtemperature overvoltage

undertemperature overcurrent

Step Change-An abrupt and sustained change in one of the influence or control quantities of a power supply.

Step-Down Transformer - A transformer with a turns ratio more than one. The output voltage is less than the input voltage. See also, Isolation Transformer, Step-up Transformer, Transformer

Step-Up transformer - A transformer in which the power transfer is from the lower voltage source circuit to a higher voltage circuit.

Storage Battery-A secondary battery designed for use in a fixed location.

Storage Life-See Shelf Life

Storage Temperature-The range of ambient temperatures through which an inoperative power supply can remain in storage without degrading its subsequent operation. See also Ambient Temperature, Operating Temperature

Storage Transformer-A transformer with a turns ratio less than one. The output voltage is greater than the input voltage. See also, Isolation Transformer, Step-Down Transformer, Transformer

Sulphation-The formation of lead sulphate on the electrodes of a lead-acid battery. The term is usually applied to large crystals or crusts of insoluble lead sulphate which form after inappropriate or abusive use.

Summing Point-The point at which two or more inputs of an operational amplifier are algebraically added.

Supplementary Insulation-As defined by Underwriters Laboratories, Inc., an independent insulation provided in addition to the basic insulation to protect against electric shock in case of mechanical rupture or electrical breakdown of the basic insulation. An enclosure of insulating material may form a part of the whole of the supplementary insulation.

Surface Mounted Devices (SMD)-A family of components intended to be mounted directly upon the surface of a substrate or circuit board.

Switching Frequency-The rate at which the dc voltage is switched in a converter or power supply.

Switching Power Supply - "Switchers" are typically smaller (by about 10X), lighter (by about 10X) and generate less heat (by about 5X) compared to an equivalent linear supply. At output power ratings above about 25W they are usually less expensive. However, their transient response is slower, output regulation less precise, and have higher PARD (noise). These latter issues aren't usually a problem for most digital circuits, but must be considered when powering sensitive analog circuits.

Switching Regulator-A switching circuit that operates in a closed loop system to regulate the power supply output.

Synchronous Rectification-A rectification scheme in a switching power supply in which a FET or bipolar transistor is substituted for the rectifier diode to improve efficiency.

Systeme International d'Unites (SI)-The International System of Units comprised of Base Units, Supplementary Units and Derived Units.

t-Symbol for temperature in ^{0}C.

T-Variously, the symbol for transformer, absolute temperature. The abbreviation for Tesla

TTL-Abbreviation for transistor-transistor logic.

Tank Circuit-Parallel resonant circuit.

Tape Core-A magnetic toroid whose magnetic core is formed by concentric wraps of an iron alloy with thin insulated film between layers.

Taper Charge-A charge regime delivering moderately high rate charging current when the battery is at a low state of charge and tapering the charging current to lower rates as the battery is charged.

Technischer Uberwachungs-Verein (TUV)-Laboratories licensed by the West German government or testing electronic products to DIN, IEO and VDE standards.

Temperature Coefficient-The average percent change in output voltage per degree Centigrade change in ambient temperature over a specified temperature range. See also Ambient Temperature

Temperature Derating-The amount by which power source or component ratings are decreased to permit operation at elevated temperatures.

Temperature Effect-See Temperature Coefficient

Temperature Range, Operating . The range of ambient or case temperatures within which a power supply may be safely operated and meet its specifications. See Operating Temperature Range

Temperature Range, Storage . The range of ambient temperatures within which a power supply may be safely stored, non-operating, with no degradation in its subsequent operation. See Storage Temperature Range

Tertiary Winding - The third winding of the transformer and often provides the substation service voltage, or in the case of a wye-wye connected transformer, it prevents severe distortion of the line-to-neutral voltages.

Tesla (T)- SI unit of magnetic flux density (magnetic induction) expressed as 1 weber/square meter.

Thermal Equilibrium-The point at which the temperature of a component or device becomes stable.

Thermal Protection-A protective feature that shuts down a power supply if its internal temperature exceeds a predetermined limit.

Thermal Runaway-A condition. in a power source or component where an increase in temperature increases current flow causing a further increase in temperature, the spiraling effect of which leads to failure.

Thermistor-An electronic device that makes use of the change of resistivity of semiconductor with a change in temperature. In power supplies, negative temperature coefficient thermistors frequently are used as inrush current limiting devices.

Three-Phase Current-Combination of three alternating currents having their voltages displaced by 120 degrees, or one-third cycle.

Three Terminal Regulator-A power integrated circuit in a 3-terminal standard transistor package. It can be either a series or shunt regulator IC.

Thyristor-A solid state device that has bistable electrical characteristics. Three common thyristor devices are diacs, silicon-controlled-rectifiers (SCRs) and triacs.

Time Constant-Time period required for the voltage of a capacitor in an RC circuit to increase to 63.2 percent of maximum value or decrease to 36.7 percent of maximum value.

Time Effect-See Drift

Tolerance-Measured or specified percentage variation from nominal.

Toroid-A round magnetic core with a hole in the middle. A doughnut shaped core.

Total Effect-The change in a stabilized output produced by concurrent worst case changes in all influence quantities within their rated range.

Total Regulation Band-The range of combined regulation tolerances such as the effects of input voltage variation, output load variation, temperature variation, drift and other specified variables. It is expressed as a plus/minus percent from nominal. Also called accuracy limits.

Trace-A conducting path on a printed circuit board.

Tracking-A characteristic of a multiple-output power supply that describes the changes in the voltage of one output with respect to changes in the voltage or load of another.

Tracking Regulator-A plus and minus two-output supply in which one output tracks the other.

Traction Battery-A secondary battery designed for the propulsion of electric vehicles or electrically operated mobile equipment operating in a deep-cycle regime.

Train Lighting Battery-A secondary battery used in trains to maintain essential services such as lighting and air conditioning.

Transformer-Device which transfers energy from one circuit to another by electromagnetic induction.

See Isolation Transformer, Step-Down Transformer, Step-up Transformer

Transient-An excursion in a given parameter, typically associated with input voltage or output loading.

Transient Effect-The result of a step change in an influence quantity on the steady state values of a circuit.

Transient Recovery Time-The time required for the output voltage of a power supply to settle within specified output accuracy limits following a transient.

Transient Response-Ability of a power supply to recover a constant voltage following a step change in output current.

Transient Response Time-The interval between the time a transient is introduced and the time it returns and remains within a specified amplitude range.

Transition Time-The time of an electrode process from the initiation of the process at constant current to the moment an abrupt change in potential occurs signifying that a new electrode process is controlling the electrode potential.

Transport Number-The fraction of the total cell current carried by the cation of an electrolyte solution is called the "cation transport number." Similarly, the fraction of the total current carried by the anion is referred to as the "anion transport number."

Triac-A bi-directional silicon-controlled switch.

Trickle Charge-A charge at low rate, balancing losses through local action and/or periodic discharge, to maintain a cell or battery in a fully charged condition.

Trifilar-Three conductors in parallel on a magnetic core form in which all three conductors are wound in the same operation. Three in hand.

True Power-Actual power generated or consumed in a circuit.

Tubular Plate-A battery plate in which an assembly of perforated metal or polymer tubes holds the active materials.

Tuned Circuit-Circuit containing capacitance, inductance and (optionally) resistance, connected in series or parallel, which when energized at a specific frequency known as its resonant frequency, an inter-change of energy occurs between the coil and the capacitor.

Turns Ratio-Ratio of the number of turns on the primary winding of a transformer to the number of turns on the secondary winding.

Twin Cell-A two-cell unit in steel-container where the positive pole of one of the plate packs and the negative pole of the other are connected to the bottom of the container.

Two-Step Charge-A charge which starts at one current and, at a predetermined point, continues at a lower current.

UL-Abbreviation for Underwriters Laboratories Incorporated.

UPS-Abbreviation for Uninterruptible Power Supply

Unactivated Shelf Life-The period of time, under specified conditions of temperature and environment, that an inactivated or reserve cell or battery can stand before deteriorating below a specified capacity.

Under reach - the propensity for a relay or fault locator to perceive a fault location closer than it actually is.

Undershoot-A transient change in output voltage in excess of specified output regulation limits. See Overshoot

Undervoltage Protection-A circuit that inhibits the power supply when output voltage falls below a specified minimum.

Underwriters Laboratories Incorporated (UL)-American association chartered to test and evaluate products, including power sources. The group has four locations so an applicant can interact with the office closest in the country to his/her own location.

Uninterruptible Power Supply (UPS)-A type of power supply designed to support the load for specified periods when the line varies outside specified limits. UPS systems generally filter the AC line voltage and provide battery-backup power in the event that the main AC power fails. UPS systems are separated into two major categories, standby and continuous operation systems. Within each of these categories are square, quasi-square and sinewave output systems. The simplest and least expensive UPS is a standby UPS with square wave output. In a standby UPS, input power flows through the UPS (usually through a triac) to the output. If there is no filtering, the output will include noise or transients present at the input. When the input AC voltage falls below a minimum value, the input is turned off, battery power is inverted to AC and delivered to the output. The transition or switching time (from mains power to battery power) must be shorter than the power supply's holdup time or the power supply will momentarily fail. In a continuous UPS, the DC/AC inverter is continuously supplying power to the load and the AC power serves to maintain battery charge. Of the three different types of waveforms, generating a square waveform is the easiest, least expensive and least desirable waveform. Not only does a square wave include a rich compliment of undesirable harmonics, it also charges the input energy storage capacitor of a conventional switcher (which is usually the UPS load) to a lower-than-normal peak voltage, increasing switching current, switch transistor temperature and reducing component lifetime. On the other hand, generating a sinewave output is far more difficult, expensive but more electrically desirable.

Universal Input. Power supply's ability to accept a wide input voltage range (90VAC to 264VAC) without the selection of input range, either manually or electronically. As opposed to autoranging or auto-select input. See Autoranging Input

Unity Coupling-The theoretical positioning of two coils so all lines of magnetic flux of one coil cut across all turns of a second coil.

Unity Gain Bandwidth-The upper frequency limit at which the open-loop gain becomes unity (one).

Utilization-The percent of rated capacity that can be obtained from a cell or battery during discharge under specified conditions.

V-Abbreviation for Volt

VA-Abbreviation for Volt-Ampere. This term is used when the AC voltage and AC current waveforms can be or are out of phase, and the product of their RMS values does NOT equal the real power. Whenever a power supply output is AC (alternating current), the potential exists for the voltage and current waveforms to be out-of-phase or non-sinusiodal. In these cases, the VA product can be much larger than the real power delivered. In an extreme case, the voltage and current sine waveforms may be 90 degrees out-of-phase. The power supply providing this output is delivering no output power but could be well over its maximum voltage or current output rating.

VAR-The unit of measurement of reactive power. It is derived from Volt-Ampere Reactive.

VDE -Abbreviation for Verband Deutscher Elektrotechniker.

VPR-Abbreviation for volts-per-cell.

Vacuum Impregnation-The process of using a vacuum to remove gaseous materials from a potting compound prior to curing.

Varistor-A two-electrode semiconductor device having a voltage-dependent nonlinear resistance.

Varnish Dip-The process of dipping a transformer or coil in varnish to bind or protect materials.

Varnish Impregnation-A varnishing and baking process used to bind together the turns on a magnetic component and protect the component against moisture. The varnish prevents movement of the conductors.

Vent-A normally sealed mechanism which allows for the controlled escape of gases from within a cell.

Vented Cell-A cell design in which a vent mechanism operates to expel gases that are generated during the operation of the cell.

Vias-See Plated Through Hole

Volt (V)-Unit of measurement of electromotive force or potential difference. Symbol E, in electricity; symbol V in semiconductor circuits.

Volt-Ampere (VA)-Measurement unit of apparent power. VA implies the product of volts rms times amps rms. Whenever a power supply output is AC (alternating current), the potential exists for the voltage and current waveforms to be out-of-phase or non-sinusiodal. In these cases, the VA product can be much larger than the real power delivered. In an extreme case, the voltage and current sine waveforms may be 90 degrees out-of-phase. The power supply providing this output is delivering no real output power but could be well over its maximum voltage or current output rating.

Volt Microsecond-Rate of change of voltage over a period of time expressed in volts/microseconds.

Volt Microsecond Clamp-A circuit in the control of the pulse width modulator located in the primary which terminates the pulse when the volt microseconds applied to the primary of the transformer exceeds a predetermined value.

Voltage-A derivative electrical quantity, E, measured in the unit Volts and defined in terms of the independently obtained Ampere, I, and the unit of resistance, Ohm (R) by Ohm's Law E = IR.

Voltage Balance-The difference in magnitude, in percent, between differential tracking output voltages of a power supply where the voltages have equal nominal values with opposite polarities.

Voltage Clamp-See Clamp Circuit, Clipper Circuit

Voltage Delay-Time delay for a cell or battery to deliver the required operating voltage after it is placed under load.

Voltage Divider-Tapped or series resistance or impedance across a source voltage to produce multiple voltages.

Voltage Doubler-See Voltage Multiplier

Voltage Drop-Difference in potential between two points in a passive component or circuit.

Voltage Efficiency-The ratio of average voltage during discharge to average voltage during recharge under specified conditions of charge and discharge.

Voltage Limit-Maximum or minimum value in a voltage range.

Voltage Limiting-Bounding circuit used to set specified maximum or minimum voltage levels.

Voltage Mode-The functioning of a power supply so as to produce a stabilized output voltage.

Voltage Monitor-A circuit or device that determines whether or not an output voltage is within some specified limits.

Voltage Multiplier-Rectifier circuits that produce an output voltage at a given multiple greater than input voltage, usually doubling, tripling or quadrupling.

Voltage Regulation-The process of holding voltage constant between selected parameters, the extent of which is expressed as a percent. See also Regulation

Voltage Source-A power source that tends to deliver constant voltage.

Voltage Stabilization-The use of a circuit or device to hold constant an output voltage within given limits.

Voltaic Cell-Cell producing a potential difference by chemical action. See also Galvanic Cell

W-Abbreviation for Watt

Wb-Abbreviation for Weber

Wh-Abbreviation for Watt-Hour

Warmup-Process of approaching thermal equilibrium after turn on.

Warmup Drift-The change in output voltage of a power source from turn on until it reaches thermal equilibrium at specified operating conditions.

Warmup Effect-Magnitude of change of stabilized output quantities during warmup time.

Warmup Time-The time required after a power supply is initially turned on before it operates according to specified performance limits.

Watt (W)-Unit of measurement of power equal to 1 joule/sec. (W=[l).

Watt-Hour (Wh)-Unit of energy measurement, equal to one watt per hour (3600 joules).

Watt-Hour Capacity-The quantity of electrical energy measured in watt-hours which may be delivered by a cell or battery under specified conditions.

Watt-Hour Efficiency-The ratio of the watt-hours delivered on discharge of a battery to the watt-hours needed to restore it to its original state under specified conditions of charge and discharge.

Weber (Wb)-The SI unit of magnetic flux equal to 108 maxwells. The amount of flux that will induce 1 volt/turn of wire as the flux is reduced at a constant rate to zero over a period of one second.

Wet Shelf Life-The period of time that a cell or battery can stand in the charged or activated condition before deteriorating below a specified capacity.

Winding-A conductor wrapped onto a magnetic core or core form, e.g., a transformer primary or secondary.

Winding Area-The cross-sectional area of a bobbin or magnetic core that can be filled with a winding.

Winding Length-The allowable length on a core form or bobbin that can be occupied by a single layer winding. One dimension of the core window.

Winding Machine-A machine designed to put wire onto a bobbin or core form, or onto a toroid.

Window-The specified range of given values. See also Core Window

Wire Style Number-The categorization by regulatory and testing agencies of appliance wiring material with respect to insulation type, thickness, number of conductors and use.

Wire Table-A listing of wire gauges that includes the diameter, cross-sectional area, insulation and resistance of each wire gauge size.

Withstand Voltage-The maximum voltage that can be applied between separate circuits without causing failure.

Working Voltage-The specified operating voltage, or range of voltages, of a component, device or cell.

Worst Case Condition-A set of conditions where the combined influences on a system or device are most detrimental.

X-Symbol for Reactance

Xc-Symbol for Capacitive Reactance

XL-Symbol for Inductive Reactance

X Capacitors-EMI filter capacitors across the line that meet the requirements of certain regulatory agencies.

Y Capacitors-EMI filter capacitors between line and ground that meet the requirements of certain regulatory agencies.

Y (or Wye) Connection - So connected that one end of each of the windings of a polyphase transformer (or of each of the windings for the same rated voltage of single-phase transformers associated in a polyphase bank) is connected to a common point (the neutral point) and other end to its appropriate line terminal.

Z-Variously, symbol for **Impedance,** atomic number.

Z Match-Abbreviation for **Impedance Matching**

Zener Break Frequency-A frequency on a Bode plot at which the tangent to the gain increases.

Zener Diode-1) A diode that makes use of the breakdown properties of a PN junction. If a reverse voltage across the diode is progressively increased, a point will be reached when the current will greatly increase beyond t normal cut-off value to maintain a relatively constant voltage. Either voltage point is called the Zener voltage. 2) The breakdown may be either the lower voltage Zener effect or the higher voltage avalanche effect.

Zener Voltage The reverse voltage at which breakdown occurs in a zener diode.

Zigzag Connection - A polyphase transformer with Y-connected windings, each one of which is made up of parts in which phase-displaced voltages are induced.

Zinc Chloride-A Carbon Zinc battery with a slightly acidic electrolyte consisting mainly of zinc chloride in water.

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