ElCoM
ELECTRICAL COMPUTER MECHATRONICS

تقدم لجنة ElCoM الاكاديمية

تلخيص لمادة:

منطق رقمي والكترونيات رقمية

جزيل الشكر للطالبة:

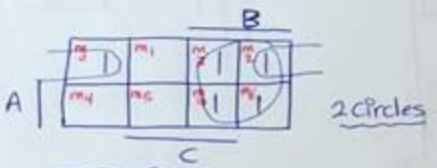
سارة ابو سارة

Ex Write the function that follows the truth table below.
Report sheet then combine IC chips according to the Logic CCT :-

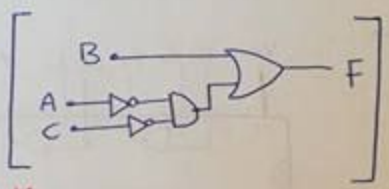
→ Using k-map :

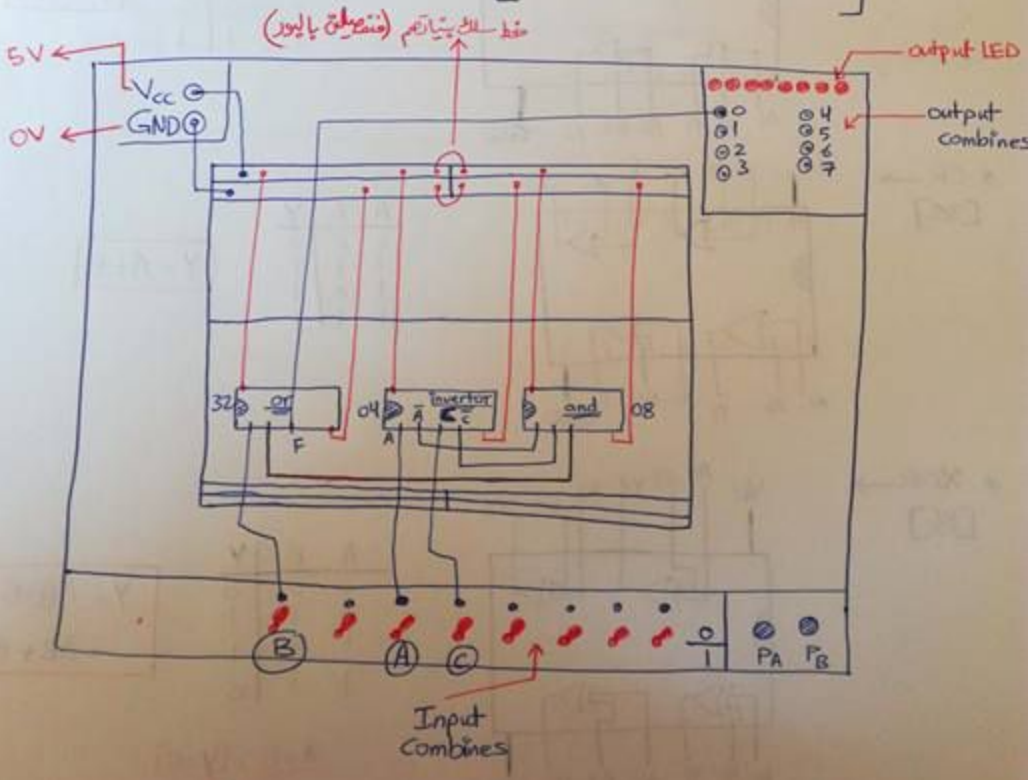
2^{3} = 8 combinations ← 3 = no of input

	MSB A	B	LSB C	F
m_0	0	0	0	1
m_1	0	0	1	0
m_2	0	1	0	1
m_3	0	1	1	1
m_4	1	0	0	0
m_5	1	0	1	0
m_6	1	1	0	1
m_7	1	1	1	1



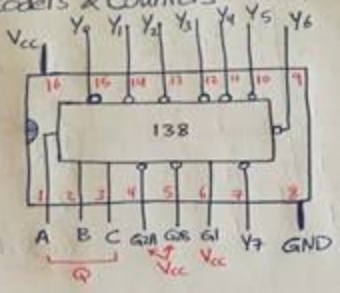
$F = B + \bar{A}\bar{C}$ → Logic CCT →





Exp(3) Decoders & Counters

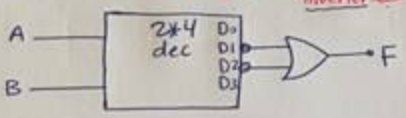
* Decoders → [138]



[G0 = L → GND
G1 = Vcc]

Ex [from manual]

Design a logic CCT using an active low 2*4 decoder where F(A,B) = ∑(1,2) where F is an active HIGH function so



F is high when D1 or D2 are low

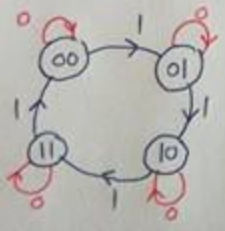
* Counter → [193]

Synchronous Counter

* If the counter counts up:-
  count up (5) → CLK
  count down (4) → Vcc
* If the counter counts down:-
  count down (4) → CLK
  count up (5) → Vcc

Ex [from manual]

Design a logic CCT that counts [0-4] then back to 0 only if an input signal is



Q_1	Q_0	X	Q_1^+	Q_0^+	J_1 K_1	J_2 K_2
0	0	0	0	0	0 X	0 X
0	0	1	0	1	0 X	1 X
0	1	0	0	1	0 X	X 0
0	1	1	1	0	1 X	X 1
1	0	0	1	0	X 0	0 X
1	0	1	1	1	X 0	1 X
1	1	0	1	1	X 0	X 0
1	1	1	0	0	X 1	X 1

$J_1 = K_1 = XQ_0$

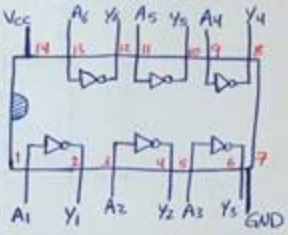
$J_0 = K_0 = X$

Logic Lab. [midterm]

Exp(1) Combinational Logic Gates

* Inverter, and, OR, XOR *

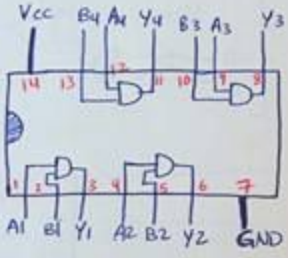
* Inverter → [04]



A	Y
0	1
1	0

$Y = \bar{A}$

* AND → [08]



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

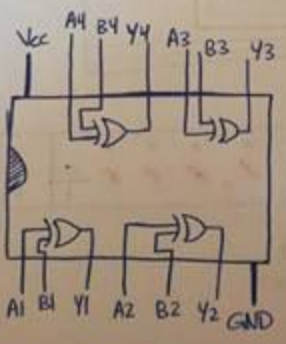
$Y = A \cdot B$

* OR → [32]

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

$Y = A + B$

* XOR → [86]



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

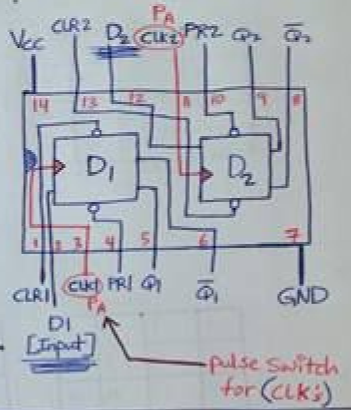
$Y = A \oplus B$
$= \bar{A}B + A\bar{B}$

$A = B$, $[Y = 0]$

Exp(2) Sequential Logic Circuit [Using f/f's]

D, T, JK

* D f/f → [74]



$D_A = Q_A^+$

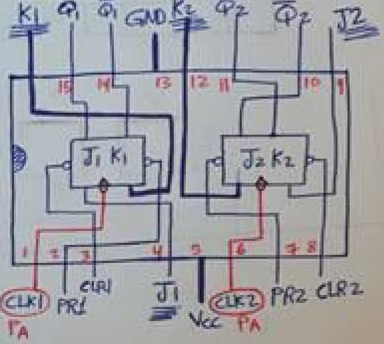
D_A	Q_A^+
0	0
1	1

Function Table

PR	CLR	CLK	D	Q^+	$\bar{Q}^+$
1	1	↑	0	0	1
1	1	↑	1	1	0

(PR, CLR) ثابتة بتشبكهم على Vcc (high) (1)

* JK f/f → [76]



$Q_A^+ = J_A\bar{Q}_A + \bar{K}_A Q_A$

J_A	K_A	Q^+
0	0	Q
0	1	0
1	0	1
1	1	$\bar{Q}$

(J_A, K_A → كل وحدة إلها function بيكون)

Function Table

PR	CLR	CLK	J	K	Q^+	$\bar{Q}^+$
1	1	⎍	0	0	Q	$\bar{Q}$
1	1	⎍	0	1	0	1
1	1	⎍	1	0	1	0
1	1	⎍	1	1	$\bar{Q}$ (toggle)	

(PR, CLR) → Vcc

* T f/f → JK f/f chip منقدر نحصل عليها من خلال

[76]

$Q_A^+ = T\bar{Q} + \bar{T}Q$

J	K	Q^+
0	0	Q
1	1	$\bar{Q}$

J = K

← نفس تشبيكة الـ JK السابقة
بس بهاي الحالة الفرق إنو (J=K)

Recall

* 4 variable kmap:→

[A B C D]
↑ MSB ↑ LSB

$2^4 = 16$ combinations

$m_0 - m_{15}$

0	1	3	2
4	5	7	6
12	13	15	14
8	9	11	10

A, B, C, D

(بتمثل كرة)

* 5 variable k-map:→

[A B C D E]

$2^5 = 32$ combinations

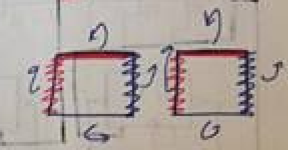
$m_0 - m_{31}$

0	1	3	2
4	5	7	6
12	13	15	14
8	9	11	10

16	17	19	18
20	21	23	22
28	29	31	30
24	25	27	26

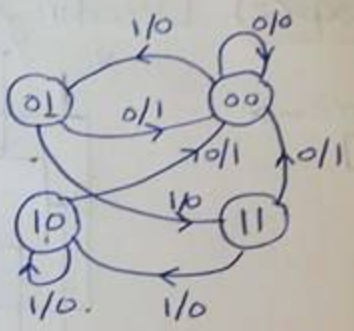
A, B, C, D, E

[ضمن الدائرة الواحدة أعداد زوجية من ال (one's)]



كرتين فوق بعض

Q_A	Q_B	x	Y	Q_A^+	Q_B^+
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	1	0	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	1	0	0
1	1	1	0	1	0



(up & down) العداد

(4)

2 seq. I/O

x/Y

comb. input

comb. output

T.T دي [state diagram] ازا جابولنا ⇐ بالنسبة لـ (state Diagram) =:

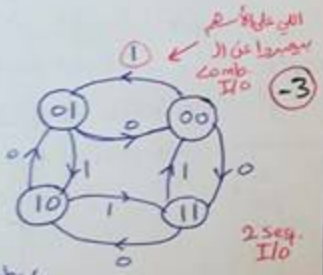
1- عدد الـ bits هوا العدائر بمثل [no. of seq input]

2- ازا كان في سهم واحد واصل فيكون العداد [up or down] مثلا عندي [combinational input]

العدائر seq بالأسهم comb.

3- ازا كان عندي سهم رايح وراجع فيكون العداد [up and down] وعندي [1 combinational input] قيمته مرة down , 0 ← ومرة up , 1 ←

4- ازا كان عندي سهم رايح وراجع والواحد منهم بيعبر عن حالتين [up and down] يعني عندي [1 combinational input + 1 combinational output]



اللي على السهم يوصلوا على الـ comb I/O

-3

2 seq. I/O

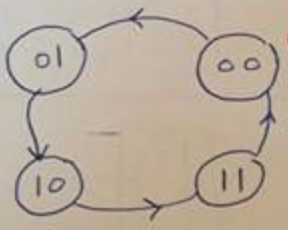
1 comb. input / العداد (up and down)

Q_A	Q_B	X	Q_A^+	Q_B^+
0	0	0	0	1
0	0	1	1	0
0	1	0	0	0
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	0
1	1	1	0	0

من الرسمة بنستنتج

توضيح

-2



2 sequential input

2 sequential output

العداد (up)

ما في داعي لـ comb input عندي

(A) Q_A	(B) Q_B	Q_A^+	Q_B^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

current state — Next state

(Ex) Design the logic CCT using D f/f for state Q_A and

[Report sheet] JK f/f for state Q_B :

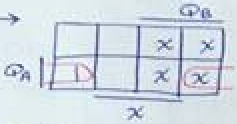
Q_A	Q_B	x	Q_A^+	Q_B^+	D_A	J_B	K_B
0	0	0	0	0	0	0	x
0	0	1	1	0	1	0	x
0	1	0	0	1	0	x	0
0	1	1	1	1	1	x	0
1	0	0	0	1	0	1	x
1	0	1	1	0	1	0	x
1	1	0	0	0	0	x	1
1	1	1	1	1	1	x	0

current state / input / next state / Excitation table

Find : D_A / J_B / K_B ?

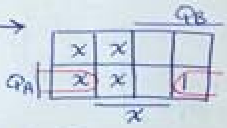
* $D_A = Q_A^+ = x$ — direct way

* J_B →



$J_B = Q_A \cdot \bar{x}$

* K_B →



$K_B = Q_A \bar{x}$

[$J_B = K_B = Q_A \bar{x}$ طلعنا إنه فعلي عبارة عن Toggle]

ملاحظة

* بالريبورت هاد أعطونا T.T جاهز من كل اشي بضل بس نوجد [K_B / J_B / D_A]

إما من ← Kmap

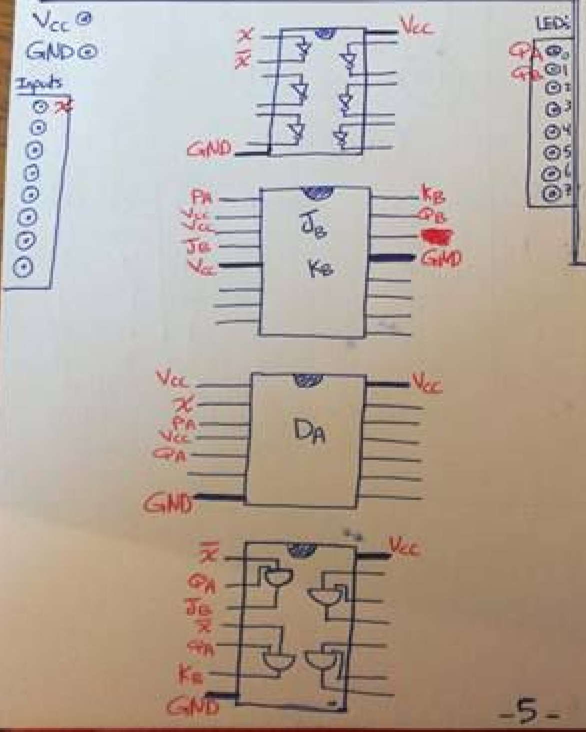
← نلاحظ إنه بنستعمل الـ inputs [direct way]

* ممكن ما يكونوا كاتبين الـ(Excitation table) فبهاي الحالة منلجأ للـ Characteristic Equ. الخاصة بكل F/F مطلوب.

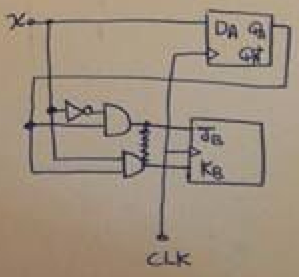
$$D_A = Q_A^+$$

$$Q_B^+ = J_B \bar{Q}_B + \bar{K}_B Q$$

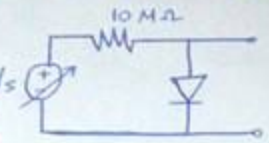
ونفس المبدأ إزا كانوا موعطينا الـ (Next states)

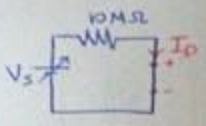


* قبل ما تشبك، ارسم اللوجيك سيركت :



Part (3): Forward Voltage → LED, diode, Zener diode





$V_s > V_\gamma$ (diode on)

$V_\gamma = 0.7V$

V_D / V_Z / V_{LED}

theoritically

* If $V_{in} = 3V$, find V_D?

(V_D) $-3 + (10M)I_D + 0.7 = 0 \rightarrow I_D = 2.3 \times 10^{-7}$

$V_D = 3 - (10 \times 10^6 \times 2.3 \times 10^{-7})$

$= 0.7$

Experimentally

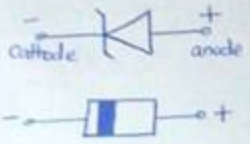
if $V_{in} = 3V$

$V_D = 0.52V$

Part (4): Reverse Voltage → LED, diode (Increase V_D with increasing V_s), zenerdiode (almost V_Z is constant with increasing V_s)

2] Zener Diode

definition ⇒

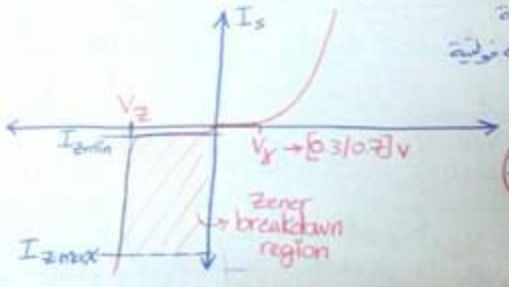


connection ⇒

① forward bias : It works as a normal diode

② reverse bias : It allows the current to pass through it, when :

- $V_s > V_z$
- $I_z < I_{zmax}$



* لحتى يمرّ الزينر دايود تيار في حالة الانحياز العكسي لازم أطبق عليه فولتية أكبر من V_z ويكون التيار الماي أقل من (I_{zmax}) وأعلى من الـ (I_{zmin})

- يعرفها من الداتا شيت (بعطاك)
- أوجدها إذا عرفت الـ P_{rated}

In this CCT, the bias type is the reverse bias

$V_s > V_z$

$I_z < I_{z,max}$

$R_s = \frac{V_s - V_z}{I_{zmax}}$

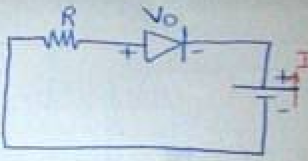
Examples ⇒ ① for the above CCT, if the zener diode works at (5V, 2W) to be using as a voltage regulator for (12V → 5V) !! ...

for $V_s = 12V > V_z(5V)$

$I_{zmax} = \frac{2W}{5V} = 400mA$

$R_s = \frac{12-5}{400m} = 17.5\,\Omega$ / يجب زيادتها أو أكبر منها. وكل ما زادت قيمتها كلما كان أمان (يعني أقل تيار أقل من الـ max) $I_{zmax} > I_z$

② Reverse Bias



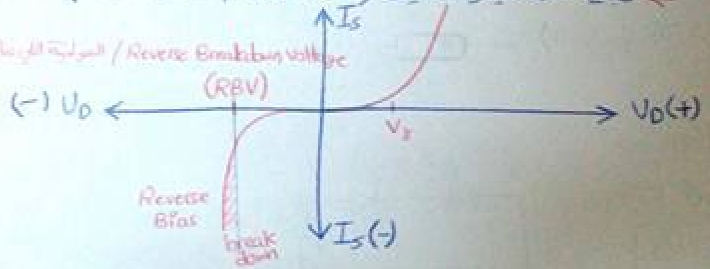
$I_s = I_D = 0$

(I_s) لما يمر التيار الخارج من البطارية من الـ − للـ + عبر الدايود

لما نوصل البطارية بهالشكل I_s ع الدايود تتجاذب الحوامل مع بعض وبالتالي تزداد الـ (depletion region) في الدايود وما بيمرّ بالدايود تيار نهائياً

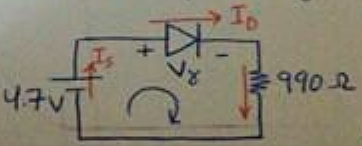
⇐ بهاي الحالة بيكون الدايود (switch opened / open CCT)

الفولتية التي بعدها يتلف الدايود ويحترق عندها / Reverse Breakdown Voltage (RBV)



Examples ⇒

ex.1 Find V_D, I_D when $V_\gamma = 0.7\,V$, $r_f = 10\,\Omega$?



Forward Bias

$R_f = 990 + 10$ (reference)

$= 1000\,\Omega$

$= 1K\Omega$

$-4.7 + 0.7 + I_D(1K) = 0$

$\boxed{I_D = 4mA} > 0$ ، يعني فرضنا صحيح Forward bias diode

$V_D = 4.7 - 990(4m) = 0.74\,V$

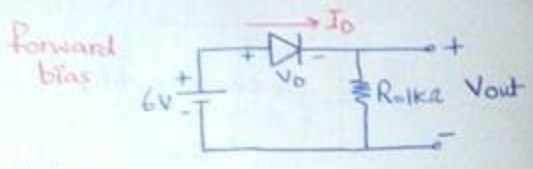
or

$= 0.7 + 10(4m) = 0.74$

ex.2] Find V_D, I_D, P_D, V_{out}, when the diode is :

a- Ideal

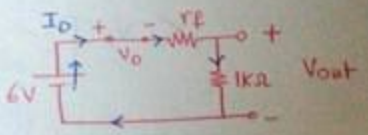
b- $V_\gamma = 0.6\,V$, $R_f = 20\,\Omega$



a) ideal diode $\rightarrow$

$V_D = 0$

(w/o r_f) $I_D = \frac{6\,V}{1K\Omega} = 6\,mA$



$P_D = I_D V_D = 0\,[W]$

$V_{out} = I_D R = (6m)(1K) = 6\,V$

b) Real diode ($V_\gamma = 0.6$)

$-6 + 0.6 + 1020\, I_D = 0 \rightarrow I_D = 5.3\,mA$

$V_D = 6 - 5.3(1) \cong 0.7\,V$ ✓

$V_{out} = I_D R = (5.3)(1) = 5.3\,V$

$P_D = I_D R_D = 5.3(1) = 5.3\,W$

If $V_s < V_\gamma$, by set $V_s = 0.5\,V$

$I_D = \frac{0.5 - 0.6}{1020} < 0$, diode is off

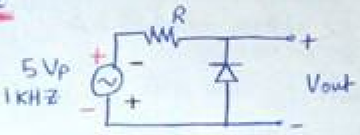
V_D , open CCT $\Rightarrow$ $-0.5 + V_D + I_D R = 0$ (open CCT)

$V_D = 0.5\,V < V_\gamma$

$I_D = 0$

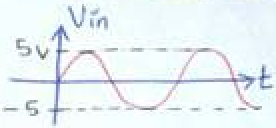
Clippers → تستخدم لقص جزء معين من الإشارة أو لقطعها عند اجتياز قيمة معينة ..

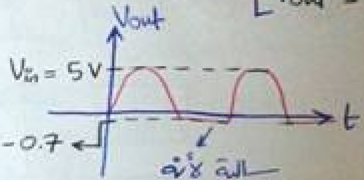
Ex



+ve half cycle → diode is off
[Vout = Vin]

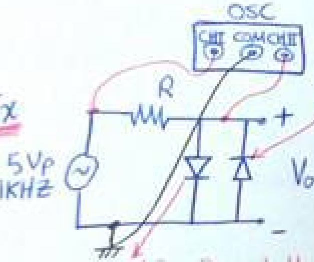
−ve half cycle → diode is on
[Vout = Vγ = 0.7V]



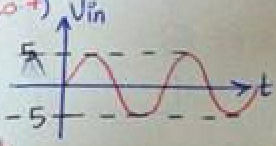


سالبة لأنه قطبية (Vout) عكس قطبية الدايود

Ex



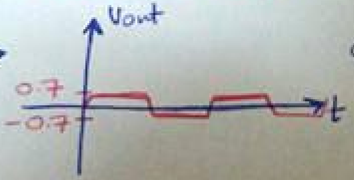
cut the −ve side of Vin at (−0.7)



CHI

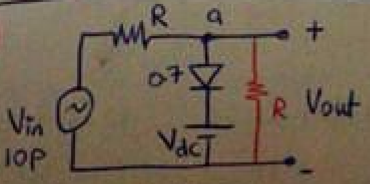
so, this will cut the +ve side of Vin at (0.7V)

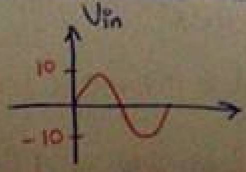
→



CHII

Ex (manual)





+ve side

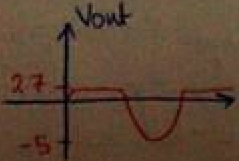
حتى يشتغل الدايود لازم يكون [redacted]

$V_a > 2.7$ إذا كانت قيمة الـ $V_{dc} = 2V$

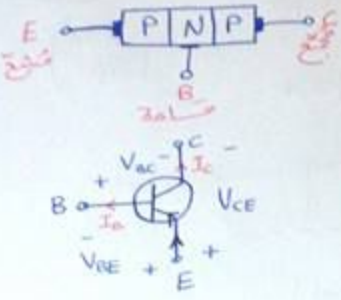
$V_{a\,min} = 2 + 0.7 = 2.7V$ ليشتغل الدايود

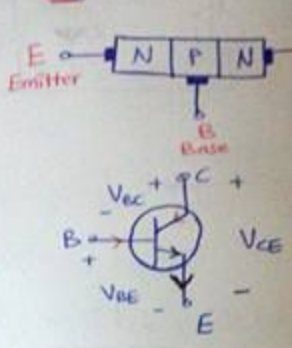
−ve side

$V_{out} = V_{in}$

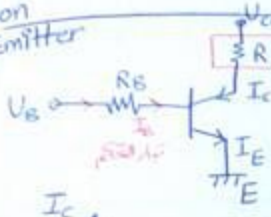


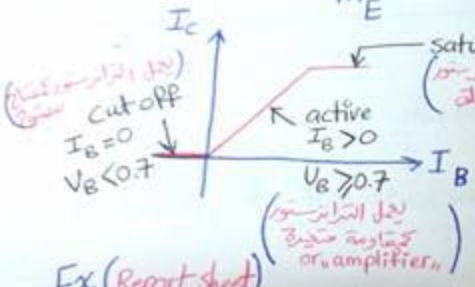
Exp(6) BJT





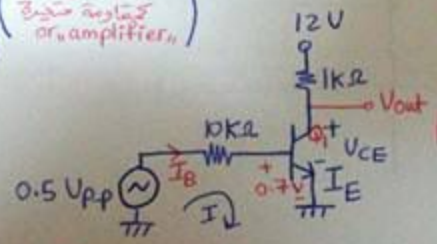
Common Emitter





$I_c = \beta I_B$ — in the active region

Ex (Report sheet)



Find V_C, V_B, V_E, I_{CQ}, I_{BQ}, I_{EQ}, V_{CEQ}, V_{BEQ} ?

$V_C = V_{CE}$

$V_E = 0$

$V_{CE} = 12 - I_c(1K\Omega)$

$= 7.62\,V$

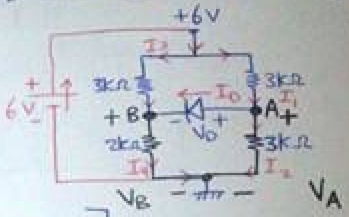
$= \frac{12 - 7.62}{1K}$

$I_{BQ} = \frac{0.47}{10K} =$

$V_{CEQ} = 7.62\,V$

$V_{BEQ} = 0.7\,V$

ex.3 Find I_D, V_D, P_D when $V_\gamma = 0.7\,V$ (si diode)



* assume diode is off

$V_{AB} = V_A - V_B$ [illegible]

Voltage regulator method

$= \frac{6 \times 3}{3+3} - \frac{6 \times 2}{3+2}$

$= 0.6\,V < V_\gamma$ [اذا فرضنا صحيح الدايود off]

$I_D = 0$

$V_D = 0.6\,V$

$P_D = 0$

→ when $V_\gamma = 0.3$ (Gr diode) / diode is on

$I_1 = I_D + I_2$

$\frac{6 - V_A}{3k} = I_D + \frac{V_A}{3k}$ → 1 $\boxed{\frac{6 - V_A}{3k} = I_D + \frac{V_A}{3k}}$

$I_4 = I_D + I_3$

2 $\boxed{\frac{V_B}{2} = I_D + \frac{6 - V_B}{3}}$

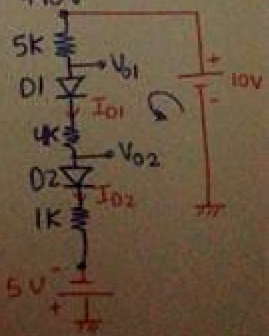
3 $\boxed{V_A = 0.3 + V_B}$

هنا طلبنا نعوض كل V_A $(0.3+V_B)$
بيصير عندي معادلتين بمجهولين
بطلع I_D و V_B
ثم V_A

---

ex.4 If $V_{\gamma 1} = 0.3\,V$, $V_{\gamma 2} = 0.7\,V$, then find:
I_{D1}, V_{D2}, V_{o1}, V_{o2}, P_{D1} ?

Forward bias



* $-10 + (5k)I_{D1} + 0.3 + (4k)I_{D1} + 0.7 + (1k)I_{D1} - 5 = 0$

$\boxed{I_{D1} = 1.4\,mA}$

$\boxed{V_{D2} = V_{\gamma 2} = 0.7\,V}$

$P_{D1} = [1.4 \times 10^{-3}] \times 0.3 = 0.42\,mW$

* $-10 + (5k)(1.4 \times 10^{-3}) + V_{o1} = 0 \rightarrow \boxed{V_{o1} = 3V}$

$-10 + (5 \times 1.4) + 0.3 + (4 \times 1.4) + V_{o2} = 0 \rightarrow \boxed{V_{o2} = -2.9V}$

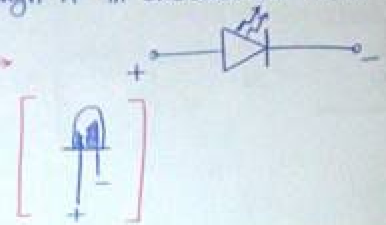
$-V_{o2} + 0.7 + (1 \times 1.4) - 5 = 0$ ← أو بأخذ اللوب التحتية

$(V_{o2} = -2.9V)$

3] LED, it's a PN Junction that allows the current to pass through it in one direction with a light

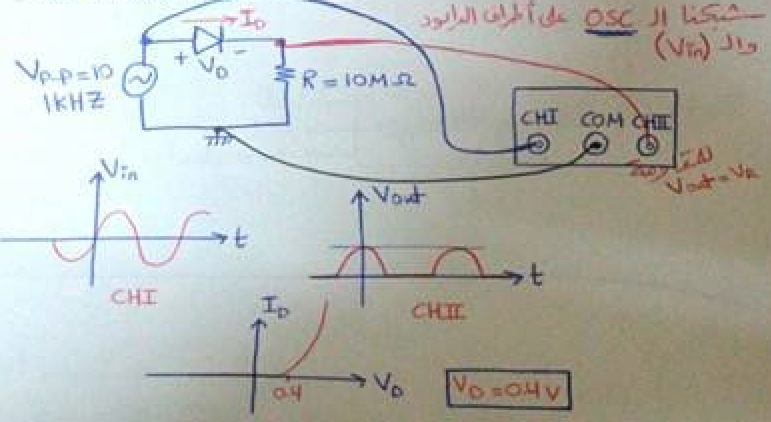
schematic →

form →

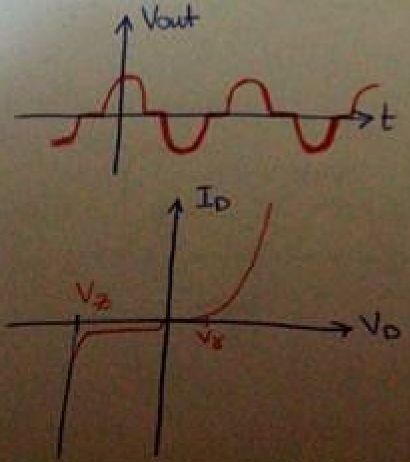


Report Sheet

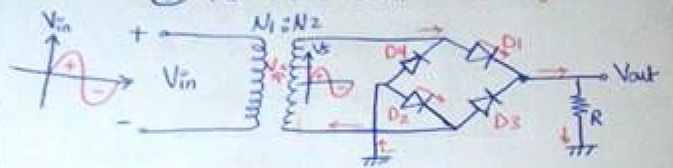
Part(1): Diode characteristic Curve



Part(2): Zener diode characteristic curve (نفس السيركت اللي فوق)



② Full wave rectifier: (bridge rectifier)

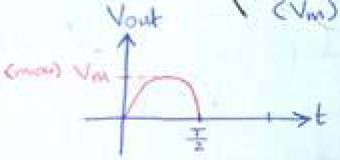


هو نوع آخر ، بيحتوي على
دايودز لكنه بيحتاج 2 لحمل
center tapped
(غير علي)

* during +ve half cycle → D_1/D_2 is on
D_3/D_4 is off

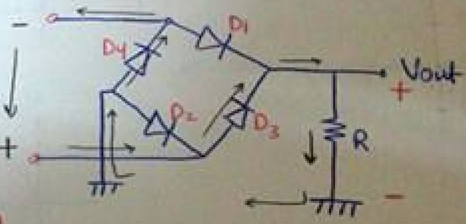
$[I_R = I_{D_1} = I_{D_2}]$ causing $V_{out} = I_D R$

KVL: $V_{out} = V_s - 2V_\gamma$
$V_{out,max} = V_{sp} - 2V_\gamma$ (V_m) , $I_D = \frac{V_s - 2V_\gamma}{R}$



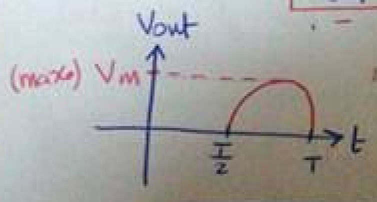
$V_{avg} = \frac{V_m}{\pi}$

* during −ve half cycle →



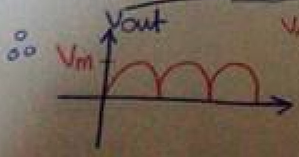
D_3/D_4 is on
D_1/D_2 is off

$[I_R = I_{D_3} = I_{D_4}]$ causing $V_{out} = I_D R$

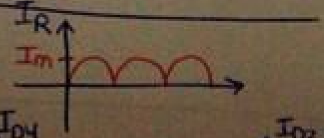


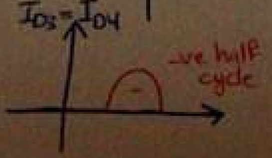
Peak inverse voltage (PIV) $= V_{sp} - V_\gamma$

∴

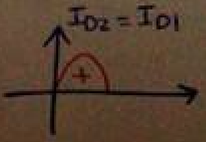


$V_m = V_{sp} - 2V_\gamma$





−ve half cycle

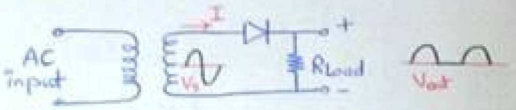


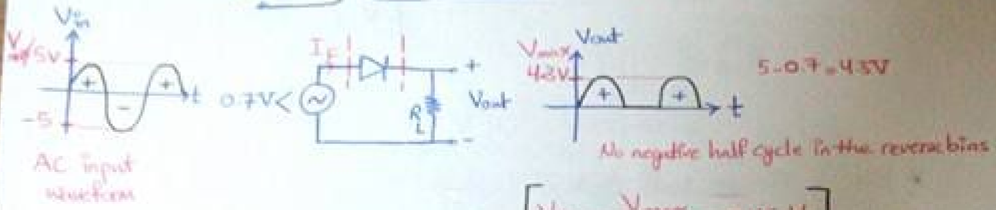
+ve half cycle

Exp(5) Diodes' Applications (rectifiers)

Rectifiers → an electrical device that converts alternating current (AC) to direct current (DC).

① Half wave rectifier :



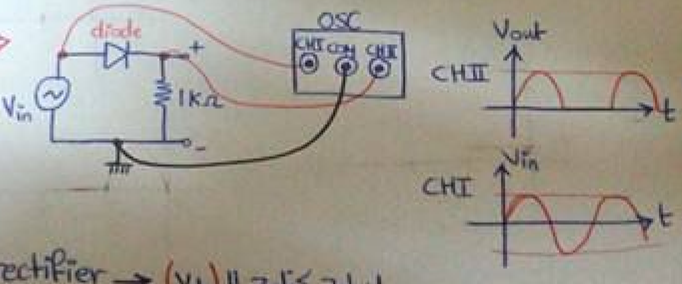


$$\left[V_{dc} = \frac{V_{max}}{\pi} = 0.45\, V_s\right]$$

note

V_{out} Lagg V_{in} ، لأنه الـ Vout مستنيا ع بين ما V_{in} تصير فولتيتها أكبر من 0.7V ليشتغل الدايود

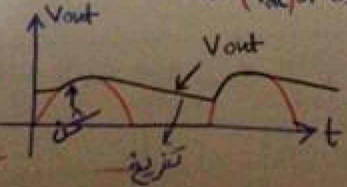
In the report sheet ⇒

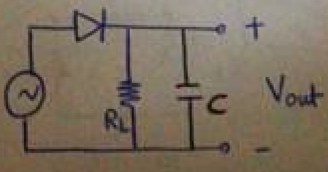


Filtered half wave rectifier → زيادة كفاءة الـ (V_{dc})

هيحسن من الـ Vdc

$$\left[r = \frac{V_r}{V_{avg}}\right] \text{ ripple factor}$$

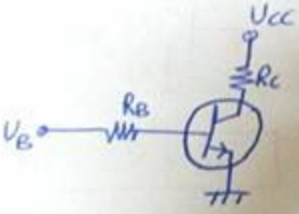




* لو قللنا قيمة R_L مستهلك تيار أكبر كلما زاد الـ ripple لل Vdc

∴ حتى أحصل ع (V_{out}) أقرب ما يكون لل dc بزيد قيمة (R_L) وسعة (المواسع)

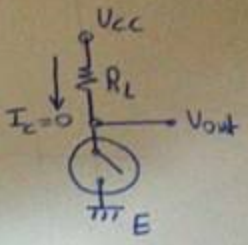
Transistor as switch → saturation region
on ↙ ↘ off



* Switch open :

when $I_B = 0$

$$V_{out} = V_{cc}$$

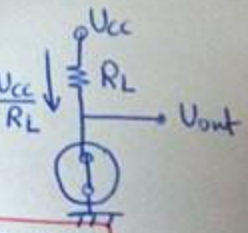


* Switch closed :

at $I_B|_{sat}$

I_c (sat)

$$I_c = \frac{V_{cc}}{R_L}$$



$$V_{out} = V_{CE} = V_{cc} = 0.2 \cong 0V$$

= Saturation JL

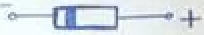
Logic and Digital Electronics Lab.

Exp(4) Diode types and Characteristics

- diode (real, ideal)
- Zener diode
- LED

1) definition ⇒

يسمح الدايود بمرور التيار في اتجاه واحد فقط ... من الـ ⊕ للـ ⊖

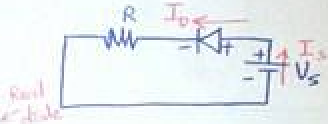


(الطرف المظلل فيه يمثل طرف الـ -)

Connections ⇒

① Forward Bias

when $[V_s > V_D]$



$V_D = 0.7$, Si

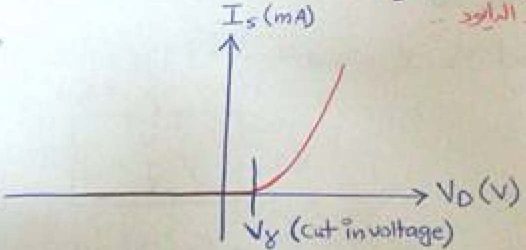
$= 0.3$, Gr

ويكون I_s عم يمر من الـ + للـ -

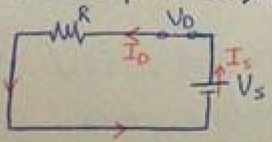
عبر الدايود

$I_D = I_s = I_{max}$

لعدم تكون الفولتية اللازمة على الدايود (فولتية البطارية) أكبر من حد الدايود (V_γ) لأن تقدر تتغلب على الـ [depletion region] ويمر التيار عبر الدايود ..



⇐ بهاي الحالة، الدايود بيكون (switch closed / short CCT)



ملاحظة

diode is on ⇐ $[I_D > 0]$ ⇐ $[V_s > V_\gamma]$

diode is off ⇐ $[I_D < 0]$ ⇐ $[V_s < V_\gamma]$

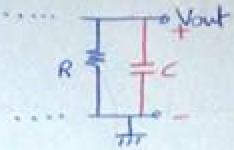
so $I_D = 0$

open CCT, $V_D < V_\gamma$

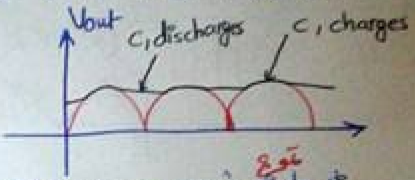
Forward Bias

اذا كان التيار عم يمر من ⊕ ⇐ ⊖ عبر الدايود لكن قيمة التيار سالبة أو جهد البطارية أقل من V_γ بيكون الدايود $I_D = 0$, off

open CCT



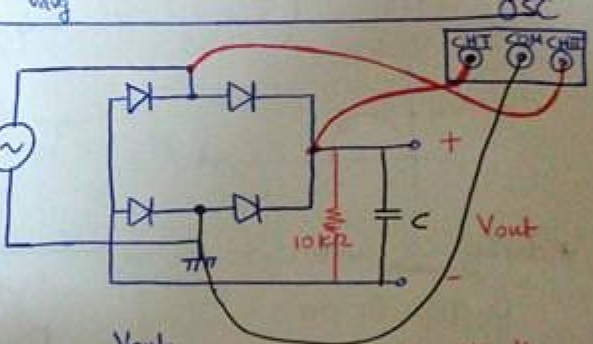
← كل ما Vout أقرب ما تكون لل Vdc

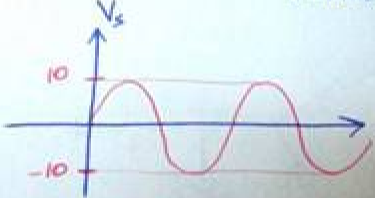


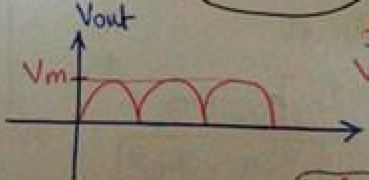
في ripple (تموج) شوي ومدى وجودها بالسيجنال بيعتمد بقيمة (المقاومة)
كل ما قللنا قيمة ال [ripple] رح تكون Vout أقرب لل Vdc

* ripple voltage $(V_r) = \frac{V_m}{2fCR}$ (f: frequency), the voltage between charge & discharge.
* ripple factor $= \frac{V_r}{V_{avg}}$

In the report sheet →







theoritically
$V_m = 10 - 2(V_\gamma)$
$= 10 - (2*0.7)$
$= 8.6\ V$

غالبا مطلع أقل بشوي

→ when adding the Capacitor (1 μF)
the ripple voltage $(V_r) = \frac{V_m}{2(1K)(1\mu)(10K)}$ ← القيمة من ال OSC CH1 علي

لما نزيد مقدار المواسعة بيقل ال (V_r) $\left[V_r \propto \frac{1}{C}\right]$ / عكسي