ElCoM
ELECTRICAL COMPUTER MECHATRONICS

تقدم لجنة ElCoM الاكاديمية

دفتر لمادة:

منطق رقمي والكترونيات رقمية

جزيل الشكر للطالبتين:

رؤى وماريا

First Logic :

بسم الله الرحمن الرحيم

RoAA IKbarich

number system.

- Decimal system (10)
- Binary system (2)
- Hexa system (16)
- Octal system (8)

1 Decimal system:- (10)

0 $1_{(10)}$ 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 ----

2 Binary system : (2)

0 $1_{(2)}$ 10 11 100 101 110 111 1000 1001 1010 1011 1100
1101 1110 1111 ----

3 Octal system : (8)

0 $1_{(8)}$ 2 3 4 5 6 7 10 11 12 13 14 15 16 17 20 21 22 23
24 25 26 27 30 ----- 67 70 ·· 100 -----

* 77 100

4 Hexa system : (16)

0 $1_{(16)}$ 2 3 4 5 6 7 8 9 A B C D E F 10 11 12 13 14 15 16 17 18
19 1A 1B 1C 1D 1E 1F ····· 99 9A 9B 9C 9D 9E 9F 100 ···

-* Conversion From Hexa to decimal:

* Hexa (16) → decimal (10)

① $A0_{16}$: $160_{(10)}$

$A_{(16)} = 16^1$, $0_{(16)} = 16^0$

$A_{(10)} = 10$, $0_{(10)} = 0$ ⇒ $16^1 * 10 + 16^0 * 0 = \underline{\underline{160}}$

② $ABCD_{16}$: $43981_{(10)}$

$A_{(16)} = 16^3$, $B_{(16)} = 16^2$, $C_{(16)} = 16^1$, $D_{(16)} = 16^0$

$A_{(10)} = 10$, $B_{(10)} = 11$, $C_{(10)} = 12$, $D_{(10)} = 13$

$16^3 * 10 + 16^2 * 11 + 16^1 * 12 + 16^0 * 13 = \underline{\underline{43981}}$

③ $0.A3_{(16)} = 0.636_{(10)}$

$A_{(16)} = 16^{-1}$, $3_{(16)} = 16^{-2}$ ⇒ $16^{-1} * 10 + 16^{-2} * 3 = 0.636$

$A_{(10)} = 10$, $3_{(10)} = 3$

④ $2B.07_{(16)} = 43.02_{(10)}$

2B

$2_{(16)} = 16^{1}$, $B_{(16)} = 16^{0}$ ⇒ $16^{1} * 2 + 16^{0} * 11 = 43$

$2_{(10)} = 2$, $B_{(10)} = 11$

.07

$0_{(16)} = 16^{-1}$, $7_{(16)} = 16^{-2}$ ⇒ $16^{-1} * 0 + 16^{-2} * 7 = .02$

$0_{(10)} = 0$, $7_{(10)} = 7$

Conversion From Binary to Decimal:

* Binary (2) → Dicimal (10)

① $10111_{(2)} = 23_{(10)}$

$1 * 2^{0} + 1 * 2^{1} + 1 * 2^{2} + 0 * 2^{3} + 1 * 2^{4} = 23$

② $110.0011_{(2)} = 6.1875_{(10)}$

$0 * 2^{0} + 1 * 2^{1} + 1 * 2^{2} + 0 * 2^{-1} + 0 * 2^{-2} + 1 * 2^{-3} + 1 * 2^{-4} = 6.1875$

Conversion From octal to Decimal :-

* octal (8) → Decimal (10)

① $36_{(8)} = 30_{(10)}$

$3_{(8)} = 8^{1}$, $6_{(8)} = 8^{0}$ ⇒ $8^{1} * 3 + 8^{0} * 6 = 30$

$3_{(10)} = 3$, $6_{(10)} = 6$

② $2.07_{(8)} = 2.125_{(10)}$

$2_{(8)} = 8^{0}$, $0_{(8)} = 8^{-1}$, $7_{(8)} = 8^{-2}$ ⇒ $8^{0} * 2 + 8^{-1} * 0 + 8^{-2} * 7 = 2.125$

$2_{(10)} = 2$, $0_{(10)} = 0$, $7_{(10)} = 7$

③ $38_{(8)} =$

لا يوجد لانه داخل نظام ال octal

لا يوجد لا 8 ولا 9.

Conversion From Decimal to Binary :

Decimal (10) → Binary (2)

① $6_{(10)} = 110_{(2)}$

* قسمة كل 2

6	
3	0 → Lost signifcant bit
1	1
0	1 → most signifcant bit

↑

② $.25_{(10)} = .01_{(2)}$

* الضرب بـ 2

.25	
.5	0 → most signifcant bit
1.0	1 → lost signifcant bit

↓

③ $.2_{(10)} = .0011_{(2)}$

.2	
.4	0 msb
.8	0
.6	1
.2	1 Lsb

↓

دوري
بوقف

④ $6.2_{(10)} = 110.0011_{(2)}$

$6_{(10)}$ $110_{(2)}$

6	
3	0 LSb
1	1
0	1 msb

↑

ضرب 2

$.2_{(10)} = .0011_{(2)}$

.2	
.4	0
.8	0
.6	1
.2	1

msb ↓ Lsb

تقسيم 2

Conversion From Decimal to octal :-

Decimal (10) → octal (8)

① $83_{(10)} = 123_{(8)}$

83	
10	3 Lsb
1	2
0	1 msb

↑

نقسم كل 8

② $.0625_{(10)} = .04_{(8)}$

.0625	
.5	0 msb
0	4 Lsb

↓

نضرب بـ 8

③ $83.0625_{(10)} = 123.04_{(8)}$

83	
10	3 Lsb
1	2
0	1 msb

↑

.0625	
.5	0 msb
0	4 Lsb

↓

Converglont From Decimal to Hexa:-

① $69_{(10)} = 45_{(16)}$

69	
4	5 Lsb ↑
0	4 msb

نقسم على 16

② $.01325_{(10)} = .08_{(16)}$

.01325	
.5	0 msb ↓
0	8 Lsb

⇒ نضرب ب 16

Decimal → Hexa
(10) (16)

③ $69.01325_{(10)} = 45.08_{(16)}$.

Octal to Binary

0 → 000
1 → 001
2 → 010
3 → 011
4 → 100
5 → 101
6 → 110
7 → 111

3bit

Hexa to binary

0 → 0000
1 → 0001
2 → 0010
3 → 0 011
4 → 0 100
5 → 0 101
6 → 0 110
7 → 0 111
8 → 1000
9 → 1001
A → 1010
B → 1011
C → 1100
D → 1101
E → 1110
F → 1111

→ 4 bit

Note:-
octal to Hexa
or Hexa to octal:
Octal to binary to Hexa
Hexa to binary to octal

Conversion from binary to octal:

binary → octal
(2) (8)
3 bit

① $011011_{(2)} = 33_{(8)}$

$\underbrace{011}_{3}\ \underbrace{011}_{3}$

② $1.1_{(2)} = 1.4_{(8)}$

$\underbrace{001}_{1}\ \underbrace{100}_{4}$

Conversion From Octal to binary:

Octal → binary
(8) (2)
3 bit

① $7.3_{(8)} = 111.011_{(2)}$

② $3.06_{(8)} = 011.000110_{(2)}$

③ $12.17_{(8)} = 001010.001111_{(2)}$

Conversion From binary to Hexa:

binary → Hexa
(2) (16)

$\boxed{4\text{ bit}}$

① $0101 : 11011000_{(2)} = 5.D8_{(16)}$

$$\underbrace{0101}_{5}\ \underbrace{1101}_{D}\ \underbrace{1000}_{8}$$

② $0110.0100_{(2)} = 6.4_{(16)}$

$$\underbrace{0110}_{6}\ \underbrace{0100}_{4}$$

Conversion From Hexa to binary:

Hexa → binary
(16) (2)

4 bit

① $5BC_{(16)} = 0101\ 1011\ 1100_{(2)}$

② $43.BF_{(16)} = 0100\ 0011 . 1011\ 1111_{(2)}$

Conversion From octal to Hexa:

$\boxed{241.570_{(8)} = A1.BC_{(16)}}$

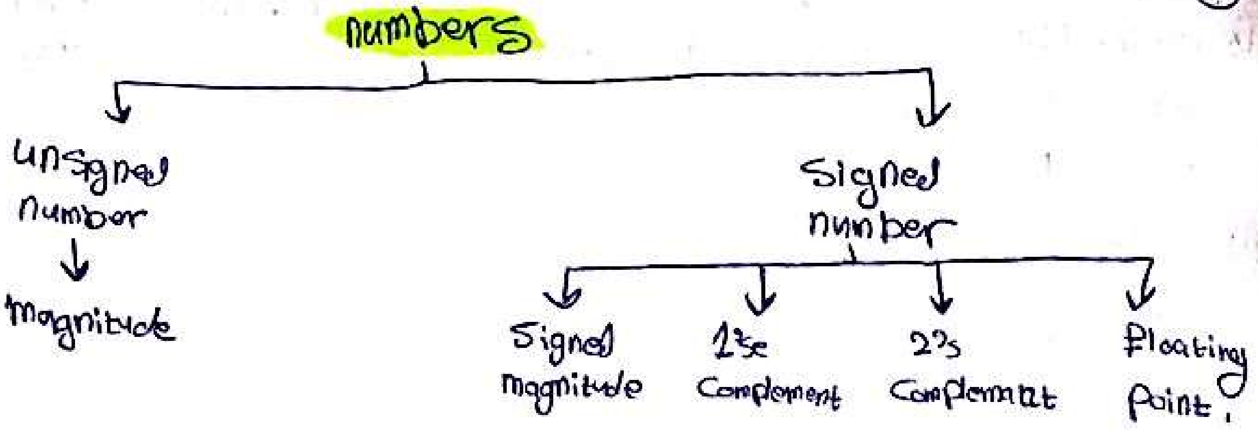
$241.570_{(8)} = 010\ 100\ 001 . 101\ 111\ 000_{(2)}$

* octal → binary → Hexa
(8) (2) (16)

$010100001 . 101111000_{(2)} =$

1010 = A
0001 = 1
1011 = B
1100 = C

⇒ $A1.BC_{(16)}$



Complement:

1. First Complement:- (1's Complement): $0 \rightarrow 1$, $1 \rightarrow 0$

Example: Find the First complement:-

110 → 001
1001 → 0110
10101 → 01010
1111 → 0000

2. Second Complement:- (2's Complement):

1's complement + 1 = 2's complement.

Example: Find 2's Complement :-

$1001 \xrightarrow{1's} 0110 + 1$

$\boxed{0111}$ → 2's complement.

OR: Constant Leading number and 1's Complement:

Example:-

$110110\boxed{1} \rightarrow 001001\boxed{1}$

$\boxed{1}0000 \rightarrow \boxed{1}0000$

$1\boxed{1}0000 \rightarrow 0\boxed{1}0000$

$10100\boxed{1} \rightarrow 01011\boxed{1}$

$110\boxed{1} \rightarrow 001\boxed{1}$

$100\boxed{1} \rightarrow 01\boxed{1}$

The purpose of Complement is to convert Substraction operation to addition operation.

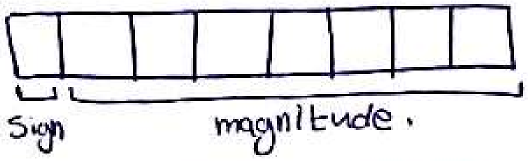
number representation For digital numbers

① Sign-magnitude representation:-

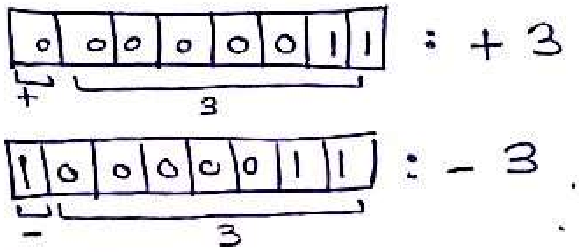
الإشارة :

0 → + sighn
1 → - sigh

8 bits



Example: represent [+3] and [-3] using 8bits sign magnitude



Example: 4Bits sign magnitude representation:-

① -2 : 1 0 1 0
② +6 : 0 1 1 0
③ -7 : 1 1 1 1
④ +7 : 0 1 1 1

(Note) for 4Bit maximum number for magnitude 7 OR -7

Sign number Representation :-

1. sign magnitude Representation → محجوزة لل Sign ▨

2. 1's complement :-

Positive number → Same as binary.

Negative number → First Complement of binary number.

Example:- Sign Represent the Following using First Complement in 4Bit system:-

+3 : 0011   +4 : 0100

-3 : 1100   -4 : 1011

3. Second complement:-

Positive number → take binary only.

Negative number → 2's complement the binary number.

Example:- Representation the Following number using 2's representation in 4Bit and 8bit system:-

	4Bit	8 bit.
+3	0011	00000011
−3	1101	11111101
+4	0100	00000100
−4	1000	11111100

Note: Computers use 2's Complimement For number representation to Convert subtraction operation.

Example: in 4Bit Find:-

1. 4 0100
+ 3 0011
+7 0111

2. +4 0100
−3 1101
+1 0001

3. +3 0011
−4 1100
−1 1111
⇓
Sign = −
Value = 2's Complem
$1111 \xrightarrow[2's]{} 0001$

Range of signal number:-

① sign magntude
② First Complemant → $-(2^{n-1}-1)$, $+(2^{n-1}-1)$
③ Second Complemant → $-(2^{n-1})$, $+(2^{n-1}-1)$

Example:- Find the Range of 4Bit sign number For All 3 sys:

sign magntude and First complemant : n = 4 :

$-(2^{4-1}-1) \,/\, +(2^{4-1}-1) \Rightarrow \boxed{-7 \text{ to } 7}$

Second Complemant n = 4 :

$-2^{4-1} \,/\, +(2^{4-1}-1) \Rightarrow \boxed{-8 \text{ to } 7}$

Example:- Represent the following in 4Bit system in at three system:- ⑨

number	sign	1's Complemant	2's complemant
+3	0011	0011	0011
-3	1011	1100	~~000~~ 1101
0	0000	0000	0000
1	0001	0001	0001
-1	1001	1110	1111
-8	not Valid	not Valid	1000

Code:-

Binary Coded decimal (BCD)

Decimal	BCD
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

Digit এর জন্য 4 Bit লাগে *
এর জন্য Bit এর Decimal এর
Digital Decimal.

Example:- express the following Decimal number in BCD.

Decimal	BCD	
$3_{(10)}$	0011	1 Digit.
$23_{(10)}$	0010, 0011	2 Digit.
$101_{(10)}$	0001, 0000, 0001	3Digit

Gray Code	decimal equivelant
0	0000
1	0001
2	0011
3	0010
4	0110
5	0111
6	0101
7	0100
8	1100
9	1101

Boolean Gates:

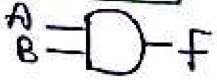
① AND Gate:-

Circut:

truth table

A	B	F
0	0	0
1	1	1
0	1	0
1	0	0

Symbol



A,B : input
F : output

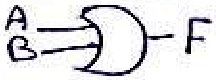
② OR Gate:

Circut:

truth table:-

A	B	F
0	0	0
1	0	1
0	1	1
1	1	1

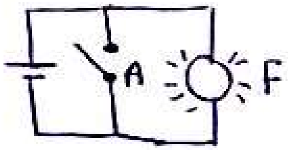
Symbol:



A,B: input
F: output.

③ Not Gate:-

CirCuit:



truth table

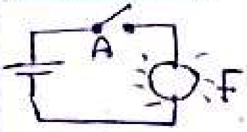
A	F
0	1
1	0

Symbol

A: input
F: output

④ Buffer Gate:-

Circut:-



truth table

A	F
0	0
1	1

Symbol:

A: input
F: output.

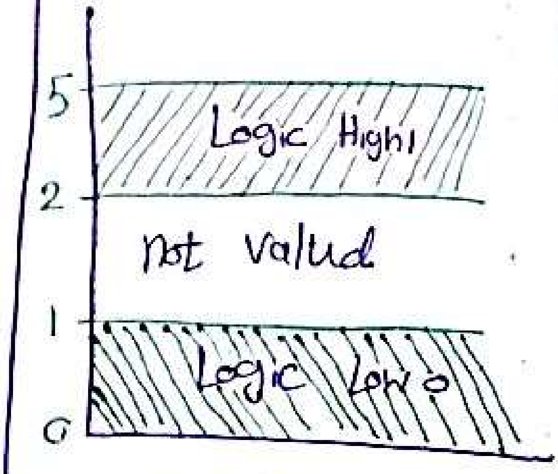
Note:-

1. Folting Follower ↑ input ↓ output.
2. bubble $\xrightarrow{\text{يعني}}$ not أداة
3. $F = A \cdot B$, AB] → AND ~~Ba~~ opolater

   F = A+B → OR oporater.

   F = A' → Not operator.

   F = A → Buffer operator.



threshold منطقة.

Boolean Theorems and Properties.

1) * aclosure with respect the operator OR (+)
   * aclosure with respect the operator AND (·)

2) * An identity element with respect +

$$X+0=0+X=X$$

   * An identity element with respect ·

$$X\cdot 1=1\cdot X=X$$

3) * Commutative with respect to +

$$X+Y=Y+X$$

   * Commutative with respect to ·

$$X\cdot Y=Y\cdot X$$

4) * · is distributive over +

$$X\cdot(Y+Z)=(X\cdot Y)+(X\cdot Z)$$

   * + is distributive over ·

$$X+(Y\cdot Z)=(X+Y)\cdot(X+Z)$$

5) * $X+X'=1$
   * $X\cdot X'=0$ ← $\boxed{: X' : \text{is a 1's complemant}}$

---

theorem $\boxed{1}$:-

$\boxed{a}$

$$\begin{aligned} X+X &= (X+X)\cdot 1 \\ &= (X+X)(X+X') \\ &= XX+XX'+XX+XX' \\ &= XX+XX' \\ &= X+0 \\ &= \boxed{X} \end{aligned}$$

$\boxed{b}$

$$\begin{aligned} X\cdot X &= (X\cdot X)+0 \\ &= (X\cdot X)+(X\cdot X') \\ &= X(X+X') \\ &= X\cdot 1 \\ &= \boxed{X} \end{aligned}$$

theorem [2] :-

[a] $X + XY = X \cdot 1 + (XY)$

$= (X \cdot (X + X')) + (XY)$

$= X(1 + Y)$

$= X \cdot 1$

$= \boxed{X}$

[b] $X(X+Y) = (X+0)(X+Y)$

$= XX + 0 \cdot X + XY + 0 \cdot Y$

$= XX + XY +$

$= \boxed{X}$

theorem [3] :-

- $X + (Y + Z) = (X + Y) + Z$
- $X + (y + x) = x + (x + y)$
- $x(yz) = (xy)z$ Associative
- $x(y + z) = xy + xz$
- $x + (y \cdot z) = (x + y) \cdot (x + z)$

⊛ Demorgan theorem:-

- $(x + y)' = x' \cdot y'$
- $(x \cdot y)' = x' + y'$

Example: Apply Demorgan theorm on the Following:

ⓐ $\overline{(A' \cdot B')} = A'' + B'' = A+B$

ⓑ $(A' \cdot B)' = A'' + B' = A + B'$

ⓒ $\overline{A+B+C} = A' \cdot B' \cdot C'$

ⓓ $\overline{ABC} = A' + B' + C'$

ⓔ $\overline{A \cdot (B+C)} = A' + (B+C)' = A' + (B' \cdot C')$

ⓕ $\overline{(A \cdot C) + (A \cdot B)} = \overline{(A \cdot C)} \cdot \overline{(A \cdot B)} = (A'+C') \cdot (A'+B')$

$= A' + A'B' + A'C' + B'C' = A' + B'C'$

Ⓖ $\overline{AB} + \overline{CD} = A'+B'+C'+D'$

Ⓗ $\overline{AB+CD} = \overline{AB} \cdot \overline{CD} = (A'+B') \cdot (C'+D')$.

Ⓘ $(A+\overline{B}) \cdot (\overline{C}+D) = \overline{(A+\overline{B})} + \overline{(C'+D)} = (A' \cdot B'') + (C'' \cdot D')$

$= (A' \cdot B) + (C \cdot D')$

ⓞ $\overline{A \cdot (B+C)} = A' + \overline{(B+C)} = A' + (B' \cdot C')$

~~Example~~:

Example:- Simplify using Bolean properties and theorms.-

* 1 $A(A+B) = AA + AB = A + AB = A(AB) = A(1\cdot B)$

$A\cdot 1 = \boxed{A}$

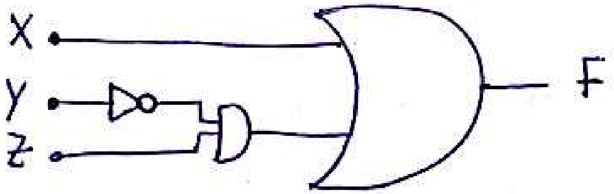
2 $A(\bar{A}+AB) = AA' + AAB = 0 + AB = \boxed{AB}$

3 $BC + B'C = C[B+B'] = C[1] = \boxed{C}$

4 $A(A+A'B) = AA + AA'B = A + 0\cdot B = A + 0 = \boxed{A}$

Truth tuble

$2^3 = 8$



X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

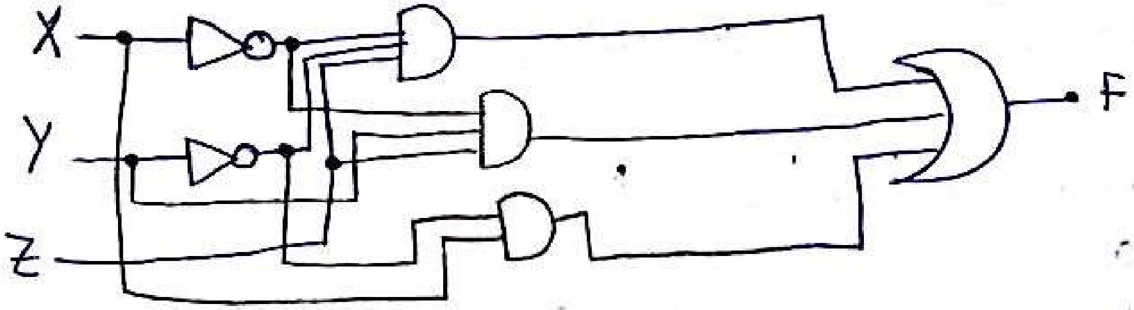
$X + (Y'\cdot Z) = F(x,y,z)$

* $\overline{A\cdot(B+C)} =$

$A' + \overline{(B+C)} =$

$A' + (B'\cdot C')$

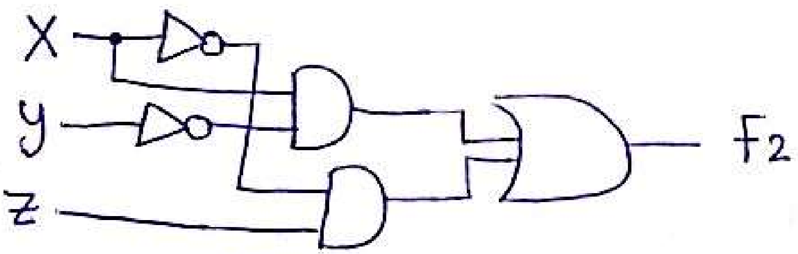
Example:- $F_2 = x'y'z + x'yz + xy'$



$$F_2 = x'y'z + x'yz + xy' =$$

$$= x'z(y'+y) + xy'$$

$$= x'z \cdot 1 + xy' = \boxed{x'z + xy'} = F_2$$



truth table:- $\boxed{2^3 = 8}$

x	y	z	F_2	$x' \cdot z$	$x \cdot y'$
0	0	0	0	0	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	1	1	1	0
1	0	0	1	0	1
1	0	1	1	0	1
1	1	0	0	0	0
1	1	1	0	0	0

Minterms and Maxterms

minterms ⇒ m
Maxterm ⇒ M

when $2^3 = 8$ The binary number From 0 to 8

Number	X	Y	Z	Minterm Term	Minterm Designation	Max term Term	Max term Designation
0	0	0	0	$\dot{x}\dot{y}\dot{z}$	m_0	$x+y+z$	M_0
1	0	0	1	$\dot{x}\dot{y}z$	m_1	$x+y+\dot{z}$	M_1
2	0	1	0	$\dot{x}y\dot{z}$	m_2	$x+\dot{y}+z$	M_2
3	0	1	1	$\dot{x}yz$	m_3	$x+\dot{y}+\dot{z}$	M_3
4	1	0	0	$x\dot{y}\dot{z}$	m_4	$\dot{x}+y+z$	M_4
5	1	0	1	$x\dot{y}z$	m_5	$\dot{x}+y+\dot{z}$	M_5
6	1	1	0	$xy\dot{z}$	m_6	$\dot{x}+\dot{y}+z$	M_6
7	1	1	1	xyz	m_7	$\dot{x}+\dot{y}+\dot{z}$	M_7

Example:-

	x	y	z	F_1	F_2
0	0	0	0	0	0
1	0	0	1	1	0
2	0	0	0	0	0
3	0	1	1	0	1
4	1	0	0	1	0.
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1

① minterm F_1

$F_1 = \dot{x}\dot{y}z + x\dot{y}\dot{z} + xyz = m_1 + m_4 + m_7$

② minterm F_2

$F_2 = \dot{x}yz + x\dot{y}z + xy\dot{z} + xyz$

$= m_3 + m_5 + m_6 + m_7$

③ Complemant minterm F_1

$F_1' = \dot{x}\dot{y}\dot{z} + \dot{x}y\dot{z} + \dot{x}yz + x\dot{y}z + xy\dot{z}$

$= m_0 + m_2 + m_3 + m_5 + m_6$

④ Complemant minterm F_2

$F_2' = \dot{x}\dot{y}\dot{z} + \dot{x}\dot{y}z + \dot{x}y\dot{z} + x\dot{y}\dot{z}$

$= m_0 + m_1 + m_2 + m_4$

⑤ maxterm F_1:

$F_1 = (x+y+z)(x+\dot{y}+z)(x+\dot{y}+\dot{z})(\dot{x}+y+\dot{z})(\dot{x}+\dot{y}+z)$

$= M_0 M_2 M_3 M_5 M_6$

⑥ Complemant maxterm F_1:-

$F_1' = (x+y+\dot{z})(\dot{x}+y+z)(\dot{x}+\dot{y}+\dot{z})$

$= M_1 M_4 M_7$

⑦ Maxterm F_2:

$F_2 = (x+y+z)(x+y+\dot{z})(x+\dot{y}+z)(\dot{x}+y+z)$

$= M_0 M_1 M_2 M_4$

⑧ Complemant Maxterm F_2:-

$F_2' = (x+\dot{y}+\dot{z})(\dot{x}+y+\dot{z})(\dot{x}+\dot{y}+z)(\dot{x}+\dot{y}+\dot{z})$

$= M_3 M_5 M_6 M_7$

Example:- Express the Boolean function (F) in a sum of minterm the function has 3 Varibles A, B, C

$F = A + B'C$:

$F = A(B+B') = AB + AB' + B'C$

$F = AB(C+C') + AB'(C+C') + B'C(A'+A)$

$= ABC + ABC' + AB'C + AB'C' + B'CA' + B'CA$

$F(ABC) = ABC + ABC' + AB'C + AB'C' + A'B'C + AB'C$

$= 111 + 110 + 101 + 100 + 001 + 101$

$= m_7 + m_6 + m_5 + m_4 + m_1 + m_5$

$= m_1 + m_4 + m_5 + m_6 + m_7$

$= A'B'C + AB'C' + AB'C + ABC' + ABC$

Sum of min term $F(A,B,C) = \Sigma(m_1 + m_4 + m_5 + m_6 + m_7)$

m_0	000
m_1	001
m_2	010
m_3	011
m_4	100
m_5	101
m_6	110
m_7	111

Example:- $F = A + B'C$ ~~minterm~~ in truth table ↑

A	B	C	F	number
0	0	0	0	m_0
0	0	1	1	m_1
0	1	0	0	m_2
0	1	1	0	m_3
1	0	0	1	m_4
1	0	1	1	m_5
1	1	0	1	m_6
1	1	1	1	m_7

Complement minterm:- of function:-

$A'B'C' + A'BC' + A'BC$

$m_0 + m_2 + m_3$

Example: $F(A, B, C, D) = AB'C + ACD + A'B'D' + A'D$

* $AB'C(D+D') = AB'CD + AB'CD' = 1011 + 1010$

$\Rightarrow \boxed{m_{11} + m_{10}}$

* $A(B'+B)CD = AB'CD + ABCD = 1011 + 1111$

$\Rightarrow \boxed{m_{11} + m_{15}}$

* $A'B'(C+C')D' = A'B'CD' + A'B'C'D' = 0010 + 0000$

$\Rightarrow \boxed{m_2 + m_0}$

* $A'(B+B')(C+C')D = A'BCD + A'BC'D + A'B'CD + A'B'C'D$

$= 0111 + 0101 + 0011 + 0001 \Rightarrow \boxed{m_1 + m_3 + m_5 + m_7}$

$F(A, B, C, D) = \sum (m_0 + m_1 + m_2 + m_3 + m_5 + m_7 + m_{10} + m_{11} + m_{15})$

Complemand oR Max Term oR Product of sum

~~[illegible]~~

$F(A, B, C, D) = (M_4 \cdot M_6 \cdot M_8 \cdot M_9 \cdot M_{12} \cdot M_{13} \cdot M_{14})$

$= \prod (4, 6, 8, 9, 12, 13, 14)$

$F = (A+B'+C+D)(A+B'+C'+D)(A'+B+C+D)(A'+B+C+D')(A'+B'+C+D)(A'+B'+C+D')(A'+B'+C'+D)$

1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	A
1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	B
1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	C
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	D
m_{15}	m_{14}	m_{13}	m_{12}	m_{11}	m_{10}	m_9	m_8	m_7	m_6	m_5	m_4	m_3	m_2	m_1	m_0	m
1	0	0	0	1	1	0	0	1	0	1	0	1	1	1	1	F

Example:- $F(A, B, C, D) = ABC$

$ABC(D+D') = AB'CD + AB'CD'$

$= 1011 + 1010$

$= m_{10} + m_{11}$

$F(A, B, C, D) = \Sigma(m_{10}, m_1)$

$F'(A, B, C, D) = \Sigma(m_0+m_1+m_2+m_3+m_4+m_5+m_6+m_7+m_8+m_9+m_{12}+m_{13}+m_{14}+m_{15})$

$F(A, B, C, D) = \Pi(m_0, m_1, m_2, m_3, m_4, m_5, m_6, m_7, m_8, m_9, m_{12}, m_{13}, m_{14}, m_{15})$

Example:- express the following function in all possible representation.

$F(A, B, C) = (A'+B+C')\cdot(A'+B)\cdot(A+C')$

$A'+B+C' \Rightarrow (101) \Rightarrow (M_5)$

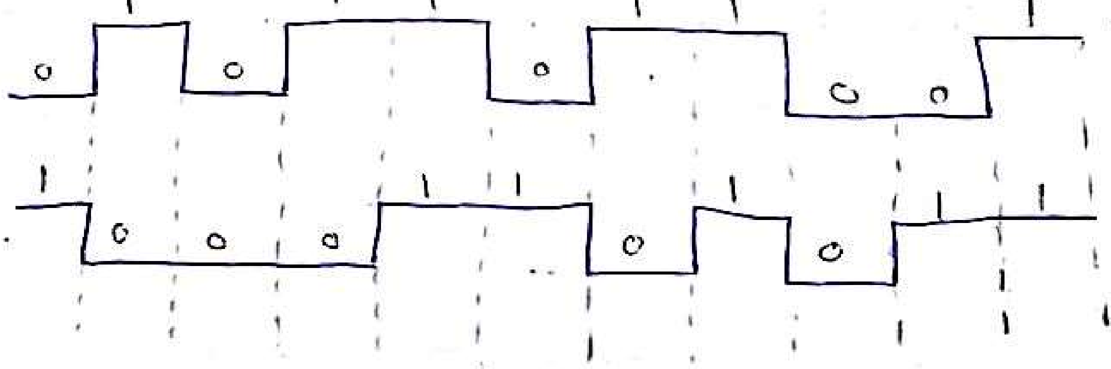
$(A'+B+C)(A'+B+C') \Rightarrow (100)(101) \Rightarrow (M_4)(M_5)$

$(A+C') \Rightarrow (A+B+C')(A+B'+C') \Rightarrow (001)(011)$

$(M_1)(M_3)$

$F(A, B, C) = \Pi(1, 4, 5, 3)$

$F'(A, B, C) = \Sigma(0, 2, 6, 7) = \Pi(0, 2, 6, 7)$



Example:- $F = xy + x'z$ ... max term

$(x+x')(x+z)(y+x')(y+z) \Rightarrow (x+z)(y+x')(y+z)$

* $(x+z) \Rightarrow (x+y+z)(x+y'+z) \Rightarrow (M_0)(M_2)$.

* $(x'+y) \Rightarrow (x'+y+z)(x'+y+z') \Rightarrow (M_4)(M_5)$

* $(y+z) \Rightarrow (x+y+z)(x'+y+z) \Rightarrow (M_0)(M_4)$

$F(x,y,z) = \Pi(0,2,4,5)$

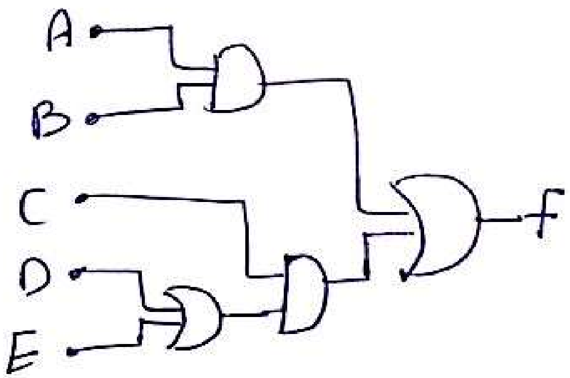
$F'(x,y,z) = \Pi(1,3,6,7)$

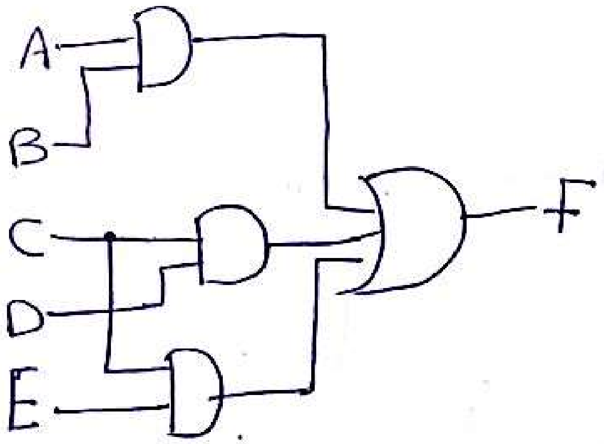
$F(x,y,z) = \Sigma(1,3,6,7)$

$F'(x,y,z) = \Sigma(0,2,4,5)$

Example:- $AB + C(D+E) = F$

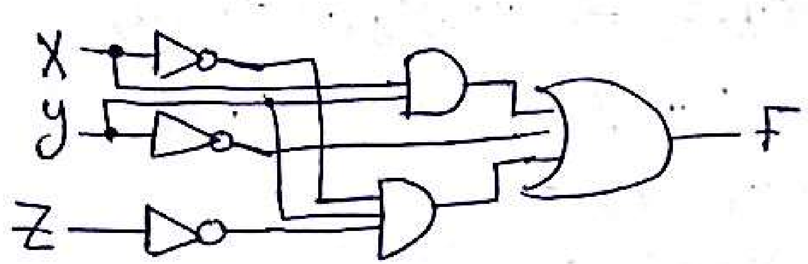
$AB + CD + CE = F$





نفس الاجابة.

Example:- $F = y' + xy + x'yz'$



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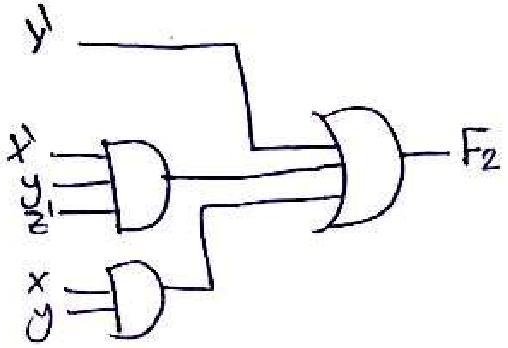
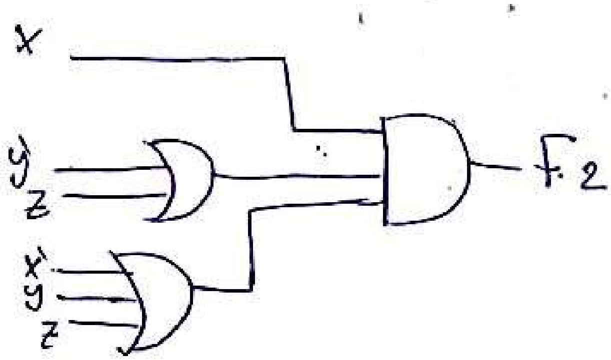
* $F_2 = x(x'+z)(x'+y+z')$

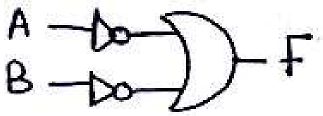
Sum of products. minterm

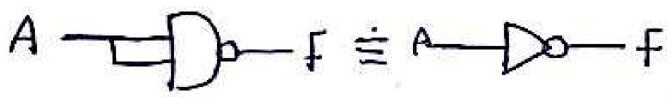


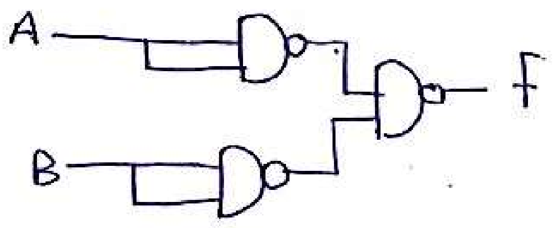
Products of sum max term



$F = \overline{A \cdot B} = A' + B'$

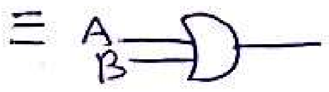




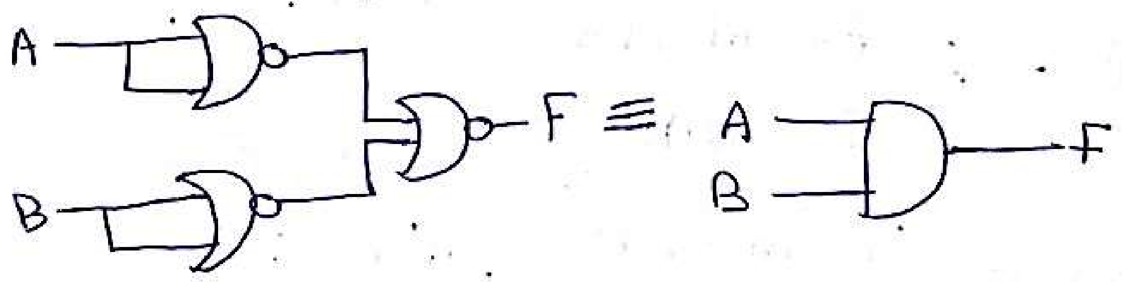


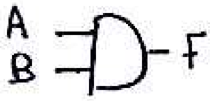
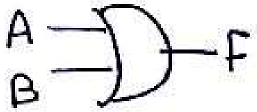
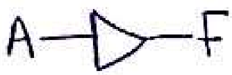
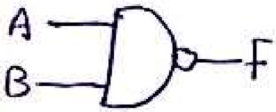
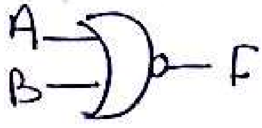
$F = \overline{A' \cdot B'} = A'' + B''$

$= A + B$



$F = \overline{A' + B'} = A'' \cdot B'' = \underline{\underline{A \cdot B}}$



Name	Gate	Function	trut table.
AND		$F = A \cdot B$	x | y | F 0 | 0 | 0 0 | 1 | 0 1 | 0 | 0 1 | 1 | 1
OR		$F = A + B$	A | B | F 0 | 0 | 0 0 | 1 | 1 1 | 0 | 1 1 | 1 | 1
Inverter OR NOT		$F = A'$	A | F 0 | 1 1 | 0
Buffer		$F = A$	A | F 1 | 1 0 | 0
NAND		~~F = A~~ $F = (A \cdot B)'$	A | B | F 0 | 0 | 1 0 | 1 | 1 1 | 0 | 1 1 | 1 | 0
NOR		$F = (A + B)'$	A | B | F 0 | 0 | 0 0 | 1 | 0 1 | 0 | 0 1 | 1 | 0
XOR		$F = AB' + BA'$ $F = A \oplus B$	A | B | F 0 | 0 | 0 0 | 1 | 1 1 | 0 | 1 1 | 1 | 0
NXOR		$F = AB + A'B'$ $F = (A \oplus B)'$	A | B | F 0 | 0 | 0 0 | 1 | 1 1 | 0 | 1 1 | 1 | 0

K-map

1 two-Variable-map ⇒ $2^2 = 4$

* جادين ل ٤

m0	m1
m2	m3

	y'	y
x'	x' y'	x' y
x	x y'	x y

Example:-

A	B	F	
0	0	0	m0
0	1	0	m1
1	0	1	m2
1	1	1	m3

	B'	B
A'		
A	1	1

جيران موجودين بكل A ال 2

$F = AB' + AB$

$F = A(B' + B)$

$F = A \cdot 1$

$\boxed{F = A}$

من الجيران $F = A$

نفس الجواب

---

	y'	y
x'	1	
x	1	

$F = y'$

	y'	y
x'	1	1
x		

$F = x'$

	y	y'
x'		
x	1	1

$F = x$

	y	y'
x'		1
x		1

$F = y$

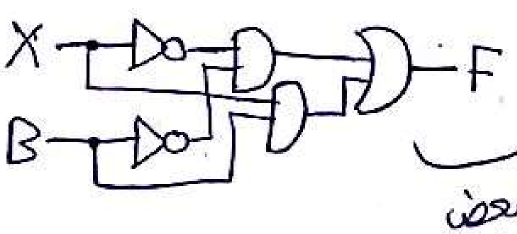
Example:-

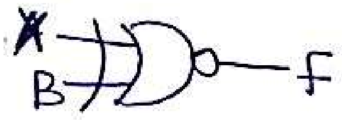
A	B	F	
0	0	1	m0
0	1	0	m1
1	0	0	m2
1	1	1	m3

		B
	1	
X		1

$F = X'B + XB$

$F = (X \oplus B)'$





نفس بعض

Three Variable - K-map ⇒ $2^3 = 8$

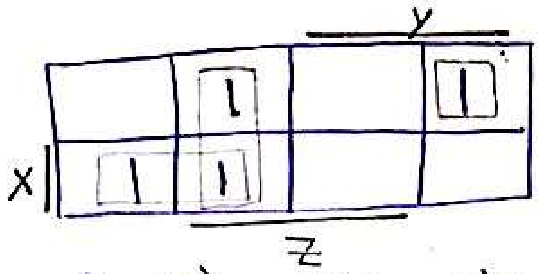
* ٣ ميران لا ١

m_0	m_1	m_3	m_2
m_4	m_5	m_7	m_6

	y'	y'	y	y
x'	$x'y'z'$	$x'y'z$	$x'yz$	$x'yz'$
x	$xy'z'$	$xy'z$	xyz	xyz'
	z'	z	z	z'

Example:-

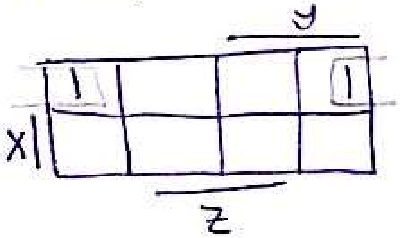
X	Y	Z	F	
0	0	0	0	m_0
0	0	1	1	m_1
0	1	0	1	m_2
0	1	1	0	m_3
1	0	0	1	m_4
1	0	1	1	m_5
1	1	0	0	m_6
1	1	1	0	m_7



عدد ال term = عدد الدوائر *

$$f = xy' + y'z + x'yz'$$

Example:-



$$F = x'z'$$

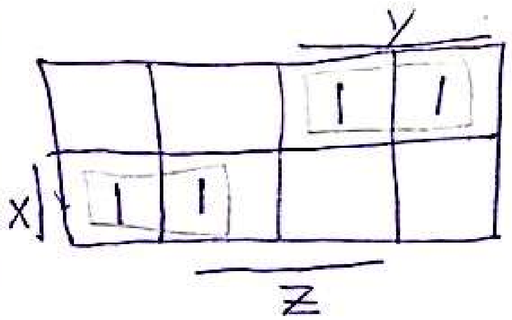
Example:

$$xy'z + xyz = F$$

$$F = xz(y' + y)$$

$$F = xz \cdot 1 \Rightarrow \boxed{xz}$$

Exumple

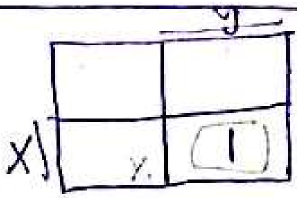


$$F(x,y,z) = \sum(2,3,4,5)$$

$$= xy' + x'y = (x \oplus y)$$

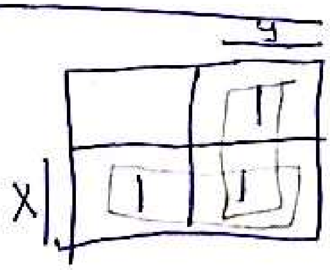
AND

$F = xy$



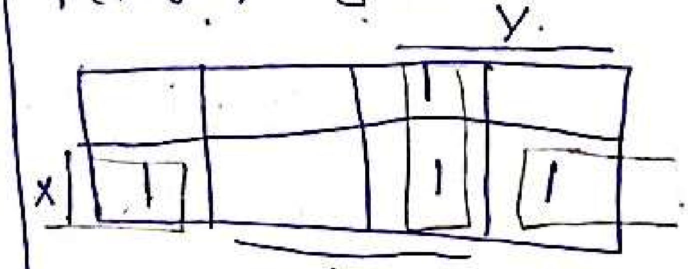
OR

$F = x + y$



Example:-

$$F(x,y,z) = \sum(3,4,6,7)$$

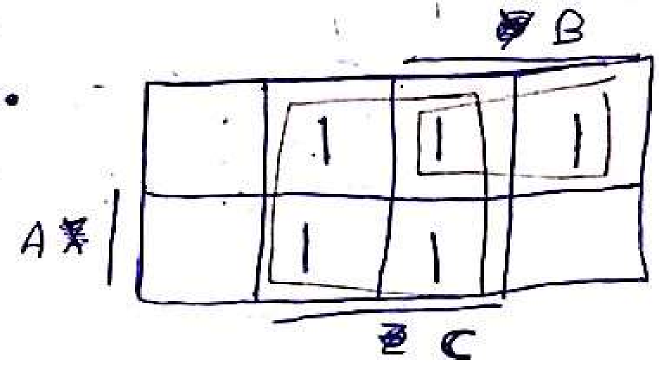


$$f = xz' + \overset{z}{z}y$$

Example:- $F = A'C + A'B + AB'C + BC$

1. sum of product.
2. product of sum.

1. $F = \sum(1, 2, 3, 5, 7)$
2. $F' = \sum(0, 4, 6)$



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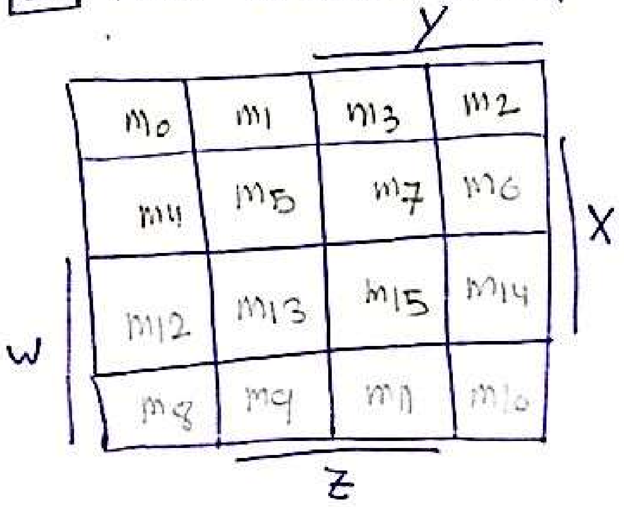
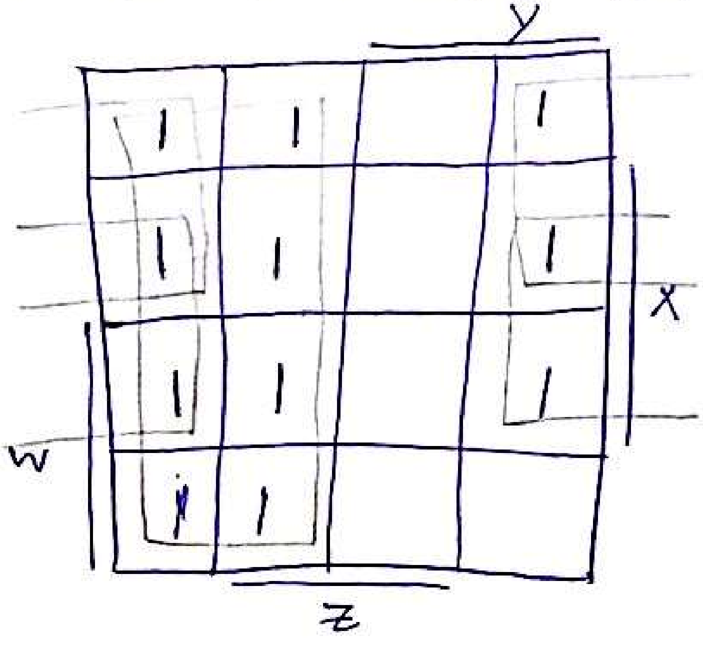
3 Four Variable Kmap ⇒ $2^4 = 16$

wxyz



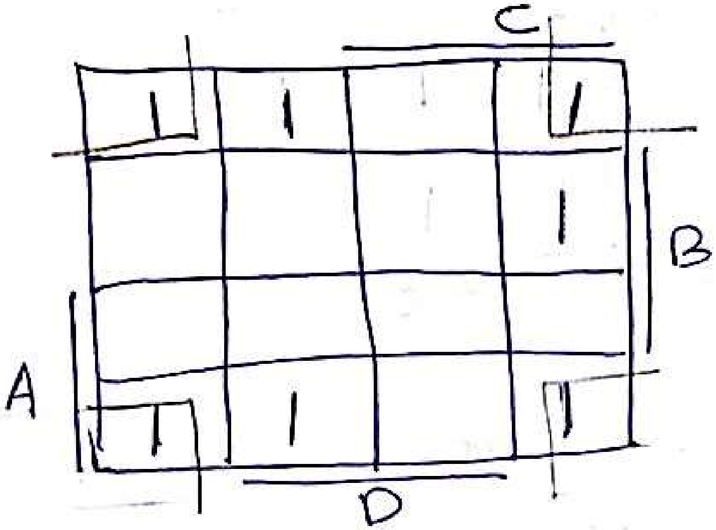
Example:- $F = (w, x, y, z) = \sum(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$

$F = y' + w'z' + xz'$



Example:- $F = A'B'C' + B'CD' + A'BCB' + AB'C'$

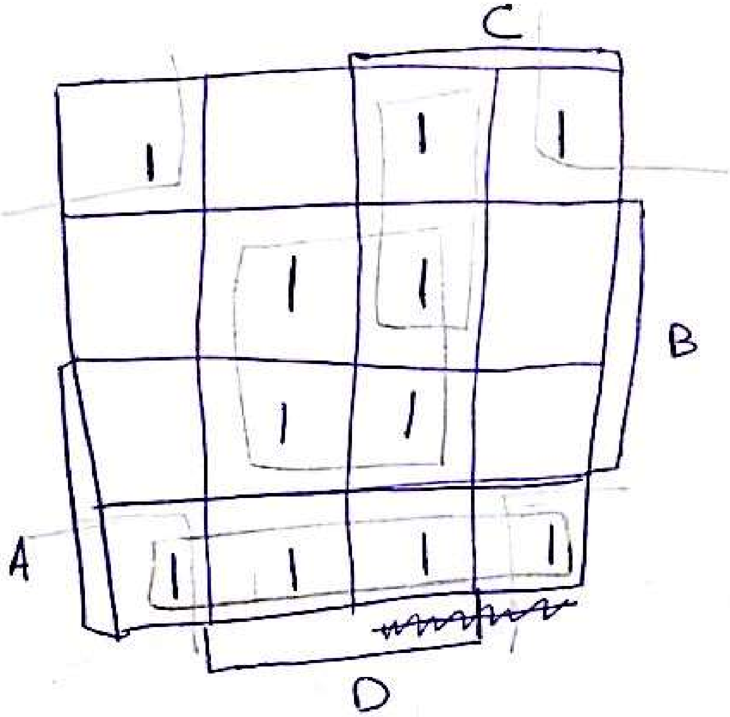
$F = A'CD' + B'C' + B'D$



1	1		1
			1
1	1		1

Example:-

$F(A,B,C,D) = \sum(0,2,3,5,7,8,9,10,11,13,15)$



1		1	1
	1	1	
	1	1	
1	1	1	1

$F = B'D' + AB' + A'CD + BD$

Scanned by CamScanner

Example:- minmiise the Following Function using K-map.

$F(A,B,C,D) = A'B'C'D' + A'B'D' + AB'CD' + A'BD + A'BD'$.

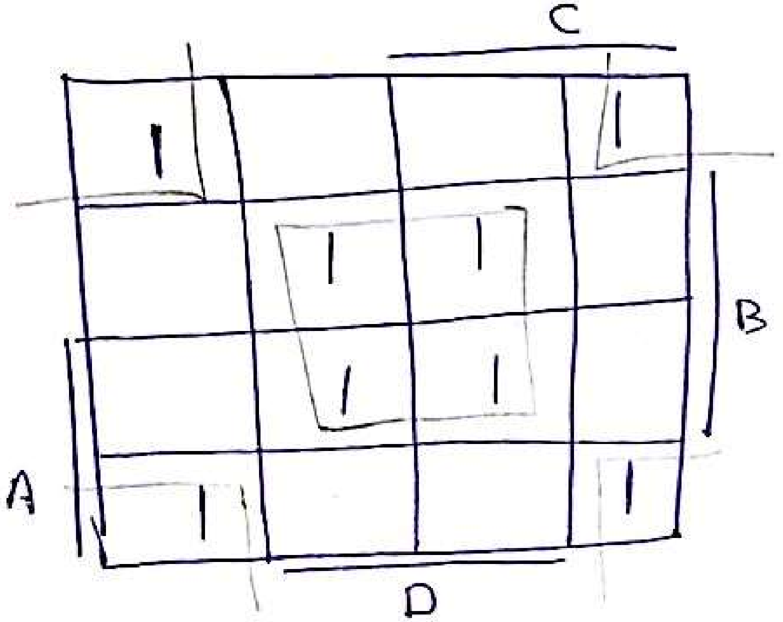
$AB'C'D' + A'B'C'D' + A'B'CD' + AB'CD' + ABCD + ABC'D + A'BCD + A'BC'D$

$1000 + 0000 + 0010 + 1010 + 1111 + 1101 + 011\phi + 010\phi$

$8 + 0 + 2 + 10 + 15 + 13 + \cancel{6}\,7 + 5$

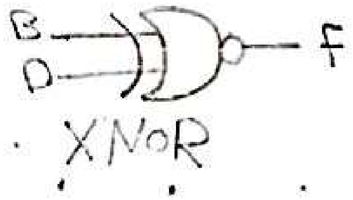
$= \Sigma(0, 2, 5, 7, 8, 10, 13, 15$

0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

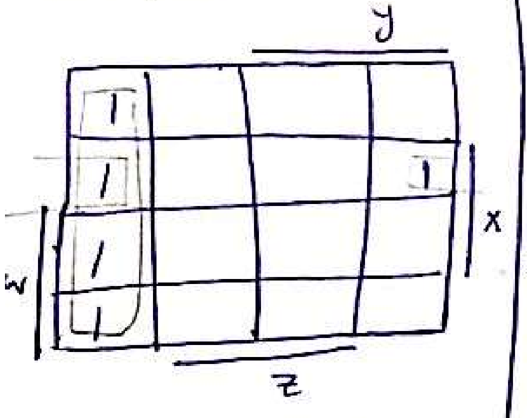


$F = B'D' + BD$

$F = (B \oplus D)'$

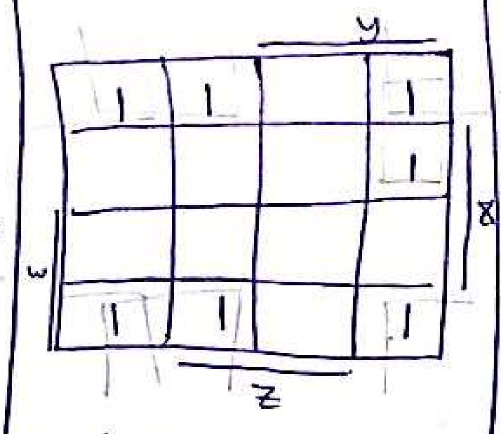


Example:-



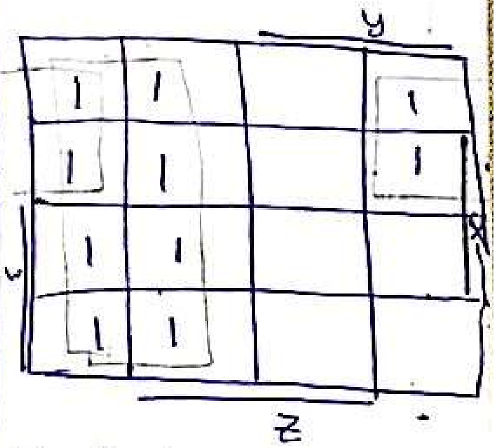
$F = y'z' + w'xz'$

Example:-



$F = x'z' + w'yz' + x'y'$

Example:-



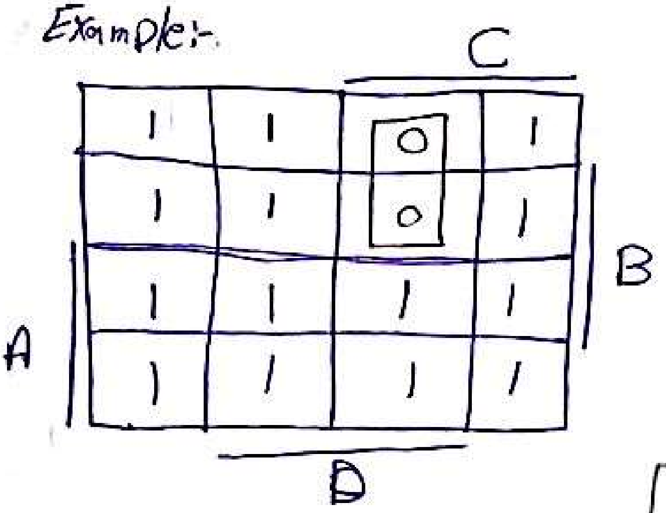
$F = w'z' + y'$

Max term:

عكس ال minterm

نضع داخل ال map ال zero بدل 1 او ناخذ صفر

Example:-



$F=\Sigma(0,1,2,4,5,6,8,9,10,11,12,13,14,15)$ minterm.

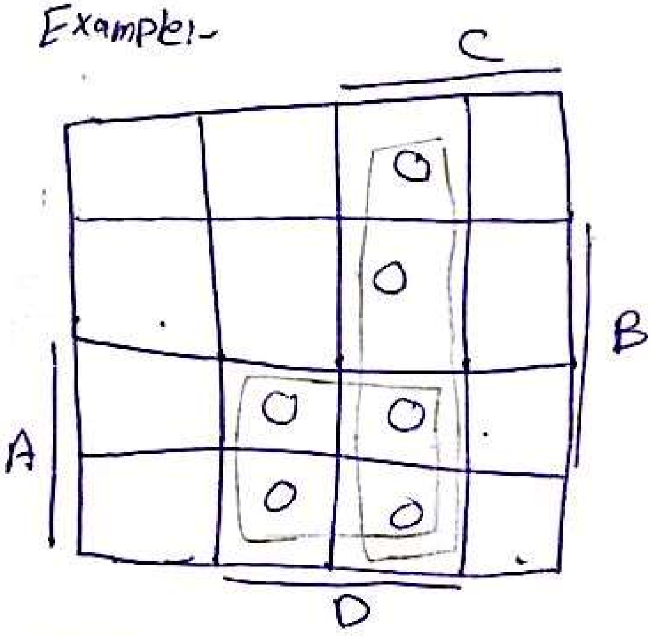
$F'=\Sigma(3,7)$ max term.

$F=\Pi(3,7)$

$F=(A'+C+D)$

$$\boxed{F=(A+C'+D')}$$

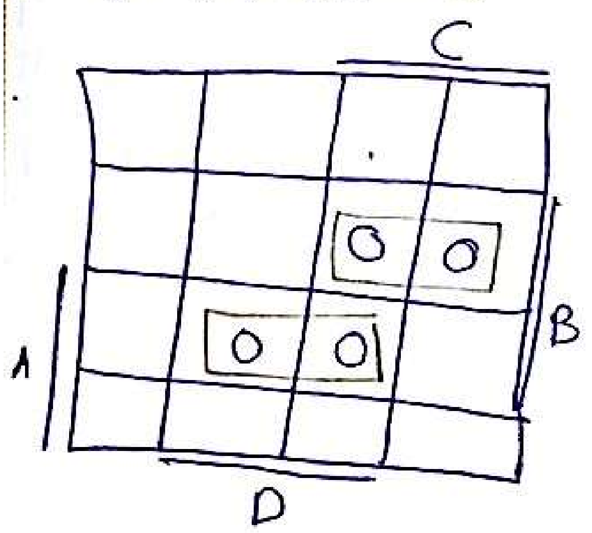
Example:-



$F=(\overset{*}{A}+D)\cdot(C+D)$

$$\boxed{F=(A'+D')\cdot(C'+D')}$$

$F=\Pi(6,7,13,15)$

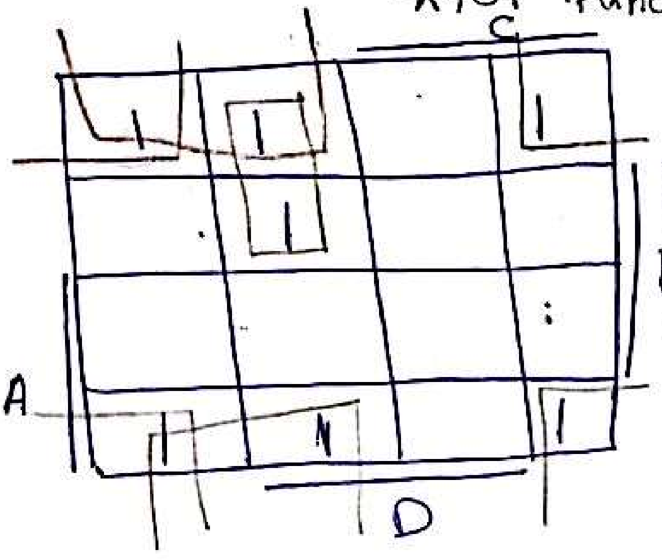


$F=(A+B+D)\cdot(A'+B+C)$

$$\boxed{F=(A'+B'+D')\cdot(A'+B+C)}$$

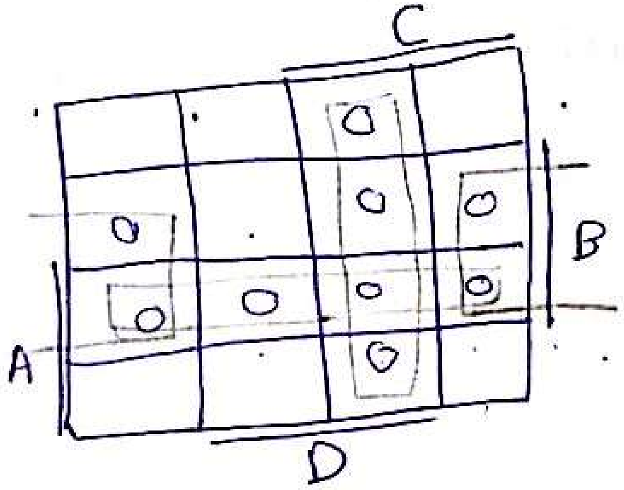
Example:- Find 1 sum of products
2 products of sum.

*For function $F(A,B,C,D)=(0,1,2,5,8,9,10)$



1 sum of product : minterm.

$$\boxed{F=A'C'D+B'C'+B'D'}\ 1$$

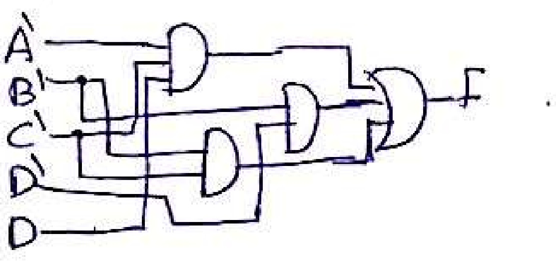


2 product of sum : Max term.

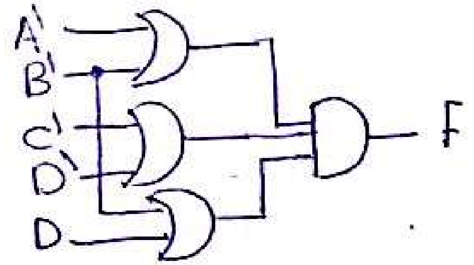
$$F=(B+D')\cdot(C+D)\cdot(A+B)$$

$$\boxed{F=(A'+B')\cdot(C'+D')\cdot(B'+D)}\ 2$$

S of P minterm



P of S max term.



Example:- $F=(A'+B'+C')(B+D)$

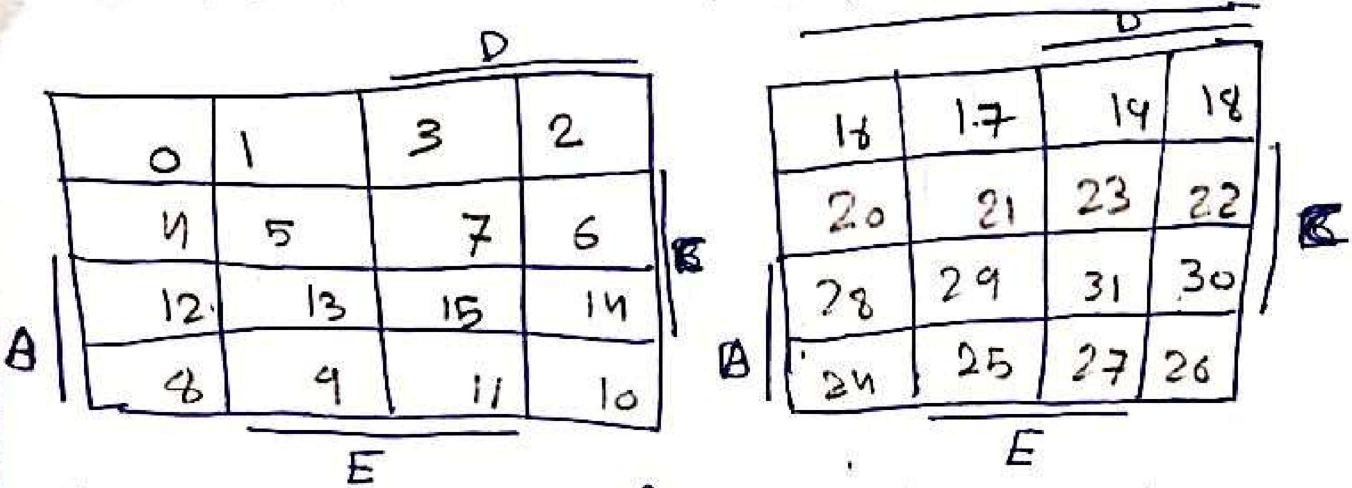
Find $F'=\overline{(A'+B'+C')(B+D)}$

$=\overline{(A'+B'+C')}+\overline{(B+D)}$

$=(A''B''C'')+(B'D')$

$=(A\cdot B\cdot C)+(B'\cdot D')$

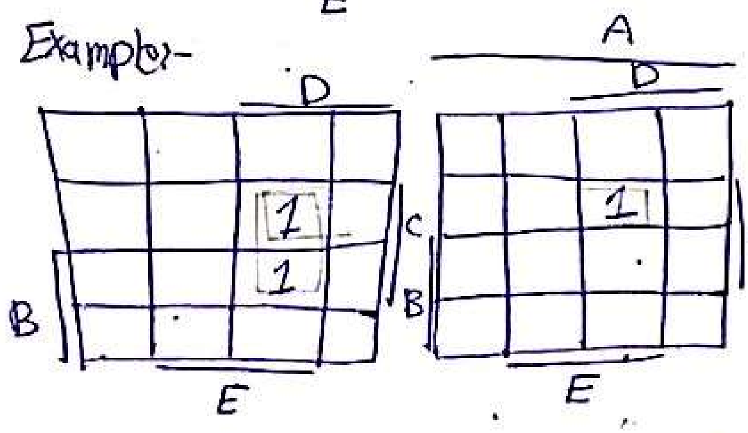
5 Five Varible - K- map $2^5 = 32$



0	1	3	2
4	5	7	6
12	13	15	14
8	9	11	10

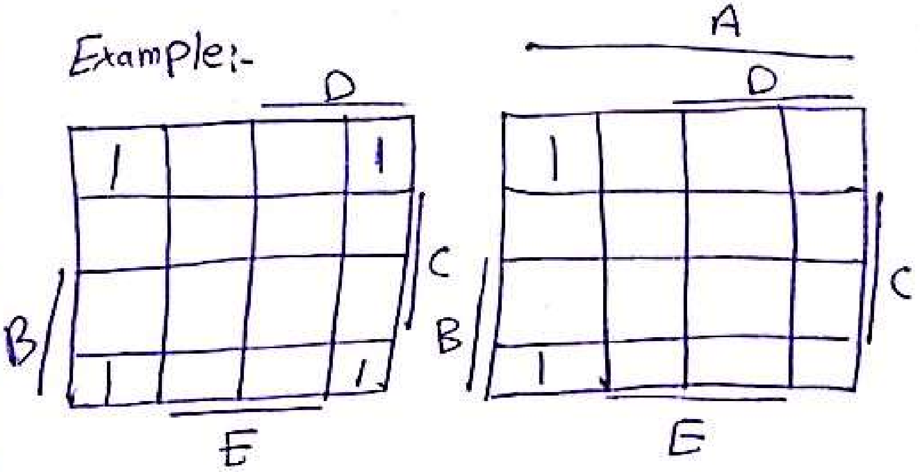
16	17	19	18
20	21	23	22
28	29	31	30
24	25	27	26

Example:-



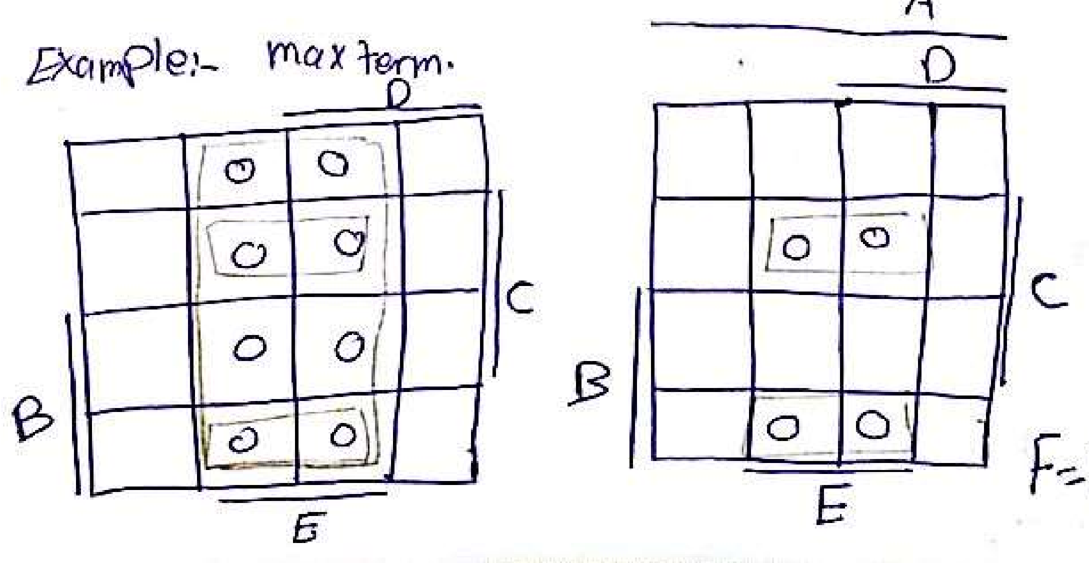
$F = A'CDE + B'CDE$

Example:-



$F = C'D'E' + A'C'E'$

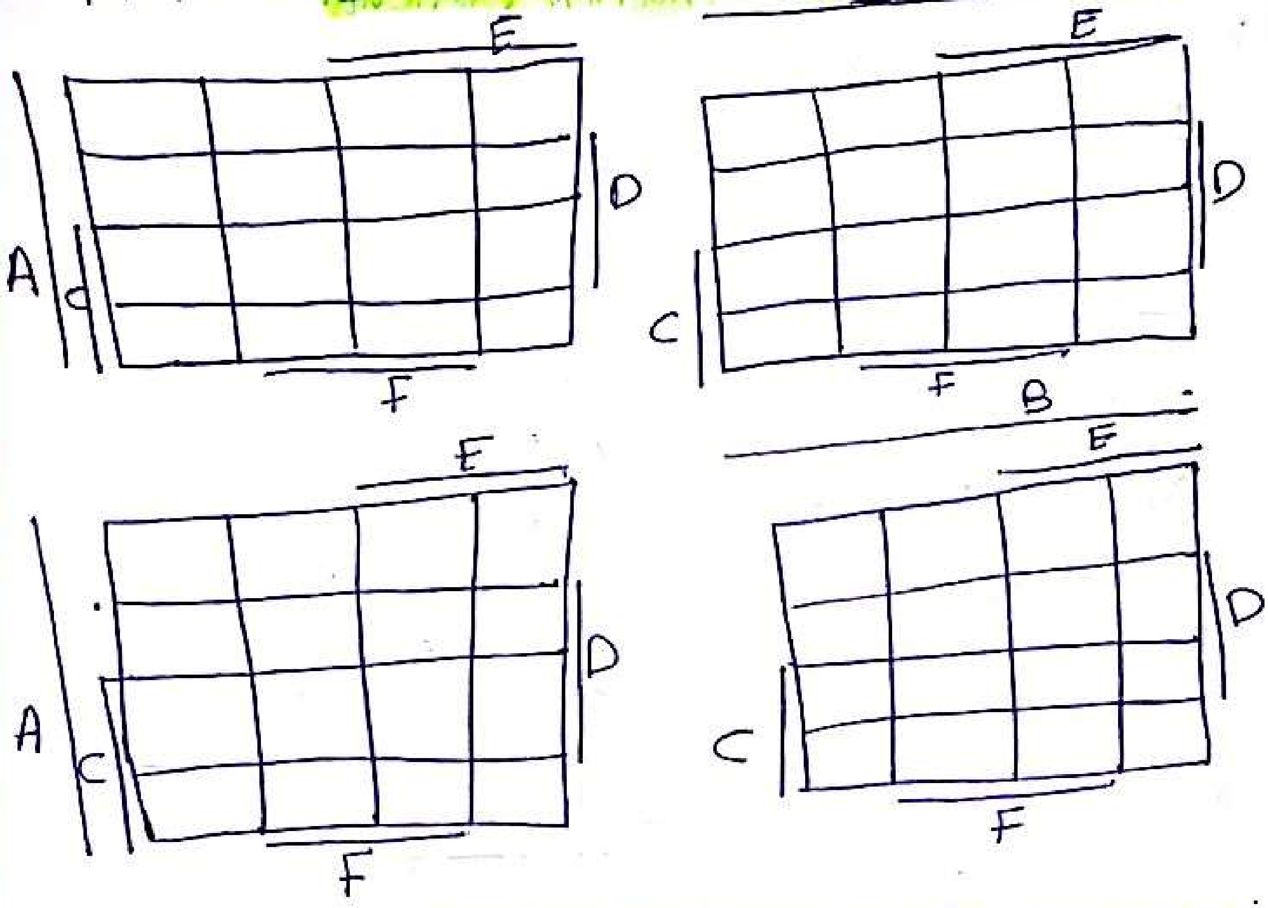
Example:- max term.



$F = (B'+C+E) \cdot$
$(B+C'+E) \cdot$
$(A'+E)$

$F = (B+C'+E') \cdot (B'+C+E')$
$\cdot (A+E')$

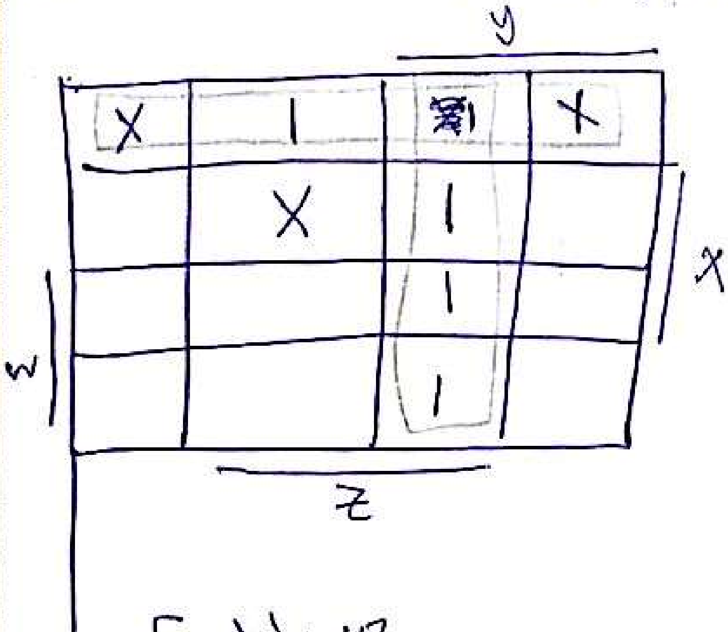
5 Six variable K-map $2^6 = 64$



Dont-Care

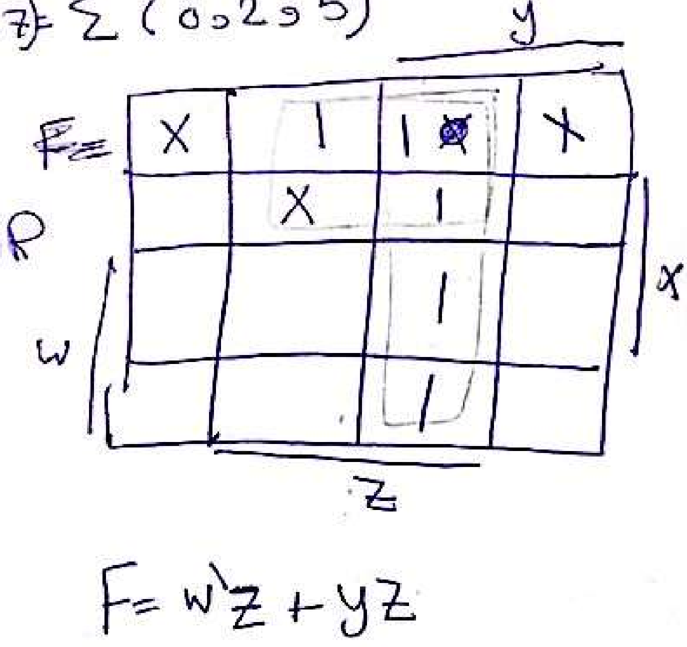
$F(w,x,y,z) = \sum(1,3,7,11,15)$

dont Care $(w,x,y,z) = \sum(0,2,5)$



X	1	1	X
	X	1	
		1	
		1	

OR



X	1	1	X
	X	1	
		1	
		1	

$F = w'x' + yz$

(0,1,2,3,7,11,15)

$F = w'z + yz$

$F = z(w' + y)$

F = (1,3,5,7,11,15)

Combination Curicut.

CombinationL → without memory.

SuquratoL → with memory.

$$\begin{array}{r} 0 \\ +\,0 \\ \hline 0 \end{array} \qquad \begin{array}{r} 0 \\ +\,1 \\ \hline 1 \end{array} \qquad \begin{array}{r} 1 \\ +\,0 \\ \hline 1 \end{array} \qquad \begin{array}{r} 10 \\ +\,1 \\ \hline 11 \end{array} \qquad \begin{array}{r} 1 \\ +\,1 \\ \hline 10 \end{array}$$

Type Combinational:

1 Half Adder [H.A]   2 Full Adder [F.A]

---

1 Half Adder

2 input
2 ourput

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

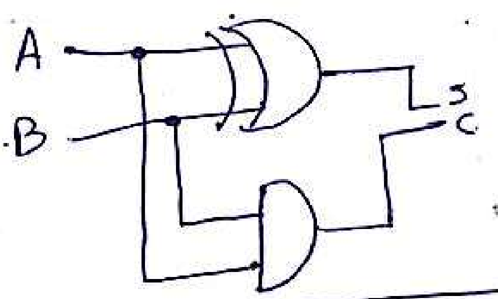
		B
		1
A	1	

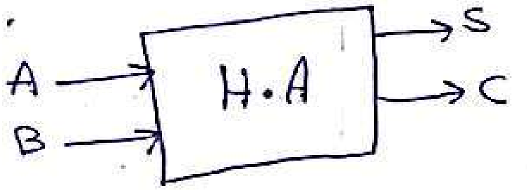
		B
A		1

$S = AB' + BA'$

$S = A \oplus B$ XoR

$C = AB$





Example:- In 4Bit system

$$\begin{array}{cccc} & 1 & & \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 \\ \hline 0 & 1 & 0 & 1 \end{array} \longrightarrow \text{3input}$$

⇒ not Half Adder use Full Adder.

2 Full Adder.

3 input
2 output.

عدد gate [illegible]
عدد ال output

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

B

		1		1
A	1		1	

Cin

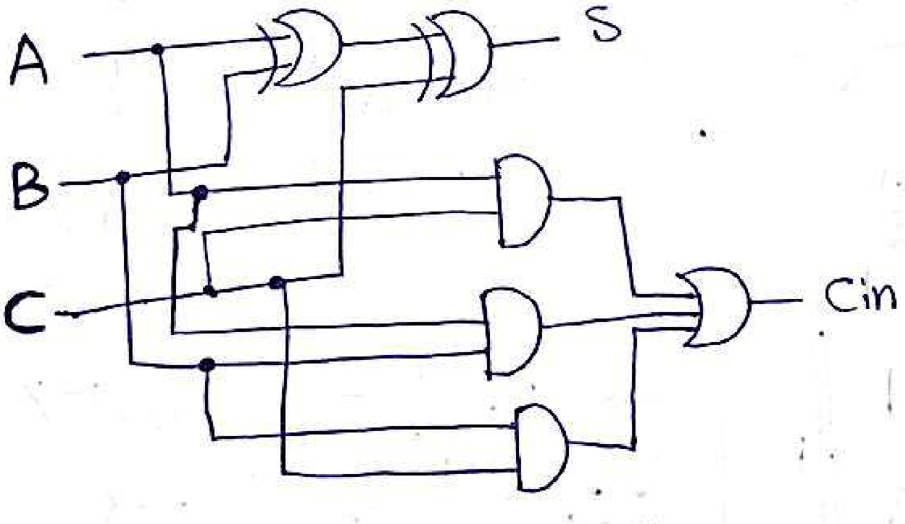
$S = AB'C' + A'B'C + ABC + A'BC'$
$= A \oplus B \oplus C$

B

			1	
A		1	1	1

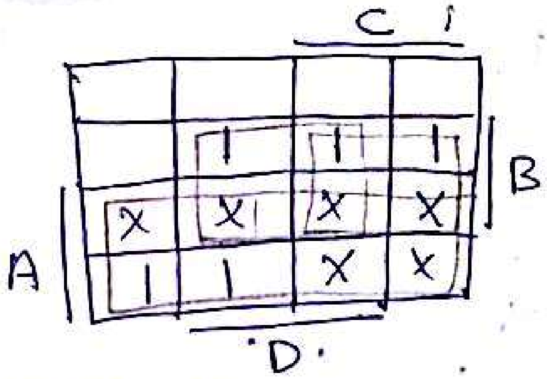
cin

$Cout = AC + AB + BC$

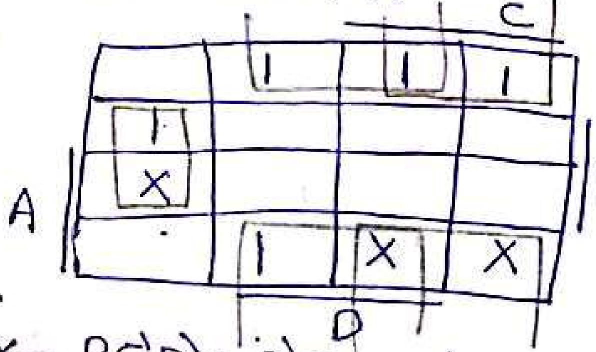


Exess 3 Code :-

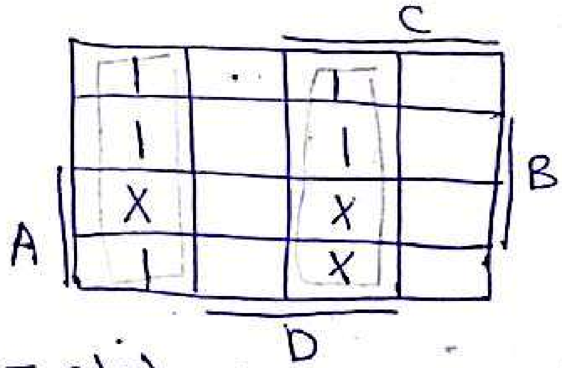
A	B	C	D	W	X	y	Z	
0	0	0	0	0	0	1	1	0
0	0	0	1	0	1	0	0	1
0	0	1	0	0	1	0	1	2
0	0	1	1	0	1	1	0	3
0	1	0	0	0	1	1	1	4
D	1	0	1	1	0	0	0	5
0	1	1	0	1	0	0	1	6
0	1	1	1	1	0	1	0	7
1	0	0	0	1	0	1	1	8
1	0	0	1	1	0	0	0	9
1	0	1	0	X	X	X	X	10
1	0	1	1	X	X	X	X	11
1	1	0	0	X	X	X	X	12
1	1	0	1	X	X	X	X	13
1	1	1	0	X	X	X	X	14
1	1	1	1	X	X	X	X	15



W= BD+ BC+ A

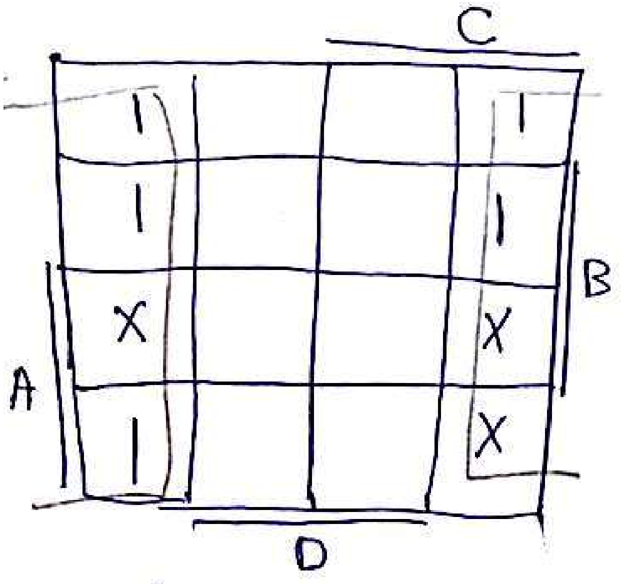


X= BC'D'+ B'D + B'C

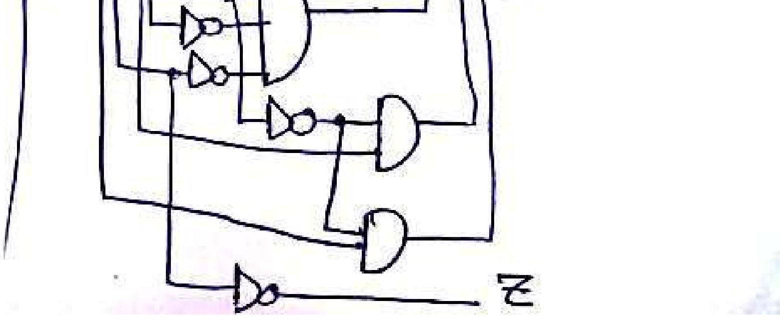


y= C'D'+ CD

y= (C⊕D)' = C⊙D



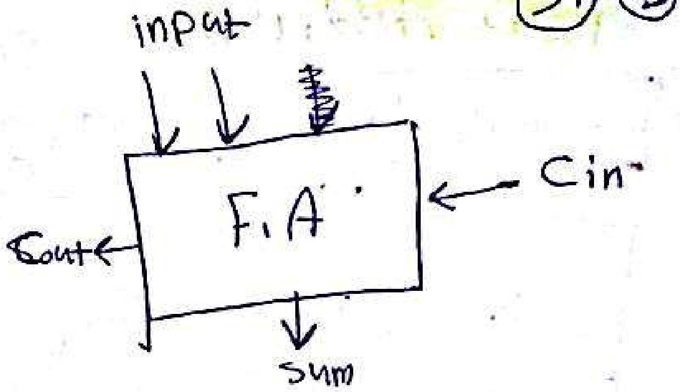
Z= D'

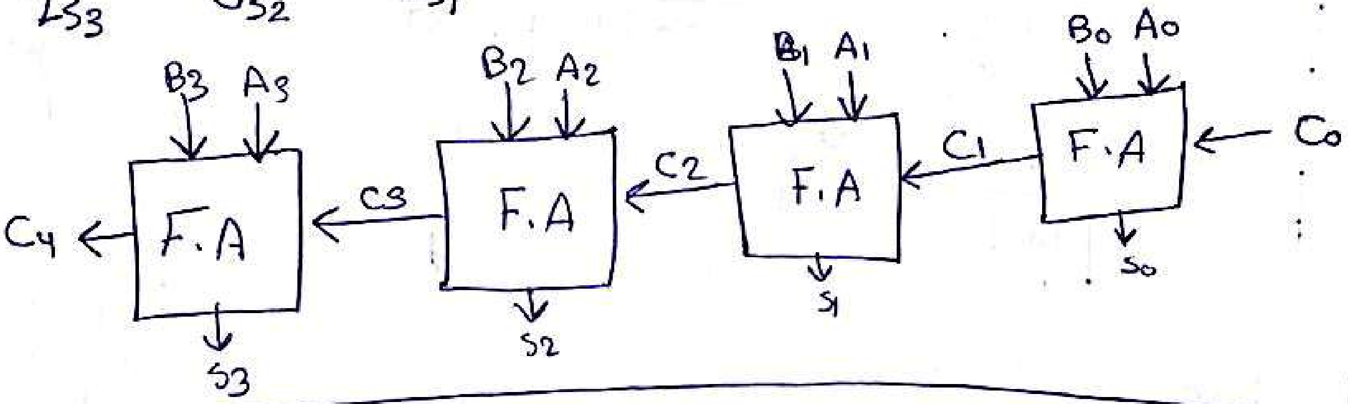


Binary Addes

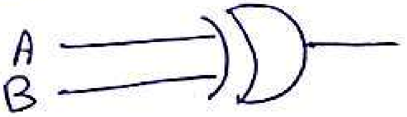
Example:-

1_{C_3}	0_{C_2}	0_{C_1}	0_{C_0}
0_{A_3}	1_{A_2}	0_{A_1}	1_{A_0}
0_{B_3}	1_{B_2}	1_{B_1}	0_{B_0}
1_{S_3}	0_{S_2}	1_{S_1}	1_{S_0}





XOR



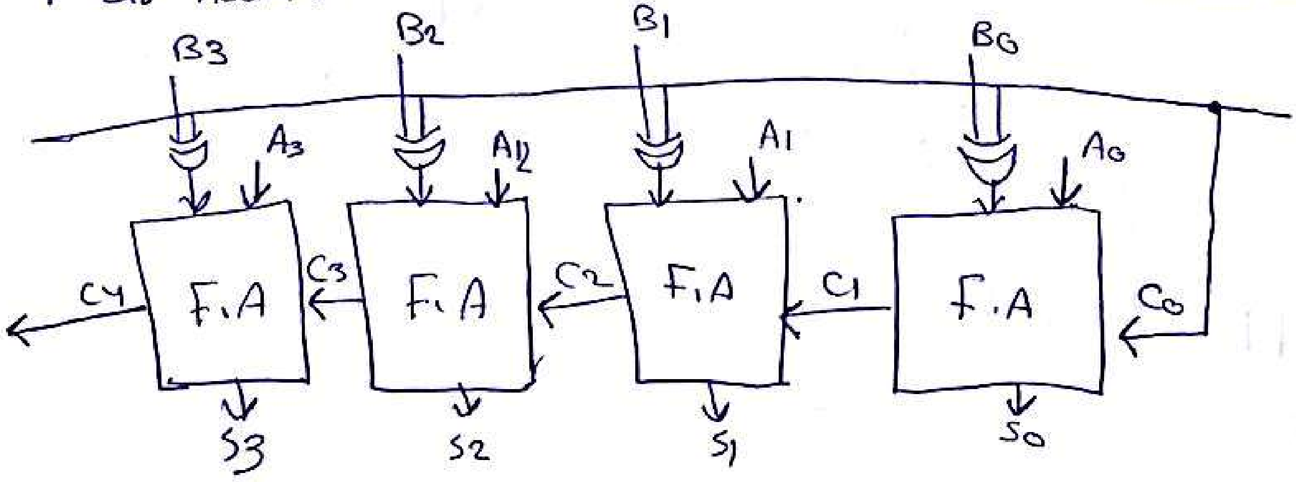
$F = A \oplus B$

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

1) $B \oplus 0 = C_0 B = 0$

2) $B \oplus 1 = C_0 B' = 1$

4- Bit Adder:-



if $M = 0 \Rightarrow$ 4bit adder $\oplus$

if $M = 1 \Rightarrow A + \underbrace{B' + 1}_{2cd} \Rightarrow$ ~~4bit adder~~ 4bit subtraton $\ominus$

BCD Addition :-

Decimal	BCD
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

Example:-

اقل من 9

1

+ 0011
0100
0111

3 +
4
7

2

111

0010 0011
+ 0001 0101
0011 1000

2 3 +
1 5
$\boxed{3}\boxed{8}$

اقل من 9

3

11

1000 0110
+ 0001 0011
1001 1001

8 6 +
1 3
9 9

يساوي 9 عادي خلي هيك

4

1 1

0100 0101 0000
+ 0100 0001 0111
1000 0110 0111

4 5 0
4 1 7
$\boxed{8}\boxed{6}\boxed{7}$

اقل من 9 عادي

Example:-

11 11

+ 0101 1001 1000
0001 1000 0011

1

1011
0110 +

11

0010 0001
0110 +

0111 1000 0001
7 8 1

① ①
5 9 8
+ 1 8 3
7 $\boxed{8}\boxed{1}$

اكبر من 9 بزيد 6

Comparator

$\underline{3}\underline{2}\underline{4}\underline{5}⑥ . 701$

$\underline{3}\underline{2}\underline{4}\underline{5}⑦ . 701 \rightarrow$ آكبر

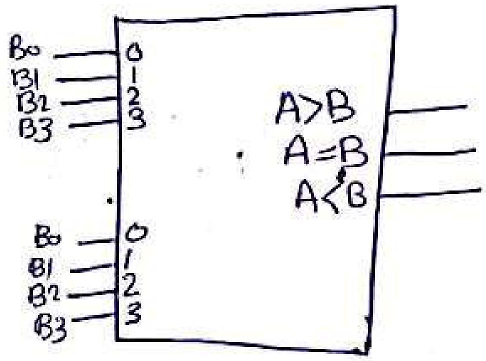
For Decimal

$\underline{1}\underline{1}⓪11 . 1101$

$\underline{1}\underline{1}①01 . 1111 \rightarrow$ آكبر

For Binary.

Comparator 4-Bit



ناتج المقارنة

إذا تساوى الشرط بحط فيه 1

إذا لم يساوي الشرط بحط فيه zero.

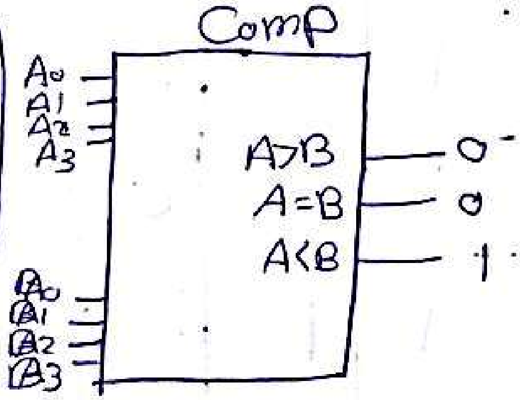
Example :-

$A_0 = 1 \quad A_1 = 5 \,, \; B_0 = 4 \,, \; B_1 = 7$

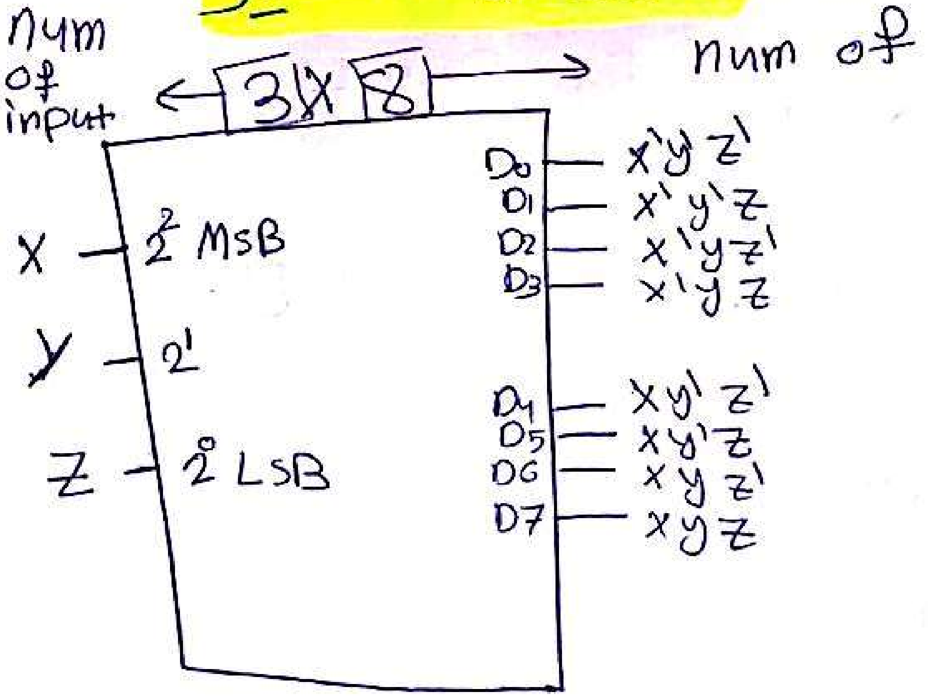
= OR < OR >

$A_3 A_2 A_1 A_0 \; \boxed{\phantom{<}} \; B_3 B_2 B_1 B_0$

$\underline{0} \; \underline{0} \; \boxed{5} \; 1 \; \boxed{<} \; \underline{0} \; \underline{0} \; \boxed{7} \; 4$



فك التشفير de Coder



X	y	Z	D0	D1	D2	D3	D4	D5	D6	D7	~~D8~~
0	0	0	1	0	0	0	0	0	0	0	
0	0	1	0	1	0	0	0	0	0	0	
0	1	0	0	0	1	0	0	0	0	0	
0	1	1	0	0	0	1	0	0	0	0	
1	0	0	0	0	0	0	1	0	0	0	
1	0	1	0	0	0	0	0	1	0	0	
1	1	0	0	0	0	0	0	0	1	0	
1	1	1	0	0	0	0	0	0	0	1	

Example:- Implement a full adder using a decoder.

A	B	Cin	S	Cout	
0	0	0	0	0	D0
0	0	1	1	0	D1
0	1	0	1	0	D2
0	1	1	0	1	D3
1	0	0	1	0	D4
1	0	1	0	1	D5
1	1	0	0	1	D6
1	1	1	1	1	D7

$S = \Sigma(1, 2, 4, 7)$

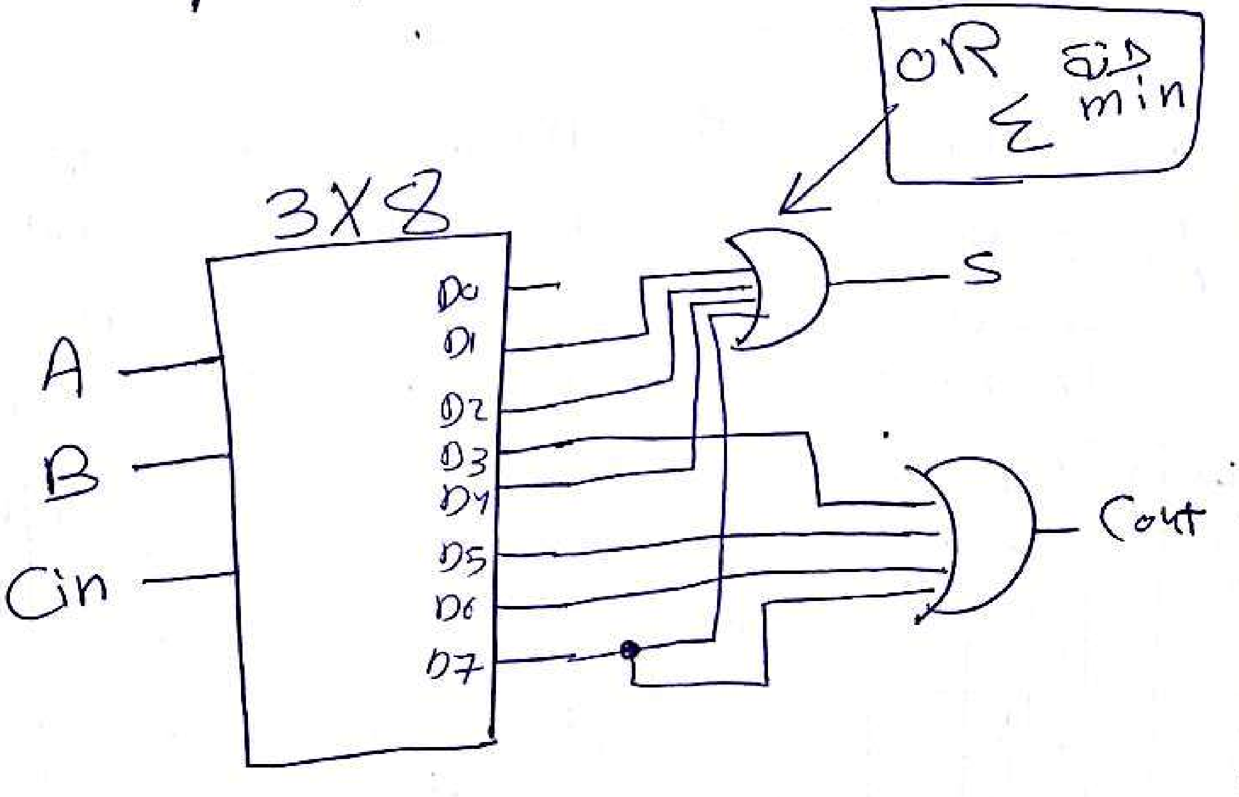
$Cout = \Sigma(3, 5, 6, 7)$

input ⇒ 3

$output = 2^{input}$

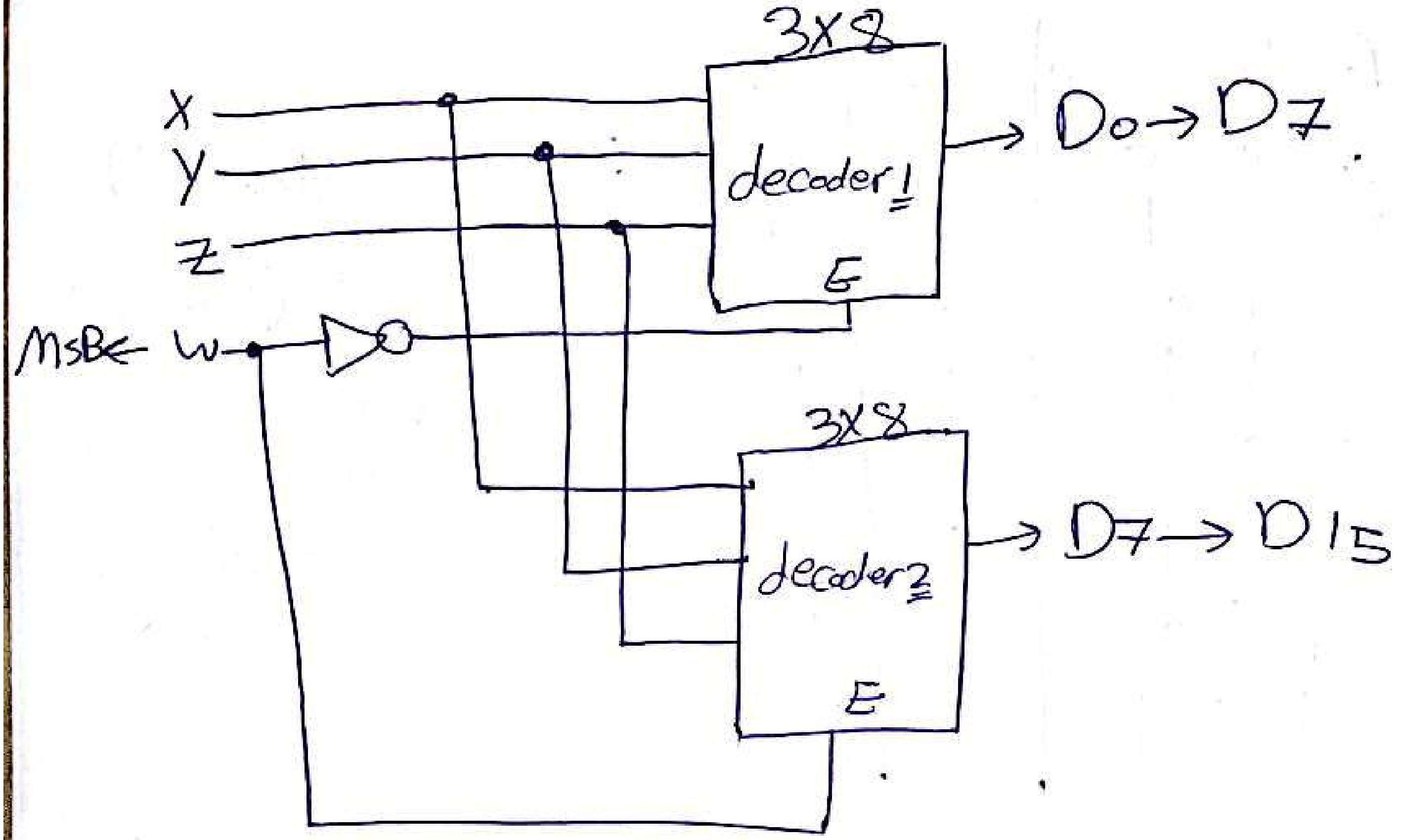
$= 2^3 = \underline{\underline{8}}$

$D_0 \rightarrow D_7$



Not :- 4 input 16 output use 2 decoder.

Example:-



E is Active Hige that mean decoder work when w=1

E is Active Low that mean decoder work when w=0

w=0 → decoder 1 work dec 2 not work

w=1 → dec 1 Not work dec 2 work.

W	X	y	Z	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0					1	0	0	0	0	0	0	0	0	0	0
0	1	0	1						1	0	0	0	0	0	0	0	0	0
0	1	1	0							1	0	0	0	0	0	0	0	0
0	1	1	1								1	0	0	0	0	0	0	0
1	0	0	0									1	0	0	0	0	0	0
1	0	0	1										1	0	0	0	0	0
1	0	1	0											1	0	0	0	0
1	0	1	1												1	0	0	0
1	1	0	0													1	0	0
1	0	0															1	0
[illegible]	[illegible]	[illegible]	[illegible]															1

مهم الترتيب

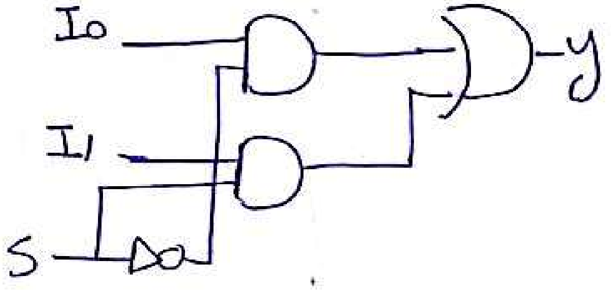
Multiplexer [MUX]

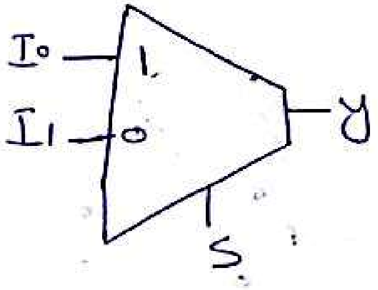
More than Input → كتير

one output → واحد فقط

Type of Mux:-

1 2 to 1 Line Multiplexer.



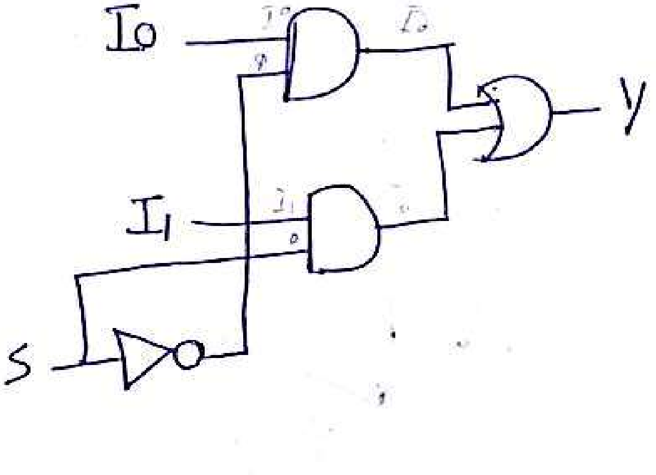


I0 , I1 → Data

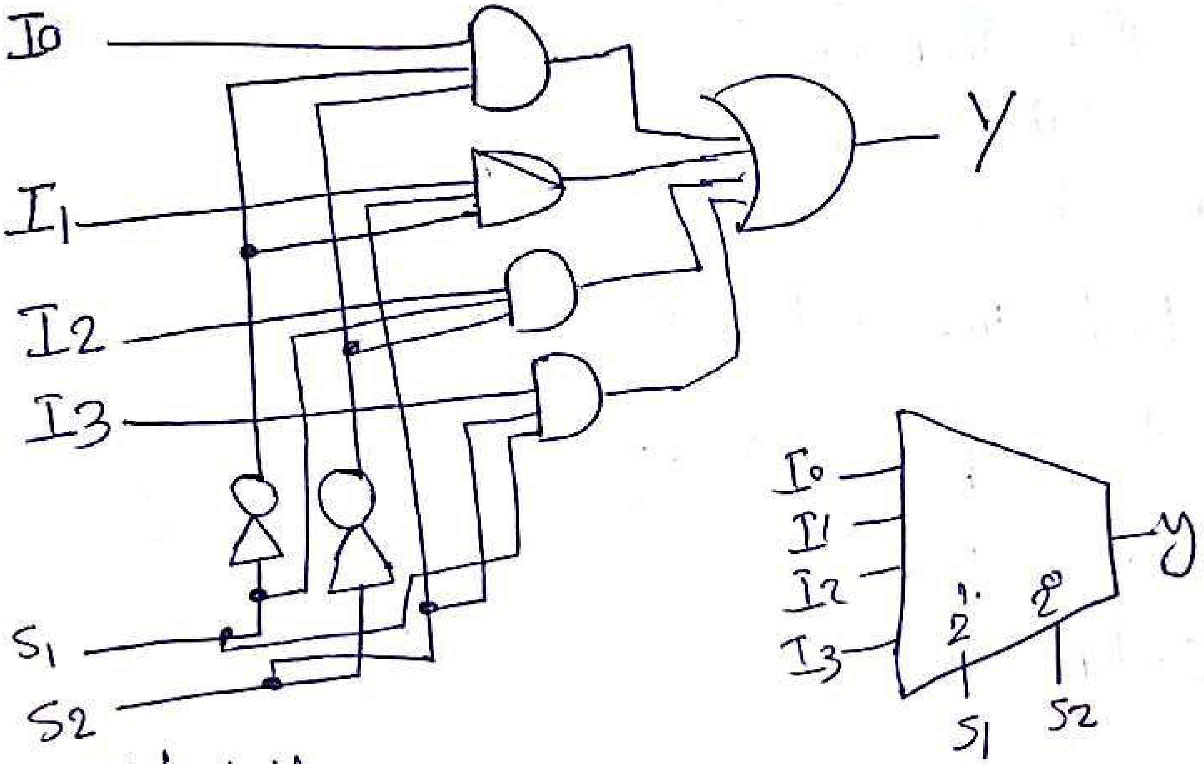
S → Control Bit

X → Adeesi لا يهم

S	
0	I0
1	I1

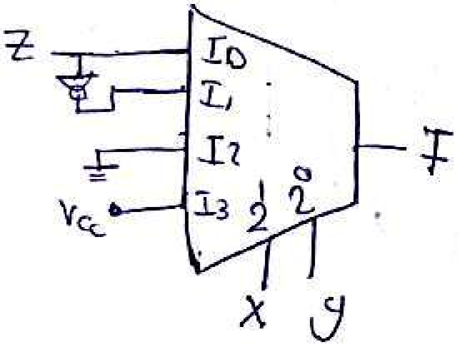


2 4 to 1 → Line Mux



S1	S0	y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

	X	y	Z	F	
I0	0	0	0	0	F=Z
	0	0	1	1	
I1	0	1	0	1	F=Z'
	0	1	1	0	
I2	1	0	0	0	F= Zero
	1	0	1	0	
I3	1	1	0	1	F=1
	1	1	1	1	



Example:- Implement function using mux?

$F(x,y,z) = x'yz + xy'z + z'$

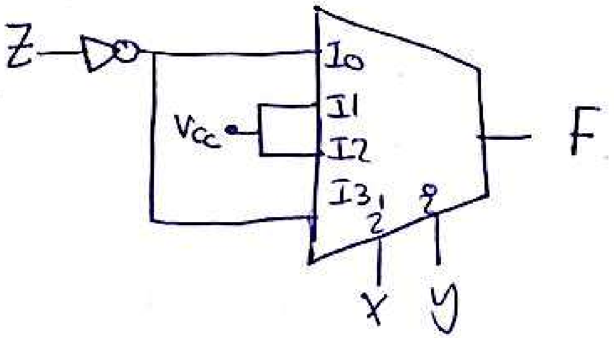
$= x'yz + xy'z + xyz' + xy'z' + x'y'z' + x'yz'$

$011 + 101 + 110 + 100 + 000 + 010$

	x	y	z	F	
I_0	0	0	0	1	F = z'
	0	0	1	0	
I_1	0	1	0	1	F = 1
	0	1	1	1	
I_2	1	0	0	1	F = 1
	1	0	1	1	
I_3	1	1	0	1	F = z'
	1	1	1	0	

$F = \Sigma(0,2,3,4,5,6)$

$F = \Pi(1,7)$



---

minterm → ' → 0
→ بدون → 1
→ Truthtable 1

Maxterm → ' → 1
→ بدون → 0
→ truth table 0

Example:- Implement the following function using Mux? (46)

$\boxed{1}$ $F_1(A,B,C,D) = (A+B+C')\cdot(A+B)(A'+B'+D')$

$\boxed{2}$ $F_2(A,B,C,D) = (A+B'+D)(A+C)$

Solution:-

$\boxed{1}$ $F_1(A,B,C,D) = (A+B+C')\cdot(A+D')\cdot(A'+B'+D')$

$(A+B+C'+D)(A+B+C'+D')(A+B+C+D')(A+B+C'+D')(A+B'+C+D')(A+B'+C'+D')$

0 0 1 0   0 0 1 1   0 0 0 1   0 0 1 1   0 1 0 1   0 1 1 1

$(A'+B'+C+D')(A'+B'+C'+D')$

1 1 0 1   1 1 1 1

$F_1 = \Pi(1,2,3,5,7,13,15)$

$F_1 = \Sigma(0,4,6,8,9,10,11,12,14$

$F_2 = (A+B'+D')\cdot(A+C) \Rightarrow (A+B'+C'+D')(A+B'+C+D')(A+B+C'+D$

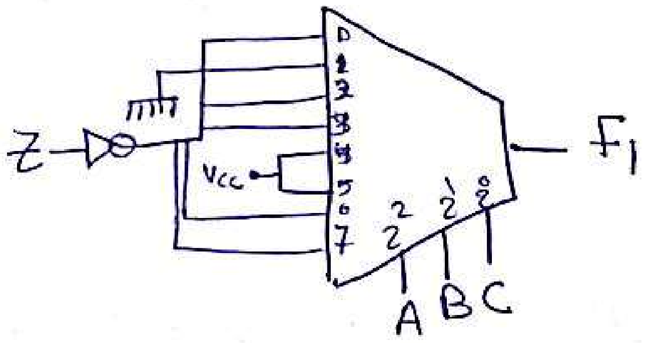
0 1 1 1   0 1 0 1   0 0 1

$(A+B+C+D)(A+B'+C+D)(A+B'+C+D')$

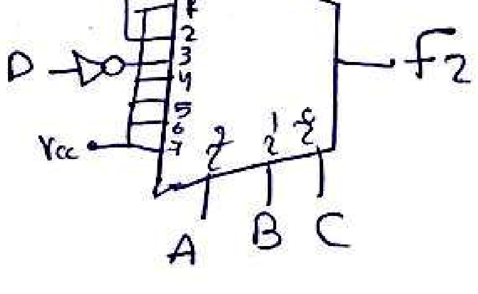
0 0 0 0   0 1 0 0   0 1 0 1

$F_2 = \Pi(0,1,4,5,7)$

$F_2 = \Sigma(2,3,6,8,9,10,11,12,13,14,15)$



A	B	C	D	F1		F2	
0	0	0	0	1	F=B	0	F=0
0	0	0	1	0		0	
0	0	1	0	0	F=0	1	F=1
0	0	1	1	0		1	
0	1	0	0	1	F=B'	0	F=0
0	1	0	1	0		0	
0	1	1	0	1	F=D'	1	F=D'
0	1	1	1	0		0	
1	0	0	0	1	F=1	1	F=1
1	0	0	1	1		1	
1	0	1	0	1	F=1	1	F=1
1	0	1	1	1		1	
1	1	0	0	1	F=D'	1	F=1
1	1	0	1	0		1	
1	1	1	0	1	F=D'	1	F=1
1	1	1	1	0		1	



~~final logic~~

SEQUENTIAL CIRCUITS

* Logic cct →

① Combinational cct : No memory. ← كل شي قبل كان

② sequental cct : with memory. ← كل شي بعد

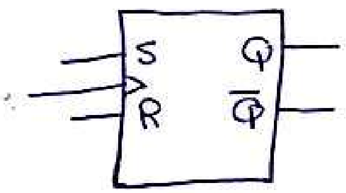
note
bit = 0, 1
byte = 8 bit
word = 16 bit
double word = 32 bit

*note.
set to 1 Hig
Rest to 0 Low

FLIP Flops

- S.R latch (set, Reset)
- J-K
- taggle
- D FlipFlops.

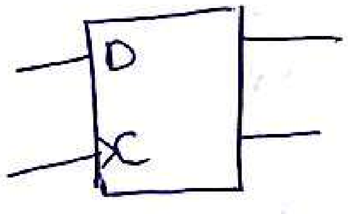
①



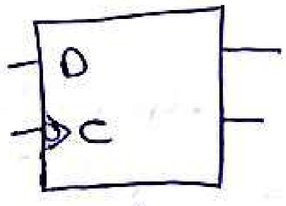
← output

← Complemon out put.

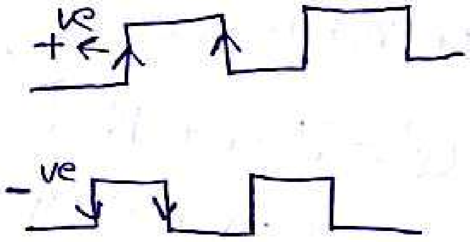
2 input
2 output.



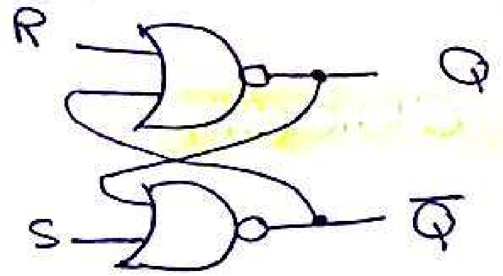
+ve edge



-ve edge



اذا كانت في Pouple تكون في Negatike



truth table

S	R	Q^{+}	→ next state (output ليش انا بتوقع شو بيطلع)
0	0	Q	→ No Change stable
0	1	0	→ Reset state
1	0	1	→ set State.
1	1	not valied	→ 1 or 0 I dont now ??

Q(t) → present State

Q(t+1) Next state.

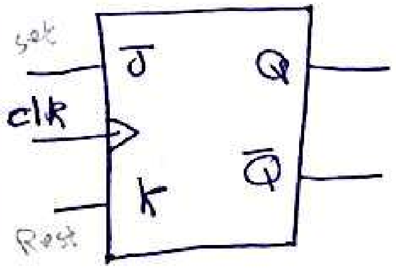
No characteristic eq because 1 equal not valied

---

② J-K- flibe flop → عشان احل مشكلة ال valied في set وال Reset

Latch → with out CLK → اي تغير على input يعطيني تغير على output (حساس)

Flip Flop → with clk → يكون عندي تغير يا من 0 او 1



truth table.

J	K	Q^{+}
0	0	Q
0	1	0
1	0	1
1	1	$\bar{Q}$ → toggle (complemant Q)

characteristic equation →

$$Q^{+} = J\bar{Q} + \boxed{K}\,\overset{\#\#\#}{Q}$$

$$0\cdot\bar{Q} + 0\cdot Q \rightarrow\rightarrow 0\cdot\bar{Q} + 1\cdot Q = Q$$

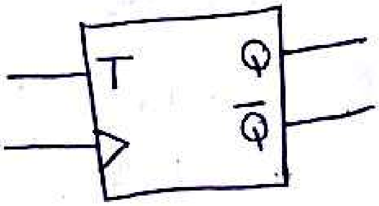
$$0\cdot\bar{Q} + 1\cdot Q \rightarrow\rightarrow 0\cdot\bar{Q} + 0\cdot Q = 0$$

$$1\cdot\bar{Q} + 0\cdot Q \rightarrow \rightarrow 1\cdot\bar{Q} + 1\cdot Q = 1$$

$$1\cdot\bar{Q} + 1\cdot Q \rightarrow \rightarrow 1\cdot\bar{Q} + 0\cdot Q = \bar{Q}$$

③ Toggle Flip Flop :

(one terminal)



T	Q^+
0	Q
1	$\overline{Q}$

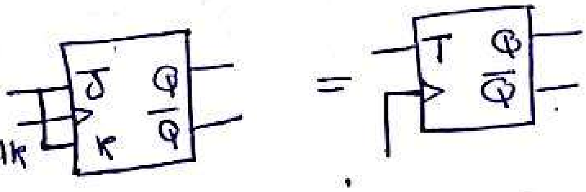
characteristic equation :

$$Q^+ = T\cdot\overline{Q} + \overline{T}\cdot Q \Rightarrow \boxed{T \oplus Q = Q^+}$$

$$0\cdot\overline{Q} + 1\cdot Q = Q$$

$$1\cdot\overline{Q} + 0\cdot Q = \overline{Q}$$

بنربط
JK and T



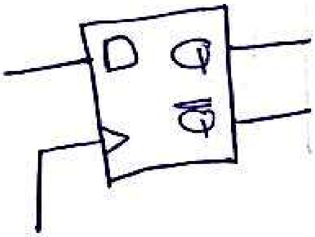
characteristic equation in truth table

J	K	Q^+
0	0	Q
1	0	1
0	1	0
1	1	$\overline{Q}$

note :-
بوخد المتشابهات
في J و K إلي نفس
بعض لانه هكذي بالوصية
نفس ال input .

---

④ Data flip flop :-

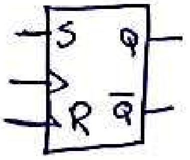
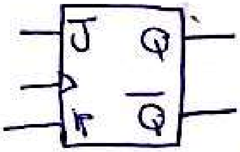
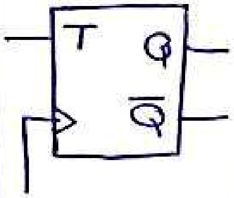
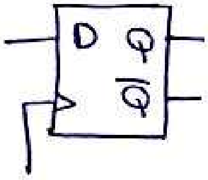


truth table

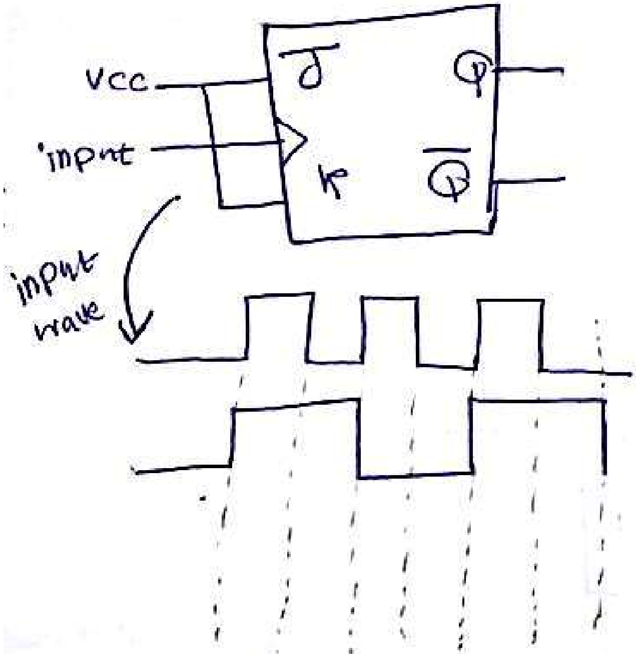
D	Q^+
0	0
1	1

characteristic equation =

$$\boxed{D = Q^+}$$

F/F	symbol	truth table	characteristic equation.
R.S		S | R | Q^+ 0 | 0 | Q 0 | 1 | 0 1 | 0 | 1 1 | 1 | not valid	Not eq because 1,1 → not valid.
J.K		J | K | Q^+ 0 | 0 | Q 0 | 1 | 0 1 | 0 | 1 1 | 1 | $\bar{Q}$	$Q^+ = J\bar{Q} \cdot \bar{K} \cdot Q$
T Toggle		T | Q^+ 0 | Q no change 1 | $\bar{Q}$ Toggel	$Q^+ = T \oplus Q$ متشابهات 0 ومختلفات 1
Data D		D | Q^+ 0 | 0 1 | 1	$D = Q^+$. input = out put

*Analoge and design.

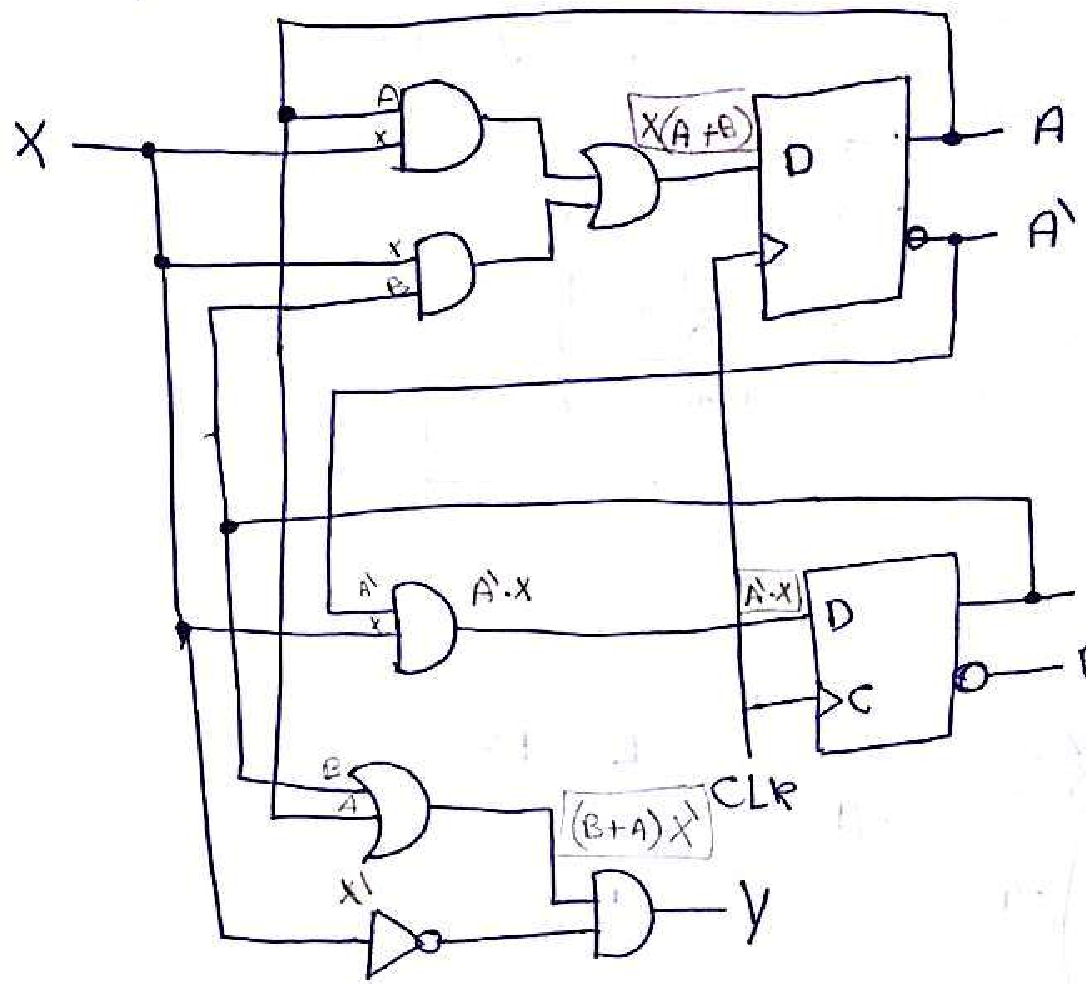


J	K	Q^+
0	0	$\bar{Q}$
0	1	0
1	0	1
1	1	$\bar{Q}$

عند الـ -ve edge

عند الـ +ve edge.

Example:-



input Combinational = 1 عدد / output Combinational = 1 عنصر

input sequential = 2 عنصر / output sequential = 2 عنصر

$D_A = A^+ = ((A+B)X)$

$D_B = B^+ = (A'.X)$

$Y = ((B+A)X')$

$\boxed{\text{Data Flbe Flob}}$

$\boxed{D = Q^+}$

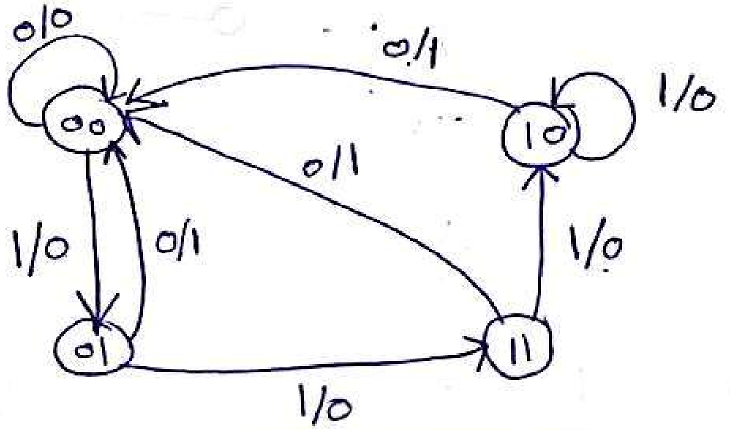
truth table.

A	B	X	A^+	B^+	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

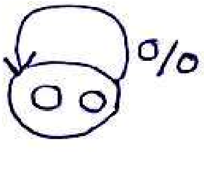
⟶

trut table design State diagram

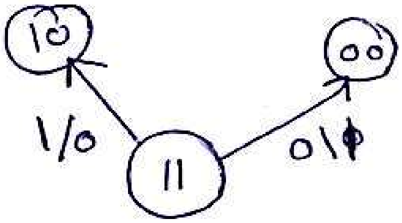
Present		Next state		y output	
A	B	$\overset{AB}{X}=0$	$\overset{AB}{X}=1$	X=0	X=1
0	0	0 0	0 1	0	0
0	1	0 0	1 1	1	0
1	0	0 0	1 0	1	0
1	1	0 0	1 0	1	0



Example : Taking First Line in the table State $\boxed{00}$ input $\boxed{0}$ Next State $\boxed{00}$ output y=0



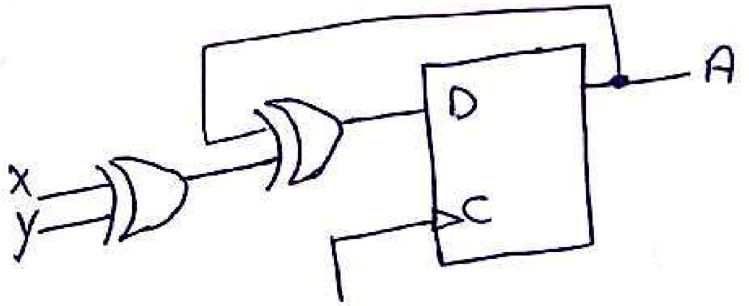
Example: Taking State $\boxed{11}$ input Can be $\underline{0}$ or $\underline{1}$ output is $\underline{1}$ or $\underline{0}$ next State is $\underline{00}$ or $\underline{10}$ (From table)?

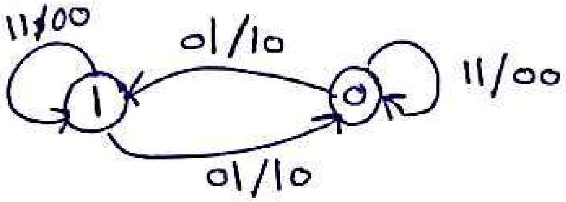


Analysis with D Flip-Flops:-

$D_A = A \oplus X \oplus Y$

A	xy	A^+
0	00	0
0	01	1
0	10	1
0	11	0
1	00	1
1	01	0
1	10	0
1	11	1





Analysis with JK

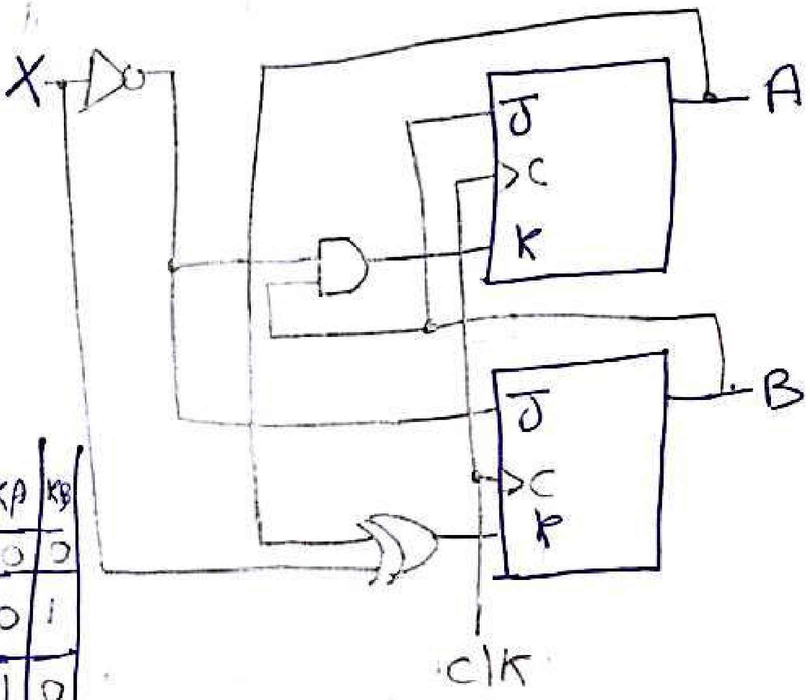
$J_A = B$

$J_B = X'$

$K_A = BX'$

$K_B = A'X + AX'$

$= A \oplus X$



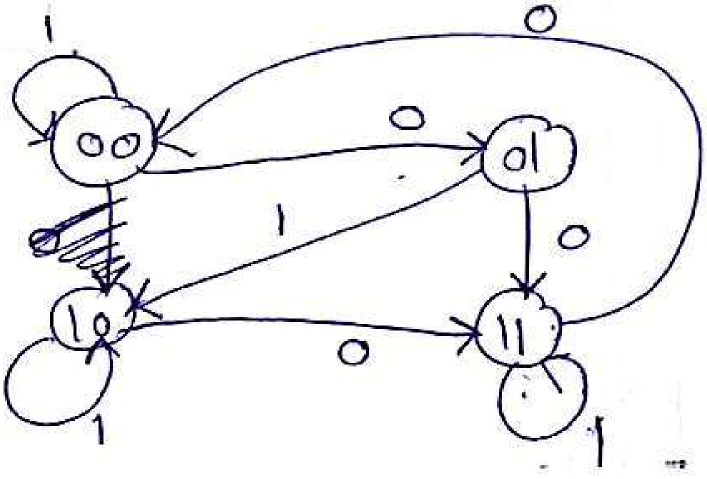
A B X	A^+ B^+	J_A	J_B	K_A	K_B
0 0 0		0	1	0	0
0 0 1		0	0	0	1
0 1 0		1	1	1	0
0 1 1		1	0	0	1
1 0 0		0	1	0	1
1 0 1		0	0	0	0
1 1 0		1	1	1	1
1 1 1		1	0	0	0

$$(J_A \cdot A') + (K'_A \cdot A) = A^+$$

$$\begin{pmatrix} 0 \cdot 1 \\ 0 \cdot 1 \\ 1 \cdot 1 \\ 1 \cdot 1 \\ 0 \cdot 0 \\ 0 \cdot 0 \\ 1 \cdot 0 \\ 1 \cdot 0 \end{pmatrix} + \begin{pmatrix} 1 \cdot 0 \\ 1 \cdot 0 \\ 0 \cdot 0 \\ 1 \cdot 0 \\ 1 \cdot 1 \\ 1 \cdot 1 \\ 0 \cdot 1 \\ 1 \cdot 1 \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 1 \\ 1 \\ 1 \\ 1 \\ 0 \\ 1 \end{pmatrix}$$

$$(J_B \cdot B') + (K'_B \cdot B) = B^+$$

$$\begin{pmatrix} 1 \cdot 1 \\ 0 \cdot 1 \\ 1 \cdot 0 \\ 0 \cdot 0 \\ 1 \cdot 1 \\ 0 \cdot 1 \\ 1 \cdot 0 \\ 0 \cdot 0 \end{pmatrix} + \begin{pmatrix} 1 \cdot 0 \\ 0 \cdot 0 \\ 1 \cdot 1 \\ 0 \cdot 1 \\ 0 \cdot 0 \\ 1 \cdot 0 \\ 0 \cdot 1 \\ 1 \cdot 1 \end{pmatrix} = \begin{pmatrix} 1 \\ 0 \\ 1 \\ 0 \\ 1 \\ 0 \\ 0 \\ 1 \end{pmatrix}$$



at K- map

$J_A = B$

$J_B = X'$

$K_A = BX'$

$K_B = A \oplus X$

$$A^+ = J_A \cdot A' + \overline{K_A} \cdot A$$

$$(B \cdot A') + (BX')' \cdot A = A^+$$

$$\boxed{A^+ = BA' + B'A + X \cdot A}$$

$$B^+ = J_B \cdot \overline{B} + \overline{K_B} \cdot B$$

$$\boxed{B^+ = (X' \cdot B') + (ABX) + (A \cdot X')}$$

A \ BX	00	01	11	10
0			1	1
1	1	1	1	

$A'B + AB' + X \cdot A$

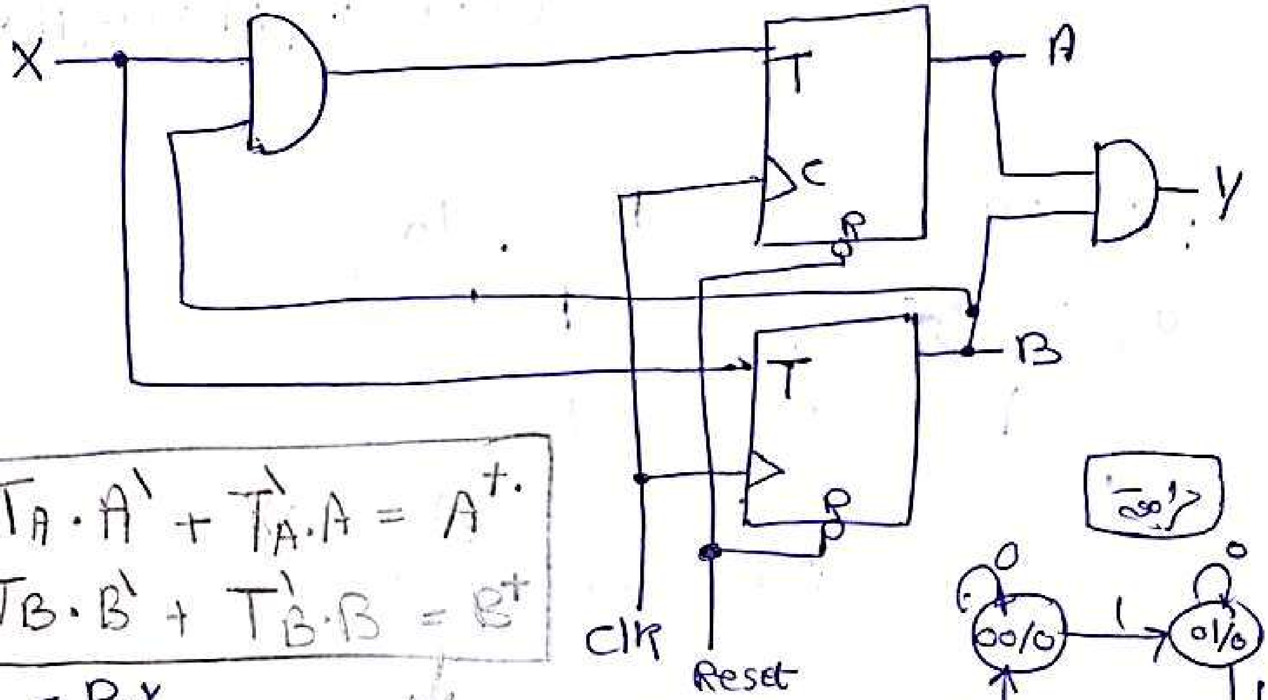
A \ BX				
	1	0	0	1
	1	0	1	0

$B'X' + ABX + AX'$

$$D = T \oplus Q$$

$$\boxed{Q(t+1) = TQ' + T'Q}$$

Analysis with T Flip Flop:



$$\boxed{\begin{array}{l} T_A \cdot A' + T'_A \cdot A = A^+ \\ T_B \cdot B' + T'_B \cdot B = B^+ \end{array}}$$

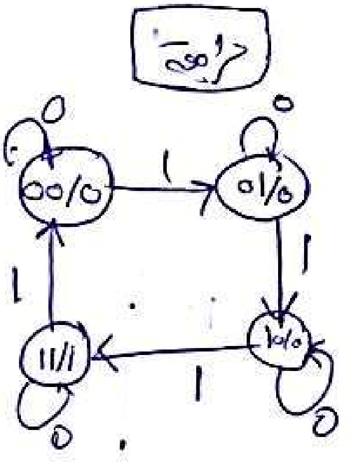
$T_A = BX$

$T_B = X$

$y = AB$

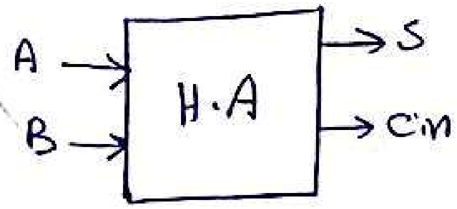
$$\boxed{B \cdot X \cdot A' + B'A + X'A}$$

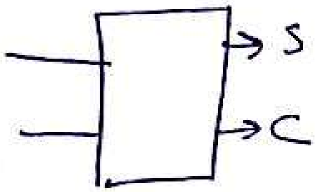
$$\boxed{X \cdot B' + X' \cdot B \cdot}$$

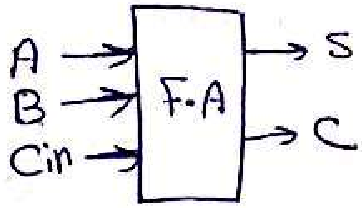


A	B	X	A^+	B^+	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1

How to make a full adder using half adders?

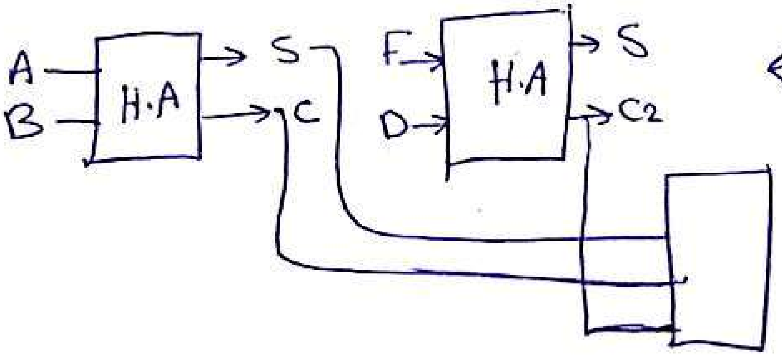




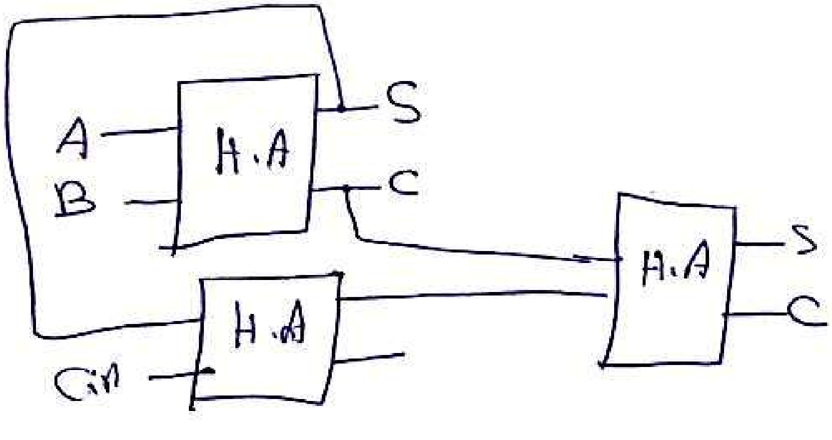


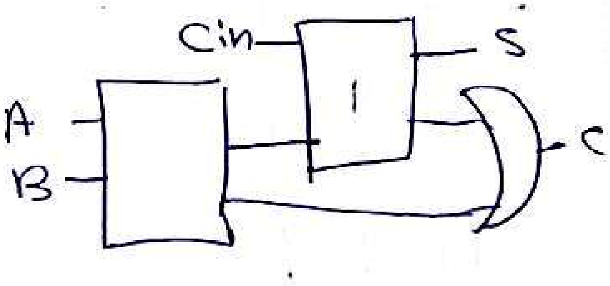
A	B	S	Cin
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

A	B	Cin	S	Co	cin
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	0	1	1
1	1	1	1	1	1



three half aders.





Excitation table:

العكس

① JK/F/F

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

$$\boxed{J\bar{Q} + \bar{K}Q =}$$

② T F/F

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

$$\boxed{D = T = Q \oplus Q^+}$$

T	Q^+
0	Q
1	Q'

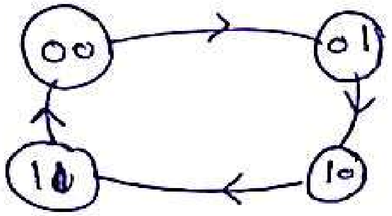
③ D F/F

$$\boxed{D = Q^+}$$

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

Example:- Design a 2 bit up Counter using

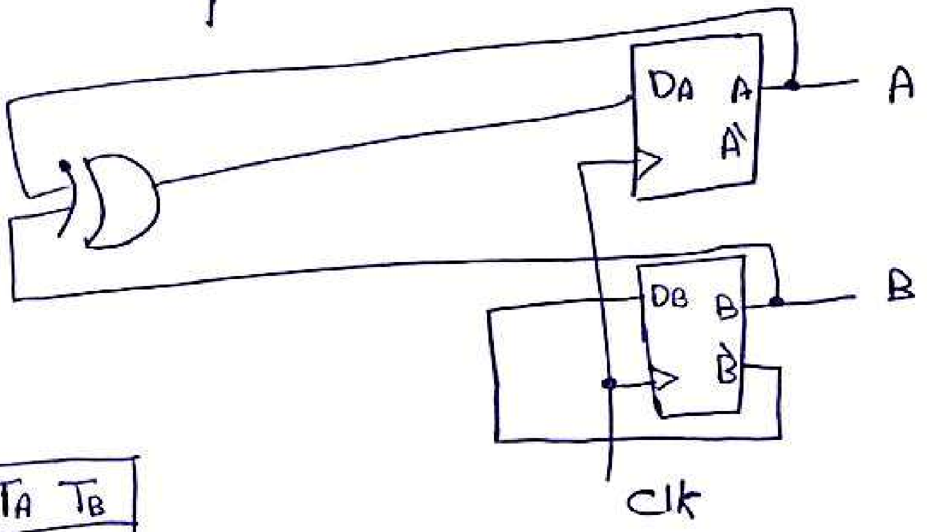
① D F/F ② T F/F ③ JK F/F



$D = Q^+$

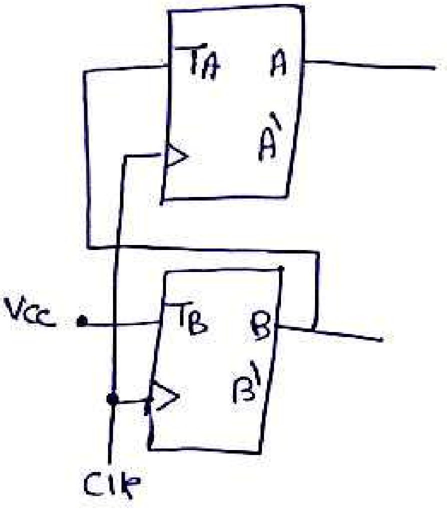
D F/F

input		output		D_A	D_B
A	B	A^+	B^+		
0	0	0	1	0	1
0	1	1	0	1	0
1	0	1	1	1	1
1	1	0	0	0	0



② using T F/F

A	B	B^+	A^+	T_A	T_B
0	0	1	0	0	1
0	1	0	1	1	1
1	0	1	1	0	1
1	1	0	0	1	1



①

Logic final

* Logical circuits *

① Combinational circuit :- No memory كل اللي قبل ما طفي بيتمسح

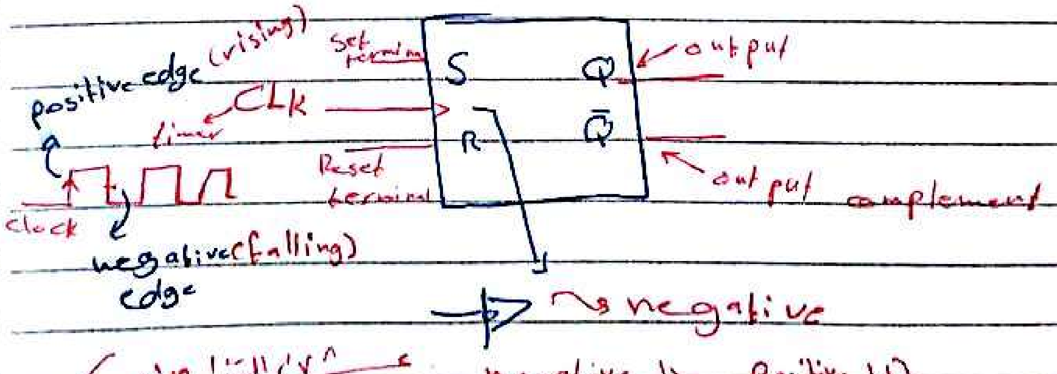
② Sequential circuit :- with memory.

bit → 0,1
byte → 8 bit
word → 16 bit
double word → 32 bit

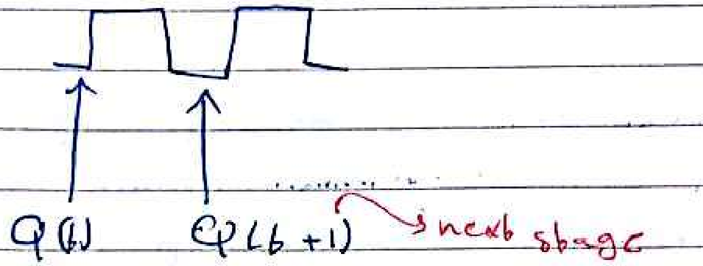
* Set reset flipflop :- :

Set to one / high } Reset to Zero / low

* Set Reset flip flop *



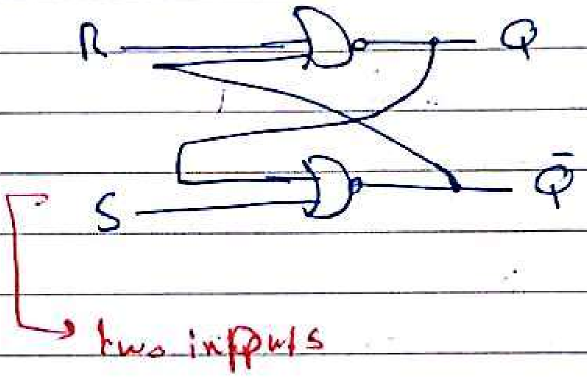
(الشكل [illegible]) negative ⊔ positive ⊔



Q — present state

بنشتغل عليها وبنتنبأ اللي وراها

Q^+



two inputs

هاد شكل ال memory

S	R	Q^+
0	0	Q
0	1	0
1	0	1
1	1	Not valid

Q^+ → next state

no change state

Reset state

set state

Not valid → لا zero يا once احنا ما بنعرف

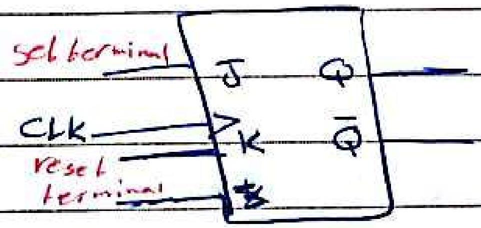
NOR ب

0	0	1
0	1	0
1	0	10
1	1	0

② JK flipflop (JK f/f)

Latch → without CLK → بتتغير على أي تغيير

flipflop → with clk → بس بتتغير على ال negative/ positive



* Characteristic table →

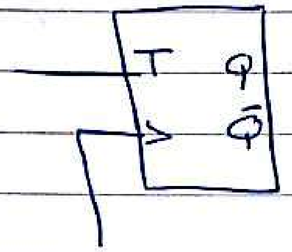
set → J	reset → K	Q^+ → next state	
0	0	Q	no change
0	1	0	reset
1	0	1	set
1	1	$\bar{Q}$	→ toggle (complement)

* Characteristic equation → أخذ ال Table

$$Q^+ = J\bar{Q} + \bar{K}Q$$

③ Toggle flip flop: $\boxed{T\ f/f}$

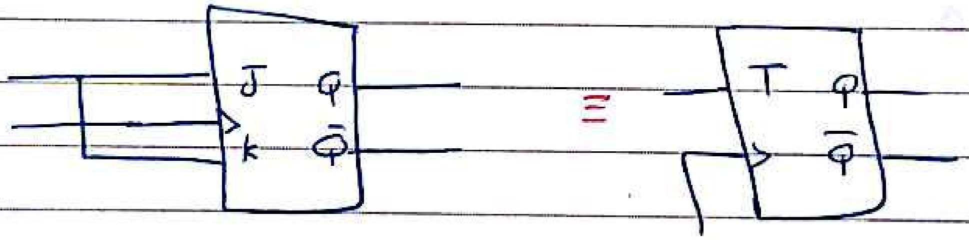
↳ one terminal



T	Q^+
0	Q
1	$\bar{Q}$

$$Q^+ = T\bar{Q} + \bar{T}Q$$
$$= T \oplus Q$$

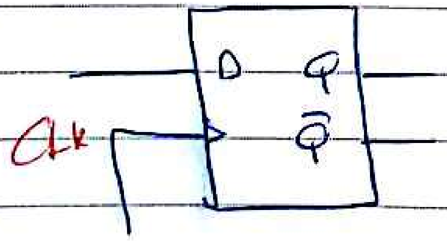
* How you do make a T f/f from JK f/f?



JK	Q^+
0 0	Q
0 1	0
1 0	1
1 1	$\bar{Q}$

أهم واحدة

④ Data flip flop $\boxed{D\ f/f}$



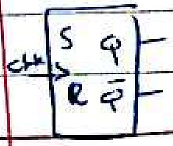
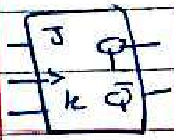
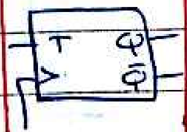
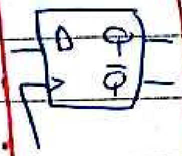
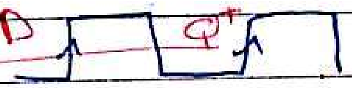
D	Q^+
0	0
1	1

$$\boxed{Q^+ = D}$$

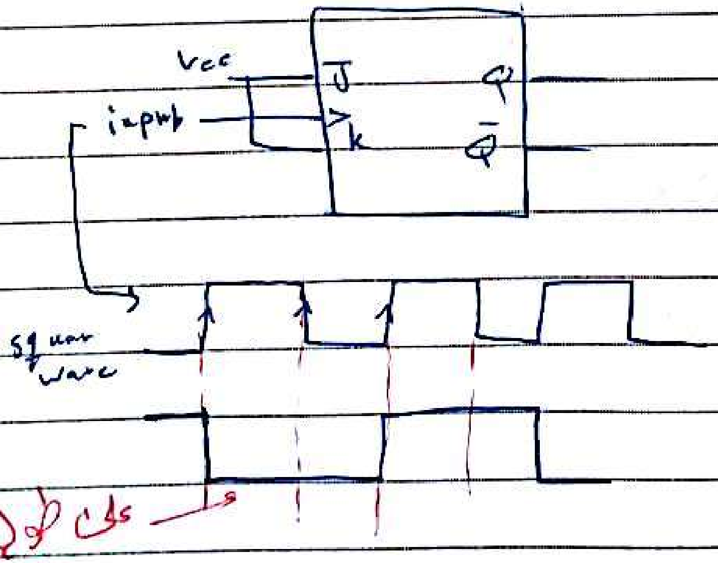
يعني ال Current state = next state

⑤

* إكتب الفرق بين set terminal و set state *

#	f/f	Symbol	char. table	char equation
①	RS		S R | Q^+ 0 0 | Q 0 1 | 0 1 0 | 1 1 1 | Not valid	—
②	J k		J k | Q^+ 0 0 | Q 0 1 | 0 1 0 | 1 1 1 | $\bar{Q}$	$Q^+ = J\bar{Q} + \bar{k}Q$
③	T Toggle		T | Q^+ 0 | Q 1 | $\bar{Q}$	$Q^+ = \bar{T}Q + T\bar{Q}$ $= T \oplus Q$
④	D Data		D | Q^+ 0 | 0 1 | 1	$Q^+ = D$  نفس بعض

* Analysis and design * عكس بعض



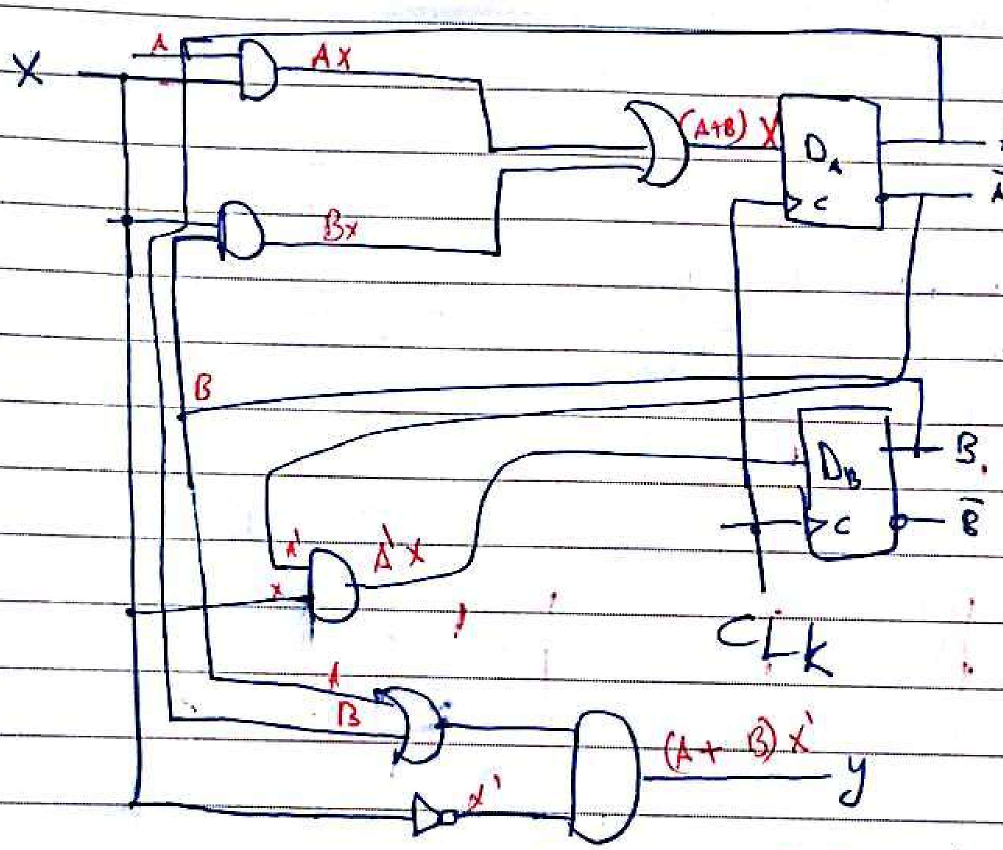
J	k	Q^+
0	0	q
0	1	0
1	0	1
1	1	$\bar{Q}$

على طول range العالي

انا هون بقال positive edge

Analysis using D f/f

مراجع بالدوسية



⟹ One input (combinational)
two sequential inputs

⟹ two sequential outputs
one combinational

$D = Q^+$

$D_A = A^+$

$D_B = B^+$

$A^+ = D_A = (A+B)X$

$B^+ = D_B = A'x$

$y = (A+B)\,x'$

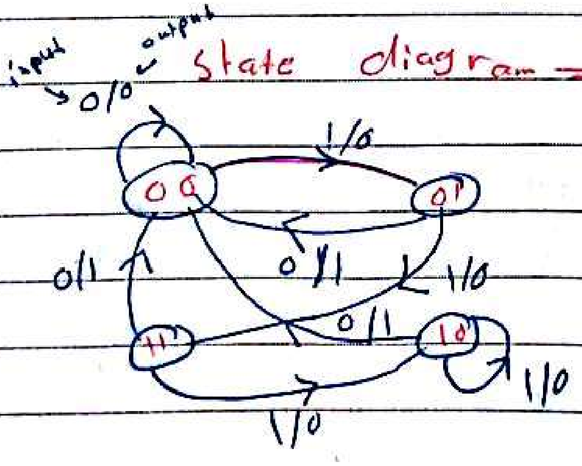
Truth table ⟹

A	B	X	A^+	B^+	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

State ~~diag~~ table

Present state		next state		output = ⓨ	
A	B	X = 0	X = 1	X = 0 y	X = 1 y
0	0	00	01	0	0
0	1	00	11	1	0
1	0	00	10	1	0
1	1	00	10	1	0

State diagram ← مو شرط الترتيب بس أعكس المطلوب
الي قبل هون ←

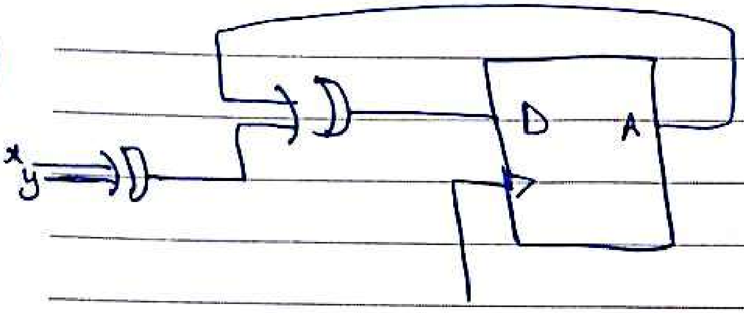


هاد design

8

ملاحظة * ممكن ما يكون في input / output وممكن input وممكن output
وممكن two inputs كـ

* Analysis using D f/f *



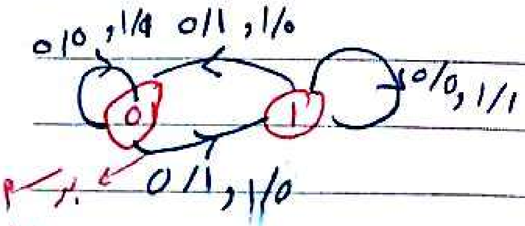
one sequential output
3 inputs

A	X	y	X ⊕ y	A^+
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

$A^+ = D = A \oplus (x \oplus y)$

x	y	x ⊕ y
0	0	0
0	1	1
1	0	1
1	1	0

State diagram



برسم بس path واحد [illegible]

مهم * عدد الدوائر يعتمد على عدد الـ sequential output +

$\boxed{2^1 = 2}$ 0 & 1

شرح الرسمة

الرسمة بالدوسية ص 76

A and B two sequantiol outputs

Comb. output لا 6

X → Combinational input

$$\left.\begin{array}{l} J_A = B \\ K_A = X'B \end{array}\right] \Rightarrow A^+ = J A' + K' A$$

$$= B A' + X'B \cdot A$$

$$= A'B + A(X + B')$$

$$= A'B + AX + AB'$$

$$= A \oplus B + AX$$

عندي طريقتين للحل

$2^3 \to 8$

① Table

A	B	X	A^{Next}	B^{Next}	J_A	K_A	J_B	K_B
					$\to B$	$\to X'B$	$\to X'$	$\to X \oplus A$
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	0
1	0	1	1	0	0	0	0	1
1	1	0	0	0	1	1	1	0
1	1	1	1	1	1	0	0	1

J	K	Q^+
0	0	Q
0	1	0
1	0	1
1	1	Q'

⑩

$A^+ = J_A \bar{A} + K_A' A$

$= B \bar{A} + (x'B)' A$

$= A'B + (X + B')A$

$= A'B + AB' + AX$

0 1 0/1   1 0 0/1   1 0/1 1

A^+ 5 ⑩ $\rightarrow m_2 + m_3 + m_4 + m_5 + m_5 + m_7$

Table [illegible]

$B^+ = J_B B' + K_B' B$

$= X'B' + (\overline{X \oplus A})B$

$= B'X' + (X \odot A)B$

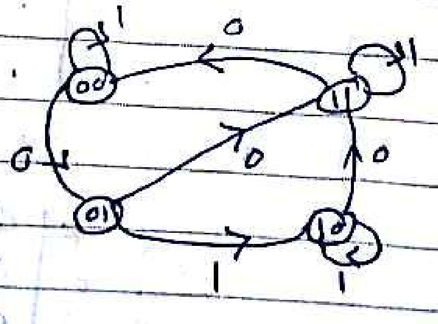
$= B'X' + ABX + A'BX'$.

0/1 0 0   1 1 1   0 1 0

$m_0 + m_4 + m_7 + m_2 \rightarrow B^+$

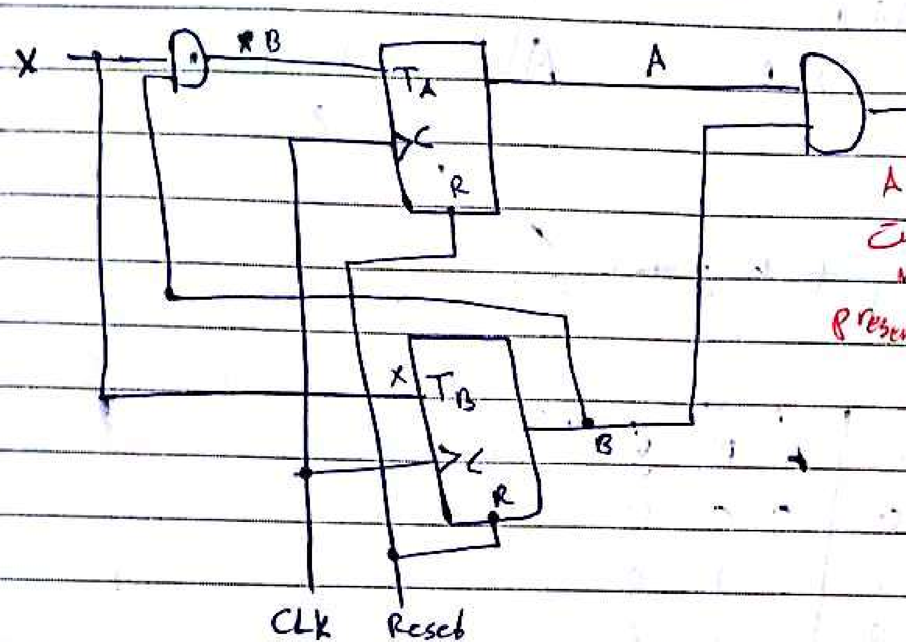
two flipflop $\rightarrow 2^2 \rightarrow$ circles

state diagram $\rightarrow$



ص 79 ← أدرسها

* Analysis using T flipflop *



إنتبه مش A^+B^+ ← لأني لسا ما وصلت next أنا جاي present

* two inputs one output combinational
* two inputs and one output sequential

$$A^+ = T_A \oplus A$$
$$= X_B \oplus A$$
$$= XBA' + \overline{XB}\,A$$
$$= A'BX + (X' + B')A$$
$$= A'BX + AX' + AB'.$$ ← ممكن أطلعها بالK-map

			B	
	0		1	
A'	1	1		1
		X	X	

$m_3 + m_4 + m_5 + m_6$

$B^+ = T_B \oplus B$

$= X \oplus B$

$= XB' + X''B$

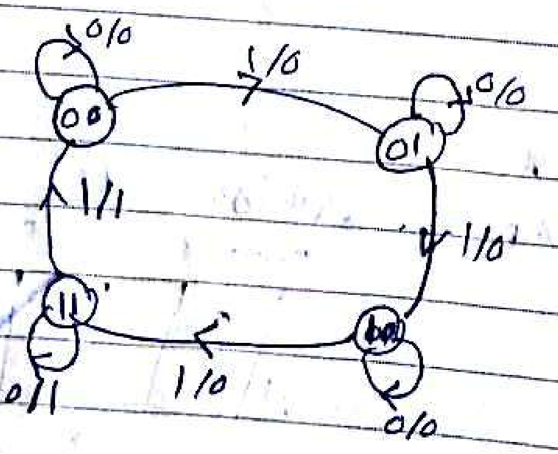
B

A				
		1		1
A		1		1

X

$m_1 + m_2 + m_5 + m_6$

			next		
A	B	X	A	B	y → AB
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1



* Excitation table * (حفظ بصم)

① JK f/f

Q	Q⁺	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

X → don't care (0 or 1)

J	K	Q^+
0	0	Q
0	1	0
1	0	1
1	1	Q'

② T f/f

T → $T = Q \oplus Q^+$

Q	Q⁺	T	
0	0	0	no change
0	1	1	Toggle
1	0	1	
1	1	0	

T	Q^+
0	Q
1	Q'

③ D f/f

Q	Q⁺	D
0	0	0
0	1	1
1	0	0
1	1	1

$$\boxed{D = Q^+}$$

RS مالها
لأن مفيش
Toggle

Scanned by CamScanner

سبحان الله .. والحمد لله .. ولا إله إلا الله .. والله

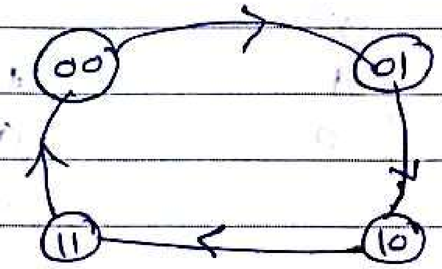
١٤

*Ex: ⟶ Design a 2 bits up counter using ⟶ ① D f/f ② T f/f ③ Jk f/f

(بدي أدرج رح أوضح)

(حفظ خطوات)

①



②

inputs		outputs		$D = Q^+$	
A	B	A^+	B^+	D_A	D_B
0	0	0	1	0	1
0	1	1	0	1	0
1	0	1	1	1	1
1	1	0	0	0	0

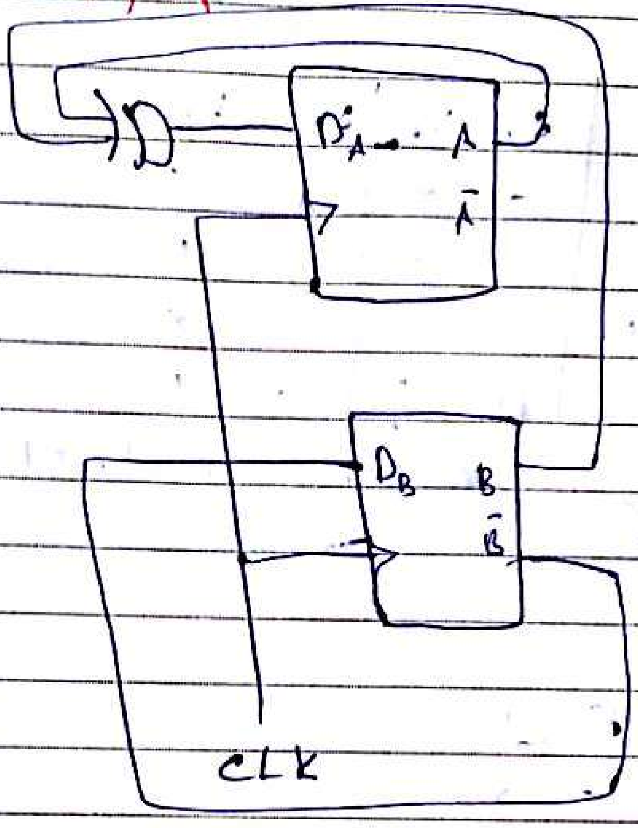
$D_A = A^+$

$D_B = B^+ = \bar{B}$

$A \oplus B$ B'

أو بالـ k-map

two flipflop



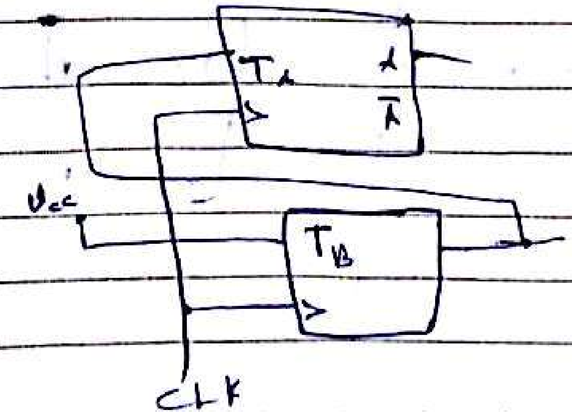
$D_A = A^+$

② using T f/f

A	B	A^+	B^+	T_A	T_B
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

$T_A = B$

$T_B = 1$ [illegible] V_{cc}



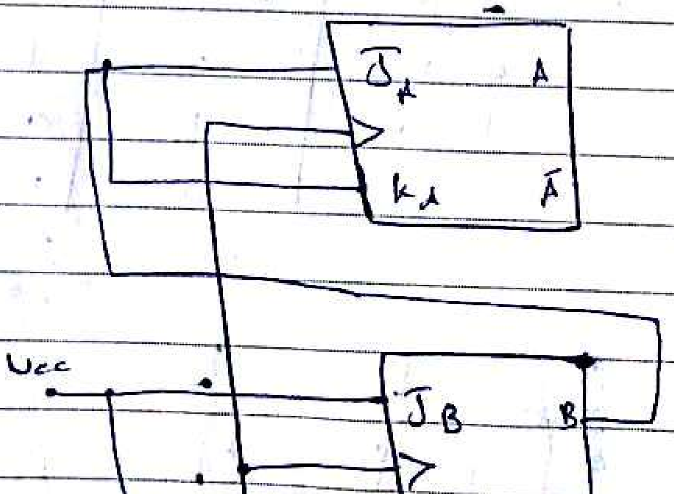
③ using JK f/f

		Next					
A	B	A	B	J_A	K_A	J_B	K_B
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	ɸ	ɸ	X	0	1	X
1	1	0	0	X	1	X	1

$J_A = K_A = B$ $J_B = K_B = 1$

↳ Recall

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



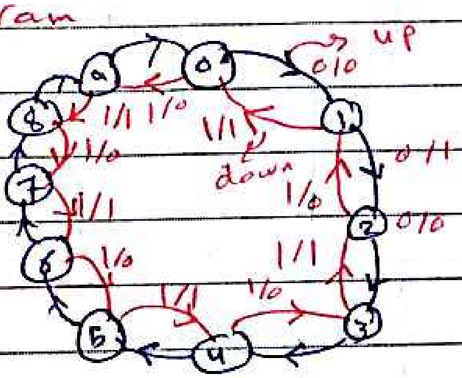
* Example ⇒ Design a one BCD digit up/down counter such that it will give an indication when the output count is even number using ⇒ D, T & JK f/f

تحليل السؤال ← ① BCD ← يعني من (0 - 9) بـ decimal

② up/down ← بدي أحط input عشان أعرف

③ even ← بدي أحط output

① State diagram



① let input X=0 up
X=1 down

y=0 odd
y=1 even

هنا لا يلزم أعمل coding لحتى أحول من خلالو Table

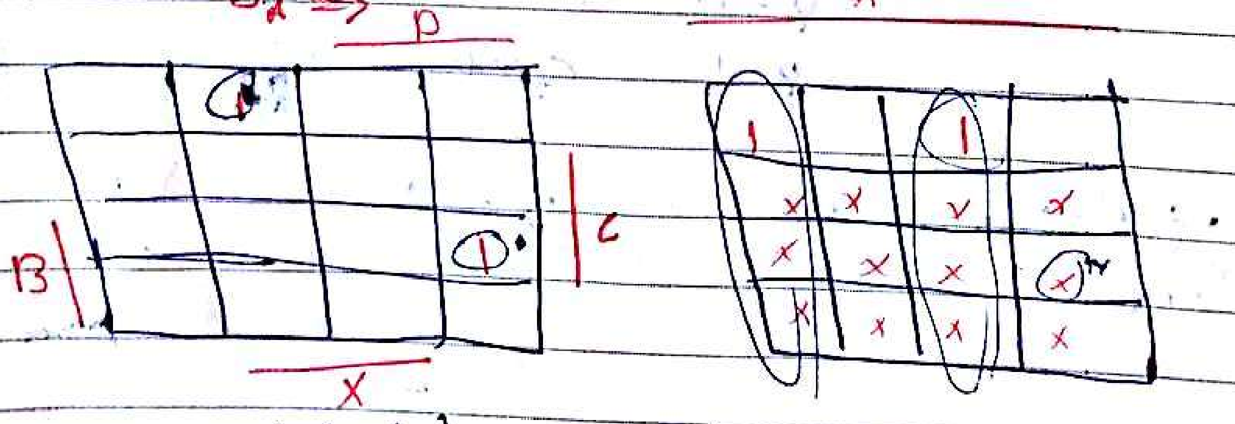
18

present						Next				
A	B	C	D	X		A	B	C	D	y
0	0	0	0	0	0	0	0	0	1	0
0	0	0	0	1	1	1	0	0	1	0
0	0	0	1	0	2	0	0	1	0	1
0	0	0		1	3	0	0	0	0	1
0	0	1	0	0	4	0	0	1	1	0
0	0	1	0	1	5	0	0	0	1	0
0	0	1	1	0	6	0	1	0	0	1
0	0	1	1	1	7	0	0	1	0	1
0	1	0	0	0	8	0	1	0	0	0
0	1	0	0	1	9	0	0	1	1	0
0	1	0	1	0	10	0	1	1	0	1
0	1	0	1	1	11	0	1	0	0	1
0	1	1	0	0	12	0	1	1	1	0
0	1	1	0	1	13	0	1	0	1	0
0	1	1	1	0	14	1	0	0	0	1
0	1	1	1	1	15	0	1	1	0	1
1	0	0	0	0	16	1	0	0	1	0
1	0	0	0	1	17	0	1	1	1	0
1	0	0	1	0	18	0	1	0	0	1
1	0	0	1	1	19	1	0	0	0	1
1	0	1	0	0	20	x	x	x	x	x
1	0	1	0	1	21	x	x	x	x	x
1	0	1	1	0	22	x	x	x	x	x
1	0	1	1	1	23	x	x	x	x	x
1	1	0	0	0	24	x	x	x	x	x
1	1	0	0	1	25	x	x	x	x	x
1	1	0	1	0	26	x	x	x	x	x
1	1	0	1	1	27	x	x	x	x	x
1	1	1	0	0	28	x	x	x	x	x
1	1	1	0	1	29	x	x	x	x	x
1	1	1	1	0	30	x	x	x	x	x
1	1	1	1	1	31	x	x	x	x	x

مش موجود
رقم ٢٠ =
فبعتبروا
don't care

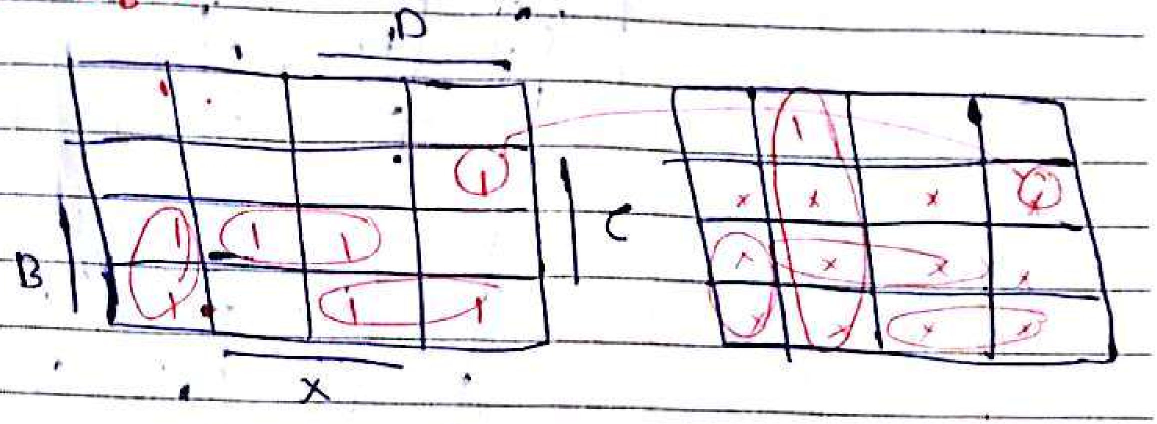
$D^{+} = D'$ // $y = D$ → k-map الباقي

for $D_A \Rightarrow$



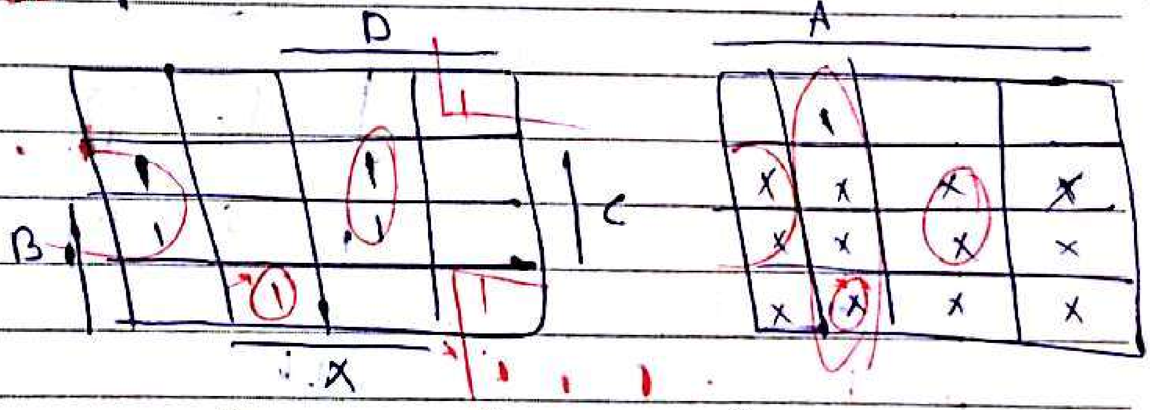
$$D_A = A'B'C'D'X + AD'X' + ADX + BCDX'$$

for $D_B \Rightarrow$



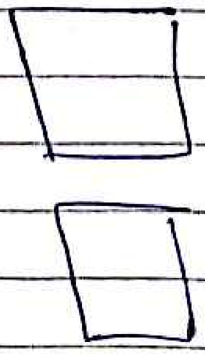
$$D_B = B^+ = BD'X' + BCX + BC'D + B'CDX' + AD'X$$

for $D_C \Rightarrow$

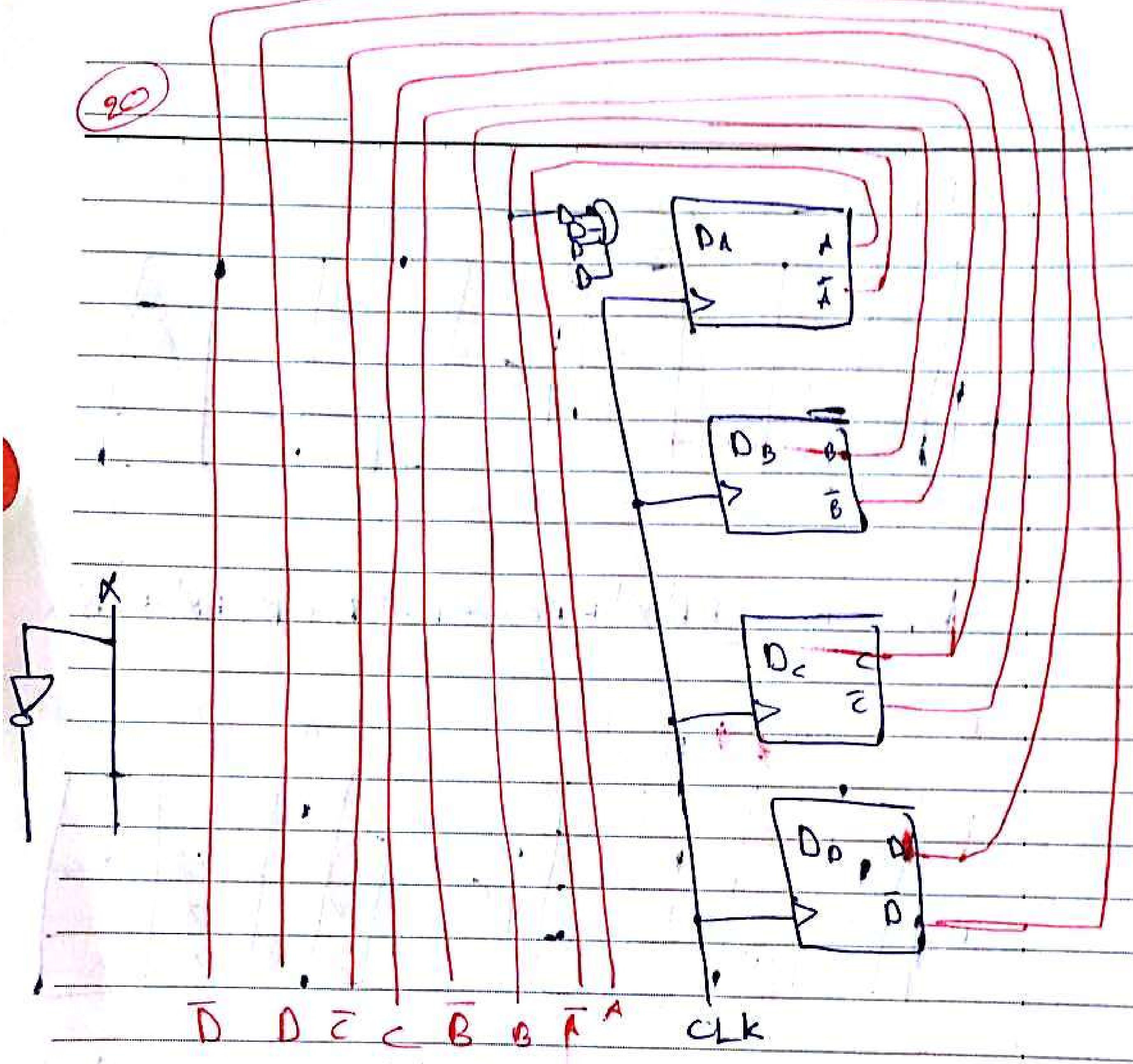


$$D_C = C^+ = CD'X' + BC'D'X + CDX + A'C'DX' + AD'X$$

~~for~~ implementation ⇒

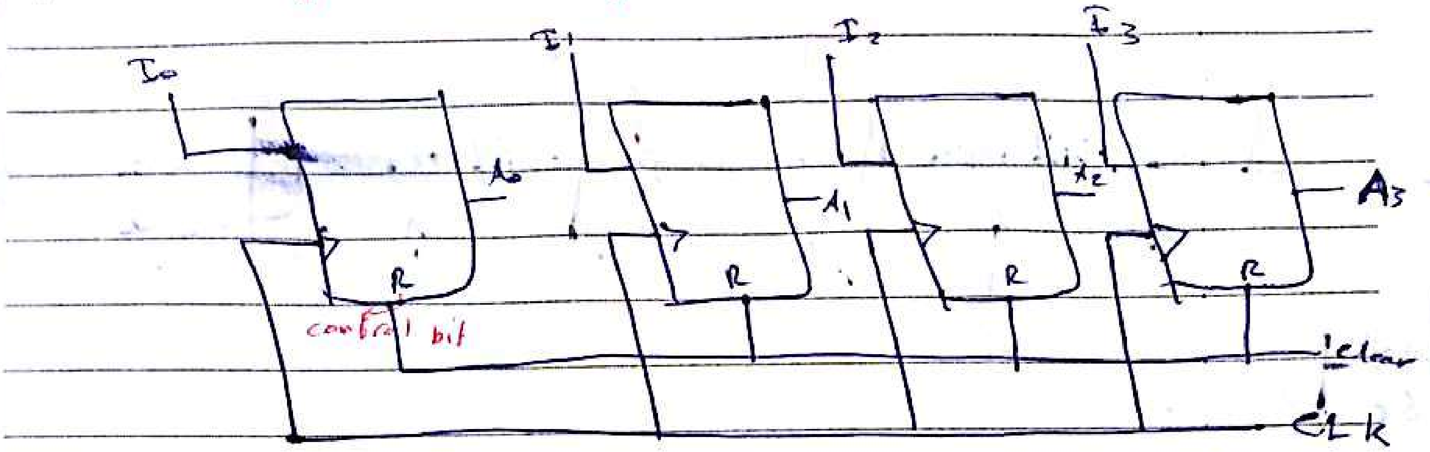


20



** من هون رح يصير كل الاعتماد على الدوسية والدراسة منها

** 4-bit parallel in parallel out register.

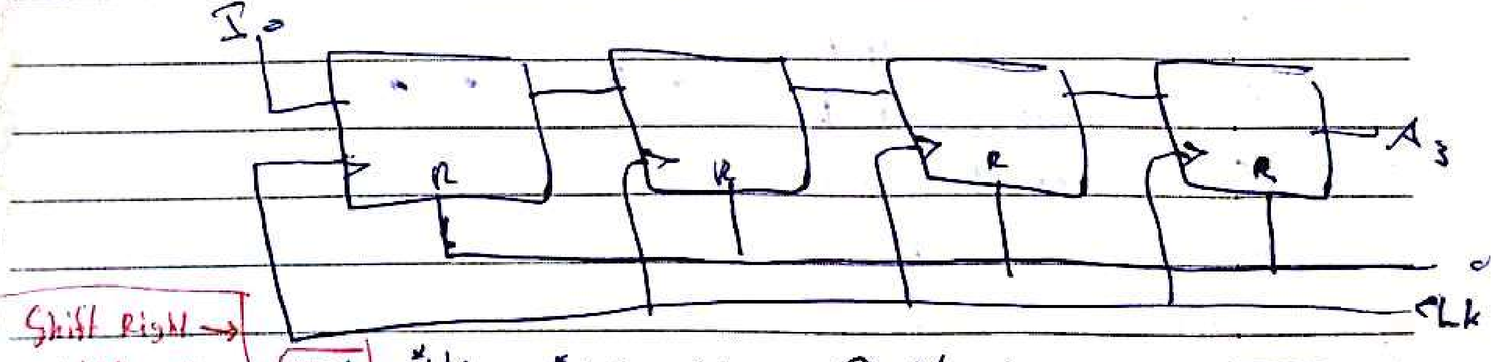


{ parallel → chanel by chanel
serial → bit by bit

+ هون ما بعطيني ال data إلا بعد one cycle لأنو seguantial

→ present ≠ next

* Serial in / serial out *



Shift Right →
shift left ←

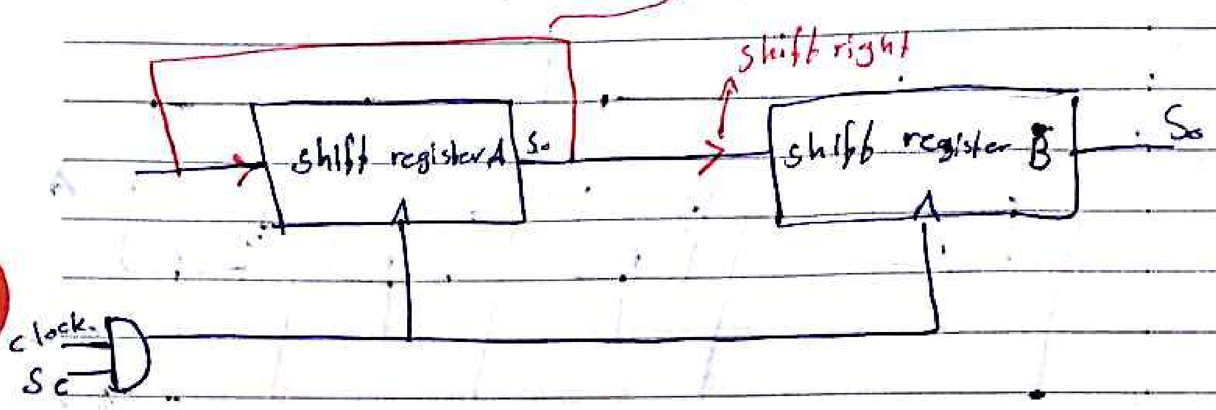
1101 ← اطلع بدي ~ data →

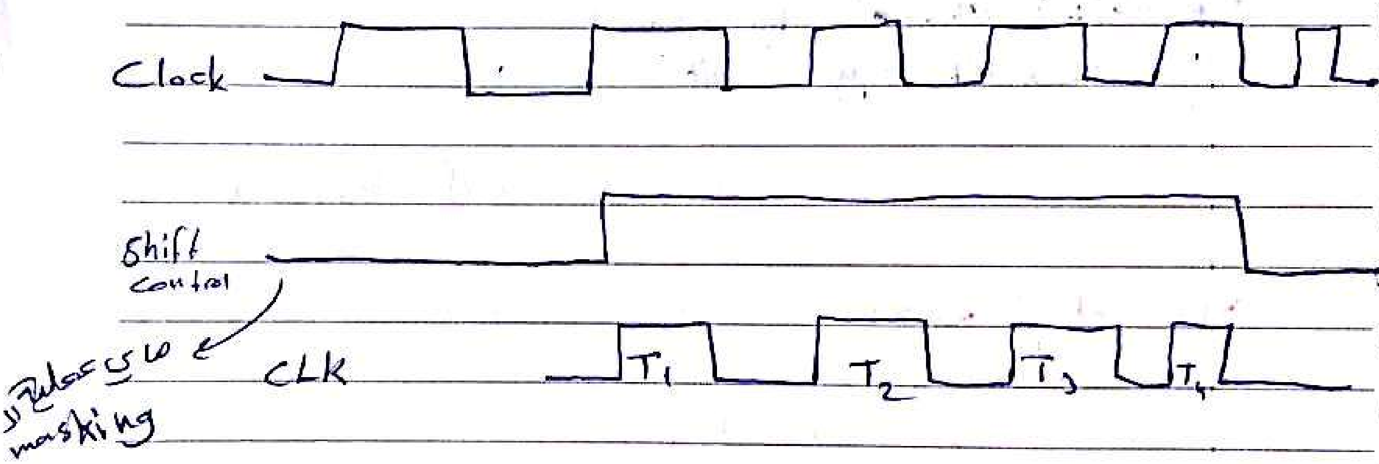
هاد shift right

① X X X X
② 1 X X X
③ 0 1 X X
④ 1 0 1 X
⑤ 1 1 0 1

بدي أربع cycle عشان أدخل ال data وبدي رابعة عشان أقرأها

* Serial Transfer * → shift right rotate



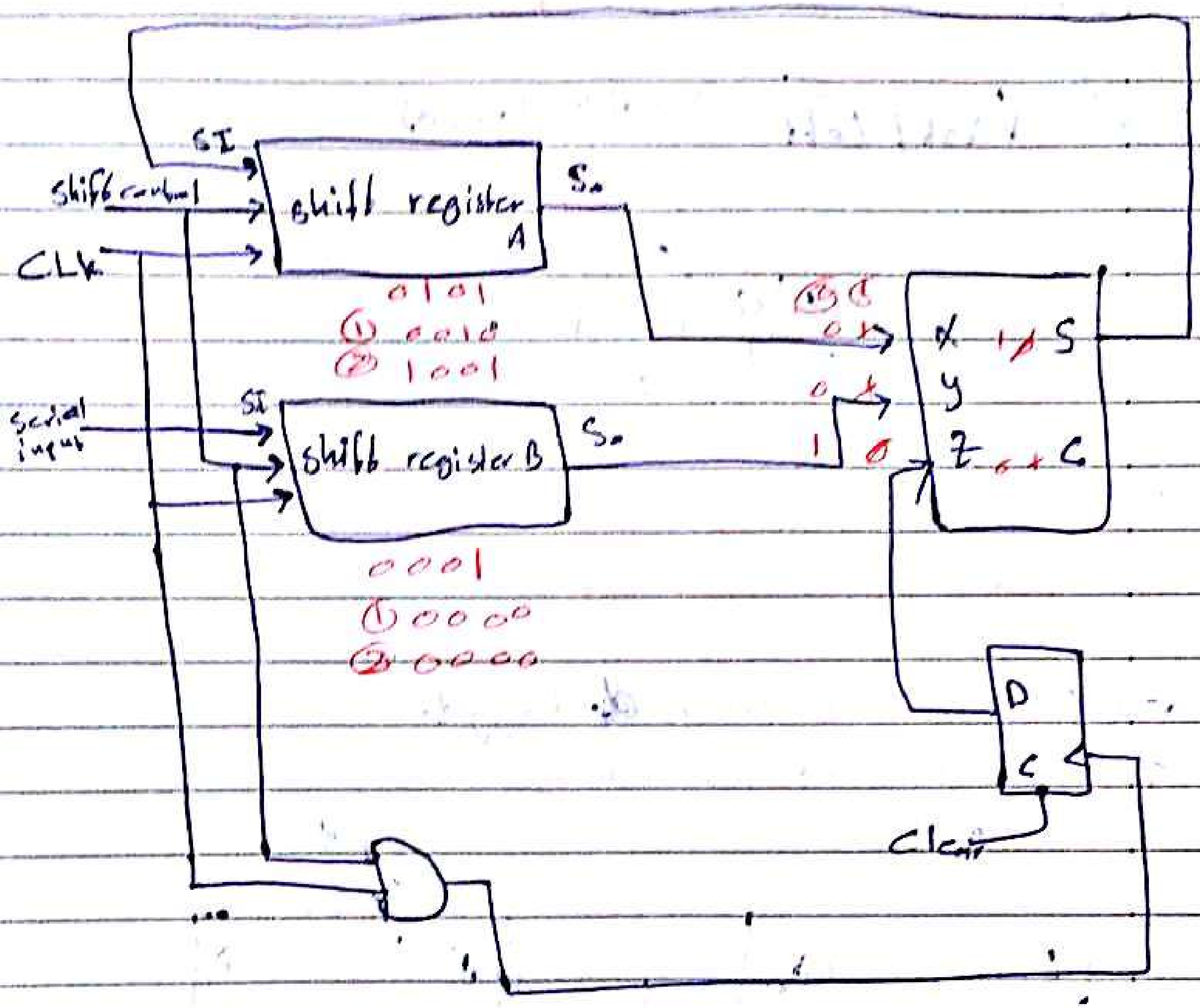


S_o = serial output
S_c = shift control
S_I = serial input

	A	B
zero عاد rotate جاي	0100	1110
أول cycle ①	0010	0111
②	0001	0011
	1000	1001
	0100	0100

لما رجع لنفس القيمة

* Serial adder *

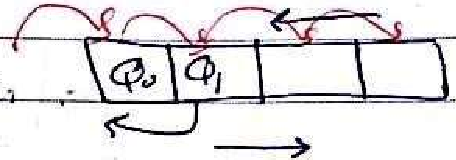


ص87 بالوثيقة ← موجودة

4-bit shift left / right register

active high → Right / $\overline{\text{Left}}$ → active low (0)

Control bit.

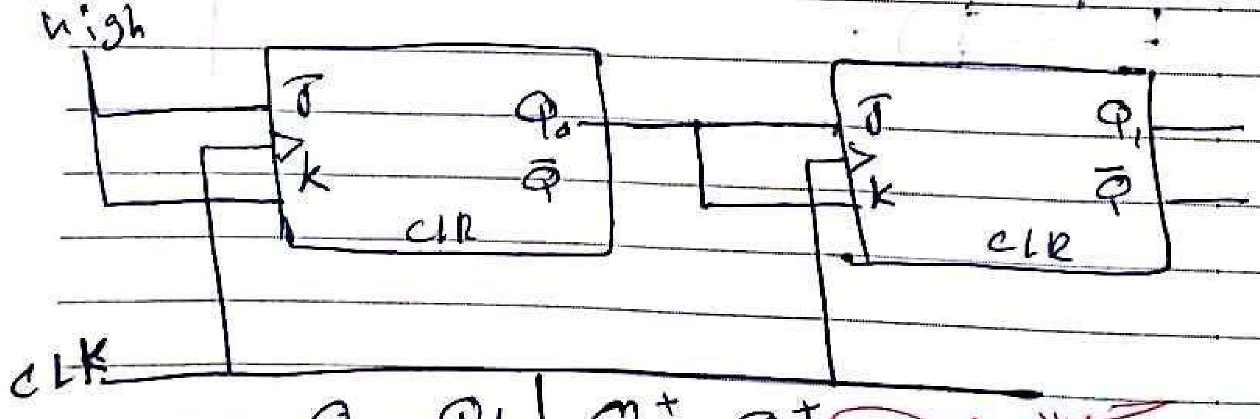


إذا ربطنا Jk مع ال Vcc ← Toggle

〃 〃 〃 مع بعض ← T f/f

T f/f → ones → always Q0 toggle

→ zero → no change



Q_0	Q_1	Q_0^+	Q_1^+
0	0	1	0
0	1	1	1
1	0	0	1
1	1	0	0

Q_1^+ → باعتماد Q0

← no change

← Toggle

إذا zero → no change

إذا one → Toggle

م 90 ← Binary counter مهم

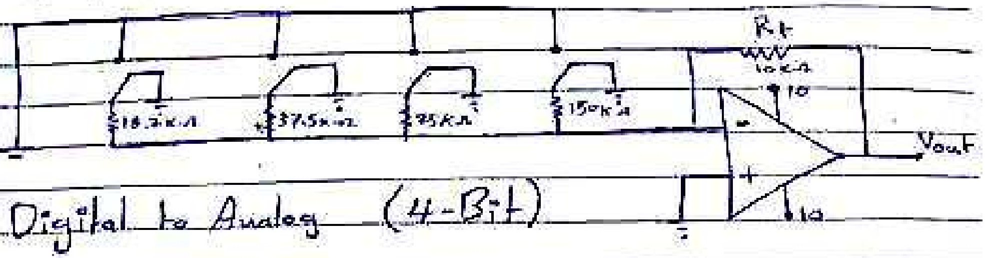
م 101 + م 102 // مهمة جداً جداً

+ م 103

لآخر الدوسية دراسة كامل

(حفظ كل إشي) مهم جداً

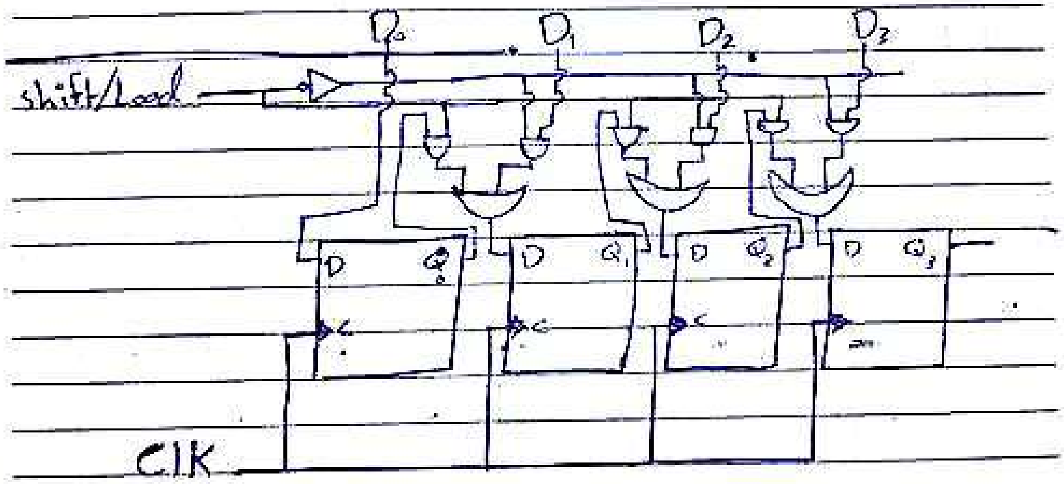
Region	V_{cc} (v)	V_{CE} (v)	current relation
Cut-off	< 0.6	O.C	$I_B = I_c = 0$
Active	$0.6 - 0.7$	> 0.8	$I_c = h_{ff} I_B$
Saturation	$0.7 - 0.8$	0.2	$I_B \geqslant \frac{I_c}{h_{ff}}$



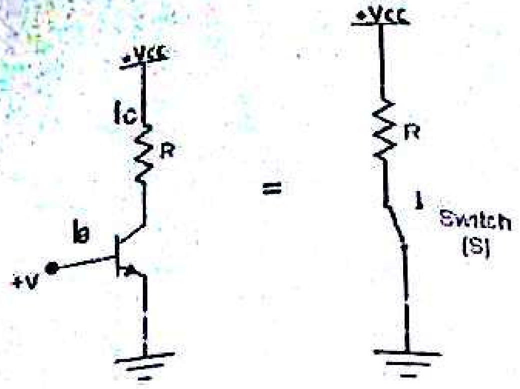
Digital to Analog (4-Bit)

DAC

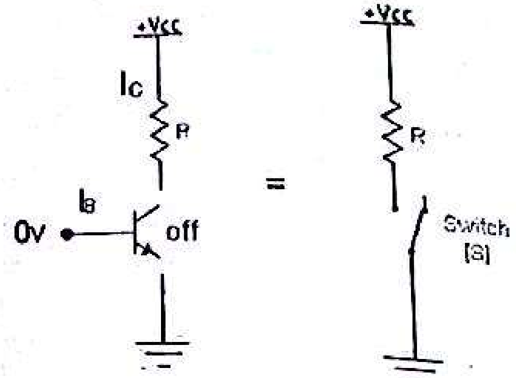
- Mosfit → 3v
- Bipolar → 5v



Parallel in Serial out shift Register



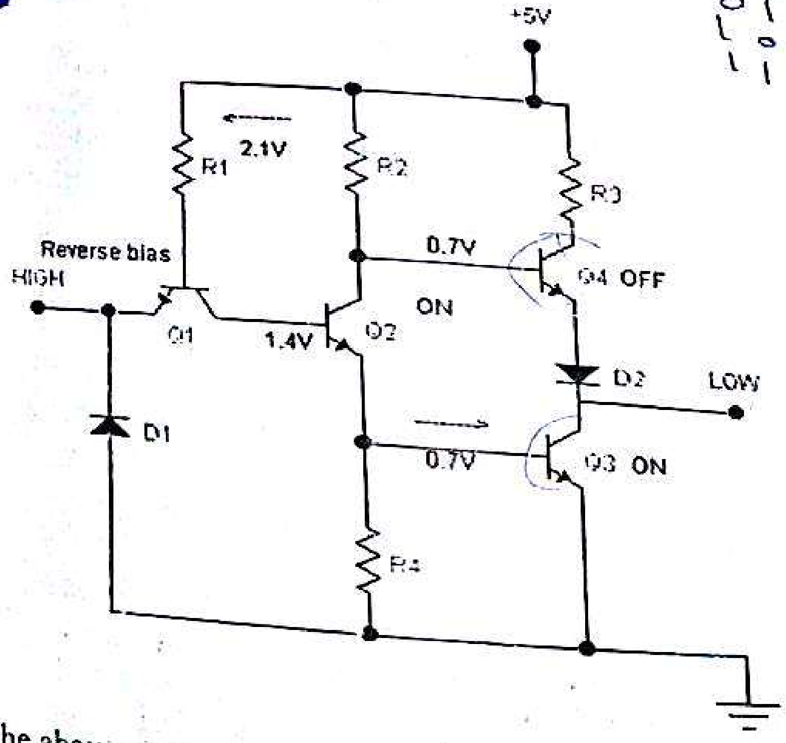
Saturated (ON) Transistor closed switch, ideal switch equivalent



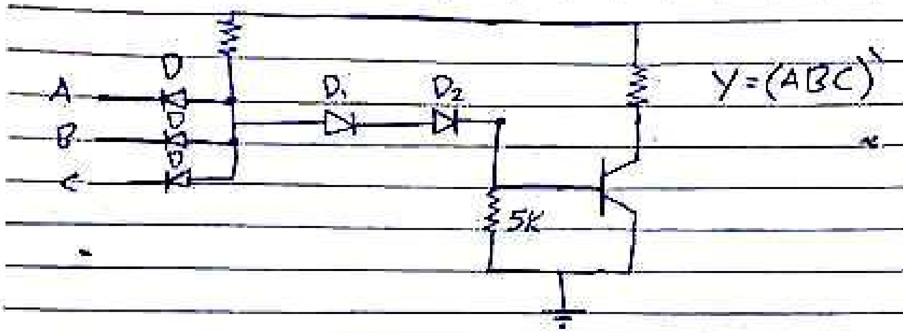
Off Transistor , ideal switch equivalent

TTL inverter

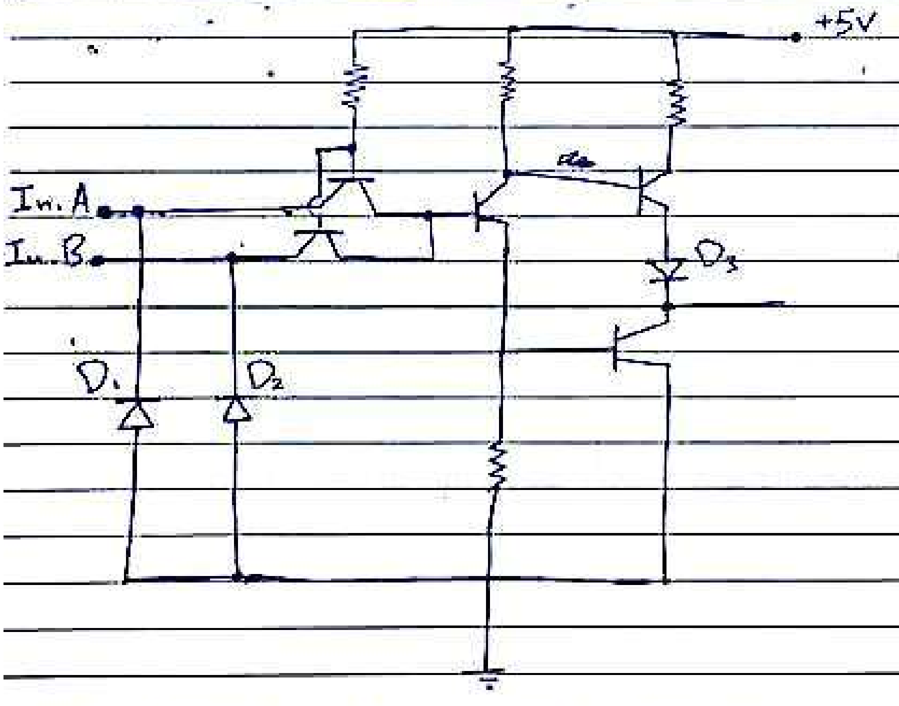
A	B	output
0	0	1
0	1	1
1	0	1
1	1	0



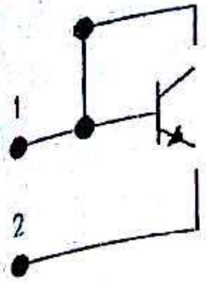
The above arrangement is called totem – pole arrangement.



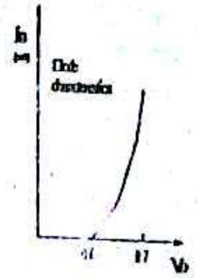
DTL NAND Gate

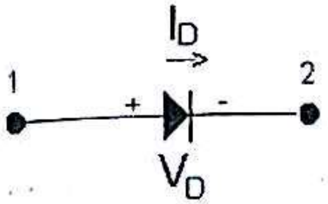


TTL NAND Gate



Transistor adapted for use as a diode





Diode graphical symbol

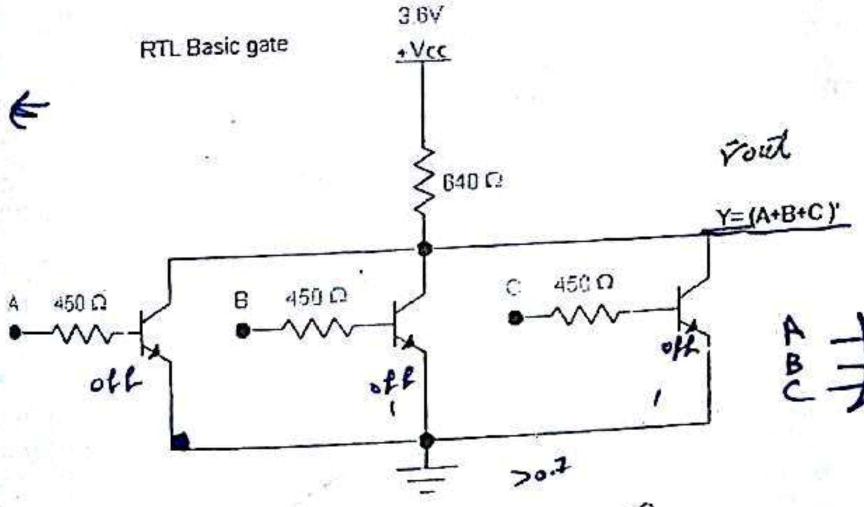
The diode is off and non – conducting when its forward voltage V_O is less than 0.6 V. When diode conducts $V_D = 0.7V$ and I_D flows in the direction of the arrow.

A diode or "Rectifier" is any device through which electricity can flow in one direction only.

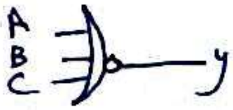
Resistor - transistor Logic

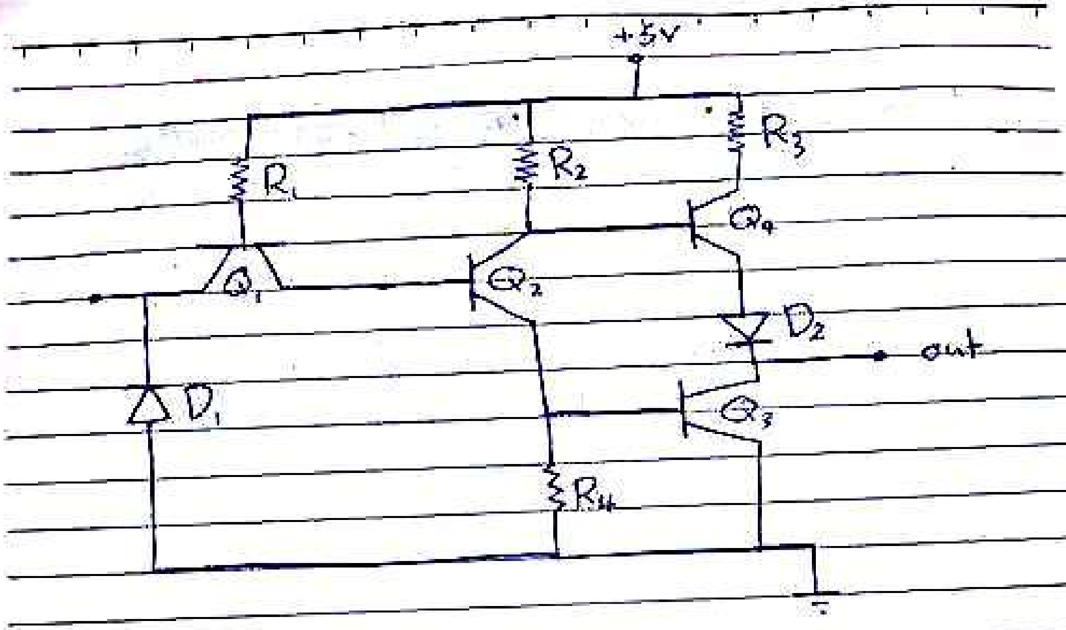
RTL Basic Gate

RTL Basic gate

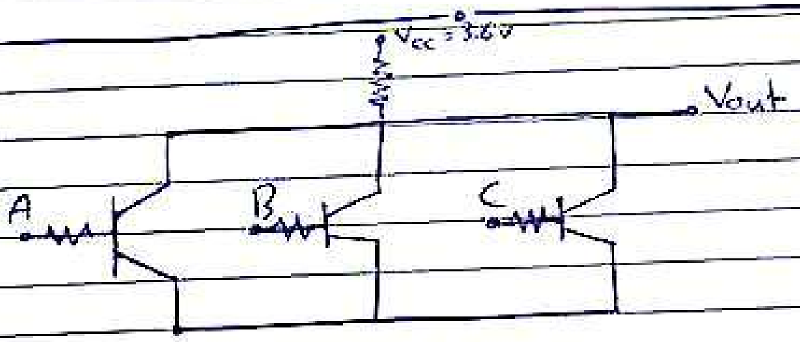


nor





TTL

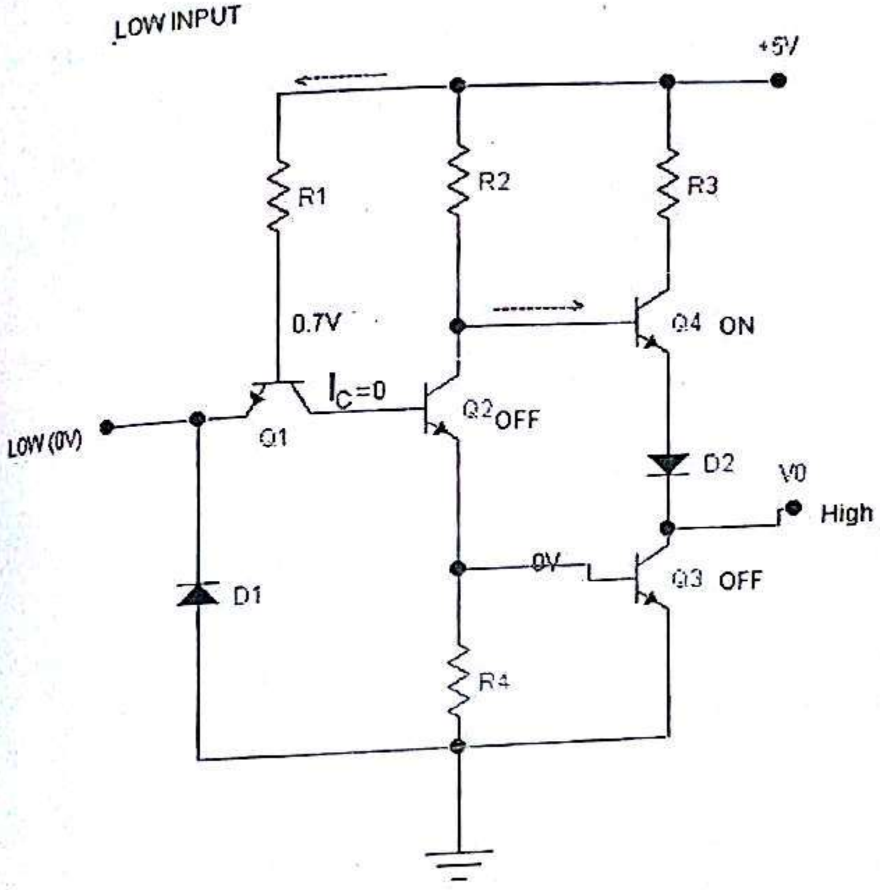


RTL (NOR)

When the input is high the base emitter junction of Q1 is reverse biased and the base – collector junction is forward biased. This condition permits current through R1 and the base – collector junction of Q1 into the base of Q2 thus driving Q2 into saturation as a result Q3 is turned on by Q2 and its collector voltage which is the output is near ground potential.

We therefore have a low output for a high input, at the same time, the collector of Q2 is at sufficiently low voltage level to keep Q4 off.

Low input



When the input is LOW, the base – emitter junction of Q1 is forward biased and the base – collector junction is reverse biased. There is current through R1 and the base – emitter junction of Q1 to the LOW input. A LOW provides a path to ground for the current. There is no current into the base of Q2, so it is off. The collector of Q2 is high

Digital Integrated Circuits

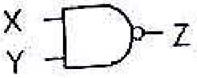
The IC digital logic families to be considered here are:

RTL	Resistor Transistor Logic
DTL	Diode Transistor Logic
TTL	Transistor – Transistor Logic
ECL	Emitter – Coupled Logic
MOS	*Metal – Oxide semiconductors*
CMOS	*Complementary Metal Oxide Semiconductor*

RTL & DTL have only historical significance since they are no longer used in digital systems RTL was the first commercial family to be used extensively.

DTL have been replace by TTL, In fact TTL is a modification of DTL gate.

The basic circuit in each IC digital logic family is either a NAND or NOR gate this basic circuit is the primary building Block from which all other more complex digital components are obtained.



X	Y	Z
L	L	H
L	H	H
H	L	H
H	H	L

Positive Logic Nand Gate

X	Y	Z
L	L	H
L	H	L
H	L	L
H	H	L

Positive Logic Nor Gate

A Bipolar junction transistor (BJT) can be either an npn or pnp junction transistor. Field – effect transistors are said to be Unipolar. The operation of a bipolar transistor depends on the flow of two types of carriers electronics and holes a unipolar Transistor depends on the flow of only one type of majority carrier which may be electronics (n – channel) or holes (p – channel) RTL, DTL, TTL, ECL are Bipolar Transistors.

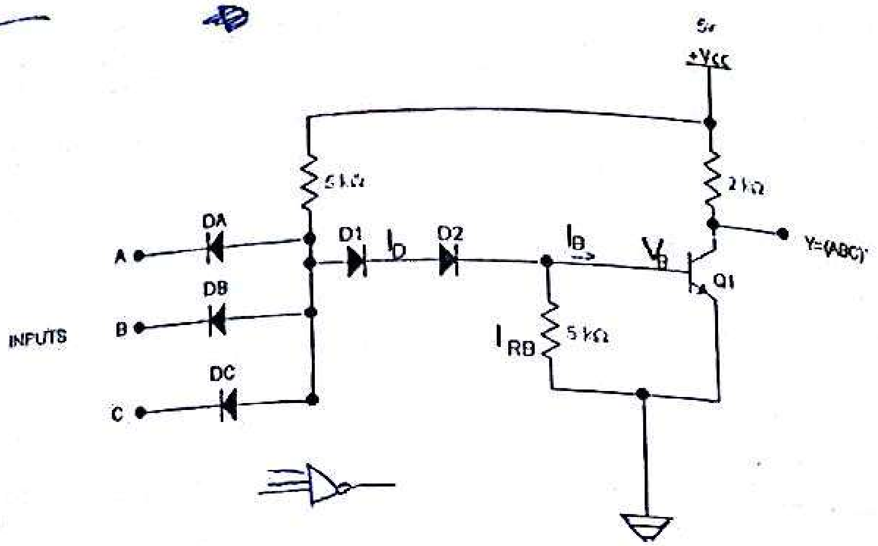
MOS and CMOS employ a type of unipolar transistor called metal – oxide – semiconductor field effect Transistor MOSFET.

IF any input of the RTL gate is High (A, B, C) the corresponding transistor is driven into saturation. This causes the output to be low, regardless of the states of the other transistor. If all inputs are low (0.2 V) all transistors are cut off because $V_{BE} < 0.6V$. This causes the output to be high, approaching the value of supply voltage V_{CC}.

DTL Basic gates

The basic circuit in the DTL logic family is the NAND gate shown below.

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



The transistor serves as a current amplifier while inverting the digital signal. If any input is low (0.2 V) the corresponding input diode conducts current. This means that the diode is forward biased and here is a voltage drop of 0.75 Volts.
But at output there is 0.2V the means that point P is 0.75 + 0.2 = 0.95V.

0.95 volts is not enough to forward bias D1, D2.

Therefore Q1 is cut off and Y=V_{CC} High.

$$V_B = V_P - V_{D1} - V_{D2} = 0.95 - 0.65 - 0.65 = -0.35v$$

$$\therefore$$

$$I_{RB} = \frac{V_{B2} - 0}{5*10^{-3}} = \frac{0.35}{5*10^{-3}} = 0.07mA$$

If all inputs are simultaneously at logic level 0 the current through resistor R will divide among the diodes D_A, D_B, D_C. Thus Vp decreases slightly and Q_1 is forced further into cutoff. Hence Vo remains at logic 1.

h_{FE} = Transistor parameter called dc current gain

mportant to remember that I_C maximum does not depend on I_B. looking at gram line V_{cc} is maximum when $V_{CE} = 0$ this gives

$$I_C = \frac{V_{CC}}{R_C}$$

aturation

e condition for saturation is determined from the relationship

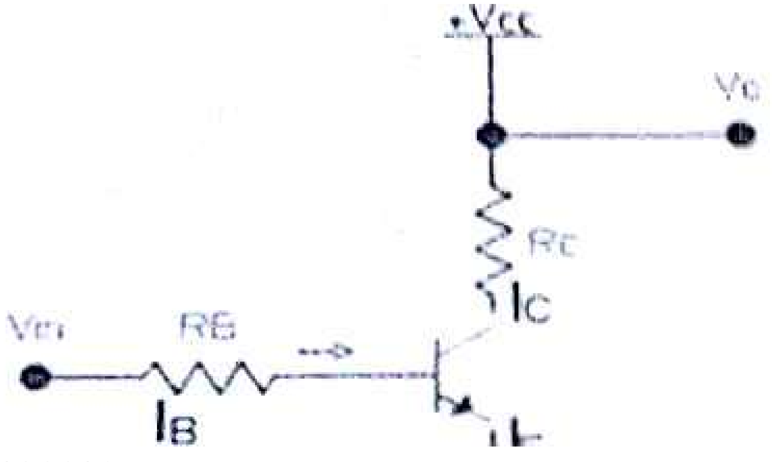
$$I_B \geq \frac{I_C}{h_{FE}}$$

uring saturation V_{CE} is not exactly 0 but almost equal to 0.2 V. V_{BE} hardly changes.

pical npn silicon Transistor Parameters

Region	V_{BE} (Volts)	V_{CE} (volts)	Current Relationship
Cut-off	<0.6	Open circuit	$I_B = I_C = 0$
Active	0.6-0.7	>0.8	$I_C = h_{FE} I_B$
Saturation	0.7-0.8	0.2	$I_B \geq I_C/h_{FE}$

c



V_{BE} is less than 0.6V, transistor cut – off $I_B = 0$, $I_C = 0$, the collected to emitter circuit behaves like an open circuit (i.e. switch off).

Active region

V_{CE} may be any where between 0.8V up to V_{CC}

$$I_C = I_B h_{FE}$$

h_{FE} = Transistor parameter called dc cutrrent gain

It is important to remember that I_C maximum does not depend on I_B. looking at diagram line V_{cc} is maximum when $V_{CE} = 0$ this gives

$$I_C = \frac{V_{CC}}{R_C}$$

Saturation

The condition for saturation is determined from the relationship

$$I_B \geq \frac{I_C}{h_{FE}}$$

During saturation V_{CE} is not exactly 0 but almost equal to 0.2 V. V_{BE} hardly changes.

Typical npn silicon Transistor Parameters

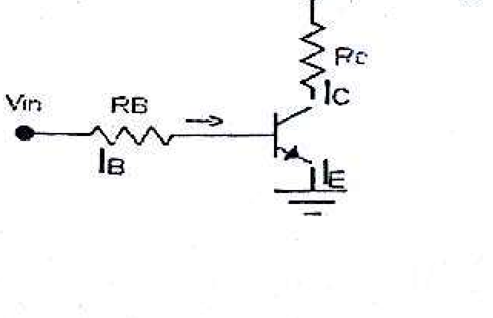
Region	V_{BE} (Volts)	V_{CE} (volts)	Current Relationship
Cut-off	<0.6	Open circuit	$I_B = I_C = 0$
Active	0.6-0.7	>0.8	$I_C = h_{FE} I_B$ → β
Saturation short cct	0.7-0.8	0.2	$I_B \geq I_{Cs}/h_{FE}$

off

on

Vb>0.7

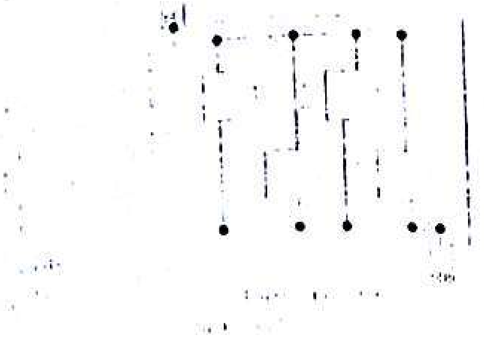
Example



Transistor-Transistor logic (TTL)

The usefulness of a DTL gate is limited by its speed of operation.

DC supply: The nominal value of the dc supply voltage for TTL (transistor – transistor logic) and CMOS (complementary metal oxide semiconductor) devices is +5V connected to V_{CC} or V_{DD} pins.



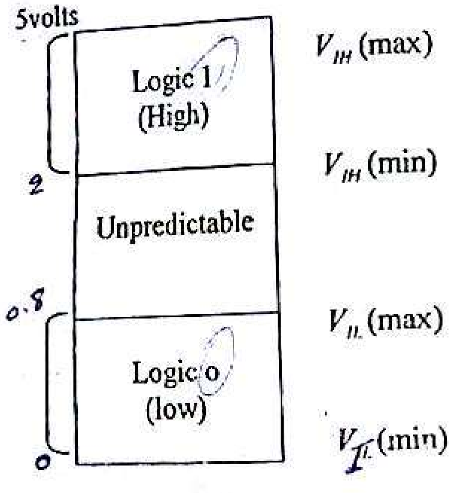
TTL logic levels

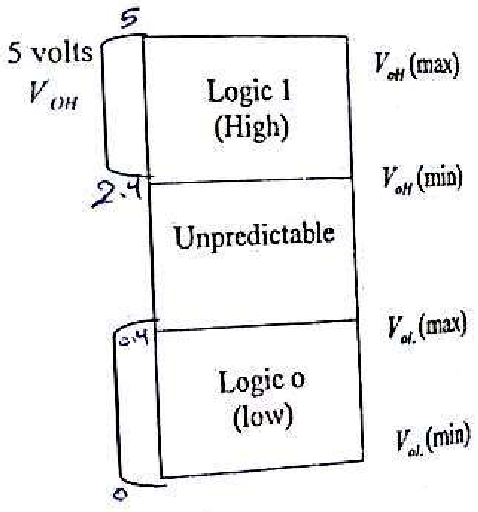
Input low = 0V to 0.8 V
High = 2 V to V_{CC} (5V)

When an input voltage is in this range (0.8 – 2 V) it can be interpreted as either high or low by the logic circuit thus given unpredictable performance. Therefore TTL gates cannot be operated reliably when input voltages are in this range.

The output voltages of TTL

Logic low = 0 – 0.4 volts, Logic high = 2.4 – 5 volts , Unpredictable = 0.4 – 2.4 volts





$$I_{OH} = 400\mu A$$
$$I_{IH} = 40\mu A$$
$$I_{OL} = 16mA$$
$$I_{IL} = \overset{1.6}{\text{[illegible]}}mA$$

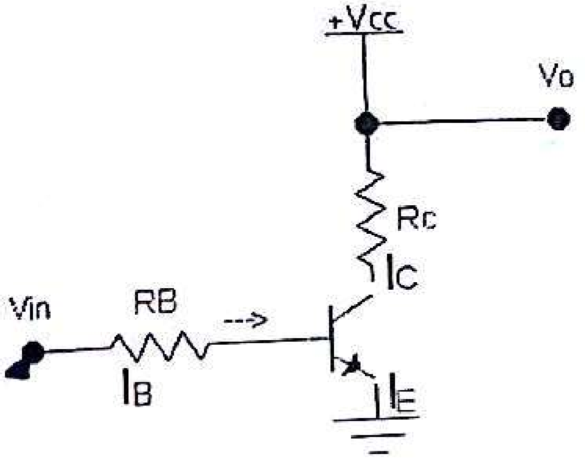
The two ratios give the same number in this case

$$\frac{400\mu A}{40\mu A} = \frac{16mA}{1.6mA} = 10$$

Therefore the fan – out of standard TTL is 10. This means that the output of a TTL gate can be connected to no more than ten inputs of other gates in the same logic family.

CMOS اكثر استخداما

Bipolar-Transistor Characteristics



Common-Emitter npn silicon Transistor connected between Vcc and ground, Vi is input voltage

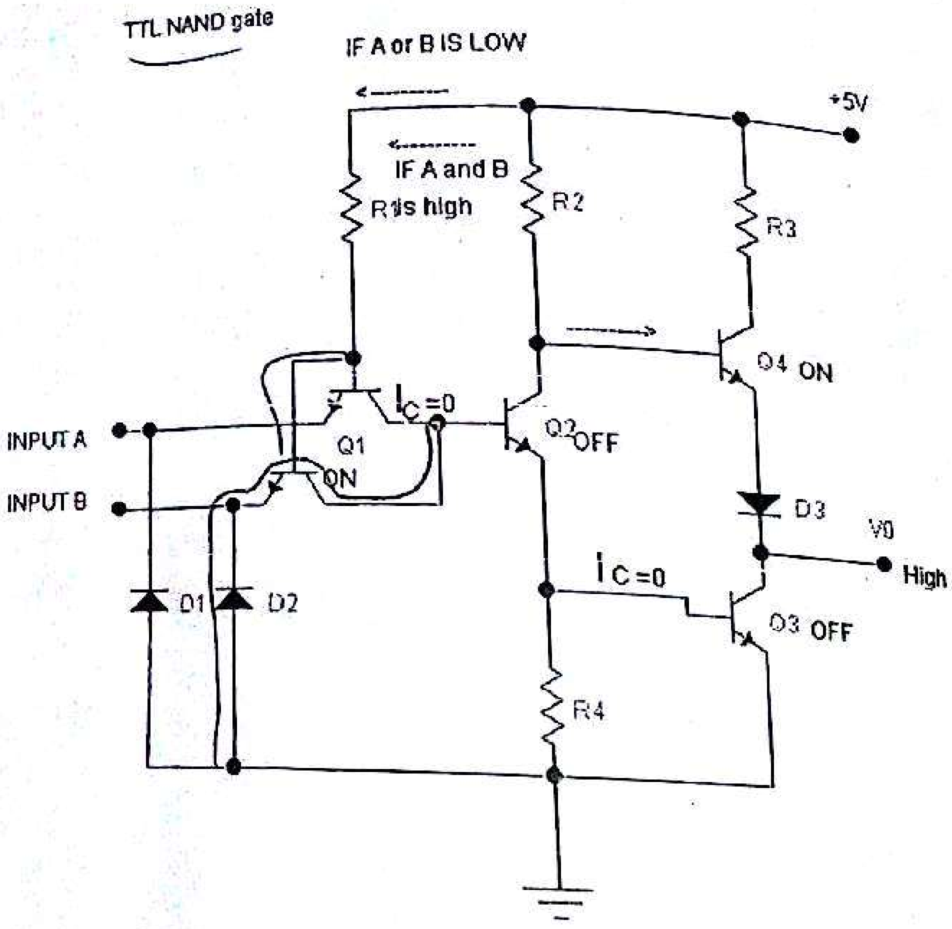
Ic=Collector current, it flows through RC and the collector of the transistor
I_B= Base Current, Flows through R_B and base of the transistor
$I_E = I_C + I_B$ Emitter connected to ground , Vcc is supply voltage

thus turning Q4 on. A saturated Q4 provides a low resistance path from Vcc to the output. We therefore have a HIGH on the output for a low on the input. At the same time the emitter of Q2 is (ground potential keeping Q3 off.

Diode DI is called the input clamp diode. D1 in the TTL circuit prevents negative spikes of voltage on the input from damaging Q1, Diode D2 ensures that Q4 will turn off when Q2 is on (HIGH input).

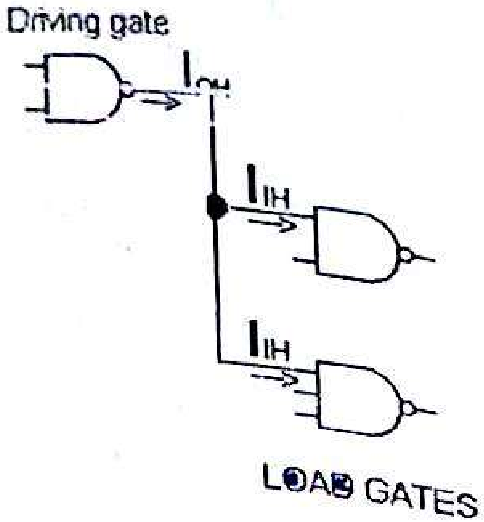
TTL NAND gate

[illegible]
Inverter.



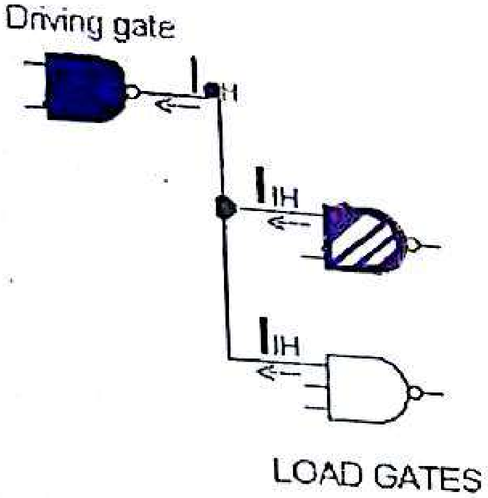
Basically TTL NAND is the same as the inverter circuit except for he additional input emitter of Q1. In TTL technology multiple – emitter transistors are used for the input devices. These multiple emitter transistors can be compared to the diode arrangement shown below.

above which it ceases to operate properly and is said to be overloaded.



I_{OH} current output high

The fan – out is calculated from the amount of current available in the output of a gate and the amount of current needed in each input of a gate.

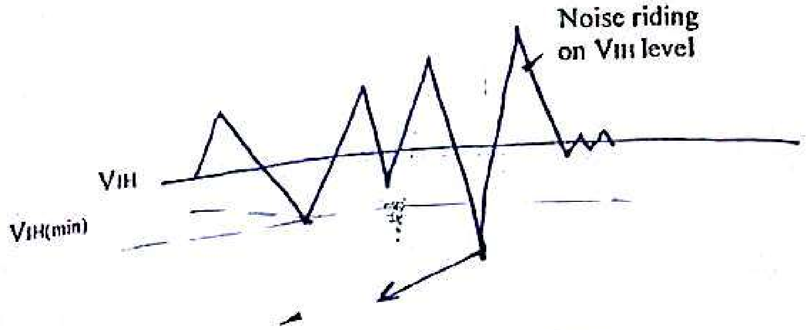


The Fan – but of the gate is calculated from the ratio I_{OH}/I_{IH} or I_{OL}/I_{IL} which ever is smaller. For example the standard TTL gates have the following valves.

Noise Immunity

Noise is unwanted voltage that is induced in electrical circuits and can present a threat to the proper operation of the circuit. Wires and other conductors within a system can pickup stray high – frequency electromagnetic radiation from adjacent conductors.

In order not to be adversely affected by noise, a logic circuit must have a certain amount of noise immunity. This is the ability to tolerate a certain amount of unwanted voltage fluctuation on its inputs without changing its output state.



If excessive noise causes input to go below 2v ,the gate may "think" that there is A low on its input and respond accordingly .

If excessive noise causes input to go above 0.8v ,the gate may "think" that there is A HIGH on its input and respond accordingly .

VIL (max)

VIL

Noise
riding
on VIL
LEVEL