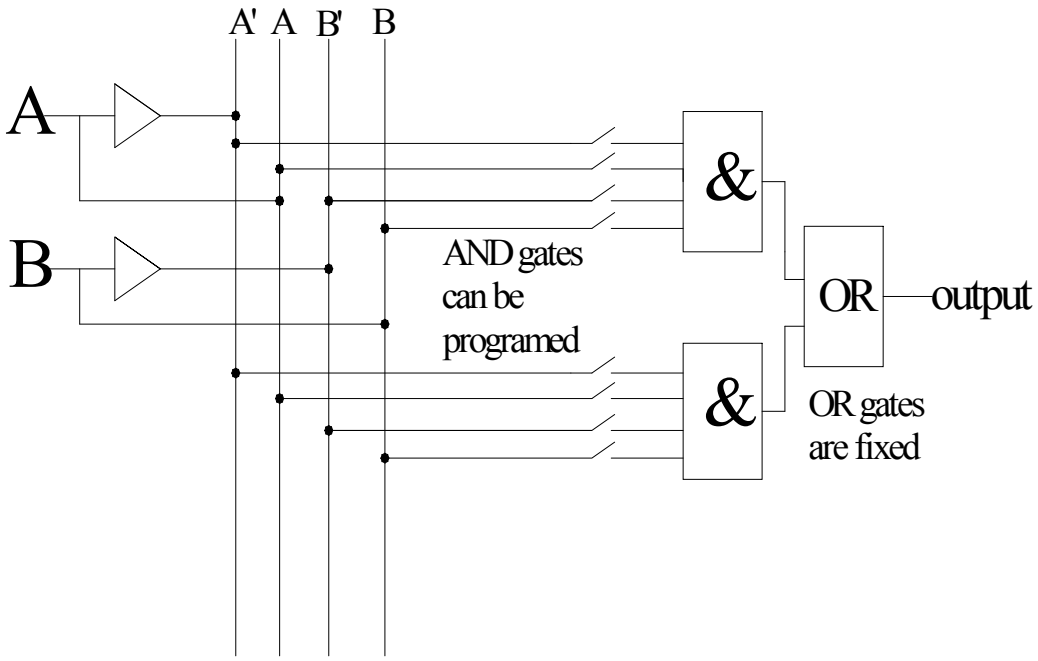
Programmable Logic Devices

A PLD is an IC that can be programmed to perform a wide variety of specific combination and or sequential logic functions.

PLD consists of two arrays of gates firstly AND gates and secondly OR gates (Flip Flop, Registers).

Programmable Array Logic

(PAL) consists of an array of AND gates whose inputs can be programmed and whose outputs are connected to a fixed array of gates.



Figure

The user is able to program the AND array to perform a wanted sum of product logic function by Blowing certain fuses in the array.

Every input and its complement can be connected to or disconnected from every and gate.

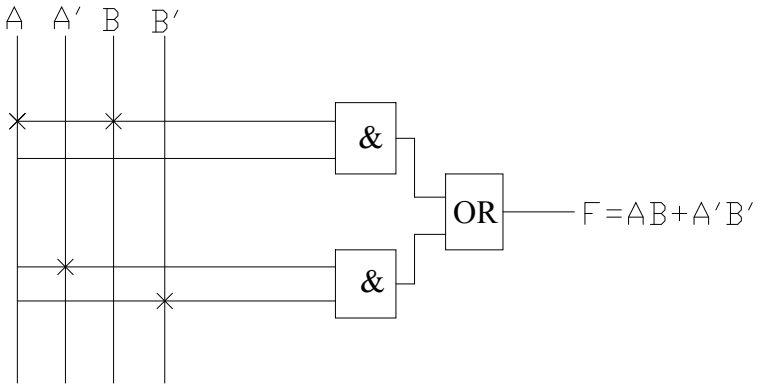
Usually the symbol X indicates a connection.

OR gates can not be programmed,

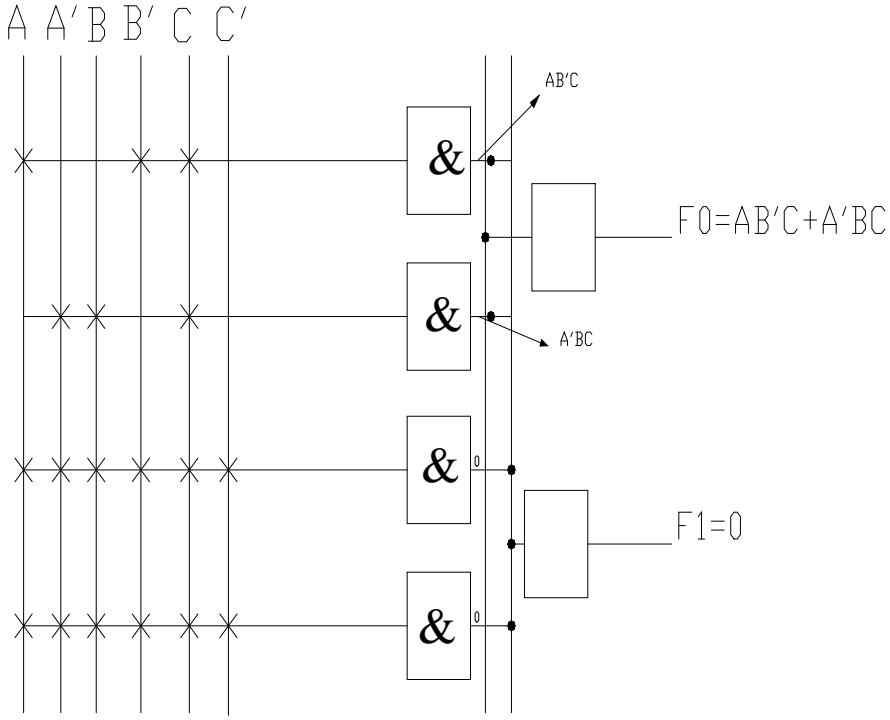
Example

Implement the logical function

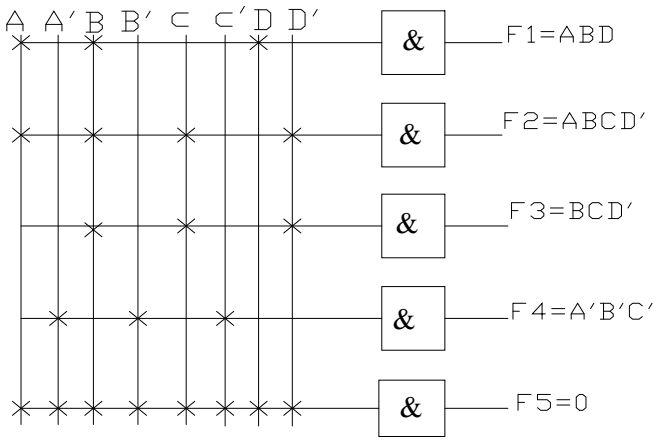
F = AB + A`B`



Example 2: Implement F = AB`C + A`BC on 3-4 PAL (where 3 indicates the number of inputs ABC and 4 represent the number of AND gates)



In summary.



Figure

Programmable Logic Array

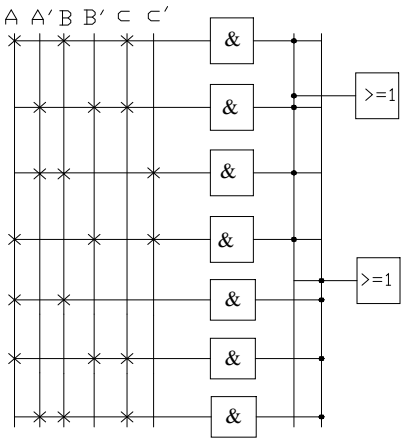
PLA also contains both AND gate array and OR gate array but now both are fully programmable.

Example

Implement a full adder using a PLA

S = ABC + A`B`C + AB`C` + A`BC` (this requires 4 AND gates 1 OR gate)

C = AB + AB`C + A`BC (this requires 3 AND gates 1 OR gate)



Figure

Memory

Read Only Memory

A read-only memory (ROM) is a memory device intended to store information which is fixed. That is there is an initial operation during which information is written into the memory and thereafter the memory is read only. Generally these come ready from manufacture.

There are however, memories which allow the user to establish the store of information in the memory. Such memories are referred to as programmable memories (PROM).

There are also ROMs in which the stored information can be changed. However in such cases the writing operation is accomplished in a time which is many orders of magnitude larger than the time required to read. Such memory devices (described as erasable) are read only memories in the sense that to change the stored information it is necessary to interrupt the digital processing in which the memory is involved.

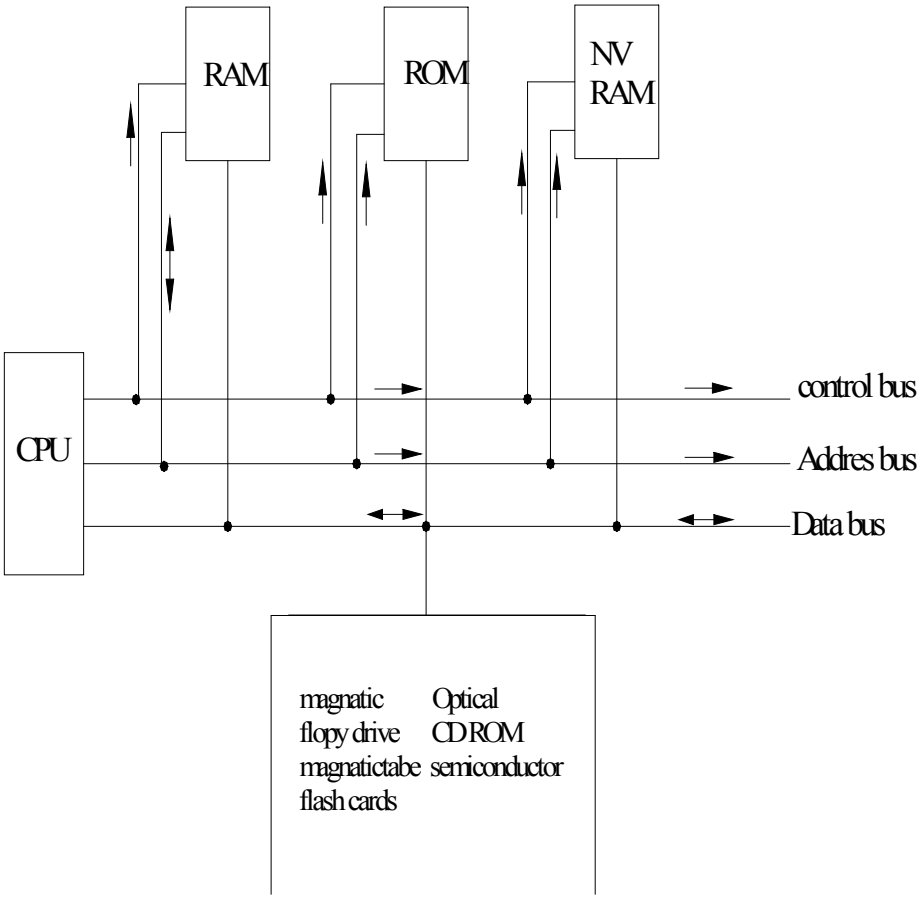
A most important attribute of the ROM is that the information it stores will not be lost if the electric power that it uses to operate should be interrupted. Such memories are referred to as nonvolatile.

The ROM has many applications in digital systems. It can be used to provide the realization of an arbitrary truth table. It can be used to store any information. Truth tables, arithmetic operation (sin x or ln x) all these are easier to store than to physically build the circuits that carry these operations.

The most important characteristic that a digital system has over an analog system is its ability t store data for short or long periods. The entire Internet system is dependent on the transfer of data form one storage/memory device to another.

The compact disk read-only memory (CD-ROM) is a modern example of an optical storage device that features very high storage device capacity at low cost.

Memory Device in Computers:



Address Bus, control Bus, Bus is a group of parallel conductor whose Job is to transfer information to other parts of the computer or microprocessor.

- Address Bus, Control Bus:
  One way communication lines that tell memory, storage and other peripheral devices who does what and when

- Data Bus:
  Two way communication channel for sending information to and receiving information from memory, storage and other peripheral devices.

- From diagram Notice:

data from data bus can flow into (to write in memory) or out of (to read from memory) both RAM & (NVRAM). ROM is different because it is permanently programmed and data can flow out of this semiconductor device.

Semiconductor storage cells

- **SRAM** (static random-access memory)
  high access speed, read or write requires continuous power (volatile memory), low density, high cost.

- **DRAM** (Dynamic random-access memory)
  good access speed, read or write volatile memory plus a need for refresh circuitry, high density, lower cost. Used in most PCs.

- **ROM** (read only memory)
  high density non-volatile (cannot be altered) reliable, low cost specially at high volumes.

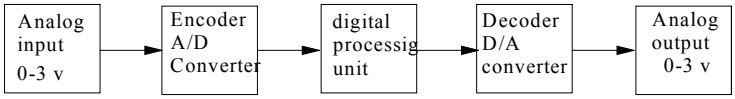
- **EPROM** (electrically programmable read only memory)
  high density, non-volatile (can be updated although not easily) ultraviolet light erasable before reprogramming.

- **EEPROM** (electrically erasable programmable read only memory)
  non-volatile but electrically erasable by bytes for reprogramming lower density high cost.

- **Flash memory**
  very high density, low power non-volatile but rewritable (bit – by – bit) with in the digital system, fairly new and developing technology extremely promising.

Connecting with analog devices D/A

Most real-world information is analog, Time, Speed, Weight, Pressure, Light intensity and Position measurement are all analog in nature.



HYBRID SYSTEM

The encoder is a special device that converts the analog signal to a digital information. The encoder is called an Analog – to – digital converter (A/D).

The decoder is a special type; it converts the digital information from the digital processing unit to an analog output. The analog output may be a continuous voltage change from 0 to 3V. We call this decoder D/A, Digital to analog.

Any system that contain both digital & analog devices is called a hybrid system.

The encoders and decoders that convert from analog to digital and digital to analog are called interface devices by engineers. The word “interface” is generally used when referring to a device or circuit that converts from one mode of operation to another.

Note that the input block of the block diagram refers to an analog voltage ranging from 0 to 3V. This voltage could be produced by a transducer. A transducer is defined as a device that converts one form of energy to another. For instance a photocell could be used as the input transducer to give voltage proportional to light intensity. Other transducers, microphones, speakers, strain gauges, temperature sensors, potentiometers.

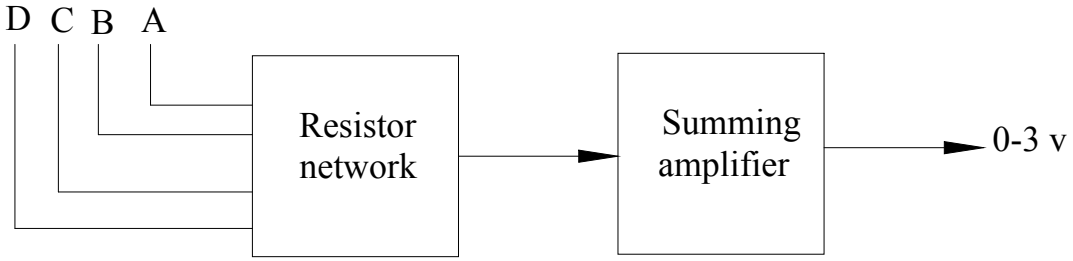
D/A conversion

Let us suppose we want t convert the binary from the processing unit to a 0 to 3V output. As with any decoder, we must set up a truth table of all the possible situations. The table overleaf shows four inputs (D, C, B, A) into the D/A converter. The inputs are in binary form so the exact value of he inputs is not important each one is about 3V to 5V and each 0 is about 0V.

	Digital Inputs				Analog output Volts
	D	C	B	A	
Row1	0	0	0	0	0
Row2	0	0	0	1	0.2
Row3	0	0	1	0	0.4
Row4	0	0	1	1	0.6
Row5	0	1	0	0	0.8
Row6	0	1	0	1	1.0
Row7	0	1	1	0	1.2
Row8	0	1	1	1	1.4
Row9	1	0	0	0	1.6
Row10	1	0	0	1	1.8
Row11	1	0	1	0	2.0
Row12	1	0	1	1	2.2
Row13	1	1	0	0	2.4
Row14	1	1	0	1	2.6
Row15	1	1	1	0	2.8
Row16	1	1	1	1	3.0

Truth table for D/A converter

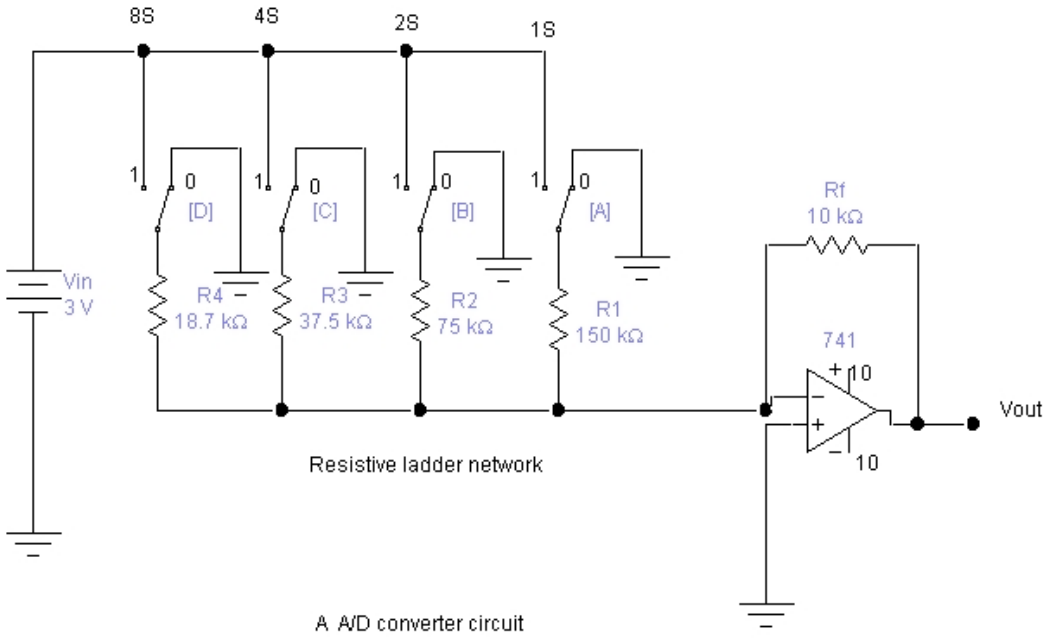
When the binary number 0000 appears at the input of the D/A the output becomes 0 volts if input 0001 output o.2 volts and so on



Block diagram of D/A converter

The decoder consists of two sections, the resistor network and the summing amplifier. The resistor network must take into account that a 1 at input B is worth twice as much as a 1 at input A, Also a 1 at input C is worth four times as much as 1 at input A. These circuits are called resistive ladder network.

The summing amplifier takes the output voltage from the resistor network and amplifies it to the proper amount shown on the right of the truth table.



The resistor network on the left is made up of resistors R1, R2, R3 and R4. the summing amplifier on the right consists of an op amp and a feedback resistor. The input V_{in} is 3V applied to switches.

With all switches at GND (0V) the input voltage is 0V and the output voltage is 0V. This corresponds to (row 1).

Switch A is moved to Logic 1 (on)

The input voltage is applied to the op amp through R1. Therefore the Op amp gain is calculated as follows

$$A_v = \frac{R_f}{R_{in}} = \frac{R_f}{R_1} = \frac{10{,}000}{150{,}000} = 0.066$$

To calculate the output voltage.

$$V_{out} = A_v * V_{in} = 0.066 * 3 = 0.2V$$

This corresponds to binary input 0001 (Row 2 in table)

Only switch B is moved to logic 1

$$A_v = \frac{R_f}{R_{in}} = \frac{10{,}000}{75{,}000} = 0.133$$

$$V_{out} = 3 * 0.133 = 0.4V$$

The procedure is the same when only one switch is on at the time. However say if switch A & B are on (Row 4).

Now, resistor R_1 & R_2 are in parallel

$$R_T = \frac{R_1 R_2}{R_1 + R_2} = \frac{150{,}000 * 75{,}000}{150{,}000 + 75{,}000} = 50{,}000$$

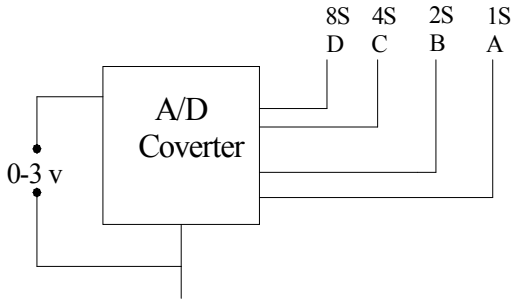
$$A_V = \frac{10{,}000}{50{,}000} = 0.2$$

$V_{out} = 3 * 0.2 = 0.6 volts$ which is the same as Row 4 & so on.

When all switches are on, then the op amp gain is 1 & $V_{in} = V_{out} = 3V$

A/D converter

An analog – to – digital converter is a special type of encoder. A basic block diagram of an A/D converter is shown below.

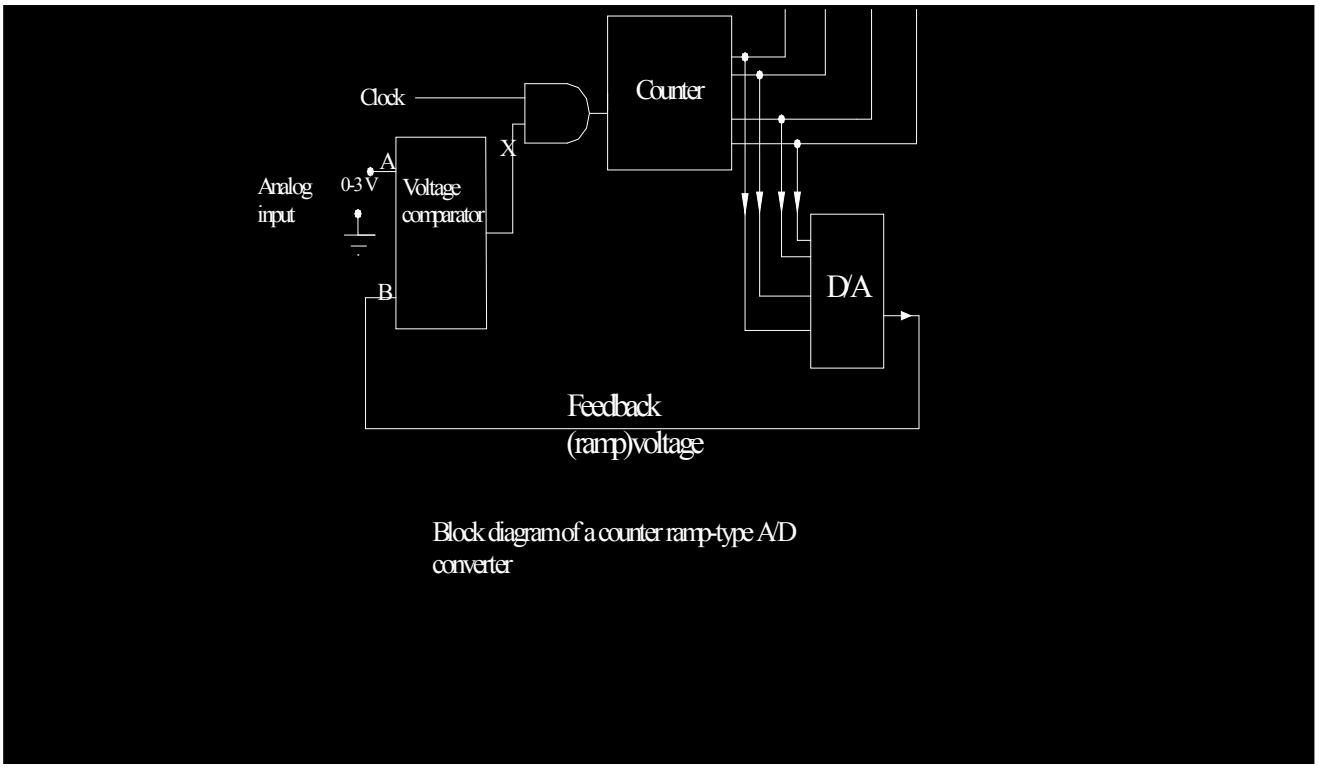


Block diagram of an A/D Converter

The input is a single variable voltage (0 - 3 V). The A/D converter translates the analog voltage at the input into a 4 – bit binary word. The following Truth table shows the inputs and outputs of the A/D.

	Analog Input Volts	Digital Output (Binary)			
		D	C	B	A
Row1	0	0	0	0	0
Row2	0.2	0	0	0	1
Row3	0.4	0	0	1	0
Row4	0.6	0	0	1	1
Row5	0.8	0	1	0	0
Row6	1.0	0	1	0	1
Row7	1.2	0	1	1	0
Row8	1.4	0	1	1	1
Row9	1.6	1	0	0	0
Row10	1.8	1	0	0	1
Row11	2.0	1	0	1	0
Row12	2.2	1	0	1	1
Row13	2.4	1	1	0	0
Row14	2.6	1	1	0	1
Row15	2.8	1	1	1	0
Row16	3.0	1	1	1	1

Notice the Truth table is the exact reverse of the D/A Truth table. The Truth table for the A/D converter looks quite simple. The electronic circuits that perform the task detailed in the Truth table are somewhat complicated. Look at the following Figure.



Block diagram of a counter ramp-type A/D converter

The A/D converter contains a voltage comparator, an AND gate, a binary counter and a D/A converter.

The analog voltage is applied at the left. The comparator checks the voltage coming from the D/A converter. If the analog input voltage at A is greater than the voltage at input B of the comparator, the clock is allowed to increase the count. The count increases until the feedback voltage from the D/A converter becomes greater than the analog input voltage. At this point the comparator stops the counter from advancing to a higher count.

Example:

Assume logic 1 at point x (comparator output).
Counter 0000.
Analog voltage input = 0.55V

The logic 1 at point x enables the AND gate and the first pulse of the clock is sent to CLK of the counter.

Counter advances to 0001, this number is fed to the D/A converter.

The D/A converter converts 0001 to analog number and according to the Truth table, 0001 produces 0.2V.

0.2 V is sent to point B input of comparator.

Comparator checks and compares point A & B point A = 0.55V, B = 0.2V. If point A which is the analog number is higher then the comparator puts out logic 1.

The AND gate is enabled and another clock pulse is sent to the counter.

The counter advances its count by 1, count now is 0010, (0.4 volts), this converted by D/A sent Back to B.

Comparator compares again till B is equal or grater than A, comparator puts logic 0 to the output and counter is stopped.

Digital Integrated Circuits

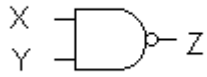
The IC digital logic families to be considered here are:

- RTL Resistor Transistor Logic
- DTL Diode Transistor Logic
- TTL Transistor – Transistor Logic
- ECL Emitter – Coupled Logic
- *MOS* *Metal – Oxide semiconductors*
- *CMOS* *Complementary Metal Oxide Semiconductor*

RTL & DTL have only historical significance since they are no longer used in digital systems RTL was the first commercial family to be used extensively.

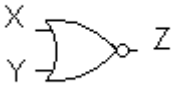
DTL have been replace by TTL, In fact TTL is a modification of DTL gate.

The basic circuit in each IC digital logic family is either a NAND or NOR gate this basic circuit is the primary building Block from which all other more complex digital components are obtained.



X	Y	Z
L	L	H
L	H	H
H	L	H
H	H	L

Positive Logic Nand Gate



X	Y	Z
L	L	H
L	H	L
H	L	L
H	H	L

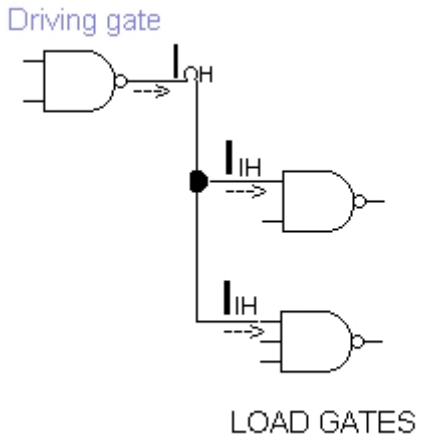
Positive Logic Nor Gate

A Bipolar junction transistor (BJT) can be either an npn or pnp junction transistor. Field – effect transistors are said to be Unipolar. The operation of a bipolar transistor depends on the flow of two types of carriers electronics and holes a unipolar Transistor depends on the flow of only one type of majority carrier which may be electronics (n – channel) or holes (p – channel) RTL, DTL, TTL, ECL are Bipolar Transistors.

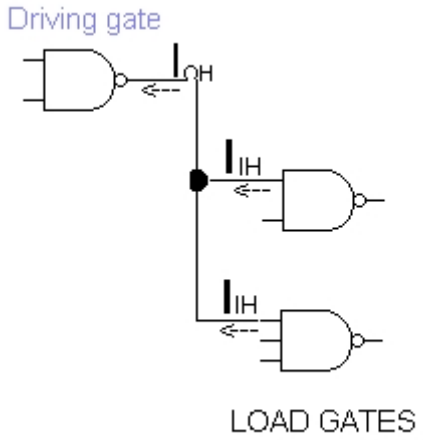
MOS and CMOS employ a type of unipolar transistor called metal – oxide – semiconductor field effect Transistor MOSFET.

Fan – out

The output of all gates can supply a limited amount of current above which it ceases to operate properly and is said to be overloader.



The fan – out is calculated from the amount of current available in the output of a gate and the amount of current needed in each input of a gate.



The Fan – out of the gate is calculated from the ratio I_{OH}/I_{IH} or I_{OL}/I_{IL} which ever is smaller. For example the standard TTL gates have the following valves.

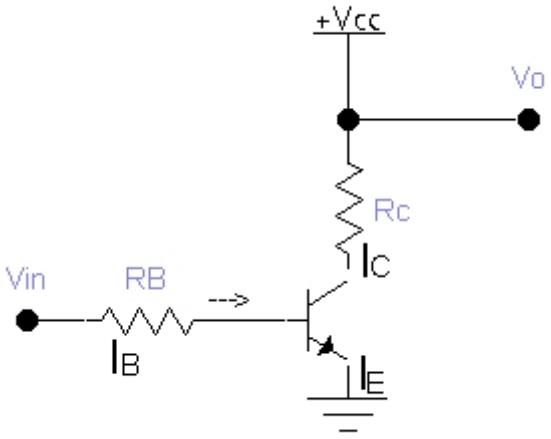
$$I_{OH} = 400\mu A$$
$$I_{IH} = 40\mu A$$
$$I_{OL} = 16mA$$
$$I_{IL} = 10mA$$

The two ratios give the same number in this case

$$\frac{400\mu A}{40\mu A} = \frac{16mA}{1.6mA} = 10$$

Therefore the fan – out of standard TTL is 10. This means that the output of a TTL gate can be connected to no more than ten inputs of other gates in the same logic family.

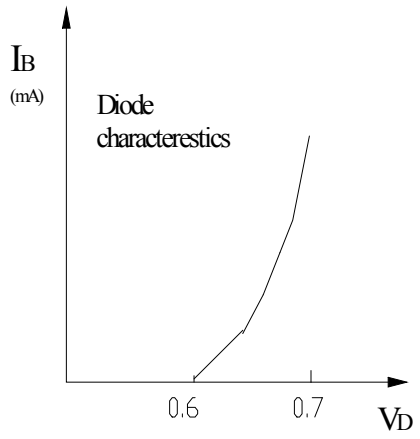
Bipolar-Transistor Characteristics



Common-Emitter npn silicon Transistor connected between Vcc and ground, Vi is input voltage

Ic=Collector current, it flows through RC and the collector of the transistor
I_B *= Base Current, Flows through* R_B *and base of the transistor*
$I_E = I_C + I_B$ *Emitter connected to ground ,Vcc is supply voltage*

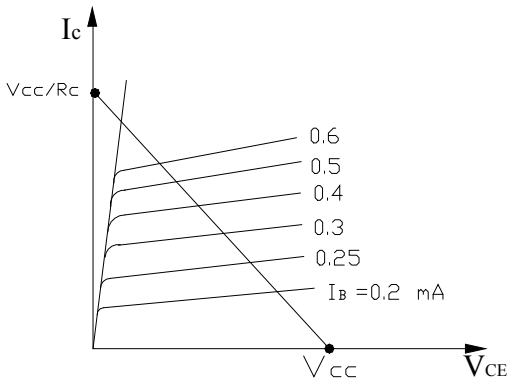
Transistor Base Characteristic:



V_{BE} = Voltage drop across the Base – emitter junction. This junction is forward biased when V_{BE} is positive, i.e. as indicated by the arrows. It is reversed Biased when V_{BE} is negative (opposite arrows).

Looking at the characteristics shows that if the base – emitter voltage is less than 0.6 Volts the Transistor is said to be **cut off** and no base current flows.

When the base – emitter junction is forward biased with a voltage greater than 0.6V the transistor conducts and I_B starts rising very fast where as V_{BE} changes very little. The voltage V_{BE} seldom exceed 0.8V.



Collector emmiter characteristic

V_{BE} is less than 0.6V, transistor cut – off $I_B = 0$, $I_C = 0$, the collected to emitter circuit behaves like an open circuit (i.e. switch off).

Active region

V_{CE} may be any where between 0.8V up to V_{CC}

$$I_C = I_B h_{FE}$$

h_{FE} = Transistor parameter called dc cutrrent gain

It is important to remember that I_C maximum does not depend on I_B. looking at diagram line V_{cc} is maximum when $V_{CE} = 0$ this gives

$$I_C = \frac{V_{CC}}{R_C}$$

Saturation

The condition for saturation is determined from the relationship

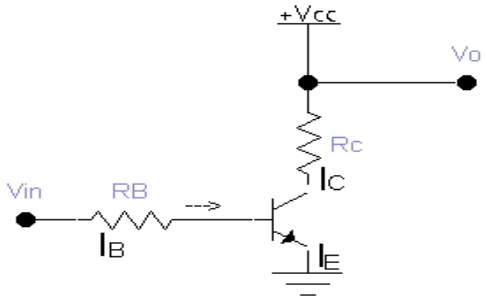
$$I_B \geq \frac{I_C}{h_{FE}}$$

During saturation V_{CE} is not exactly 0 but almost equal to 0.2 V. V_{BE} hardly changes.

Typical npn silicon Transistor Parameters

Region	$V_{BE}(Volts)$	$V_{CE}(volts)$	**Current Relationship**
Cut-off	**<0.6**	**Open circuit**	$I_B = I_C = 0$
Active	**0.6-0.7**	**>0.8**	$I_C = h_{FE} I_B$
Saturation	**0.7-0.8**	**0.2**	$I_B \geq I_{Cs} / h_{FE}$

Example



Given

$$R_c = 1k\Omega, \qquad R_B = 22k\Omega, \qquad h_{FE} = 50, \qquad V_{cc} = 5volts$$
$$H(high) = 5volts, \qquad L(low) = 0.2volts$$

If input voltage V_{in} = L = 0.2 V. This means that V_{BE} is less than 0.6 V and the Transistor is cut off. The collector – emitter circuit behaves like an open circuit where V_O = 5V = H

If input V_I = H = 5V then V_{BE} is greater than 0.6 V assume V_{BE} = 0.7 volts we calculate the base current.

$$I_B = \frac{V_i - V_{BE}}{R_B} = \frac{5 - 0.7}{22k\Omega} = 0.195mA$$

The maximum Ic occurs when V_{cc}=0.2volts

$$I_{cs} = \frac{V_{cc} - V_{CE}}{Rc} = \frac{5 - 0.2}{1k\Omega} = 4.8mA$$

Check for saturation

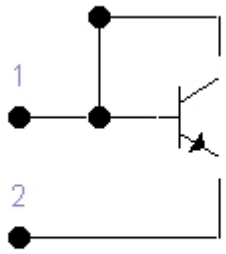
$$I_B \geq \frac{I_C}{h_{FE}}$$

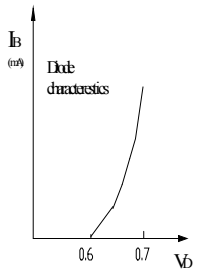
$$\frac{I_{CS}}{h_{FE}} = \frac{4.8}{50} = 0.096mA$$
$$0.195mA \geq 0.096mA$$

We find that the inequality is satisfied since 0.195mA is greater than 0.096mA. We conclude that the transistor is saturated and output voltage

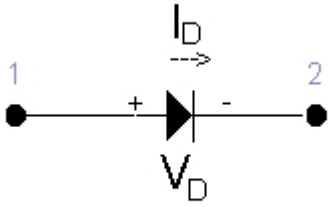
$V_O = V_{CE}$ = 0.2 V = L (INVERTER)

Transistor as a Diode





Transistor adapted for use as a diode

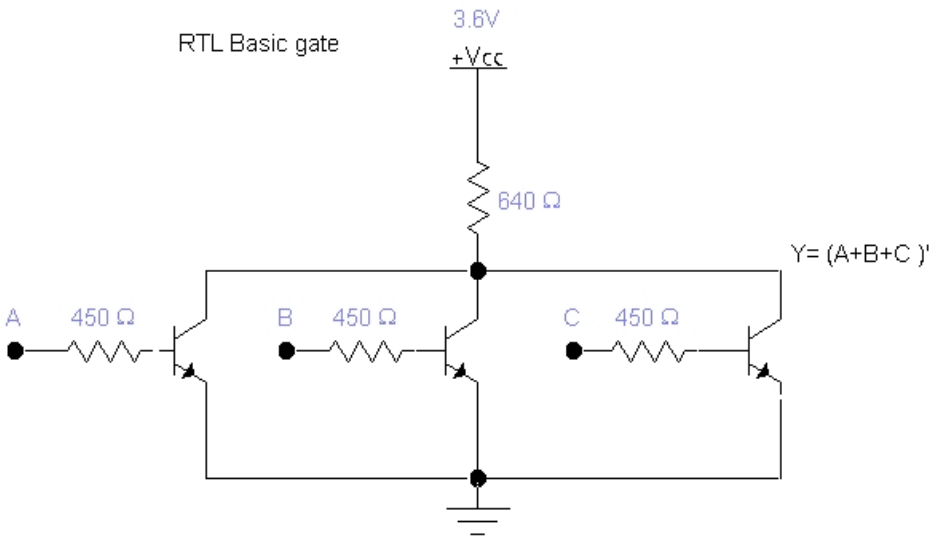


Diode graphical symbol

The diode is off and non – conducting when its forward voltage V_O is less than 0.6 V. When diode conducts $V_D = 0.7V$ and I_D flows in the direction of the arrow.

A diode or "Rectifier" is any device through which electricity can flow in one direction only.

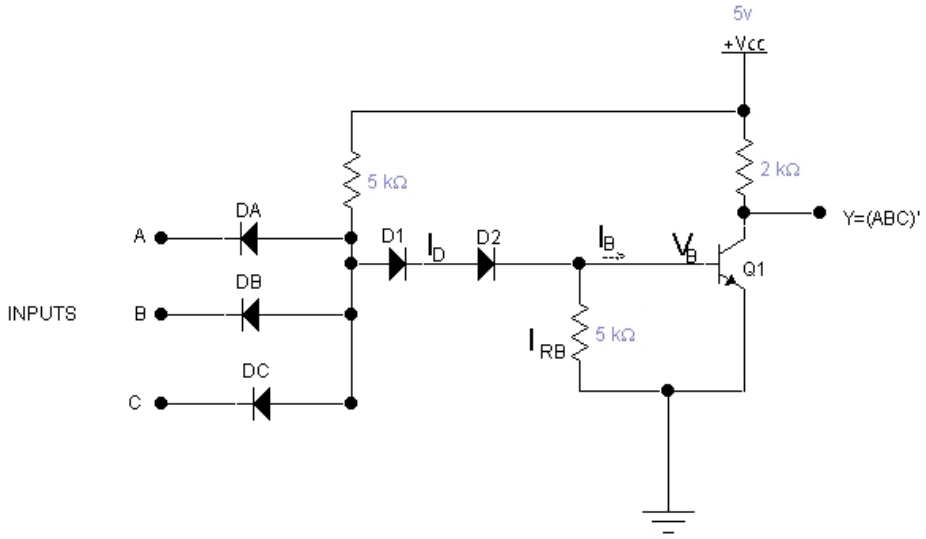
RTL Basic Gate



IF any input of the RTL gate is High (A, B, C) the corresponding transistor is driven into saturation. This causes the output to be low, regardless of the states of the other transistor. If all inputs are low (0.2 V) all transistors are cut off because $V_{BE} < 0.6V$. This causes the output to be high, approaching the value of supply voltage V_{CC} .

DTL Basic gates

The basic circuit in the DTL logic family is the NAND gate shown below.



The transistor serves as a current amplifier while inverting the digital signal. If any input is low (0.2 V) the corresponding input diode conducts current. This means that the diode is forward biased and here is a voltage drop of 0.75 Volts.
But at output there is 0.2V the means that point P is 0.75 + 0.2 = 0.95V.

0.95 volts is not enough to forward bias D1, D2.

Therefore Q1 is cut off and $Y=V_{CC}$ High.

$$V_B = V_P - V_{D1} - V_{D2} = 0.95 - 0.65 - 0.65 = -0.35v$$

$$\therefore$$

$$I_{RB} = \frac{V_{B2} - 0}{5*10^{-3}} = \frac{0.35}{5*10^{-3}} = 0.07mA$$

If all inputs are simultaneously at logic level 0 the current through resistor R will divide among the diodes D_A, D_B, D_C . Thus Vp decreases slightly and Q_1 is forced further into cutoff. Hence Vo remains at logic 1.

Saturation of Q_1

If all inputs are at logic 1 (5v) the current through (5kΩ resistor) will flow through D1 and D2 and into the base of Q_1, Q_1 will be driven into saturation and the output will drop to logic 0 as required for Nand gate operation.

$$I_{RB} = \frac{V_{B2} - 0}{5 \times 10^3} = \frac{0.75}{5 \times 10^3} = 0.15mA$$

$$I_D = \frac{V_{cc} - V_P}{R}$$

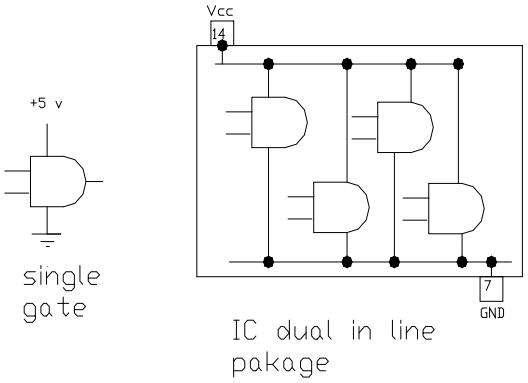
$$I_B = I_D - I_{RB}$$

Transistor-Transistor logic (TTL)

The usefulness of a DTL gate is limited by its speed of operation.

DC supply:

The nominal value of the dc supply voltage for TTL (transistor – transistor logic) and CMOS (complementary metal oxide semiconductor) devices is +5V connected to V_{CC} or V_{DD} pins.



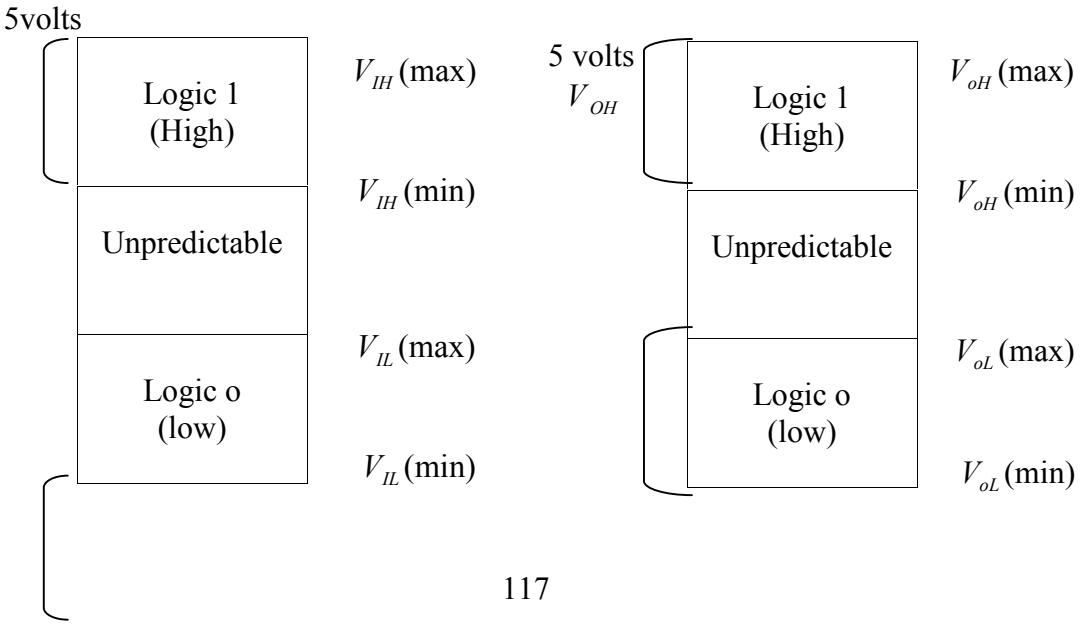
TTL logic levels

Input low = 0V to 0.8 V
High = 2 V to V_{CC} (5V)

When an input voltage is in this range (0.8 – 2 V) it can be interpreted as either high or low by the logic circuit thus given unpredictable performance. Therefore TTL gates cannot be operated reliably when input voltages are in this range.

The output voltages of TTL

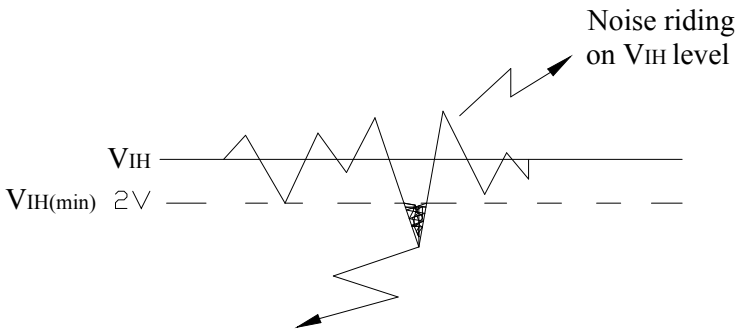
Logic low = 0 – 0.4 volts, Logic high = 2.4 – 5 volts , Unpredictable = 0.4 – 2.4 volts



Noise Immunity

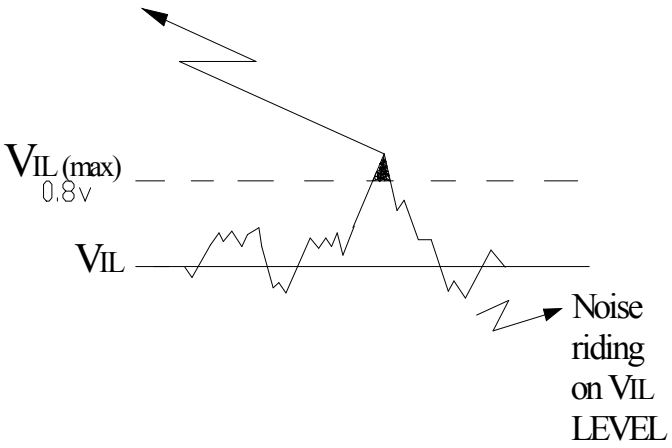
Noise is unwanted voltage that is induced in electrical circuits and can present a threat to the proper operation of the circuit. Wires and other conductors within a system can pickup stray high – frequency electromagnetic radiation from adjacent conductors.

In order not to be adversely affected by noise, a logic circuit must have a certain amount of noise immunity. This is the ability to tolerate a certain amount of unwanted voltage fluctuation on its inputs without changing its output state.



If excessive noise causes input to go below 2v ,the gate may "think" that there is A low on its input and respond accordingly .

If excessive noise causes input to go above 0.8v ,the gate may "think" that there is A HIGH on its input and respond accordingly .



Noise margin

A measure of circuits noise immunity is called the noise margin which is expressed in volts.

High level noise margin (V_{NH})

$$V_{NH} = V_{OH}(\min) - V_{IH}(\min)$$

Low level noise margin (V_{NL})

$$V_{NL} = V_{IL}(\max) - V_{OL}(\max)$$

Example:

Determine the high – level and low – level noise margins for TTL.
From information from logic low and logic high diagram we have

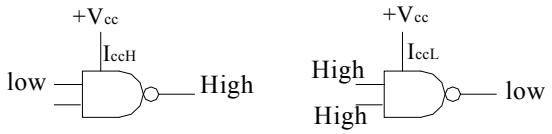
$V_{IH}(\min) = 2V$ $V_{IL}(\max) = 0.8\ V$
$V_{OH}(\min) = 2.4\ V$ $V_{OL}\ (\max) = 0.4\ V$

$V_{NH} = VOH(\min) - V_{IH}(\min) = 2.4 - 2 = 0.4V$
$V_{NL} = VIL(\max) - V_{OL}(\max) = 0.8 - 0.4 = 0.4V$

A TTL gate is immune to up to 0.4V of noise for both the high & low input states.

Power dissipation

A logic gate draws current from the dc supply, when the gate is in the high output state an amount of current designated by I_{CCH} is drawn an in the low output state, a different amount of current I_{CCL} is drawn.



Example: if I_{CCH} is specified as 1.5 mA when V_{CC} is 5V and gate is high

$$P_D = V_{CC}I_{CCH} = 5 * 1.5mA = 75\ mW$$

When the gate is pulsed its output switches back & forth between high and low and the amount of supply current varies between I_{CCH} and I_{CCL}.
The average power dissipation depends on the duty cycle and is usually specified for a duty cycle of 50% when the duty cycle is 50% the output is high half the time and low the other half. The average supply current is therefore

$$I_{CC} = \frac{I_{CCH} + I_{CCL}}{2}$$

The average power dissipation is

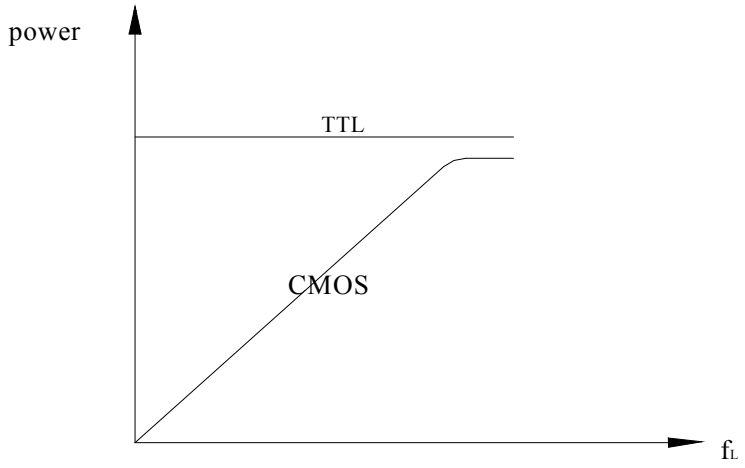
$$P_D = V_{CC} * I_{CC}$$

Example:
A certain gate draws 2mA when its output is high and 3.6mA when the output is low what is the average power dissipation if V_{CC} is 5V and the gate is operated on a 50% duty cycle.

Solution:
The average I_{CC} is

$$I_{CC} = \frac{I_{CCH} + I_{CCL}}{2} = \frac{2mA + 3.6mA}{2} = 2.8mA$$
$$P_o = V_{CC}I_{CC} = 5 * 2.8mA = 14mW$$

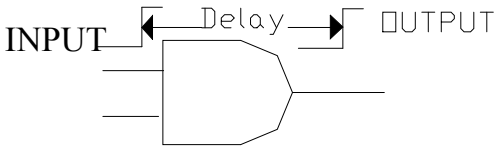
Power dissipation in a TTL circuit is essentially constant over a range of operating frequencies . Power dissipation in CMOS, however is frequency dependent.



Power-versus Frequency Curve for TTL and CEMOS

Propagation delay

When a signal passes (propagates) through a logic circuit it always experiences a time delay.

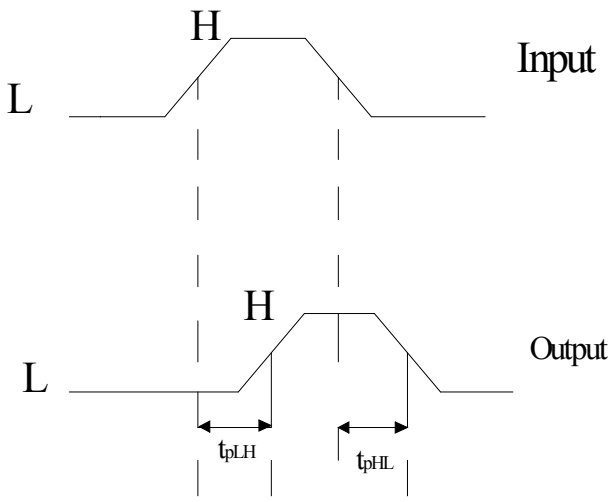


A change in the output level always occurs a short time called the propagation delay time later than the change in the input level that caused it.

There are two propagation delay times specified for logic gates

t_{PHL} : The time between a designated point on the input pulse and the corresponding point on the output pulse when the output is changing from HIGH to LOW.

t_{PLH} : the time between a designated point on the input pulse and the corresponding point on the output pulse when the output is changing from LOW to HIGH.



The propagation delay of a gate limits the frequency at which it can be operated. The greater the propagation delay, the lower the maximum frequency. Thus a higher – speed circuits one that has a smaller propagation delay. A gate with a delay of 3ns is faster than one with a 10ns delay.

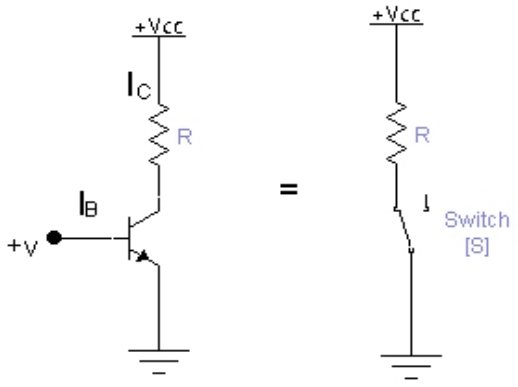
The Bipolar junction transistor

The bipolar junction transistor (BJT) is the active switching element used in all TTL circuits. npn (BJT) has three terminals base emitter and collector. A BJT has two junction base emitter junction and base collector junction.

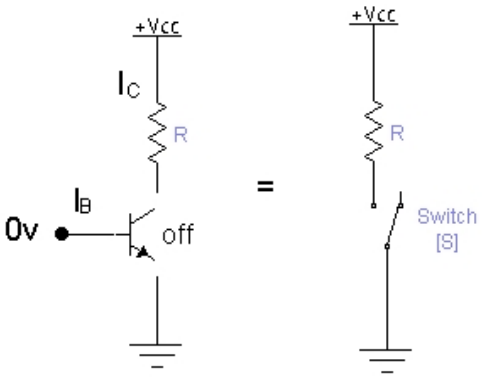
The basic switching operation is as follows when the base is approximately 0.7V more positive than the emitter and when sufficient current is provided into the base the transistor turns on and goes into saturation. In saturation the transistor ideally acts like a closed switch between the collector and the emitter.

When the base is less than 0.7V more positive than the emitter, the transistor turns off and becomes an open switch between the collector and the emitter.

To summarize in general terms, a HIGH on the base turns the transistor on and makes it a closed switch. A low on the base turns the transistor off and makes it an open switch. In TTL some BJTs have multiple emitters.

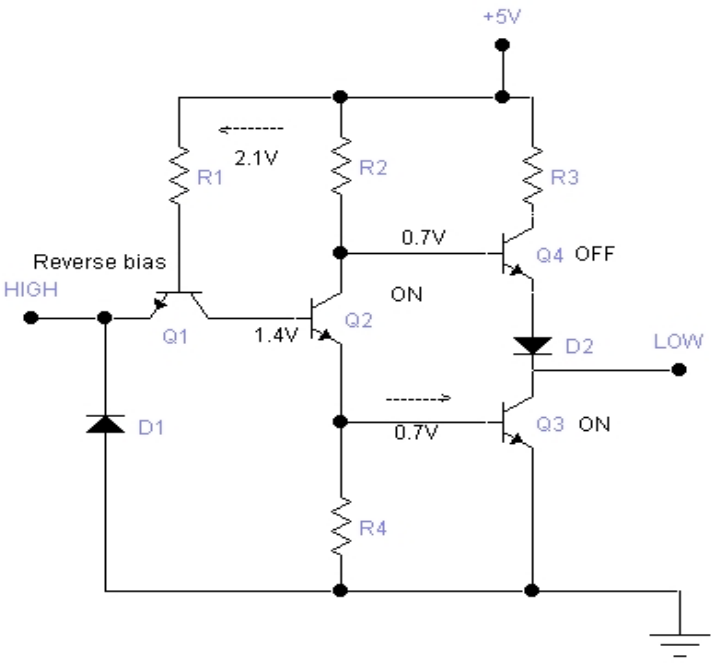


Saturated (ON) Transistor closed switch, ideal switch equivalent



Off Transistor , ideal switch equivalent

TTL inverter

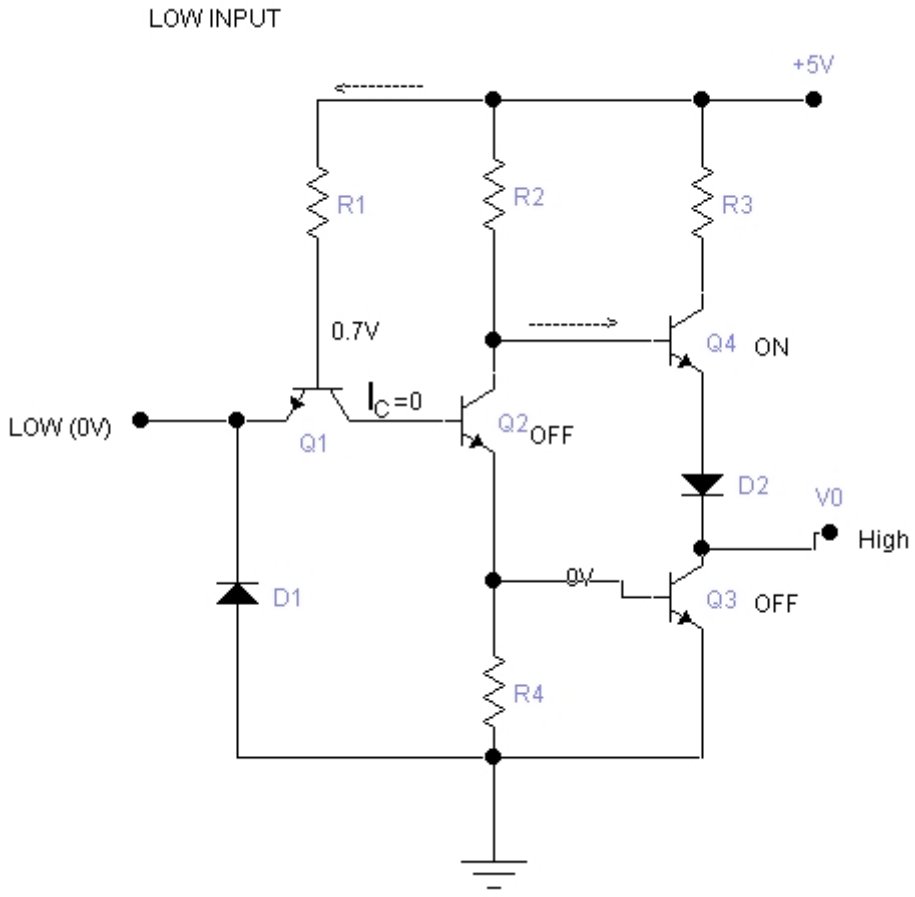


The above arrangement is called totem – pole arrangement.

When the input is high the **base emitter junction of Q1 is reverse biased** and the **base – collector junction is forward biased**. This condition permits current through R1 and the base – collector junction of Q1 into the base of Q2 thus driving Q2 into saturation as a result Q3 is turned on by Q2 and its collector voltage which is the output is near ground potential.

We therefore have a low output for a high input, at the same time, the collector of Q2 is at sufficiently low voltage level to keep Q4 off.

Low input

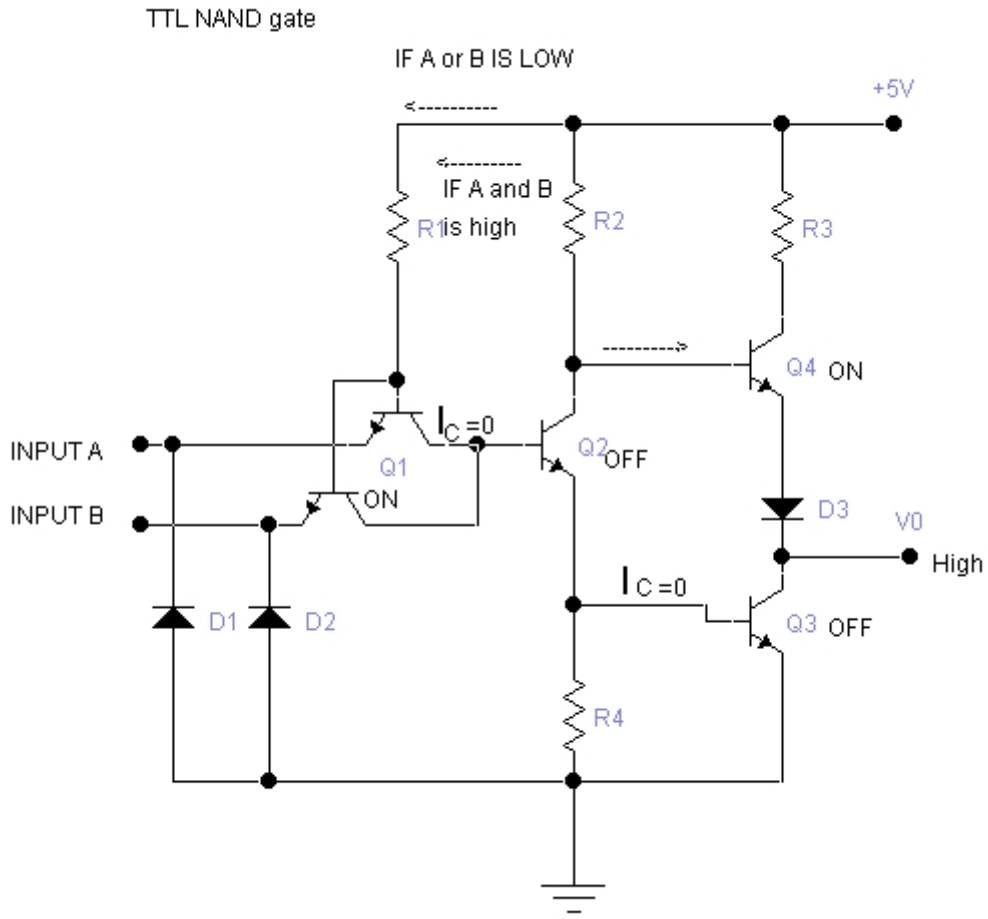


When the input is LOW, the base – emitter junction of Q1 is forward biased and the base – collector junction is reverse biased. There is current through R1 and the base – emitter junction of Q1 to the LOW input. A LOW provides a path to ground for the current. There is no current into the base of Q2, so it is off. The collector of Q2 is high

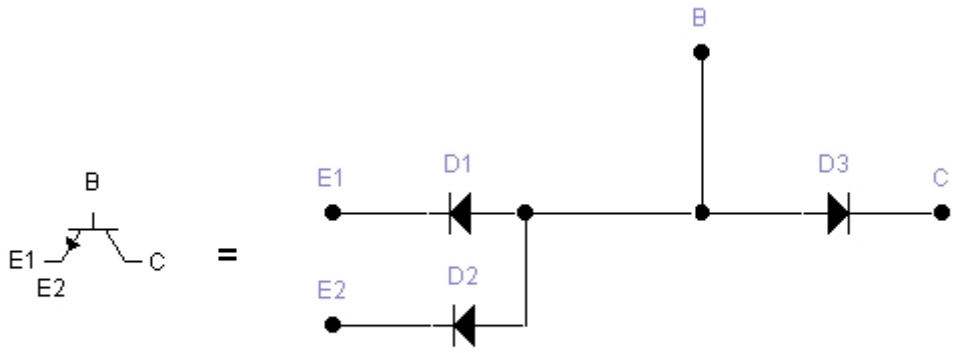
thus turning Q4 on. A saturated Q4 provides a low resistance path from Vcc to the output. We therefore have a HIGH on the output for a low on the input. At the same time the emitter of Q2 is t ground potential keeping Q3 off.

Diode D1 is called the input clamp diode. D1 in the TTL circuit prevents negative spikes of voltage on the input from damaging Q1, Diode D2 ensures that Q4 will turn off when Q2 is on (HIGH input).

TTL NAND gate



Basically TTL NAND is the same as the inverter circuit except for he additional input emitter of Q1. In TTL technology multiple – emitter transistors are used for the input devices. These multiple emitter transistors can be compared to the diode arrangement shown below.



Diode equivalent of a TTL multiple emitter

TTL NAND operation

A LOW on either input A or B forward Biases the Transistor (diodes in equivalent circuit), Q1 is on ,Q2 is OFF, Q3 is OFF, Q4 is on (same as inverter) output is high.

High on Both inputs A & B, reverse Biases the Transistor and Forward Biases D3 in equivalent circuit Q1 base – collector junction, Q2 is turned on resulting in LOW output same as inverter.