Chapter 9

Memory Devices, Circuits, and Subsystem Design

Introduction

9.1 Program and Data Storage Memory—·
9.2 Read-Only Memory—·
9.3 Random Access Read/Write Memories—·
9.4 Parity, Parity Bit, and Parity-Checker/Generator Circuit
9.5 FLASH Memory
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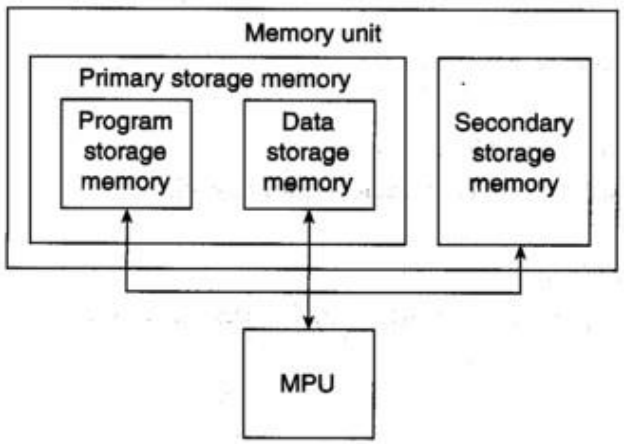
9.1 Program and Data Storage Memory- The Memory Unit



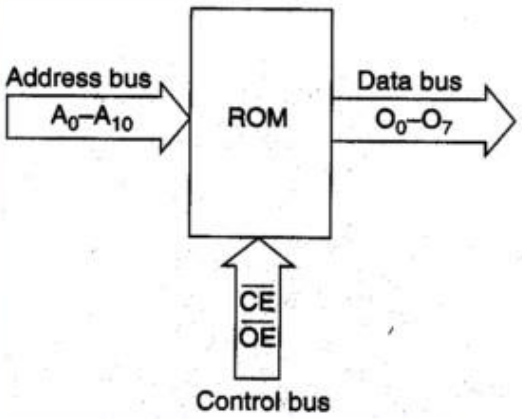
- Memory—provides the ability to store and retrieve digital information
  - Instructions of a program
  - Data to be processed
  - Results produced by processing
- Organization of the Microcomputer memory unit
  - Secondary storage—stores information that is not currently in use
    - Slow-speed
    - Very large storage capacity
    - Implemented with magnetic/optical storage devices—in PC
      - Hard disk drive
      - Floppy disk drive
      - Zip drive
  - Primary storage—stores programs and data that are currently active
    - High-speed
    - Smaller storage capacity
    - Implemented with semiconductor memory
  - Partitioning of Primary Storage
    - Program storage memory—holds instructions of the program and constant information such as look-up tables
      - EPROM (BIOS in PC)
      - FLASH memory
      - DRAM (volatile code storage in a PC)
    - Data storage memory—holds data that frequently changes such as the information to be processed by a program
      - SRAM
      - DRAM (PC)

9.2 Read-Only Memory- Types

Read-only memory (ROM)

- Used for storage of machine code of program
- Stored information can only be read by the MPU
- Information is nonvolatile—not lost when power turned off
- Types:
  - ROM—mask-programmable read only memory
    - Programmed as part of manufacturing process
    - Lowest cost
    - High volume applications
  - PROM—one-time programmable read-only memory
    - Permanently programmed with a programming instrument
  - EPROM—erasable programmable read-only memory
    - Programmed like a PROM
    - Erasable by Ultraviolet light
- Electrically alterable ROM-like devices
  - FLASH memory
  - EEROM (E^2ROM)

9.2 Read-Only Memory- Block Diagram



- Block diagram of the ROM, PROM, and EPROM are essentially the same
- Signal interfaces
  - Address bus (A10-A0)—MPU inputs address information that selects the storage location to be accessed
  - Data Bus (D7-D0)—information from the accessed storage location output to be read by MPU
  - Control bus—enables device and/or enables output from device
    - CE* = chip enable—active 0; 1 low-power stand by mode
    - OE* = output enable—active 0; 1 high-Z state
- Byte capacity- number of bytes a device can store
  - Calculated from number of address bits

    EX: Address = 11-bit address

    Storage capacity = 2_{11} = 2048 bytes
- Organization—how the size of a ROM is described
  - Formed from capacity and data bus width

    EX: 2048 X 8 or just 2K X 8
- Storage density—number of bits of storage in a ROM
  - Calculated from byte capacity and data width

    EX: Storage density = 2048 X 8 = 16384 bits (16K bits)

9.2 Read-Only Memory- Organization and Capacity

- Example:

A ROM device has 15 address lines and 8 data lines. What are the address range, byte capacity, organization, and storage density?

- Solution:
  - Address range

    $A14\text{-}A0 = 000\ 0000\ 0000\ 0000_2$ · $111\ 1111\ 1111\ 1111_2$

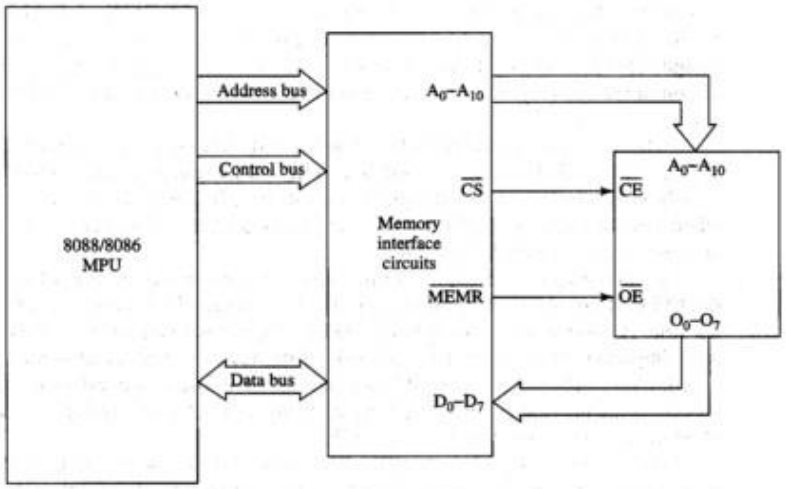
    = 0000H · 7FFFH
  - Byte capacity

    2_{15} = 32,768 bytes = 32K bytes
  - Organization

    32,768 X 8 bit
  - Storage density

    32,768 x 8 = 262144 bits = 256K bits

9.2 Read-Only Memory- Operation



Read operation

- MPU outputs address and control information on its bus.
- Interface circuit applies Address A10-A0 to the address inputs of the ROM to select a specific byte wide storage location
- Interface circuits decode additional address bits to produce a chip select output
- Logic 0 at CS* applied to the CE* input of the ROM to enable it for operation
- Memory interface circuitry produces appropriately timed MEMR* output
- MEMR* applied to OE* input of the ROM to enable the information at the addressed storage location onto the output bus D7-D0
- Memory interface supplies the byte of data from the ROM to the MPUs data bus
- MPU reads the byte of data from the ROM from its data bus

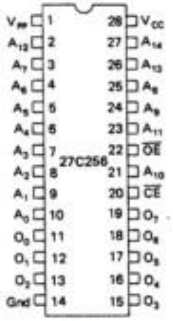
9.2 Read-Only Memory- Standard EPROM ICs

EPROM	Density (bits)	Capacity (bytes)
2716	16K	2K × 8
2732	32K	4K × 8
27C64	64K	8K × 8
27C128	128K	16K × 8
27C256	256K	32K × 8
27C512	512K	64K × 8
27C010	1M	128K × 8
27C020	2M	256K × 8
27C040	4M	512K × 8

- EPROM part numbers formed by adding the prefix "27" to the device total Kbits of storage capacity
  - Examples:
    - 16K bit EPROM · 2716
    - 32K bit EPROM · 2732
    - 1M bit EPROM · 27C010
- Most EPROM available in byte wide organization
  - Examples:
    - 2764 · 8K X 8
    - 27C020 · 256K X8
- NMOS versus CMOS process
  - Manufacturing processes used to make EPROMs
    - NMOS=N-channel metal-oxide semiconductor
    - CMOS= complementary symmetry metal-oxide semiconductor
    - "CMOS" designated by "C" in part number
  - NMOS—older devices such as 2716 and 2732
  - CMOS—all newer devices 27C64 and up

9.2 Read-Only Memory- Pin Layouts

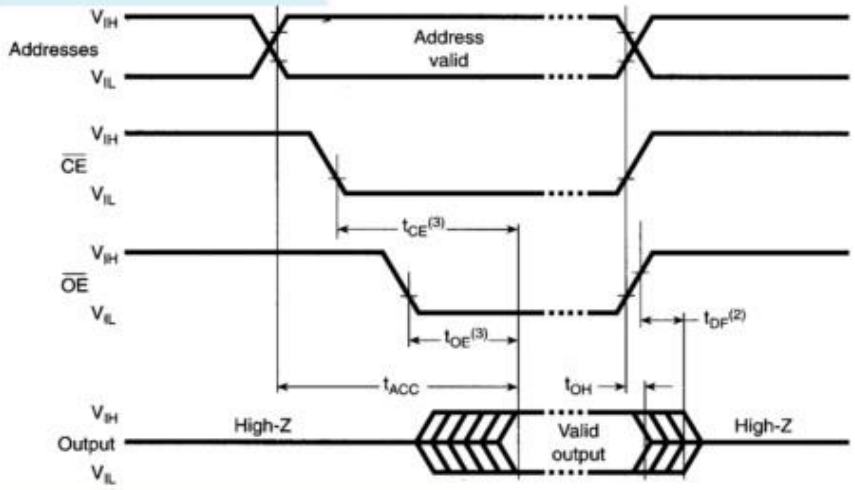
27C512	27C128	27C64	2732A	2716	Pin
A_{15}	V_{PP}	V_{PP}			1
A_{12}	A_{12}	A_{12}			2
A_7	A_7	A_7	A_7	A_7	3
A_6	A_6	A_6	A_6	A_6	4
A_5	A_5	A_5	A_5	A_5	5
A_4	A_4	A_4	A_4	A_4	6
A_3	A_3	A_3	A_3	A_3	7
A_2	A_2	A_2	A_2	A_2	8
A_1	A_1	A_1	A_1	A_1	9
A_0	A_0	A_0	A_0	A_0	10
O_0	O_0	O_0	O_0	O_0	11
O_1	O_1	O_1	O_1	O_1	12
O_2	O_2	O_2	O_2	O_2	13
Gnd	Gnd	Gnd	Gnd	Gnd	14



Pin	2716	2732A	27C64	27C128	27C512
28			V_{CC}	V_{CC}	V_{CC}
27			$\overline{PGM}$	$\overline{PGM}$	A_{14}
26	V_{CC}	V_{CC}	N.C.	A_{13}	A_{13}
25	A_8	A_8	A_8	A_8	A_8
24	A_9	A_9	A_9	A_9	A_9
23	V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}
22	$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
21	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
20	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
19	O_7	O_7	O_7	O_7	O_7
18	O_6	O_6	O_6	O_6	O_6
17	O_5	O_5	O_5	O_5	O_5
16	O_4	O_4	O_4	O_4	O_4
15	O_3	O_3	O_3	O_3	O_3

- EPROM pin layouts are designed for compatibility
  - Permit easy upgrade from lower to higher density
  - Publish pin layouts of future densities
  - Allows design of circuit boards to support drop in upgrade to higher densities
- Most pins are independent and serve a common function for all densities
  - Examples:
    - pin 10- A0
    - pin 11--O0
    - pin 14- Gnd
- Some have one multi-function pin
  - OE*/Vpp
    - Vpp mode during programming only

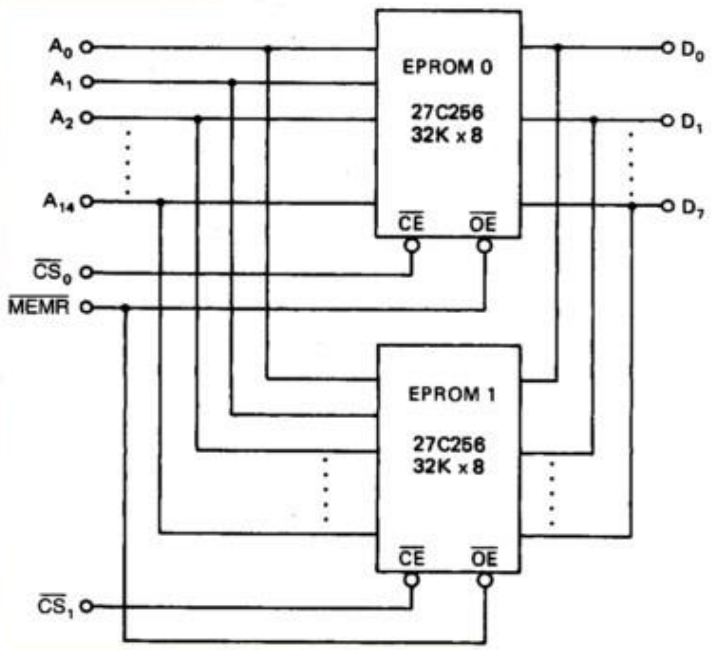
9.2 Read-Only Memory- EPROM Switching Waveforms



Timing of the read operation

- Output data is not immediately available at the outputs
  - Delays exist between the application of the address,CE* and OE* signals and the occurrence of a valid output
  - tacc= access time—address to valid output delay time
  - tCE= chip-enable time—chip enable to valid output delay
  - tOE=output-enable time—output enable to valid data delay
- To assure that the MPU reads valid data, these inputs must be applied at the appropriate times
  - Responsibility of the memory interface circuitry
- Another delay occurs at the removal of OE* before the outputs lines are returned to the high-Z state
  - tDF= chip-deselect time—time for the outputs to recover

9.2 Read-Only Memory- Expanding Byte Capacity



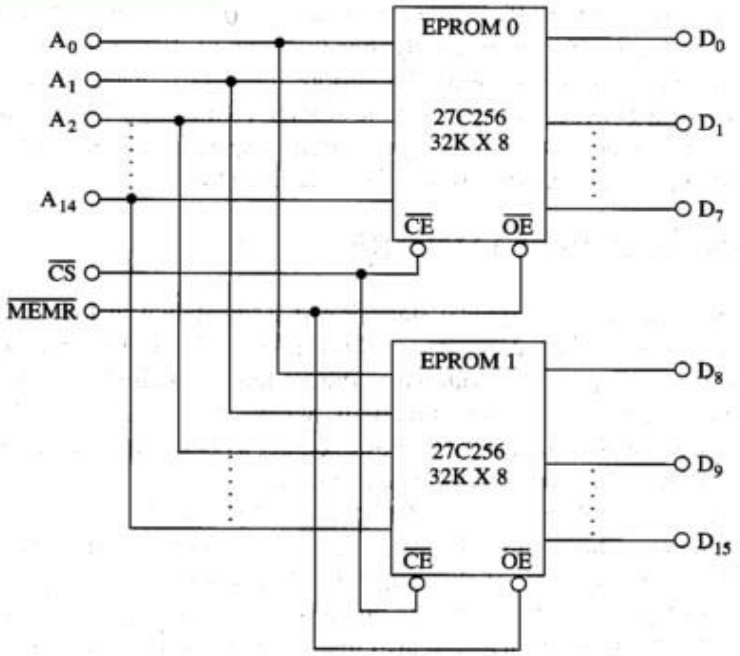
- Many applications require more ROM capacity than is available in a single device
  - Need more bytes of storage
  - Connects to a wider data bus
- Expanding byte capacity with 2 EPROMS
  - Connect address bus lines in parallel
  - Connect output lines in parallel
  - Connect OE* in parallel
  - Enable chips with separate chip selects
    - Address bit A15 decoded to produce CS0* and CS1*
      - A15=0 · CS0*
      - A15=1 · CS1*
      - Implemented with inverting buffer
  - Byte capacity

    2_{16} = 64K bytes
  - Organization

    64K X 8 bit
  - Storage density

    2 X 32K x 8 = 512K bits

9.2 Read-Only Memory- Expanding Word Length



Expanding word length with 2 EPROM

- Connecting to 8086 16-bit data bus
  - Connect address bus lines in parallel
  - Connect CE* in parallel
  - Connect OE* in parallel
  - 8 data outputs of EPROM 0 used to supply the lower data bus lines D0-D7
  - 8 data outputs of EPROM 1 used to supply the upper 8 data bus lines D8-D15
- Byte capacity

  $2 \times 2_{15}$ = 64K byte
- Organization

  32K X 16 bit
- Storage density

  32K x 16 = 512K bits

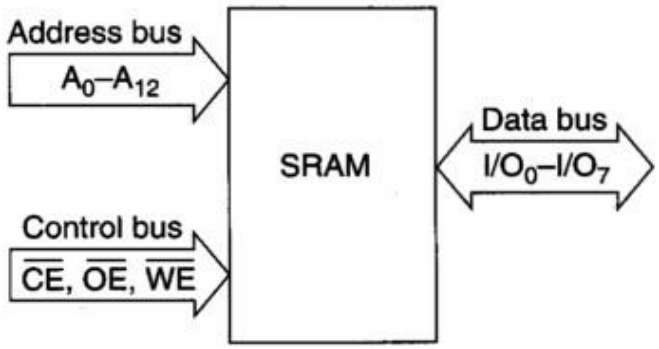
9.3 Random Access Read/Write Memories-

Types of RAMs

Random Access Read/Write Memory (RAM)

- Used for **temporary** storage of data and program information
- Stored information can be **altered** by MPU—read or written
  - Information read from RAM
  - Modified by processing
  - Written back to RAM for reuse at a later time
- Information normally more frequently **randomly accessed** than ROM
- Information is **volatile**— lost when power turns off
- Types:
  - Static RAM (**SRAM**)— data once entered remains valid as long as power supply is not turned off
    - Lower densities
    - Higher cost
    - Higher speeds
  - Dynamic RAM (**DRAM**)—data once entered requires both the power to be maintained and a periodic refresh
    - Higher densities
    - Lower cost
    - Lower speeds
    - Refresh requires additional circuitry

9.3 Random Access Read/Write Memories-
SRAM Block Diagram



Signal interfaces

- **Address bus (A12-A0)—MPU inputs address information that selects the storage location to be accessed**
- **Data Bus (I/O7-I/O0)—input/output of information for the accessed storage location from/to MPU**
- **Control bus—enables device, enables output from device, and selects read/write operation**
  - **CE* = chip enable—active 0**
  - **OE* = output enable—active 0**
  - **WE* = write enable**
    - **0 = write to RAM**
    - **1 = read from RAM**

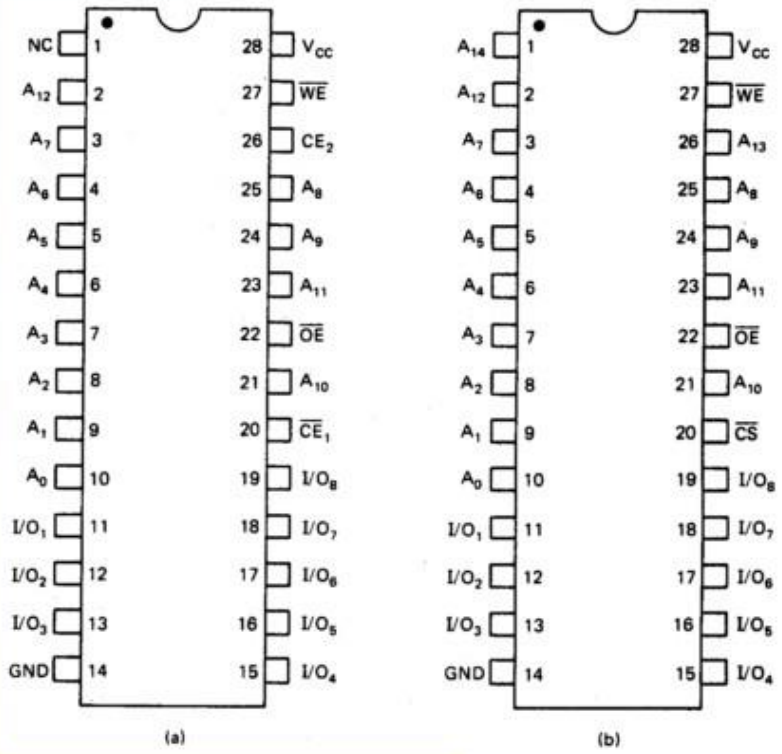
9.3 Random Access Read/Write Memories-
Standard SRAM ICs

SRAM	Density (bits)	Organization
4361	64K	64K × 1
4363	64K	16K × 4
4364	64K	8K × 8
43254	256K	64K × 4
43256A	256K	32K × 8
431000A	1M	128K × 8

- Part numbers vary widely by manufacturer—Hitachi/NEC use “43xxx
- SRAMs are available in a variety of densities and organization
  - Typical SRAM densities
    - 64K bit
    - 256K bit
    - 1M bit
  - Typical organizations of the 64K bit

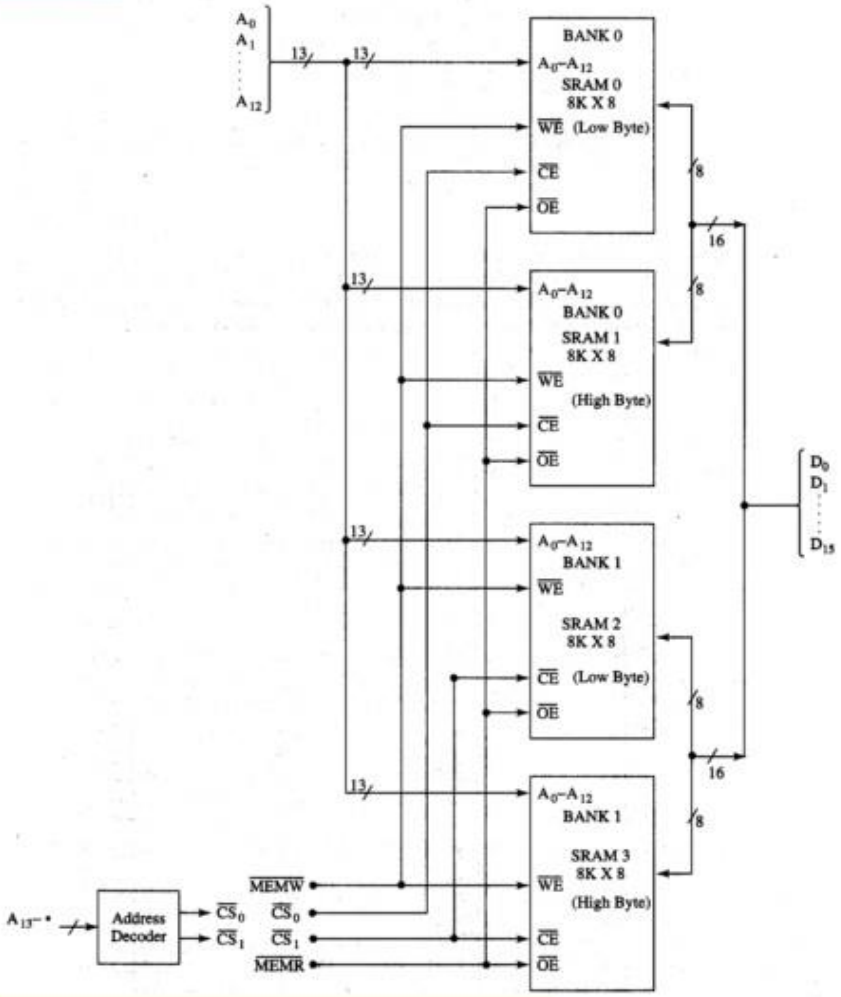
SRAM
- 64K X 1 bit
- 16K X 4 bit
- 8K X 8 bit

9.3 Random Access Read/Write Memories- Pin Layout of SRAMs



- 4364 and 43256A pin layouts are designed for compatibility
- 4364 pin configuration (Fig a)
  - A12-A0 · 13-bit address
    2_{13} = 8K bytes
  - I/O7-I/O0 · byte wide
  - Pin 1 NC = no connect
  - Pin 27 WE*
  - Pin 20 CE1* · active 0
  - Pin 26 CE2 · active 1
  - Pin 22 · OE*
  - Pin 28 Vcc
  - Pin 14 GND
- 43256A differences (Fig b)
  - Pin 1 · A14
  - Pin 26 · A13
  - Pin 20 called CS* (function unchanged)

9.3 Random Access Read/Write Memories-
Expanding Word-Width and Capacity



Most SRAM subsystems

- Require both word-width and bit capacity expansion
- Require the ability to write on byte-wide or word wide basis- design only supports words

- Expansions performed in a similar way as for EPROMs
- 16K X 16-bit SRAM circuit
  - A0-A12 in parallel
  - A13 decoded to form CS0* and CS1*
    - CS0* · enable Bank 0
    - CS1* · enable Bank 1
  - SRAMs 0 & 2—input/outputs connected in parallel and supply low byte of data bus
  - SRAMs 1 & 3—input/ outputs connected in parallel and supply high byte of data bus
  - MEMW* and MEMR* produces independent write and read enables

MEMW*	MEMR*	Data Transfer
0	0	Invalid
0	1	Word write
1	0	Word read
1	1	Inactive

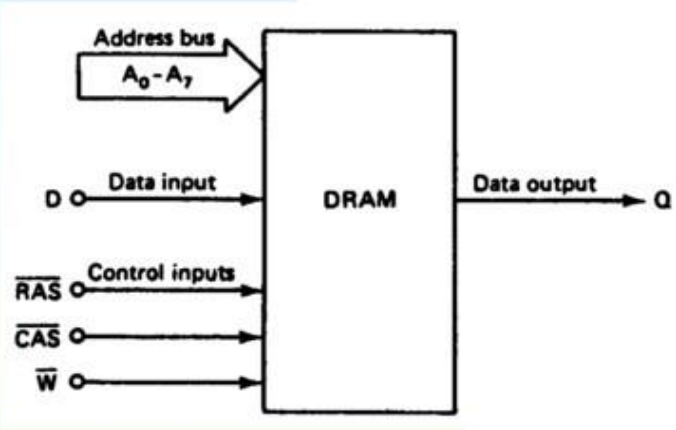
- How can the circuit be modified to support byte wide write?

9.3 Random Access Read/Write Memories- Standard Read/Write Cycle Times

Part number	Read/write cycle time
4364-10	100 ns
4364-12	120 ns
4364-15	150 ns
4364-20	200 ns

- Speed of a SRAM identified as read/write cycle time
  - Variety of speeds available—4364 available in speeds ranging from 100ns to 200ns
  - Shorter the cycle time the better.
- Designated by a dash speed indicator following the part number
  - -10 = 100ns
  - -12 = 120ns

9.3 Random Access Read/Write Memories-
DRAM Block Diagram



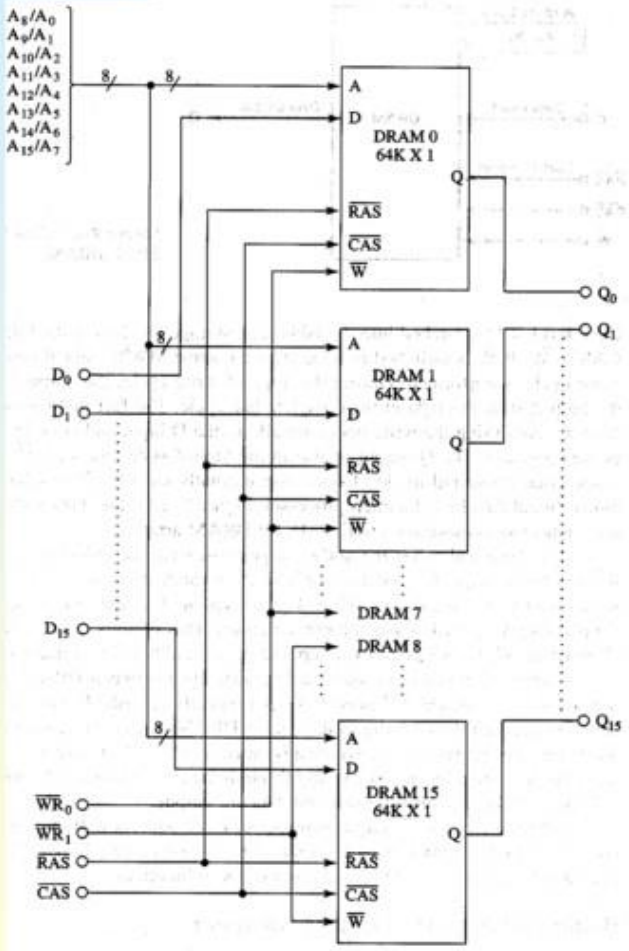
- DRAM signal interfaces
  - Address multiplexed in external circuitry into a separate row and column address
    - Row address = A_7-A_0
    - Column address = A_{15}-A_8
  - Special RAS* and CAS* inputs used to strobe address into DRAM
  - Row and column addresses applied at different times to address inputs A_0 through A_7
    - Row address first
    - Column address second
    - Known as “RAS before CAS”
    - Address reassembled into 16-bit address inside DRAM
  - Frequently data organizations are X1, X2, and X4
    - Separate data inputs and outputs
    - Data input labeled D
    - Data output labeled Q
  - Read/write (W) input signals read or write operation

9.3 Random Access Read/Write Memories- Standard DRAM ICs

DRAM	Density (bits)	Organization
2164B	64K	64K × 1
21256	256K	256K × 1
21464	256K	64K × 4
421000	1M	1M × 1
424256	1M	256K × 4
44100	4M	4M × 1
44400	4M	1M × 4
44160	4M	256K × 16
416800	16M	8M × 2
416400	16M	4M × 4
416160	16M	1M × 16

- DRAMs are available in a variety of densities and organization
  - Typical DRAM densities
    - 64K bit
    - 256K bit
    - 1M bit, Etc.
    - Modern DRAMS as large as 1G bit
  - Typical organizations of the 4M bit DRAM
    - 4M X 1 bit
    - 1M X 4 bit
    - Modern higher density devices also available in X8, X16, and X32 organizations

9.3 Random Access Read/Write Memories-
Circuit Design using DRAMS



- Sixteen 64KX1-bit DRAMs interconnected to form a 64K word memory subsystem—1M-bits of memory
  - Circuit connections
    - 8 multiplexed address inputs of all devices connected in parallel
    - RAS and CAS lines of all devices connected in parallel
    - Data input and output lines
      - Independent data lines arranged to form a 16-bit wide output bus
      - Independent input lines arranged to form a 16-bit wide input bus
      - In most microprocessor applications input and output lines are connected together
    - Read/write lines
      - W inputs of upper 8 DRAMs connected together and driven by WR0*
      - W inputs of lower 8 DRAMs connected together and driven by WR1*
      - Permits byte-wide or word-wide reads and writes

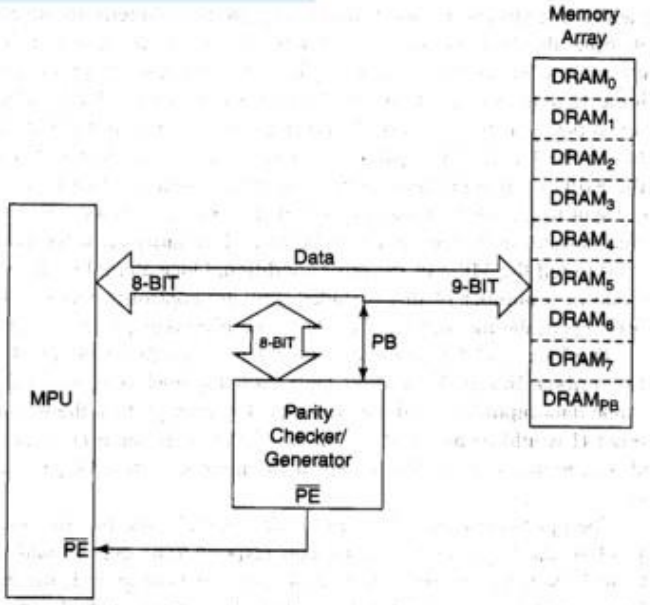
9.3 Random Access Read/Write Memories

- The primary memory section of a microcomputer system is normally formed from both read-only memories and random access read/write memories (RAM)
- RAM is different from ROM in two ways:
  - Data stored in RAM is not permanent in nature.
  - RAM is volatile – that is, if power is removed from RAM, the stored data are lost.
- RAM is normally used to store temporarily data and application programs for execution.

9.3 Random Access Read/Write Memories

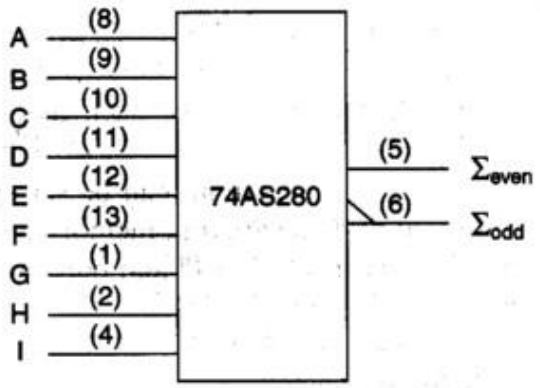
- Static and dynamic RAMs
  - For a static RAM (SRAM), data remain valid as long as the power supply is not turned off.
  - For a dynamic RAM (DRAM), we must both keep the power supply turned on and periodically restore the data in each location.
  - The recharging process is known as *refreshing* the DRAM.

9.4 Parity, The Parity Bit, and Parity-Checker/Generator Circuit- Parity and the Parity Bit



- Data exchange between the MPU and data memory subsystem in a microcomputer must be done without error
  - Sources of errors
    - Emissions that affect data on the data bus line
    - Electrical noise signals—spikes or transients that affect data on data lines
    - Defective bit in a DRAM
    - Soft errors of DRAM
  - Solutions for improving data integrity
    - 1. Parity
    - 2. Error correction code (ECC)
    - Parity most frequently used
  - Parity bit
    - Add an additional bit of data to each byte or word of data so that all elements of data have the same parity
    - Extra bit is known as the "parity bit"
      - Even parity—element of data has an even number of bits at the 1 logic level
      - Odd parity—element of data has an odd number of bit that are logic 1
    - Circuitry added to the DRAM memory interface to generate an appropriate parity bit on writes to memory
    - Extra DRAM required to store the parity bit
    - Circuitry checks element of data from correct parity during read operations
    - Parity errors (PE) reported to MPU usually as an interrupt

9.4 Parity, The Parity Bit, and Parity-Checker/Generator Circuit- Parity Generator/Checker Circuitry



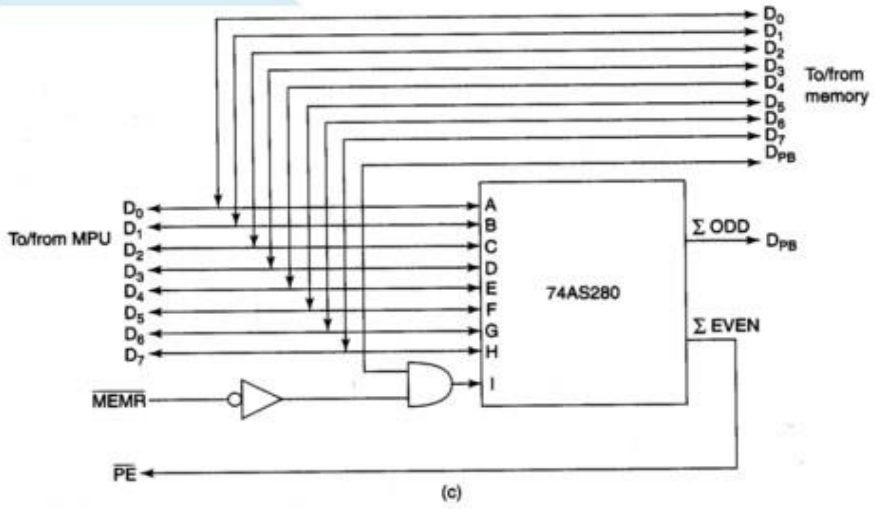
(a)

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0,2,4,6,8	H	L
1,3,5,7,9	L	H

(b)

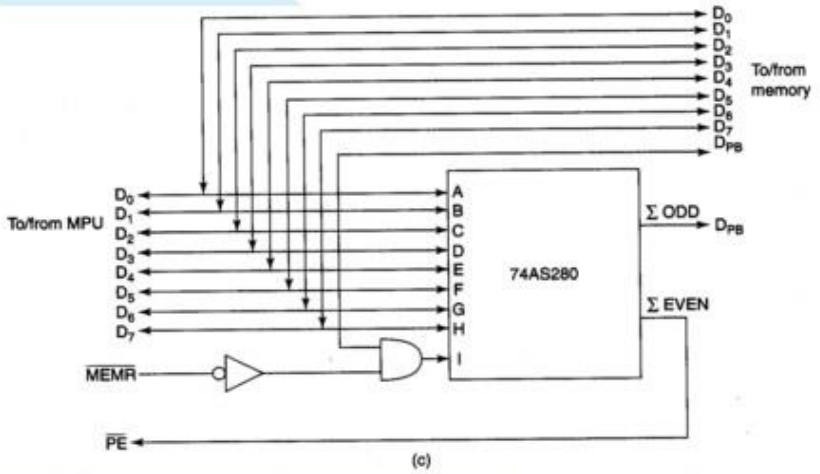
- Parity generator/checker circuit—circuit added to the data memory interface to implement parity
  - May be implemented with a 74AS280 parity generator/checker IC
    - 9 inputs A through I
    - Two outputs Σodd and Σeven
    - Operation:
      - Even number of inputs are logic 1
        - Σeven = 1 and Σodd = 0
        - Signals that input has even parity
      - Odd number of inputs are logic 1
        - Σeven = 0 and Σodd = 1
        - Signals that input has odd parity

9.4 Parity, The Parity Bit, and Parity-Checker/Generator Circuit- Parity Generator/Checker Circuitry



- Even parity generator circuit
  - Circuit configuration
    - Inputs A through H attach in parallel to data bus lines D0 through D7
    - Input I is attached to the data output of the parity DRAM
      - Only activated during read operations
    - Σodd output is attached to the data input of parity DRAM
  - MPU write operation
    - Accepts byte of data to be written to memory as input from the data bus
    - Data also applied in parallel to the input of the DRAMs for data lines D0 through D7
    - Circuit checks parity and generates Σodd and Σeven outputs
    - Σodd output supplied to input of parity DRAM for storage along with the byte in memory
    - If parity is even—Σodd = 0 and 9-bit value saved in memory still has even parity
    - If parity is odd—Σodd = 1 and parity of 9-bit value changed to even and saved in memory

9.4 Parity, The Parity Bit, and Parity-Checker/Generator Circuit- Parity Generator/Checker Circuitry



- **Read operation:**
  - Accepts 9-bit wide input from data outputs of the DRAM subsystem
  - Checks the number of bits that are at the 1 logic level
  - Produces appropriate logic level signals at odd parity and even parity outputs
    - If parity is even—Σeven = 1 and parity is correct
      - Memory operation completes normally
    - If parity is odd—Σeven = 0 and a parity error is detected
      - Error condition signaled to MPU by logic 0 at PE*
      - Usually applied as NMI input to the MPU
      - Must get serviced before executing next instruction
      - MPU may
        - Reattempt memory access
        - Initiate an orderly shut down of application

9.7 8088/8086 Microcomputer System

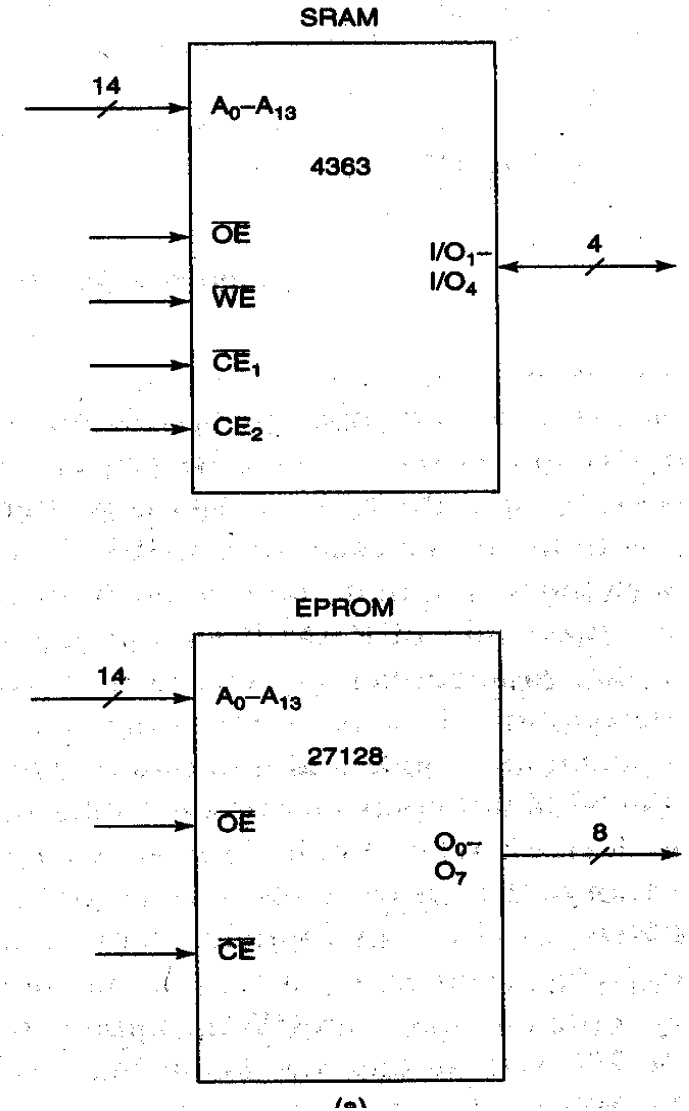
Memory Circuitry

- Data storage memory
  - Information that frequently changes is normally implemented with random access read/write memory (RAM).
  - If the amount of memory required in the microcomputer is small, the memory subsystem is usually designed with SRAMs.
  - DRAMs require refresh support circuit which is not warranted if storage requirement are small.

9.7 8088/8086 Microcomputer System Memory Circuitry

EXAMPLE

Design a memory system consisting of 32Kbytes of R/W memory and 32Kbytes of ROM memory. Use SRAM devices to implement R/W memory and EPROM devices to implement ROM memory. The memory devices to be used are shown below. R/W memory is to reside over the address range 00000H through 07FFFH and the address range of ROM memory is to be F8000H through FFFFFH. Assume that the 8088 microprocessor system bus signals that follow are available for use: A_0 through A_{19}, D_0 through D_7, MEMR', MEMW'.



9.7 8088/8086 Microcomputer System Memory Circuitry

SOLUTION:

First let us determine the number of SRAM devices needed.

No. of SRAM devices = 32Kbyte/(16K x 4) = 4

To provide an 8-bit data bus, two SRAMs must be connected in parallel. Two pairs connected in this way are then placed in series to implement the R/W address range, and each pair implements 16Kbytes.

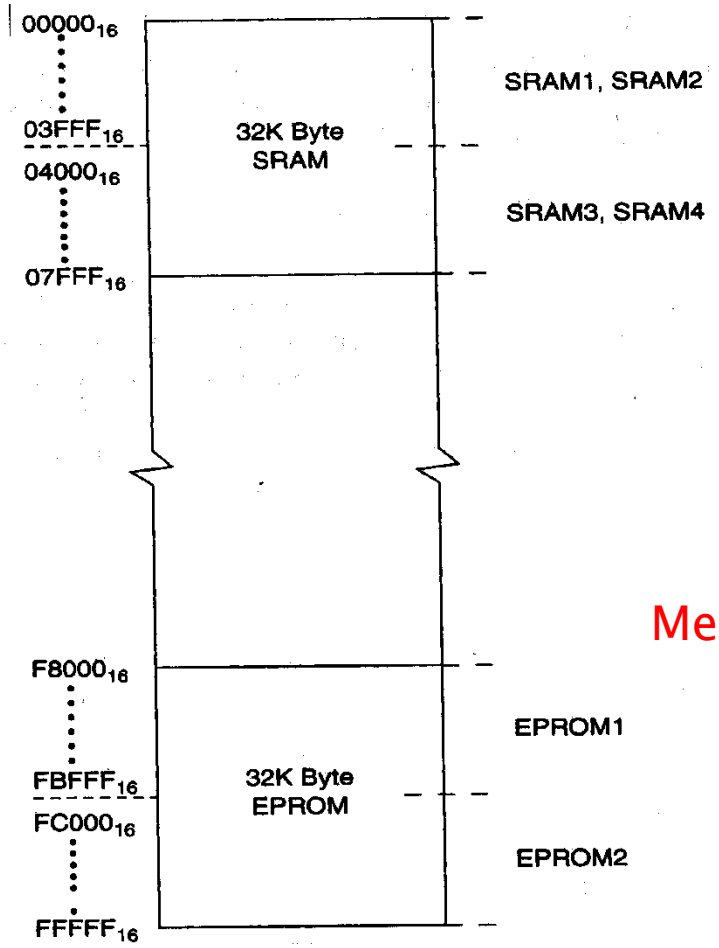
Next let us determine the number of EPROM devices needed.

No. of EPROM devices = 32Kbyte/16Kbyte = 2

These two devices must be connected in series to implement the ROM address range and each implement 16Kbytes of storage.

9.7 8088/8086 Microcomputer System Memory Circuitry

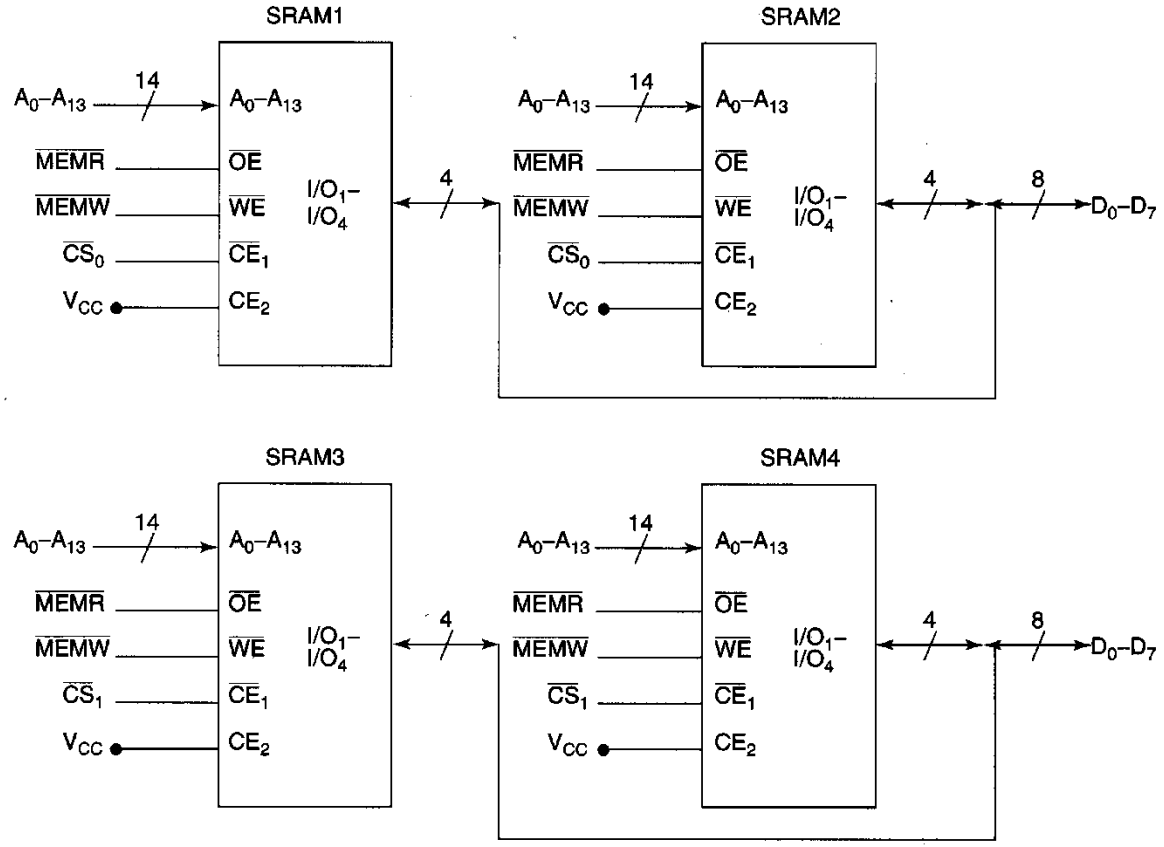
SOLUTION:



Memory map of the system

9.7 8088/8086 Microcomputer System Memory Circuitry

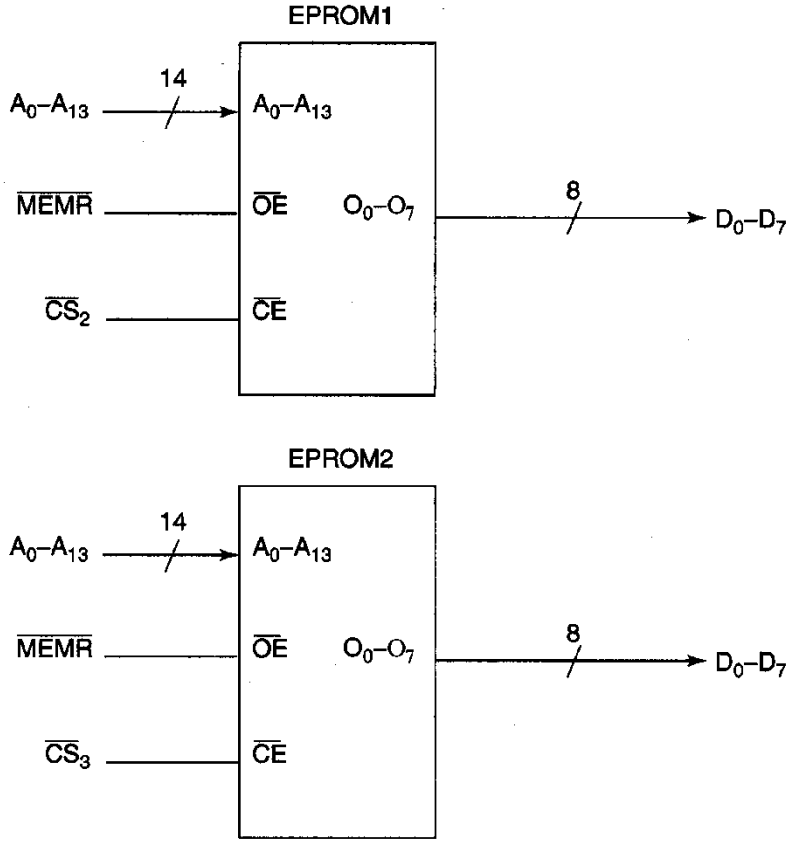
SOLUTION:



RAM memory organization for the system design

9.7 8088/8086 Microcomputer System Memory Circuitry

SOLUTION:



ROM memory organization for the system design

9.7 8088/8086 Microcomputer System Memory Circuitry

SOLUTION:

$A_{19} \ldots\ldots\ldots\ldots\ldots\ldots A_0$

$00000_{16} = 0000\ 0000\ 0000\ 0000\ 0000$

$\vdots \qquad\qquad\qquad \vdots$

$03FFF_{16} = \underbrace{0000\ 0011}_{\overline{CS}_0}\ 1111\ 1111\ 1111$

$04000_{16} = 0000\ 0100\ 0000\ 0000\ 0000$

$\vdots \qquad\qquad\qquad \vdots$

$07FFF_{16} = \underbrace{0000\ 0111}_{\overline{CS}_1}\ 1111\ 1111\ 1111$

$F8000_{16} = 1111\ 1000\ 0000\ 0000\ 0000$

$\vdots \qquad\qquad\qquad \vdots$

$FBFFF_{16} = \underbrace{1111\ 1011}_{\overline{CS}_2}\ 1111\ 1111\ 1111$

$FC000_{16} = 1111\ 1100\ 0000\ 0000\ 0000$

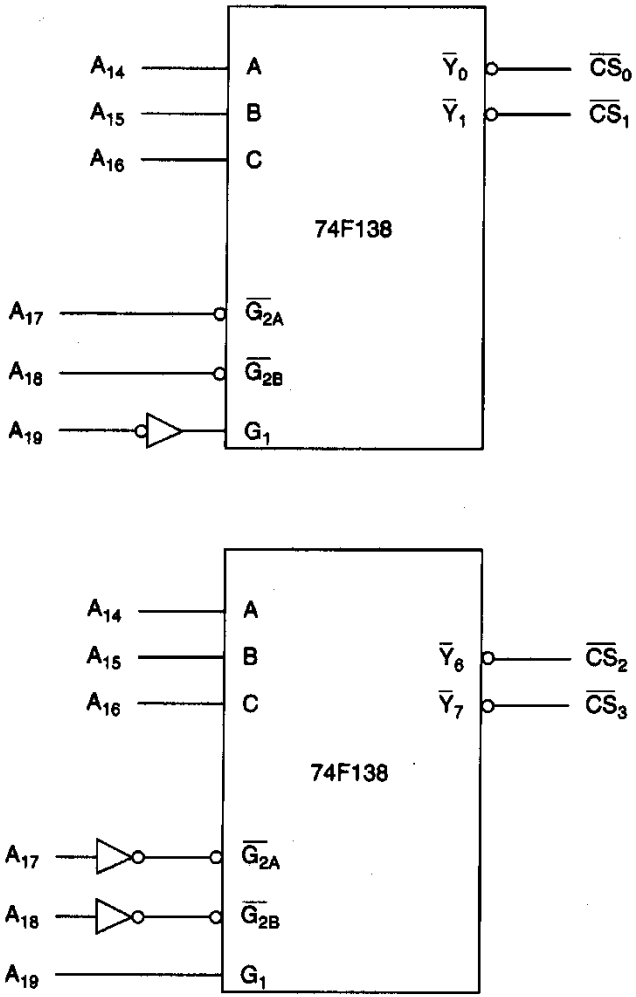
$\vdots \qquad\qquad\qquad \vdots$

$FFFFF_{16} = \underbrace{1111\ 1111}_{\overline{CS}_3}\ 1111\ 1111\ 1111$

Address range analysis for the design of chip select signals

9.7 8088/8086 Microcomputer System Memory Circuitry

SOLUTION:



Chip-select logic