Communication Electronics

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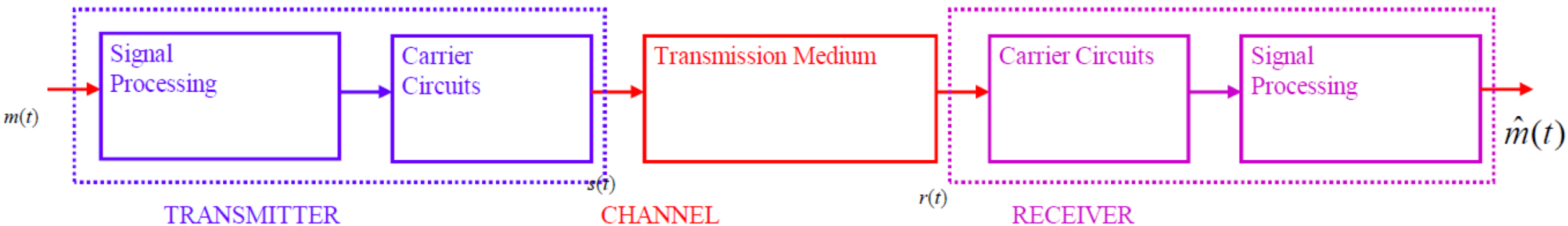
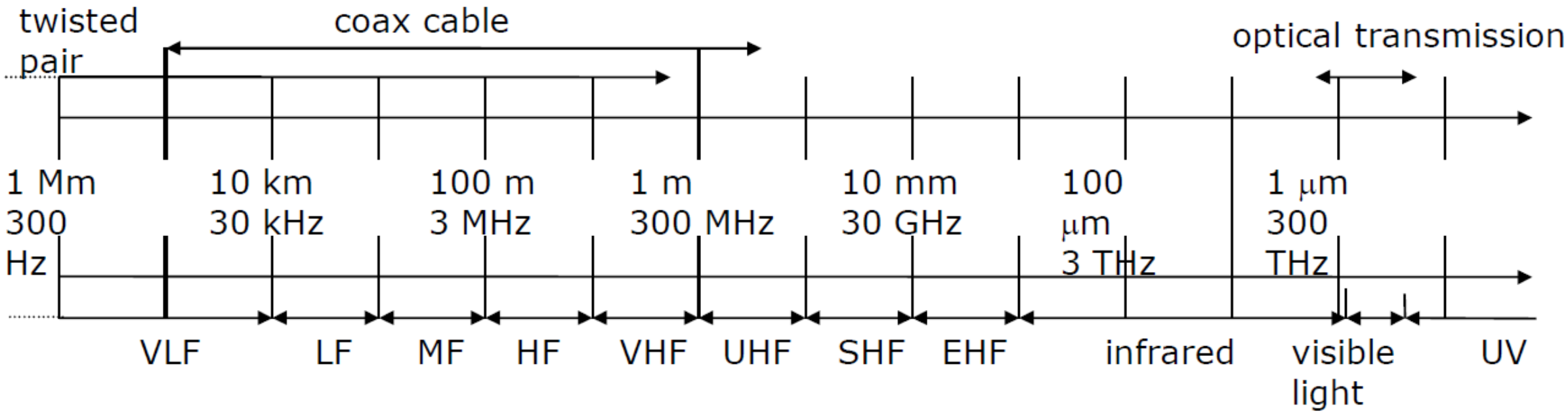
- Elements of a communication system
  - Basic components
    - Transmitter
      - Convert Source (information) to signals
      - Send converted signals to the channel (by antenna if applicable)
    - Channel
      - Wireless: atmosphere (free space)
      - Wired: coaxial cables, twisted wires, optical fibre
    - Receiver
      - Reconvert received signals to original information
      - Output the original information



Frequencies for communication



- VLF = Very Low Frequency
- LF = Low Frequency
  Frequency
- MF = Medium Frequency
- HF = High Frequency
- VHF = Very High Frequency

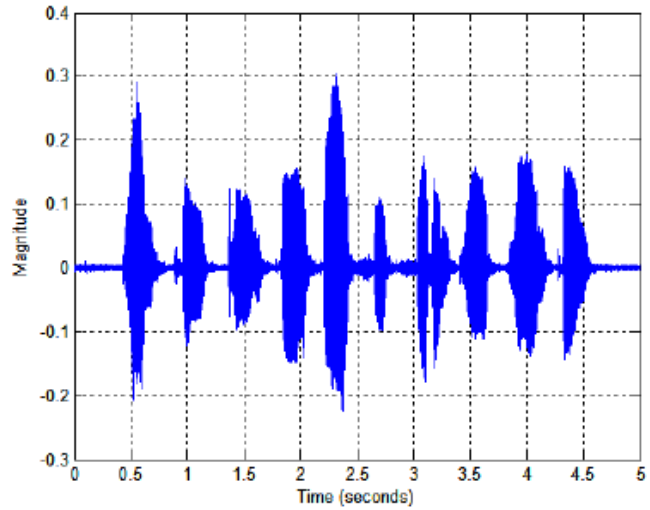
UHF = Ultra High Frequency
SHF = Super High

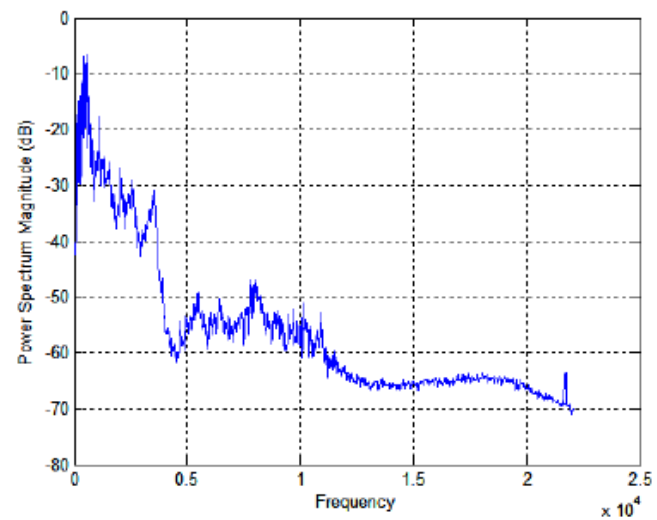
EHF = Extra High Frequency
UV = Ultraviolet Light

- Frequency and wave length:
  $\lambda = c/f$
  wave length λ, speed of light $c \cong 3 \times 10^8$m/s, frequency f

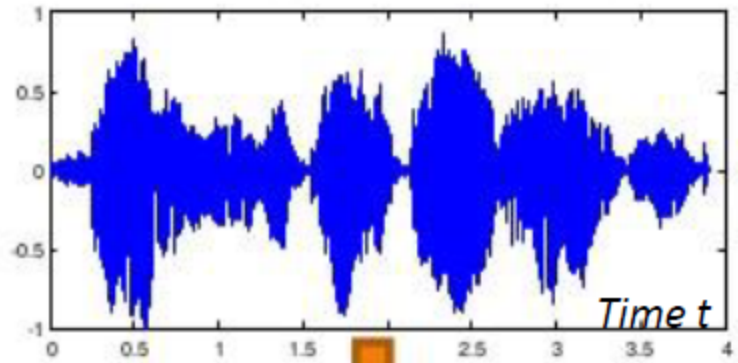
Baseband vs Passband Transmission

- Baseband signals:
  - Voice (0-4kHz)
  - TV (0-6 MHz)
- A signal may be sent in its baseband format when a dedicated wired channel is available.
- Otherwise, it must be converted to passband.



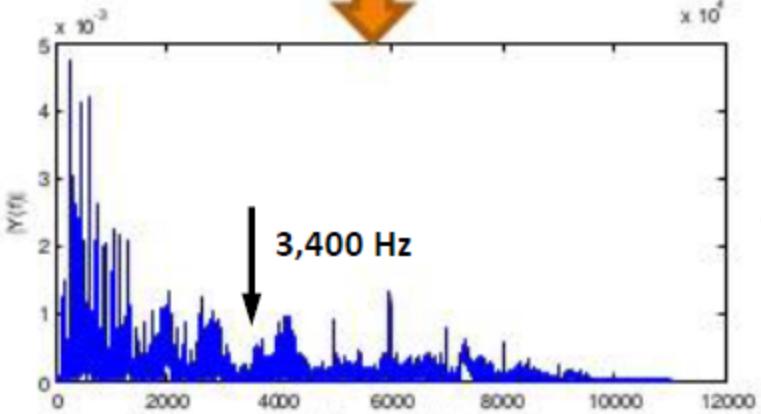


Speech signal



Waveform as received from a microphone converting acoustic energy into electrical energy.

Speech spectra



Fast Fourier transform of the above speech waveform showing energy over range of 0 Hz to 12 kHz.

Modulation: What and Why?

- The process of shifting the baseband signal to passband range is called *Modulation*.
- The process of shifting the passband signal to baseband frequency range is called *Demodulation*.
- Reasons for modulation:
  - Simultaneous transmission of several signals
  - Practical Design of Antennas
  - Exchange of power and bandwidth

Types of (Carrier) Modulation

- In modulation, one characteristic of a signal (generally a sinusoidal wave) known as the *carrier* is changed based on the information signal that we wish to transmit (*modulating signal*).
- That could be the amplitude, phase, or frequency, which result in Amplitude modulation (AM), Phase modulation (PM), or Frequency modulation (FM). The last two are combined as Angle Modulation

Types of Amplitude Modulation (AM)

- **Double Sideband with carrier (we will call it AM)**: This is the most widely used type of AM modulation. In fact, all radio channels in the AM band use this type of modulation.
- **Double Sideband Suppressed Carrier (DSBSC):** This is the same as the AM modulation above but without the carrier.
- **Single Sideband (SSB):** In this modulation, only half of the signal of the DSBSC is used.
- **Vestigial Sideband (VSB):** This is a modification of the SSB to ease the generation and reception of the signal.

Amplitude Modulation (AM)

Lets Review some
basics ….

As the name suggests, in AM, the information signal varies the amplitude of the carrier sine wave. The instantaneous value of the carrier amplitude changes in accordance with the amplitude and frequency variations of the modulating signal.

The carrier frequency remains constant during the modulation process, but its amplitude varies in accordance with the modulating signal.

Both the positive and the negative peaks of the carrier wave vary with the modulating signal. An increase or a decrease in the amplitude of the modulating signal causes a corresponding increase or decrease in both the positive and the negative peaks of the carrier amplitude.

An imaginary line connecting the positive peaks and negative peaks of the carrier waveform (the dashed line in Fig. 3-1) gives the exact shape of the modulating information signal. This imaginary line on the carrier waveform is known as the *envelope.*

Using trigonometric functions, we can express the sine wave carrier with the simple expression

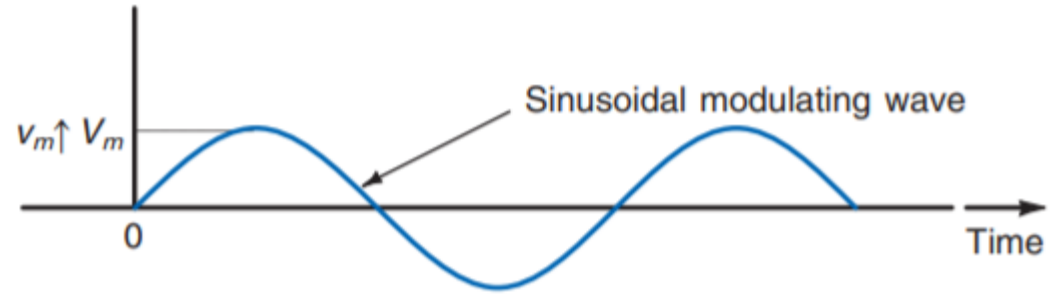
$$v_c = V_c \sin 2\pi f_c t$$

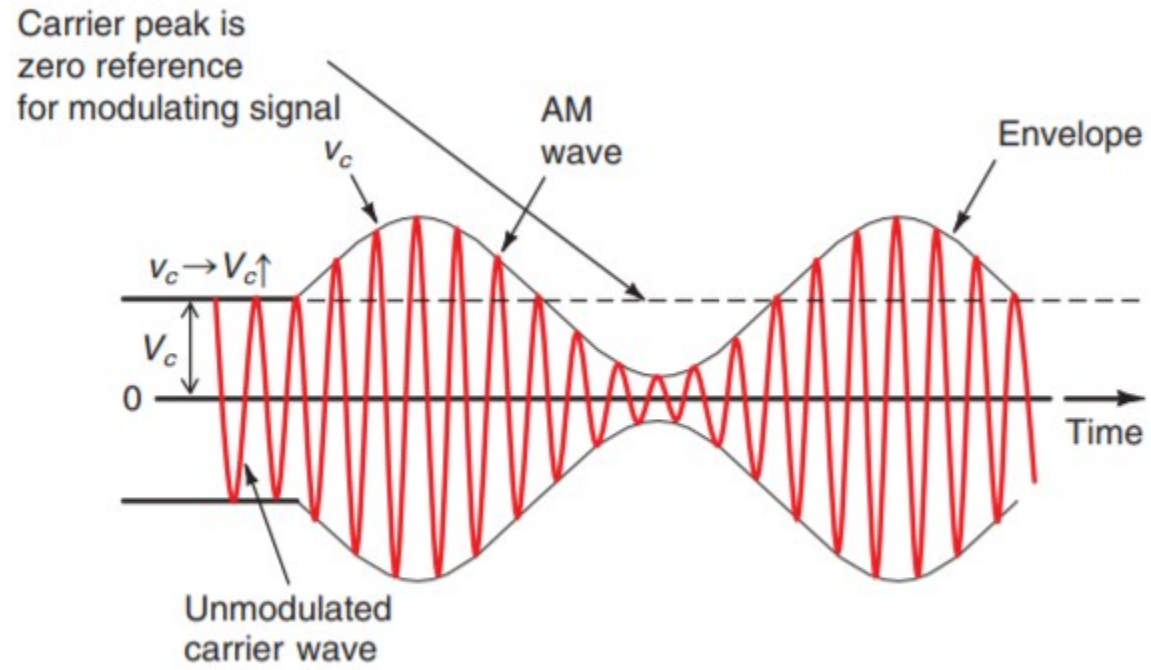
A sine wave modulating signal can be expressed with a similar formula $v_m = V_m \sin 2\pi f_m t$

where v_m = instantaneous value of information signal

V_m = peak amplitude of information signal

f_m = frequency of modulating signal

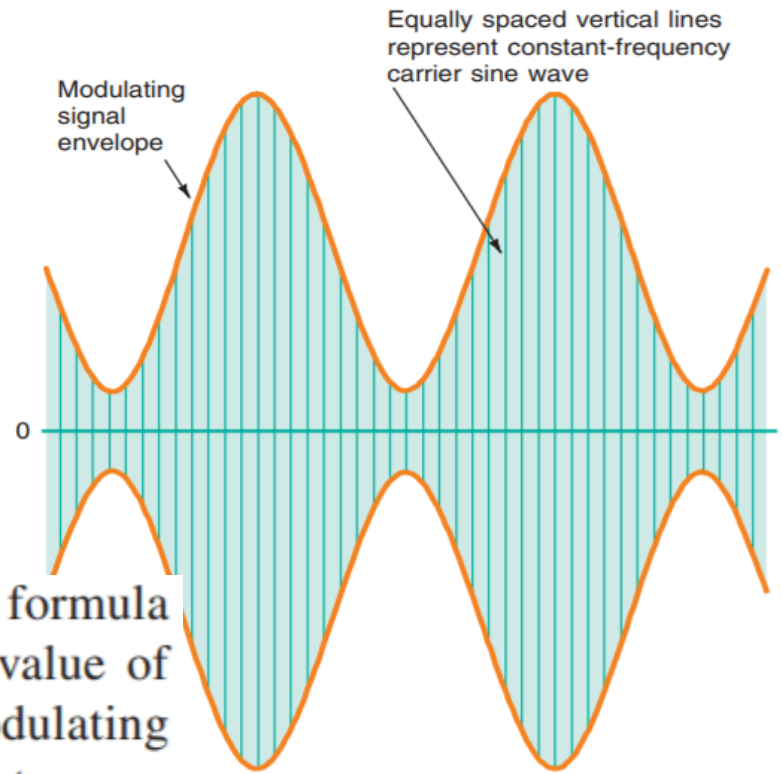




(*b*)

the modulating signal uses the peak value of the carrier rather than zero as its reference point. The envelope of the modulating signal varies above and below the peak carrier amplitude. That is, the zero reference line of the modulating signal coincides with the peak value of the unmodulated carrier.

In general, the amplitude of the modulating signal should be less than the amplitude of the carrier. When the amplitude of the modulating signal is greater than the amplitude of the carrier, distortion will occur, causing incorrect information to be transmitted. In amplitude modulation, it is particularly important that the peak value of the modulating signal be less than the peak value of the carrier.



$$V_m < V_c$$

Values for the carrier signal and the modulating signal can be used in a formula to express the complete modulated wave. First, keep in mind that the peak value of the carrier is the reference point for the modulating signal; the value of the modulating signal is added to or subtracted from the peak value of the carrier. The instantaneous value of either the top or the bottom voltage envelope v_1 can be computed by using the equation

$$v_1 = V_c + v_m = V_c + V_m \sin 2\pi f_m t$$

which expresses the fact that the instantaneous value of the modulating signal algebraically adds to the peak value of the carrier. Thus, we can write the instantaneous value of the complete modulated wave v_2 by substituting v_1 for the peak value of carrier voltage V_c as follows:

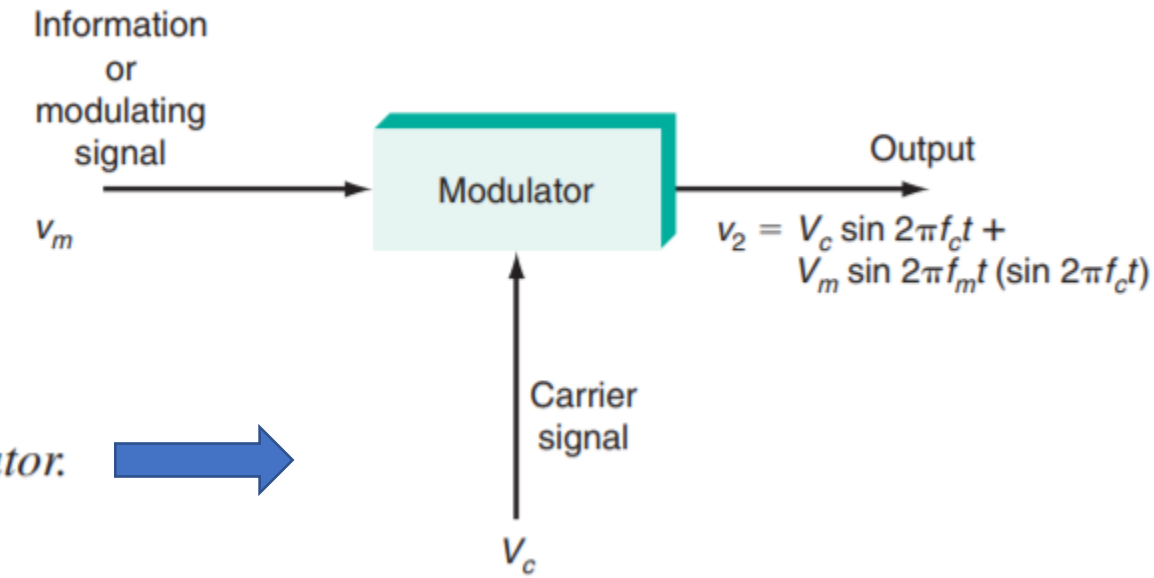
$$v_2 = v_1 \sin 2\pi f_c t$$

Now substituting the previously derived expression for v_1 and expanding, we get the following:

$$v_2 = (V_c + V_m \sin 2\pi f_m t) \sin 2\pi f_c t = V_c \sin 2\pi f_c t + (V_m \sin 2\pi f_m t)(\sin 2\pi f_c t)$$

Or can be written using angular frequency form:

$$g_{AM}(t) = [A + m(t)]\cos(\omega_C t)$$
$$= A\cos(\omega_C t) + m(t)\cos(\omega_C t)$$

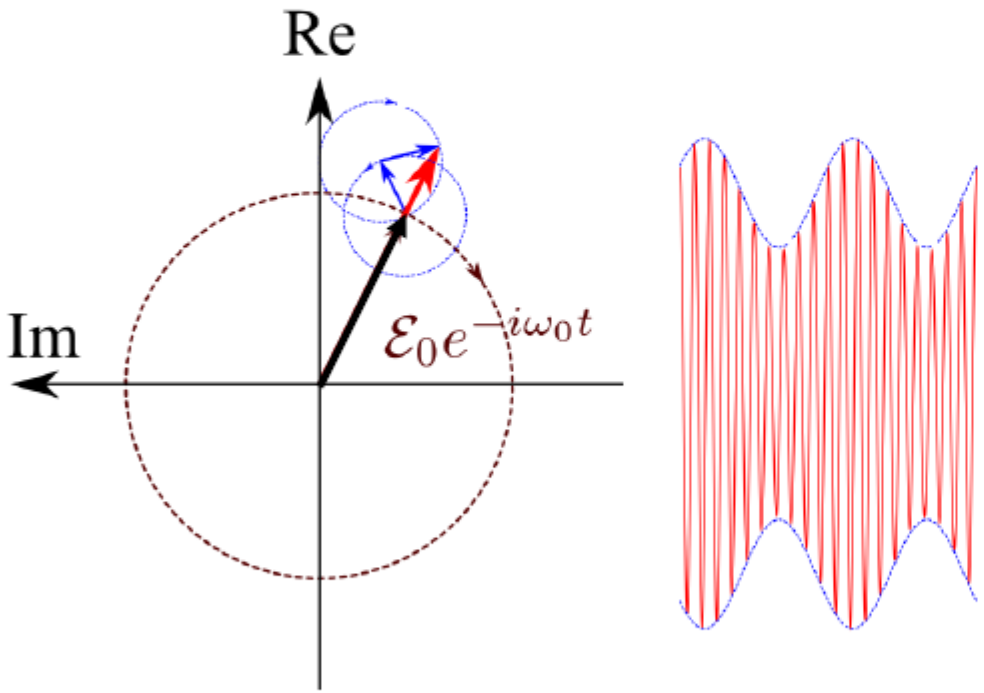


The circuit used for producing AM is called a *modulator*.

Phasor View of Amplitude Modulation

Example showing tone modulation

a) Amplitude modulation phasor diagram



Black vector ⇒ Carrier signal

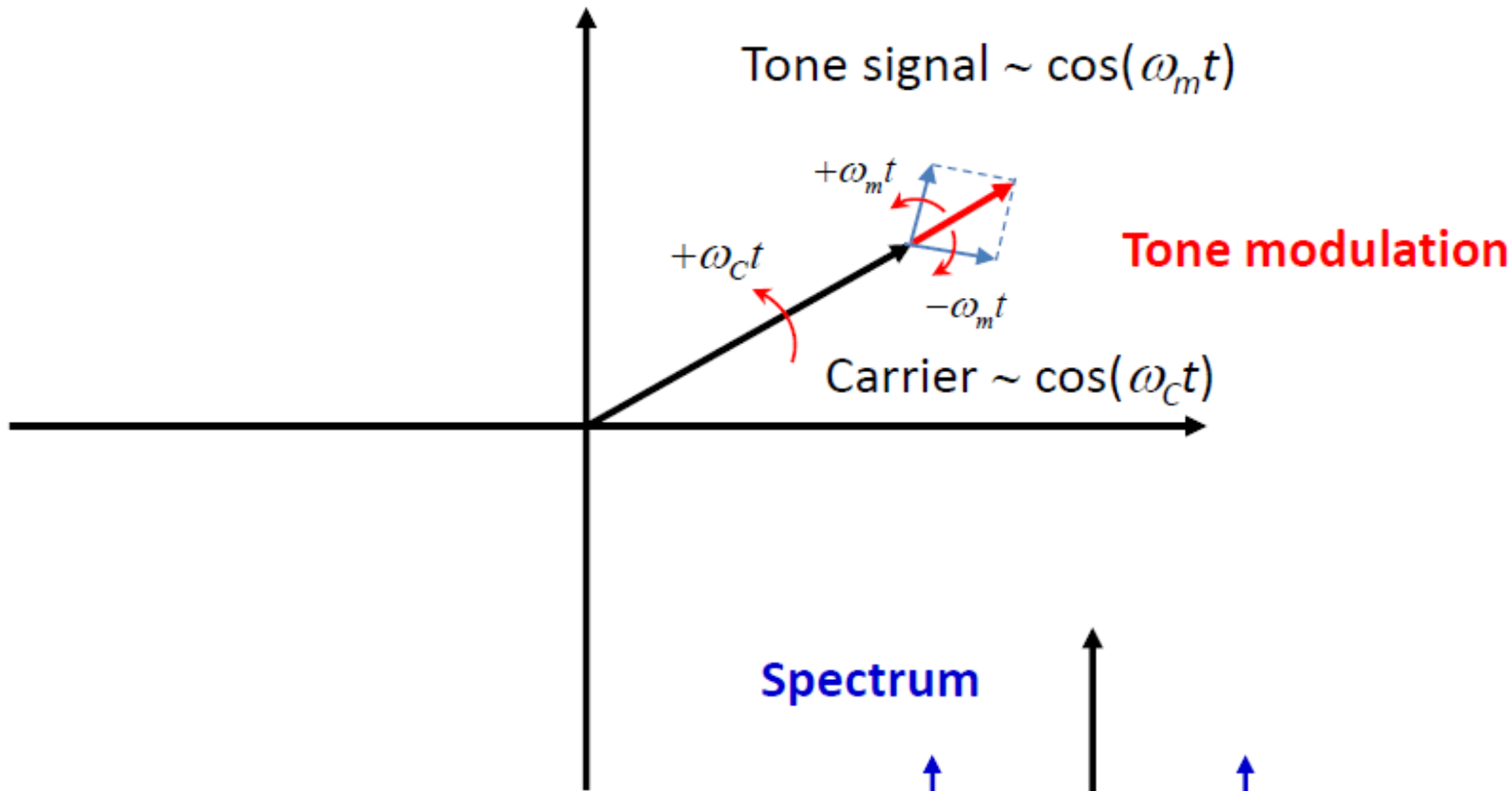
Red vector ⇒ AM modulated signal

Modulated oscillation is a sum of these three vectors an is given by the red vector. In the case of amplitude modulation (AM), the modulated oscillation vector is always in phase with the carrier field while its length oscillates with the modulation frequency. The time dependence of its projection onto the real axis gives the signal strength as drawn to the right of the corresponding phasor diagram.

Phasor Expression of Amplitude Modulation

Complex Exponential Format

$$\phi_{AM}(t) = \mathrm{Re}\left[e^{j\omega_C t}\left(1 + \frac{e^{j\omega_m t}}{2} + \frac{e^{-j\omega_m t}}{2}\right)\right]$$



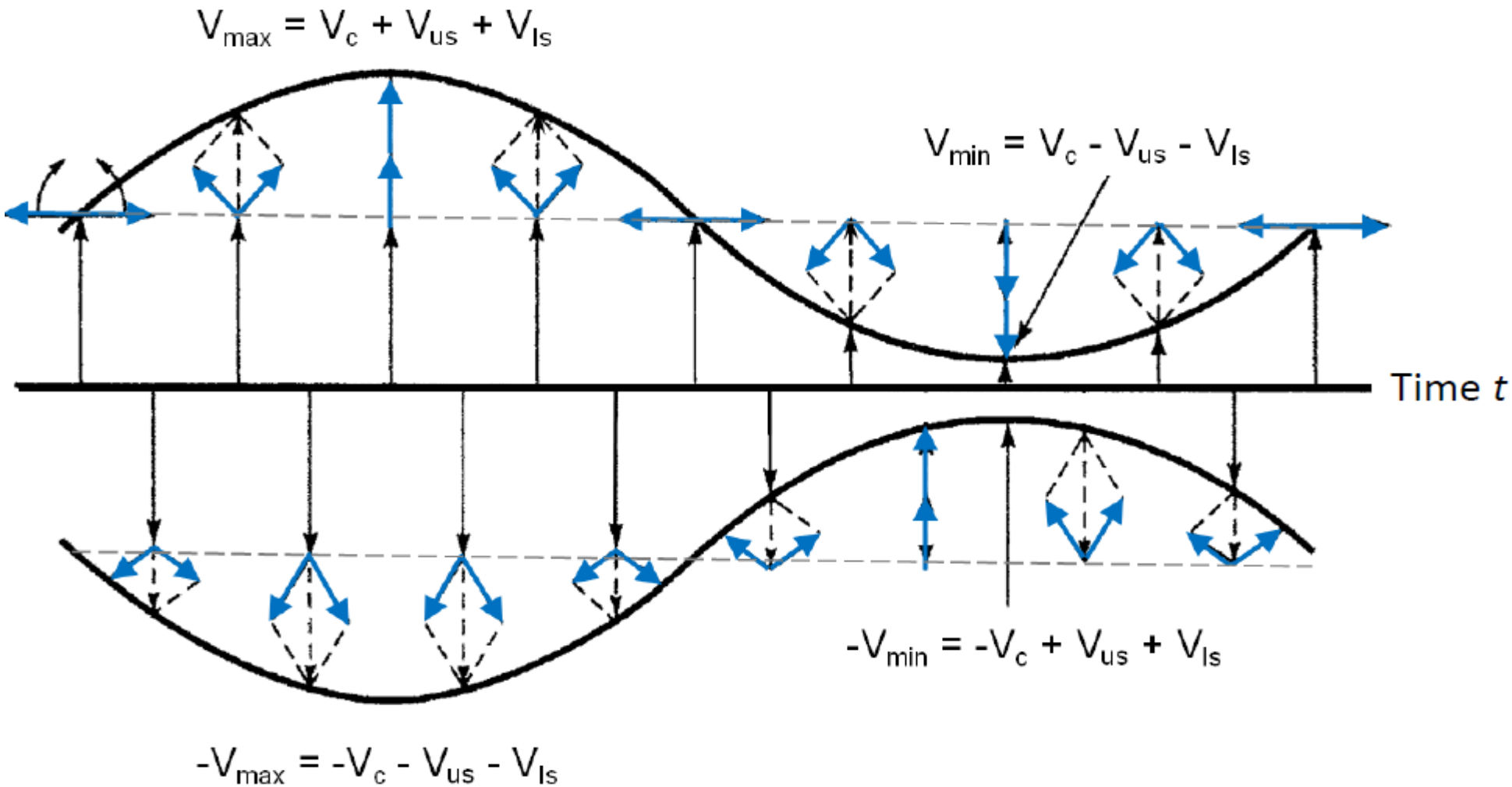
Tone modulation

Spectrum

Phasor Interpretation of AM DSB with Carrier (continued)

Tone modulation

V_{us} = Voltage of upper sideband phasor
V_{ls} = Voltage of lower sideband phasor
V_c = Voltage of the carrier



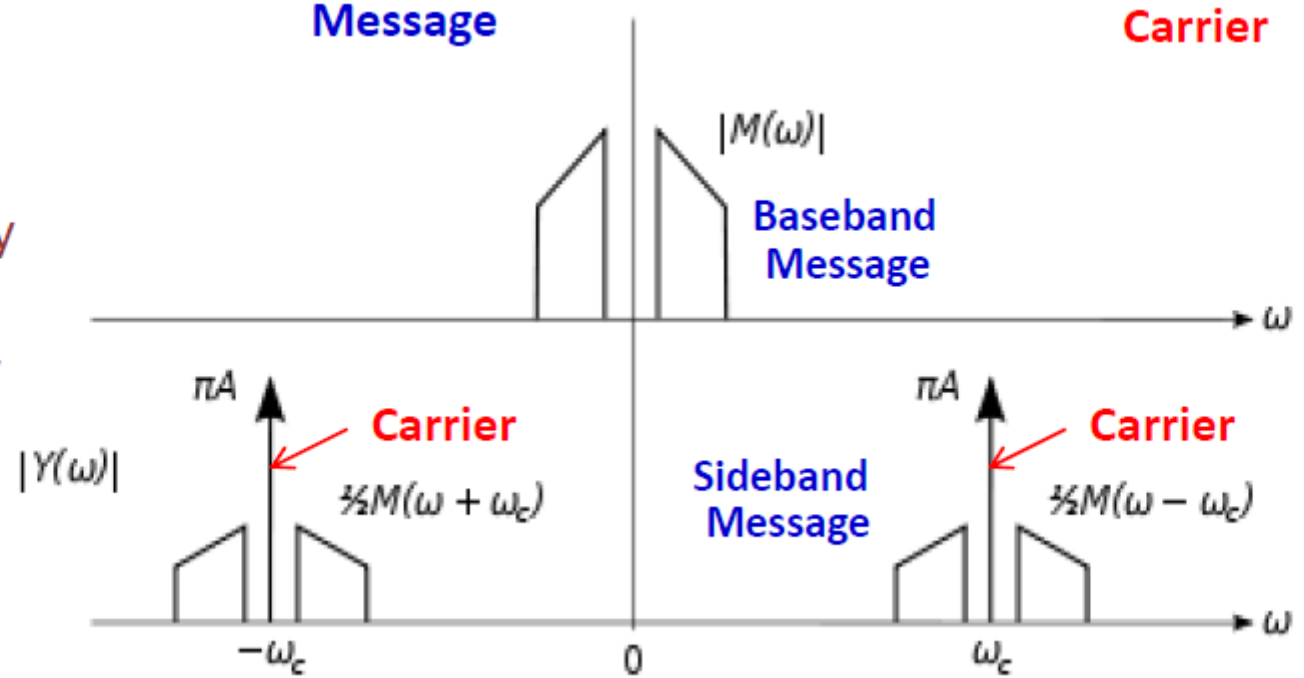
Double-Sideband Amplitude Modulation Spectrum

$$\phi_{AM}(t) = m(t)\cdot\cos(\omega_C t) + A_C\cos(\omega_C t) = [A_C + m(t)]\cdot\cos(\omega_C t)$$

The spectrum $\Phi_{AM}(\omega)$ is found from the Fourier transform of $\phi_{AM}(t)$

$$\mathcal{F}\left[\phi_{AM}(t)\right] = \underbrace{\tfrac{1}{2}M(\omega-\omega_C) + \tfrac{1}{2}M(\omega+\omega_C)}_{\text{Message}} + \underbrace{\pi A[\delta(\omega-\omega_C)+\delta(\omega+\omega_C)]}_{\text{Carrier}}$$

Frequency Shifting Property



What is Modulation Index?

the relationship between the amplitude of the modulating signal and the amplitude of the carrier signal is important. This relationship, known as the *modulation index m* (also called the modulating factor or coefficient, or the degree of modulation), is the ratio

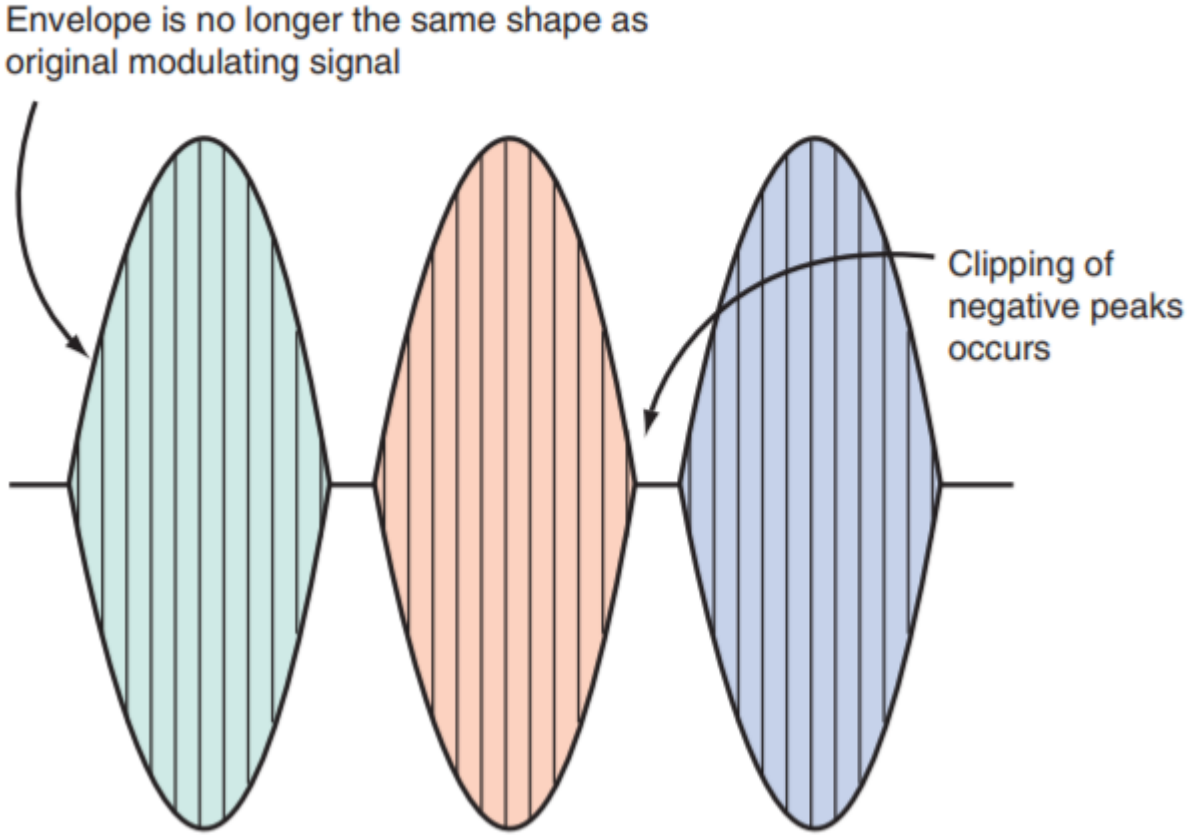
$$m = \frac{V_m}{V_c}$$

For example, if the carrier voltage is 9 V and the modulating signal voltage is 7.5 V, the modulation factor is 0.8333 and the percentage of modulation is $0.833 \times 100 = 83.33$.

The modulation index should be a number between 0 and 1.

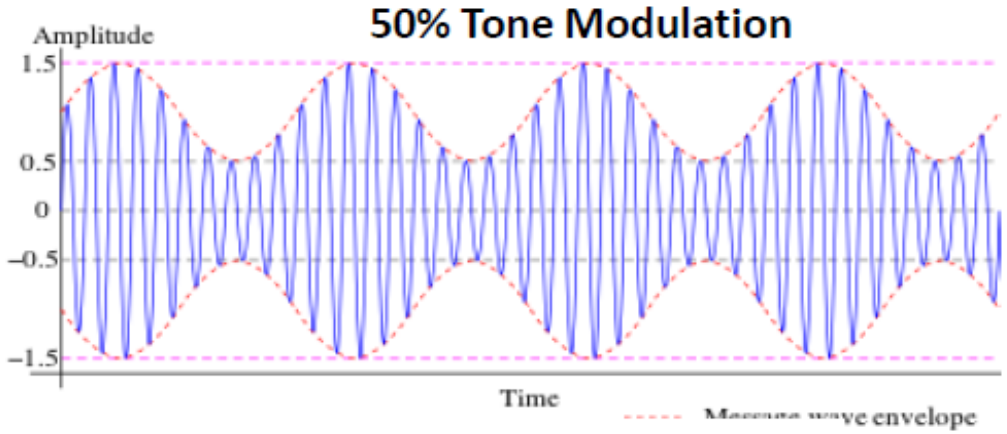
Distortion due to Overmodulation

Distortion of the envelope caused by overmodulation where the modulating signal amplitude V_m is greater than the carrier signal V_c.

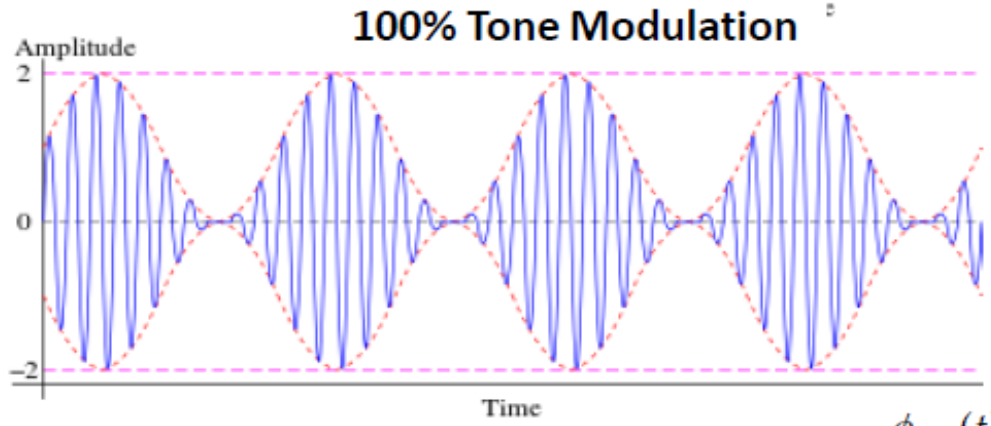


AM Modulation Index Basics – Examples

50%



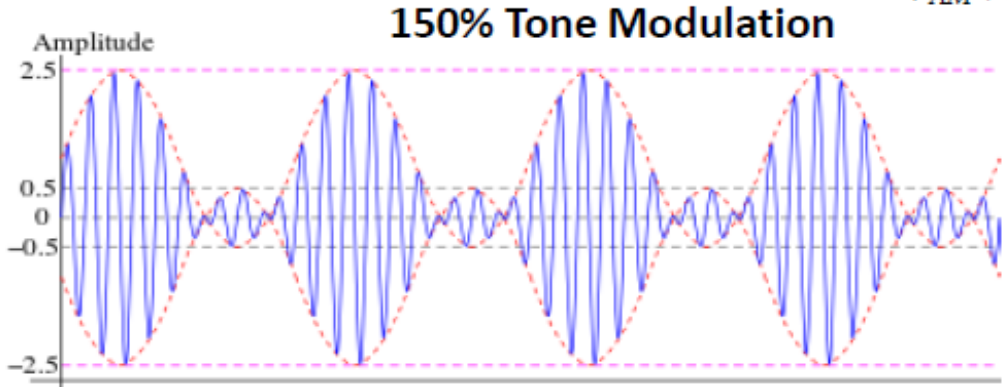
100%



$$\mu = \frac{m_p}{A_C}$$

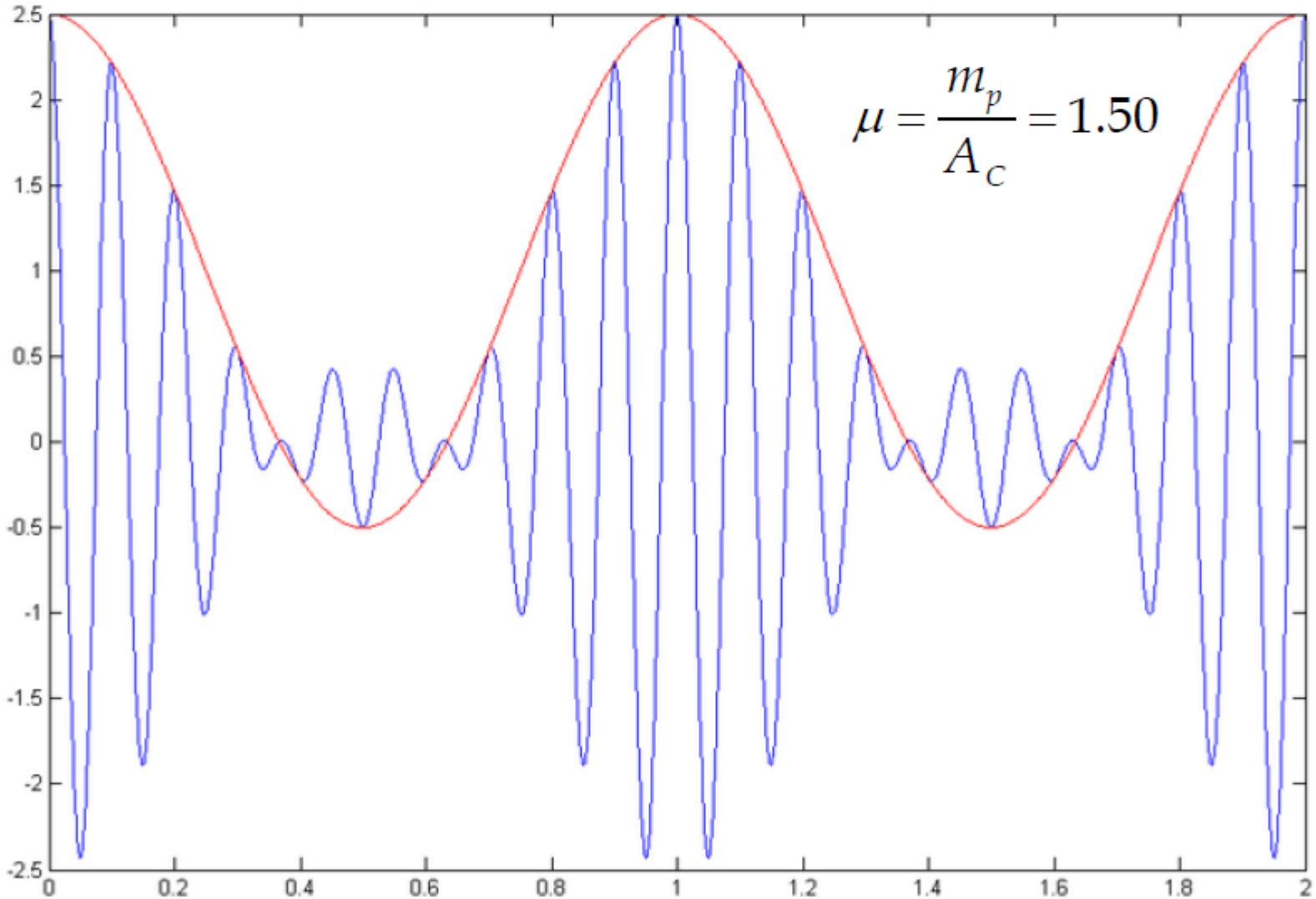
$$\phi_{AM}(t) = A_C\left[1 + \mu \cdot \cos(\omega_m t)\right] \cdot \cos(\omega_c t)$$

150%



Overmodulation
or
Envelope Distortion

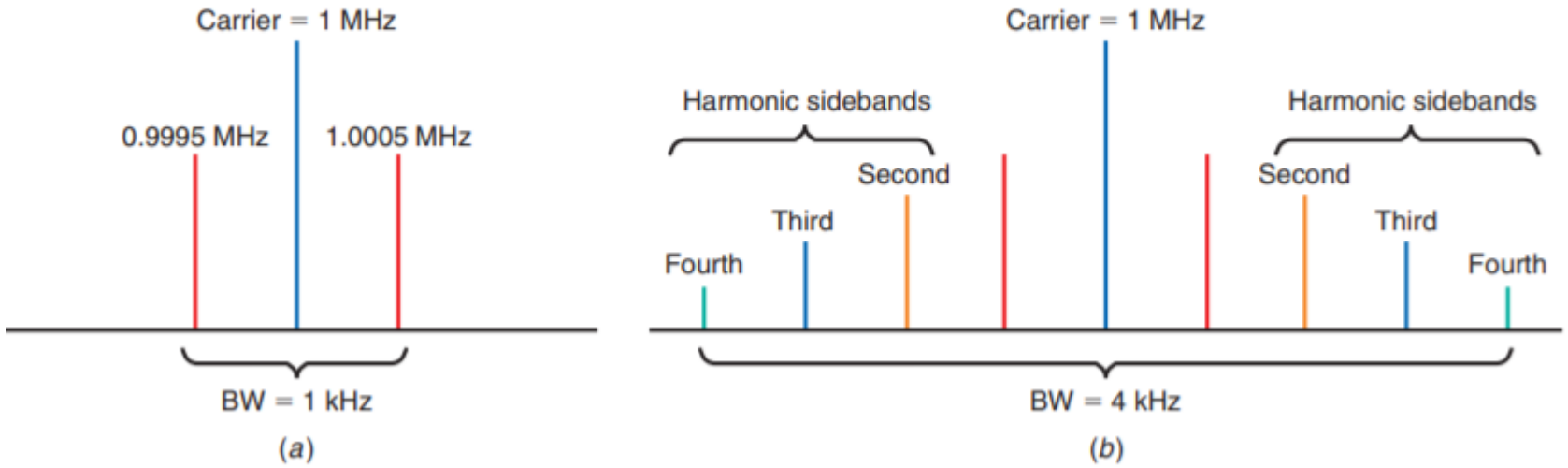
AM Overmodulation → Envelope Distortion



Effect of distortion or overmodulation over spectrum

the spectrum produced by a 500-Hz sine wave mod ulating a carrier of 1 MHz is shown in Fig. 3-14(*a*). The total bandwidth of the signal is 1 kHz. However, if the modulating signal is distorted, the second, third, fourth, and higher harmonics are generated. then the total bandwidth of the resulting signal is about 4 kHz instead of the 1-kHz bandwidth that would result without overmodulation and distortion.

The effect of overmodulation and distortion on AM signal bandwidth. (*a*) Sine wave of 500 Hz modulating a 1-MHz carrier. (*b*) Distorted 500-Hz sine wave with significant second, third, and fourth harmonics.



Percentage of modulation

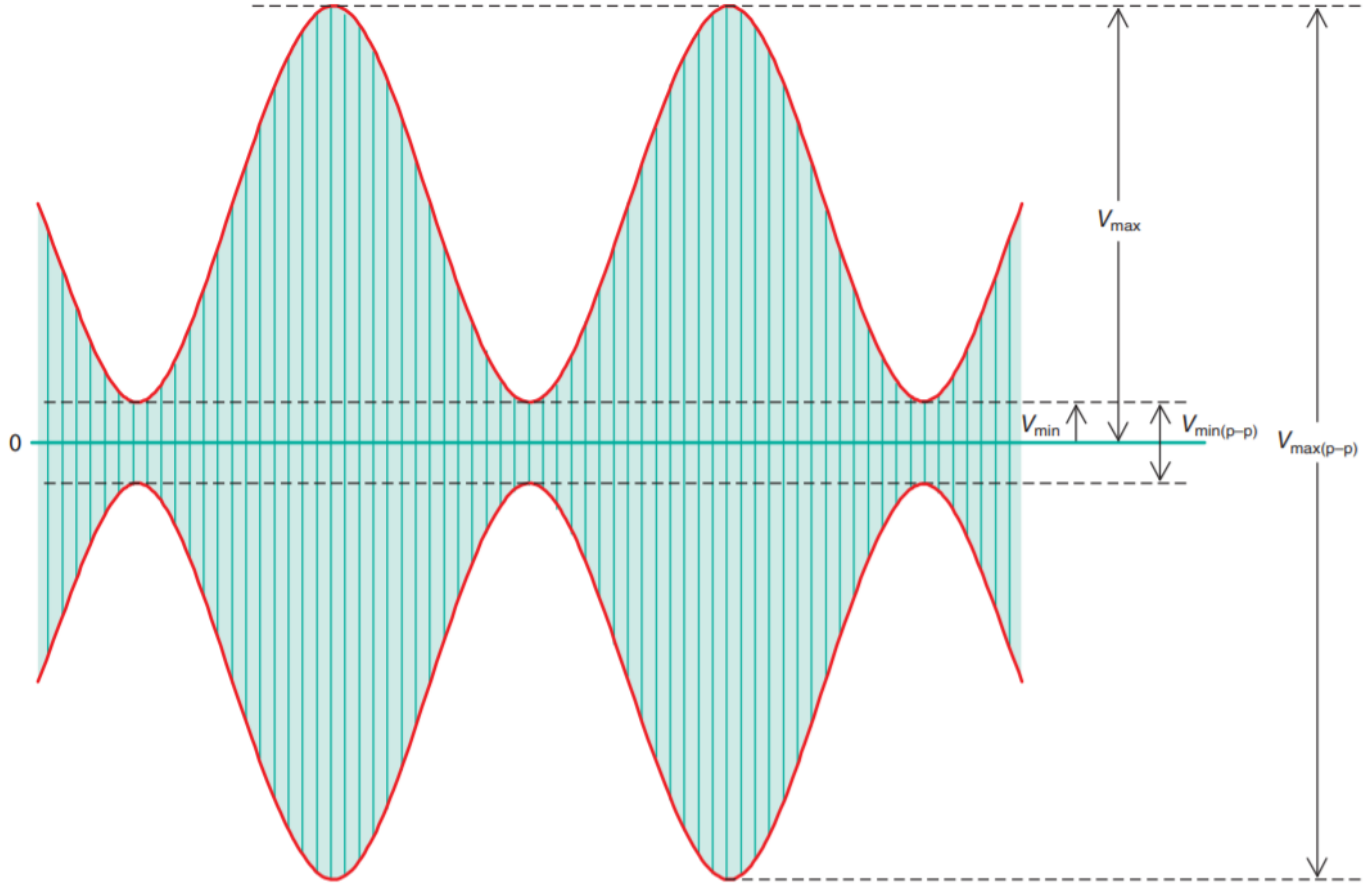
The modulation index can be determined by measuring the actual values of the modulation voltage and the carrier voltage and computing the ratio.

$$V_m = \frac{V_{max} - V_{min}}{2}$$

$$V_c = \frac{V_{max} + V_{min}}{2}$$

The modulation index is

$$m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$$



Sidebands and Frequency Domain

The upper sideband f_{USB} and lower sideband f_{LSB} are computed as

$$f_{USB} = f_c + f_m \quad \text{and} \quad f_{LSB} = f_c - f_m$$

where f_c is the carrier frequency and f_m is the modulating frequency.

The existence of sidebands can be demonstrated mathematically, starting with the equation for an AM signal described previously:

$$\upsilon_{AM} = V_c \sin 2\pi f_c t + (V_m \sin 2\pi f_m t)(\sin 2\pi f_c t)$$

By using the trigonometric identity that says that the product of two sine waves is

$$\sin A \sin B = \frac{\cos (A - B)}{2} - \frac{\cos (A + B)}{2}$$

and substituting this identity into the expression a modulated wave, the instantaneous amplitude of the signal becomes

$$\upsilon_{AM} = V_c \sin 2\pi f_c t + \frac{V_m}{2} \cos 2\pi t(f_c - f_m) - \frac{V_m}{2} \cos 2\pi t(f_c + f_m)$$

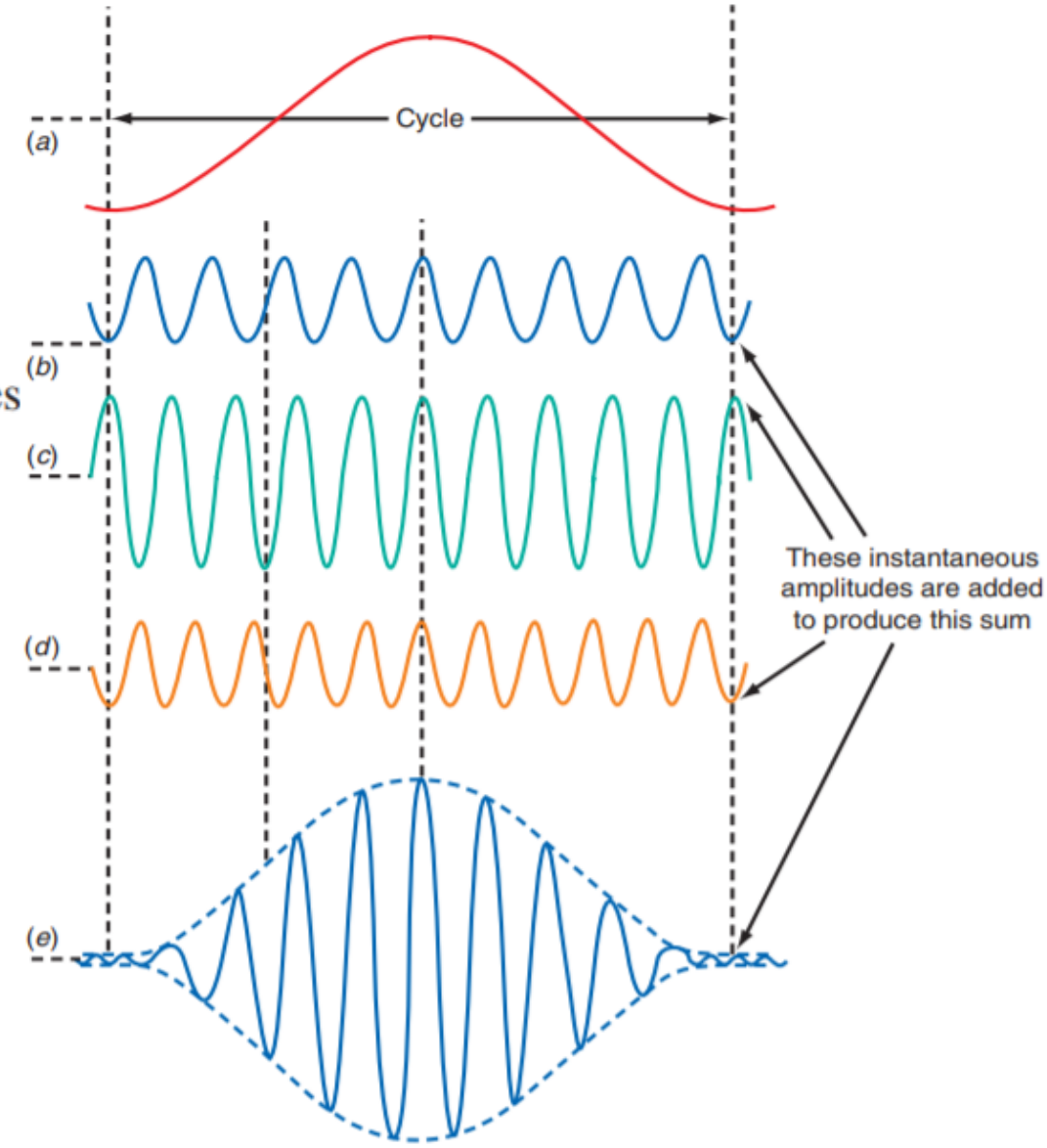
Time Domain AM

where the first term is the carrier; the second term, containing the difference $f_c - f_m$, is the lower sideband; and the third term, containing the sum $f_c + f_m$, is the upper sideband. For example, assume that a 400-Hz tone modulates a 300-kHz carrier. The upper and lower sidebands are

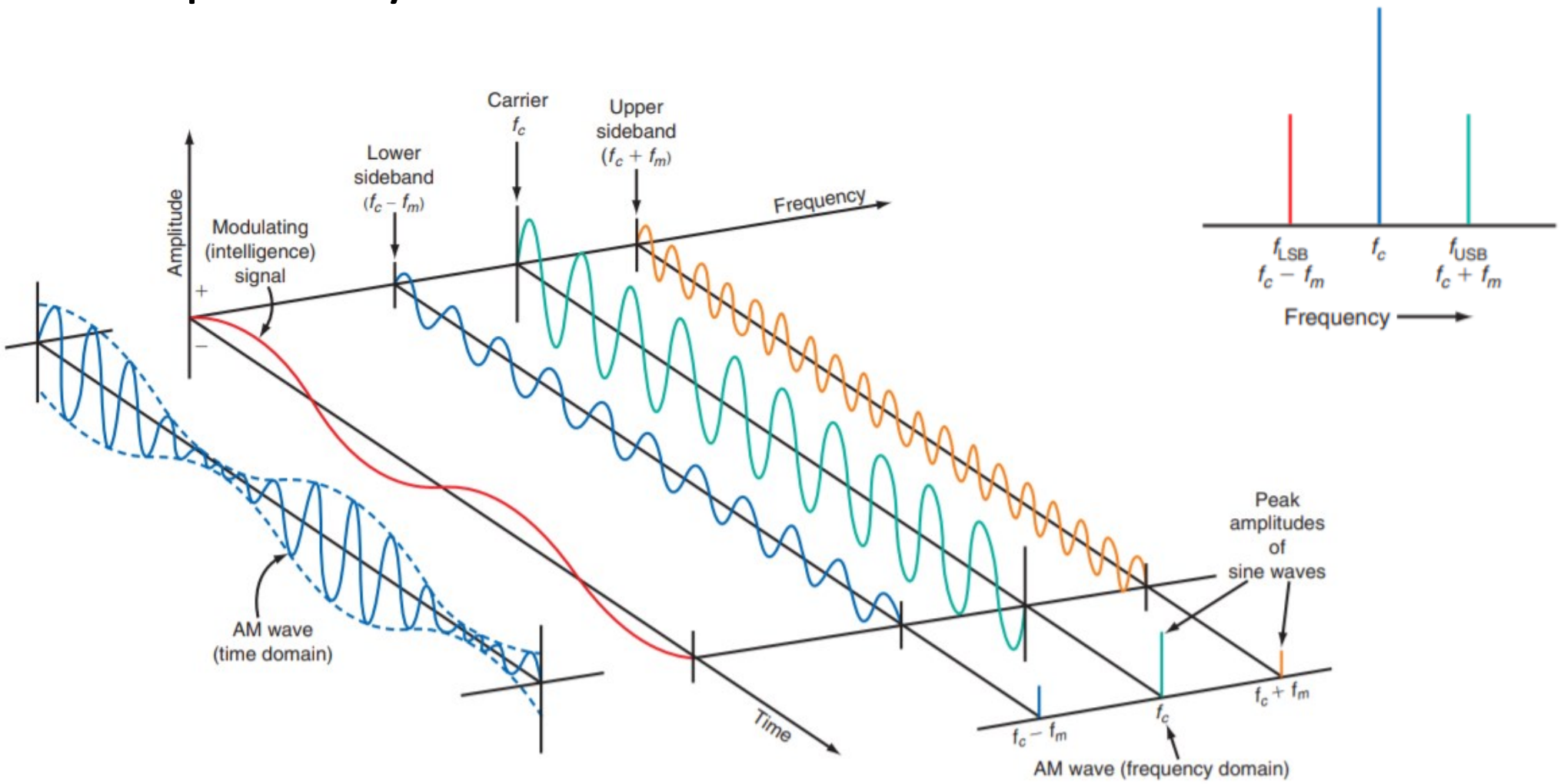
$$f_{USB} = 300{,}000 + 400 = 300{,}400 \text{ Hz} \quad \text{or} \quad 300.4 \text{ kHz}$$

$$f_{LSB} = 300{,}000 - 400 = 299{,}600 \text{ Hz} \quad \text{or} \quad 299.6 \text{ kHz}$$

The AM wave is the algebraic sum of the carrier and upper and lower sideband sine waves. (*a*) Intelligence or modulating signal. (*b*) Lower sideband. (*c*) Carrier. (*d*) Upper sideband. (*e*) Composite AM wave.

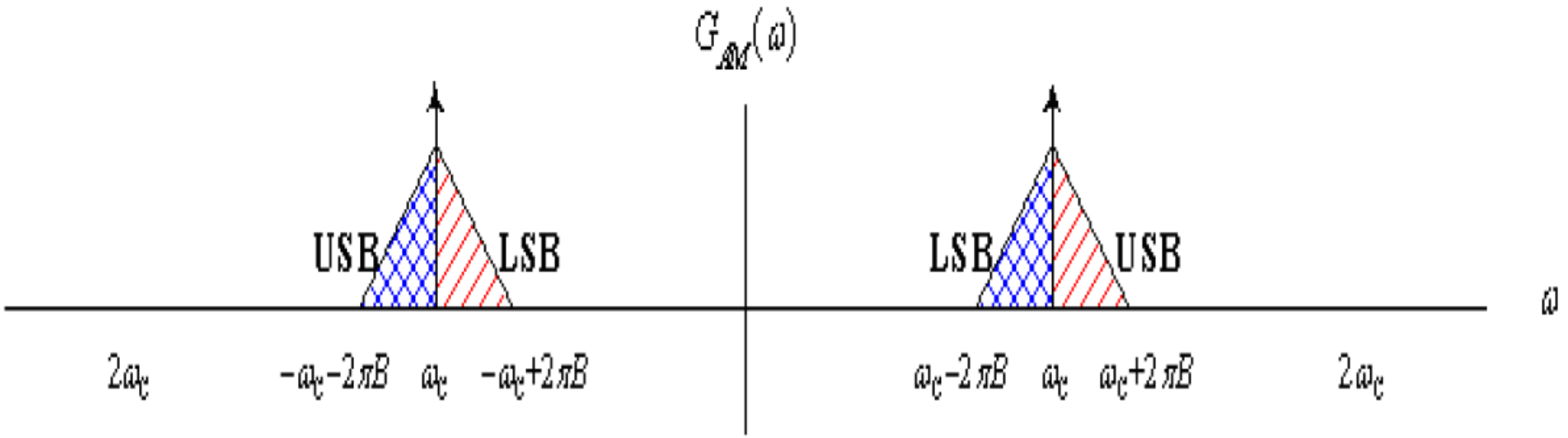


Frequency Domain AM



Fourier transform of AM modulated signal

$$g_{AM}(t) = [A + m(t)]\cos(\omega_C t)$$
$$= A\cos(\omega_C t) + m(t)\cos(\omega_C t)$$
$$g_{AM}(t) \Leftrightarrow \pi A[\delta(\omega - \omega_C) + \delta(\omega + \omega_C)] + \frac{1}{2}[M(\omega - \omega_C) + M(\omega + \omega_C)]$$



Voice signal Modulation

The total bandwidth of an AM signal is calculated by computing the maximum and minimum sideband frequencies. This is done by finding the sum and difference of the carrier frequency and maximum modulating frequency (3000 Hz, or 3 kHz).

For example, if the carrier frequency is 2.8 MHz (2800 kHz), then the maximum and minimum sideband frequencies are

$$f_{USB} = 2800 + 3 = 2803 \text{ kHz} \quad \text{and} \quad f_{LSB} = 2800 - 3 = 2797 \text{ kHz}$$

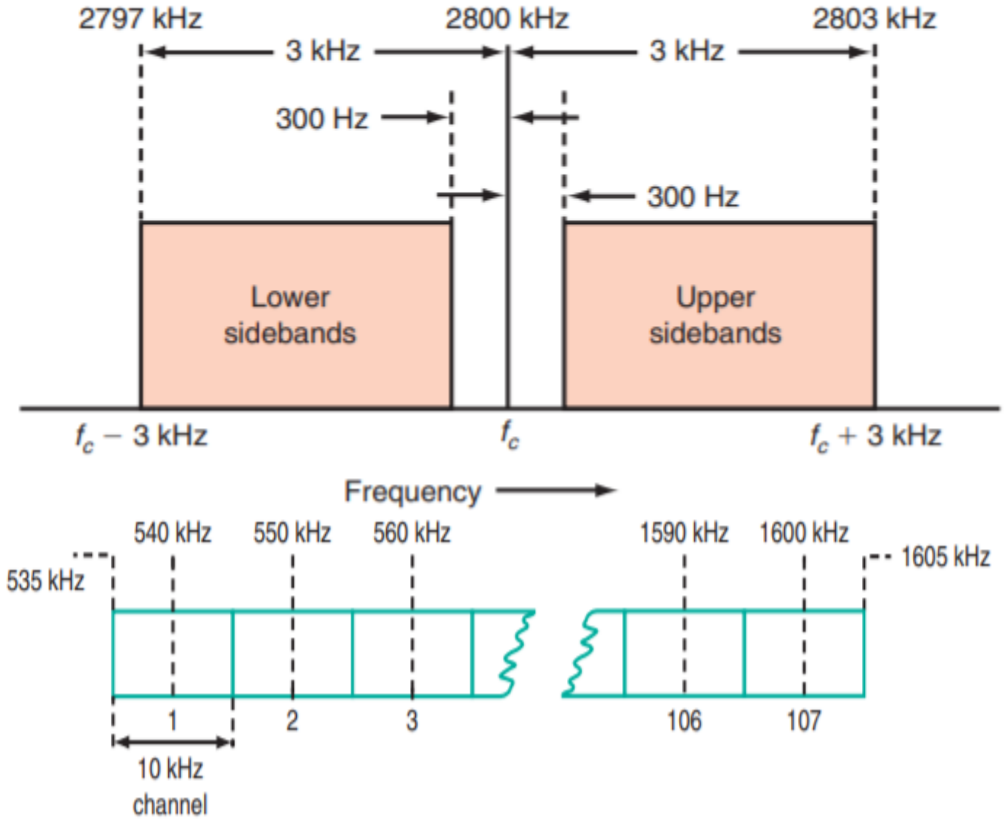
The total bandwidth is simply the difference between the upper and lower sideband frequencies:

$$BW = f_{USB} - f_{LSB} = 2803 - 2797 = 6 \text{ kHz}$$

As it turns out, the bandwidth of an AM signal is twice the highest frequency in the modulating signal: $BW = 2f_m$, where f_m is the maximum modulating frequency. In the case of a voice signal whose maximum frequency is 3 kHz, the total bandwidth is simply

$$BW = 2(3 \text{ kHz}) = 6 \text{ kHz}$$

The upper and lower sidebands of a voice modulator AM signal.



extending from 1595 up to 1605 kHz. There are a total of 107 10-kHz-wide channels for AM radio stations.

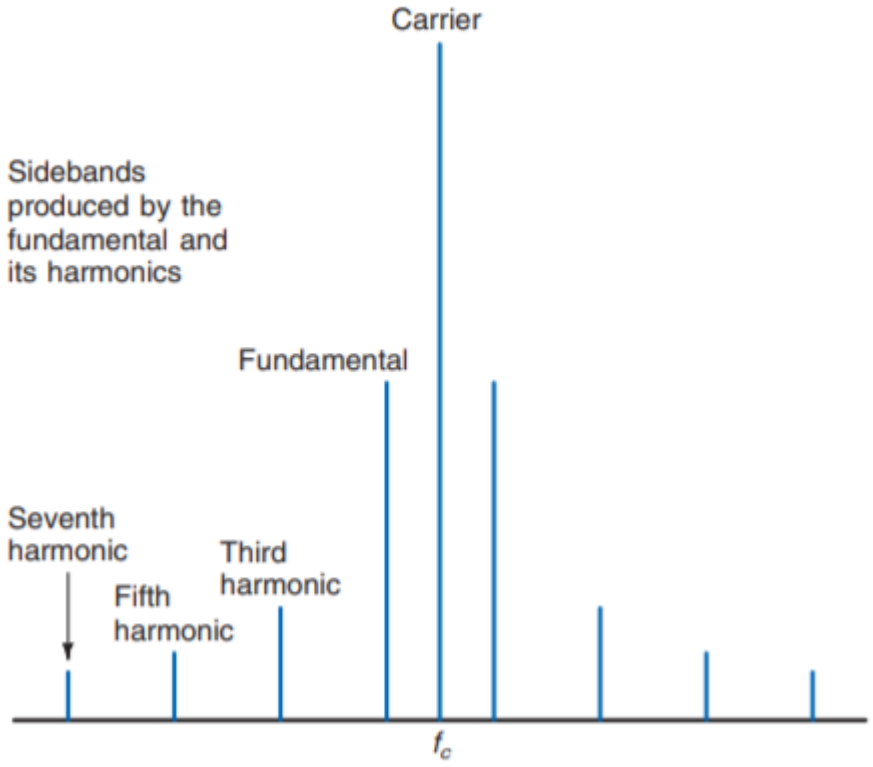
Pulse Modulation

When complex signals such as pulses or rectangular waves modulate a carrier, a broad spectrum of sidebands are produced.

In order for a square wave to be transmitted and faithfully received without distortion or degradation, all the most significant sidebands must be passed by the antennas and the transmitting and receiving circuits.

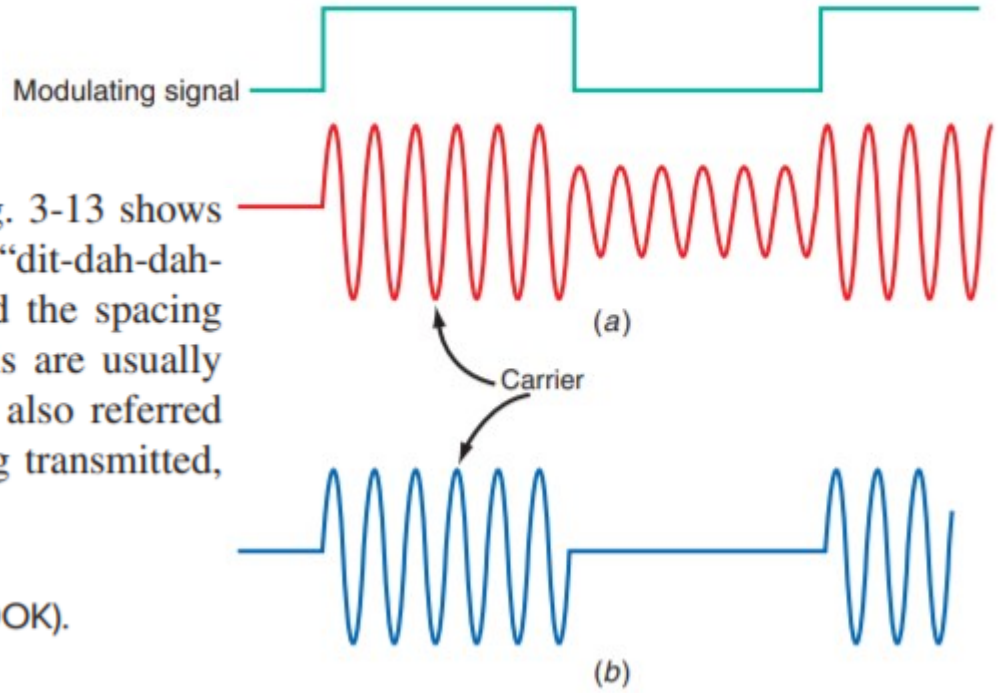
Amplitude modulation by square waves or rectangular binary pulses is referred to as *amplitude-shift keying (ASK)*. ASK is used in some types of data communication when binary information is to be transmitted.

Another crude type of amplitude modulation can be achieved by simply turning the carrier off and on. An example is the transmitting of Morse code by using dots and dashes.



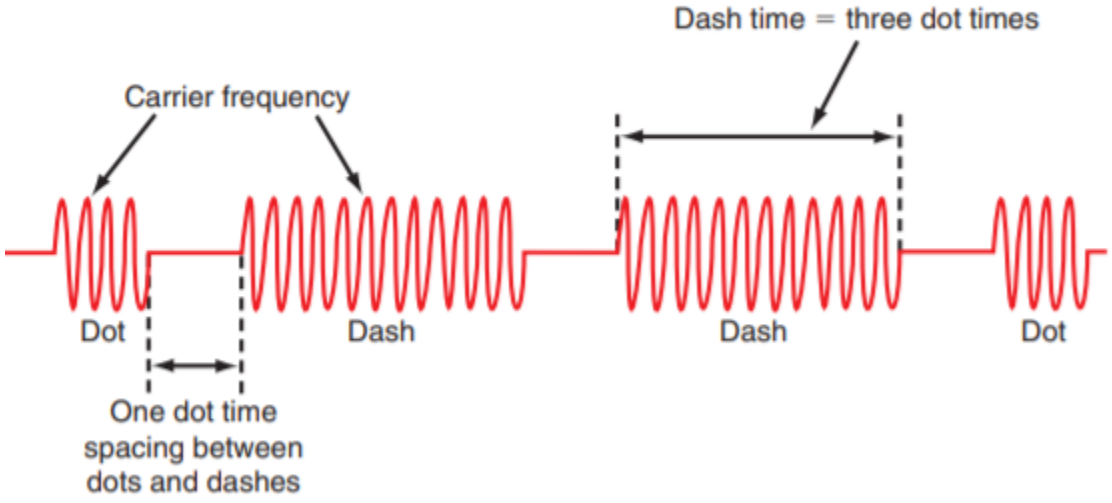
Morse Code

Amplitude modulation of a sine wave carrier by a pulse or rectangular wave is called amplitude-shift keying. (*a*) Fifty percent modulation. (*b*) One hundred percent modulation.



A dot is a short burst of carrier, and a dash is a longer burst of carrier. Fig. 3-13 shows the transmission of the letter P, which is dot-dash-dash-dot (pronounced "dit-dah-dah-dit"). The time duration of a dash is three times the length of a dot, and the spacing between dots and dashes is one dot time. Code transmissions such as this are usually called *continuous-wave (CW) transmissions.* This kind of transmission is also referred to as *ON/OFF keying (OOK).* Despite the fact that only the carrier is being transmitted,

Sending the letter P by Morse code. An example of ON/OFF keying (OOK).



AM Power

The AM signal is really a composite of several signal voltages, namely, the carrier and the two sidebands, and each of these signals produces power in the antenna. The total transmitted power P_T is simply the sum of the carrier power P_c and the power in the two sidebands P_{USB} and P_{LSB}:

$$P_T = P_c + P_{LSB} + P_{USB}$$

You can see how the power in an AM signal is distributed and calculated by going back to the original AM equation:

$$v_{AM} = V_c \sin 2\pi f_c t + \frac{V_m}{2} \cos 2\pi t (f_c - f_m) - \frac{V_m}{2} \cos 2\pi t (f_c + f_m)$$

The rms carrier and sideband voltages are then

$$v_{AM} = \frac{V_c}{\sqrt{2}} \sin 2\pi f_c t + \frac{V_m}{2\sqrt{2}} \cos 2\pi t (f_c - f_m) - \frac{V_m}{2\sqrt{2}} \cos 2\pi t (f_c + f_m)$$

$$P_T = \frac{(V_c/\sqrt{2})^2}{R} + \frac{(V_m/2\sqrt{2})^2}{R} + \frac{(V_m/2\sqrt{2})^2}{R} = \frac{V_c^2}{2R} + \frac{V_m^2}{8R} + \frac{V_m^2}{8R}$$

by using the expression given earlier for the modulation index $m = V_m/V_c$; we can write

$$V_m = mV_c$$

If we express the sideband powers in terms of the carrier power, the total power becomes

$$P_T = \frac{(V_c)^2}{2R} + \frac{(mV_c)^2}{8R} + \frac{(mV_c)^2}{8R} = \frac{V_c^2}{2R} + \frac{m^2V_c^2}{8R} + \frac{m^2V_c^2}{8R}$$

AM power

Since the term $V_c^2/2R$ is equal to the rms carrier power P_c, it can be factored out, giving

$$P_T = \frac{V_c^2}{2R}\left(1 + \frac{m^2}{4} + \frac{m^2}{4}\right)$$

Finally, we get a handy formula for computing the total power in an AM signal when the carrier power and the percentage of modulation are known:

$$P_T = P_c\left(1 + \frac{m^2}{2}\right)$$

For example, if the carrier of an AM transmitter is 1000 W and it is modulated 100 percent ($m = 1$), the total AM power is

$$P_T = 1000\left(1 + \frac{1^2}{2}\right) = 1500 \text{ W}$$

Of the total power, 1000 W of it is in the carrier. That leaves 500 W in both sidebands. Since the sidebands are equal in size, each sideband has 250 W.

AM Power

When the percentage of modulation is less than the optimum 100, there is much less power in the sidebands. For example, for a 70 percent modulated 250-W carrier, the total power in the composite AM signal is

$$P_T = 250\left(1 + \frac{0.7^2}{2}\right) = 250(1 + 0.245) = 311.25 \text{ W}$$

Of the total, 250 W is in the carrier, leaving $311.25 - 250 = 61.25$ W in the sidebands. There is 61.25/2 or 30.625 W in each sideband.

Example

An AM transmitter has a carrier power of 30 W. The percentage of modulation is 85 percent. Calculate (*a*) the total power and (*b*) the power in one sideband.

a. $P_T = P_c\left(1 + \frac{m^2}{2}\right) = 30\left[1 + \frac{(0.85)^2}{2}\right] = 30\left(1 + \frac{0.7225}{2}\right)$

$P_T = 30(1.36125) = 40.8$ W

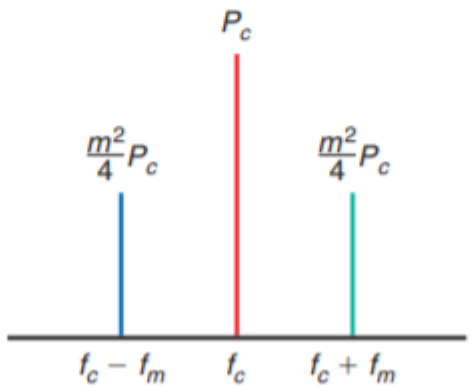
b. P_{SB} (both) $= P_T - P_c = 40.8 - 30 = 10.8$ W

P_{SB} (one) $= \frac{P_{SB}}{2} = \frac{10.8}{2} = 5.4$ W

As you can see, the power in the sidebands depends on the value of the modulation index. The greater the percentage of modulation, the higher the sideband power and the higher the total power transmitted. Of course, maximum power appears in the sidebands when the carrier is 100 percent modulated. The power in each sideband P_{SB} is given by

$$P_{SB} = P_{LSB} = P_{USB} = \frac{P_c m^2}{4}$$

An example of a time-domain display of an AM signal (power) is as follows.



The carrier itself conveys no information. The carrier can be transmitted and received, but unless modulation occurs, no information will be transmitted. When modulation occurs, sidebands are produced. It is easy to conclude, therefore, that all the transmitted information is contained within the sidebands. Only one-third of the total transmitted power is allotted to the sidebands, and the remaining two-thirds is literally wasted on the carrier.

Power Efficiency of Amplitude Modulation

Given the AM signal: $\phi_{AM}(t) = A_c \cos(\omega_c t) + m(t)\cos(\omega_c t)$

The power in the carrier is $P_c = \dfrac{A_c^2}{2}$ {Let $P_S \triangleq$ power in one sideband}

The power in the sidebands (modulated message) is

$$P_S = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} m^2(t)\cos^2(\omega_c t)dt = \frac{1}{2}\lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} m^2(t)\left[1+\cos(2\omega_c t)\right]dt$$

But $\displaystyle\int_{-T/2}^{T/2} m^2(t)\left[\cos(2\omega_c t)\right]dt = 0$, and so

we are left with $P_S = \dfrac{1}{2}\lim_{T\to\infty} \dfrac{1}{T} \displaystyle\int_{-T/2}^{T/2} m^2(t)\,dt \triangleq \frac{1}{2}P_m$

That is, P_S is one-half the total message power P_m.

In AM the power in the message (useful power) is the power in the two sidebands. Next, we define power efficiency η.

Power Efficiency in Amplitude Modulation (continued)

The power efficiency of a modulated signal is the ratio of the power in the message part of the signal relative to the total power of the modulated signal.

$$\text{Power efficiency} \quad \eta = \frac{\text{messsage power}}{\text{total power}} = \frac{\text{sideband power}}{\text{total power}}$$

$$\text{In symbols,} \quad \eta = \frac{P_S}{P_C + P_S} = \frac{\frac{1}{2}P_m}{P_C + \frac{1}{2}P_m}, \qquad \text{and} \qquad P_C = \frac{A_C^2}{2}$$

$$\therefore \boxed{\eta = \frac{P_m}{A_C^2 + P_m}}$$

Power Efficiency in Amplitude Modulation (continued)

In general, the form of P_m is complicated and not known precisely. However, we can study AM power efficiency η using a tone modulation message.

For tone modulation, $m(t) = m_p \cos(\omega_C t) = \mu A_C \cos(\omega_C t)$,

$$\therefore \quad P_m = \frac{m_p^2}{2} = \frac{(\mu A_C)^2}{2} \quad \text{and} \quad \eta = \frac{m_p^2}{2A_C^2 + m_p^2} = \frac{\mu^2}{2 + \mu^2}$$

Example: (For double-sideband with carrier is AM)

Modulation index = μ	$\eta = \frac{\mu^2}{2 + \mu^2}$
0.25	0.0303 or 3.03 %
0.5	0.111 or 11.1 %
1.0	0.333 or 33.3 %

Conclusion: AM power efficiency is very low (highly undesirable).

Power Efficiency in Amplitude Modulation (continued)

In general, the form of P_m is complicated and not known precisely. In practice, We find P_m by the integral,

$$P_m = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} m^2(t)\cdot\cos^2(\omega_C t)dt = \lim_{T\to\infty} \frac{1}{2T} \int_{-T/2}^{T/2} m^2(t)\cdot\left[1+\cos(2\omega_C t)\right]dt$$

$$P_m = \lim_{T\to\infty} \frac{1}{2T} \int_{-T/2}^{T/2} m^2(t)dt\,.$$

If $m(t)$ is a single tone, then we have

$m(t) = m_p \cdot \cos(\omega_C t)$, then

$$P_m = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} m_p^2 \cdot\cos^2(\omega_C t)dt = \lim_{T\to\infty} \frac{1}{2T} \int_{-T/2}^{T/2} m_p^2 \cdot\left[1+\cos(2\omega_C t)\right]dt$$

$$P_m = \lim_{T\to\infty} \frac{1}{2T} \int_{-T/2}^{T/2} m_p^2 dt = \frac{1}{2}\left(m_p^2\right)\left[\frac{(T/2)-(-T/2)}{T}\right] = \frac{1}{2}\left(m_p^2\right)$$

and $\quad P_S = \frac{P_m}{2} = \frac{1}{4}(m_p^2)$

Can We Reduce Transmitted Power in AM?

1. **Do we need to transmit the carrier, which is the majority of the transmitted power, in AM?**

   No, but we will need to have a more sophisticated demodulation scheme in the receiver. We will do this with "double-sideband suppressed carrier" modulation.

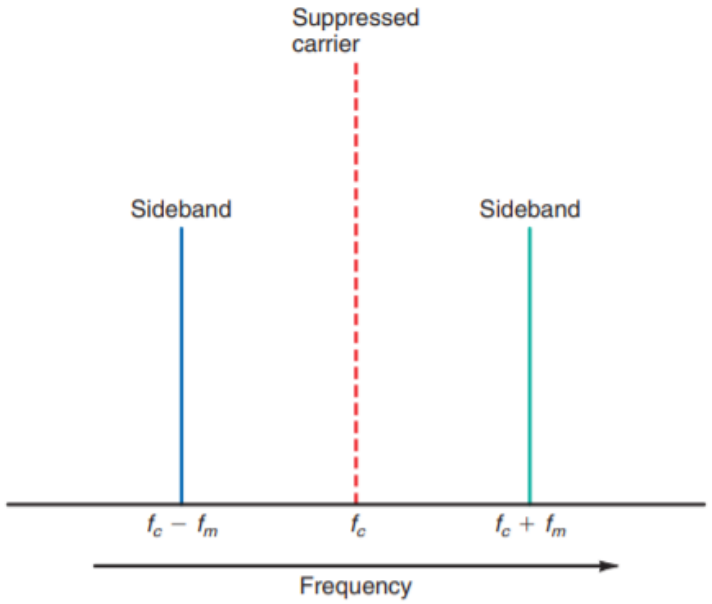
2. **Do we have to transmit both sidebands in AM?**

   No, because both sidebands contain identical information. We will do this by introducing "single-sideband modulation" (without carrier).

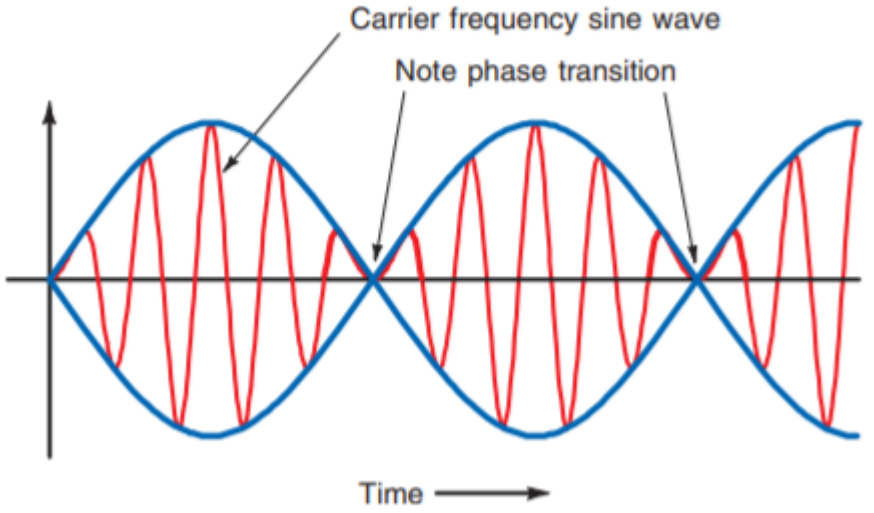
Single Side Band Modulation

One way to improve the efficiency of amplitude modulation is to suppress the carrier and eliminate one sideband. The result is a single-sideband (SSB) signal. SSB is a form of AM that offers unique benefits in some types of electronic communication.

The first step in generating an SSB signal is to suppress the carrier, leaving the upper and lower sidebands. This type of signal is referred to as a *double-sideband suppressed carrier (DSSC* or *DSB)* signal.



A time-domain display of a DSB AM signal.



Note that the envelope of this waveform is not the same as that of the modulating signal, as it is in a pure AM signal with carrier. A unique characteristic of the DSB signal is the phase transitions that occur at the lower-amplitude portions of the wave.

spectrum space occupied by a DSB signal is the same as that for a conventional AM signal.

Double-sideband suppressed carrier signals are generated by a circuit called a *balanced modulator.* The purpose of the balanced modulator is to produce the sum and difference frequencies but to cancel or balance out the carrier.

Despite the fact that elimination of the carrier in DSB AM saves considerable power, DSB is not widely used because the signal is difficult to demodulate (recover) at the receiver. One important application for DSB, however, is the transmission of the color information in a TV signal.

Why SSB?

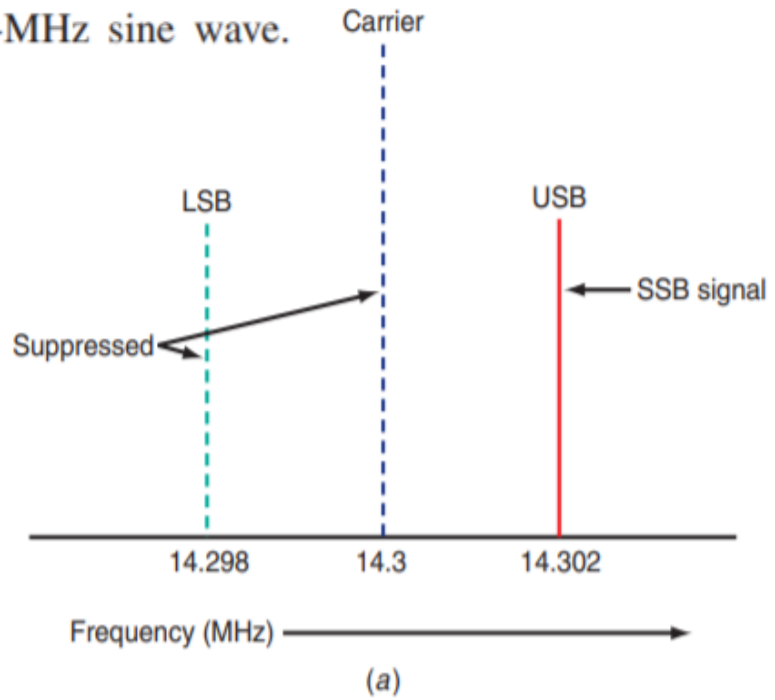
there is no reason to transmit both sidebands in order to convey the information. One sideband can be suppressed; the remaining sideband is called a *single-sideband suppressed carrier (SSSC* or *SSB)* signal. SSB signals offer four major benefits.

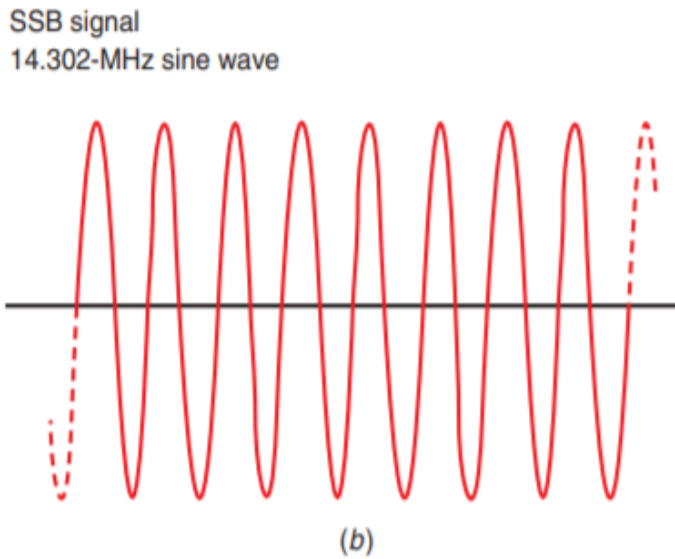
1. The primary benefit of an SSB signal is that the spectrum space it occupies is only one-half that of AM and DSB signals. This greatly conserves spectrum space and allows more signals to be transmitted in the same frequency range.
2. All the power previously devoted to the carrier and the other sideband can be channeled into the single sideband, producing a stronger signal that should carry farther and be more reliably received at greater distances. Alternatively, SSB transmitters can be made smaller and lighter than an equivalent AM or DSB transmitter because less circuitry and power are used.
3. Because SSB signals occupy a narrower bandwidth, the amount of noise in the signal is reduced.
4. There is less selective fading of an SSB signal over long distances. An AM signal is really multiple signals, at least a carrier and two sidebands. These are on different frequencies, so they are affected in slightly different ways by the ionosphere and upper atmosphere, which have a great influence on radio signals of less than about 50 MHz. The carrier and sidebands may arrive at the receiver at slightly different times, causing a phase shift that can, in turn, cause them to add in such a way as to cancel one another rather than add up to the original AM signal. Such cancellation, or *selective fading,* is not a problem with SSB since only one sideband is being transmitted.

- No Signal is transmitted if the modulation signal value is zero!

An SSB signal produced by a 2-kHz sine wave modulating a 14.3-MHz sine wave carrier.

The RF signal is simply a constant-power 14.302-MHz sine wave.





Why NOT SSB or DSB?

The main disadvantage of DSB and SSB signals is that they are harder to recover, or demodulate, at the receiver. Demodulation depends upon the carrier being present.

To solve this problem, a low-level carrier signal is sometimes transmitted along with the two sidebands in DSB or a single sideband in SSB. Because the carrier has a low power level, the essential benefits of SSB are retained

Such a low-level carrier is referred to as a *pilot carrier.* This technique is used in FM stereo transmissions as well as in the transmission of the color information in a TV picture.

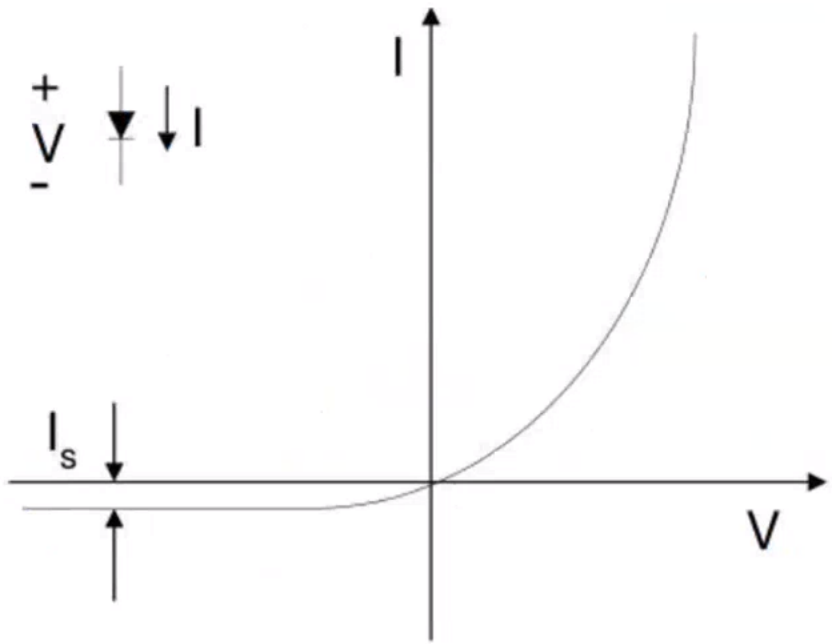
AM Modulation using Non-Linear Devices

Non-Linear Devices (NLD)

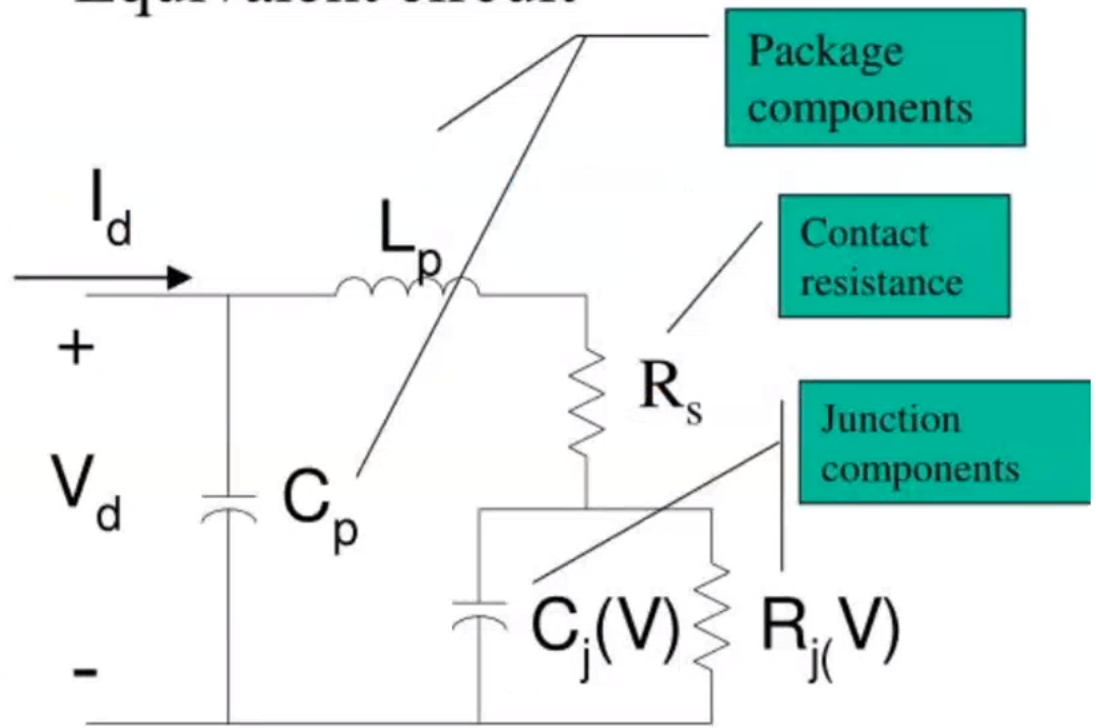
- A NLD is a device whose input-output relation is non-linear. One such example is the diode ($i_D = e^{v_D/v_T}$).
- The output of a NLD can be expressed as a power series of the input, that is
  $y(t) = ax(t) + bx^2(t) + cx^3(t) + \ldots$
- When $x(t) << 1$, the higher powers can be neglected, and the output can be approximated by the first two terms.
- When the input $x(t)$ is the sum of two signal, $m(t)+c(t)$, $x^2(t)$ will have the product term $m(t)c(t)$

Basic diode characteristic

V-I characteristic



Equivalent circuit



$$I(V) = I_s\left(e^{\alpha V} - 1\right)$$

where $\alpha = q / nkT$, q =charge, k=Boltzmann's constant, T = temperature, n = ideality factor and I_s = saturation current.

Continue

Let's say diode voltage $V = V_o + \upsilon$ where V_o is a DC bias voltage and υ is a small AC signal voltage. We expand using Taylor series

Taylor series $$f(x) = f(a) + f'(a)(x-a) + \frac{1}{2!} f''(a)(x-a)^2 + \ldots + \frac{f^{(n-1)}(a)(x-a)^{n-1}}{(n-1)!} + R_n$$

Reminder

Taking f(x) = I(V), then $x = V_o + \upsilon$ and $a = V_o$

By substituting, we have $(x-a) = (V_o + \upsilon - V_o) = \upsilon$ and the Taylor series for I(V) is

$$I(V) = I_o + \upsilon \left.\frac{dI}{dV}\right|_{V_o} + \frac{1}{2}\upsilon^2 \left.\frac{d^2 I}{dV^2}\right|_{V_o} + \ldots.$$

where $I(V) = I_s\left(e^{\alpha V} - 1\right)$ and $I_o = I(V_o) = I_s\left(e^{\alpha V_o} - 1\right)$

Continue

By substituting $I(V) = I_s\left(e^{\alpha V} - 1\right)$ and $I_o = I(V_o)$ in the first derivative

$$\left.\frac{dI}{dV}\right|_{V_o} = \alpha I_s e^{\alpha V_o} = \alpha\left(I_o + I_s\right) = G_d = \frac{1}{R_j}$$

where

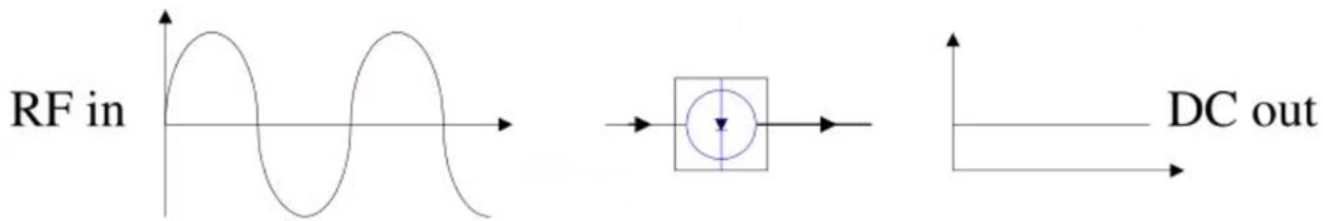
$$I_o = I(V_o) = I_s\left(e^{\alpha V_o} - 1\right)$$

Similarly in the second derivative, we have

$$\left.\frac{d^2 I}{dV^2}\right|_{V_o} = \left.\frac{dG_d}{dV}\right|_{V_o} = \alpha^2 I_s e^{\alpha V_o} = \alpha^2\left(I_o + I_s\right) = \alpha G_d = G_d^{'}$$

Then $$I(V) = I_o + \upsilon G_d + \frac{\upsilon^2}{2} G_d^{'} + \ldots$$

Rectifier application



If the diode voltage consist of DC and small RF signal $V = V_o + \upsilon_o \cos \omega_o t$ where Vo is a DC bias voltage and $\upsilon \cos \omega_o t$ is a small RF signal voltage. Then by substituting

$$I(V) = I_o + \upsilon_o G_d \cos \omega_o t + \frac{\upsilon_o^{\,2}}{2} G_d^{'} \cos^2 \omega_o t + ...$$

$$= I_o + \upsilon_o G_d \cos \omega_o t + \frac{\upsilon_o^{\,2}}{4} G_d^{'} + \frac{\upsilon_o^{\,2}}{4} G_d^{'} \cos 2\omega_o t + ...$$

continue

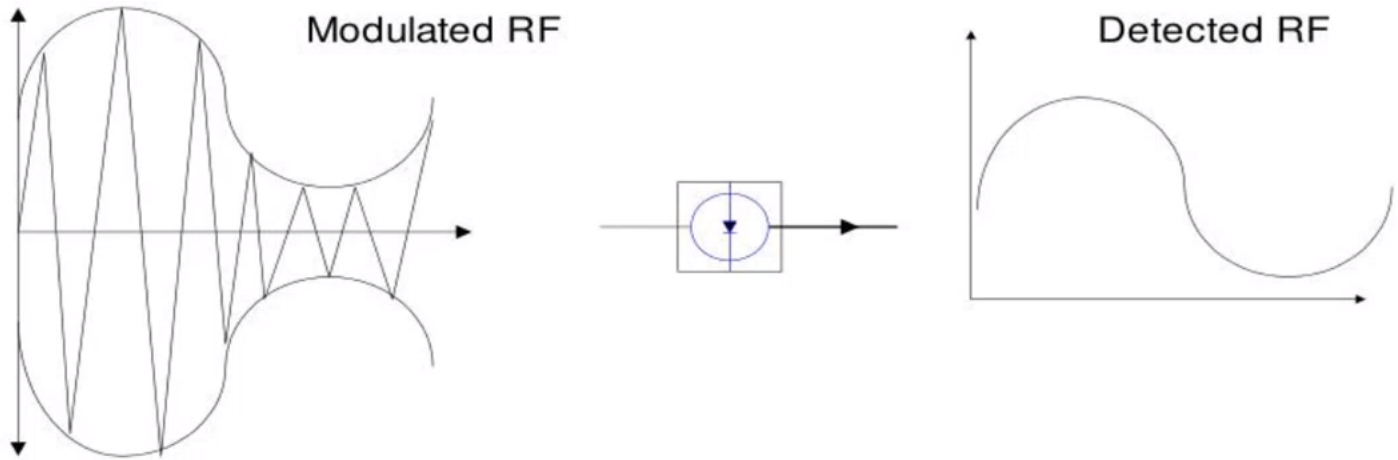
Rearrange

$$I(V) = I_o + \frac{\upsilon_o^{\,2}}{4} G_d^{'} + \upsilon_o G_d \cos\omega_o t + \frac{\upsilon_o^{\,2}}{4} G_d^{'} \cos 2\omega_o t + \ldots.$$

DC rectified current

AC harmonics current of frequency ω_o and $2\omega_o$. This can be filtered off by using lowpass filter

Detector application



Modulated signal representation

$$V = \upsilon_o\left(1 + m\cos\omega_m t\right)\cos\omega_o t$$

where

m = modulation index

ω_o= RF carrier frequency

ω_m= modulation frequency

continue

$$I(V) = I_o + \upsilon_o G_d \left(1 + m\cos\omega_m t\right)\cos\omega_o t +$$

$$\frac{\upsilon_o{}^2}{2} G_d^{'} \left(1 + m\cos\omega_m t\right)^2 \cos^2\omega_o t + \ldots.$$

$$= I_o + \upsilon_o G_d \left[\cos\omega_o t + \frac{m}{2}\cos\left(\omega_o + \omega_m\right)t + \frac{m}{2}\cos\left(\omega_o - \omega_m\right)t\right] +$$

$$\frac{\upsilon_o{}^2}{4} G_d^{'} \left[1 + \frac{m^2}{2} + 2m\cos\omega_m t + \frac{m^2}{2}\cos 2\omega_m t + \cos 2\omega_o t +\right.$$

$$+ m\cos\left(2\omega_o + \omega_m\right)t + m\cos\left(2\omega_o - \omega_m\right) + \frac{m^2}{2}\cos 2\omega_o t$$

$$\left. + \frac{m^2}{4}\cos 2\left(\omega_o + \omega_m\right)t + \frac{m^2}{4}\cos 2\left(\omega_o - \omega_m\right)t\right]$$

Trigonometry relationship

$$\sin x \sin y = \frac{1}{2}[\cos(x-y) - \cos(x+y)]$$

$$\cos x \cos y = \frac{1}{2}[\cos(x-y) + \cos(x+y)]$$

$$\sin x \cos y = \frac{1}{2}[\sin(x+y) + \sin(x-y)]$$

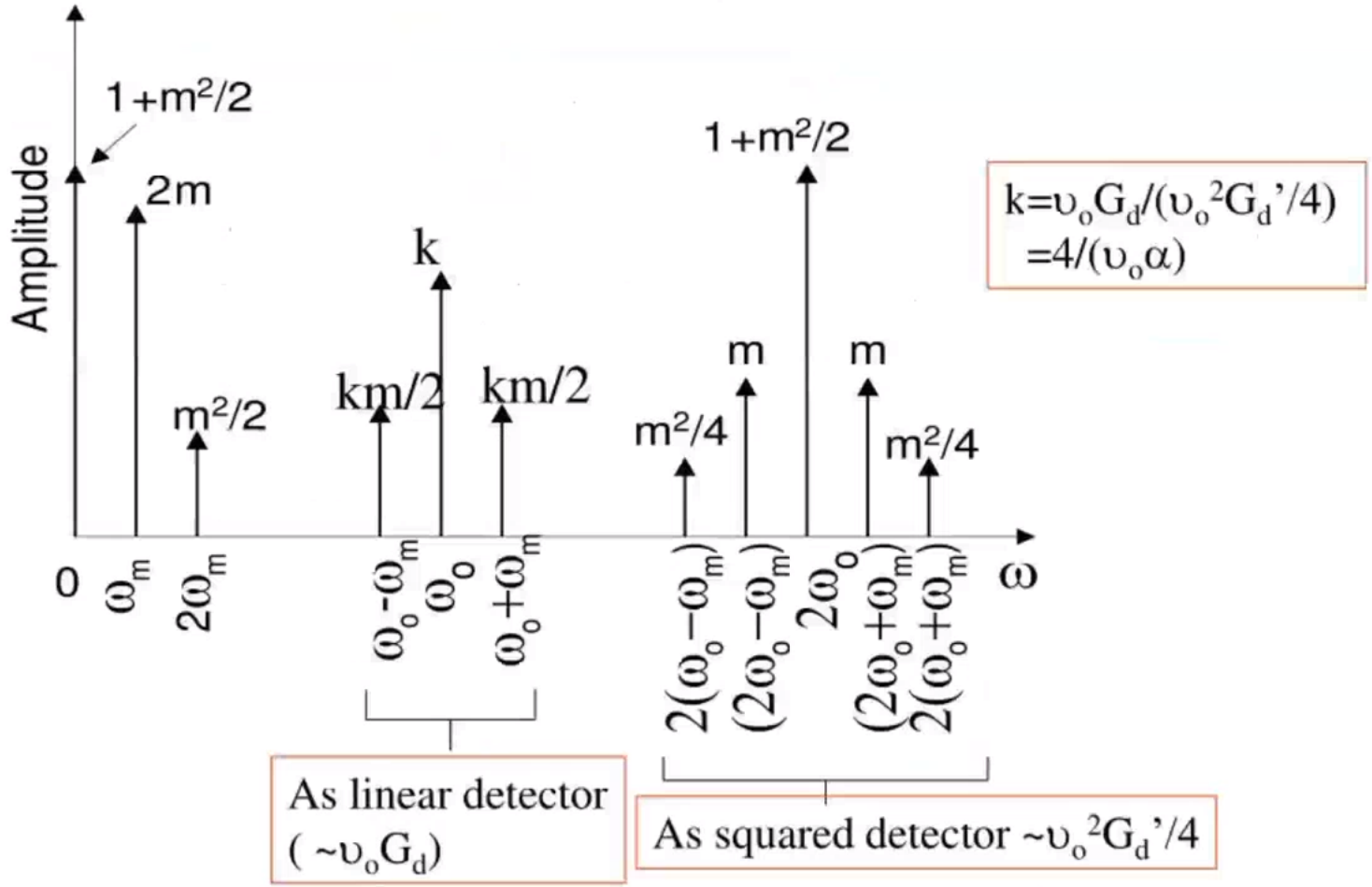
$$\cos x \sin y = \frac{1}{2}[\sin(x+y) - \sin(x-y)]$$

$$2\sin^2 x = 1 - \cos(2x)$$

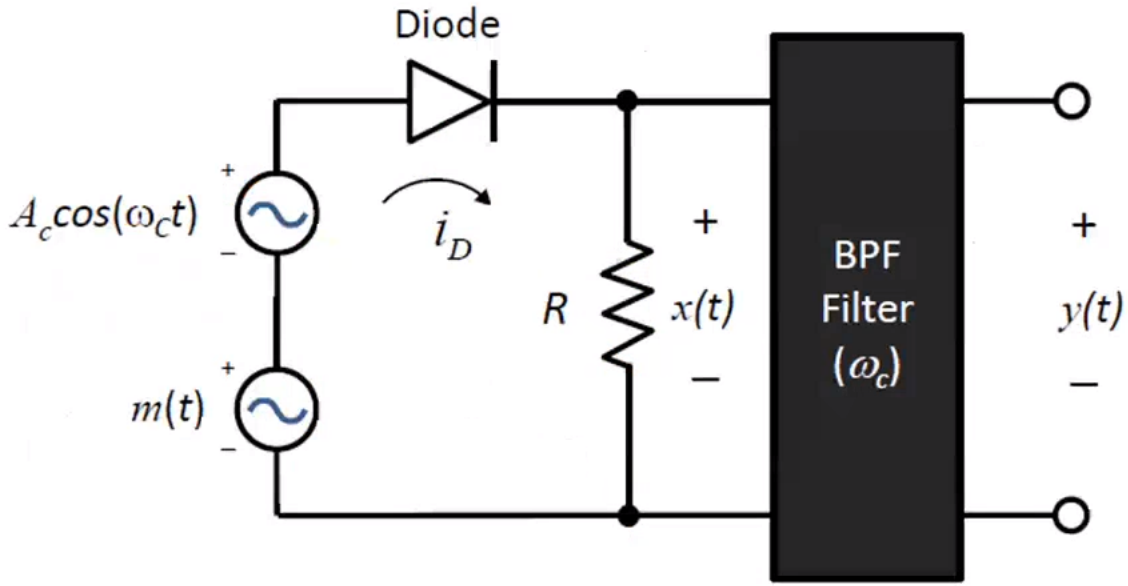
$$2\cos^2 x = 1 + \cos(2x)$$

continue

From the eq. above we have several harmonics as shown with relative amplitude.



Using Nonlinearity For Modulation (*i.e.*, AM Generation)



The diode is the nonlinear component (it has an exponential characteristic). Using a **Taylor's series** we can express the diode current i_D as (with only first two terms of the Taylor's series),

$$i_D(t) = b_1 v_D(t) + b_2 v_D^2(t); \quad v_D(t) \text{ is diode voltage.}$$

"Square Law" behavior

The voltage across resistor R is given by

$$x(t) = i_D(t)R = b_1 R v_D(t) + b_2 R v_D^2(t) = a_1 v_D(t) + a_2 v_D^2(t)$$

Amplitude Modulation Circuits

- There are two ways of modulation:
- 1) multiplying the carrier by a gain attenuation factor that varies of information signal.
- 2) linearly mix or algebraically add the carrier and modulating signal.

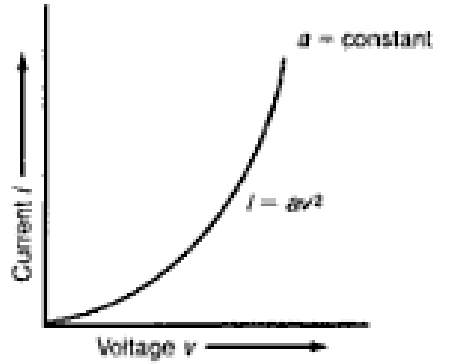
➔Analog multiplication :

$$V_{am} = V_c \sin 2\pi f_c t + (V_m \sin 2\pi f_m t)(\sin 2\pi f_c)$$

$$V_m = mV_c$$

$$V_{am} = \sin 2\pi f_c t(V_c + mV_c \sin 2\pi f_m t)$$
$$= V_c \sin 2\pi f_c t(1 + m \sin 2\pi f_m t)$$

- Non-linear Mixing:
- Carrier and modulation signal are linearly mixed
- Then resulting voltage is used to vary current in a non linear device such as : FET , Diode, and BJT (FET has a square I/V characteristic curve relation, Diodes and BJT has an exponential I/V relation which is the bases of AM)
- Square law response is the response of NLD with square I/V relation (such as FET)
- Since filters can remove the unwanted harmonies, FET (squared response) and Diodes or BJT (exponential response) can all be used alternatively as AM modulators.



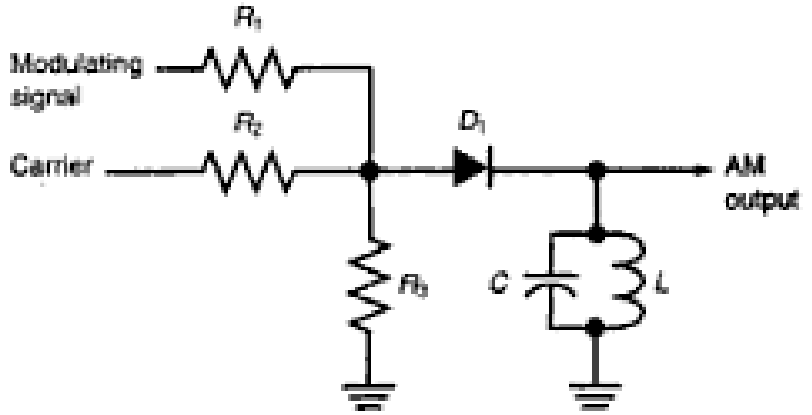
1 A square law response curve produced by a diode or appropriately biased transistor.

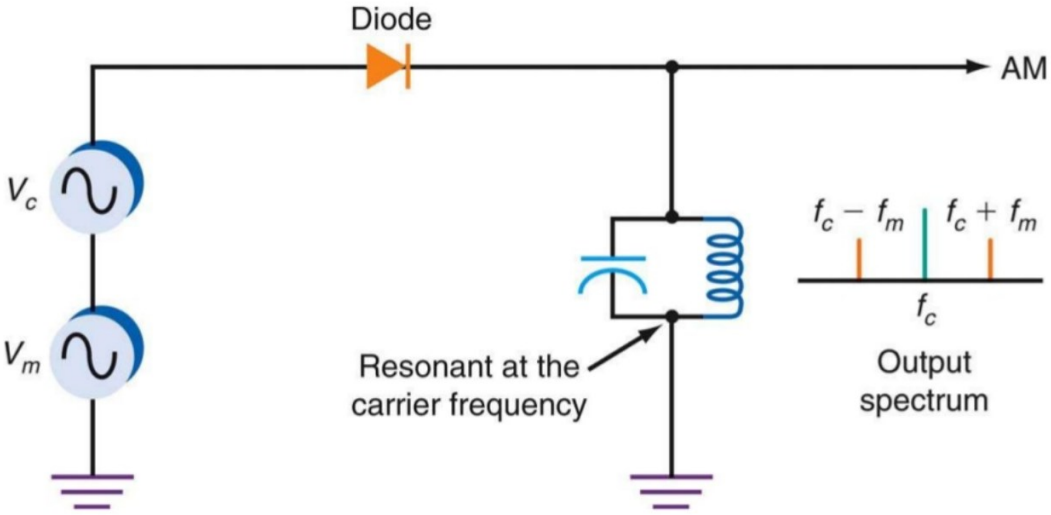
Amplitude Modulation with a Diode

- The modulating signal $A_m \cos(2\pi f_m t)$ and carrier signals $A_c \cos(2\pi f_c t)$

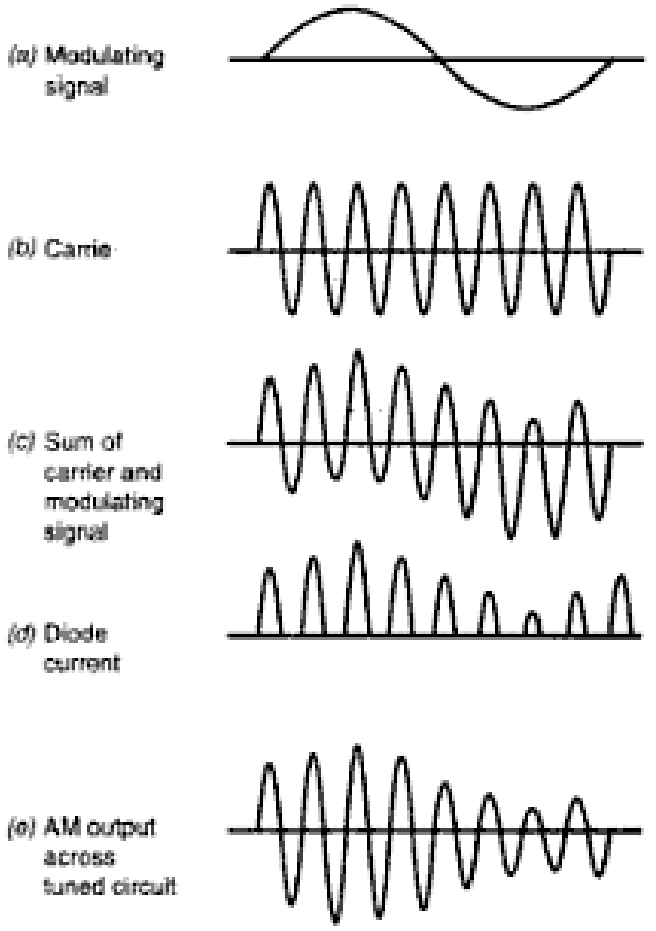
are both applied as inputs to the circuit.

- The mixing network linearly mixes the two input signals or algebraically adds them (superposition)
- The resulting signal (composite) is directly applied to the diode which will be forward during positive portions and reverse during the negative ones.
- positive pulses will be applied to the LC tuned circuit which is designed to resonate at the carrier frequency.





- Every time a current pulse is applied , C and L exchange a energy causing oscillation (or ringing) at resonant frequency.
- A negative pulse is generated for each applied positive pulse, which result in AM signal.
- Higher positive amplitudes generate higher negative counterparts and vice versa.
- Quality factor of the tuned circuit (Q) should be high enough to avoid damping (get a clear sinusoidal signal) and low enough so that the bandwidth will include sidebands around the carrier.
- Q=fr/Δ f where fr is the resonance freq. and Δ f = 2fm bandwidth.

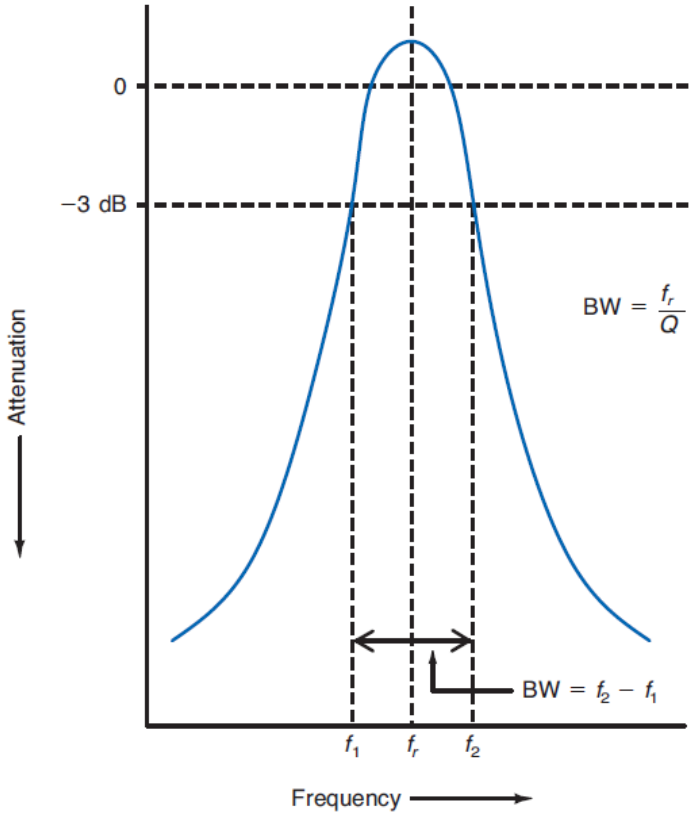


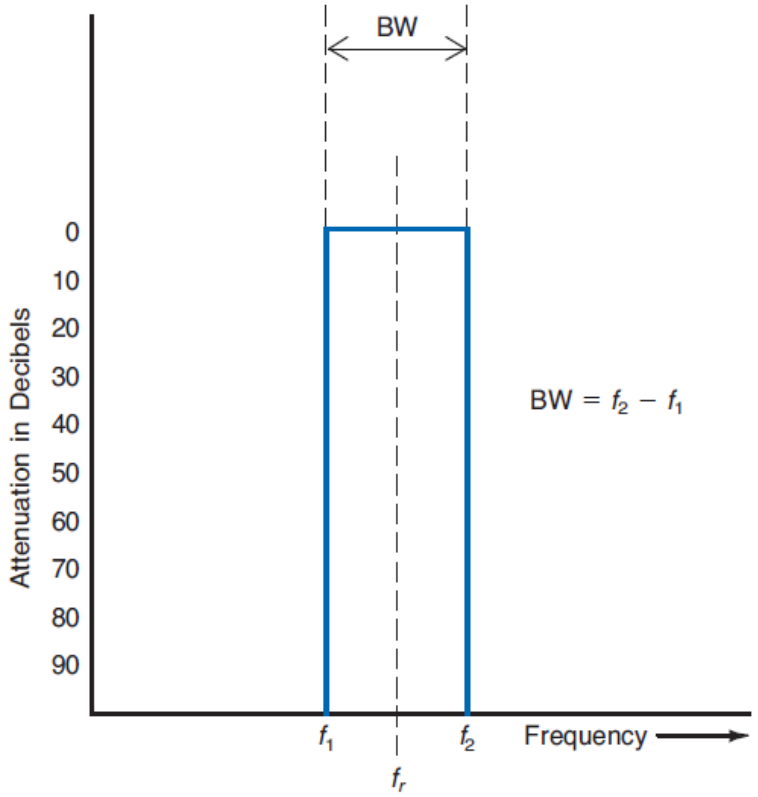
Q and Bandwidth.

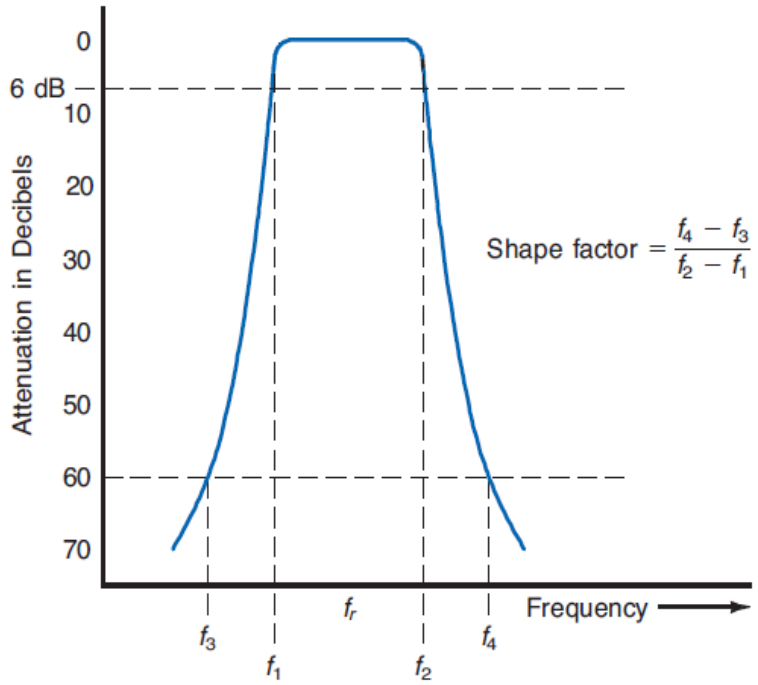
Selectivity in a receiver is obtained by using tuned circuits and/or filters. The *LC* tune circuits provide initial selectivity; filters, which are used later in the process, provide additional selectivity.

Initial selectivity in a receiver is normally obtained by using *LC* tuned circuits. By carefully controlling the *Q* of the resonant circuit, you can set the desired selectivity.

The optimum *bandwidth* is wide enough to pass the signal and its sidebands but also n enough to eliminate or greatly attenuate signals on adjacent frequencies.



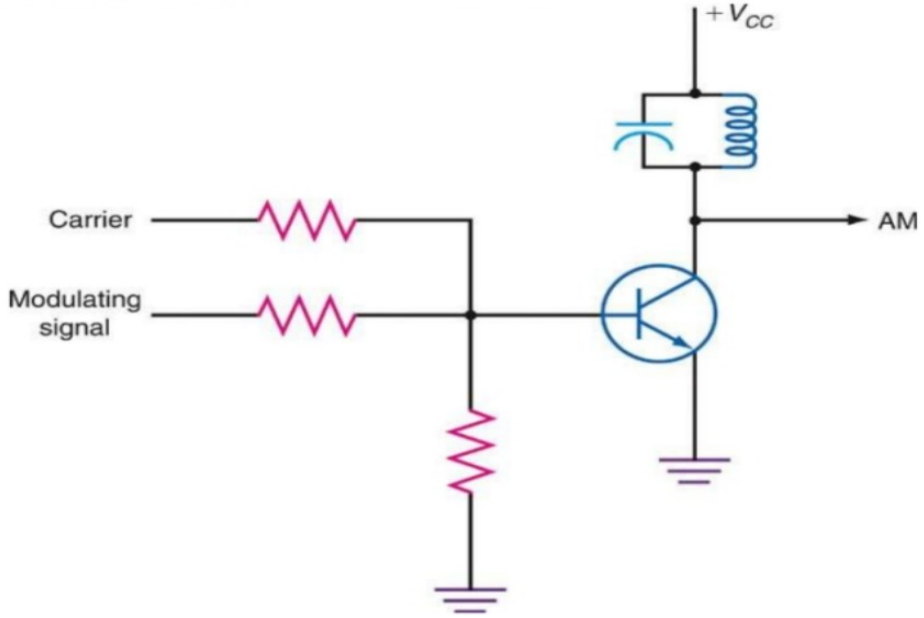


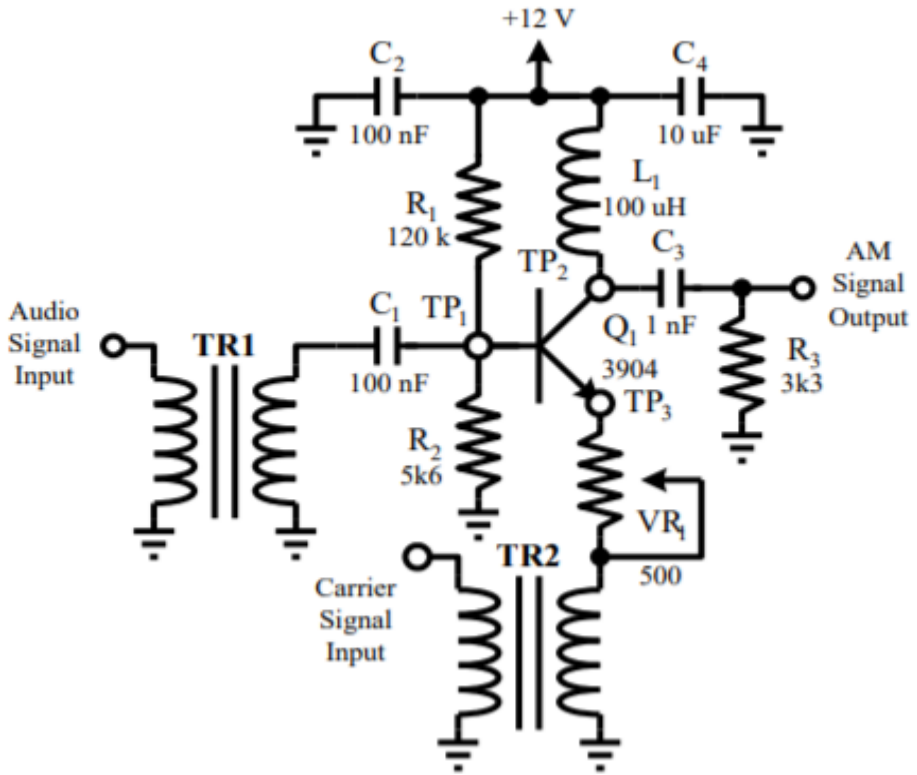


Differential Amplifier Modulator

- Transistor and diode modulator are considered d low level modulators to the low power of the output
- The audio signal (Am cos(2πfmt)) will pass through a transformer and send into the base of the transistor.
- The carrier signal (A cos(2 π fc t)) also passes through a transformer and sends into the emitter of the transistor
- These two signals will form a small amount of small signal voltage difference at the base and emitter of the transistor

$$V_{be} = V_b - V_e = A_m \cos(2\pi f_m t) - A_c \cos(2\pi f_c t)$$





$$I_c = I_s e^{V_{be}/V_T}$$

Expand by Taylor's expansion, then we get:

$$I_c = aV_{be} + bV_{be}^2$$

we notice that after the audio signal and the carrier signal input into the base and collector of the transistor, we can obtain the following signals at collector.

$$\cos^2(2\pi f_m t)\,,\quad \cos^2(2\pi f_c t)\quad \text{and}\quad \cos(2\pi f_m t)\times\cos(2\pi f_c t)$$

Then we utilize the filter to obtain the modulated AM signal

$$\cos(2\pi f_m t)\times\cos(2\pi f_c t)$$

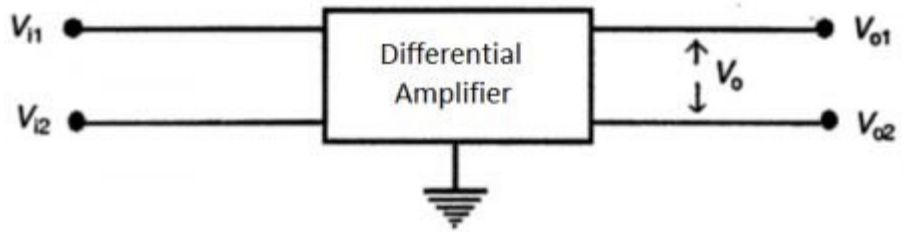
the inductor L1, capacitor C3 and resistor R3 comprise a high-pass filter, which is used to obtain the modulated AM signal

Capacitor C1 is the coupling capacitor. Capacitor C2 and C3 are the bypass capacitors. Resistors R1 and R2 are the bias resistors. Variable resistor VR1 is used to change the operation point of the transistor and it also used to control the magnitude of the carrier, which inputs into the collector of the transistor. Therefore, it can adjust the output signal waveform of the modulator.

Differential Amplifier

- As the name indicates **Differential Amplifier** is a dc-coupled amplifier that amplifies the difference between two input signals. It is the building block of analog integrated circuits and operational amplifiers (op-amp).
- One of the important feature of differential amplifier is that it tends to reject or nullify the part of input signals which is common to both inputs. This provides very good noise immunity in a lot of applications. Let's see the block diagram of a differential amplifier.
- V_{i1} and V_{i2} are input terminals and V_{o1} and V_{o2} are output terminals with respect to ground.

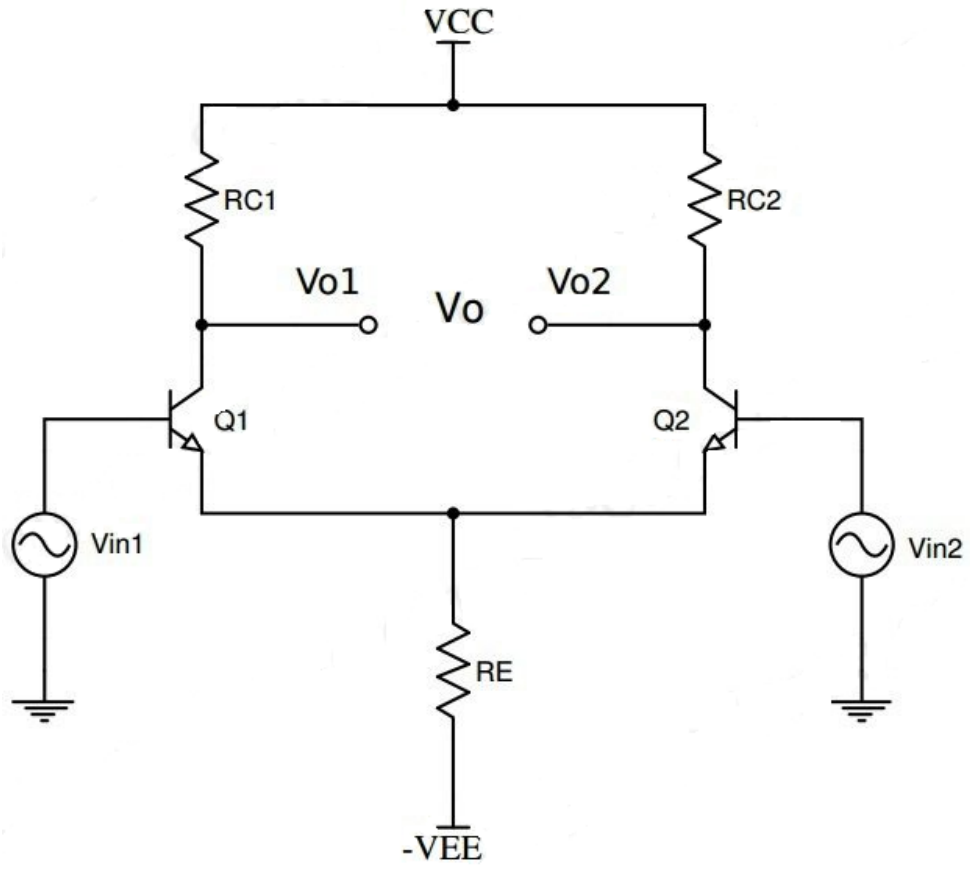
  Dual input , single input , unbalanced output, balanced output



Differential Amplifier using BJT

- The simplest form of differential amplifier can be constructed using Bipolar Junction Transistors as shown in the below circuit diagram. It is constructed using two matching transistors in common emitter configuration whose emitters are tied together.
- Based on the methods of providing input and taking output, differential amplifiers can have four different configurations as below.

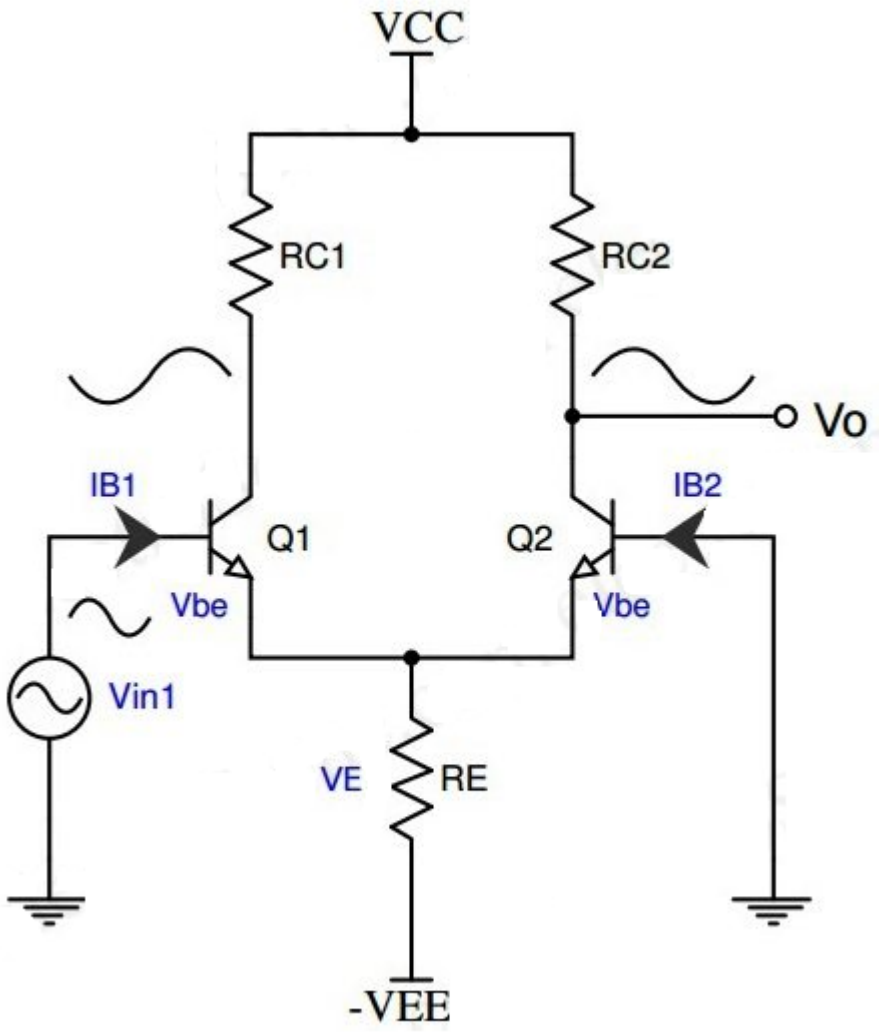
1. Single Input Unbalanced Output
2. Single Input Balanced Output
3. Dual Input Unbalanced Output
4. Dual Input Balanced Output



Single Input Unbalanced Output

- In this case, only one input signal is given and the output is taken from only one of the two collectors with respect to ground as shown below.

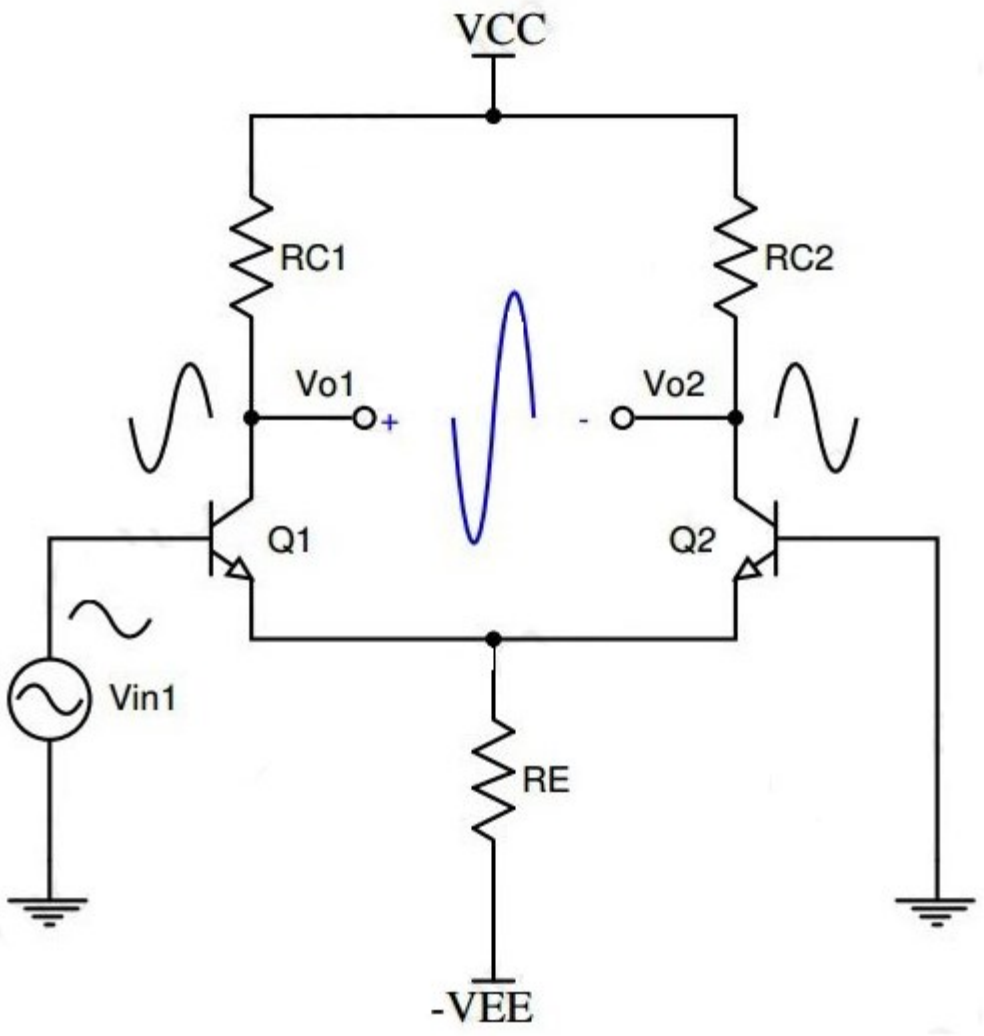
- When input signal V_{in1} is applied to the transistor Q1, it's amplified and inverted voltage gets generated at the collector of the transistor Q1. At the same time it's amplified and non-inverted voltage gets generated at the collector of the transistor Q2 as shown in the next diagram.
- The effect of input voltage V_{in1} is coupled to the transistor Q2 via the common emitter resistor R_E. You can see the proof of this in the AC Analysis section later.



Single Input Balanced Output

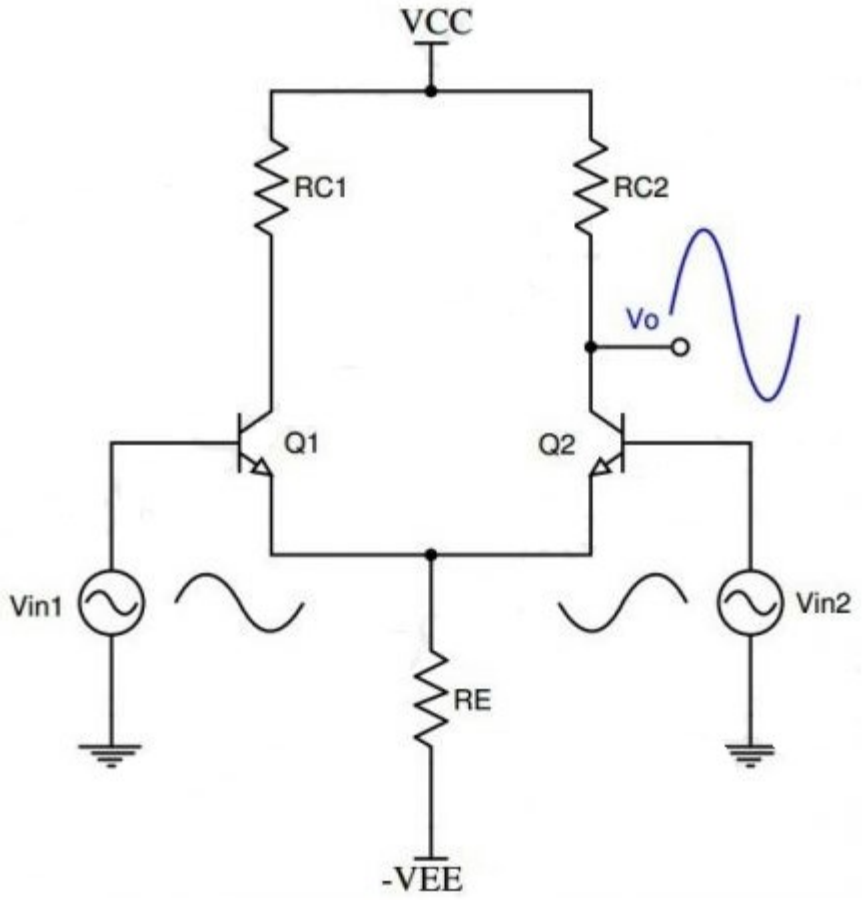
- As above only one input signal is given even though the output is taken from both collectors.
- This will give us more amplified version of o effect of both transistors. There won't be ar balanced output as the dc contents in both other.

Vo = Vo1 – Vo2



Dual Input Unbalanced Output

- Both inputs are given in this case ie, differential input but the output is taken from only one of the two collectors with respect to ground as shown below.
- Amplified version of difference in both signals will be available at the output. The voltage gain is half the gain of the dual input, balanced output differential amplifier. Unbalanced output will contain unnecessary dc content as it is a dc coupled amplifier therefore this configuration should follow by a level translator circuit.



Dual Input Balanced Output

- next circuit consists of two identical transistors Q1 and Q2 with its emitters coupled together. Collectors are connected to main supply VCC through collector resistor Rc. Magnitude of power supplies VCC and –VEE will be same.

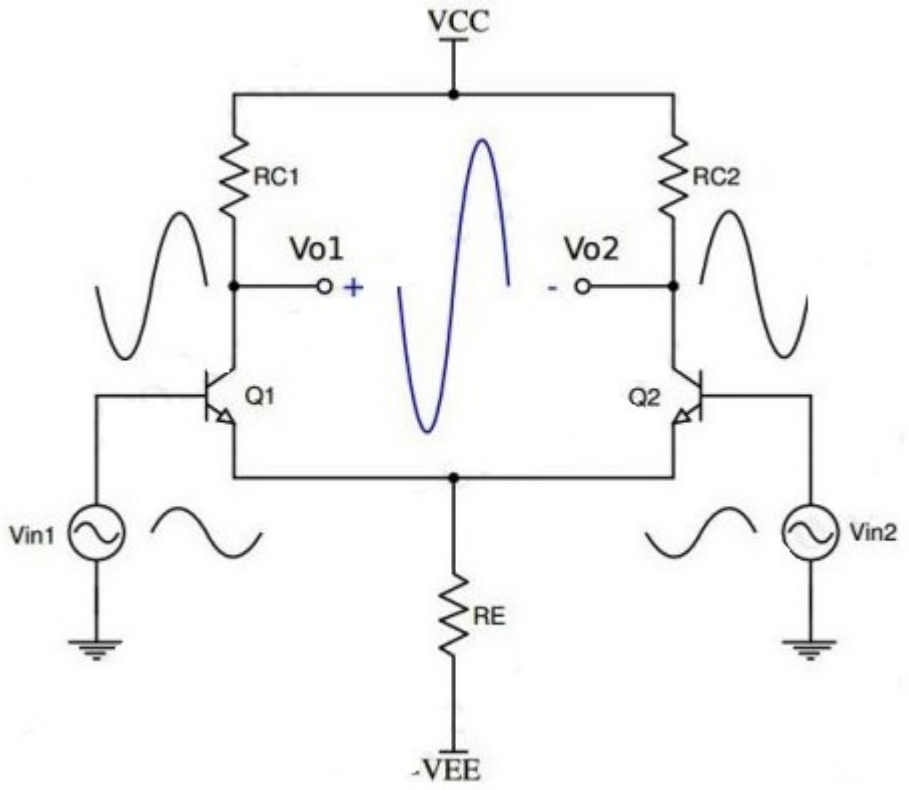
Vo = Ad($V_{in1} – V_{in2}$)

Where Ad = differential gain

V_{in1}, V_{in2} = input voltages

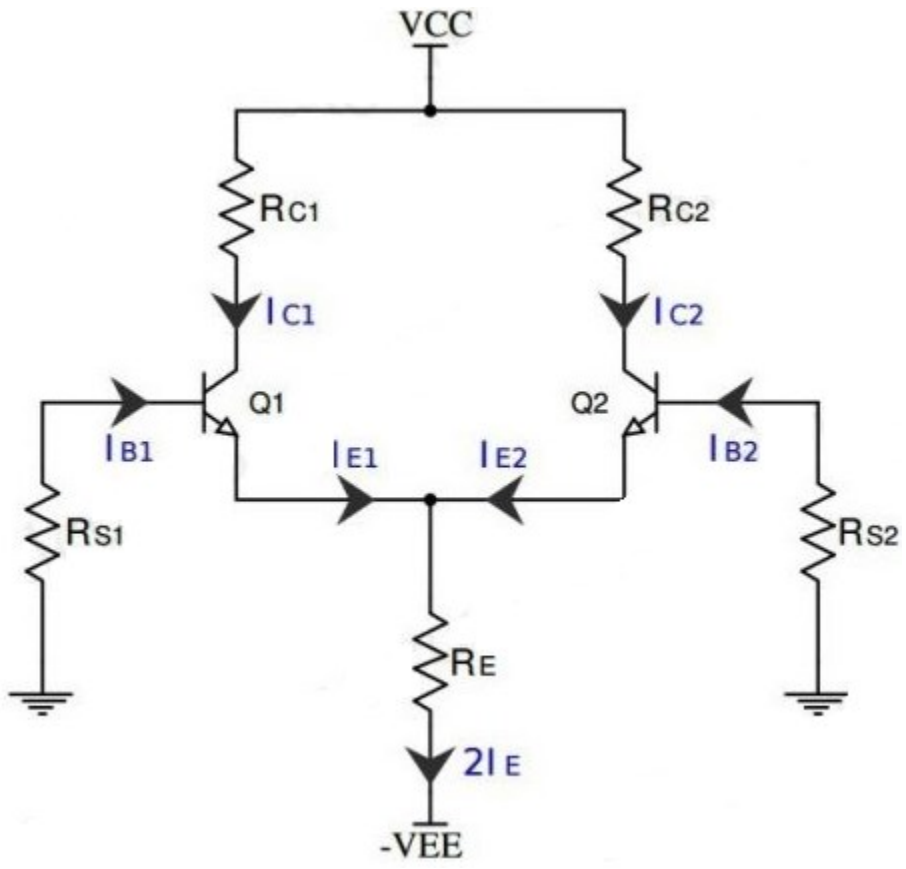
When $V_{in1} = V_{in2}$, obviously the output will be zero. ie, differential amplifier suppresses common mode signals.

For effective operation, components on either sides should be match properly. Input signals are applied at base of each transistor and output is taken from both collector terminals. There won't be any unnecessary dc content in balanced output as the dc contents in both outputs gets canceled each other.



DC Analysis

- DC analysis provides the operating point values I_{CQ} and V_{CEQ} for the transistors used in the circuit. The DC equivalent circuit obtained by reducing all AC signals to zero as shown in figure below.



Assume :

Source Resistance, $R_{S1} = R_{S2} = R_S$

Q1 = Q2

$R_{E1} = R_{E2}$ hence $R_E = R_{E1} || R_{E2}$

$R_{C1} = R_{C2} = R_C$

|VCC|=|VEE|

Applying KVL to base – emitter loop of Q1,

$-I_B R_S - V_{BE} - 2I_E R_E + VEE = 0$ ——————————-(1)

Since $I_C = \beta I_B$ and $I_C \approx I_E$

$I_B \approx I_E/\beta$ ——————————-(2)

Substituting (2) in (1) :

$-I_E R_S/\beta - V_{BE} - 2I_E R_E + VEE = 0$

$-I_E(R_S/\beta - 2R_E) + VEE - V_{BE} = 0$; Where $V_{BE} = 0.7V$ for silicon and $0.2V$ for germanium.

Also $R_S/\beta << 2R_E$

Therefore,

$$I_E = (V_{EE} - V_{BE})/2R_E \quad \text{——————————(3)}$$

Eqn.(3) =>

R_E determines the emitter current of Q1 and Q2

I_E is independent of R_C

Since the voltage drop across R_S is too small, we can neglect it. So,

$$V_E = -V_{BE}$$

$$V_C = VCC - I_C R_C$$

$$V_{CE} = V_C - V_E = (V_{CC} - I_C R_C) - (-V_{BE}) = VCC + V_{BE} - I_C R_C \quad \text{——————-(4)}$$

We can determine operating point values using equations (3) and (4). Since two transistors are identical, same equations can be used for both.

$$I_E = I_C = (V_{EE} - V_{BE})/2R_E$$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C$$

AC Analysis

- We can find **Voltage Gain Ad** and **Input Resistance Ri** of the differential amplifier by doing AC Analysis. The ac equivalent circuit is obtained by reducing all DC voltage sources to zero and replacing transistor with its equivalent.

Since both **dc emitter currents** are equal resistances $r_{e1}' = r_{e2}' = r_e'$

Applying KVL in loop 1 and 2,

$V_{in1} = R_{S1} i_{b1} + i_{e1} r_e' + (i_{e1} + i_{e2}) R_E$

$V_{in2} = R_{S2} i_{b2} + i_{e2} r_e' + (i_{e1} + i_{e2}) R_E$

We know that,

$i_{b1} \approx i_{e1}/\beta$ and $i_{b2} \approx i_{e2}/\beta$

Thus,

$V_{in1} = (R_{S1}/\beta)\, i_{e1} + i_{e1} r_e' + (i_{e1} + i_{e2})\, R_E$

$V_{in2} = (R_{S2}/\beta)\, i_{e2} + i_{e2} r_e' + (i_{e1} + i_{e2}) R_E$

Consider $\boldsymbol{R_{S1}/\beta}$ & $\boldsymbol{R_{S2}/\beta} << \boldsymbol{R_E}$ & $\boldsymbol{r_e'}$

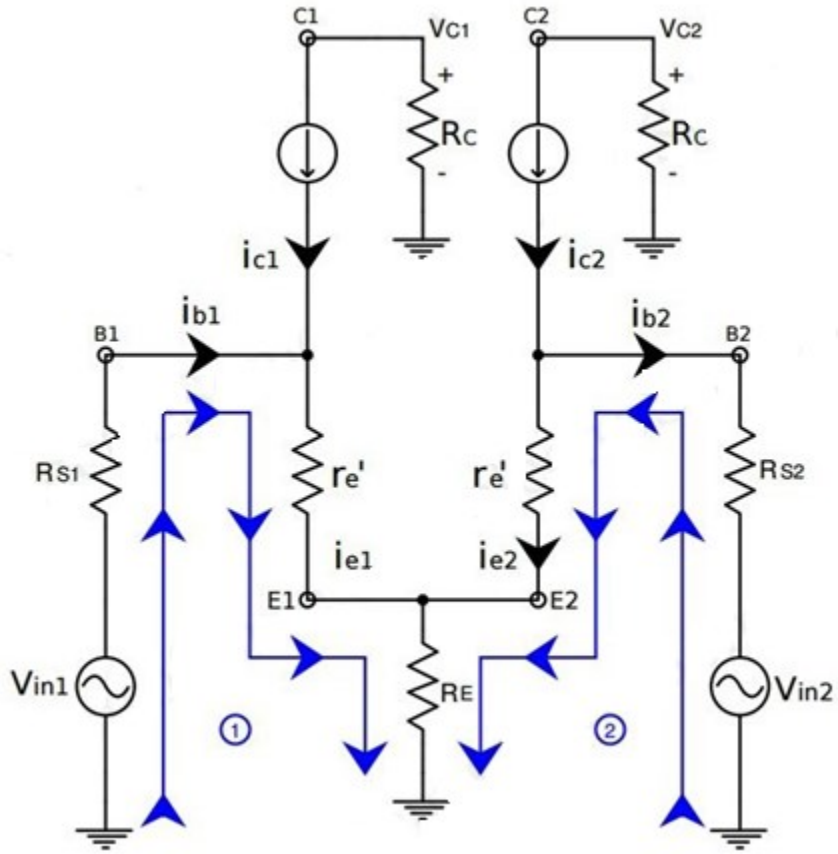
$V_{in1} = i_{e1} (r_e' + R_E) + i_{e2} R_E$

$V_{in2} = i_{e2} (r_e' + R_E) + i_{e1} R_E$

On solving these equations we get,

$i_{e1} = (V_{in1}(r_e' + R_E) - V_{in2} R_E)/((r_e' + R_E)^2 - R_E^2)$ ——————(5)

$i_{e2} = (V_{in2}(r_e' + R_E) - V_{in1} R_E)/((r_e' + R_E)^2 - R_E^2)$ ——————(6)



Voltage Gain

Output voltage, *Vo* $= V_{C2} - V_{C1}$

$= -R_C i_{c2} - (-R_C i_{c1})$
$= Rc(i_{c1} - i_{c2})$
$\Rightarrow Rc(i_{e1} - i_{e2})$ ————————(7)

On substituting (5) and (6) in (7) and solving

$Vo = (Rc(V_{in1} - V_{in2})(r_e' - 2R_E))/(r_e'(r_e' + 2R_E))$

$\boldsymbol{Vo = (R_C/r_e')(V_{in1} - V_{in2})}$ ————————————(8)

Thus the differential gain, $\boldsymbol{Ad = R_C/r_e'}$

This proves a differential amplifier amplifies the difference between two input signals.

Differential Input Resistance

Differential Input Resistance is the equivalent resistance measured across either of input terminals and ground. Thus to find out R_{i1}, V_{in2} should be grounded and to measure R_{i2}, V_{in1} should be grounded.

$\mathbf{R_{i1}}$ $= V_{in1}/i_{b1}$ when $V_{in2} = 0$

$= V_{in1}/(i_{e1}/\beta)$

Substituting equation (5) of i_{e1}

$\mathbf{R_{i1}}$ $= (V_{in1}\beta)/((V_{in1}(r_e' + R_E) - V_{in2}R_E)/((r_e' + R_E)^2 - R_E^2))$

$= \beta/((r_e' + R_E)/(r_e'^2 + 2r_e'R_E)$

$= \beta r_e'(r_e' + 2R_E)/(r_e' + R_E)$

$R_E >> r_e'$
$r_e' + 2R_E \approx 2R_E$
$r_e' + R_E \approx R_E$

$\mathbf{R_{i1}}$ $= 2\beta r_e'$

- $\mathbf{R_{i1} = 2\beta r_e'}$

Similarly,

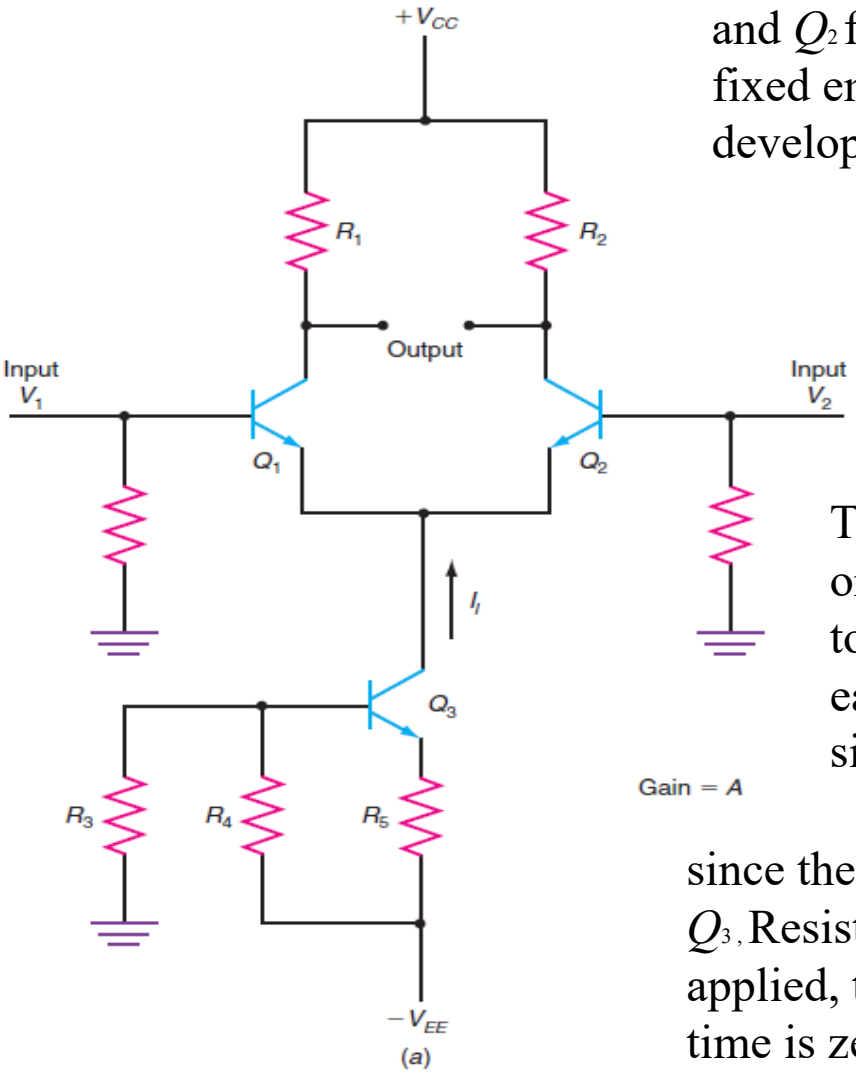
- $\mathbf{R_{i2} = 2\beta r_e'}$

Output resistance

The effective resistance measured at output terminal with respect to ground. So the output resistance is measured between the collector and the ground, which is same as the collector resistance R_C.

- $\mathbf{R_{O1} = R_{O2} = R_C}$

Differential Transistor as AM modulator



A *differential amplifier modulator* makes an excellent amplitude modulator. Transistors Q_1 and Q_2 form the differential pair, and Q_3 is a constant-current source. Transistor Q_3 supplies a fixed emitter current I_E to Q_1 and Q_2, one-half of which flows in each transistor. The output is developed across the collector resistors R_1 and R_2.

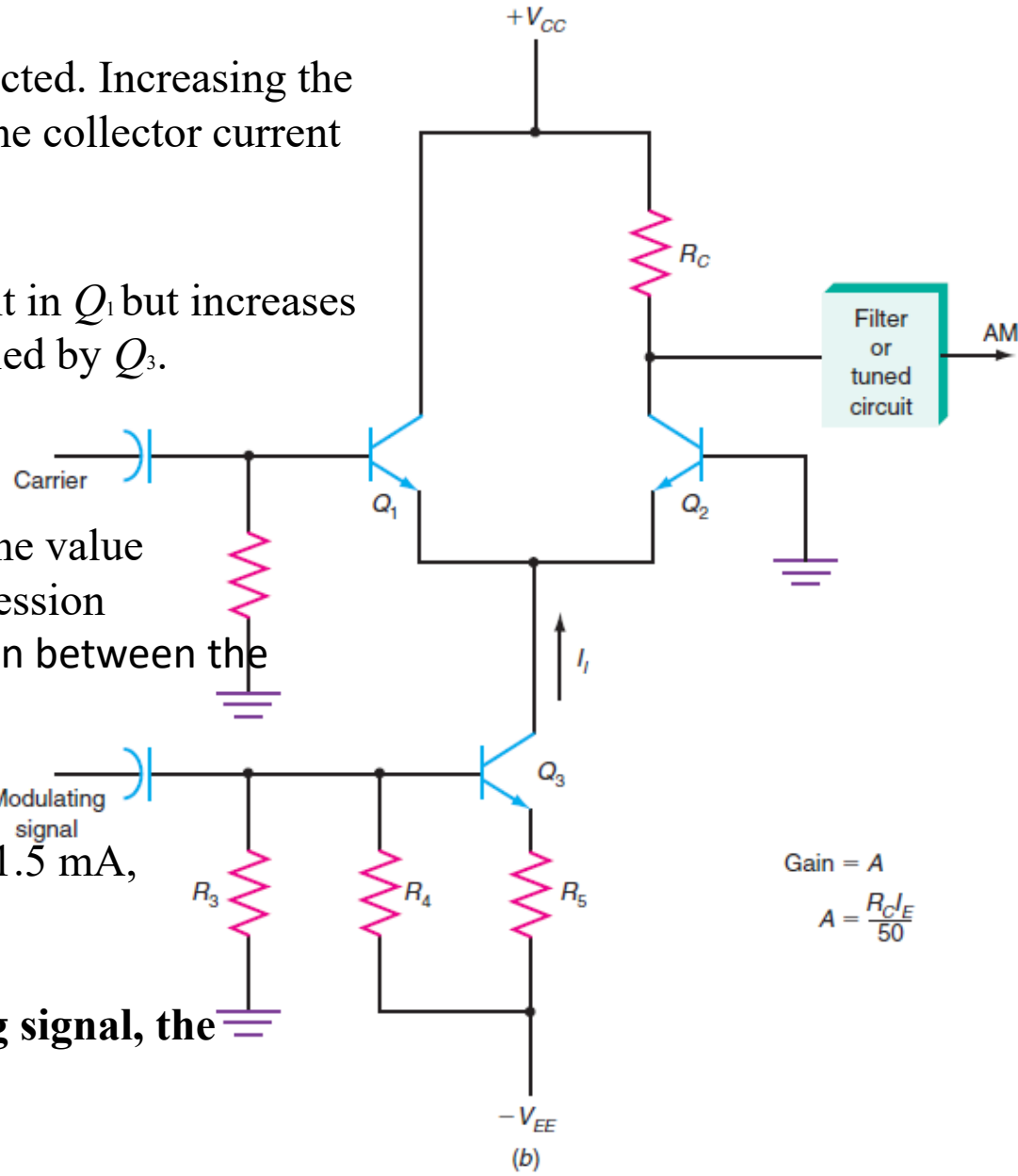
The output is a function of the difference between inputs V_1 and V_2; that is, $\boldsymbol{V_{out} = A(V_2 - V_1)}$. The amplifier can also be operated with a single input. When this is done, the other input is grounded or set to zero. if V_1 is zero, the output is $V_{out} = A(V_2)$. If V_2 is zero, the output is $V_{out} = A(-V_1) = -AV_1$. This means that the circuit inverts V_1.

The output voltage can be taken between the two collectors, producing a *balanced,* or *differential,* output. The output can also be taken from the output of either collector to ground, producing a single-ended output. The two outputs are 180° out of phase with each other. If the balanced output is used, the output voltage across the load is twice the single-ended output voltage.

since the correct value of collector current is supplied directly by the constant-current source Q_3, Resistors R_3, R_4, and R_5, along with V_{EE}, bias the constant-current source Q_3. With no inputs applied, the current in Q_1 equals the current in Q_2, which is $I_E/2$. The balanced output at this time is zero. When no inputs are applied, R_1 equals R_2, and Q_1 and Q_2 conduct equally. Therefore, the bridge is balanced and the output between the collectors is zero.

Now, if an input signal V_1 is applied to Q_1, the conduction of Q_1 and Q_2 is affected. Increasing the voltage at the base of Q_1 increases the collector current in Q_1 and decreases the collector current in Q_2 by an equal amount, so that the two currents sum to I_E.

Decreasing the input voltage on the base of Q_1 decreases the collector current in Q_1 but increases it in Q_2. The sum of the emitter currents is always equal to the current supplied by Q_3.



The gain of a differential amplifier is a function of the emitter current and the value of the collector resistors. An approximation of the gain is given by the expression $A = R_C I_E/\mathrm{K}$. $(10<\mathrm{K}<100)$ This is the single-ended gain. If the output is taken between the collectors, the gain is two times the above value.**(Prove this HW!!)**

Example : Resistor R_C is the collector resistor value in ohms, and I_E is the emitter current in milliamperes. if K=50, If $R_C = R_1 = R_2 = 4.7$ kV and $I_E = 1.5$ mA, the gain will be about $A = 4700(1.5)/50 = 7050/50 = 141$.

If the emitter current can be varied in accordance with the modulating signal, the circuit will produce AM.

Differential Amplifiers as modulators have high gain , good linearity and can be 100% modulated

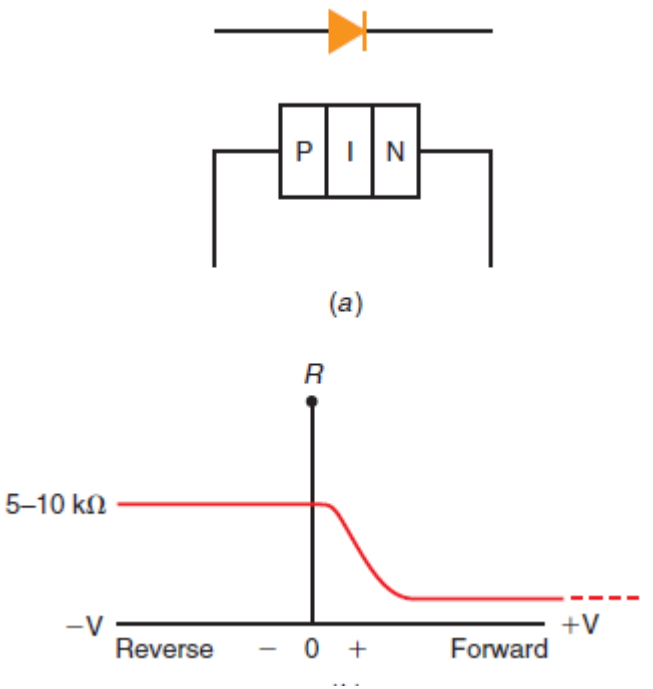
PIN Diode

A *PIN diode* is a special PN-junction diode with an I (intrinsic) layer between the P and N sections. The P and N layers are usually silicon. In practice, the I layer is a very lightly doped N-type semiconductor.

At frequencies less than about 100 MHz, the PIN diode acts just like any other PN junction diode. At higher frequencies, it acts like a variable resistor or like a switch.

When the bias is zero or reverse, the diode acts like a high value of resistance, 5k V and higher.

If a forward bias is applied, the diode resistance drops to a very low level, typically a few ohms or less. When the amount of forward bias is varied, the value of the resistance can be varied over a linear range.



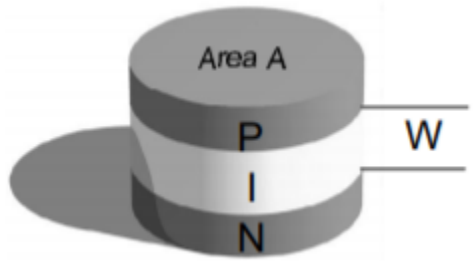
Forward Biasing PIN

When a PIN diode is forward biased, holes and electrons are injected from the P and N regions into the I-region. These charges do not recombine immediately. Instead, a finite quantity of charge always remains stored and results in a lowering of the resistivity of the I-region. The quantity of stored charge, Q, depends on the recombination time, τ (the carrier lifetime), and the forward bias current, I_F, as follows (Equation 1):

$$Q = I_F \tau \qquad [Coulombs]$$

The resistance of the I-region under forward bias, R_S is inversely proportional to Q and may be expressed as (Equation 2):

$$R_S = \frac{W^2}{(\mu_N + \mu_p)\, Q} \qquad [Ohms]$$



where: W = I-region width
μ_N = electron mobility
μ_p = hole mobility

Combining equations 1 and 2, the expression for R_S as an inverse function of current is shown as (Equation 3):

$$R_S = \frac{W^2}{(\mu_N + \mu p)\, \tau\, I_F} \qquad [Ohms]$$

At dc and very low frequencies, the PIN diode is similar to a PN diode; the diode resistance is described by the dynamic resistance of the I-V characteristics at any quiescent bias point. The dc dynamic resistance point is not, however, valid in PIN diodes at frequencies above which the period is shorter than the transit time of the I-region. The frequency at which this occurs, f_T, is called transit time frequency and may be considered the lower frequency limit for which Equatior 3 applies. This lower frequency limit is primarily a function of W, the I-region thickness and can be expressed as (Equation 4):

$$f_\tau = \frac{1300}{W^2} \qquad [MHz]$$

where W is the I-region thickness in microns. For Microsemi PIN diodes, this low frequency limit ranges from approximately 5 KHz for the thickest diodes (UM2100 and UM2300 series) to approximately 1 MHz for the thinnest diodes (UM6200, UM7200).

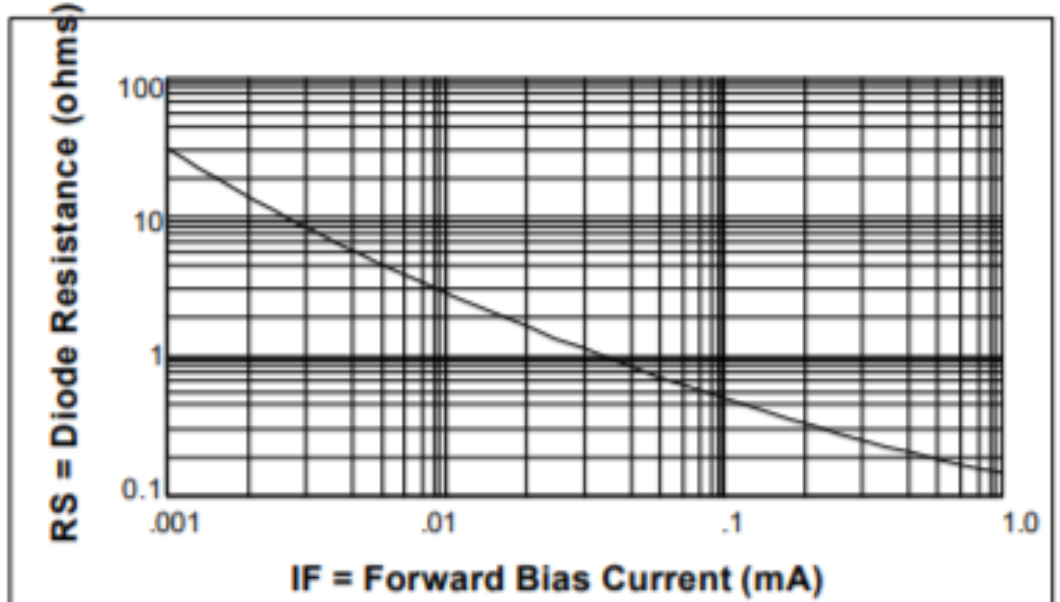


Figure 2

R_S vs Forward Current (UM4000 PIN Diode)

Reverse Biased PIN Diodes

IN diode

At high RF frequencies when a PIN diode is at zero or reverse bias, it appears as a parallel plate capacitor essentially independent of reverse voltage, having a value of (Equation #5):

$$C = \frac{\varepsilon A}{W} \qquad [Farads]$$

where: ε = silicon dielectric constant
A = junction area
W = I-region thickness

The lowest frequencies at which this effect begins to predominate is related to the dielectric relaxation frequency of the I-region, f_τ, which may be computed as (Equation #6):

$$f_\tau = \frac{I}{2\pi\rho\varepsilon} \qquad [Hz]$$

where: ρ = I-region resistivity

For Microsemi PIN diodes, this dielectric relaxation frequency occurs below 20 MHz and the total packaged capacitance, C_T, is specified for most Microsemi diodes when zero biased at 100 MHz. Additional data is supplied in the form of typical curves showing the capacitance variation as a function of reverse bias at lower frequencies.

Layer Name	Thickness (Nm)	Doping Concentration Set 1 (Cm^{-3})	Doping Concentration Set 2 (Cm^{-3})	Doping Concentration Set 3 (Cm^{-3})
P+	80	10^{18}	10^{20}	10^{22}
P-	70	$3x10^{16}$	$3x10^{18}$	$3x10^{20}$
I	600	-	-	-
N+	300	10^{18}	10^{20}	10^{22}

PIN diode Modulator

- Considered as a low level category of modulators and mainly used for Microwave , UHF and VHF frequency bands.

➔When forward biased, intrinsic layer (i) is overloaded with carriers , current crosses depletion region which in this case is the intrinsic layer.

➔Diode performs like regular diode when a low frequency signal is used to bias it. That is it has the same I/V characteristic curve. (enough time to remove the charge from the depletion region when reverse biased)

➔For high frequency biasing signals, diode has no time to remove charge when reverse biased, therefor remains on. When forward biased, high current will pass through depletion region and PIN diode acts like variable resistance.

➔Resistance is reversely proportional to the current passing through PIN.

PIN modulators

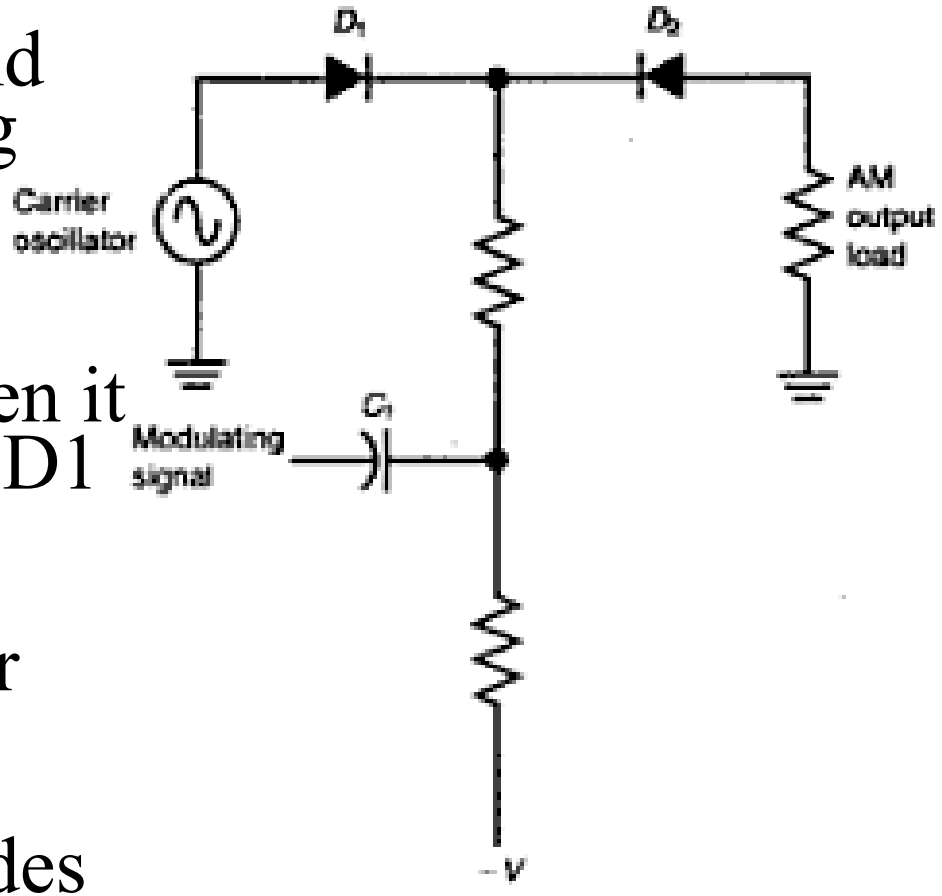
When forward biased , resistance of both D1 and D2 are linearly varying with the current flowing through it.

The modulating signal rides the negative DC voltage V- and adds to it or subtract from it. Then it varies the current and therefor the resistance of D1 and D2.

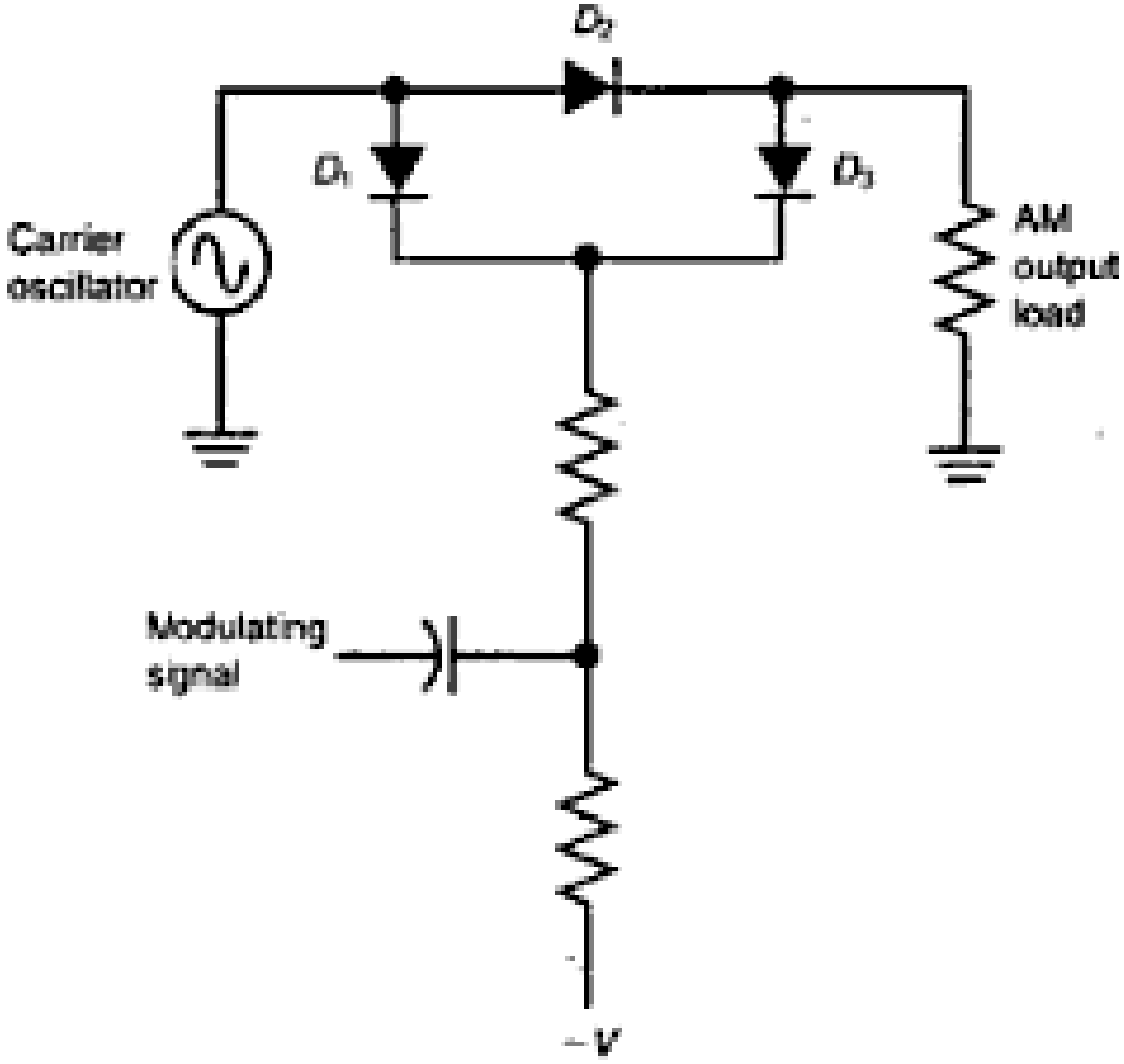
The two resistances are in series with the carrier signal and the load.

Positive going m(t) reduce the bias on both diodes and increase their resistances. And carrier will be reduced.

Negative going m(t) will add on the forward bias and reduce the resistance of diodes and therefore increase the carrier amplitude.



- Diodes can be arranged as a Pi network, which helps to maintain constant impedance even in under modulation.
- PIN diodes forms variable attenuator circuits whose attenuation varies with the amplitude of the modulating signal m(t).
- Amplifiers are needed to amplify the attenuated signal.

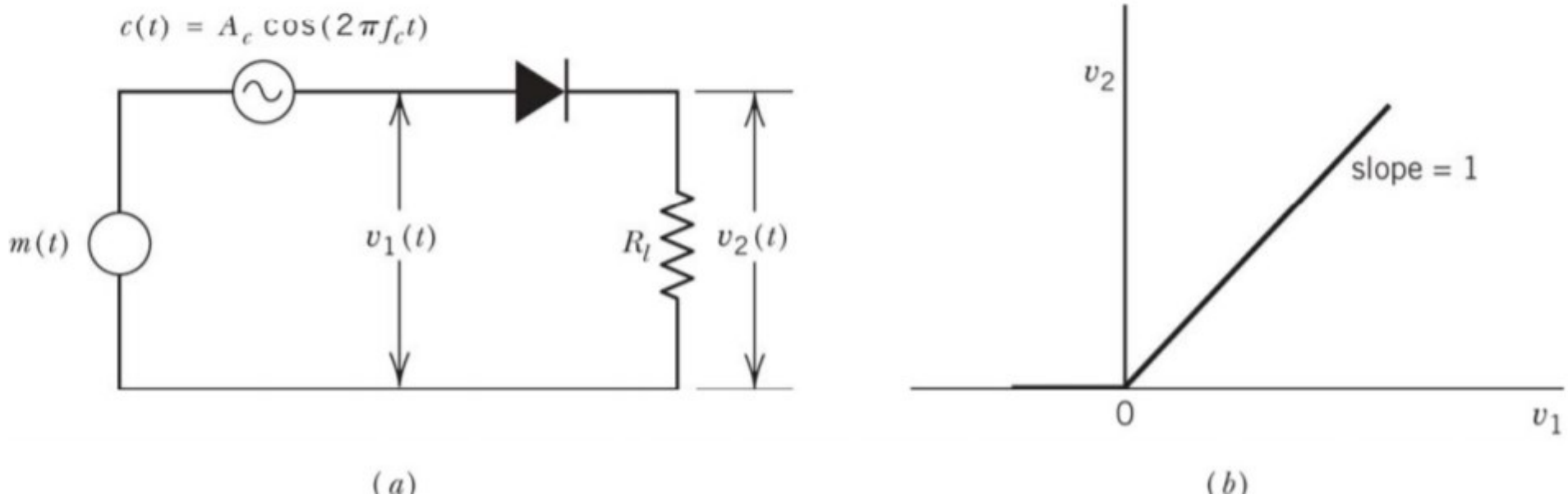


Switching Modulator (1/4)

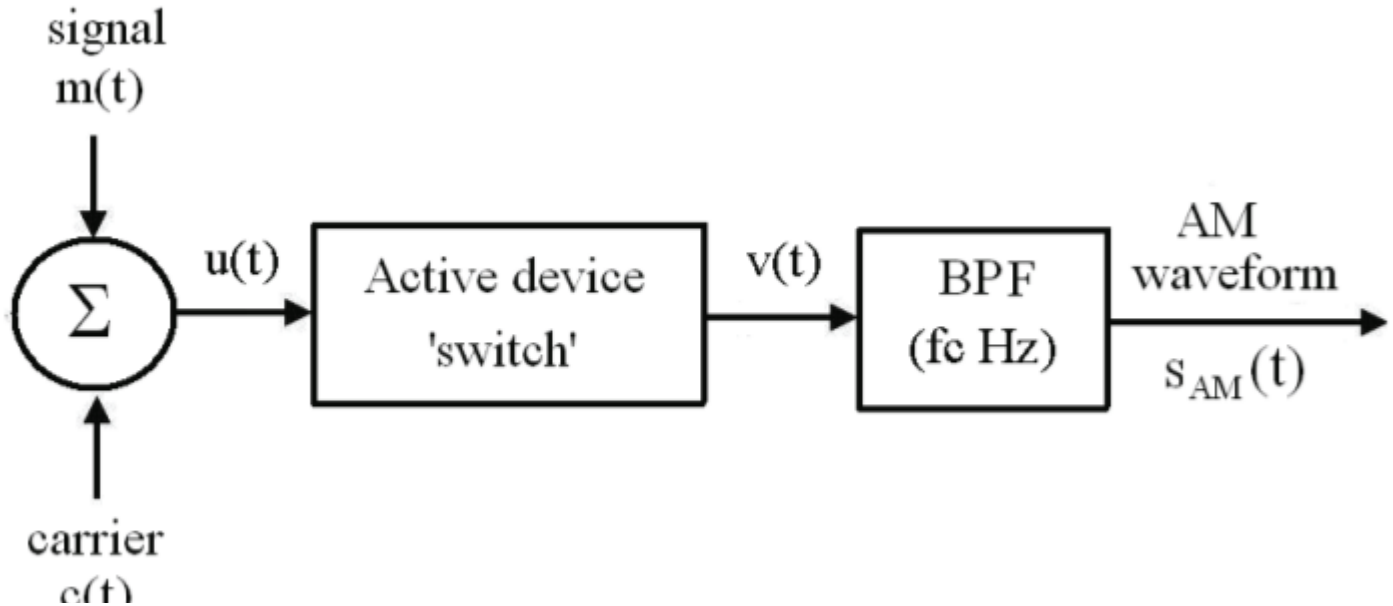
- One way to generate an AM wave: *Switching Modulator*.
  - Assume carrier wave $c(t)$ is large in amplitude and the diode acts as an *ideal switch*.

$$v_1(t) = A_c \cos(2\pi f_c t) + m(t) \tag{3.8}$$

$$v_2(t) \approx \begin{cases} v_1(t), & c(t) > 0 \\ 0, & c(t) < 0 \end{cases} \tag{3.9}$$



(a) (b)



It can be seen that the input to the active device $u(t)$, is given by,

$$u(t) = [\, m(t) + A_C \cos(2\pi f_C t)]$$

$$v(t) \cong \begin{cases} u(t) & c(t) > 0 \\ 0 & c(t) < 0 \end{cases}$$

or equivalently as,

$$v(t) = u(t)g(t)$$

where $g(t)$ is a rectangular pulse waveform, switching states between 0V and +1V, at a frequency equal to the carrier frequency f_C Hz. Using Fourier analysis, it can be shown that the output of the band pass filter (BPF), tuned to the carrier frequency f_C, and bandwidth $2f_m$, results in the desired AM waveform, given by:

$$s_{AM}(t) = \frac{A_C}{2}\left[1 + \frac{4}{\pi A_C} m(t)\right] \cos(2\pi f_C t)$$

The blocks in the 'switching modulator' can be converted to the 'square-law' modulator, which is another method of low power AM generation, by changing the region of operation of the active device of figure 1. Here the active device is operated such that its output is related to its input through,

$$v(t) = a_1 u(t) + a_2 u^2(t) \qquad (6)$$

with a_1 and a_2 being constants, and $u(t)$ remaining same as before . With signal $v(t)$ given to a BPF tuned to the carrier frequency f_C with bandwidth $2f_m$, produces the desired AM

$$s_{AM}(t) = a_1 A_C \left[1 + \frac{2a_2}{a_1} m(t) \right] \cos(2\pi f_C t)$$

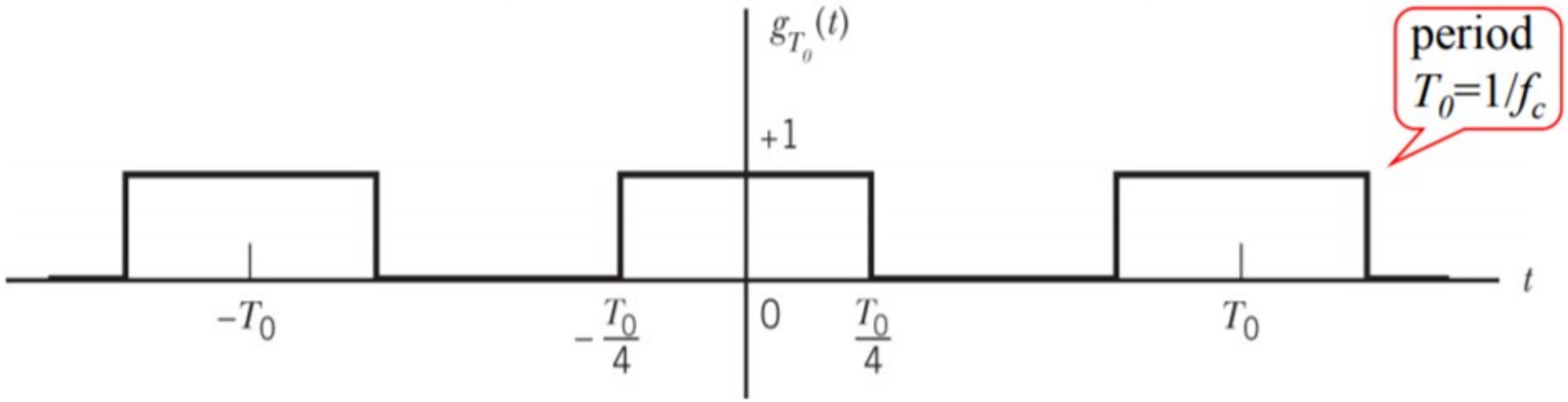
The proper functioning of this modulator depends on operating the active device in the 'square-law' region, which necessitates the transfer characteristic, can be exactly represented by $v(t) = a_1 u(t) + a_2 u^2(t)$

This is a valid assumption for any active device, for a very small operating range. Moreover, maintaining the operating range within permitted levels is practically difficult, since the amplitude swing of the message signal is unknown. Hence, the square-law modulator generates AM, for limited operating range in the carrier and signal strengths. This is the main drawback of the square-law modulator.

Switching Modulator (2/4)

- From Eq. (3.9), load voltage $v_2(t)$ varies periodically between the values $v_1(t)$ and zeros at a rate equal to the carrier frequency f_c.
- By assuming a modulating wave that is weak compared with the carrier wave, we have effectively replace the nonlinear behavior of the diode by an approximately equivalent piecewise-linear time-varying operation.
- We may express Eq. (3.9) mathematically as

$$v_2(t) \approx \left[A_c \cos(2\pi f_c t) + m(t)\right] g_{T_0}(t) \qquad (3.10)$$



Switching Modulator (3/4)

$$g_{T_0}(t) = a_0 + \sum_{n=1}^{\infty}\left(a_n \cos\left(2\pi \frac{n}{T_0} t \right) + b_n \sin\left(2\pi \frac{n}{T_0} t \right) \right)$$

$$a_0 = \frac{1}{T_0}\int_{-T_0/2}^{T_0/2} g_{T_0}(t)\,dt$$

$$a_n = \frac{2}{T_0}\int_{-T_0/2}^{T_0/2} g_{T_0}(t)\cos\left(2\pi \frac{n}{T_0} t \right) dt$$

$$b_n = \frac{2}{T_0}\int_{-T_0/2}^{T_0/2} g_{T_0}(t)\sin\left(2\pi \frac{n}{T_0} t \right) dt$$

$$b_n = \frac{2}{T_0}\int_{-\frac{T_0}{4}}^{\frac{T_0}{4}} \sin\left(2\pi \frac{n}{T_0} t \right) dt = -\frac{2}{T_0}\frac{\cos\left(2\pi \frac{n}{T_0} t \right)}{2\pi \frac{n}{T_0}}\Bigg|_{-\frac{T_0}{4}}^{\frac{T_0}{4}}$$

$$= -\frac{1}{n\pi}\left[\cos\left(\frac{n\pi}{2} \right) - \cos\left(-\frac{n\pi}{2} \right) \right] = 0$$

$$a_0 = \frac{1}{T_0}\int_{-\frac{T_0}{4}}^{\frac{T_0}{4}} dt = \frac{1}{2}$$

$$a_n = \frac{2}{T_0}\int_{-\frac{T_0}{4}}^{\frac{T_0}{4}} \cos 2\pi \frac{n}{T_0} t\,dt = \frac{2}{T_0}\frac{\sin 2\pi \frac{n}{T_0} t}{2\pi \frac{n}{T_0}}\Bigg|_{-\frac{T_0}{4}}^{\frac{T_0}{4}}$$

$$= \frac{1}{n\pi}\left[\sin\left(\frac{n\pi}{2} \right) - \sin\left(-\frac{n\pi}{2} \right) \right] = \frac{2}{n\pi}\sin\left(\frac{n\pi}{2} \right)$$

$$= \frac{2}{(2m-1)\pi}\sin\left(\frac{(2m-1)\pi}{2} \right)$$

$$= \frac{2}{(2m-1)\pi}\left[-\cos(m\pi) \right]$$

$$= \frac{2}{(2m-1)\pi}\left[-(-1)^m \right] = \frac{2}{(2m-1)\pi}(-1)^{m+1}$$

$$= \frac{2}{(2m-1)\pi}(-1)^{m-1}$$

Switching Modulator (4/4)

$$g_{T_0}(t) = \frac{1}{2} + \frac{2}{\pi}\sum_{n=1}^{\infty}\frac{(-1)^{n-1}}{2n-1}\cos\left[2\pi f_c t(2n-1)\right] \qquad (3.11)$$

- Substituting Eq. (3.11) in (3.10), $v_2(t)$ consists of two component
  - A desired AM wave:

$$v_2(t) \approx \left[A_c\cos(2\pi f_c t) + m(t)\right] g_{T_0}(t) \quad (3.10)$$

$$\frac{A_c}{2}\left[1 + \frac{4}{\pi A_c}m(t)\right]\cos(2\pi f_c t) \quad , \quad k_a = \frac{4}{\pi A_c}$$

  - Unwanted component, the spectrum of which contains
    - Delta function at 0, $\pm 2f_c$, $\pm 4f_c$ and so on.
    - Occupy frequency intervals of width $2W$ centered at 0, $\pm 3f_c$, $\pm 5f_c$ and so on, where W is the message bandwidth.
    - Be removed by using a band-pass filter with mid-band frequency f_c and bandwidth $2W$, provide that $f_c > 2W$.

Power Amplifiers

we dealt mainly with small-signal voltage gains, current gains. In this lecture, we analyze and design circuits that must deliver a specified power to a load.

A multistage amplifier may be required to deliver a large amount of power to a passive load. This power may be in the form of a large current delivered to a relatively small load resistance such as an audio speaker, or may be in the form of a large voltage delivered to a relatively large load resistance such as in a switching power supply.

Two important functions of the output stage are to provide a **low output resistance** so that it can deliver the signal power to the load without loss of gain and to **maintain linearity** in the output signal.

Types of Power Amplifiers (PAs) :
1) Linear (Classes: A, B, AB) : output is directly proportional to input , low-level AM signals need linear Amp.
2) Class C and Switching (Classes: D,E,F) : such amplifiers are used for FM signals since amplitude does not vary.

Power amplifiers can be classified by duration of conducting or by their linearity.

In (class A) PA they are biased so they conduct continuously at 360 degrees, where input varies collector current over the linear region in the I/V char. Curve.

Class A power amplifier (BJT) operation

Power transistors are large-area devices. Because of differences in geometry and doping concentrations, their properties tend to vary from those of the small-signal devices.

small-signal BJT **Vs** two power BJTs

The current gain is generally smaller in the power transistors, typically in the range of 20 to 100

Table 8.1 Comparison of the characteristics and maximum ratings of a small-signal and power BJT

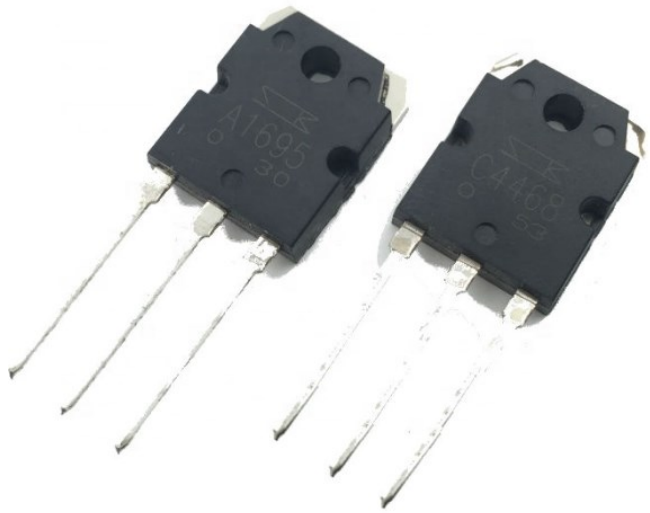
Parameter	Small-Signal BJT (2N2222A)	Power BJT (2N3055)	Power BJT (2N6078)
V_{CE}(max) (V)	40	60	250
I_C(max) (A)	0.8	15	7
P_D(max) (W) (at $T = 25$ °C)	1.2	115	45
β	35–100	5–20	12–70
f_T (MHz)	300	0.8	1

The maximum rated collector current $I_{C,rated}$ may be related to one or more of the following:

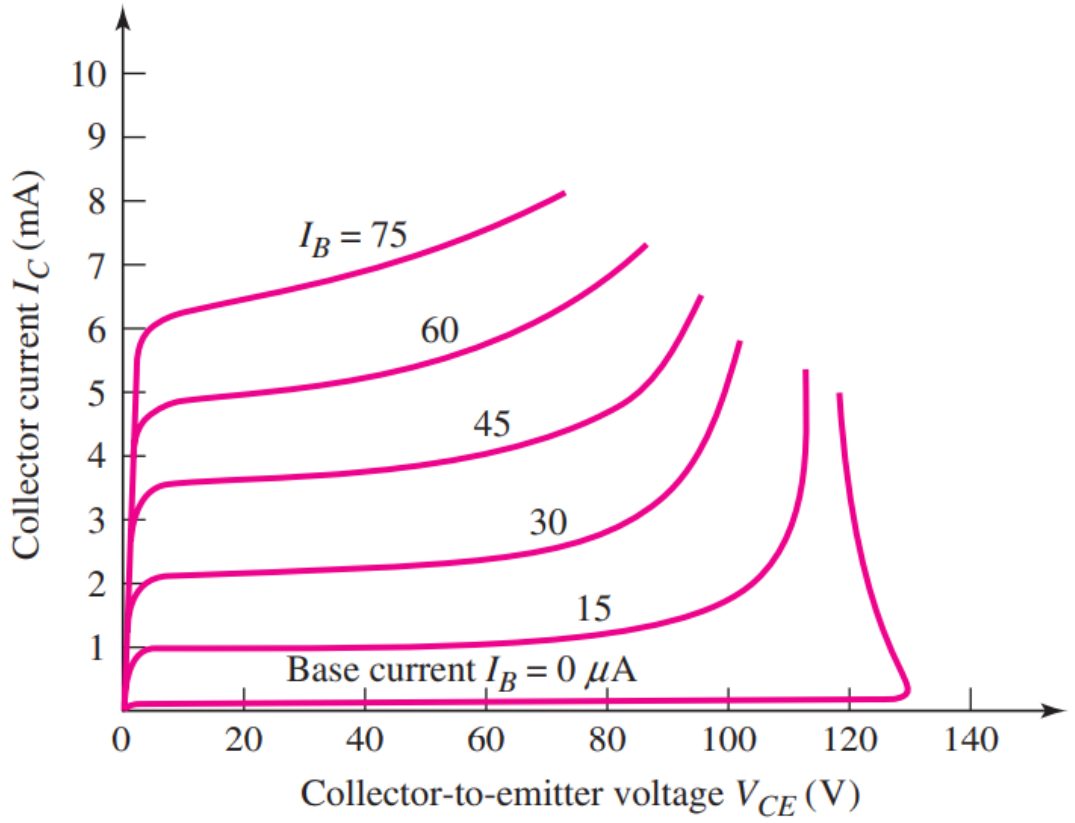
1) The maximum current that the wires connecting the semiconductor to the external terminals can handle.

2) The collector current at which the current gain falls below a minimum specified value.

3) The current that leads to the maximum power dissipation when the transistor is in saturation.



The maximum voltage limitation in a BJT is generally associated with avalanche breakdown in the reverse-biased base–collector junction. In the common-emitter configuration, the breakdown voltage mechanism also involves the transistor gain, as well as the breakdown phenomenon on the pn junction.



The breakdown voltage when the base terminal is open circuited ($I_B = 0$) is VCEO . this value is approximately 130 V

When the transistor is biased in the active region, the collector current begins to increase significantly before breakdown voltage VCEO is reached, and all the curves tend to merge to the same collector–emitter voltage once breakdown has occurred.

The voltage at which these curves merge is denoted VC E (sus) and is the minimum voltage necessary to sustain the transistor in breakdown. From the data in Figure 8.2, the value of VC E (sus) is approximately 115 V

The instantaneous power dissipation in a BJT is given by:

$$p_Q = v_{CE} i_C + v_{BE} i_B$$

The base current is generally much smaller than the collector current; therefore, to a good approximation, the instantaneous power dissipation is:

$$p_Q \cong v_{CE} i_C$$

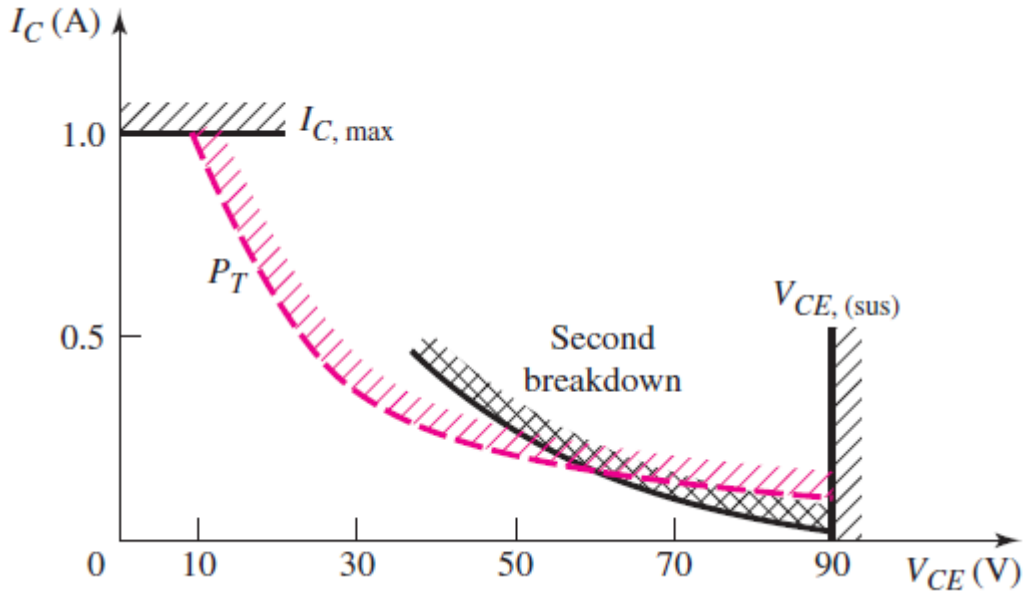
The average power, which is found by integrating above equation over one cycle of the signal, is:

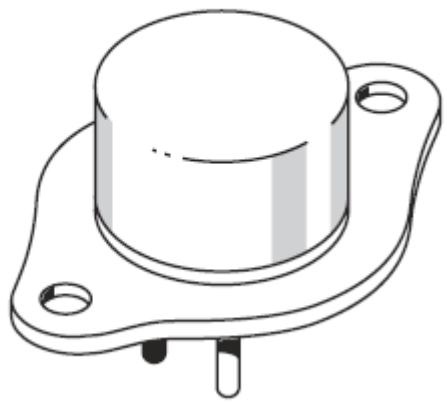
$$\bar{P}_Q = \frac{1}{T} \int_0^T v_{CE} i_C \, dt$$

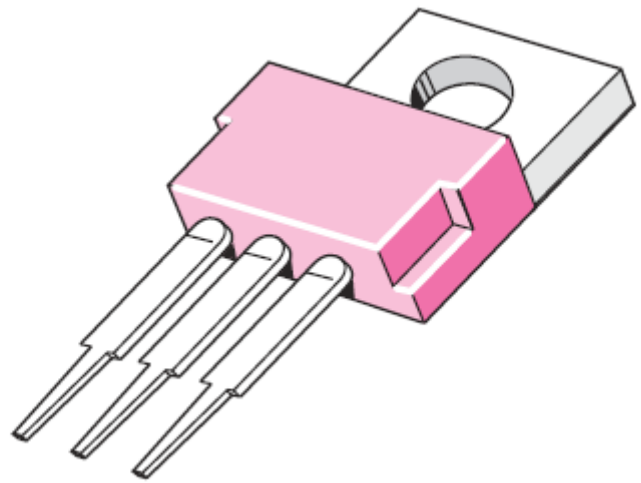
The average power dissipated in a BJT must be kept below a specified maximum value, to ensure that the temperature of the device remains below a maximum value. If we assume that the collector current and collector–emitter voltage are dc quantities, then at the maximum rated power PT for the transistor, we can write

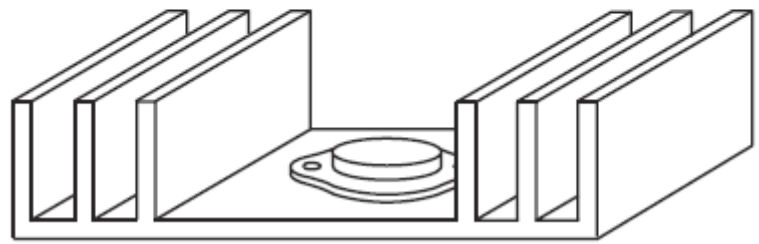
$$P_T = V_{CE} I_C$$

The maximum current, voltage, and power limitations can be illustrated on the IC versus VCE characteristics, as shown next figure. The i_C–v_{CE} operating point may move momentarily outside the safe operating area without damaging the transistor, but this depends on how far the Q-point moves outside the area and for how long. For our purposes, we will assume that the device must remain within the safe operating area at all times.









CLASSES OF AMPLIFIERS

Some power amplifiers are classified according to the percent of time the output transistors are conducting, or "turned on." Four of the principal classifications are:
class A, class B, class AB, and class C.

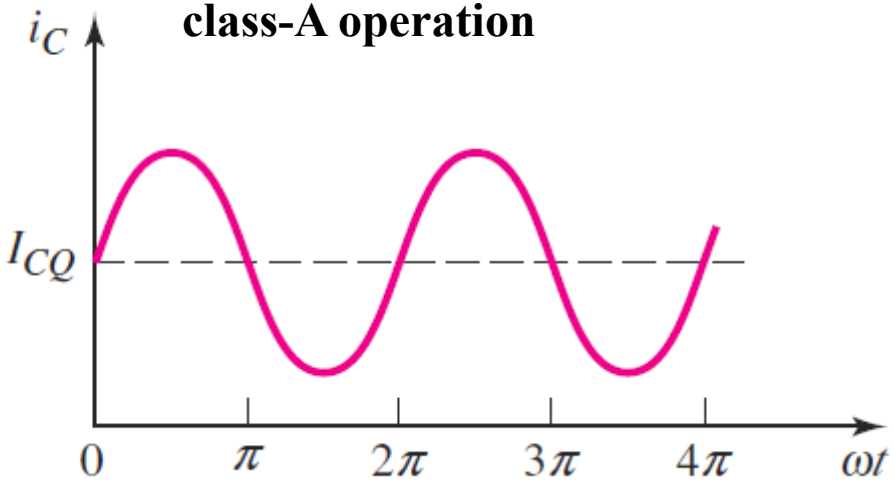
These classifications are illustrated next figure for a sinusoidal input signal. In **class-A operation,** an output transistor is biased at a quiescent current I_Q and conducts for the entire cycle of the input signal.

For **class-B operation,** an output transistor conducts for only one-half of each sine wave input cycle.

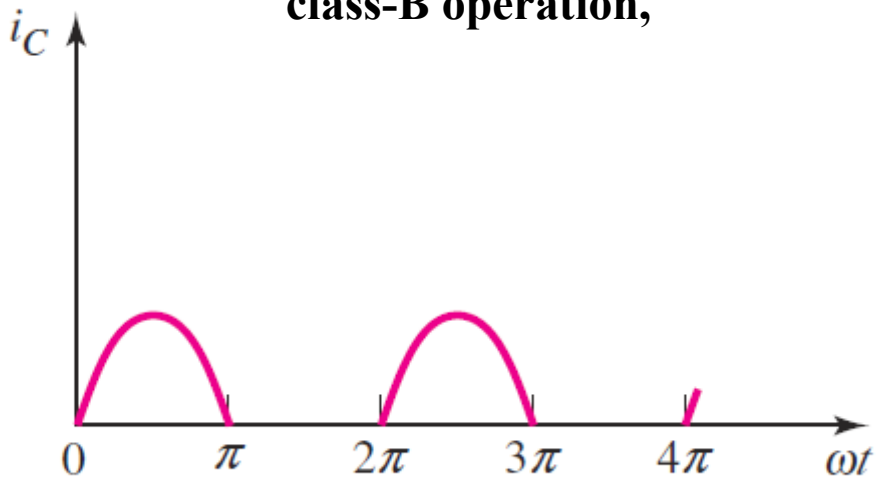
In **class-AB operation,** an output transistor is biased at a small quiescent current I_Q and conducts for slightly more than half a cycle.

In contrast, in
class-C operation an output transistor conducts for less than half a cycle.

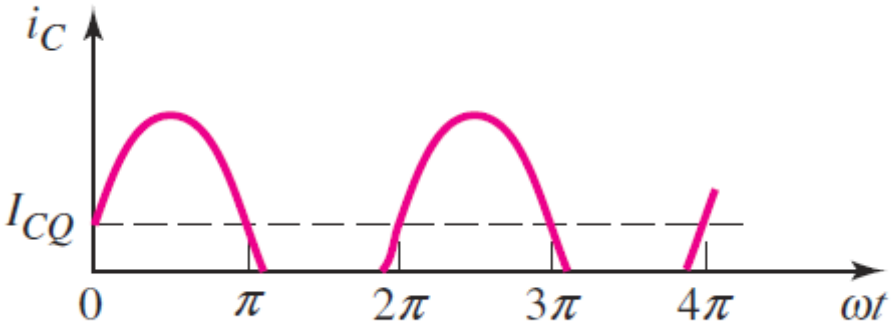
class-A operation



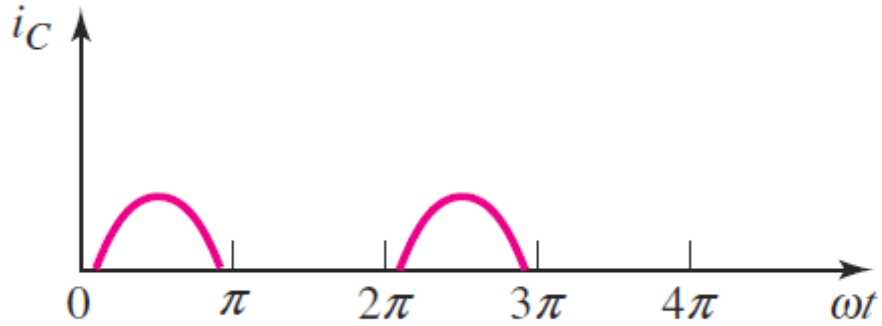
class-B operation,



class-AB operation,



class-C operation



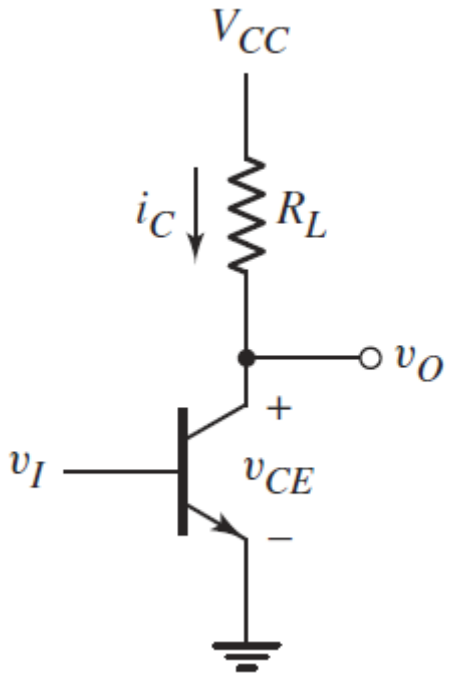
These four types of power amplifiers use the output transistors as a current source. We will analyze the biasing, load lines, and power efficiency of each class of these power amplifiers.

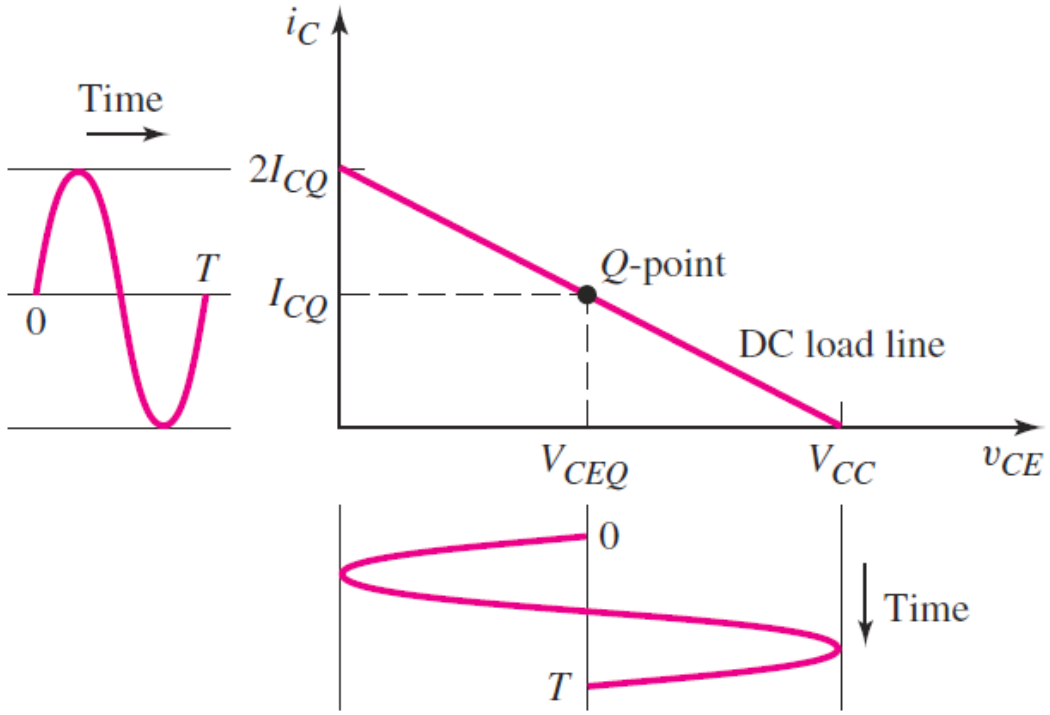
Class-A Operation

A basic common-emitter configuration is shown next figure in which bias circuitry has been omitted, for convenience. Also, in this **standard class-A amplifier** configuration, no inductors or transformers are used.

The dc load line is shown next figure. The *Q*-point is assumed to be in the center of the load line, so that $V_{CEQ} = V_{CC}/2$.

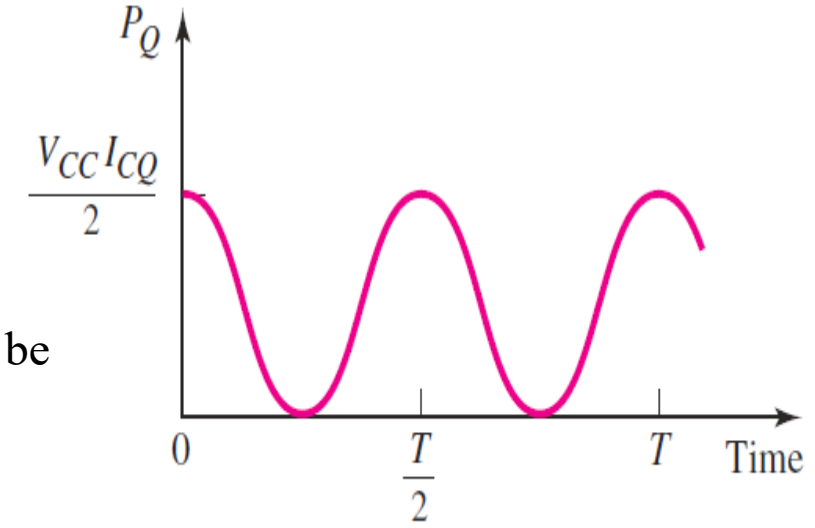
If a sinusoidal input signal is applied, sinusoidal variations are induced in the collector current and collector–emitter voltage. values of $v_{CE} = 0$ and $i_C = 2I_{CQ}$ cannot actually be attained.





The instantaneous power dissipation in the transistor, neglecting the base current, is

$$p_Q = v_{CE} i_C$$



For a sinusoidal input signal, the collector current and collector-emitter voltage can be written

$$i_C = I_{CQ} + I_p \sin \omega t \qquad v_{CE} = \frac{V_{CC}}{2} - V_p \sin \omega t$$

If we consider the absolute possible variations, then $I_p = I_{CQ}$ and $V_p = V_{CC}/2$. Therefore, the instantaneous power dissipation in the transistor is

$$p_Q = \frac{V_{CC} I_{CQ}}{2}(1 - \sin^2 \omega t)$$

Since the maximum power dissipation corresponds to the quiescent value (see Figure 8.5), the transistor must be capable of handling a continuous power dissipation of $V_{CC}I_{CQ}/2$ when the input signal is zero.

The **power conversion efficiency** is defined as: $$\eta = \frac{\text{signal load power}(\bar{P}_L)}{\text{supply power}(\bar{P}_S)}$$

where P_L is the average ac power delivered to the load and .P_s is the average power supplied by the V_{CC} power source(s)

For the standard class-A amplifier and sinusoidal input signals, the average ac power delivered to the load . Using the absolute possible variations, we have:

$$Aerage\ Load\ AC\ power\ PL_{(avg)} = \frac{V_P I_P}{2} \qquad \bar{P}_L(\max) = \left(\frac{1}{2}\right)\left(\frac{V_{CC}}{2}\right)(I_{CQ}) = \frac{V_{CC}I_{CQ}}{4}$$

The average power supplied by the V_{CC} source is: $$\bar{P}_S = V_{CC}I_{CQ}$$

The maximum attainable conversion efficiency is therefore: $$\eta(\max) = \frac{\frac{1}{4}V_{CC}I_{CQ}}{V_{CC}I_{CQ}} \Rightarrow 25\%$$

We must keep in mind that the maximum possible conversion efficiency may change when a load is connected to the output of the amplifier. This efficiency is relatively low; therefore, standard class-A amplifiers are normally not used when signal powers greater than approximately 1 W are required.

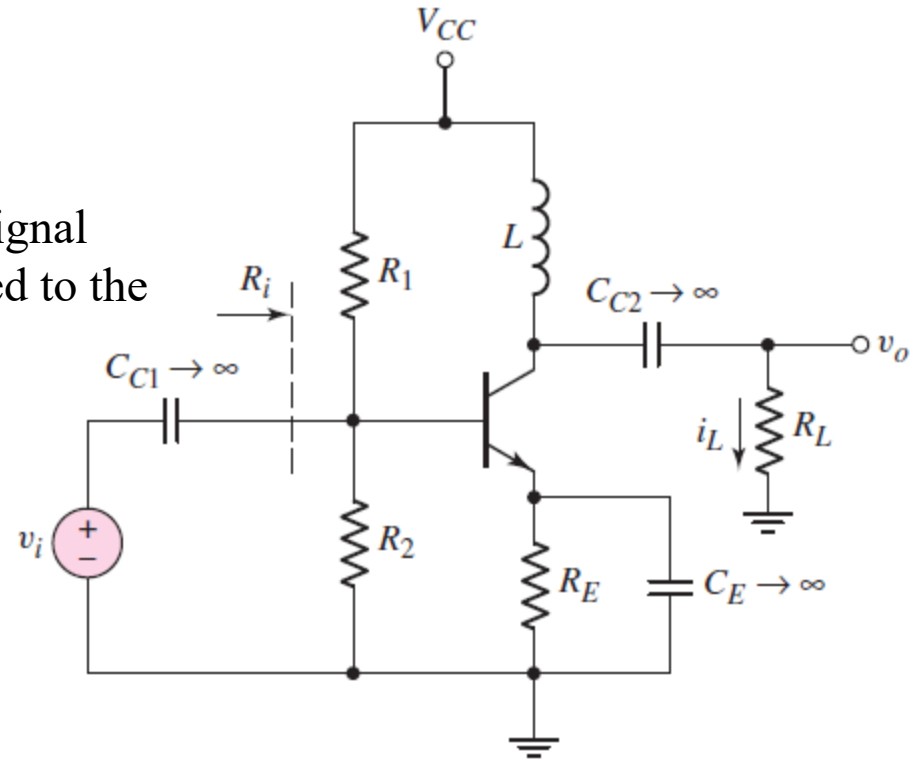
We must also emphasize that in practice, a maximum signal voltage of $V_{CC}/2$ and a maximum signal current of I_{CQ} are not possible. The output signal voltage must be limited to smaller values in order to avoid transistor saturation and cutoff, and the resulting nonlinear distortion. The calculation for the maximum possible efficiency also neglects power dissipation in the bias circuitry. Consequently, the realistic maximum conversion
efficiency in a standard class-A amplifier is on the order of 20 percent or less.

The dissipated power inside the diode due to the low power efficiency is unacceptable especially if high output power is seeked. Therefor there is a need to change the design to get higher power efficiency

Class A Power Amplifier conversion efficiency can be increased with the use of inductors and transformers.

Inductively Coupled Amplifier

Delivering a large power to a load generally requires both a large voltage and a high current. In a common-emitter circuit, this requirement can be met by replacing the collector resistor with an inductor,



The inductor is a short circuit to a dc current, but acts as an open circuit to an ac signal operating at a sufficiently high frequency. The entire ac current is therefore coupled to the load. We assume that $\omega L >> R_L$ at the lowest signal frequency.

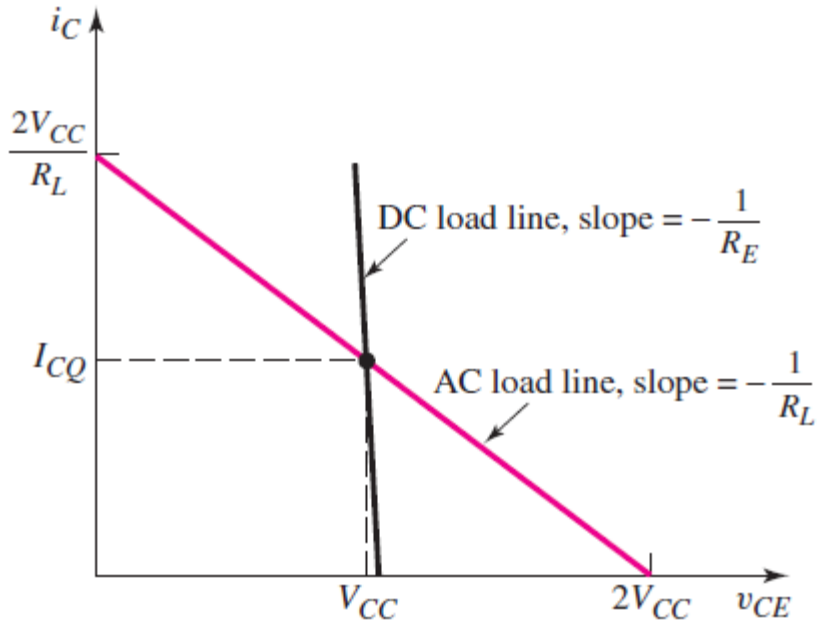
We assume that the resistance of the inductor is negligible, and that the emitter resistor value is small. The quiescent collector–emitter voltage is then approximately $V_{CEQ} \sim= V_{CC}$. The ac collector current is:

$$i_c = \frac{-v_{ce}}{R_L}$$

To obtain the maximum symmetrical output-signal swing, which will in turn produce the maximum power, we want:

$$I_{CQ} \cong \frac{V_{CC}}{R_L}$$

For this condition, the ac load line intersects the v_{CE} axis at $2V_{CC}$.



The use of an inductor or storage device results in an output ac voltage swing that is larger than V_{CC}. The polarity of the induced voltage across the inductor may be such that the voltage adds to V_{CC}, producing an output voltage that is larger than V_{CC}. The absolute maximum amplitude of the signal current in the load is I_{CQ}; therefore, the maximum possible average signal power delivered to the load is:

$$\bar{P}_L(\max) = \frac{1}{2} I_{CQ}^2 R_L = \frac{1}{2} \cdot \frac{V_{CC}^2}{R_L}$$

If we neglect the power dissipation in the bias resistors R_1 and R_2, the average power supplied by the V_{CC} source is

$$\bar{P}_S = V_{CC} I_{CQ} = \frac{V_{CC}^2}{R_L}$$

The maximum possible power conversion efficiency is then

$$\eta(\max) = \frac{\bar{P}_L(\max)}{\bar{P}_S} = \frac{\frac{1}{2} \cdot \frac{V_{CC}^2}{R_L}}{\frac{V_{CC}^2}{R_L}} = \frac{1}{2} \Rightarrow 50\%$$

This demonstrates that, in a standard class-A amplifier, replacing the collector resistor with an inductor doubles the maximum possible power conversion efficiency.

Transformer-Coupled Common-Emitter Amplifier

The design of an inductively coupled amplifier to achieve high power conversion efficiency may be difficult, depending on the relationship between the supply voltage V_{CC} and the load resistance R_L. The effective load resistance can be optimized by using a transformer with the proper turns ratio.

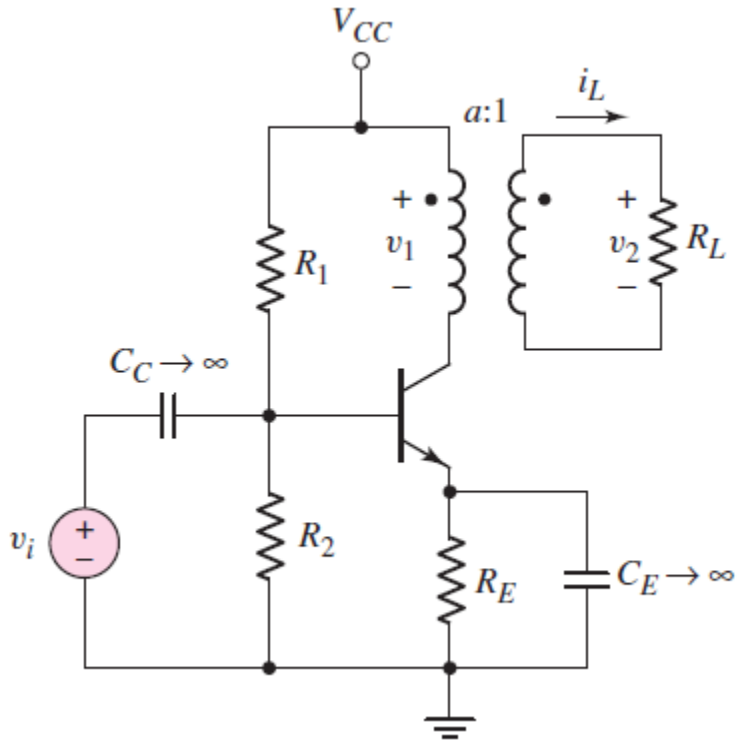
If we neglect any resistance in the transformer and assume that R_E is small, the quiescent collector–emitter voltage is: $V_{CEQ} \cong V_{CC}$

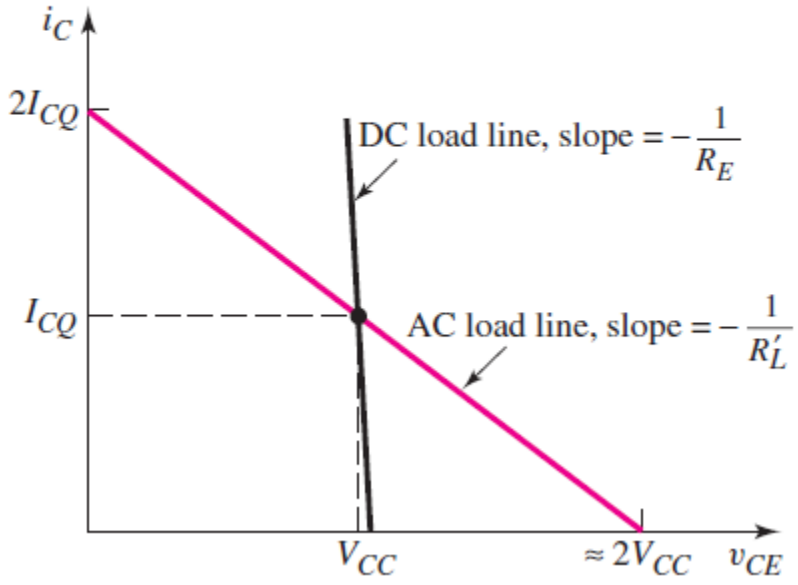
Assuming an ideal transformer, the currents and voltages are related by $i_L = ai_C$ and $v_2 = v_1/a$ where a is the ratio of primary to secondary turns, or simply the turns ratio. Dividing voltages by currents, we find:

$$\frac{v_2}{i_L} = \frac{v_1/a}{ai_C} = \frac{v_1}{i_C} \cdot \frac{1}{a^2}$$

The load resistance is $R_L = v_2/i_L$. We can define a transformed load resistance as

$$R'_L = \frac{v_1}{i_C} = a^2 \cdot \frac{v^2}{i_L} = a^2 R_L$$





The turns ratio is designed to produce the maximum symmetrical swing in the output current and voltage; therefore,

$$R'_L = \frac{2V_{CC}}{2I_{CQ}} = \frac{V_{CC}}{I_{CQ}} = a^2 R_L$$

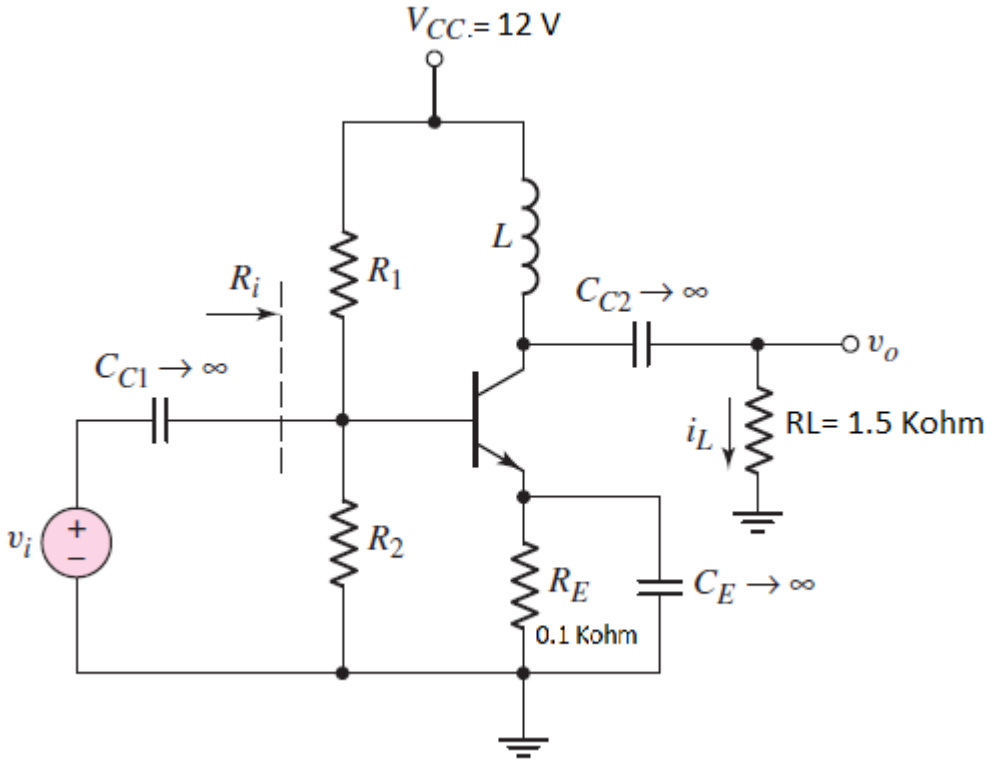
The maximum average power delivered to the load is equal to the maximum average power delivered to the primary of the ideal transformer, as follows:

$$\bar{P}_L(\max) = \tfrac{1}{2} V_{CC} I_{CQ}$$

where V_{cc} and I_{cQ} are the maximum possible amplitudes of the sinusoidal signals. If we neglect the power dissipation in the bias resistors R_1 and R_2, the average power supplied by the V_{cc} source is $\bar{P}_S = V_{CC} I_{CQ}$

and the maximum possible power conversion efficiency is again: $\eta(\max) = 50\%$

Example: for the inductive coupled amplifier shown next figure , if β = 75, R_{TH} = (1+ β) R_E, V_{CC} =12 volts, R_L=1.5 Kohm, R_E=100 Ohms. Then find the value of R_1 and R_2 at maximum symmetrical swing.



Answer: R_{TH} = (1+ β) R_E= 76 X (0.1) = 7.6 Kohm

At Maximum symmetrical swing :

$I_{CQ} = V_{CC}/R_L$ = 12/1.5K = 8 mA

➔ I_{BQ} = 107 uA

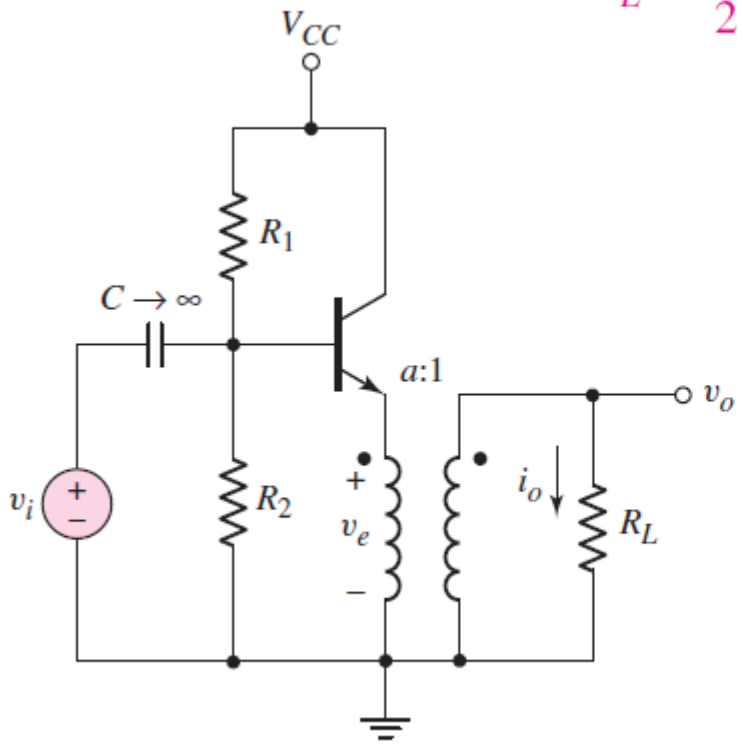
$V_{TH} = I_B \cdot R_{TH} + V_{BE} + I_E R_E$
= 107 uA (7.6 Kohm) +0.7 +76 (107 uA)
=2.33 Volts

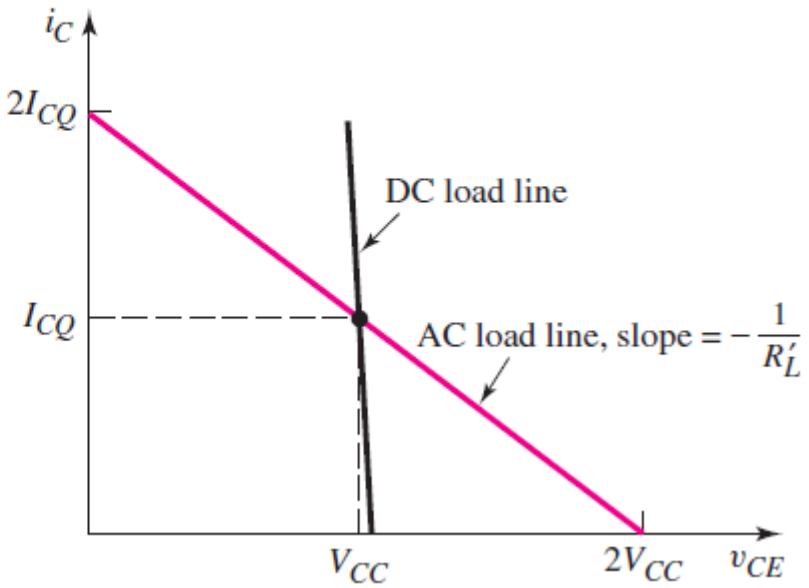
$R_1 = R_{TH} (V_{CC}/ V_{TH}) = 7.6$ K (12/2.33) = 39.14 Kohm
$R_2 = (R_1 R_{TH}) / (R_1 - R_{TH})$ = 9.43 KOhm

Transformer-Coupled Emitter-Follower Amplifier

Since the emitter follower has a low output impedance, it is often used as the output stage of an amplifier. A transformer-coupled emitter follower is shown next figure. The dc and ac load lines are shown. As before, the resistance of the transformer is assumed to be negligible. The transformed load resistance is again $R_L = a^2 R_L$. By correctly designing the turns ratio, we can achieve the maximum symmetrical swing in the output voltage and current. The average power delivered to the load is

$$\bar{P}_L = \frac{1}{2} \cdot \frac{V_p^2}{R_L}$$





where V_p is the peak amplitude of the sinusoidal output voltage. The maximum peak amplitude of the emitter voltage is V_{CC}, so that the maximum peak amplitude of the output signal is $Vp(\max) = VCC/a$

The maximum average output signal power is therefore: $\bar{P}_L(\max) = \frac{1}{2} \cdot \frac{[V_p(\max)]^2}{R_L} = \frac{V_{CC}^2}{2a^2 R_L}$

The maximum power conversion efficiency for this circuit is also 50 percent.

Example

Objective: Design a transformer-coupled emitter-follower amplifier to deliver a specified signal power.

Consider the circuit shown in Figure 8.30(a), with parameters $V_{CC} = 24$ V and $R_L = 8\ \Omega$. The average power delivered to the load is to be 5 W, the peak amplitude of the signal emitter current is to be no more than $0.9I_{CQ}$, and that of the signal emitter voltage is to be no more than $0.9V_{CC}$. Let $\beta = 100$.

Solution: The average power delivered to the load is given by $\bar{P}_L = \frac{1}{2} \cdot \frac{V_p^2}{R_L}$ The peak output voltage must therefore be

$$V_p = \sqrt{2R_L \bar{P}_L} = \sqrt{2(8)(5)} = 8.94 \text{ V}$$

and the peak output current is

$$I_p = \frac{V_p}{R_L} = \frac{8.94}{8} = 1.12 \text{ A}$$

Since

$$V_e = 0.9\, V_{CC} = aV_p$$

then

$$a = \frac{0.9\, V_{CC}}{V_p} = \frac{(0.9)(24)}{8.94} = 2.42$$

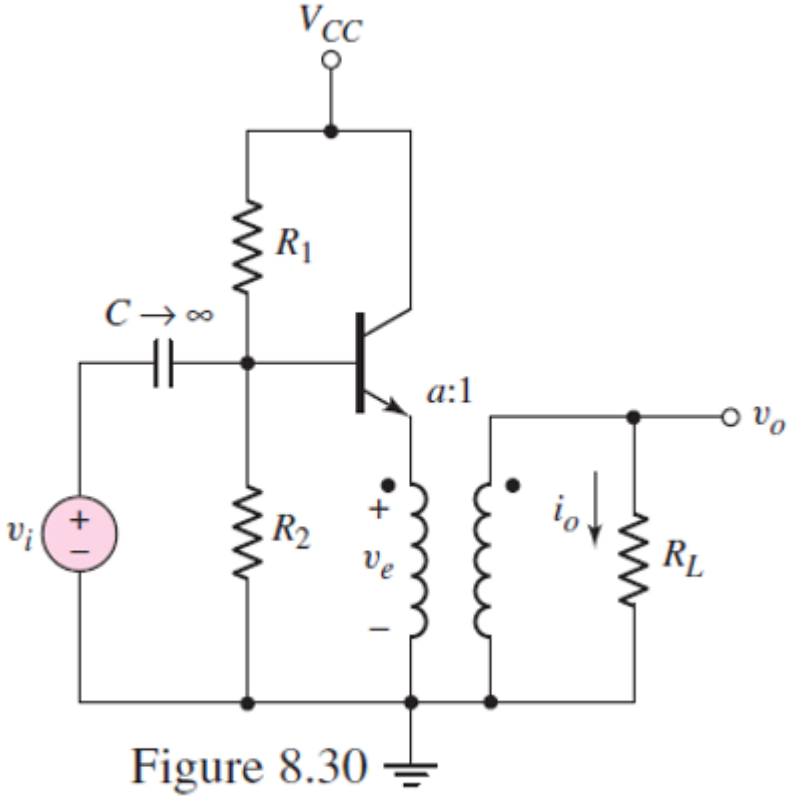


Figure 8.30

Also, since

$$I_e = 0.9 I_{CQ} = I_p / a$$

then

$$I_{CQ} = \frac{1}{0.9} \cdot \frac{I_p}{a} = \frac{1.12}{(0.9)(2.42)} = 0.514 \text{ A}$$

The maximum power dissipated in the transistor, for this class-A operation, is

$$P_Q = V_{CC} I_{CQ} = (24)(0.514) = 12.3 \text{ W}$$

so the transistor must be capable of handling this power.

Bias resistors R_1 and R_2 are found from a dc analysis. The Thevenin equivalent voltage is

$$V_{TH} = I_{BQ} R_{TH} + V_{BE}(\text{on})$$

where

$$R_{TH} = R_1 \| R_2 \quad \text{and} \quad V_{TH} = [R_2/(R_1 + R_2)] \cdot V_{CC}$$

We also have

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{0.514}{100} \Rightarrow 5.14 \text{ mA}$$

Since $V_{TH} < V_{CC}$ and $I_{BQ} \cong 5$ mA, then R_{TH} cannot be unduly large. However, if R_{TH} is small, then the power dissipation in R_1 and R_2 becomes unacceptably high. We choose $R_{TH} = 2.5$ kΩ, so that

$$V_{TH} = \frac{1}{R_1}(R_{TH})V_{CC} = \frac{1}{R_1}(2.5)(24) = (5.14)(2.5) + 0.7$$

Therefore, $R_1 = 4.43$ kΩ and $R_2 = 5.74$ kΩ.

Comment: The average power delivered by V_{CC} (neglecting bias resistor effects) is $\bar{P}_S = V_{CC} I_{CQ} = 12.3$ W, which means that the power conversion efficiency is $\eta = 5/12.3 \Rightarrow 40.7\%$. The efficiency will always be less than the 50% maximum value, if transistor saturation and distortion are to be minimized.

Class B Power Amplifier (Higher conversion efficiency)

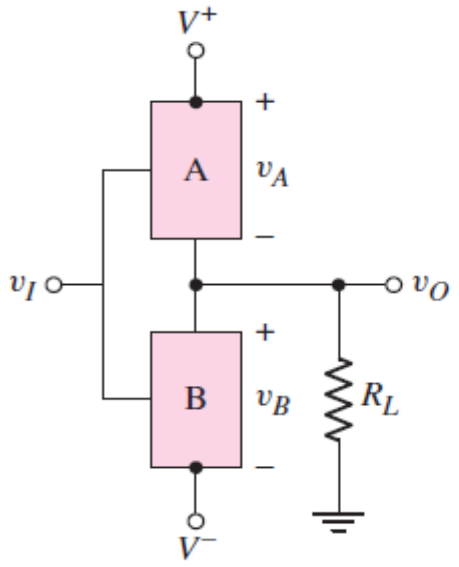
consists of a complementary pair of electronic devices.:

➔ When $v_I = 0$, both devices are off, the bias currents are zero, and $v_O = 0$.

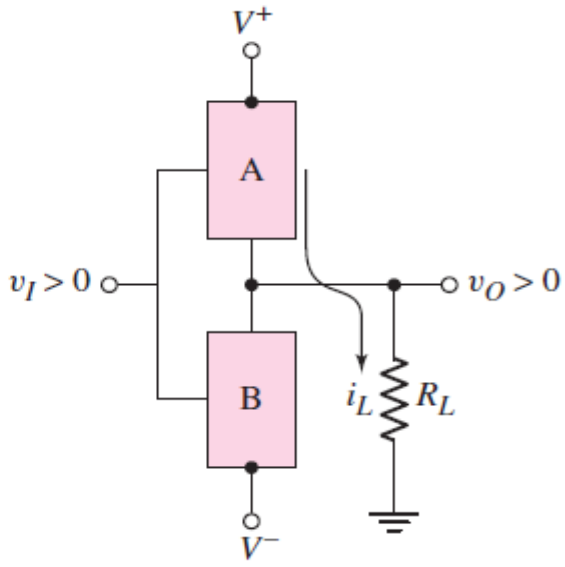
➔ For $v_I > 0$, device A turns on and supplies current to the load.

➔ For $v_I < 0$, device B turns on and sinks current from the load as shown next figure. The voltage transfer characteristics is shown next figure . The ideal voltage gain is unity.

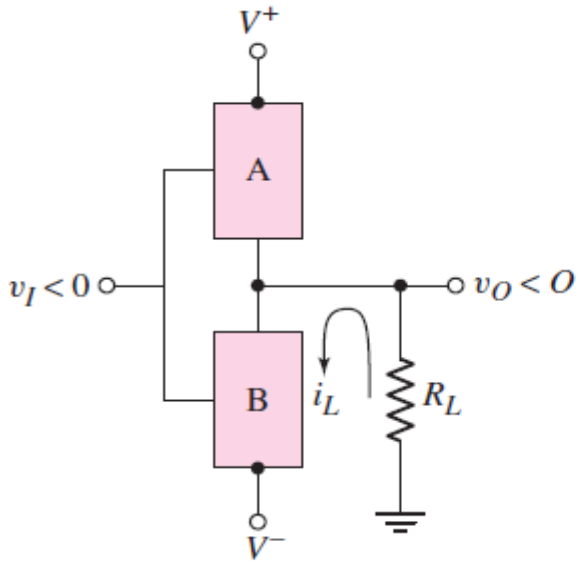
This applies for ideal class B PA only!

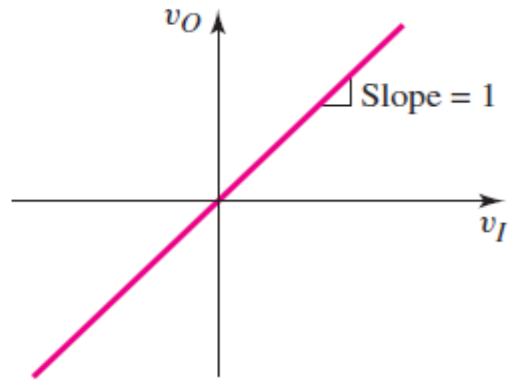


(a)



(b)





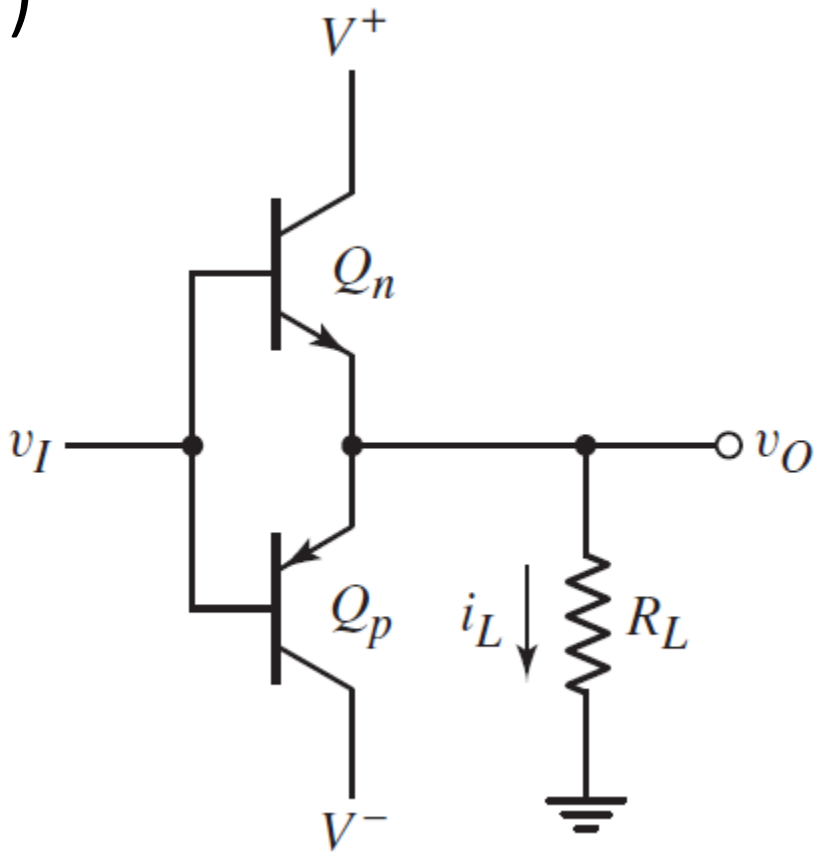
Approximate Class-B Circuit (Practical)

an output stage that consists of a complementary pair of bipolar transistors is shown next.

➔ When the input voltage is $v_I = 0$, both transistors are cut off and the output voltage is $v_O = 0$. If we assume a B–E cut-in voltage of 0.6V, then the output voltage v_O remains zero as long as the input voltage is in the range $-0.6 \le v_I \le +0.6$ V.

➔ If v_I becomes positive and is greater than 0.6 V, then Q_n turns on and operates as an emitter follower. The load current i_L is positive and is supplied through Q_n, and the B–E junction of Q_p is reverse biased.

➔ If v_I becomes negative by more than 0.6 V, then Q_p turns on and operates as an emitter follower. Transistor Q_p is a sink for the load current, which means that i_L is negative.



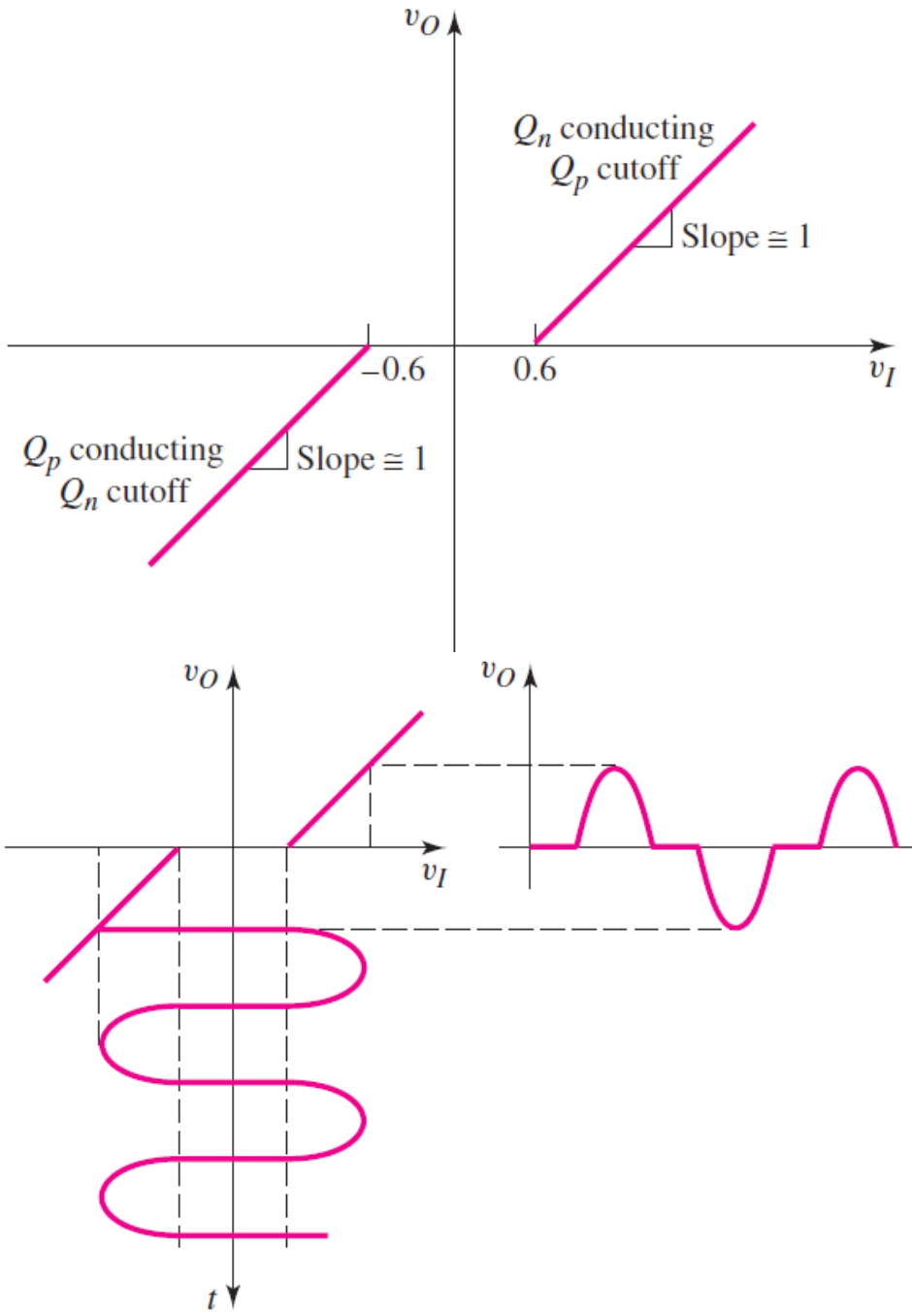
This circuit is called a **complementary push–pull** output stage.

Transistor Q_n conducts during the positive half of the input cycle, and Q_p conducts during the negative half-cycle. The transistors do not both conduct at the same time.

the voltage transfer characteristics for this circuit is shown next figure.

When either transistor is conducting, the voltage gain, which is the slope of the curve, is essentially unity as a result of the emitter follower.

The output voltage for a sinusoidal input signal. When the output voltage is positive is shown next figure , the npn transistor is conducting, and when the output voltage is negative, the pnp transistor is conducting. We can see from this figure that each transistor actually conducts for slightly less than half the time. Thus the bipolar push–pull circuit shown before is not exactly a class-B circuit.



Crossover Distortion

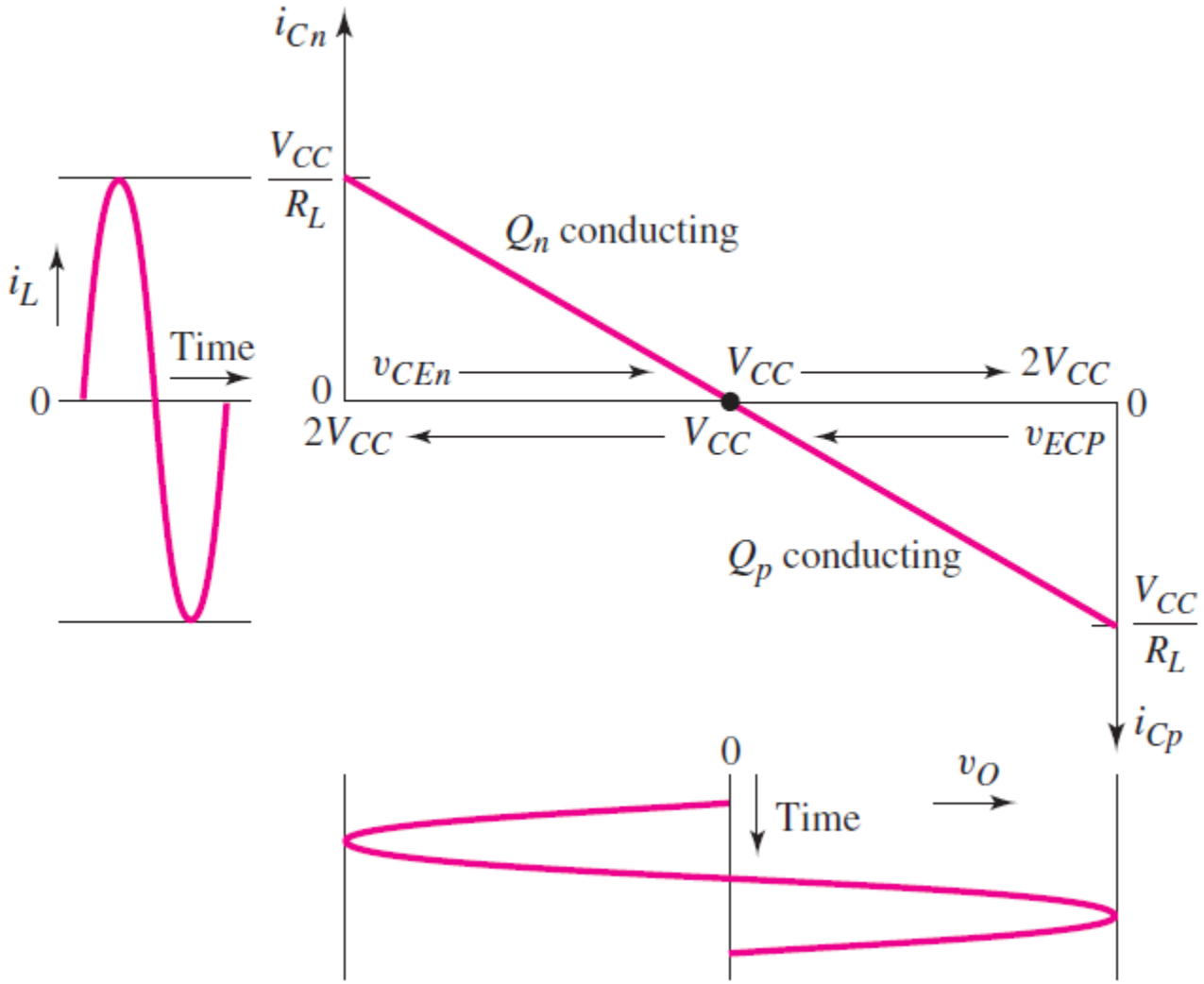
we see that there is a range of input voltage around zero volts where both transistors are cut off and v_o is zero. This portion of the curve is called the *dead band*. The output voltage for a sinusoidal input voltage is shown in Figure 8.21. The output voltage is not a perfect sinusoidal signal, which means that *crossover distortion* is produced by the dead band region.

Crossover distortion can be virtually eliminated by biasing both Qn and Qp with a small quiescent collector current when v_I is zero. This technique is discussed in the next section. The crossover distortion effect can also be minimized with an op-amp used in a feedback configuration.

Idealized Power Efficiency

If we consider an idealized version of the circuit in which the base–emitter turn-on voltages are zero, then each transistor would conduct for exactly one-half cycle of the sinusoidal input signal. This circuit would be an ideal class-B output stage, and the output voltage and load current would be replicas of the input signal. The collector–emitter voltages would also show the same sinusoidal variation.

Next figure illustrates the applicable dc load line. The *Q*-point is at zero collector current, or at cut-off for both transistors. The quiescent power dissipation in each transistor is then zero.



The output voltage for this idealized class-B output stage can be written:

$$v_O = V_p \sin \omega t$$

where the maximum possible value of V_p is V_{CC}.
The instantaneous power dissipation in Q_n is $p_{Qn} = v_{CEn} i_{Cn}$

and the collector current is

$$i_{Cn} = \frac{V_p}{R_L} \sin \omega t$$

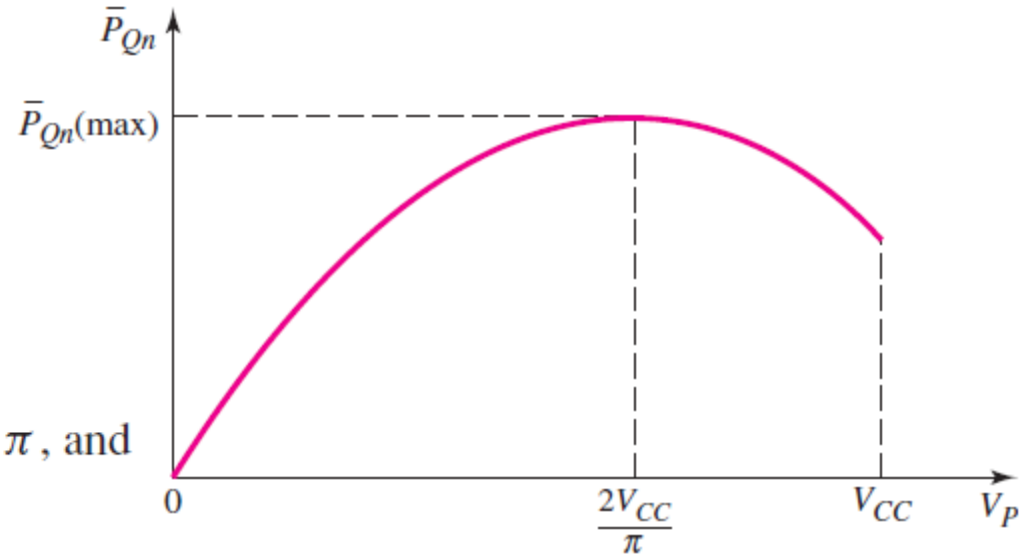
for $0 \leq \omega t \leq \pi$, and

$$i_{Cn} = 0$$

for $\pi \leq \omega t \leq 2\pi$, where V_p is the peak output voltage.

the collector–emitter voltage can be written as

$$v_{CEn} = V_{CC} - V_p \sin \omega t$$



Therefore, the total instantaneous power dissipation in Q_n is

$$p_{Qn} = (V_{CC} - V_p \sin \omega t)\left(\frac{V_p}{R_L} \sin \omega t\right) \quad \text{for } 0 \le \omega t \le \pi, \text{ and}$$

$$p_{Qn} = 0$$

for $\pi \le \omega t \le 2\pi$. The average power dissipation is therefore

$$\bar{P}_{Qn} = \frac{V_{CC} V_p}{\pi R_L} - \frac{V_p^2}{4R_L}$$

The average power dissipation in transistor Q_p is exactly the same as that for Q_n, because of symmetry.

A plot of the average power dissipation in each transistor, as a function of V_p, is shown next figure.

The power dissipation first increases with increasing output voltage, reaches a maximum, and finally decreases with increasing V_p. We determine the maximum average power dissipation by setting the derivative of P_{Qn} with respect to V_p equal to zero, producing:

$$\bar{P}_{Qn}(\max) = \frac{V_{CC}^2}{\pi^2 R_L}$$

which occurs when

$$V_p\big|_{\bar{P}_{Qn}(\max)} = \frac{2V_{CC}}{\pi}$$

The average power delivered to the load is

$$\bar{P}_L = \frac{1}{2} \cdot \frac{V_p^2}{R_L}$$

Since the current supplied by each power supply is half a sine wave, the average current is $V_p/(\pi R_L)$. The average power supplied by each source is therefore

$$\bar{P}_{S+} = \bar{P}_{S-} = V_{CC}\left(\frac{V_p}{\pi R_L}\right)$$ and the total average power supplied by the two sources is $$\bar{P}_S = 2V_{CC}\left(\frac{V_p}{\pi R_L}\right)$$

Then, the conversion efficiency is:

$$\eta = \frac{\frac{1}{2} \cdot \frac{V_p^2}{R_L}}{2V_{CC}\left(\frac{V_p}{\pi R_L}\right)} = \frac{\pi}{4} \cdot \frac{V_p}{V_{CC}}$$

The maximum possible efficiency, which occurs when $V_p = V_{CC}$, is $\eta(\max) = \frac{\pi}{4} \Rightarrow 78.5\%$

This maximum efficiency value is substantially larger than that of the standard class-A amplifier. we find the maximum possible average power that can be delivered to the load, as follows:

$$\bar{P}_L(\max) = \frac{1}{2} \cdot \frac{V_{CC}^2}{R_L}$$

The actual conversion efficiency obtained in practice is less than the maximum value because of other circuit losses, and because the **peak output voltage must remain less than V_{CC} to avoid transistor saturation**. As the output voltage amplitude increases, output signal distortion also increases. To limit this distortion to an acceptable level, the peak output voltage is usually limited to several volts below V_{CC} .we have seen that the maximum transistor power dissipation occurs when $V_p = 2V_{CC}/\pi$. At this peak output voltage, the conversion efficiency of the class-B amplifier is:

$$\eta = \frac{\pi}{4V_{CC}} \cdot V_p = \left(\frac{\pi}{4V_{CC}}\right) \cdot \left(\frac{2V_{CC}}{\pi}\right) = \frac{1}{2} \Rightarrow 50\%$$

Example:

For an Idealised class B output stage PA (turns on at 0 V and the saturation voltages for devices A and B is zero) V_+ and V_- are set to +5 and -5 volts consequently. Then:

1) What is the peak output voltage that maximises the power conversion efficiency.

Answer: $V_{OP} = V_{CC} = 5$ volts (zero voltage drop on devices at saturation)

2) What is the peak output voltage when each device dissipated the maximum power ?

Answer: $P_{MAX} = V_{CC}^2 /(\pi^2 R_L)$ at which output voltage is $V_{OP}= 2V_{cc}/ \pi = 10/ \pi = 3.18V$

3) Maximum allowed power in each device is 2W and output voltage is max, what is the smallest allowed R_L permitted value?

Answer: $P_{Qn}(Max) = V_{CC}^2 /(\pi^2 RL)$ ➔

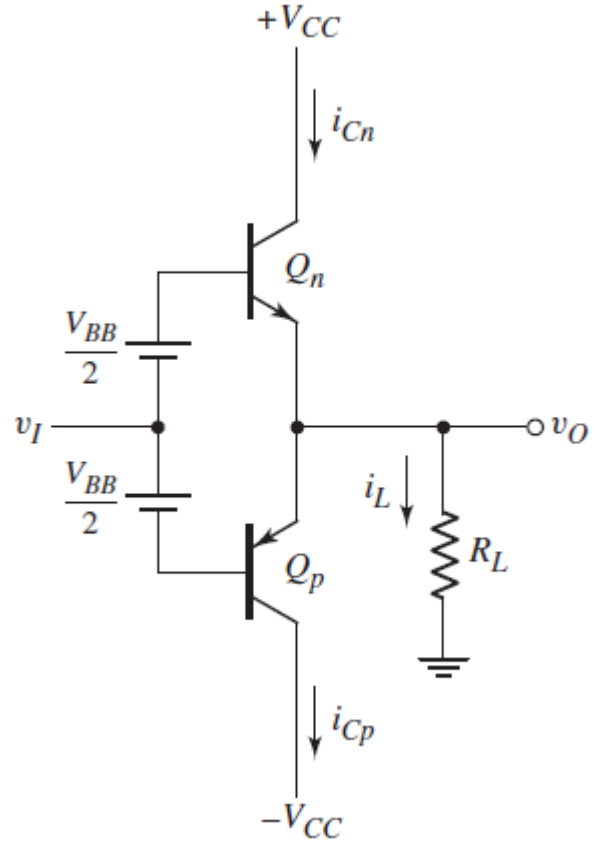
$2=25 /(\pi^2 RL)$

$R_{Lmin} = 1.266$ Ohms

Class AB Power Amplifier

Crossover distortion can be virtually eliminated by applying a small quiescent bias on each output transistor, for a zero input signal. This is called a class-AB output stage and is shown schematically next figure. If Q_n and Q_p are matched, then for $v_I = 0$, $V_{BB}/2$ is applied to the B–E junction of Q_n, $V_{BB}/2$ is applied to the E–B junction of Q_p, and $v_O = 0$. The quiescent collector currents in each transistor are given by:

$$i_{Cn} = i_{Cp} = I_S e^{V_{BB}/2V_T}$$



➔ As v_I increases, the voltage at the base of Q_n increases and v_O increases. Transistor Q_n operates as an emitter follower, supplying the load current to R_L. The output voltage is given by

$$v_O = v_I + \frac{V_{BB}}{2} - v_{BEn}$$

and the collector current of Q_n (neglecting base currents) is

$$i_{Cn} = i_L + i_{Cp}$$

Since i_{Cn} must increase to supply the load current, V_{BEn} increases. Assuming V_{BB} remains constant, as V_{BEn} increases, V_{EBp} decreases resulting in a decrease in i_{Cp}.

As v_I goes negative, the voltage at the base of Q_p decreases and v_O decreases. Transistor Q_p operates as an emitter follower, sinking current from the load. As i_{Cp} increases, v_{EBp} increases, causing a decrease in v_{BEn} and i_{Cn}.

Figure (a) shows the voltage transfer characteristics for this class-AB output stage. If v_{BEn} and v_{EBp} do not change significantly, then the voltage gain, or the slope of the transfer curve, is essentially unity.

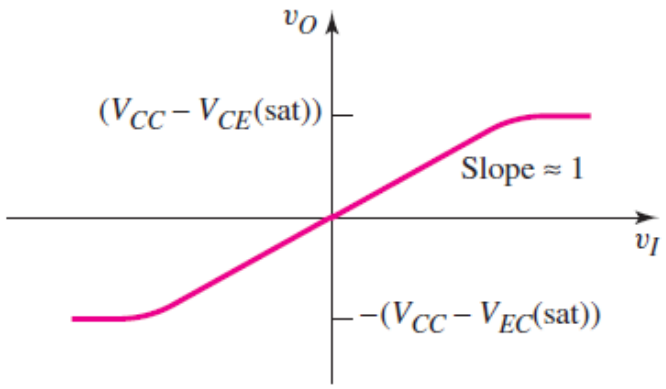
A sinusoidal input signal voltage and the resulting collector currents and load current are shown in Figures (b), (c), and (d).

Each transistor conducts for more than one-half cycle, which is the definition of class-AB operation.

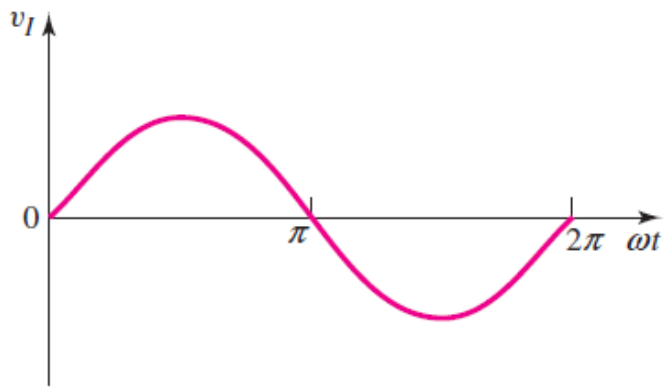
There is a relationship between i_{Cn} and i_{Cp}. We know that: $v_{BEn} + v_{EBp} = V_{BB}$

which can be written

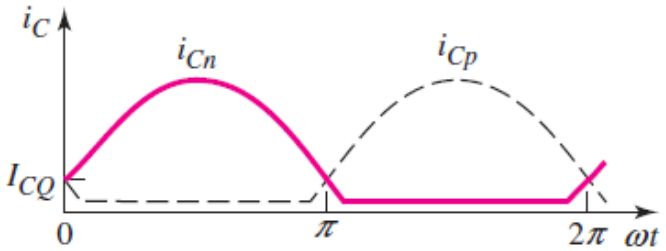
$$V_T \ln\left(\frac{i_{Cn}}{I_S}\right) + V_T \ln\left(\frac{i_{Cp}}{I_S}\right) = 2V_T \ln\left(\frac{I_{CQ}}{I_S}\right)$$



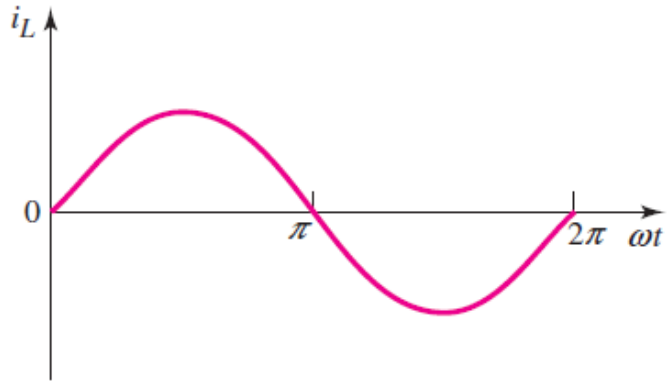
(a)



(b)



(c)



(d)

Combining terms in Equation , we find: $i_{Cn} i_{Cp} = I_{CQ}^2$

The product of i_{Cn} and i_{Cp} is a constant; therefore, if i_{Cn} increases, i_{Cp} decreases, but does not go to zero.

➔ Since, for a zero input signal, quiescent collector currents exist in the output transistors, the average power supplied by each source and the average power dissipated in each transistor are larger than for a class-B configuration.

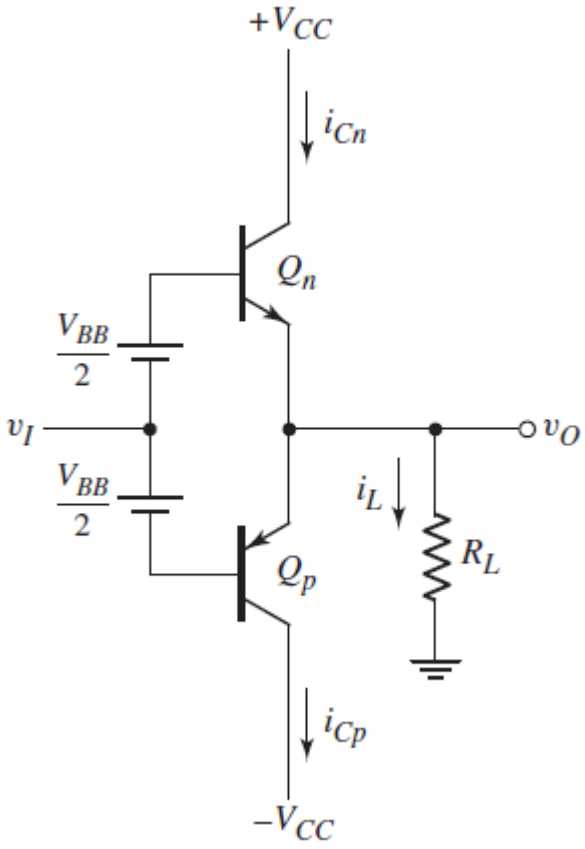
➔ This means that the power conversion efficiency for a class-AB output stage is less than that for an idealized class-B circuit. In addition, the required power handling capability of the transistors in a class-AB circuit must be slightly larger than in a class-B circuit.

➔ However, since the quiescent collector currents I_{CQ} are usually small compared to the peak current, this increase in power dissipation is not great. The advantage of eliminating crossover distortion in the class-AB output stage greatly outweighs the slight disadvantage of reduced conversion efficiency and increased power dissipation.

Example : A simplified class-AB output stage with BJTs is shown next figure. The circuit parameters are V_{CC} = 5 V and R_L = 1 k. For each transistor, I_S = 2 × 10^{-15} A.

(a) Determine the value of V_{BB} that produces $i_{Cn} = i_{Cp}$ = 1 mA when v_I = 0. What is the power dissipated in each transistor?

(b) For v_O = −3.5 V, determine i_L, i_{Cn}, i_{Cp}, and v_I. What is the power dissipated in Q_n, Q_p, and R_L?



(a) : i_{Cn} i_{Cp} = i^2_{CQ} ➔ i_{CQ} = 1 mA

VBB = 2VT Ln (1 × 10^{-3} / 2 × 10^{-15})= 1.4008 Volts

At v_I = 0 , then v_O = 0, ➔ $V_{CE} = V_{CC} - V_O = V_{CC}$ = 5 volts

$P_{Qn} = i_{CQ} \cdot V_{CE} = 5\ mW = P_{Qp}$

(b) : if VO = -3.5 volts, find i_L, i_{Cn}, i_{Cp} and v_I. *Also find the* power dissipated in Q_n, Q_p, and R_L

$i_L = -(V_O/R_L) = (-3.5/R_L)$ *(This means that QP is pulling the current from RL)*

$i_{CP} . i_{CN} = I_{CQ}^2$ ➔ $i_{CN} = (I_{CQ}^2/i_{CP}) = (1 \times 10^{-3}/i_{CP})$

But $i_{CP} = i_{CN} + i_{RL}$

$i_{CP} = (1 \times 10^{-3}/i_{CP}) + (3.5 \times 10^{-3})$

$i_{CP}^2 - (3.5 \times 10^{-3})\, i_{CP} - (1 \times 10^{-3})^2 = 0$

$$i_{CP} = \frac{(3.5 \times 10^{-3}) \pm \sqrt{(3.5 \times 10^{-3})^2 - 4(1)(1 \times 10^{-3})^2}}{2}$$

$$= \frac{(3.5 \times 10^{-3}) \pm 4.031 \times 10^{-3}}{2}$$ *one positive and another negative answers.*

$i_{CP} = 3.766\ mA$

$i_{CN} = (ICQ2) / (3.766 \times 10^{-3})$

$= (1 \times 10^{-3})^2 / (3.766 \times 10^{-3}) = 0.266\ mA$

$$V_{EB} = \ln \frac{3.766 \times 10^{-3}}{(2 \times 10^{-15})} \times 0.026 = 0.735\ Volt$$

$V_{BE} = 1.4008 - 0.735 = 0.666\ Volts$

$$V_I = V_O - V_{EB} + \frac{V_{BB}}{2} = -3.5 - 0.735 - \frac{1.4008}{2} = -3.534\ Volts$$

$P_{QN} = i_{CN} V_{CEn}$

$V_{CEn} = V_{CC} - V_O = 5 - (-3.5) = 8.5\ V$

$P_{Qn} = (8.5)\ (0.266 \times 10^{-3}) = 2.261\ mW$

$V_{ECp} = V_O + 5 = -3.5 + 5 = 1.5\ Volts$

$P_{Qp} = i_{CP} V_{CEp} = 3.766 \times 10^{-3}\ (1.5) = 5.649\ mW$

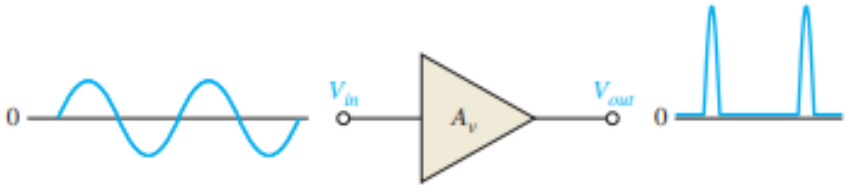
$$P_{RL} = \frac{V_o^2}{R_L} = \frac{(3.5)^2}{1\ K} = 12.25\ mW$$

Class C Operation

➔ Class C amplifiers are biased so that conduction occurs for much less than 180 degrees .

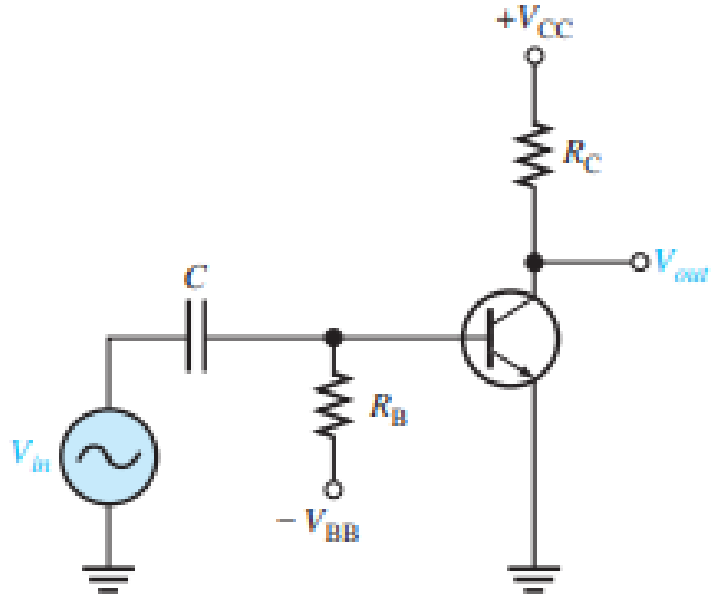
➔ Class C amplifiers are more efficient than either class A or push-pull class B and class AB, which means that more output power can be obtained from class C operation.

➔ The output amplitude is a nonlinear function of the input, so class C amplifiers are not used for linear amplification. They are generally used in radio frequency (RF) applications, including circuits, such as oscillators, that have a constant output amplitude, and modulators, where a high-frequency signal is controlled by a low-frequency signal.



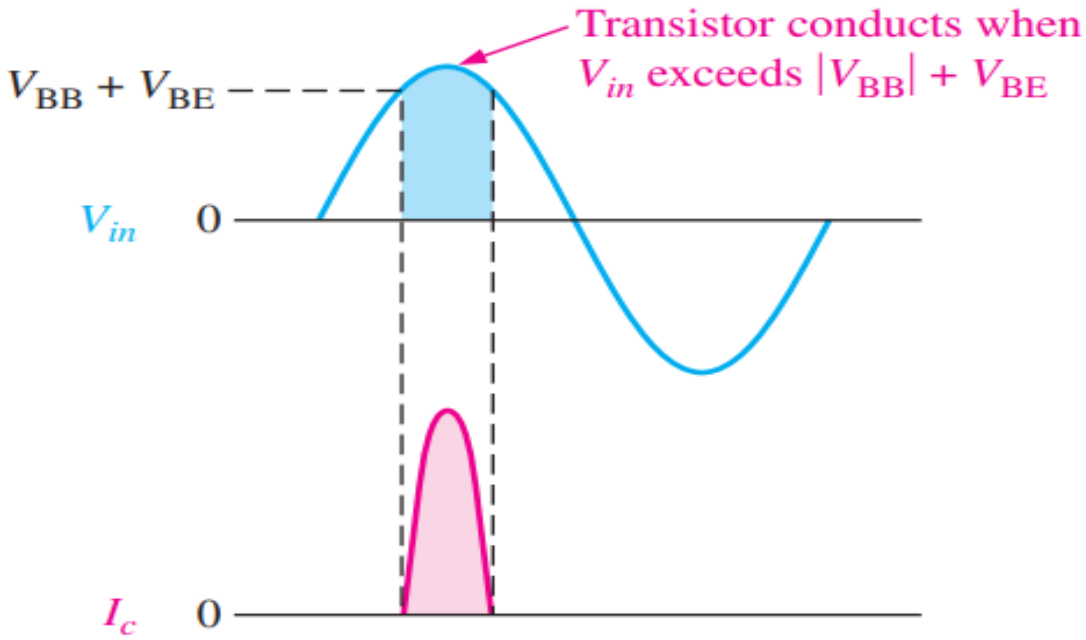
➔ Basic concept of class C Amplifier is shown next figure .

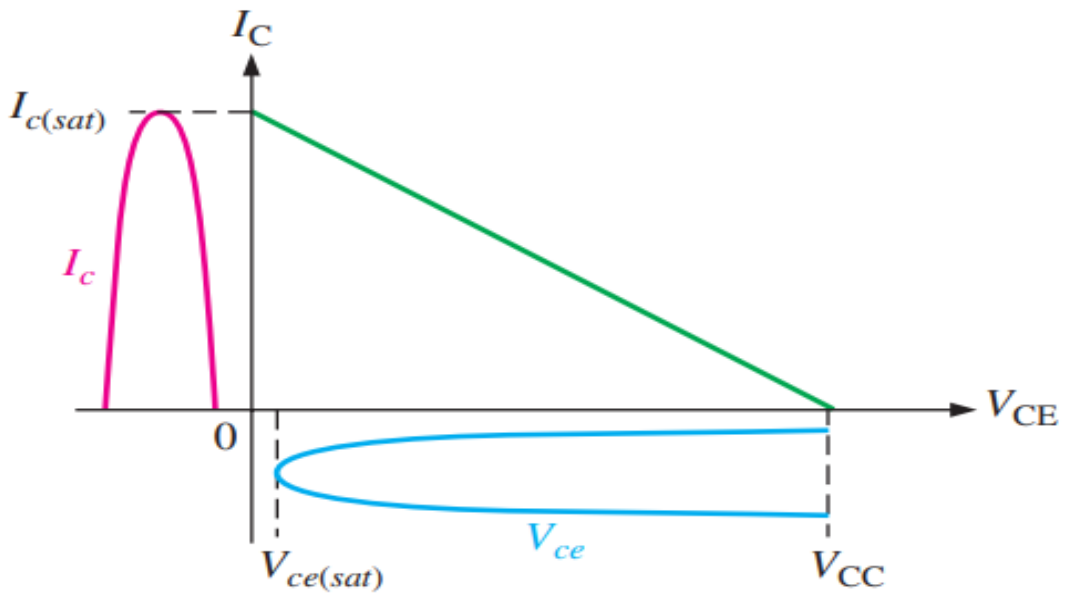
➔ A common-emitter class C amplifier with a resistive load is shown next figure. A class C amplifier is normally operated with a resonant circuit load, so the resistive load is used only for the purpose of illustrating the concept. It is biased below cutoff with the negative VBB supply.

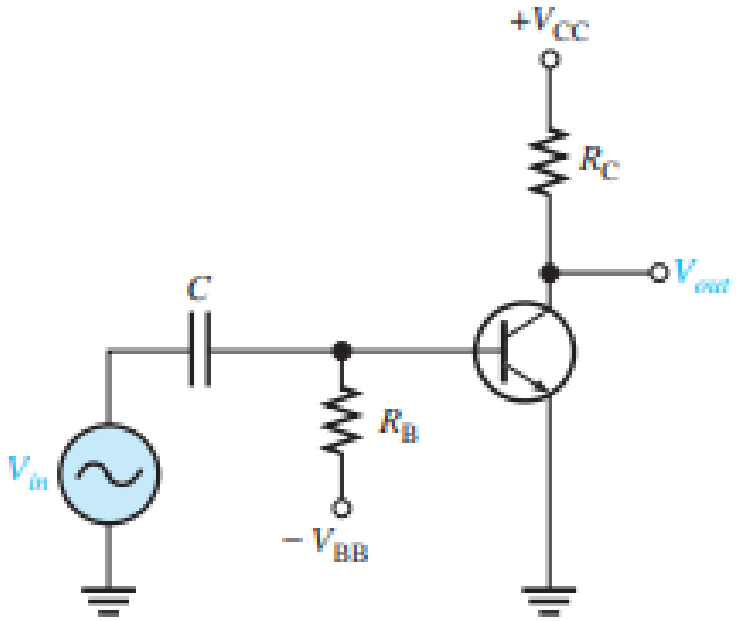


The ac source voltage has a peak value that is slightly greater than |VBB| + VBE so that the base voltage exceeds the barrier potential of the base-emitter junction for a short time near the positive peak of each cycle.

During this short interval, the transistor is turned on. When the entire ac load line is used, as shown in the lower figure, the ideal maximum collector current is Ic(sat), and the ideal minimum collector voltage is Vce(sat).





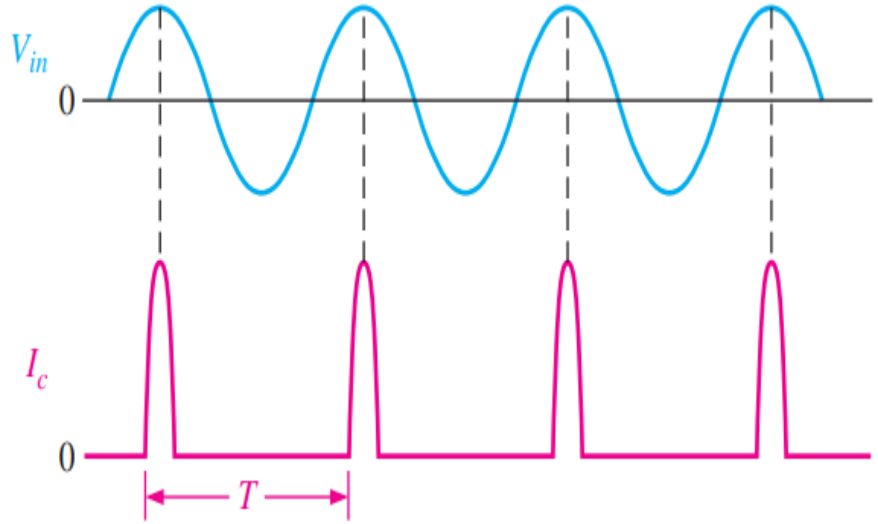


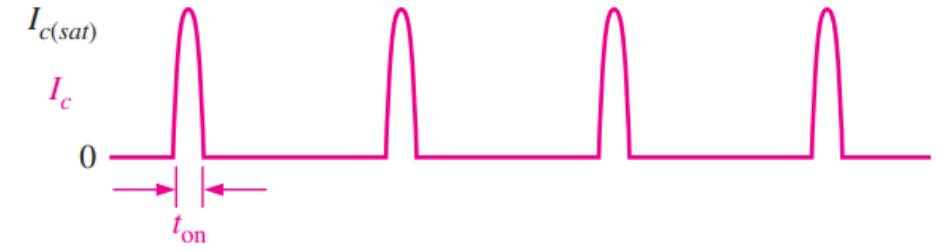
Power dissipation in Class C PA

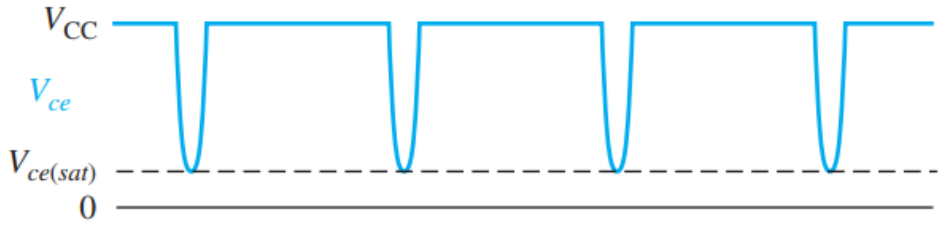
The power dissipation of the transistor in a class C amplifier is low because it is on for only a small percentage of the input cycle.

The upper figure shows the collector current pulses. The time between the pulses is the period (T) of the ac input voltage. The collector current and the collector voltage during the on time of the transistor are shown in the lower figure.

To avoid complex mathematics, we will assume ideal pulse approximations. Using this simplification, if the output swings over the entire load, the maximum current amplitude is Ic(sat) and the minimum voltage amplitude is Vce(sat) during the time the transistor is on.







The power dissipation during the on time is, therefore,

$$P_{\mathrm{D(on)}} = I_{c\,(sat)} V_{ce\,(sat)}$$

The transistor is on for a short time, t_{on}, and off for the rest of the input cycle. Therefore, assuming the entire load line is used, the power dissipation averaged over the entire cycle is

$$P_{\mathrm{D(avg)}} = \left(\frac{t_{\mathrm{on}}}{T}\right) P_{\mathrm{D(on)}} = \left(\frac{t_{\mathrm{on}}}{T}\right) I_{c\,(sat)} V_{ce\,(sat)}$$

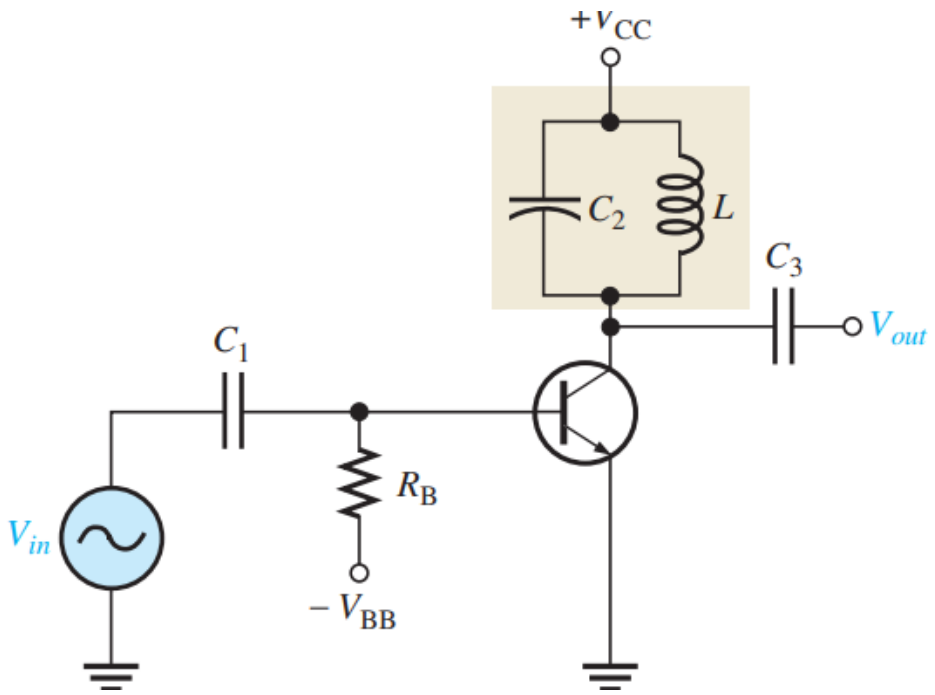
Class C with a Resonant Circuit

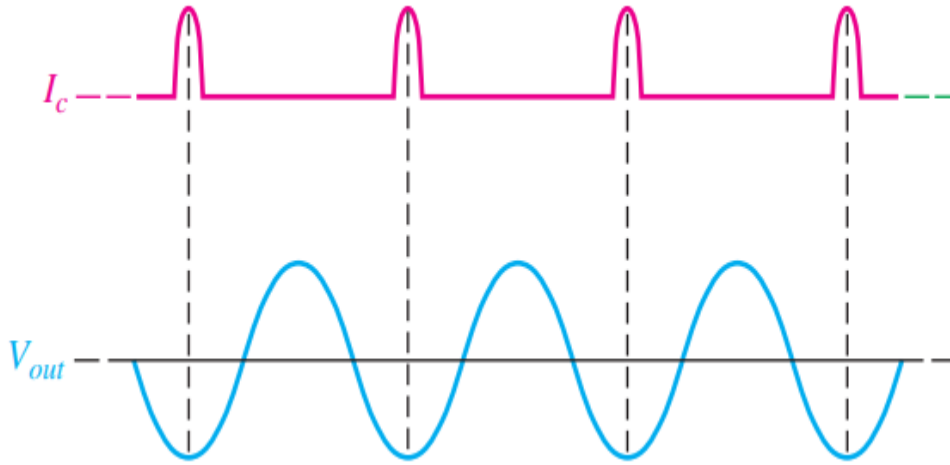
Because the collector voltage (output) is not a replica of the input, the resistively loaded class C amplifier alone is of no value in linear applications. It is therefore necessary to use a class C amplifier with a parallel resonant circuit (tank), as shown next figure.

The resonant frequency of the tank circuit is determined by the formula:

$$f_r = 1/(2\pi\sqrt{LC})$$

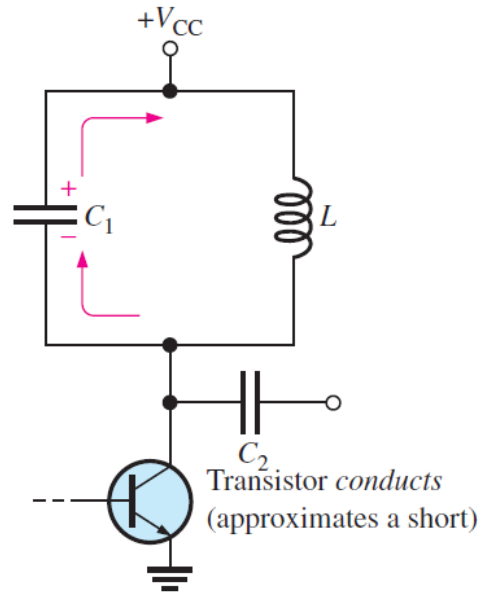
The short pulse of collector current on each cycle of the input initiates and sustains the oscillation of the tank circuit so that an output sinusoidal voltage is produced. The tank circuit has high impedance only near the resonant frequency, so the gain is large only at this frequency.



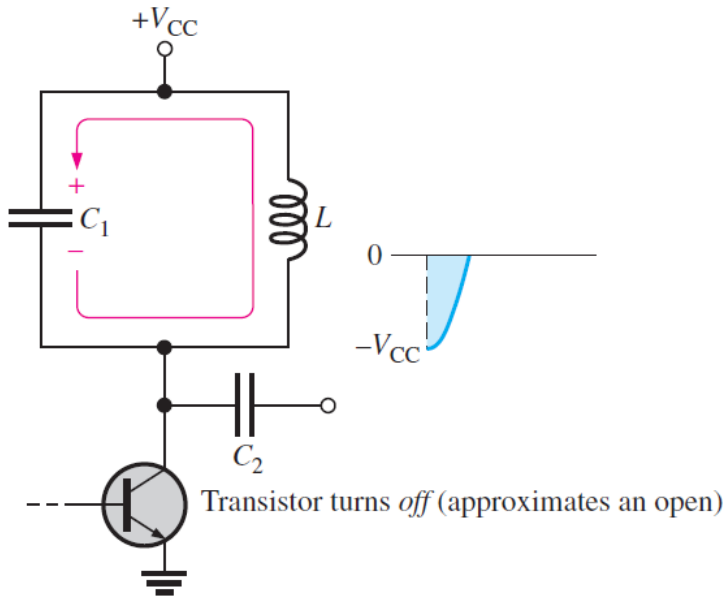


The current pulse charges the capacitor to approximately VCC. After the pulse, the capacitor quickly discharges, thus charging the inductor. Then, after the capacitor completely discharges, the inductor's magnetic field collapses and then quickly recharges C to near VCC in a direction opposite to the previous charge.

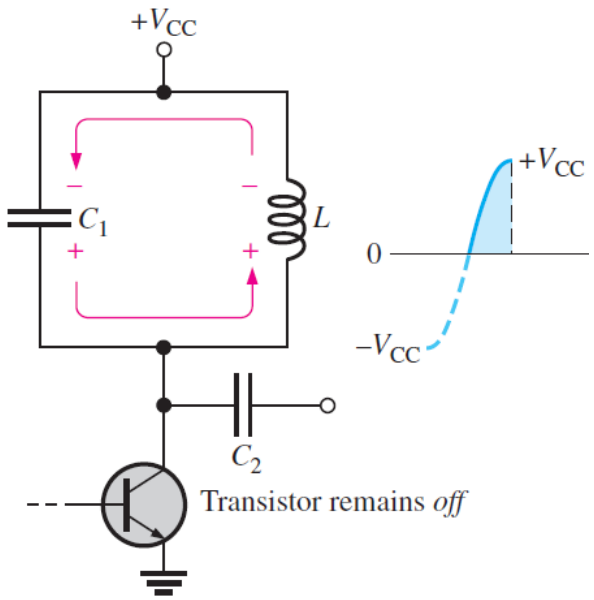
This completes one half-cycle of the oscillation, as shown in parts (b) and (c).



(a) C_1 charges to $+V_{CC}$ at the input peak when transistor is conducting.



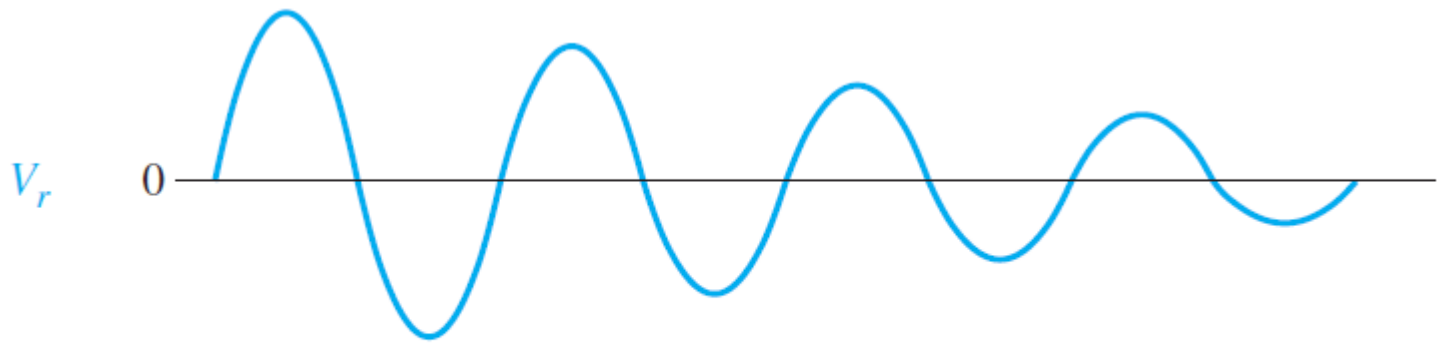
(b) C_1 discharges to 0 volts.



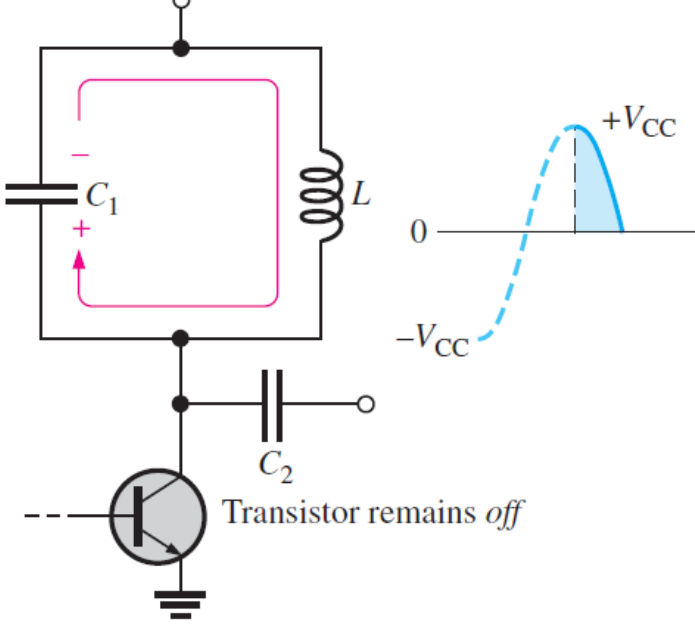
(c) L recharges C_1 in opposite direction.

Next, the capacitor discharges again, increasing the inductor's magnetic field. The inductor then quickly recharges the capacitor back to a positive peak slightly less than the previous one, due to energy loss in the winding resistance. This completes one full cycle, as shown in parts (d) and (e). The peak-to-peak output voltage is therefore approximately equal to 2VCC.

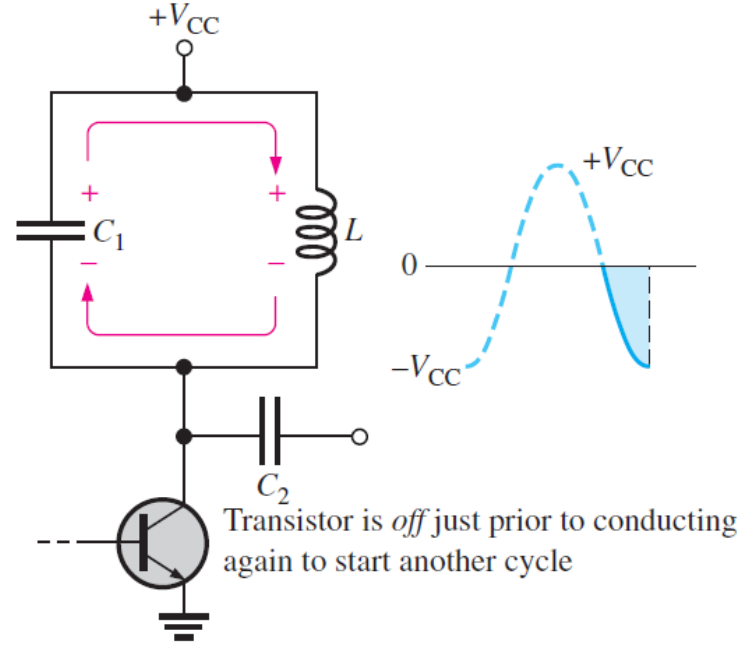
The amplitude of each successive cycle of the oscillation will be less than that of the previous cycle because of energy loss in the resistance of the tank circuit, as shown in the figure below, and the oscillation will eventually die out. However, the regular recurrences of the collector current pulse re-energizes the resonant circuit and sustains the oscillations at a constant amplitude.



(a) An oscillation will gradually die out (decay) due to energy loss. The rate of decay depends on the efficiency of the tank circuit.

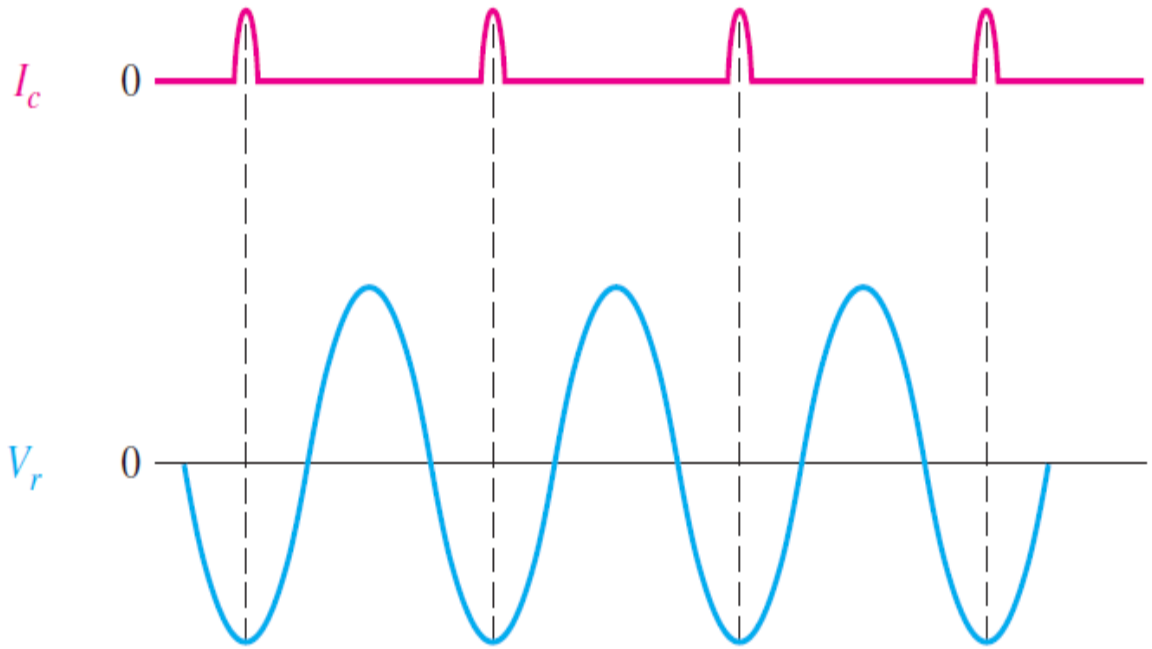


(d) C_1 discharges to 0 volts.

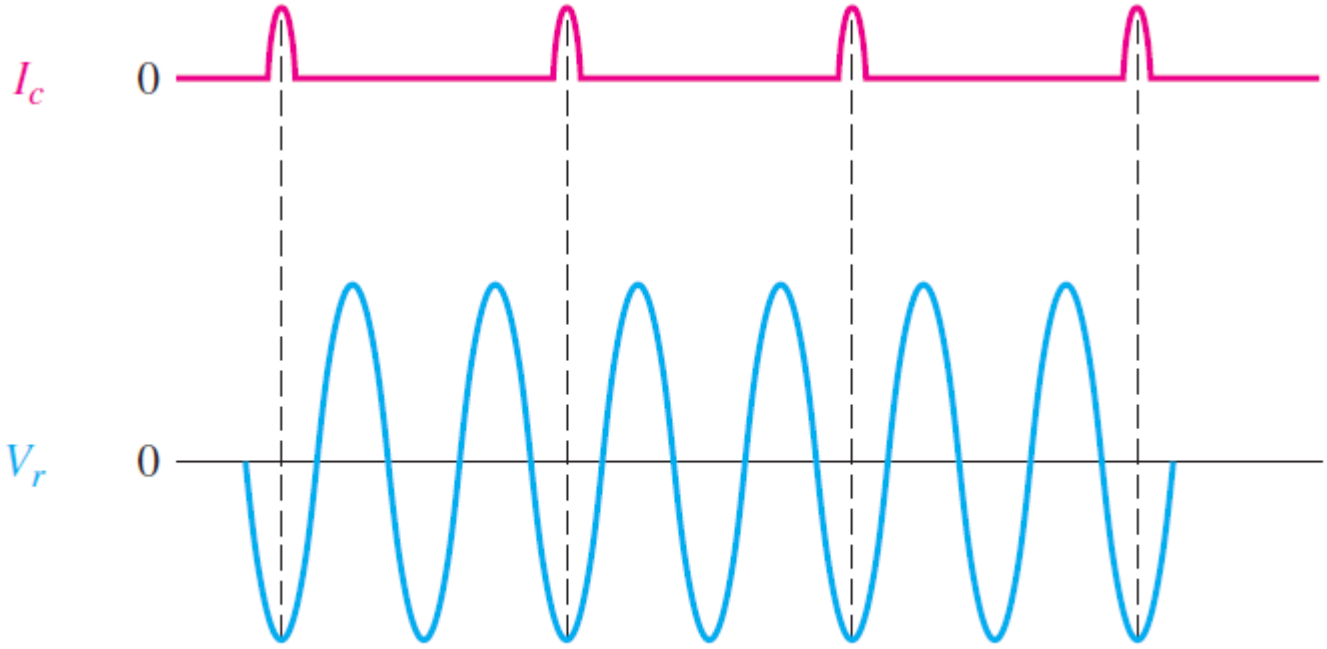


(e) L recharges C_1.

When the tank circuit is tuned to the frequency of the input signal (fundamental), reenergizing occurs on each cycle of the tank voltage, Vr, as shown in Figure (b). When the tank circuit is tuned to the second harmonic of the input signal, re-energizing occurs on alternate cycles as shown in Figure (c). In this case, a class C amplifier operates as a frequency multiplier (X 2). By tuning the resonant tank circuit to higher harmonics, further frequency multiplication factors are achieved.



(b) Oscillation at the fundamental frequency can be sustained by short pulses of collector current.



(c) Oscillation at the second harmonic frequency

Maximum Output Power

$$P_{out} = \frac{V_{rms}^2}{R_c} = \frac{(0.707V_{CC})^2}{R_c}$$

Since the voltage developed across the tank circuit has a peak-to-peak value c approximately $2V_{CC}$, the maximum output power can be expressed as ➔

$$\boldsymbol{P_{out} = \frac{0.5V_{CC}^2}{R_c}}$$

R_c is the equivalent parallel resistance of the collector tank circuit at resonance and represents the parallel combination of the coil resistance and the load resistance. It usually has a low value. The total power that must be supplied to the amplifier and the efficiency is ➔

$$P_T = P_{out} + P_{D(avg)}$$

$$\boldsymbol{\eta = \frac{P_{out}}{P_{out} + P_{D(avg)}}}$$

When $P_{out} >> P_{D(avg)}$, the class C efficiency closely approaches 1 (100 percent).

Example : A class C amplifier is driven by a 200 kHz signal. The transistor is on for 1 ms, and the amplifier is operating over 100 percent of its load line. If $I_{c(sat)}$ 100 mA and $V_{ce\,(sat)}$ 0.2 V, what is the average power dissipation of the transistor?

The period is : T =1/200 kHz = 5 ms

$P_{D(avg)} = (t_{on}/T)\ I_{c(sat)}V_{ce(sat)}$ = (0.2) (100 mA) (0.2 V) = **4 mW**

The low power dissipation of the transistor operated in class C is important because it leads to a very high efficiency when it is operated as a tuned class C amplifier in which relatively high power is achieved in the resonant circuit.

Suppose now that V_{CC} equal to 24 V and the R_c=100 Ohms determine the efficiency.

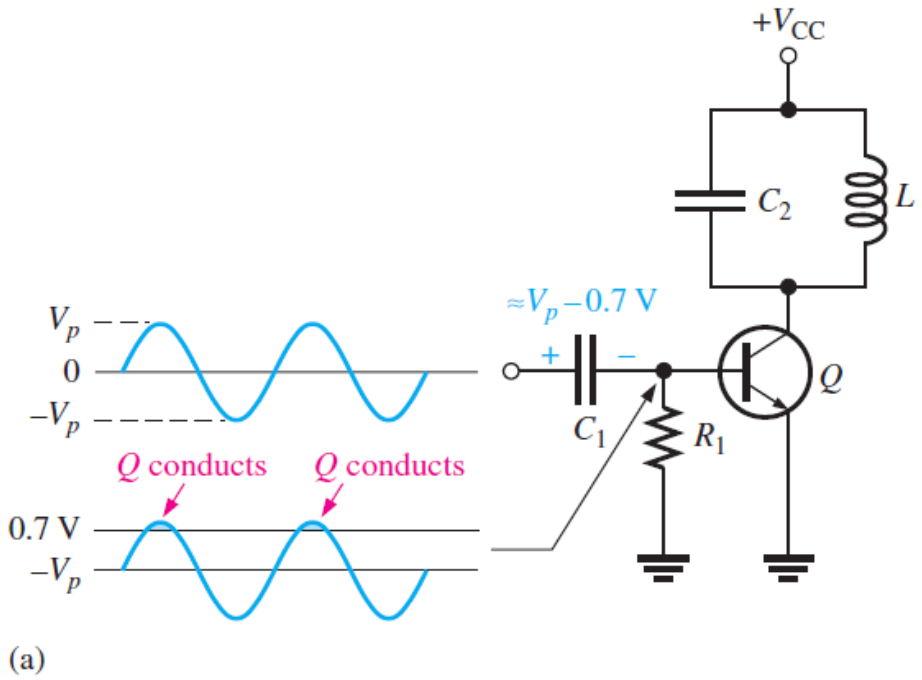
$P_{out} = 0.5V^2_{CC}/R_c = 0.5(24\ V)^2/100 = 2.88$ W

$\eta = P_{out} / (P_{out} + P_{D(avg)}) = 2.88$ W / (2.88 W + 4 mW) = **0.999**

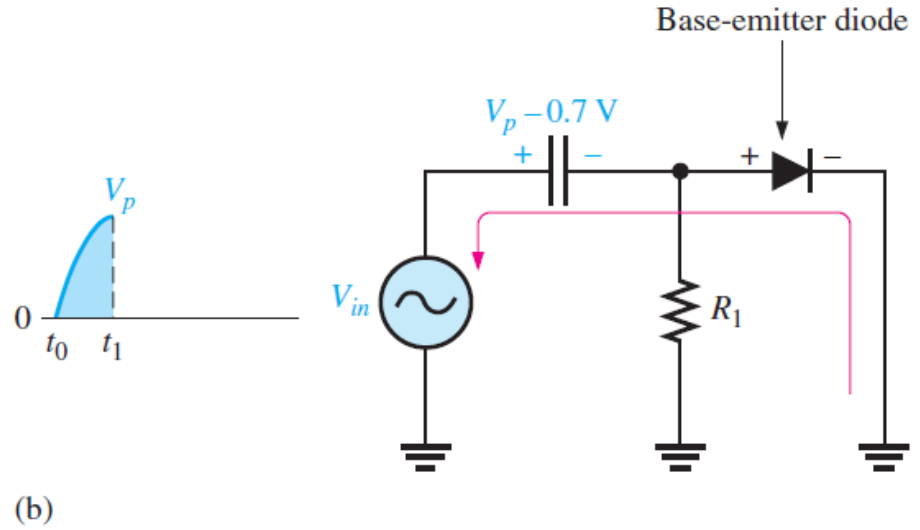
Clamper Bias for a Class C Amplifier

Next figure shows a class C amplifier with a base bias clamping circuit. The base-emitter junction functions as a diode.

When the input signal goes positive, capacitor C_1 is charged to the peak value with the polarity shown in Figure (a). This action produces an average voltage at the base of approximately –Vp This places the transistor in cut-off except at the positive peaks, when the transistor conducts for a short interval. For good clamping action, the R_1C_1 time constant of the clamping circuit must be much greater than the period of the input signal. Parts (b) through (f) of next figures illustrate the bias clamping action in more detail. During the time up to the positive peak of the input (t_0 to t_1), the capacitor charges to (Vp - 0.7) V through the base-emitter diode, as shown in part (b).

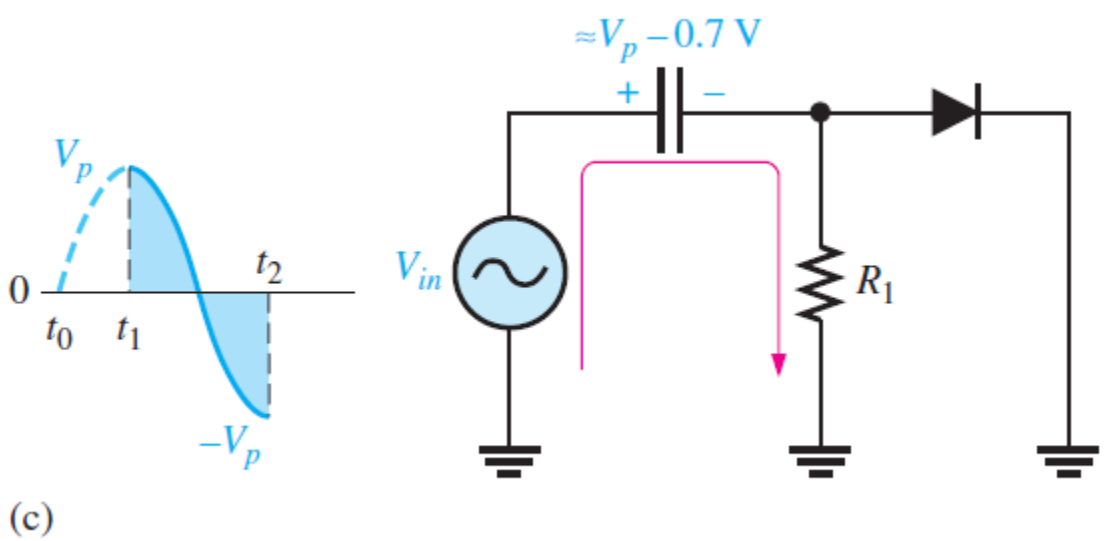


(a)

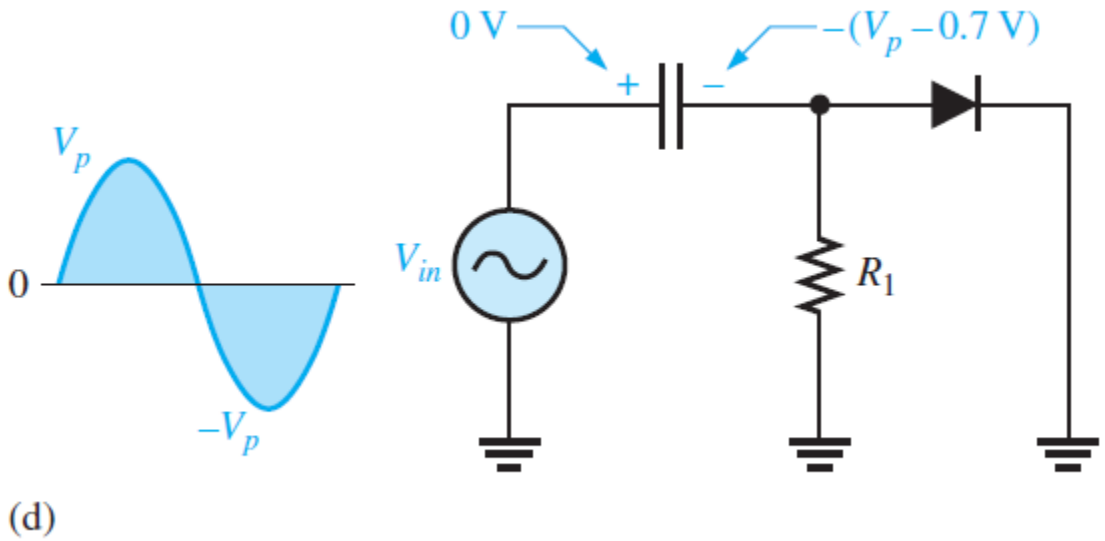


(b)

During the time from t_1 to t_2, as shown in part (c), the capacitor discharges very little because of the large *RC* time constant. The capacitor, therefore, maintains an average charge slightly less than (Vp - 0.7) V.



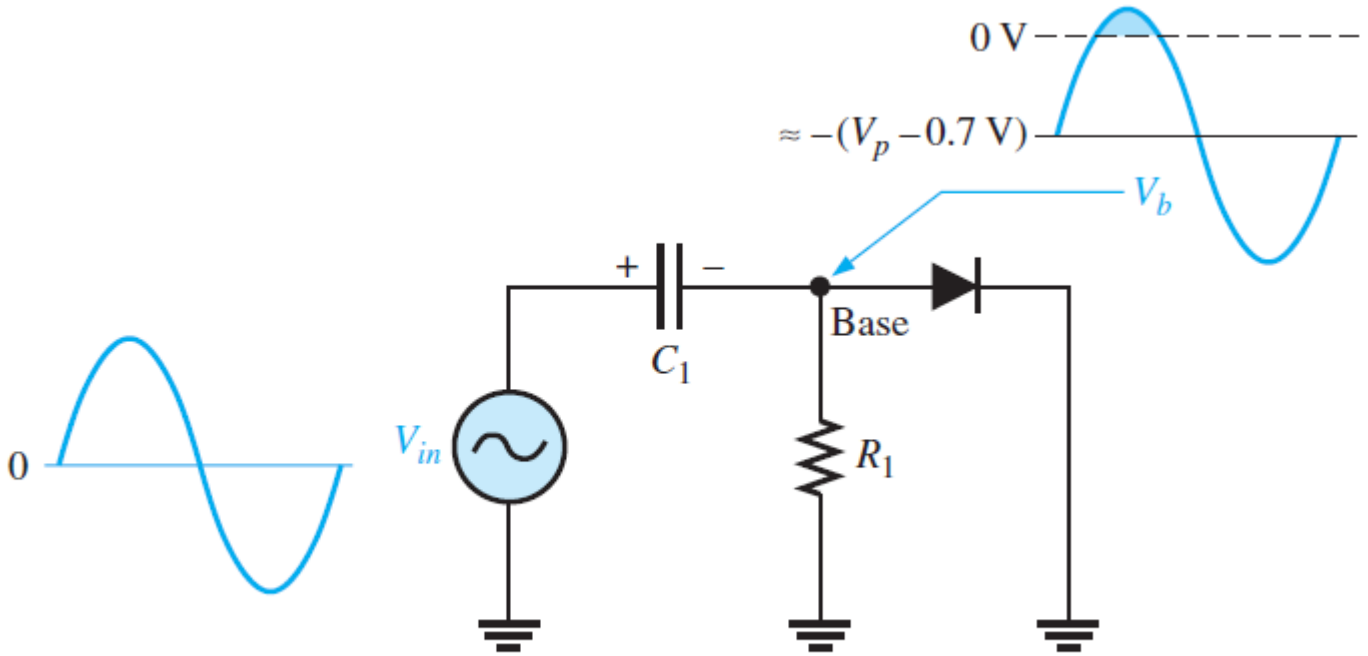
(c)



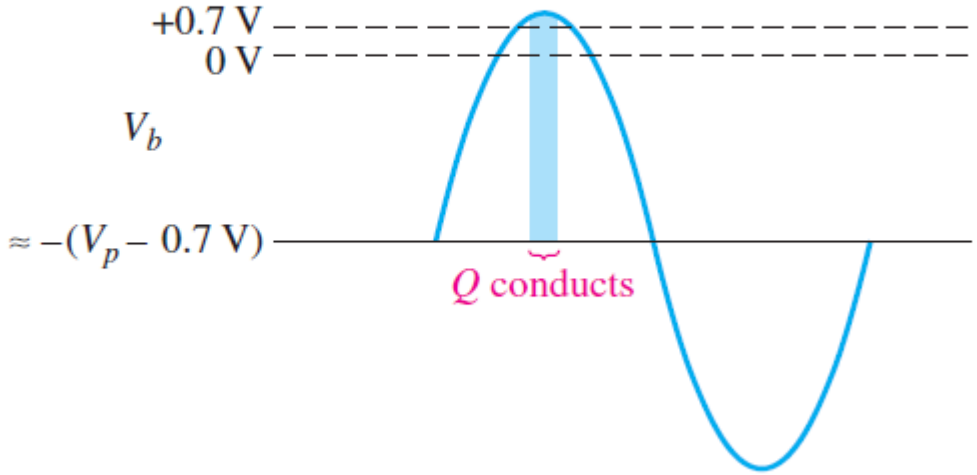
(d)

Since the dc value of the input signal is zero (positive side of C_1), the dc voltage at the base (negative side of C_1) is slightly more positive than -(V_p - 0.7 V), as indicated in Figure (d).

As shown in Figure (e), the capacitor couples the ac input signal through to the base so that the voltage at the transistor's base is the ac signal riding on a dc level slightly more positive than -(V_p - 0.7) V. Near the positive peaks of the input voltage, the base voltage goes slightly above 0.7 V and causes the transistor to conduct for a short time, as shown in (f).



(e)



(f)

Example : Determine the voltage at the base of the transistor, the resonant frequency, and the peakto-peak value of the output signal voltage for the class C amplifier in next figure.

$V_{s(p)} = (1.414)(1\text{ V})$ 1.4 V

The base is clamped at $-(V_{s(p)} - 0.7) =$ **0.7 V dc**

The signal at the base has a positive peak of +0.7 V and a negative

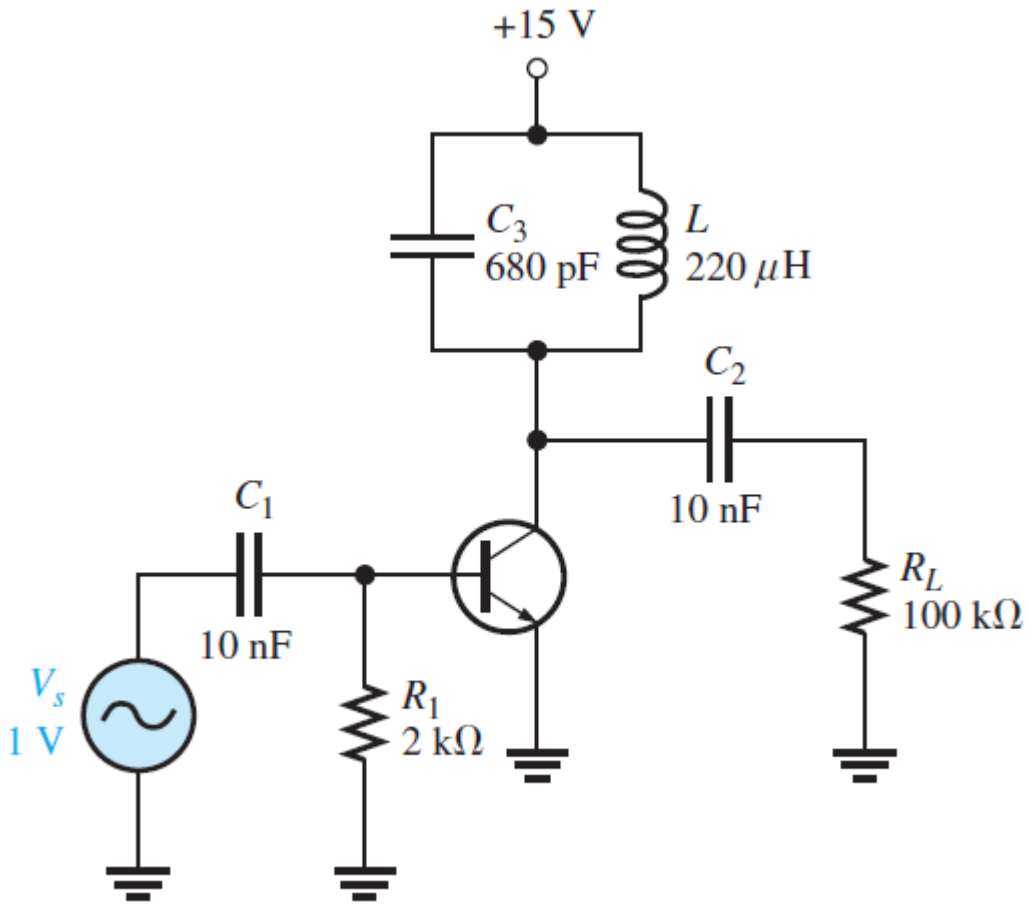
$-V_{s(p)} + (-0.7\text{ V}) = -1.4\text{ V} - 0.7\text{ V} =$ **2.1 V**

The resonant frequency is

$$f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{220\text{ mH}\ 680\text{ pF}}} = \textbf{411 kHz}$$

The output signal has a peak-to-peak value of

$V_{pp} = 2V_{CC} = 2(15\text{ V}) =$ **30 V**



Class D, E and F Power Amplifiers

Another classification of power amplifiers, including class D, class E, and class F, uses the output transistors as switches. The output of the amplifier is, in general, a high-Q resonant RLC circuit.

When the switch is closed, current and power are supplied to the output resonant circuit. In the ideal case, when the switch is closed, there is zero voltage across the switch, and when the switch is open, there is zero current through the switch. In both cases, the ideal power dissipated in the switch is zero. The power efficiency of these amplifiers can then approach 100 percent.

Because of their extremely high input resistance and low noise, FET amplifiers are a good choice for certain applications, such as amplifying low-level signals in the first stage of a communication receiver. FETs also have the advantage in certain power amplifiers and in switching circuits because biasing is simple and more efficient. The standard amplifier configurations are common-source (CS), common-drain (CD) and common-base (CB), which are analogous to CE, CC, and CB configurations of BJTs.

Class D Power Amplifier

FETs can be used in any of the amplifier types introduced earlier (class A, class B, and class C). In some cases, the FET circuit will perform better; in other cases, the BJT circuit is superior because BJTs have higher gain and better linearity. Another type of amplifier (class D) is introduced in this chapter because FETs are always superior to BJTs in class D and you will rarely see BJTs used in class D.

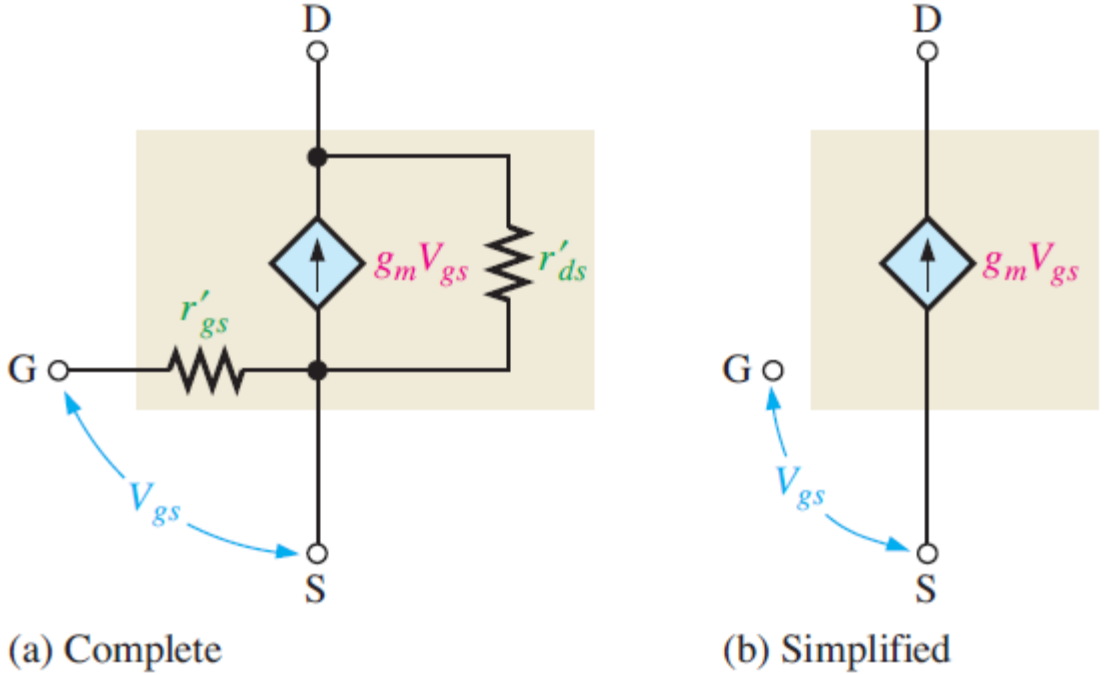
The class D amplifier is a switching amplifier that is normally either in cutoff or saturation. It is used in analog power amplifiers with a circuit called a pulse-width modulator

FETs are superior to BJTs in nearly all switching applications. Various switching circuits—analog switches, analog multiplexers, and switched capacitors—are discussed. In addition, common digital switching circuits are introduced using CMOS (complementary MOS).

THE COMMON-SOURCE AMPLIFIER

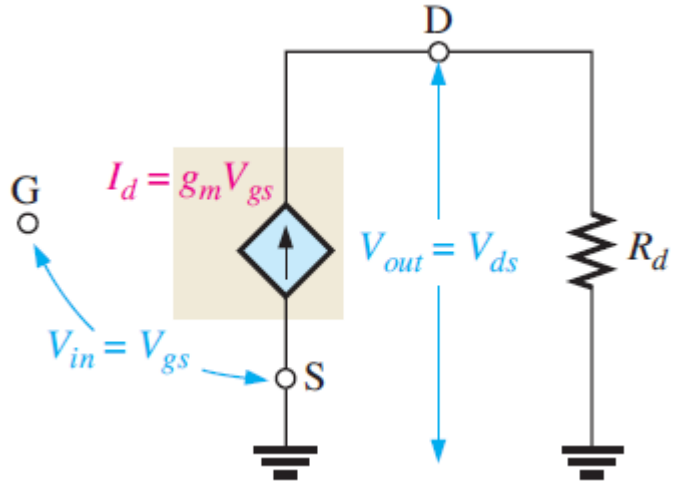
The common-source (CS) amplifier is comparable to the common-emitter BJT amplifier that we presented before.

An equivalent FET model is shown in Figure a. the internal resistance, appears between the gate and source, and a current source equal to $gmVgs$ appears between the drain and source. Also, the internal drain-to-source resistance, is included. In part (b), a simplified ideal model is shown. The resistance, is assumed to be extremely large so that an open circuit between the gate and source can be assumed. Also, is assumed large enough to neglect.



An ideal FET circuit model with an external ac drain resistance is shown in in the lower figure. The ac voltage gain of this circuit is Vou_t/Vin, where $Vin = Vgs$ and $Vout = Vds$. The voltage gain expression is :

$$A_v = \frac{V_{ds}}{V_{gs}}$$



From the equivalent circuit,

$$V_{ds} = I_d R_d$$

and from the definition of transconductance, $g_m = I_d / V_{gs}$,

$$V_{gs} = \frac{I_d}{g_m}$$

Substituting the two preceding expressions into the equation for voltage gain yields

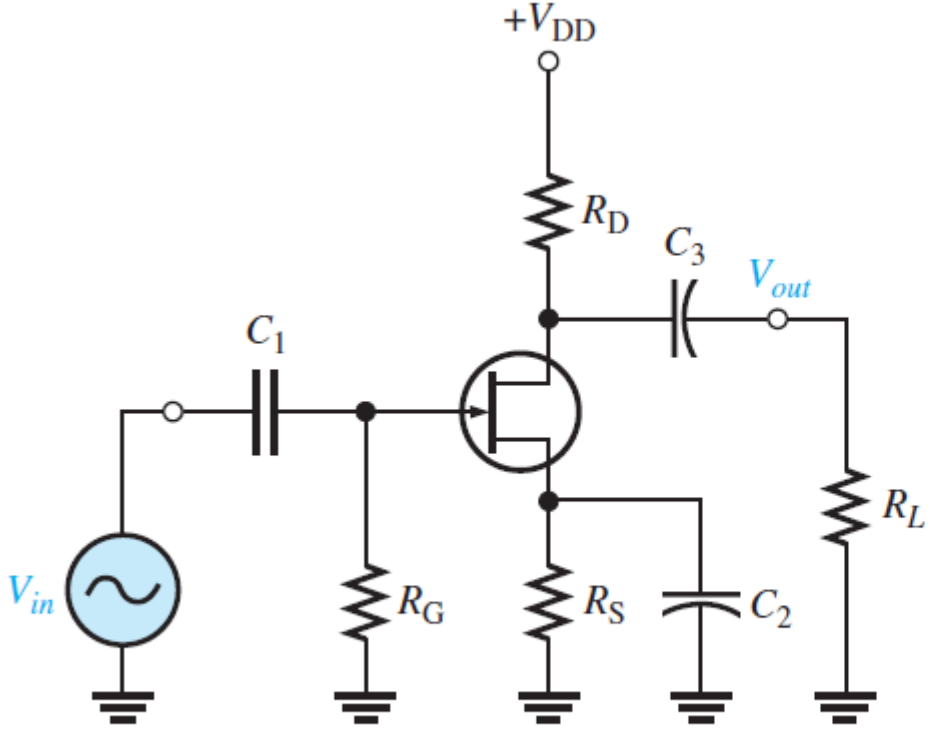
$$A_v = \frac{I_d R_d}{I_d / g_m} = \frac{g_m I_d R_d}{I_d}$$

$$\boldsymbol{A_v = g_m R_d}$$

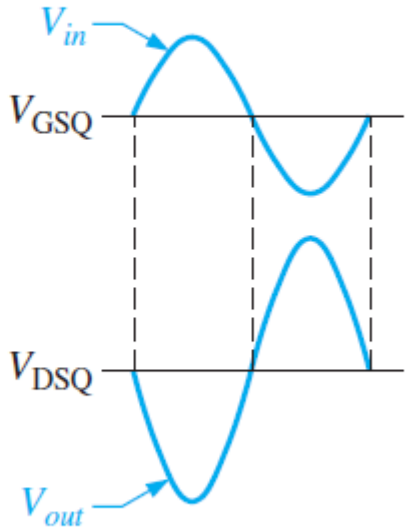
JFET Amplifier Operation

In a **common-source** JFET amplifier the source terminal is common to both the input and output signal. A common-source amplifier either has no source resistor or has a bypassed source resistor, so the source is connected to ac ground. A self-biased common-source *n*-channel JFET amplifier with an ac source capacitively coupled to the gate is shown in Figure (a). The resistor, R_G, serves two purposes: It keeps the gate at approximately 0 V dc (because I_{GSS} is extremely small), and its large value (usually several megohms) prevents loading of the ac signal source. A bias voltage is produced by the drop across R_S. The bypass capacitor, C_2, keeps the source of the JFET at ac ground.

The input signal voltage causes the gate-to-source voltage to swing above and below its Q-point value (V_{GSQ}), causing a corresponding swing in drain current. As the drain current increases, the voltage drop across R_D also increases, causing the drain voltage to decrease. The drain current swings above and below its Q-point value in phase with the gate-to-source voltage. The drain-to-source voltage swings above and below its Q-point value (V_{DSQ}) and is 180° out of phase with the gate-to-source voltage, as illustrated in Figure (b).

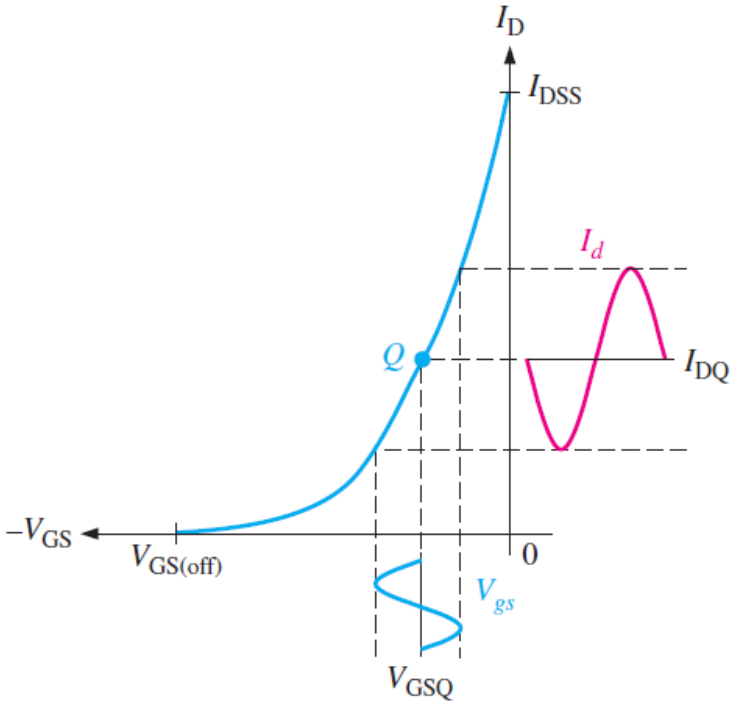


(a) Schematic

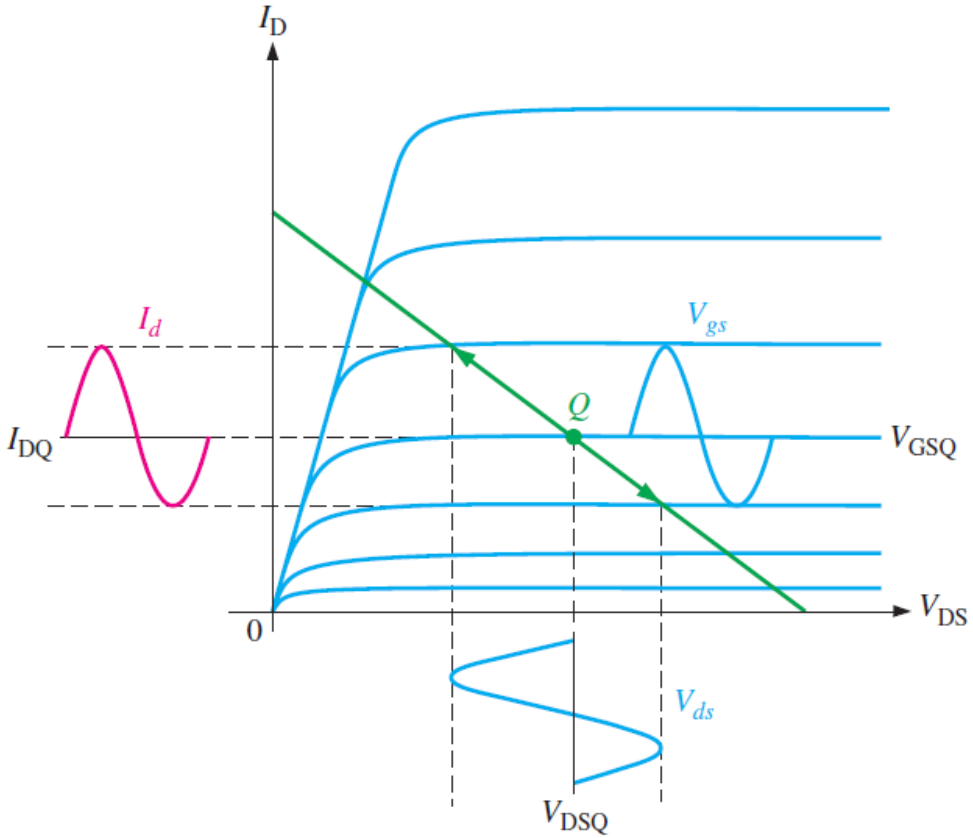


(b) Voltage waveform relationship

Part (a) shows how a sinusoidal variation, V_{gs}, produces a corresponding sinusoidal variation in I_d. As V_{gs} swings from its Q-point value to a more negative value, I_d decreases from its Q-point value. As V_{gs} swings to a less negative value, I_d increases. Figure (b) shows a view of the same operation using the drain curves. The signal at the gate drives the drain current above and below the Q-point on the load line, as indicated by the arrows. Lines projected from the peaks of the gate voltage across to the I_D axis and down to the V_{DS} axis indicate the peak-to-peak variations of the drain current and drain-to-source voltage, as shown. Because the transfer characteristic curve is nonlinear, the output will have some distortion. This can be minimized if the signal swings over a limited portion of the load line.



(a) JFET (*n*-channel) transfer characteristic curve showing signal operation

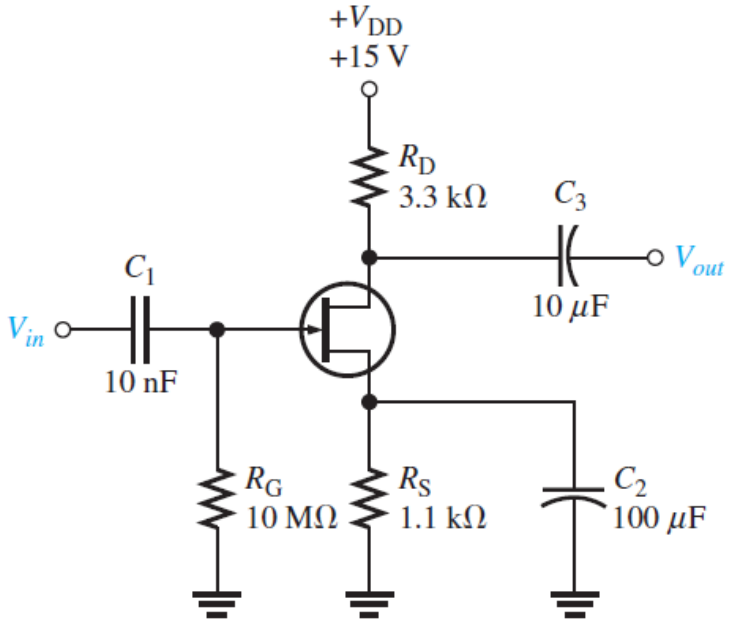


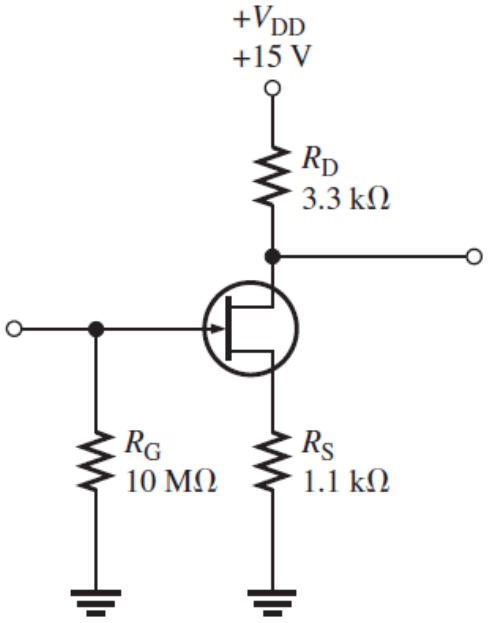
(b) JFET (*n*-channel) drain curves showing signal operation

DC Analysis

The first step in analyzing a JFET amplifier is to determine the dc conditions including I_D and V_S. I_D determines the Q-point for an amplifier and enables you to calculate V_D, so it is useful to determine its value. It can be found either graphically or mathematically. The graphical approach using the transconductance curve, will be applied to an amplifier here. To simplify the dc analysis, the equivalent circuit is shown in lower right figure;

Graphical Approach **T**he JFET universal transfer characteristic (transconductance curve) illustrates the relationship between the output current and the input voltage. The endpoints of the transconductance curve are at I_{DSS} and $V_{GS(off)}$. A dc graphical solution is done by plotting the load line (for the self-biased case shown) on the same plot and reading the values of V_{GS} and I_D at the intersection of these plots (Q-point).

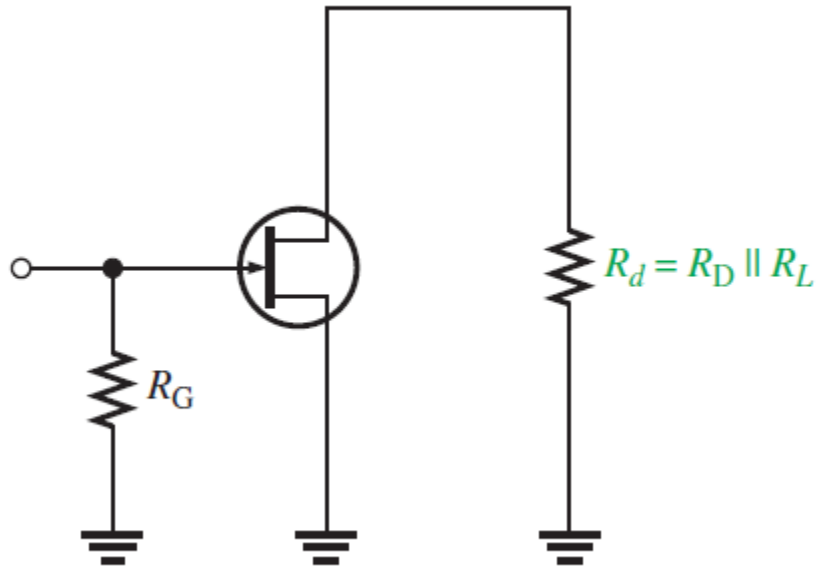




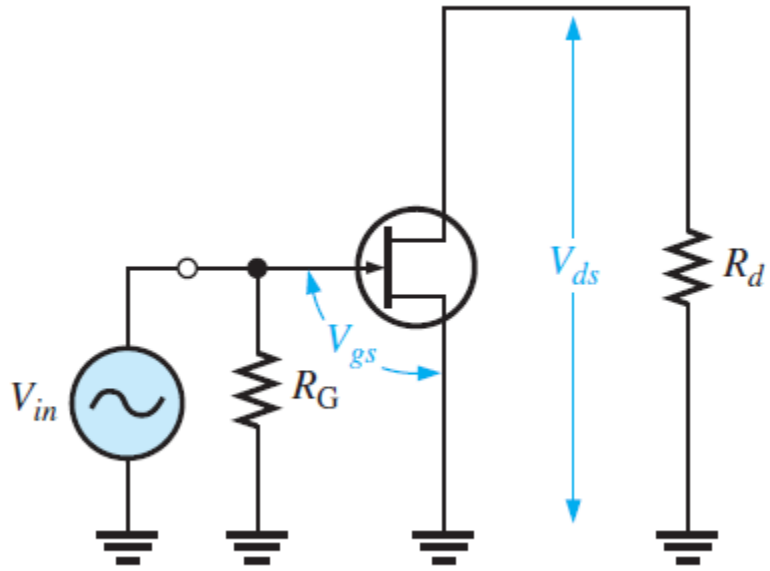
AC Equivalent Circuit

To analyze the signal operation of the amplifier, develop an ac equivalent circuit as follows. Replace the capacitors by effective shorts, based on the simplifying assumption that $X_C = 0$ at the signal frequency. Replace the dc source by a ground, based on the assumption that the voltage source has a zero internal resistance. The V_{DD} terminal is at a zero-volt ac potential and therefore acts as an ac ground. The ac equivalent circuit is shown in Figure (a). Notice that the V_{DD} end of R_d and the source terminal are both effectively at ac ground. Recall that in ac analysis, the ac ground and the actual circuit ground are treated as the same point.

An ac voltage source is shown connected to the input in Figure (b). Since the input resistance to a JFET is extremely high, practically all of the input voltage from the signal source appears at the gate with very little voltage dropped across the internal source resistance. $V_{gs} = V_{in}$



(a)



(b)

Voltage Gain The expression for JFET voltage gain that was given in the Equation below applies to the common-source amplifier

$$A_v = g_m R_d$$

The output signal voltage V_{ds} at the drain is

$$V_{out} = V_{ds} = A_v V_{gs}$$

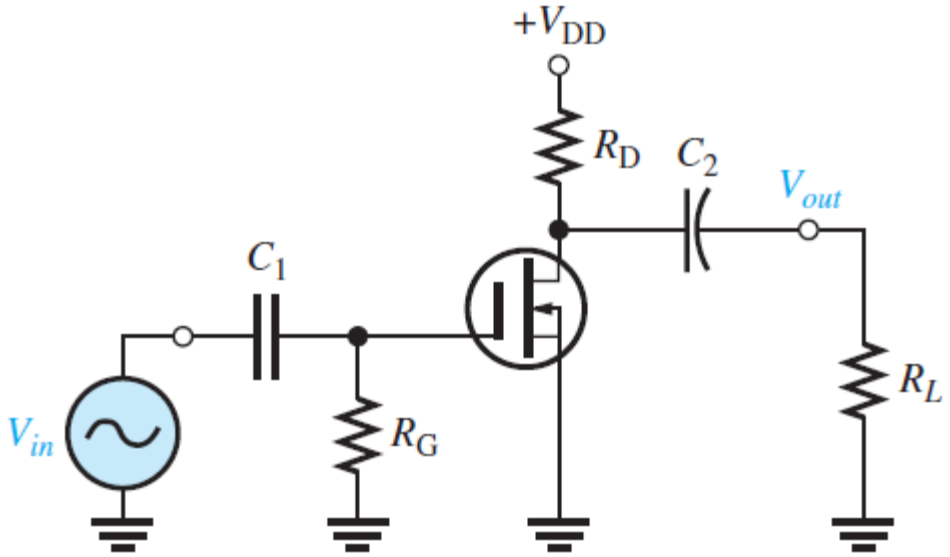
or

$$V_{out} = g_m R_d V_{in}$$

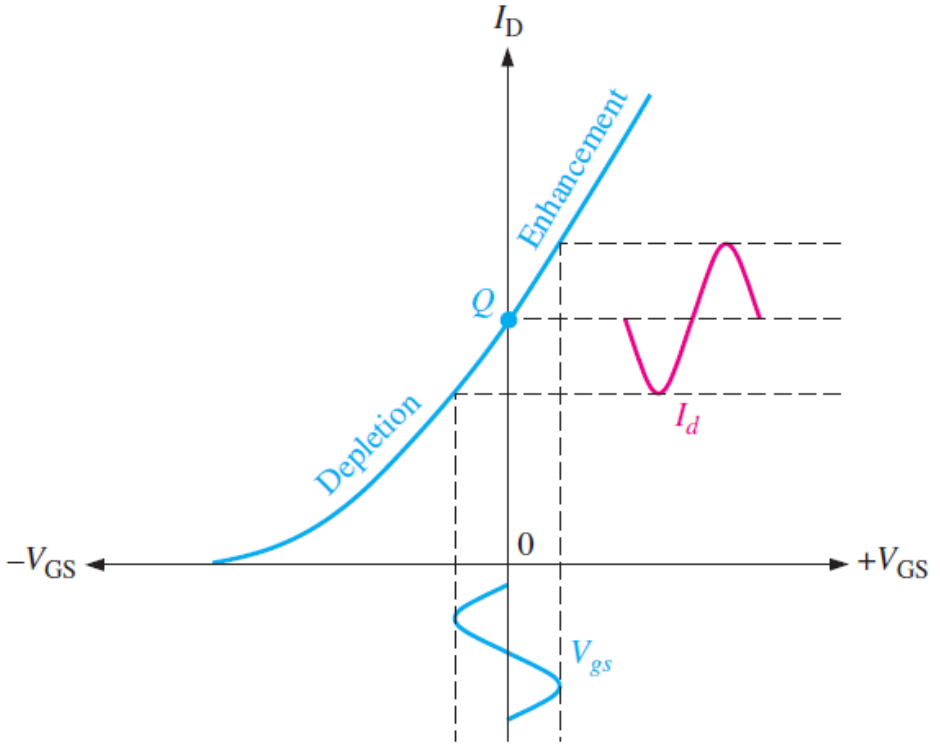
where $R_d = R_D \parallel R_L$ and $V_{in} = V_{gs}$.

D-MOSFET Amplifier Operation

A zero-biased common-source *n*-channel D-MOSFET with an ac source capacitively coupled to the gate is shown in upper figure. The gate is at approximately 0 V dc and the source terminal is at ground, thus making $V_{GS} = 0$ V.



The signal voltage causes V_{gs} to swing above and below its zero value, producing a swing in I_d, as shown in lower figure. The negative swing in Vgs produces the depletion mode, and Id decreases. The positive swing in Vgs produces the enhancement mode, and I_d increases. Note that the enhancement mode is to the right of the vertical axis ($V_{GS} = 0$), and the depletion mode is to the left. The dc analysis of this amplifier is somewhat easier than for a JFET because $I_D = I_{DSS}$ at $V_{GS} = 0$. Once I_D is known, the analysis involves calculating only V_D.



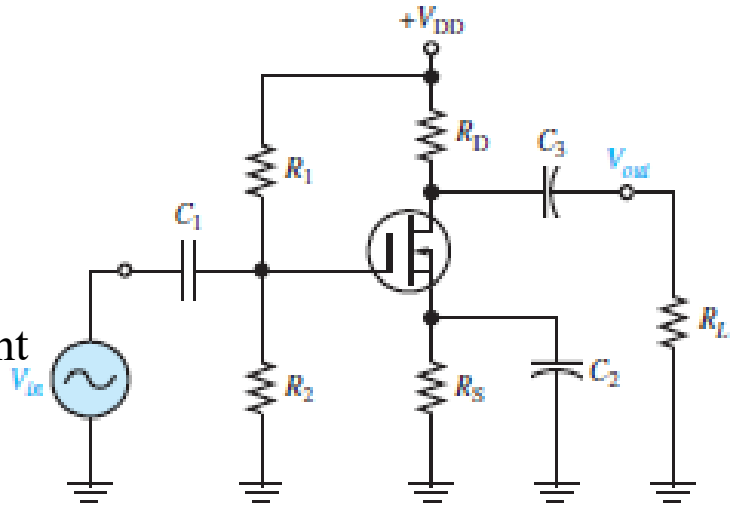
$$V_D = V_{DD} - I_D R_D$$

The ac analysis is the same as for the JFET amplifier.

E-MOSFET Amplifier Operation

A common-source *n*-channel E-MOSFET with voltage-divider bias with an ac source capacitively coupled to the gate is shown in upper figure. The gate is biased with a positive voltage such that $V_{GS} > V_{GS(th)}$.

As with the JFET and D-MOSFET, the signal voltage produces a swing in V_{gs} above and below its Q-point value, V_{GSQ}. This, in turn, causes a swing in I_d above and below its Q-point value, I_{DQ}, as illustrated in lower figure. Operation is entirely in the enhancement mode.



The circuit uses voltage-divider bias to achieve a V_{GS} above threshold. The general dc analysis proceeds as follows using the E-MOSFET characteristic equation to solve for I_D.

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD}$$

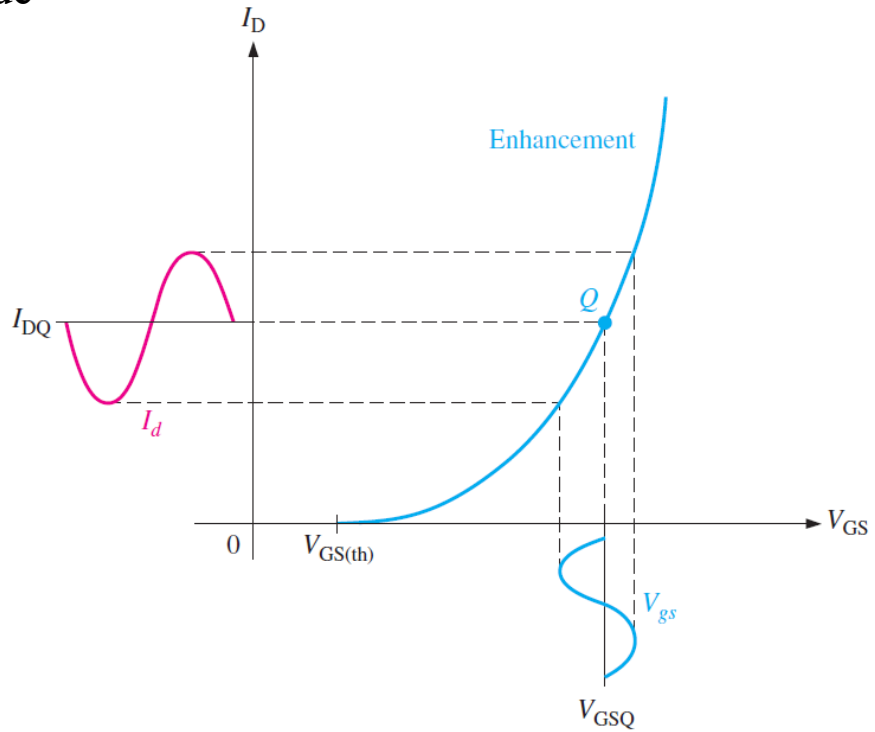
$$I_D = K(V_{GS} - V_{GS(th)})^2$$

$$V_{DS} = V_{DD} - I_D R_D$$

The voltage gain expression is the same as for the JFET and D-MOSFET circuits. The ac input resistance is:

$$R_{in} = R_1 \| R_2 \| R_{IN(gate)}$$

where $R_{IN(gate)} = V_{GS}/I_{GSS}$.



A common-source amplifier using an E-MOSFET is shown below. Find V_{GS}, I_D, V_{DS}, and the ac output voltage. Assume that for this particular device, $I_{D(on)}$ 200 mA at V_{GS} = 4 V, $V_{GS(th)}$ = 2 V, and g_m = 23 mS. V_{in} = 25 mV.

$$V_{GS} = \frac{R2}{R_1 + R_2} V_{DD} = (15)\frac{820\ \text{Kohm}}{5.52\text{Mohm}} = \mathbf{2.23\ V}$$

For V_{GS} = 4 V,

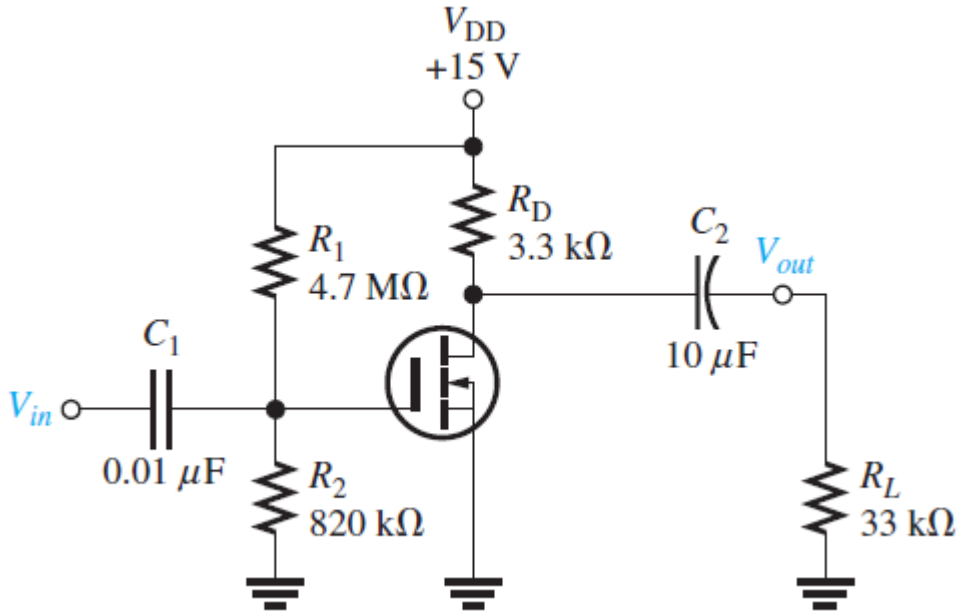
$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th))2}} = \frac{200\ \text{mA}}{(4\ \text{V} - 2\ \text{V})^2} = 50\ \text{mA/V}^2$$

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (50\ )(2.23\ \text{V} - 2\ \text{V})^2 = \mathbf{2.65\ mA}$$

$$V_{DS} = V_{DD} - I_D R_D = 15\ \text{V} - (2.65\ \text{mA})(3.3\ \text{kOhm}) = \mathbf{6.26\ V}$$

$$R_d = R_D\ //\ R_L = 3.3\ \text{kOhm}\ //\ 33\ \text{kohm} = 3\ \text{Kohm}$$

The ac output voltage is $V_{out} = A_v V_{in} = g_m R_d V_{in} = (23\ \text{mS})(3\ \text{kohm})(25\ \text{mV}) = \mathbf{1.73\ V}$



MOSFET Switching Operation

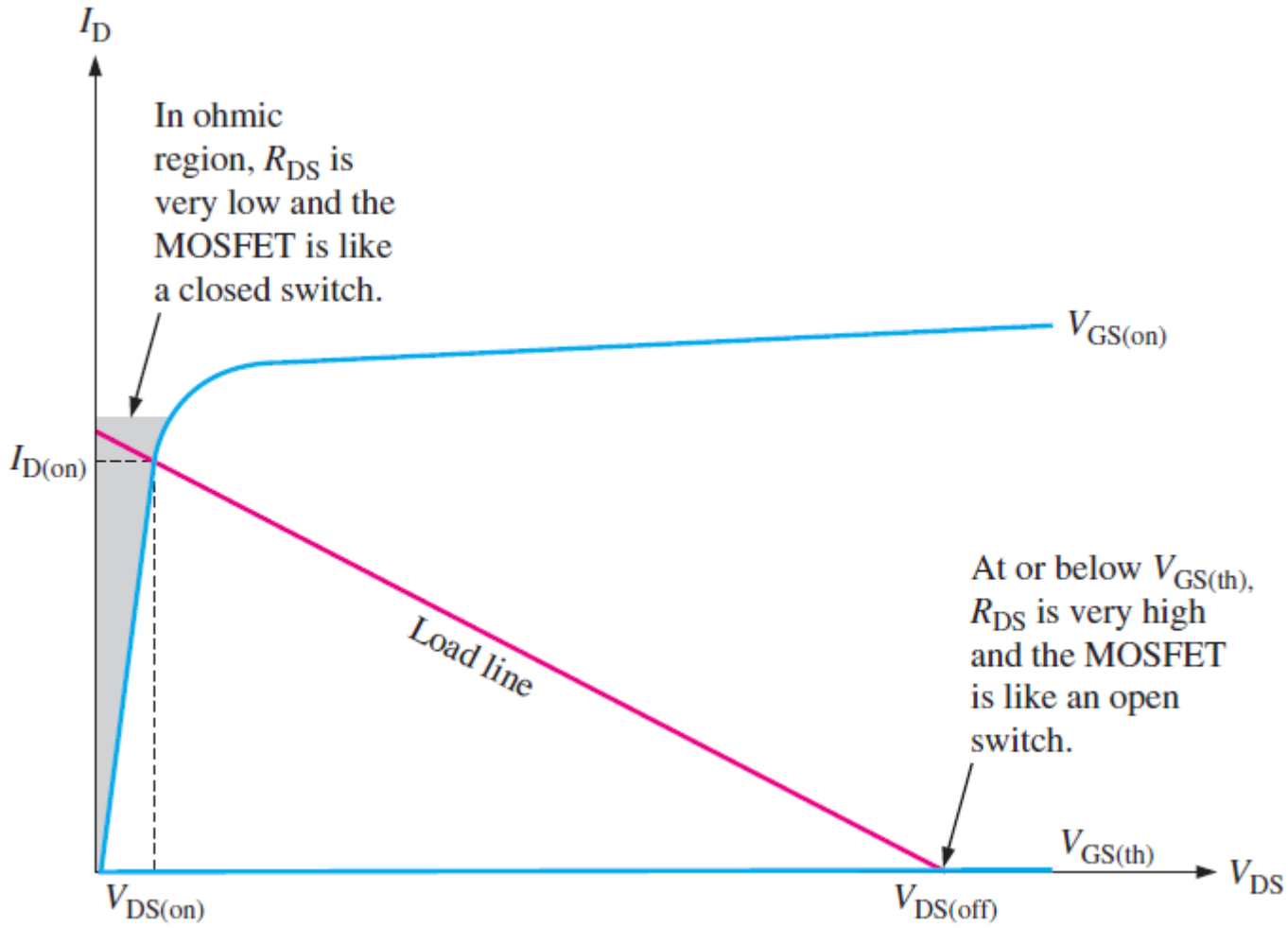
E-MOSFETs are generally used for switching applications because of their threshold characteristic, $V_{GS(th)}$.

➔ When the gate-to-source voltage is less than the threshold value, the MOSFET is *off*.

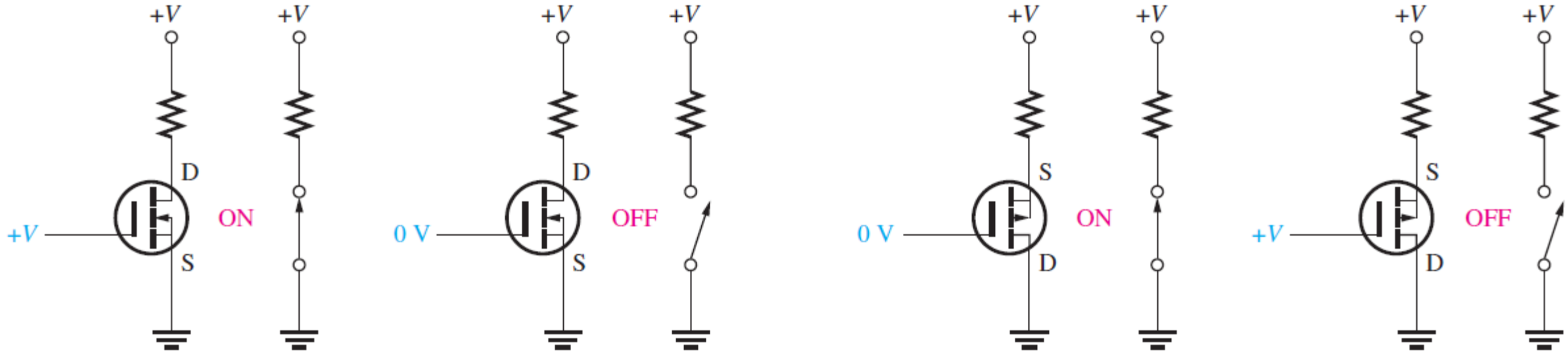
➔ When the gate-to-source voltage is greater than the threshold value, the MOSFET is *on*.

➔ When V_{GS} is varied between $V_{GS(th)}$ and $V_{GS(on)}$, the MOSFET is being operated as a switch, as illustrated in next figure. In the *off* state, when the device is operating at the lower end of the load line and acts like an open switch (very high R_{DS}).

When V_{GS} is sufficiently greater than $V_{GS(th)}$, the device is operating at the upper end of the load line in the ohmic region and acts like a closed switch (very low R_{DS}).



The Ideal Switch Refer to Figure (a). When the gate voltage of the *n*-channel MOSFET is V, the gate is more positive than the source by an amount exceeding $V_{GS(th)}$. The MOSFET is *on* and appears as a closed switch between the drain and source. When the gate voltage is zero, the gate-to-source voltage is 0 V. The MOSFET is *off* and appears as an open switch between the drain and source. Refer to Figure (b). When the gate voltage of the *p*-channel MOSFET is 0 V, the gate is less positive than the source by an amount exceeding $V_{GS(th)}$. The MOSFET is *on* and appears as a closed switch between the drain and source. When the gate voltage is V, the gate-to-source voltage is 0 V. The MOSFET is *off* and appears as an open switch between the drain and source. V_{GS} 6 $V_{GS(th)}$,

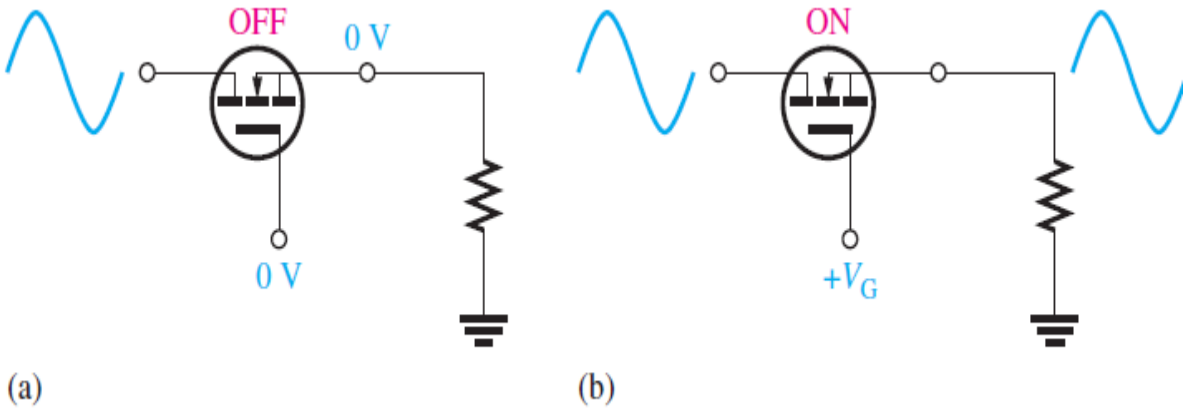


(a) *n*-channel MOSFET and switch equivalent

(b) *p*-channel MOSFET and switch equivalent

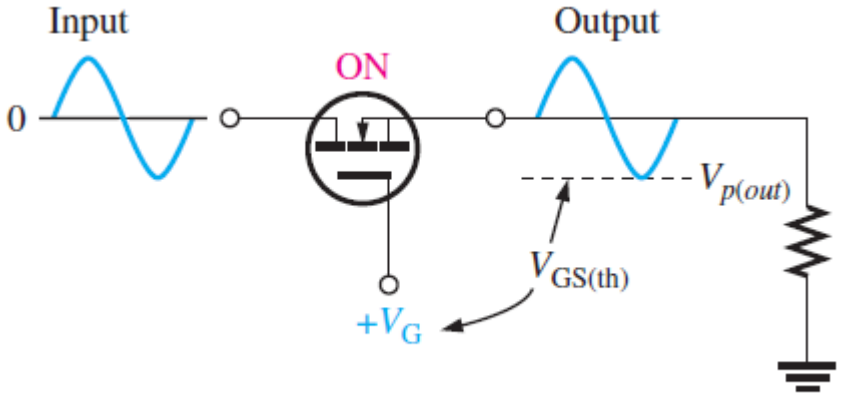
The Analog Switch

MOSFETs are commonly used for switching analog signals. Basically, a signal applied to the drain can be switched through to the source by a voltage on the gate. A major restriction is that the signal level at the source must not cause the gate-to-source voltage to drop below $V_{GS(th)}$.



A basic *n*-channel MOSFET **analog switch** is shown in Figure 9–34. The signal at the drain is connected to the source when the MOSFET is turned on by a positive V_{GS} and is disconnected when V_{GS} is 0, as indicated.

When the analog switch is *on,* as illustrated in lower figure, the minimum gate-to-source voltage occurs at the negative peak of the signal. The difference in is the gate-to-source voltage at the instant of the negative peak and must be equal to or greater than $V_{GS(th)}$ to keep the MOSFET in conduction.

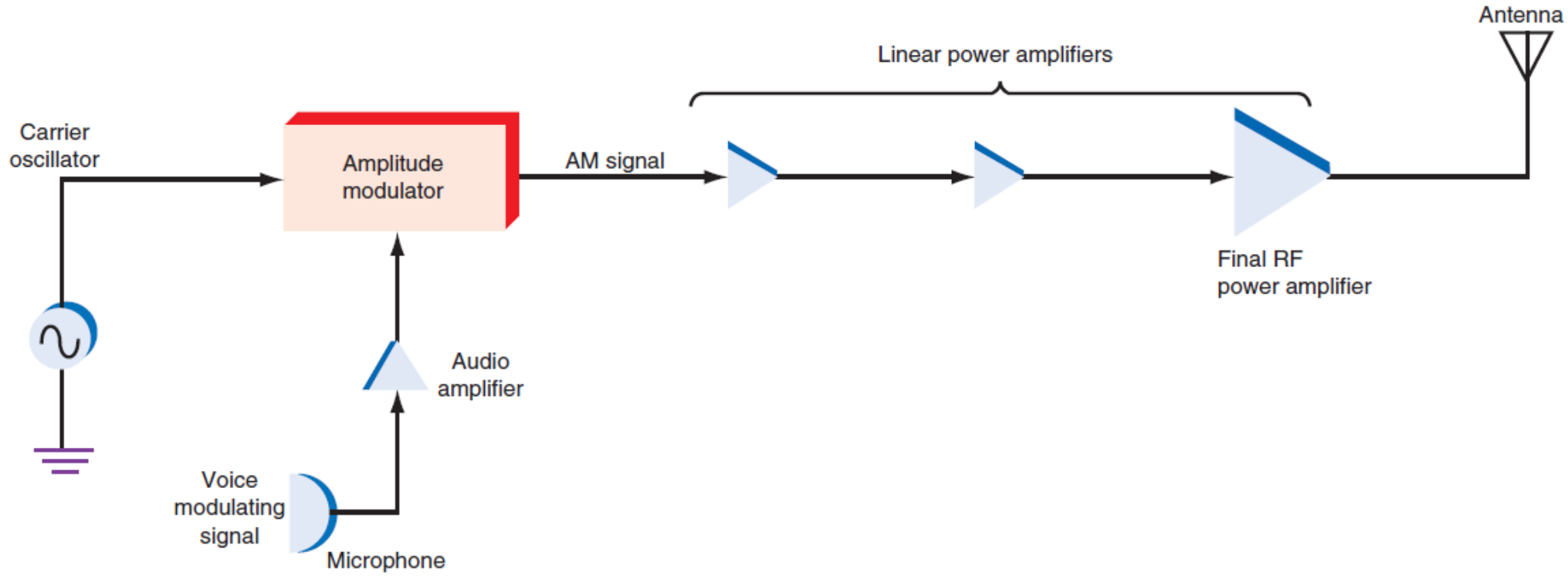


$$V_{GS} = V_G - V_{p(out)} \geq V_{GS(th)}$$

High-Level AM

In low-level modulator circuits such as those discussed above, the signals are generated at very low voltage and power amplitudes. The voltage is typically less than 1 V, and the power is in milliwatts. In systems using low-level modulation, the AM signal is applied to one or more linear amplifiers, as shown in the figure down, to increase its power level without distorting the signal. These amplifier circuits—class A, class AB, or class B—raise the level of the signal to the desired power level before the AM signal is fed to the antenna.

In high-level AM, the modulator varies the voltage and power in the final RF amplifier stage of the transmitter. The result is high efficiency in the RF amplifier and overall high-quality performance.

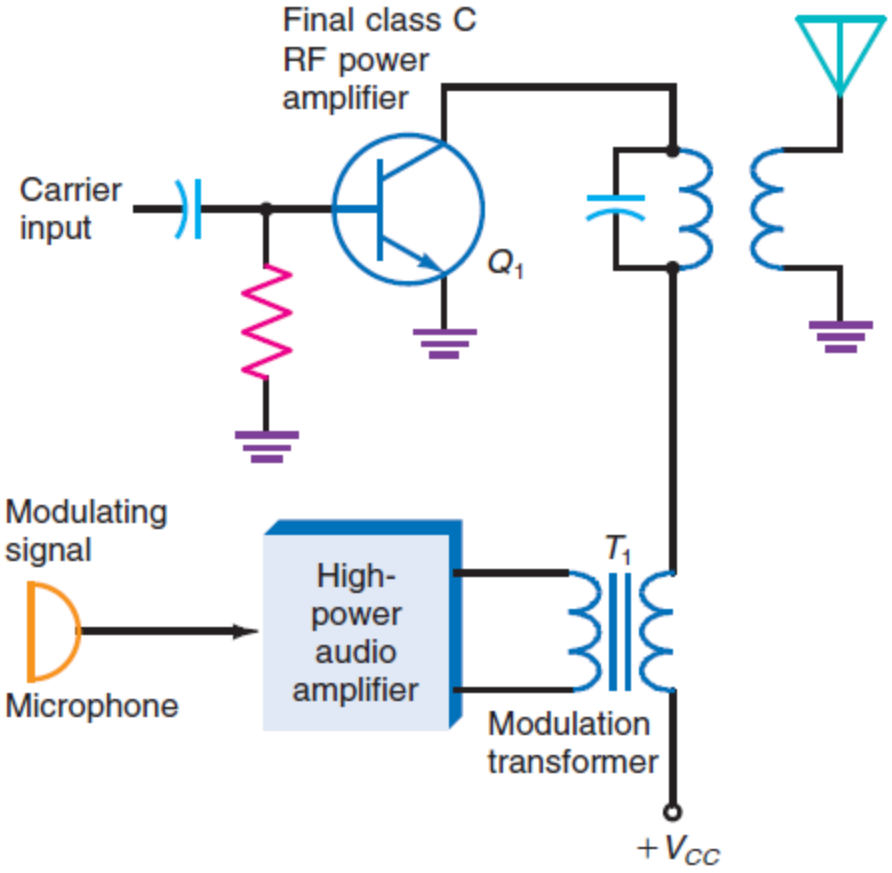


High Level Collector Modulator.

One example of a high-level modulator circuit is the *collector modulator* . The output stage of the transmitter is a high-power class C amplifier.

➔Class C amplifiers conduct for only a portion of the positive half-cycle of their input signal. The collector current pulses cause the tuned circuit to oscillate (ring) at the desired output frequency. The tuned circuit, therefore, reproduces the negative portion of the carrier signal.

➔The modulator is a linear power amplifier that takes the low-level modulating signal and amplifies it to a high-power level. The modulating output signal is coupled through modulation transformer T_1 to the class C amplifier. The secondary winding of the modulation transformer is connected in series with the collector supply voltage V_{CC} of the class C amplifier.



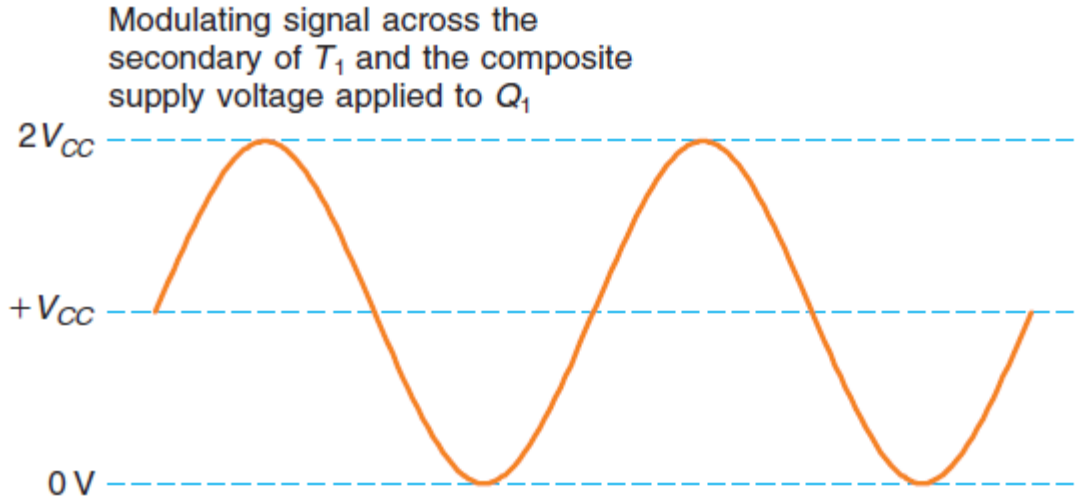
➔ With a zero-modulation input signal, there is zero-modulation voltage across the secondary of T_1, the collector supply voltage is applied directly to the class C amplifier, and the output carrier is a steady sine wave.

➔ When the modulating signal occurs, the ac voltage of the modulating signal across the secondary of the modulation transformer is added to and subtracted from the dc collector supply voltage. This varying supply voltage is then applied to the class C amplifier, causing the amplitude of the current pulses through transistor Q_1 to vary. As a result, the amplitude of the carrier sine wave varies in accordance with the modulated signal.

➔ When the modulation signal goes positive, it adds to the collector supply voltage, thereby increasing its value and causing higher current pulses and a higher-amplitude carrier. When the modulating signal goes negative, it subtracts from the collector supply voltage, decreasing it. For that reason, the class C amplifier current pulses are smaller, resulting in a lower-amplitude carrier output.

For 100 percent modulation the peak of the modulating signal must be equal to V_{CC}.

➔ For 100 percent modulation, the peak of the modulating signal across the secondary of T_1 must be equal to the supply voltage. When the positive peak occurs, the voltage applied to the collector is twice the collector supply voltage. When the modulating signal goes negative, it subtracts from the collector supply voltage. When the negative peak is equal to the supply voltage, the effective voltage applied to the collector of $Q1$ is zero, producing zero carrier output.



In practice, 100 percent modulation cannot be achieved with the high-level collector modulator circuit shown before because of the transistor's nonlinear response to small signals. To overcome this problem, the amplifier driving the final class C amplifier is collector-modulated simultaneously.

High-level modulation produces the best type of AM, but it requires an extremely high-power modulator circuit. In fact, for 100 percent modulation, the power supplied by the modulator must be equal to one-half the total class C amplifier input power. If the class C amplifier has an input power of 1000 W, the modulator must be able to deliver one-half this amount, or 500 W.

Example: An AM transmitter uses high-level modulation of the final RF power amplifier, which has a dc supply voltage V_{CC} of 48 V with a total current I of 3.5 A. The efficiency is 70 percent.

a. What is the RF input power to the final stage?

$$\text{DC input power} = P_i = V_{CC}I \qquad P = 48 \times 3.5 = 168 \text{ W}$$

b. How much AF power is required for 100 percent modulation? (*Hint:* For 100 percent modulation, AF modulating power P_m is one-half the input power.)

$$P_m = \frac{P_i}{2} = \frac{168}{2} = 84 \text{ W}$$

c. What is the carrier output power?

$$\% \text{ efficiency} = \frac{P_{\text{out}}}{P_{\text{in}}} \times 100$$

$$P_{\text{out}} = \frac{\% \text{ efficiency} \times P_{\text{in}}}{100} = \frac{70(168)}{100} = 117.6 \text{ W}$$

d. What is the power in one sideband for 67 percent modulation?

P_s = sideband power

$$P_s = \frac{P_c(m^2)}{4}$$

m = modulation percentage (%) = 0.67

P_c = 168

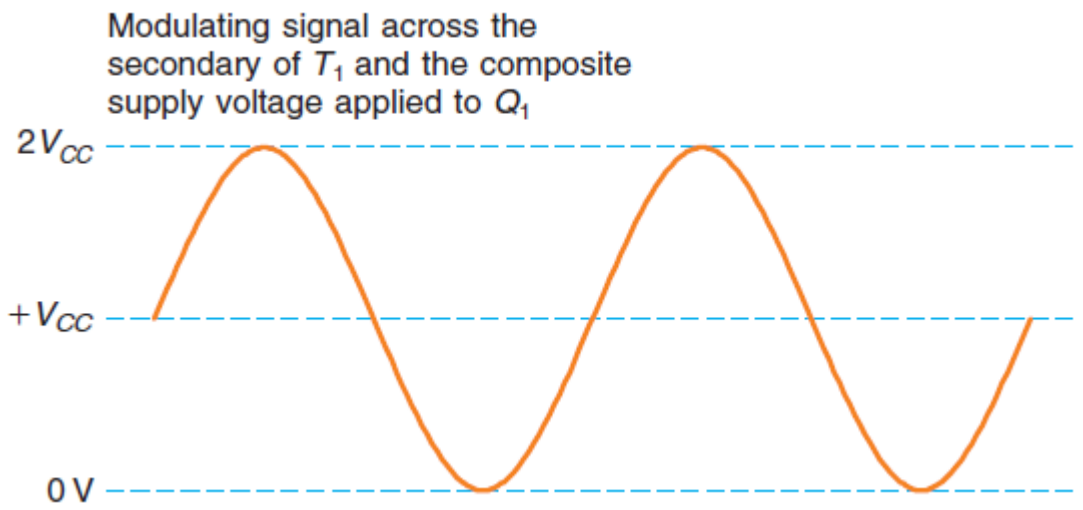
$$P_s = \frac{168(0.67)^2}{4} = 18.85 \text{ W}$$

e. What is the maximum and minimum dc supply voltage swing with 100 percent modulation?

Minimum swing = 0

Supply voltage v_{CC} = 48 V

Maximum swing $2 \times V_{CC} = 2 \times 48 = 96$ V

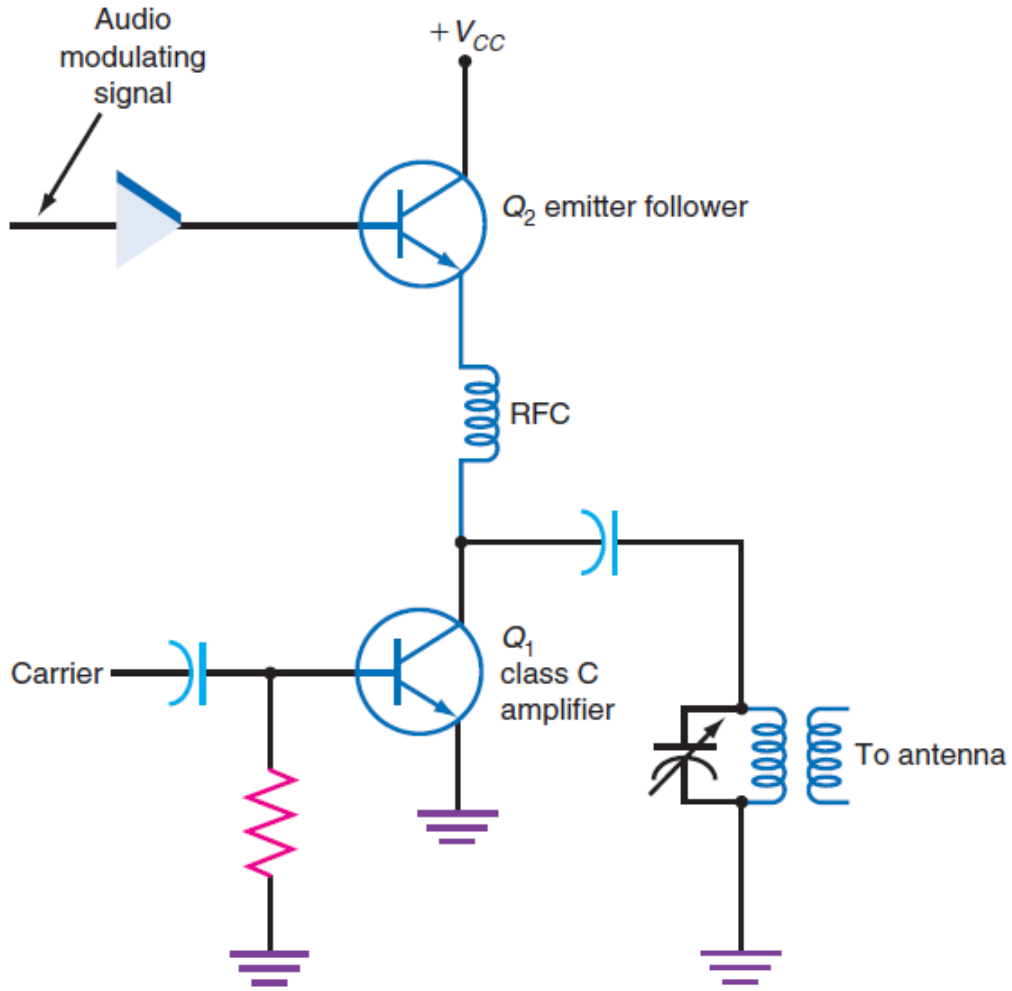


Series Modulator.

A major disadvantage of collector modulators is the need for a modulation transformer that connects the audio amplifier to the class C amplifier in the transmitter. The higher the power, the larger and more expensive the transformer. For very high power applications, the transformer is eliminated and the modulation is accomplished at a lower level with one of the many modulator circuits described in previously.

The resulting AM signal is amplified by a high-power linear amplifier. This arrangement is not preferred because linear RF amplifiers are less efficient than class C amplifiers.

One approach is to use a transistorized version of a collector modulator in which a transistor is used to replace the transformer, as in next figure. This series modulator replaces the transformer with an emitter follower. The modulating signal is applied to the emitter follower Q_2, which is an audio power amplifier

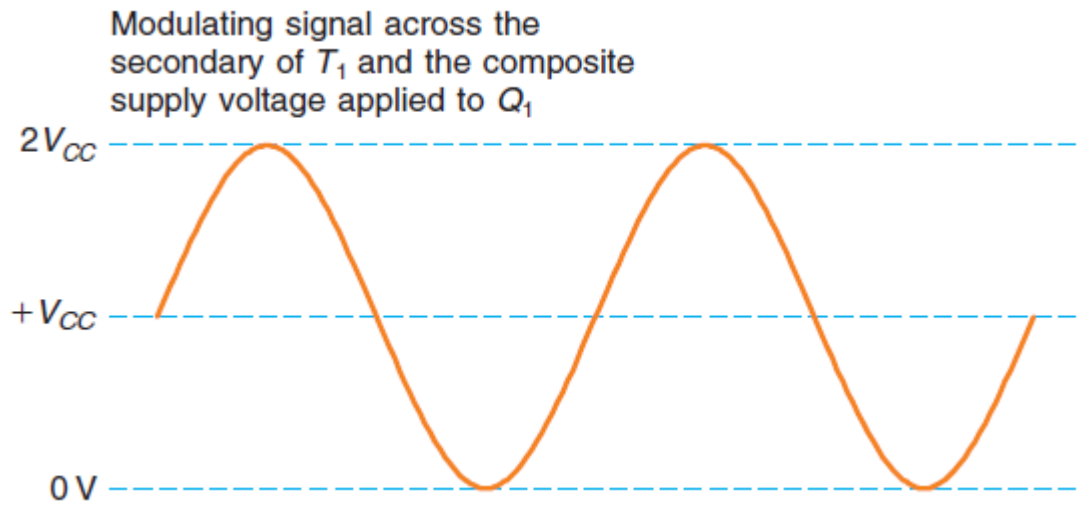


Note that the emitter follower appears in series with the collector supply voltage $+V_{CC}$. This causes the amplified audio modulating signal to vary the collector supply voltage to the class C amplifier Q_1, as illustrated in the figure down. And Q_2 simply varies the supply voltage to Q_1.

If the modulating signal goes positive, the supply voltage to Q_1 increases; thus, the carrier amplitude increases in proportion to the modulating signal.

If the modulating signal goes negative, the supply voltage to Q_1 decreases, thereby decreasing the carrier amplitude in proportion to the modulating signal. For 100 percent modulation, the emitter follower can reduce the supply voltage to zero on maximum negative peaks.

Using this high-level modulating scheme eliminates the need for a large, heavy, and expensive transformer, and considerably improves frequency response. However, it is very inefficient.



➔ The emitter-follower modulator must dissipate as much power as the class C RF amplifier. For example, assume a collector supply voltage of 24 V and a collector current of 0.5 A. With no modulating signal applied, the percentage of modulation is 0. The emitter follower is biased so that the base and the emitter are at a dc voltage of about one-half the supply voltage, or in this example 12 V. The collector supply voltage on the class C amplifier is 12 V, and the input power is therefore:

$$P_{in} = V_{CC}I_c = 12(0.5) = 6\ \text{W}$$

To produce 100 percent modulation, the collector voltage on Q_1 must double, as must the collector current. This occurs on positive peaks of the audio input, as described above. At this time most of the audio signal appears at the emitter of Q_1; very little of the signal appears between the emitter and collector of Q_2, and so at 100 percent modulation, Q_2 dissipates very little power.

When the audio input is at its negative peak, the voltage at the emitter of Q_2 is reduced to 12 V. This means that the rest of the supply voltage, or another 12 V, appears between the emitter and collector of Q_2. Since Q_2 must also be able to dissipate 6 W, it has to be a very large power transistor. The efficiency drops to less than 50 percent. With a modulation transformer, the efficiency is much greater, in some cases as high as 80 percent.

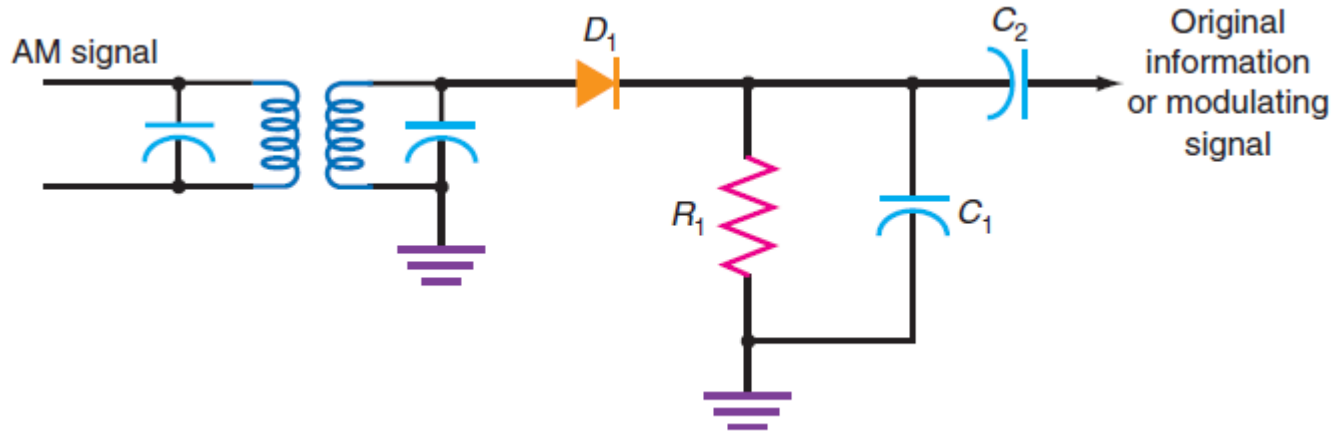
This arrangement is not practical for very high power AM, but it does make an effective higher-level modulator for power levels below about 100 W.

Amplitude Demodulators

Demodulators, or *detectors,* are circuits that accept modulated signals and recover the original modulating information. The demodulator circuit is the key circuit in any radio receiver. In fact, demodulator circuits can be used alone as simple radio receivers.

Diode Detectors:

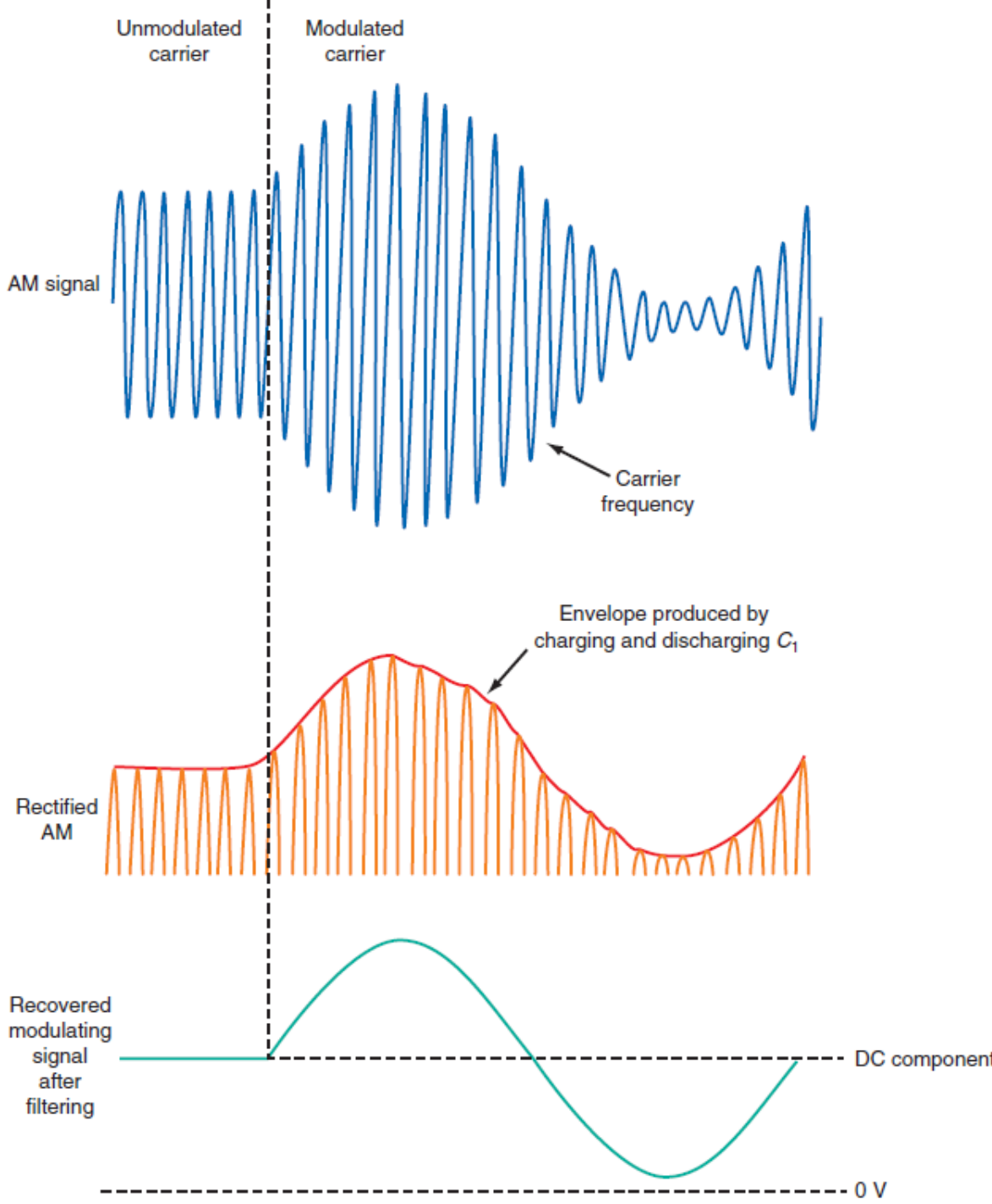
The simplest and most widely used amplitude demodulator is the *diode detector* (see figure below). As shown, the AM signal is usually transformer-coupled and applied to a basic half wave rectifier circuit consisting of D_1 and R_1. The diode conducts when the positive half-cycles of the AM signals occur. During the negative half-cycles, the diode is reverse-biased and no current flows through it. As a result, the voltage across R_1 is a series of positive pulses whose amplitude varies with the modulating signal. A capacitor C_1 is connected across resistor R_1, effectively filtering out the carrier and thus recovering the original modulating signal.



One way to look at the operation of a diode detector is to analyze its operation in the time domain. The waveforms next figure illustrate this. On each positive alternation of the AM signal, the capacitor charges quickly to the peak value of the pulses passed by the diode. When the pulse voltage drops to zero, the capacitor discharges into resistor *R*1. The time constant of *C*1 and *R*1 is chosen to be long compared to the period of the carrier. As a result, the capacitor discharges only slightly during the time that the diode is not conducting.

When the next pulse comes along, the capacitor again charges to its peak value. When the diode cuts off, the capacitor again discharges a small amount into the resistor. The resulting waveform across the capacitor is a close approximation to the original modulating signal.

Because the capacitor charges and discharges, the recovered signal has a small amount of ripple on it, causing distortion of the modulating signal. However, because the carrier frequency is usually many times higher than the modulating frequency, these ripple variations are barely noticeable.



Because the diode detector recovers the envelope of the AM signal, which is the original modulating signal, the circuit is sometimes referred to as an *envelope detector.* Distortion of the original signal can occur if the time constant of the load resistor R_1 and the shunt filter capacitor C_1 is too long or too short. If the time constant is too long, the capacitor discharge will be too slow to follow the faster changes in the modulating signal. This is referred to as *diagonal distortion.* If the time constant is too short, the capacitor will discharge too fast and the carrier will not be sufficiently filtered out. The

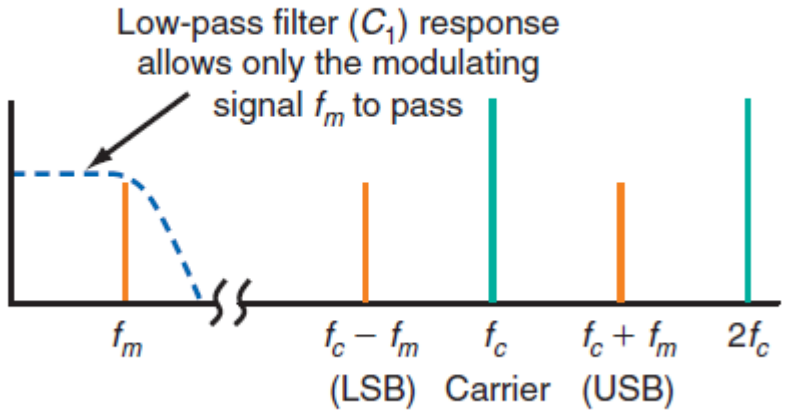
dc component in the output is removed with a series coupling or blocking capacitor, C_2, which is connected to an amplifier.

Another way to view the operation of the diode detector is in the frequency domain. In this case, the diode is regarded as a nonlinear device to which are applied multiple signals where modulation will take place. The multiple signals are the carrier and sidebands, which make up the input AM signal to be demodulated. The components of the AM signal are the carrier f_c, the upper sideband $f_c + f_m$, and the lower sideband $f_c - f_m$. The diode detector circuit combines these signals, creating the sum and difference signals:

$$f_c + (f_c + f_m) = 2f_c + f_m$$
$$f_c - (f_c + f_m) = -f_m$$
$$f_c + (f_c - f_m) = 2f_c - f_m$$
$$f_c - (f_c - f_m) = f_m$$

All these components appear in the output. Since the carrier frequency is very much higher than that of the modulating signal, the carrier signal can easily be filtered out with a simple low-pass filter. In a diode detector, this low-pass filter is just capacitor C_1 across load resistor R_1. Removing the carrier leaves only the original modulating signal. The frequency spectrum of a diode detector is illustrated in the figure below. The low-pass filter, C_1, removes all but the desired original modulating signal.

Output spectrum of a diode detector.

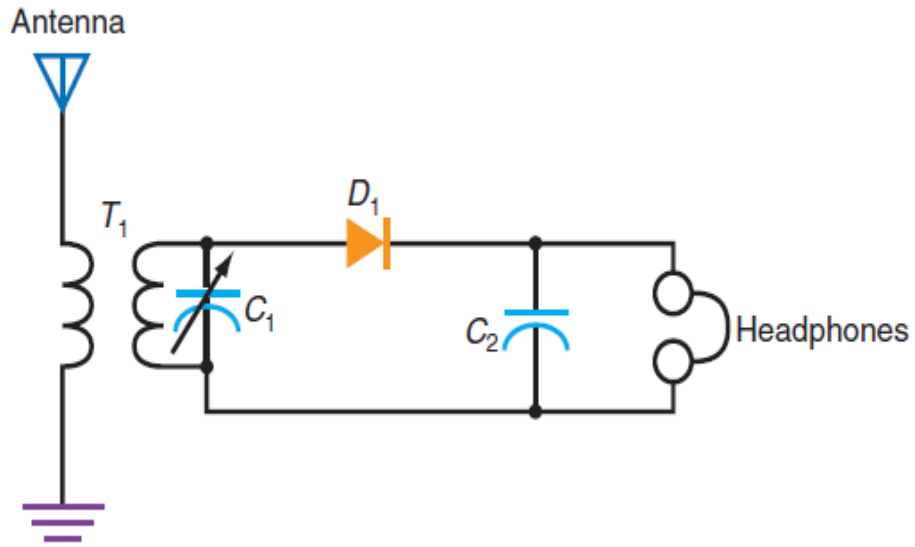


Crystal Radio Receivers

The crystal component of the *crystal radio receivers* that were widely used in the past is simply a diode. the diode detector circuit is redrawn, showing an antenna connection and headphones. A long wire antenna picks up the radio signal, which is inductively coupled to the secondary winding of T_1, which forms a series resonant circuit with C_1. Note that the secondary is not a parallel circuit, because the voltage induced into the secondary winding appears as a voltage source in series with the coil and capacitor. The variable capacitor C_1 is used to select a station. At resonance, the voltage across the capacitor is stepped up by a factor equal to the Q of the tuned circuit. This resonant voltage rise is a form of amplification.

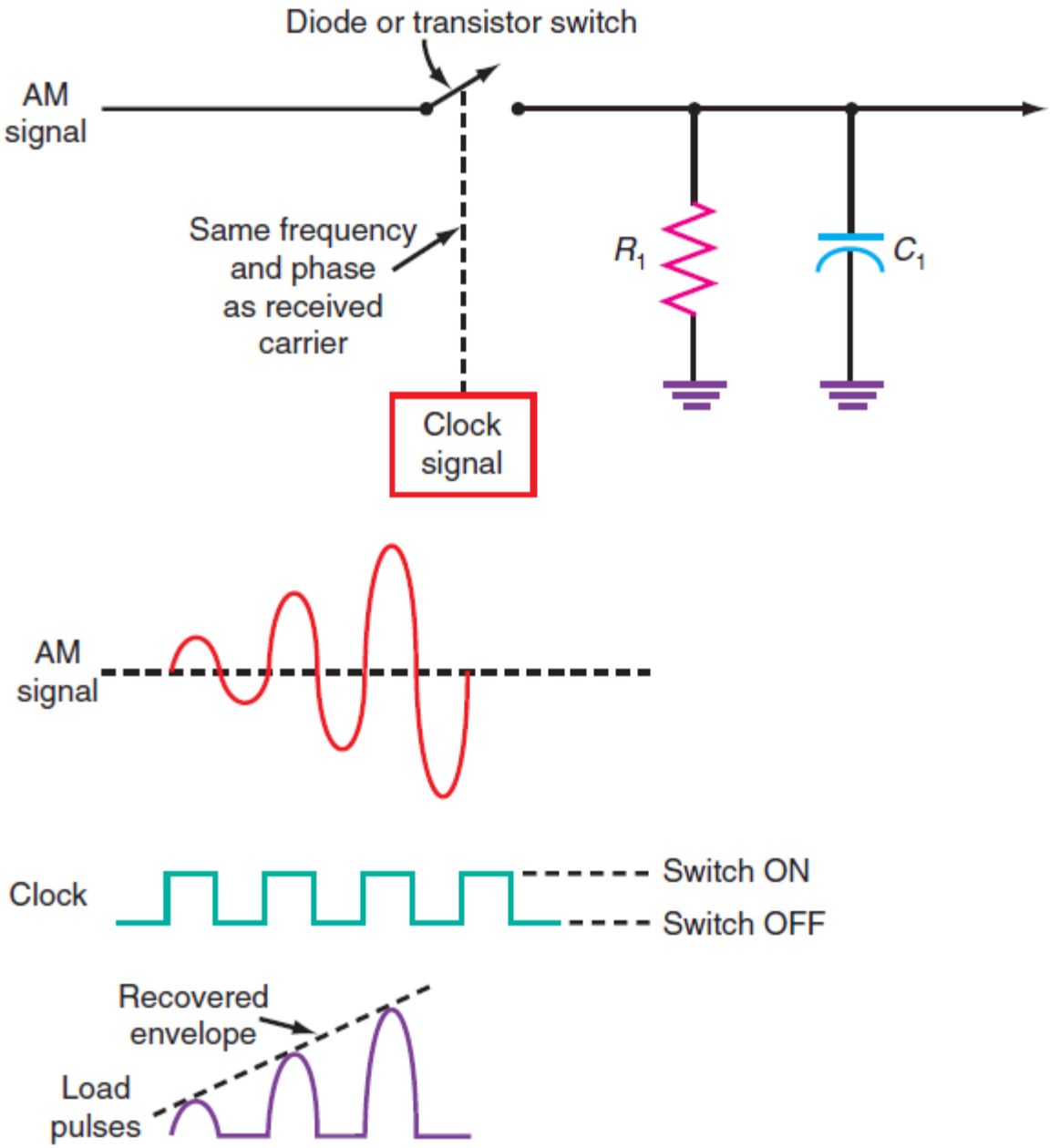
This higher-voltage signal is applied to the diode. The diode detector D_1 and its filter C_2 recover the original modulating information, which causes current flow in the headphones. The headphones serve as the load resistance, and capacitor C_2 removes the carrier. The result is a simple radio receiver; reception is very weak because no active amplification is provided. Typically, a germanium diode is used because its voltage threshold is lower than that of a silicon diode and permits reception of weaker signals. Crystal radio receivers can easily be built to receive standard AM broadcasts.

A crystal radio receiver.



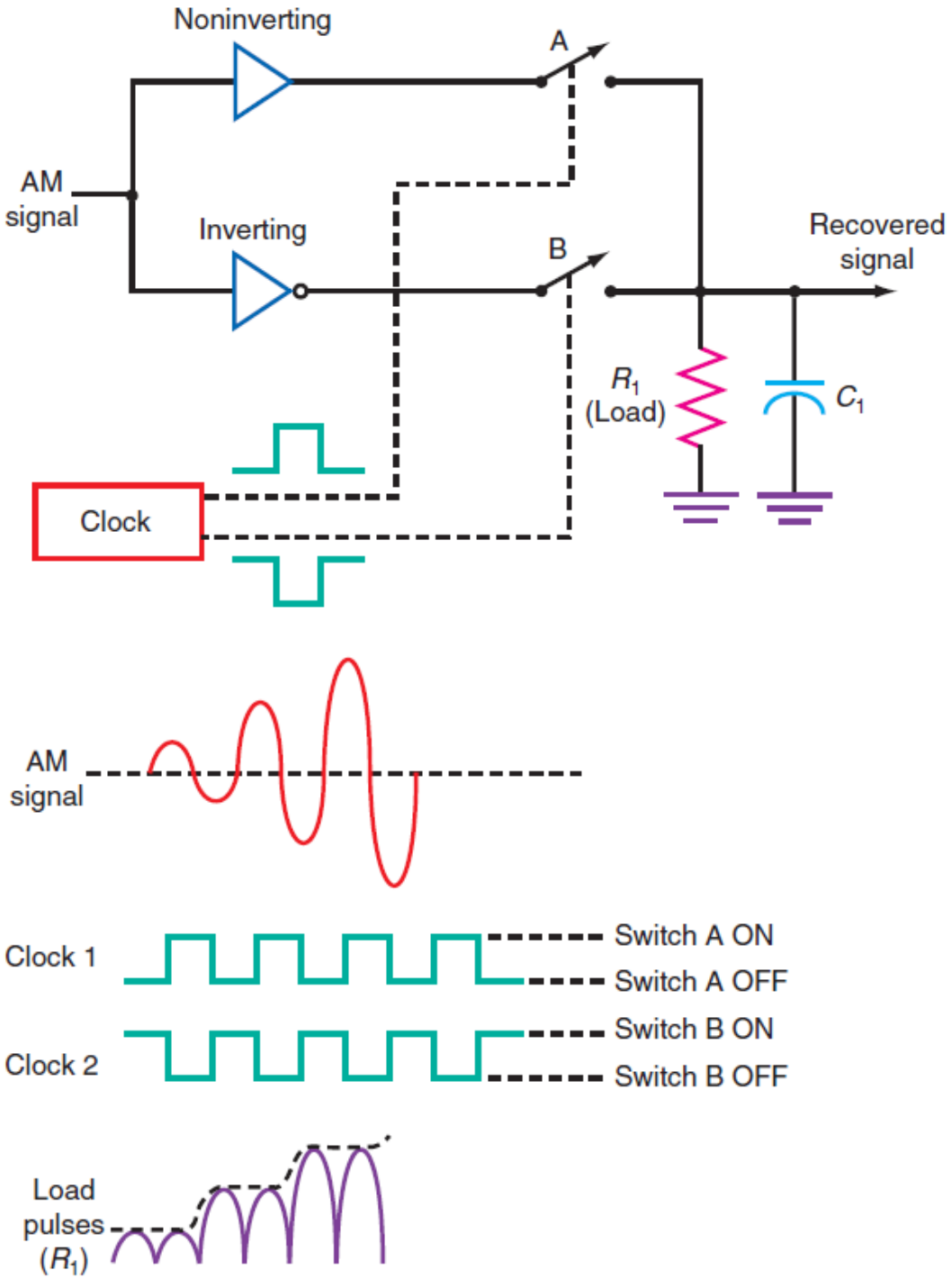
Synchronous Detection

Synchronous detectors use an internal clock signal at the carrier frequency in the receiver to switch the AM signal off and on, producing rectification similar to that in a standard diode detector. The AM signal is applied to a series switch that is opened and closed synchronously with the carrier signal. The switch is usually a diode or transistor that is turned on or off by an internally generated clock signal equal in frequency to and in phase with the carrier frequency. The switch is turned on by the clock signal during the positive half-cycles of the AM signal, which therefore appears across the load resistor. During the negative half-cycles of the AM signal, the clock turns the switch off, so no signal reaches the load or filter capacitor. The capacitor filters out the carrier.



A full wave synchronous detector is shown next figure. The AM signal is applied to both inverting and noninverting amplifiers. The internally generated carrier signal operates two switches A and B. The clock turns A on and B off or turns B on and A off. This arrangement simulates an electronic single-pole, double-throw (SPDT) switch. During positive half-cycles of the AM signal, the A switch feeds the noninverted AM output of positive half-cycles to the load. During the negative half-cycles of the input, the B switch connects the output of the inverter to the load. The negative half-cycles are inverted, becoming positive, and the signal appears across the load. The result is full wave rectification of the signal.

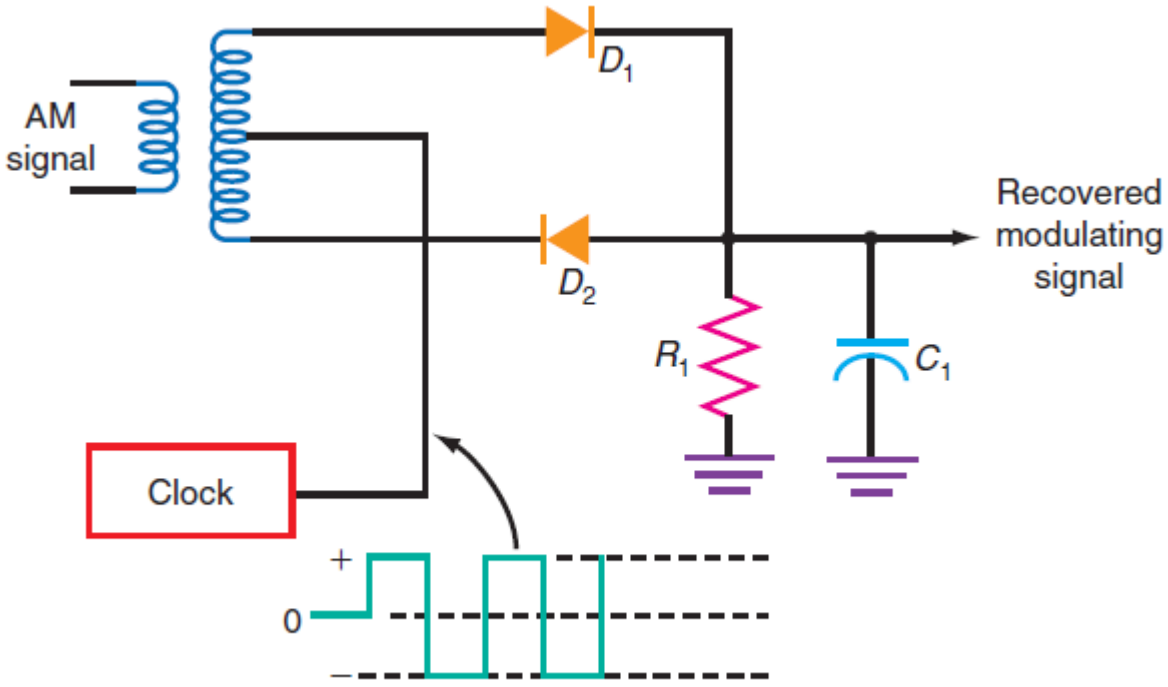
The key to making the synchronous detector work is to ensure that the signal producing the switching action is perfectly in phase with the received AM carrier. An internally generated carrier signal from, say, an oscillator will not work.



Even though the frequency and phase of the switching signal might be close to those of the carrier, they would not be perfectly equal. However, there are a number of techniques, collectively referred to as *carrier recovery circuits,* that can be used to generate a switching signal that has the correct frequency and phase relationship to the carrier.

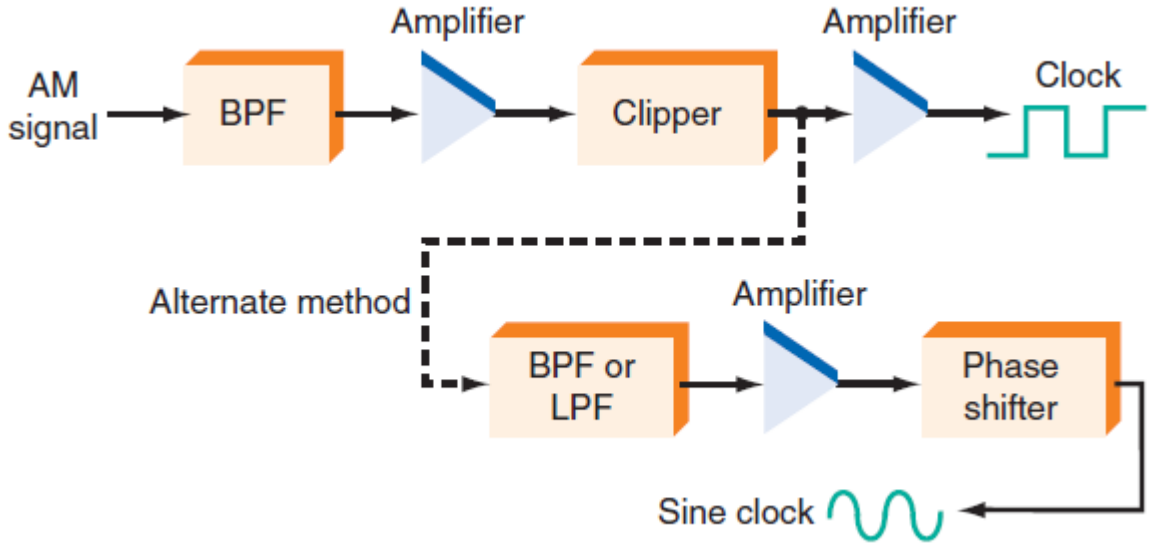
A practical synchronous detector is shown in the figure down. A center-tapped transformer provides the two equal but inverted signals. The carrier signal is applied to the center-tap. Note that one diode is connected oppositely from the way it would be if used in a full wave rectifier. These diodes are used as switches, which are turned off and on by the clock, which is used as the bias voltage. The carrier is usually a square wave derived by clipping and amplifying the AM signal. When the clock is positive, diode D_1 is forward-biased. It acts as a short circuit and connects the AM signal to the load resistor. Positive half-cycles appear across the load.

When the clock goes negative, D_2 is forward-biased. During this time, the negative cycles of the AM signal are occurring, which makes the lower output of the secondary winding positive. With D_2 conducting, the positive half-cycles are passed to the load, and the circuit performs full wave rectification. As before, the capacitor across the load filters out the carrier, leaving the original modulating signal across the load.



The circuit shown in the figure down is one way to supply the carrier to the synchronous detector. The AM signal to be demodulated is applied to a highly selective bandpass filter that picks out the carrier and suppresses the sidebands, thus removing most of the amplitude variations. This signal is amplified and applied to a clipper or limiter that removes any remaining amplitude variations from the signal, leaving only the carrier. The clipper circuit typically converts the sine wave carrier into a square wave that is amplified and thus becomes the clock signal. In some synchronous detectors, the clipped carrier is put through another bandpass filter to get rid of the square wave harmonics and generate a pure sine wave carrier. This signal is then amplified and used as the clock. A small phase shifter may be introduced to correct for any phase differences that occur during the carrier recovery process. The resulting carrier signal is exactly the same frequency and phase as those of the original carrier, as it is indeed derived from it. The output of this circuit is applied to the synchronous detector. Some synchronous detectors use a phaselocked loop to generate the clock, which is locked to the incoming carrier.

Synchronous detectors are also referred to as *coherent detectors,* and were known in the past as homodyne detectors. Their main advantage over standard diode detectors is that they have less distortion and a better signal-to-noise ratio. They are also less prone to *selective fading,* a phenomenon in which distortion is caused by the weakening of a sideband on the carrier during transmission.

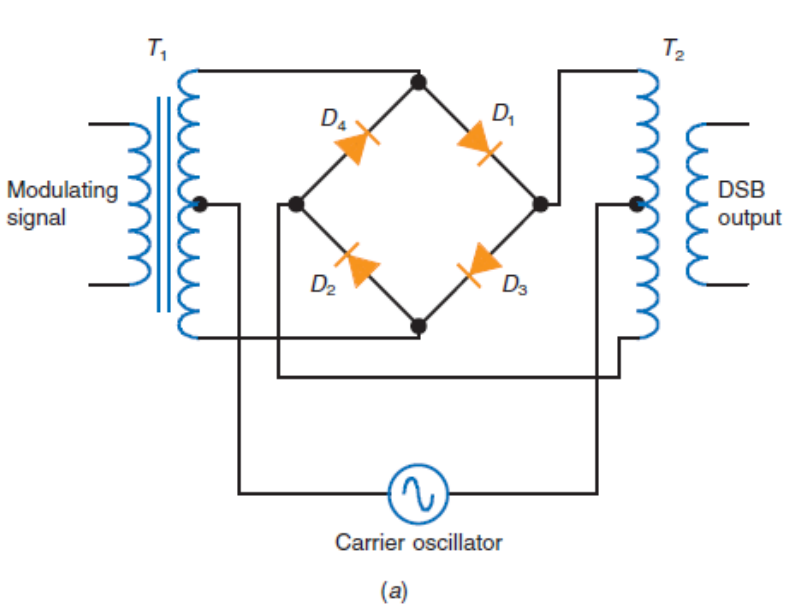


Balanced Modulators

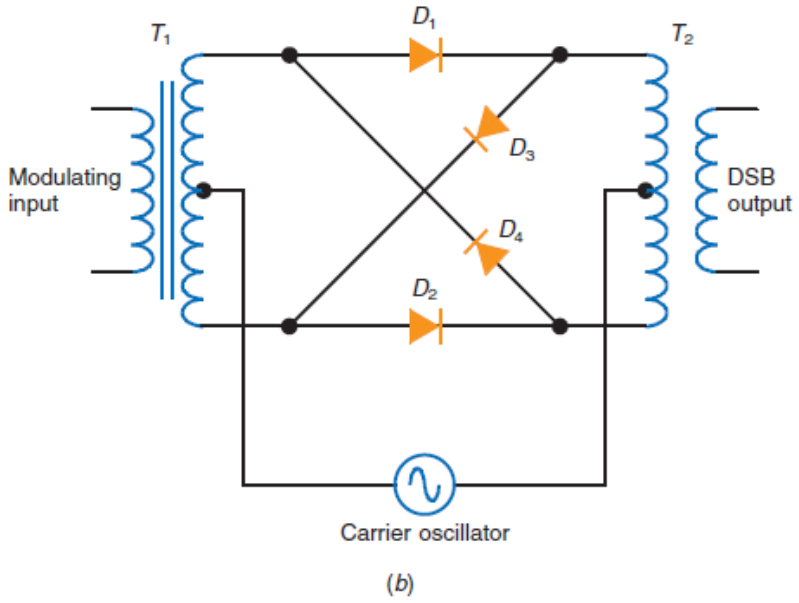
A *balanced modulator* is a circuit that generates a DSB signal, suppressing the carrier and leaving only the sum and difference frequencies at the output. The output of a balanced modulator can be further processed by fi lters or phase-shifting circuitry to eliminate one of the sidebands, resulting in an SSB signal.

Lattice Modulators

One of the most popular and widely used balanced modulators is the diode ring or *lattice modulator* in the fig down, consisting of an input transformer T_1, an output transformer T_2, and four diodes connected in a bridge circuit. The carrier signal is applied to the centre taps of the input and output transformers, and the modulating signal is applied to the input transformer T_1. The output appears across the secondary of the output transformer $T2$. The connections in Fig(a) are the same as those in Fig(b), but the operation of the circuit is perhaps more easily visualized as represented in part (b).

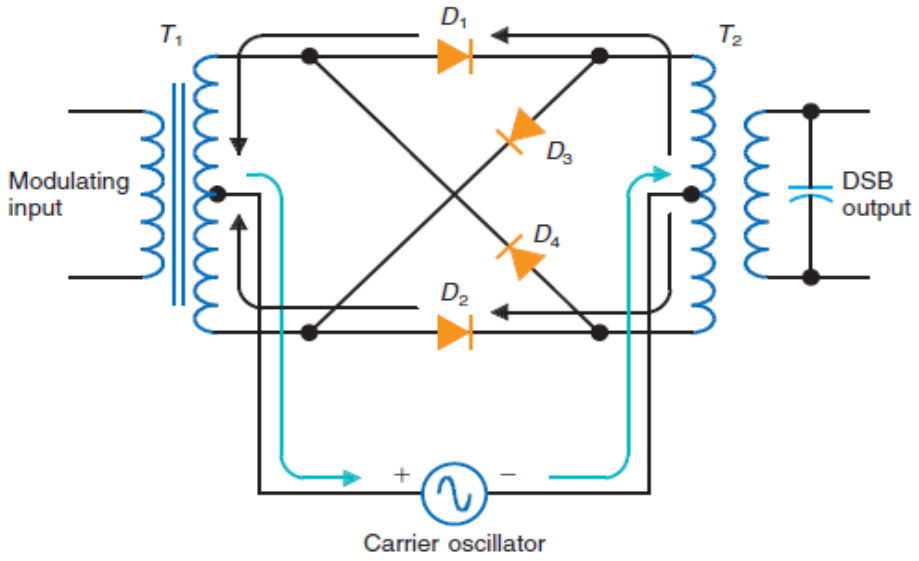


(a)



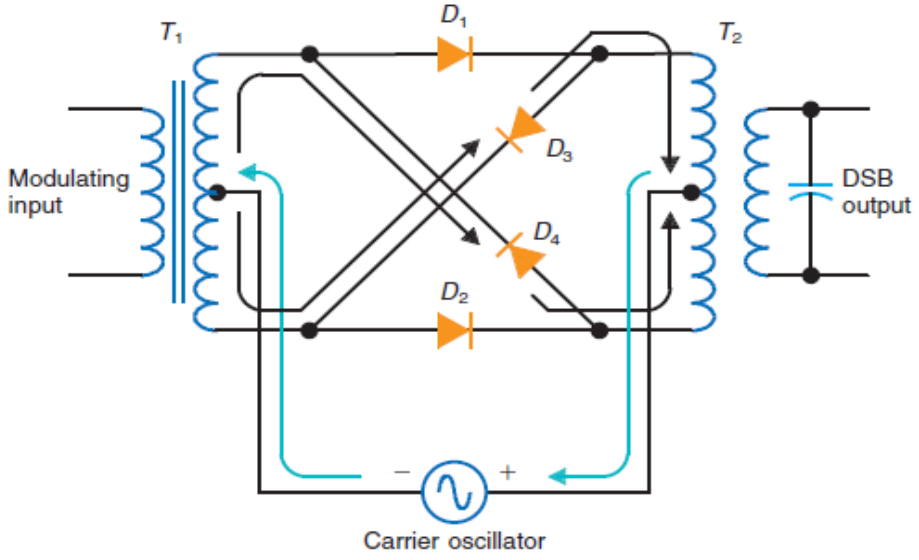
(b)

The operation of the lattice modulator is relatively simple. The carrier sine wave, which is usually considerably higher in frequency and amplitude than the modulating signal, is used as a source of forward and reverse bias for the diodes. The carrier turns the diodes off and on at a high rate of speed, and the diodes act as switches that connect the modulating signal at the secondary of T_1 to the primary of T_2.



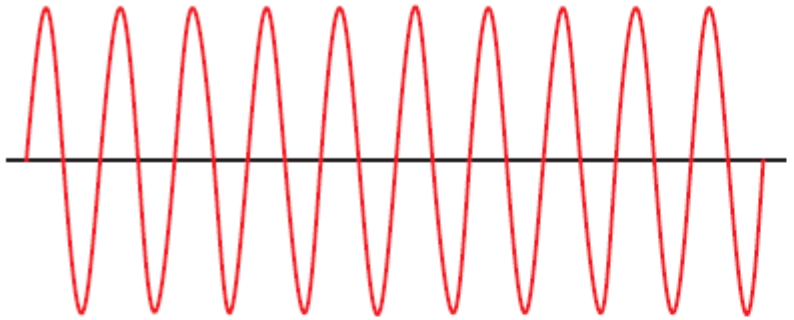
(a)

➔ Assume that the modulating input is zero. When the polarity of the carrier is positive, as illustrated in next slide figure (*a*), diodes D_1 and D_2 are forward-biased. At this time, D_3 and D_4 are reverse-biased and act as open circuits. As you can see, current divides equally in the upper and lower portions of the primary winding of T_2. The current in the upper part of the winding produces a magnetic field that is equal and opposite to the magnetic field produced by the current in the lower half of the secondary. The magnetic fields thus cancel each other out. No output is induced in the secondary, and the carrier is effectively suppressed.

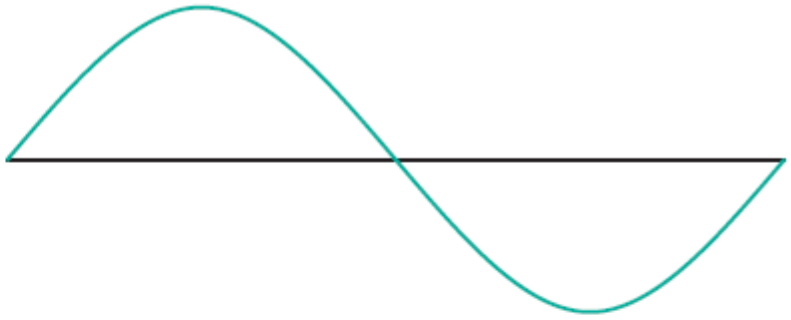


(b)

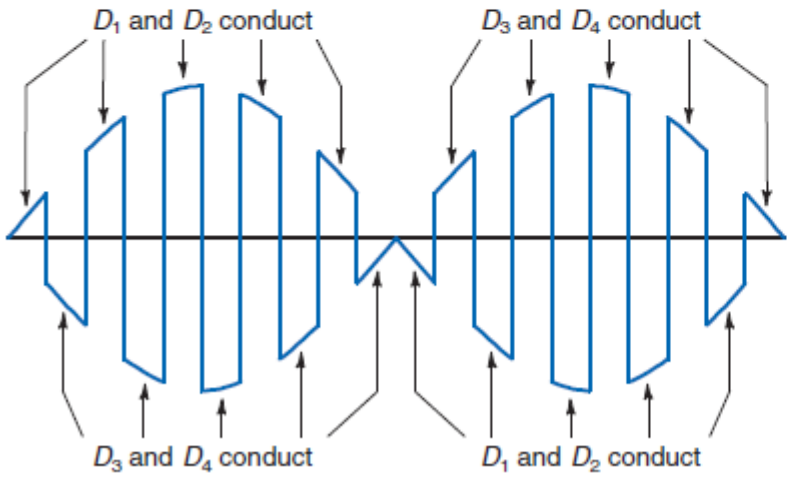
When the polarity of the carrier reverses, diodes D_1 and D_2 are reverse-biased and diodes D_3 and D_4 conduct. Again, the current flows in the secondary winding of T_1 and the primary winding of T_2. The equal and opposite magnetic fields produced in T_2 cancel each other out. The carrier is effectively balanced out, and its output is zero. The degree of carrier suppression depends on the degree of precision with which the transformers are made and the placement of the center tap: the goal is exactly equal upper and lower currents and perfect magnetic field cancellation. The degree of carrier attenuation also depends upon the diodes. The greatest carrier suppression occurs when the diode characteristics are perfectly matched. A carrier suppression of 40 dB is achievable with well-balanced components.



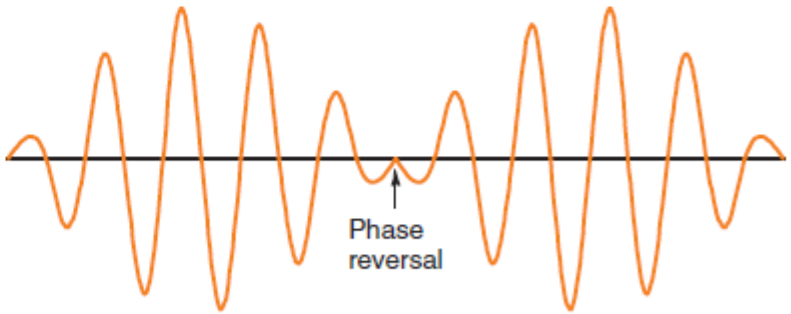
(a)



(b)



(c)



(d)

Now assume that a low-frequency sine wave is applied to the primary of T_1 as the modulating signal. The modulating signal appears across the secondary of T_1. The diode switches connect the secondary of T_1 to the primary of T_2 at different times depending upon the carrier polarity. When the carrier polarity is as shown in previous Fig., diodes D_1 and D_2 conduct and act as closed switches. At this time, D_3 and D_4 are reverse-biased and are effectively not in the circuit. As a result, the modulating signal at the secondary of T_1 is applied to the primary of T_2 through D_1 and D_2.

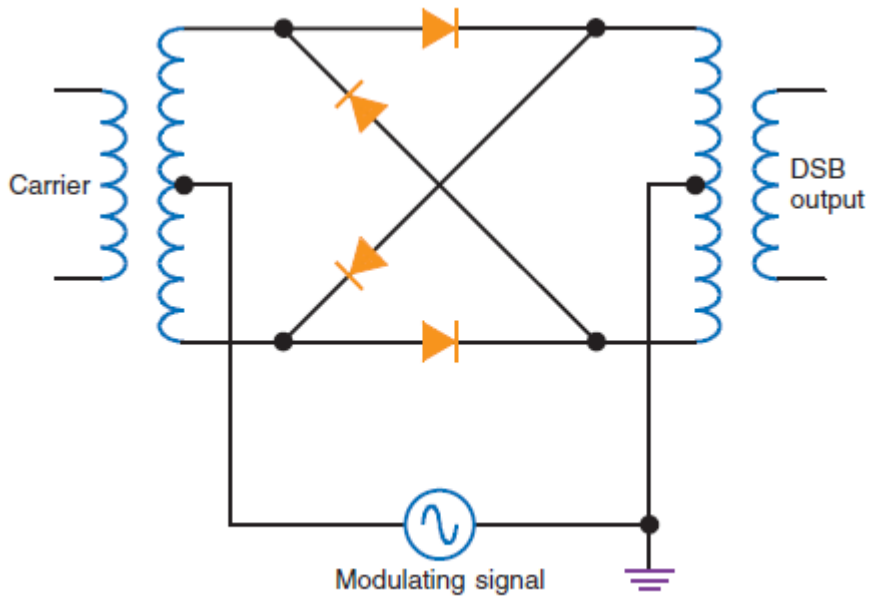
When the carrier polarity reverses, D_1 and D_2 cut off and D_3 and D_4 conduct. Again, a portion of the modulating signal at the secondary of T_1 is applied to the primary of T_2, but this time the leads have been effectively reversed because of the connections of D_3 and D_4. The result is a 180° phase reversal. With this connection, if the modulating signal is positive, the output will be negative, and vice versa.

The carrier is operating at a considerably higher frequency than the modulating signal. Therefore, the diodes switch off and on at a high rate of speed, causing portions of the modulating signal to be passed through the diodes at different times. The DSB signal appearing across the primary of T_2 is illustrated in Fig. (*c*) in previous slide. The steep rise and fall of the waveform are caused by the rapid switching of the diodes. Because of the switching action, the waveform contains harmonics of the carrier. Ordinarily, the secondary of *T*2 is a resonant circuit as shown, and therefore the high-frequency harmonic content is filtered out, leaving a DSB signal like that shown in Fig.(*d*).

There are several important things to notice about this signal. First, the output waveform occurs at the carrier frequency. This is true even though the carrier has been removed. If two sine waves occurring at the sideband frequencies are added algebraically, the result is a sine wave signal at the carrier frequency with the amplitude variation shown in Fig. (*c*) or (*d*). Observe that the envelope of the output signal is *not* the shape of the modulating signal. Note also the phase reversal of the signal in the very center of the waveform, which is one indication that the signal being observed is a true DSB signal.

Although lattice modulators can be constructed of discrete components, they are usually available in a single module containing the transformers and diodes in a sealed package. The unit can be used as an individual component. The transformers are carefully balanced, and matched hot-carrier diodes are used to provide a wide operating frequency range and superior carrier suppression.

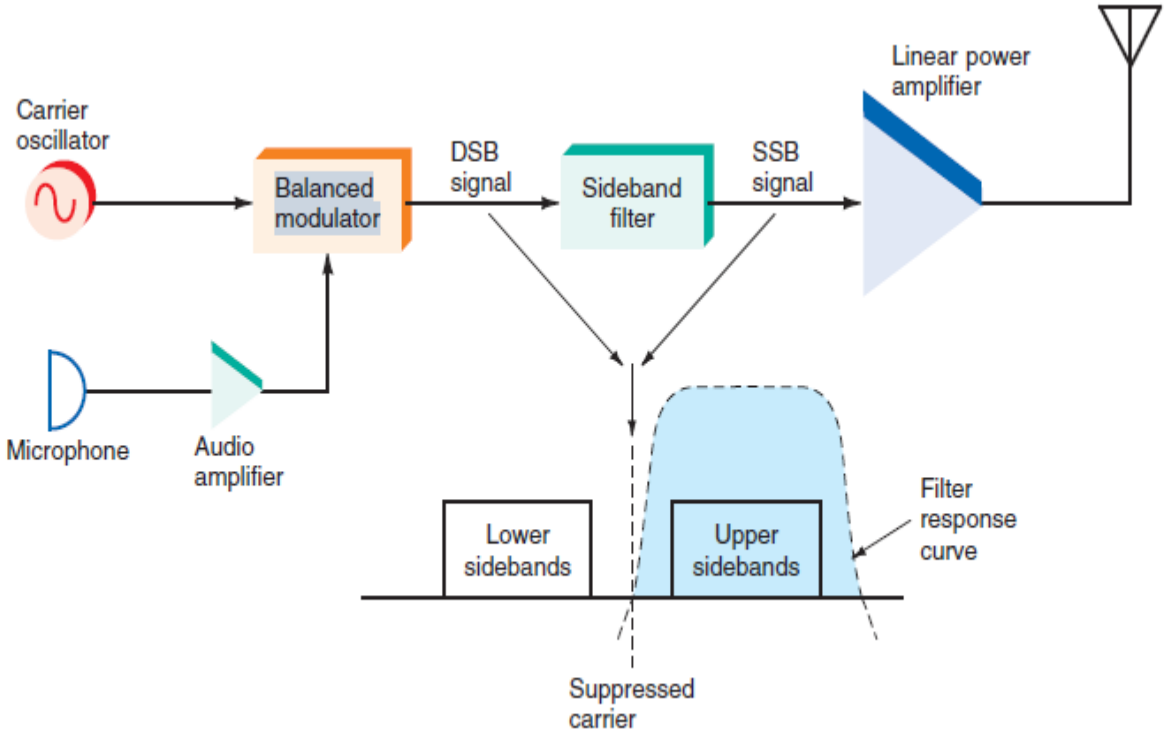
The diode lattice modulator uses one low-frequency iron-core transformer for the modulating signal and an air-core transformer for the RF output. This is an inconvenient arrangement because the low-frequency transformer is large and expensive. More commonly, two RF transformers are used, as shown in the next figure. where the modulating signal is applied to the center taps of the RF transformers. The operation of this circuit is similar to that of other lattice modulators.



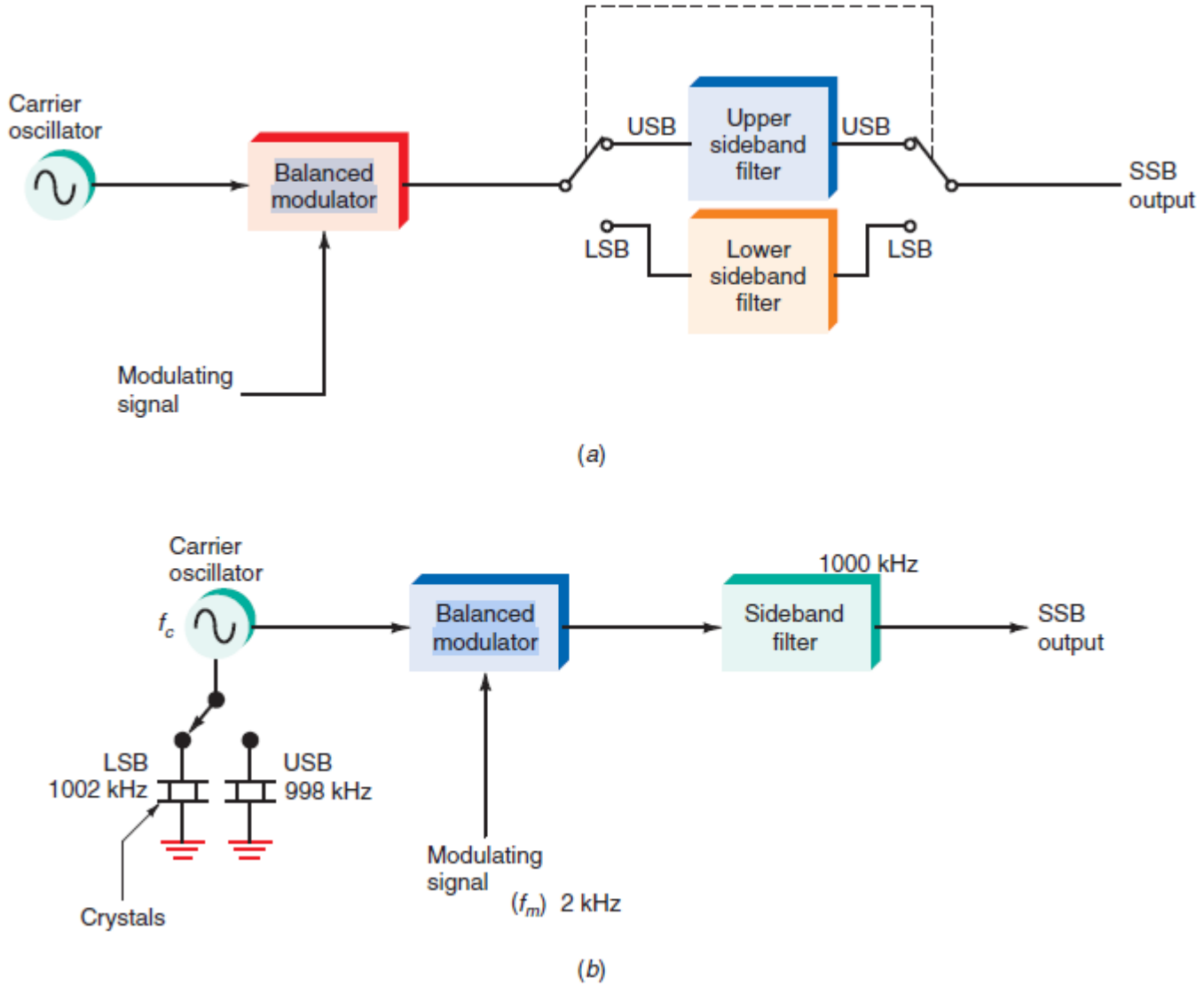
SSB Circuits

The simplest and most widely used method of generating SSB signals is the filter method. Fig. below shows a general block diagram of an SSB transmitter using the filter method. The modulating signal, usually voice from a microphone, is applied to the audio amplifier, the output of which is fed to one input of a balanced modulator. A crystal oscillator provides the carrier signal, which is also applied to the balanced modulator. The output of the balanced modulator is a *double-sideband (DSB)* signal. An SSB signal is produced by passing the DSB signal through a highly selective bandpass fi lter that selects either the upper or lower sideband.

The primary requirement of the filter is, of course, that it pass only the desired sideband. Filters are usually designed with a bandwidth of approximately 2.5 to 3 kHz, making them wide enough to pass only standard voice frequencies. The sides of the filter response curve are extremely steep, providing for excellent selectivity. Filters are fixed-tuned devices; i.e., the frequencies they can pass are not alterable. Therefore, the carrier oscillator frequency must be chosen so that the sidebands fall within the filter bandpass. Many commercially available filters are tuned to the 455-kHz, 3.35-MHz, or 9-MHz frequency ranges, although other frequencies are also used. Digital signal processing (DSP) filters are also used in modern equipment.



With the filter method, it is necessary to select either the upper or the lower sideband. Since the same information is contained in both sidebands, it generally makes no difference which one is selected, provided that the same sideband is used in both transmitter and receiver. However, the choice of the upper or lower sideband as a standard varies from service to service, and it is necessary to know which has been used to properly receive an SSB signal. There are two methods of sideband selection. Many transmitters simply contain two filters, one that will pass the upper sideband and another that will pass the lower sideband, and a switch is used to select the desired sideband [Fig. (*a*)]. An alternative method is tc provide two carrier oscillator frequencies. Two crystals change the carrier oscillator frequency to force either the upper sideband or the lower sideband to appear in the filter bandpass [see Fig.(*b*)].



As an example, assume that a bandpass filter is fixed at 1000 kHz and the modulating signal f_m is 2 kHz. The balanced modulator generates the sum and difference frequencies.

As an example, assume that a bandpass filter is fixed at 1000 kHz and the modulating signal f_m is 2 kHz. The balanced modulator generates the sum and difference frequencies. Therefore, the carrier frequency f_c must be chosen so that the USB or LSB is at 1000 kHz. The balanced modulator outputs are USB $= f_c + f_m$ and LSB $= f_c - f_m$.

To set the USB at 1000 kHz, the carrier must be $f_c + f_m = 1000, f_c + 2 = 1000$, and $f_c = 1000 - 2 = 998$ kHz. To set the LSB at 1000 kHz, the carrier must be $f_c - f_m = 1000, f_c - 2 = 1000$, and $f_c = 1000 + 2 = 1002$ kHz.

Crystal filters, which are low in cost and relatively simple to design, are by far the most commonly used filters in SSB transmitters. Their very high Q provides extremely good selectivity. Ceramic filters are used in some designs. Typical center frequencies are 455 kHz and 10.7 MHz. DSP filters are also used in contemporary designs.

Example: An SSB transmitter using the fi lter method of Fig. 4-30 operates at a frequency of 4.2 MHz. The voice frequency range is 300 to 3400 Hz.

a. Calculate the upper and lower sideband ranges.

Upper sideband

$$\text{Lower limit } f_{LL} = f_c + 300 = 4{,}200{,}000 + 300 = 4{,}200{,}300 \text{ Hz}$$

$$\text{Upper limit } f_{UL} = f_c + 3400 = 4{,}200{,}000 + 3400$$

$$= 4{,}203{,}400 \text{ Hz}$$

$$\text{Range, USB} = 4{,}200{,}300 \text{ to } 4{,}203{,}400 \text{ Hz}$$

Lower sideband

$$\text{Lower limit } f_{LL} = f_c - 300 = 4{,}200{,}000 - 300 = 4{,}199{,}700 \text{ Hz}$$

$$\text{Upper limit } f_{UL} = f_c - 3400 = 4{,}200{,}000 - 3400$$

$$= 4{,}196{,}600 \text{ Hz}$$

$$\text{Range, LSB} = 4{,}196{,}000 \text{ to } 4{,}199{,}700 \text{ Hz}$$

b. What should be the approximate center frequency of a bandpass filter to select the lower sideband? The equation for the center frequency of the lower sideband f_{LSB} is

$$f_{LSB} = \sqrt{f_{LL}\, f_{UL}} = \sqrt{4{,}196{,}660 \times 4{,}199{,}700} = 4{,}198{,}149.7 \text{ Hz}$$

An approximation is

$$f_{LSB} = \frac{f_{LL} + f_{UL}}{2} = \frac{4{,}196{,}600 + 4{,}199{,}700}{2} = 4{,}198{,}150 \text{ Hz}$$

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- Communication Electronics 3/e by Louis Frenzel | 2001
- Communication Circuits Analysis and Design, by Clarke Hess