General Lab Rules

- Be **PUNCTUAL** for your laboratory session.
- Foods, drinks and smoking are NOT allowed.
- Open-toed shoes are NOT allowed.
- The lab timetable must be strictly followed. Prior permission from the Lab Supervisor must be obtained if any change is to be made.
- Experiment must be completed within the given time.
- Respect the laboratory and its other users. Noise must be kept to a minimum.
- Workspace must be kept clean and tidy at all time. Points might be taken off on student/group who fail to follow this.
- Handle all apparatus with care.
- All students are liable for any damage to equipment due to their own negligence.
- At the end of your experiment make sure to switch off all the instruments.
- Students are strictly PROHIBITED from taking out any items from the laboratory without permission from the Lab Supervisor.
- Students are NOT allowed to work alone in the laboratory.
- Please consult the Lab Supervisor if you are not sure on how to operate the laboratory equipment.
- Report immediately to the Lab Supervisor if any injury occurred.
- Report immediately to the Lab Supervisor any damages to equipment, hazards, and potential hazards.
- Please refer to the Lab Supervisor should there be any concerns regarding the laboratory.

Grading Policy

The total mark for this lab is distributed as follows

Lab Report	20%
Quizzes	10%
Prelab	5%
Attendance	5%
Mid-term Exam	20%
Final Exam	40%

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Guidelines for Writing Lab Report

The most effective way to acquire the practical skills in engineering studies is usually by experimenting in a laboratory. The process of experimentation involves organization, observation, familiarization with various pieces of equipment, working with others, writing, and communicating ideas and information. These are the skills required of an engineer.

In a practical situation, such as that in the industry or university research, experiments are designed for the purpose of clarifying research questions or conflicting theories by means of collecting a series of data. The conclusions drawn from that data can be used to validate a theory or sometimes to develop a theory that explains the behavior of an engineering object. The report for this kind of experiments must includes an introduction to the topic and purpose of the experiment, the theory, method, procedure, equipment used in the experiment, the data presented in an organized manner, and the conclusions based on the data gathered.

In engineering education, lab experiments are usually designed to enhance the understanding in engineering topics. Students are supposed to "dirty their hand" in preparing the experiment setup, organize the experiment flow, and learn to observe the salient features as well as to spot any unexpected occurrence as part of the training to acquire the practical skill to become an engineer. Although the introduction and the procedure are usually given in the lab handouts, students should practice writing a proper lab report which includes all the necessary sections, targeting at a reader who does not have any prior knowledge about the experiment. This is to develop the skill in documenting the laboratory work and communicating that experience to others. This write-up gives some guidelines on what to write in each section in preparing laboratory reports for engineering curricula.

Title Page

The title page should contain the title of the experiment, the code and title of the course, the name of the writer, the date when the experimental work was performed, submission date of the lab report, and the name of lecturer for whom the report is prepared for.

Introduction or Objectives

An introduction is necessary to give an overview of the overall topic and the purpose of the report. The motivation to the initialization of the experimental work can be included. Its content should be general enough to orientate the reader gracefully into the subject materials.

Theoretical Background

This section is to discuss the theoretical aspects leading to the experiment. Typically, this involves the historical background of the theories published in the research literature and the questions or ambiguities arose in these theoretical work. Citations for the sources of information should be given in one of the standard bibliographic formats (for example, using square brackets with the corresponding number [2] that points to the List of References). Explore this background to prepare the readers to read the main body of the report. It should contain sufficient materials to enable the

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readers to understand why the set of data are collected, and what are the salient features to observe in the graph, charts and tables presented in the later sections.

Depending on the length and complexity of the report, the introduction and the theoretical background may be combined into one introductory section.

Experimental Method, Procedure and Equipment

This section describes the approach and the equipment used to conduct the experiment. It explains the function of each apparatus and how the configuration works to perform a particular measurement. Students should not recopy the procedures of the experiment from the lab handout, but to summarize and explain the methodology in a few paragraphs.

Observations, Data, Findings, Results

The data should be organized and presented in the forms of graphs, charts, or tables in this section, without interpretive discussion. Raw data which may take up a few pages, and most probably won't interest any reader, could be placed in the appendices.

Calculations and Analysis

The interpretation of the data gathered can be discussed in this section. Sample calculations may be included to show the correlation between the theory and the measurement results. If there exists any discrepancy between the theoretical and experimental results, an analysis or discussion should follow to explain the possible sources of error.

The experimental data and the discussions may also be combined into one section, for example, under the heading called "Discussion of Experimental Results".

Conclusions

The conclusions section closes the report by providing a summary to the content in the report. It indicates what is shown by the experimental work, what is its significance, and what are the advantages and limitations of the information presented. The potential applications of the results and recommendations for future work may be included.

Appendices

The appendices are used to present derivations of formulae, computer program source codes, raw data, and other related information that supports the topic of the report.

List of References

The sources of information are usually arranged and numbered according to the order they are cited in the report. The reference materials may be entered in the following formats:

[1] Author, "Title of the book", 2nd edition, New York: Publisher, 1989.
[2] Author, "Title of the paper", Journal name, Vol. 2, No. 3, Jan 1990, pg. 456-458.
[3] Author, "Title of the paper", Proceedings of Conference 1991, pg. 5-6.
[4] Author, "Title of the thesis", Ph.D. thesis, Rice University, Houston, May 1973.

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Lab Session 1

Diode Characteristics

OBJECTIVES:

After completing this experiment, you should be able to:

- Measure the forward voltage across a diode, and determine if the component is faulty.
- Demonstrate the forward current and voltage characteristics of *pn*-junction and zener diodes.
- Demonstrate the reverse current and voltage characteristics of *pn*-junction and zener diodes.

SUMMARY OF THEORY:

The diode is a semiconductor device that conducts currents much more readily in one direction than in the other. The voltage across the diode terminals determines whether or not the diode will conduct. If the anode is more positive than the cathode, the diode will conduct currents and is said to be forward-biased. As *forward current* (I_F) increases, so does *forward voltage* (V_F) across the device. However, V_F increases at a much lower rate than I_F, because the forward resistance of a diode *decreases* as the I_F increases. Hence, V_F increases at a very low rate when a diode is operated above its *knee voltage* (V_γ). This is true of *pn* junction diodes, zener diodes, and even LEDs.

The following formula is used to calculate the dynamic or AC resistance of the diode:

Where:

$$r_D = \frac{\Delta V}{\Delta I} \qquad (1)$$

ΔV: The small change in voltage across the diode.
ΔI: The corresponding change in current through the diode.

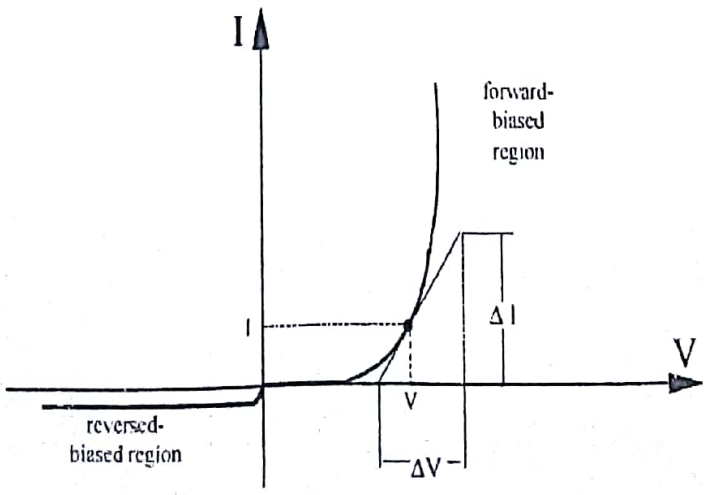

Fig.1: I-V Characteristic of Normal Diode.

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The static or DC resistance at any point along the characteristic curve is calculated using Ohm's law:

$$R_D = \frac{V}{I} \quad (2)$$

Where:

V: The voltage across the diode.
I: The current through the diode.

These relationships can be seen in the characteristic curve shown in Figure1.

If the cathode is more positive than the anode, the diode will conduct only an extremely small leakage current and is said to be reversed-biased. When a *pn*-junction diode is reverse biased. the *reverse current* (I_R) through the device is extremely low, even with a significant reverse voltage applied. This is not necessarily the case with a *zener diode.* Zener reverse current remains low until V_R reaches the *zener voltage* (V_Z) rating of the component. When the magnitude of V_R reaches V_Z, I_R increases abruptly. The forward and reverse characteristics of *pn*-junction and zener diodes are the focus of the second part of this experiment.

A diode can be tested using a simple ohmmeter, but this is not a very accurate test. Most modern multimeters have a diode-checker function, which allows you to determine the actual voltage across a forward-biased diode. If the forward voltage falls within its expected range, the diode is considered good. If the diode test indicates the component is shorted or open, then the diode should be replaced.

MATERIALS:

1. Function Generator
2. Variable DC Power Supply
3. Digital Multimeter, DMM (with diode-check function)
4. Breadboard
5. 1N4001 Small Signal Diode
6. 1N5240 Zener Diode
7. Resistors

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PROCEDURE:

Part 1: Diode Testing

Note: The schematic and component symbols for *pn*-junction and zener diodes are shown in Figure 2. Note that the indicator band on the component is always closest to the cathode terminal.

1. Set your DMM to the diode test position.

2. Connect the DMM to the 1N4001 diode as shown in Figure 2a. Measure the forward voltage (V_F) across the diode, and record your measurement in Table1.

Diode	V_F	V_R
1N4001 Normal Diode		
1N5240 Zener Diode		

Table1: Diode Test Measurements

3. Reverse the diode as shown in Figure 2a. Measure its reverse voltage (V_R), and record this reading in Table 1.

4. Repeat Steps (2) and (3) for the 1N5240 zener diode. Record the meter readings in Table 1.

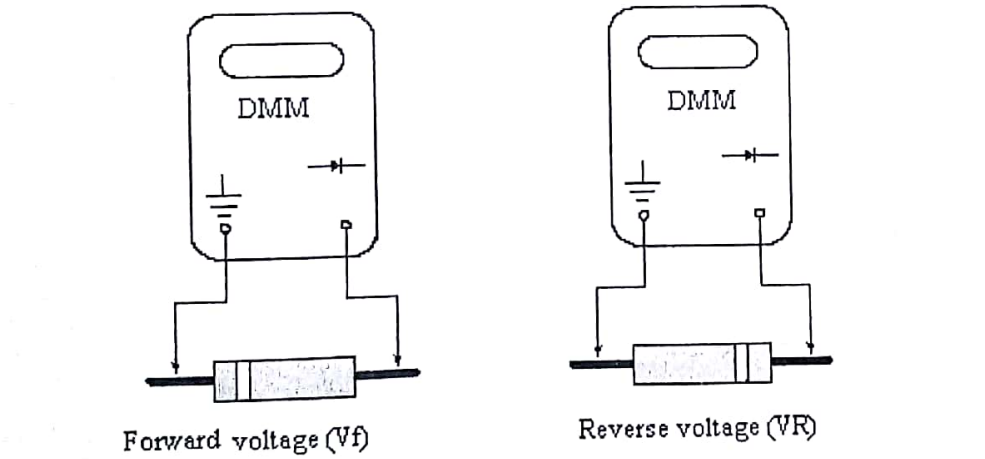

Fig.2: (a) Diode Testing (b) Diode Symbols

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Part 2: Diode Voltage and Current Characteristics:

5. Construct the circuit shown in Figure 3. The voltage source should be set initially to 0.0 V. R_1 limits the diode current to a value lower than the rated maximum forward current.

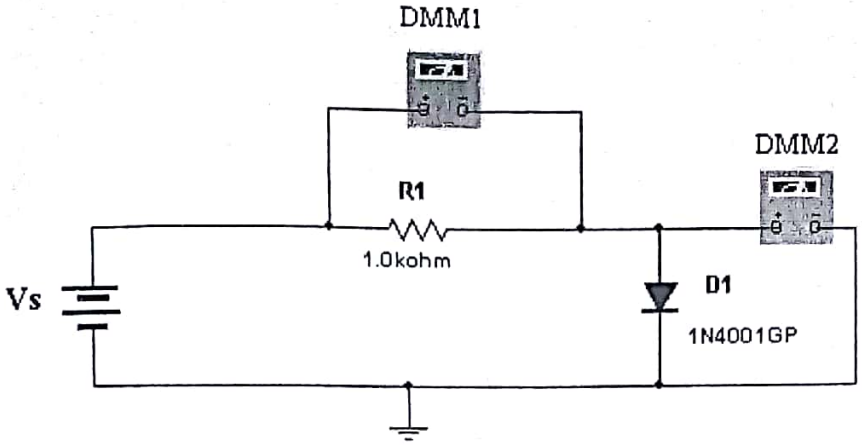

Fig.3: Measurement of the Forward Characteristics of Diode.

6. Measure V_F, V_{RI}, and compute I_F. Record these values in Table 2.

7. Repeat Step (6) for all the voltage values listed in Table 2.

8. Replace the normal diode with a zener diode. Repeat Steps (6) and (7) for the 1N5240 zener diode.

V_S (volt)	V_{RI} (volt)		V_F (volt)		$I_F = V_R / R$ (mA)	
	Normal	Zener	Normal	Zener	Normal	Zener
0.0						
0.2						
0.4						
0.6						
1.0						
3.0						
5.0						
7.0						
9.0						
11.0						
13.0						

Table2: Diode Forward Currents and Voltages

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9. Use your results from Table 2 to plot the I_F versus V_F curve for both diodes in Figure 4.

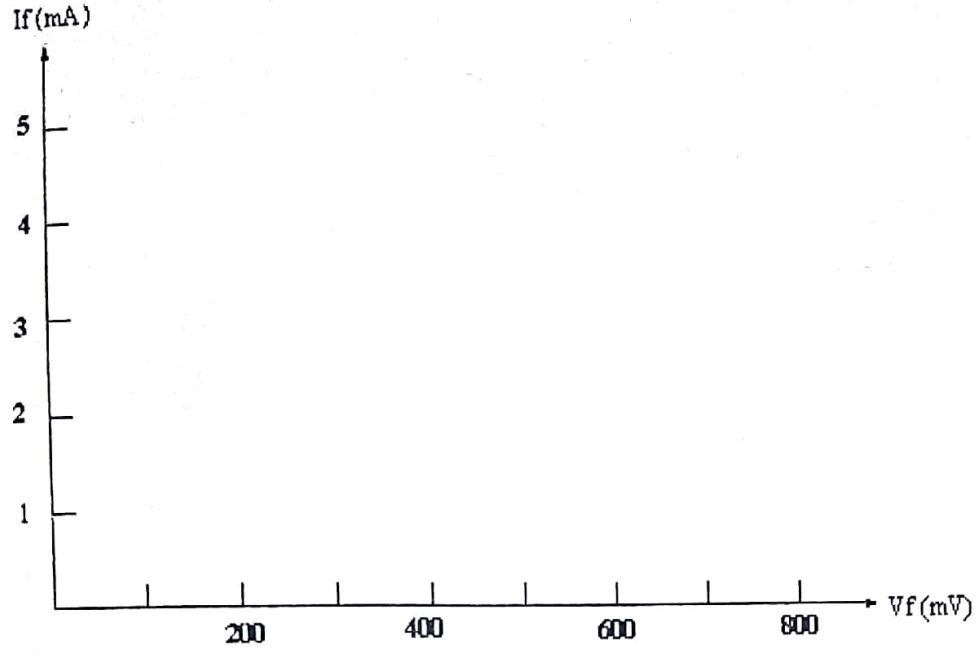

Fig.4: I_F versus V_F

10. Determine the static resistance of the normal diode at 1, 3, 5 and 10 volts using values obtained for I_F and V_F from Table l.

11. Graphically determine the dynamic resistance of the normal diode at 1, 3, 5, 7, and 13 volts using the I-V characteristic curve obtained in Figure 4.

12. To obtain the I-V characteristics of the diode using the oscilloscope, connect the circuit shown in Figure 5 below. Set the function generator to 10 V_{P-P}, 1KHz sinusoid input signal.

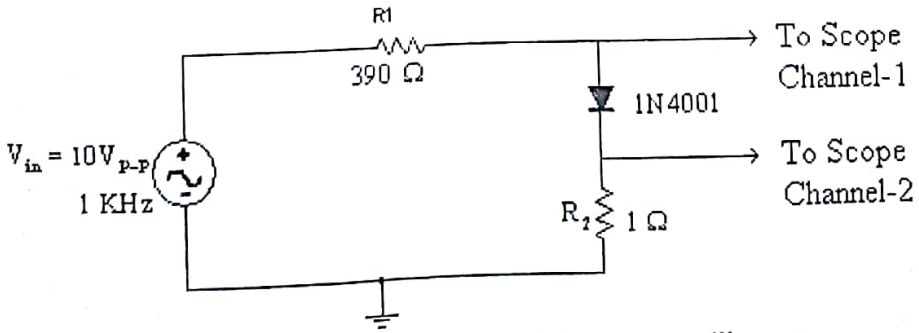

Fig.5: Measurement of I-V Characteristics using Oscilloscope

13. Set the oscilloscope to the x-y mode. Connect the horizontal input of the oscilloscope channel-l to the anode of the diode and the vertical input channel_2 to the cathode. Set the sensitivity of the vertical input to 10 mV/division and set the horizontal sensitivity at l mV/division. Draw the curve shown on the screen of the oscilloscope and find the junction potential.

14. Compare these results with the table you made.

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15. Construct the circuit shown in Figure 6. Note that the 1N4001 diode is now reverse biased.

16. Measure and record V_{RI}. Use this value (and the measured value of R_1) to calculate I_{RI}. This equals the reverse current through the diode.

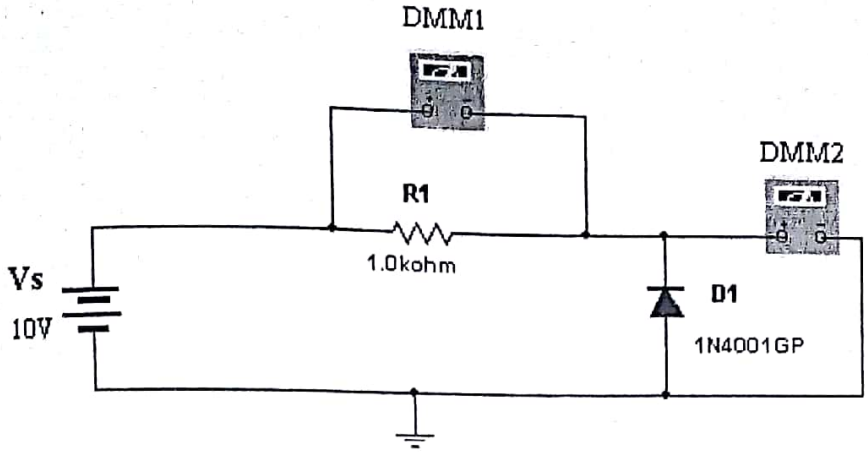

Fig.6: Measurement of I_{RI}

17. Construct the circuit shown in Figure 7.

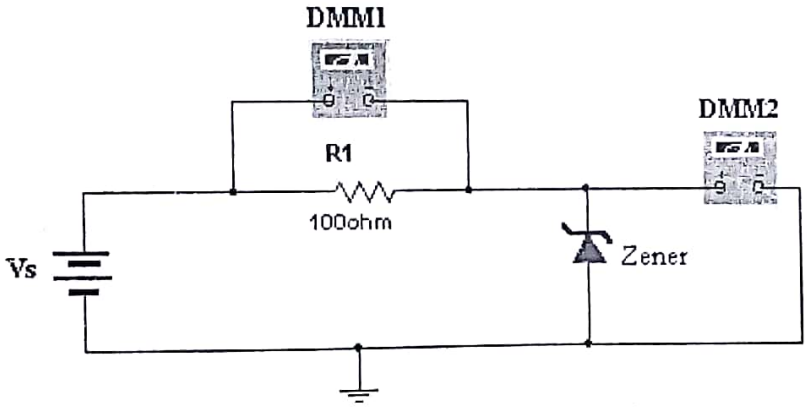

Fig.7: Zener Diode Test Circuit

18. Measure the voltage across the zener diode, and record this value in Table 3. Repeat this procedure for all the voltage values listed in the table.

V_S (volt)	V_{RI} (volt)	Vz (volt)	$I_Z = V_{RI} / R_I$ (mA)
0			
0.2			
0.4			
0.6			
1.0			
3.0			
5.0			
7.0			
9.0			
10.0			
12.0			
14.0			

Table.3: Measurement of V_{RI} and Vz

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19. Use the values from Table 3 to plot the I_Z versus V_Z curve in Figure 8.

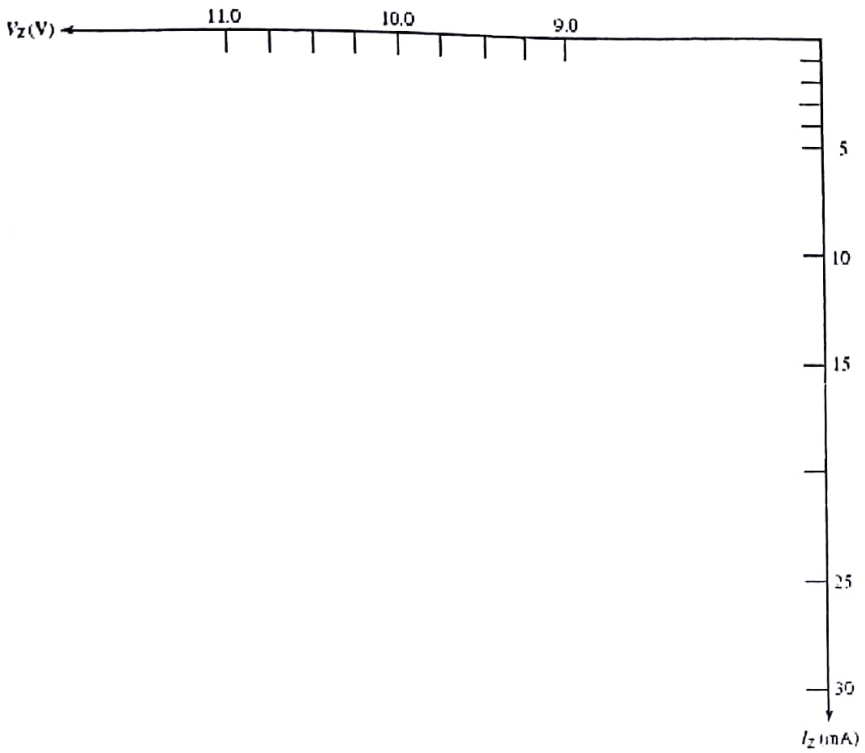

Fig.8: Zener Reverse Operating Curve.

20. Determine the internal DC resistance R_Z of your zener diode by taking the change in zener voltage, V_Z, divided by the corresponding change in current, I_Z.

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QUESTIONS & PROBLEMS:

1. Refer to your graphs in Figure 4. Compare the forward characteristics of the two diodes. Explain why they are so similar (or dissimilar).

2. Refer to your results in Table 3. Explain how you could use these results to calculate the zener impedance of this 1N5240 zener diode.

3. From step (18). what is the difference between this Zener diode and the normal diode you measured previously? Can you tell the difference between a normal diode and a Zener diode by looking to their characteristic charts?

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Lab Session 2

Diode Applications: Rectifiers, Filters, Clipper and Clamper

OBJECTIVES:

After performing this experiment, you should be able to:

- Demonstrate the strengths and weaknesses of the two basic rectifier circuits.
- Draw the output waveforms for the two basic rectifier circuits.
- Demonstrate the effect and benefit of filtering on rectifier circuits.
- Demonstrate the operation of the shunt clipper circuit.
- Demonstrate the operation of the diode clamper circuit.

SUMMARY OF THEORY:

Part 1: Rectifiers and Filters

The most popular application of the diode is the *rectification*. Rectification is simply defined as: the conversion of alternating current (AC) to direct current (DC). This almost always involves the use of some devices that conduct in only one direction, so one polarity of an AC signal, which has zero average (DC) level, can be eliminated resulting in net DC component. As we have seen in the previous experiment, this is exactly what a semiconductor diode does. This process can be used to make power supplies, peak detectors, and amplitude modulators.

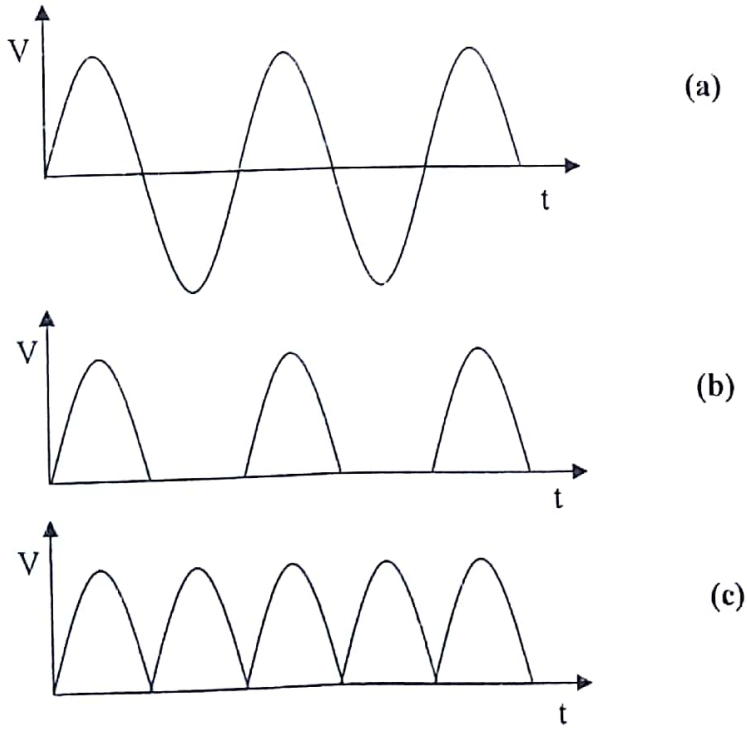

Fig. 1: (a) Input Waveform, (b) Half-Wave Rectified Waveform and (c) Full-Wave Rectified Waveform

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The three basic rectifier configurations are the half-wave, full-wave, and bridge rectifiers. The output of a positive half-wave rectifier is shown in Figure1(b). Figure1(c) shows the output of a positive full-wave, or bridge rectifier.

In any case of rectification the amount of AC voltage mixed with the rectifier's DC output is called *ripple voltage*. In most cases, since "pure" DC is the desired goal, ripple voltage is undesirable or unwanted. If the power levels are not too great, filtering networks that are composed of suitably connected capacitors and inductors may be employed to reduce the amount of ripple in the output voltage. We will be discussing and using only the simple capacitor filter. A measure of the effectiveness of a filter is given by *ripple factor* (r), which is defined as the ratio of the peak-peak value of the AC component to the DC or average value. That is

$$r = \frac{V_r}{V_{avg}} \qquad (1)$$

It is desirable and important to make ripple factor as small as possible.

The capacitor filter is the simplest filter circuit with a capacitor in parallel to the load resistor R_L. The capacitor is charged to the peak value of the rectified voltage V_p and begins to discharge through load resistance R_L after the rectified voltage decreases from the peak value. The rate of decrease in the capacitor voltage between charging pulses depends upon the relative values of time constant *RC* and the period of the input voltage. The large time constant results in slower decrease and hence smaller ripple component. The concept of capacitor filter is illustrated in Figure 2. The disadvantages of the capacitor filter lies in: (a) poor regulation and (b) increased ripple at large loads.

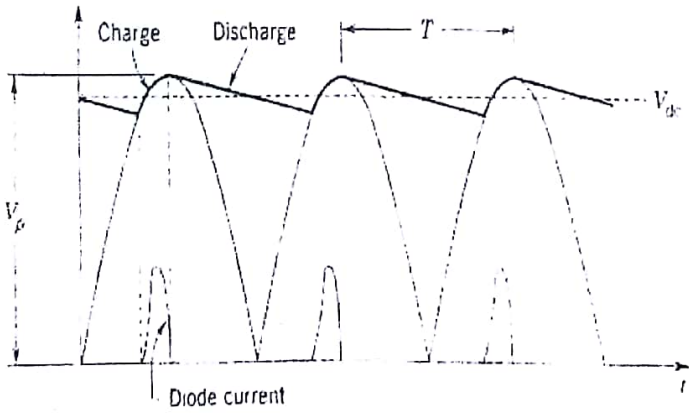

Fig. 2: Output Voltage Capacitor Filter is a DC Voltage and Small Triangular Ripple Voltage.

For most power applications, half-wave rectification is insufficient for the task. The harmonic content of the rectifier's output waveform is very large and consequently difficult to filter. Furthermore, AC power source only works to supply power to the load once every half-cycle, meaning that much of its capacity is unused. Half-wave rectification is, however, a very simple way to reduce power to the resistive load.

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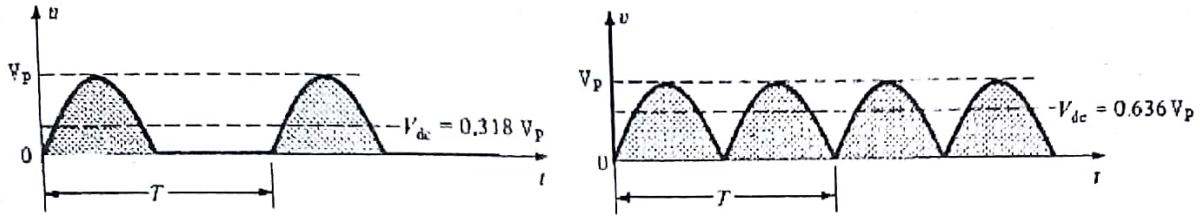
The half-wave voltage signal of Figure 3(a) normally established by a network with a single diode has an average or equivalent DC voltage level equal to 31.8% of the peak voltage V_p.
That is,

$$V_{avg} = \frac{V_p}{\pi} = 0.318\ V_{peak}\ \text{Volts}\big|_{\text{Half-wave}} \qquad (2)$$

The full-wave rectified signal of Figure 3(b) has twice the average or DC level of the half-way signal, or 63:6% of the peak value V_p.
That is,

$$V_{avg} = \frac{2\ V_p}{\pi} = 0.636\ V_{peak}\ \text{Volts}\big|_{\text{Full-wave}} \qquad (3)$$



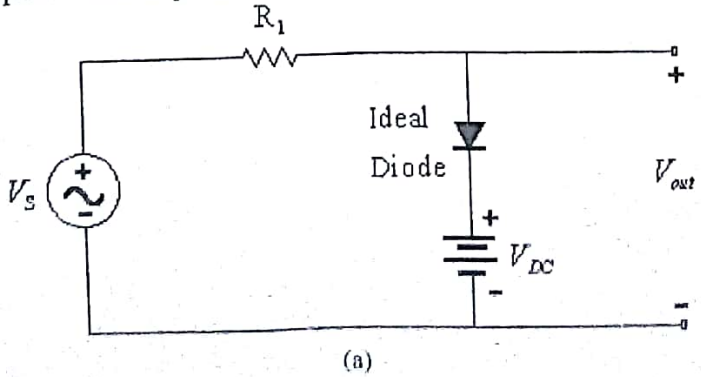
(a) (b)

Fig.3: (a) Half-Wave Rectifier (b) Full-Wave Rectifier.

In rectification systems the peak inverse voltage (PIV) or Zener breakdown voltage parameter must be considered carefully. The PIV voltage is the maximum reverse-bias voltage that a diode voltage can handle before entering the Zener breakdown region. For ideal single-diode half-wave rectification systems, the required PIV level is equal to the peak value of the applied sinusoidal signal. For the four-diode full-wave bridge rectification system, the required PIV level is again the peak value, but for a two-diode center- tapped configuration, it is twice the peak value of the applied signal.

Part 2: Clippers and Clampers

The primary function of clippers is to "clip" away a portion of an applied alternating signal. The process is typically performed by a resistor-diode combination. DC batteries are also used to provide additional shifts or "cuts" of the applied voltage. The half-wave rectifier is a simple *series* clipper. It "clips" either the positive or the negative alternation of its input waveform, depending on the polarity of the diode. Since we examined series clipper operation in the rectifier experiment, we will focus on the *shunt* clipper in this experiment.



(a)

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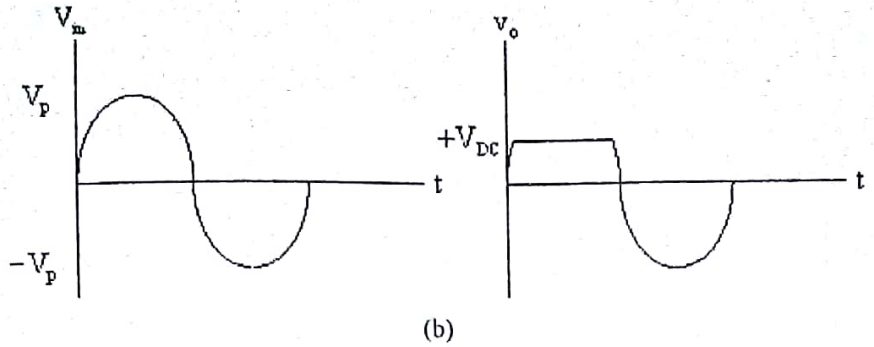
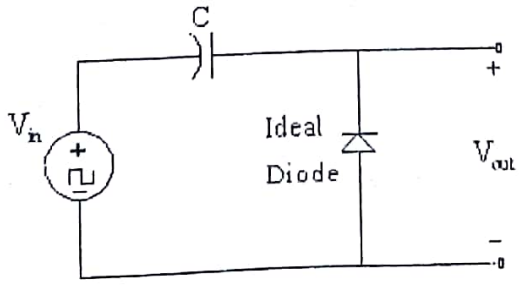


(b)

Fig.4: (a) Clipping Circuit (b) Input and Output Waveforms.

A typical clipper circuit is shown in Figure 4(a). In this circuit the output voltage can never be greater than the value of V_{DC}. The ideal diode becomes forward biased at V_S equal to V_{DC} and this ties the output directly to the V_{DC} supply as shown in Figure 4 (b). Often in the development of electronic circuits it is required that voltages be limited in some manner to avoid circuit damage. Furthermore, the limiting or clipping of voltages can be very useful in the development of wave-shaping circuits.

The *clamper* is a diode circuit used to change the *DC reference* of a waveform *without significantly altering the shape of that waveform.* The *positive* clamper shifts its input waveform in the positive direction; the *negative* clamper shifts it in the negative direction. The negative clamper is identical to the positive clamper except for the polarity of the diode and capacitor. Clampers are easily distinguished from clippers in that they include a capacitive element. A typical clamper as shown in Figure 5(a) includes a capacitor, diode, and resistor with some also having a DC battery. This circuit works by allowing the capacitor to charge up and act like a battery. This is the voltage across the capacitor depends on the input waveform, the output maximum (or the minimum depending on the orientation of the diode) will be clamped to a fixed reference point. The only design constraint is that $2\pi RC$ be five times larger than the period of the input waveform.
Observe that the output voltage is simply the input voltage shifted by the value of steady state offset (V_{DC}) as shown in Figure 5(b).



(a)

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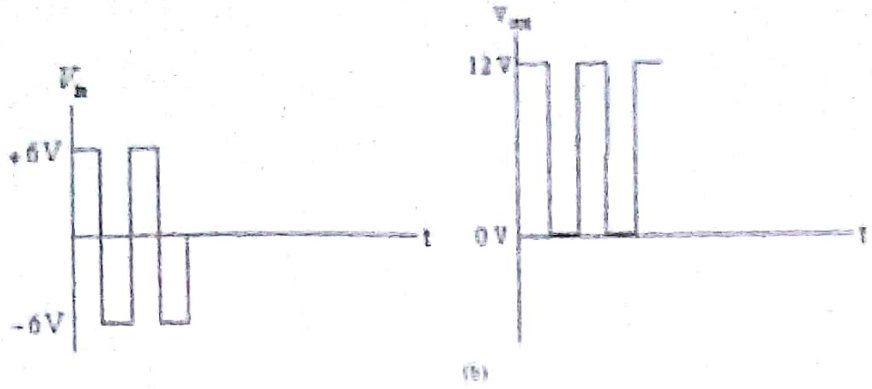

Fig.5: (a) Clamping Circuit (b) Input and Output Waveforms

Equipments:

- Dual-Trace Oscilloscope
- Digital Multimeter DMM
- Bread Board
- Resistors
- Capacitance
- Electrolytic Capacitors: 10 μF and 100 μF
- 1N4001 Rectifier Diodes

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PROCEDURE:

Part 1: Half-Wave Rectification

1. Construct the half-wave rectifier circuit shown in Figure 6. Record the measured value of the resistor. Set the function generator to a 1 KHz, $8\,V_{P-P}$ sinusoidal voltage using the oscilloscope.

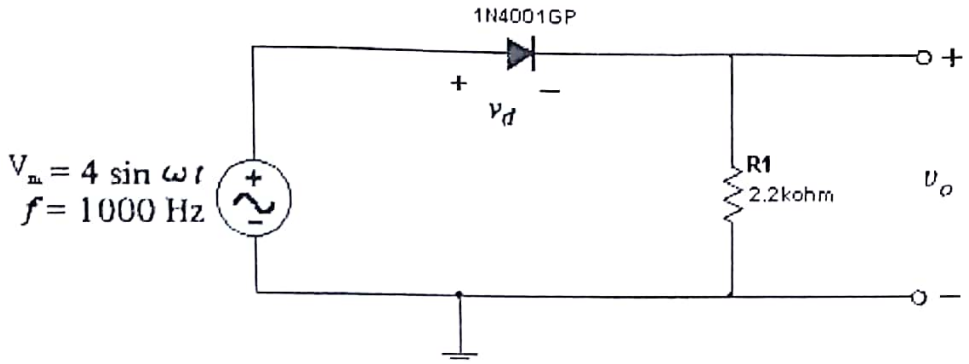

Fig.6: Half-wave Rectifier.

2. Using the oscilloscope with the AC-DC coupling switch in the DC position, obtain the input voltage V_{in} and the output voltage V_O and sketch their waveforms. Before viewing V_O be sure to set the $V_O = 0$ V line using the GND position of the coupling switch.

3. Determine the theoretical output voltage V_O for the circuit of Figure 6 and sketch its waveform for one full cycle using the same sensitivities employed in step (2). Indicate the maximum and minimum values on the output waveform. Compare the results of step (2) and (3)?

4. Set your oscilloscope to X-Y setting. This will display channel-1 (your input) on the horizontal axis and channel-2 (the output of the circuit) on the vertical axis. The X-Y mode will display the transfer characteristic of your circuit. Sketch the transfer characteristic you observed and commit.

5. Measure the DC value of V_O using the DC scale in the DMM.

6. Calculate the DC level of the half-wave rectified signal of step (2). Find the percent difference between the measured value (from step 5) and the calculated value.

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Part 2: Full-Wave Rectification

7. Construct the circuit shown in Figure 7. Sketch the input and output waveforms. Then, measure the DC load voltage using DMM.

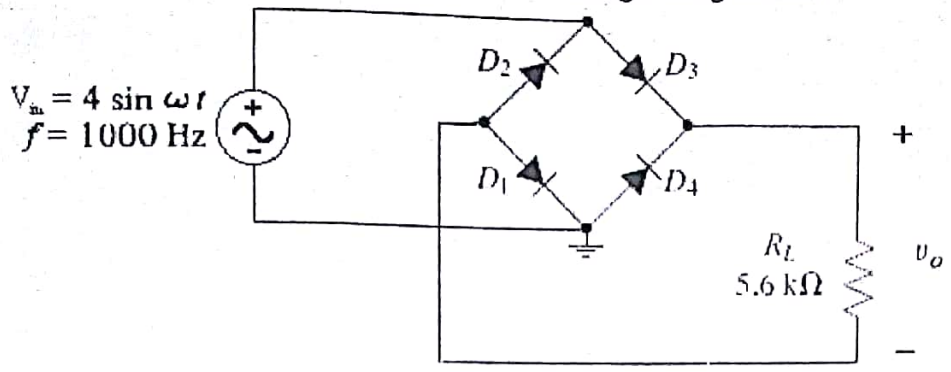

Fig.7: Bridge Rectifier.

Part 3: Rectifier Filtering

As you have seen in the previous parts of this experiment, the output from a rectifier is a pulsating DC voltage. The filter in a linear power supply is designed to reduce the variations in this DC voltage. As you will see shortly, the value of the filter capacitor determines how effective the filter is. No filter is perfect, however, so the variations in the DC voltage are never completely eliminated. The remaining variations in the DC voltage are referred to as the *ripple voltage* (V_r).

8. Add a 1 μF capacitor in parallel with the bridge rectifier load as shown in Figure 8. Use the DMM to measure V_O, and record this value.

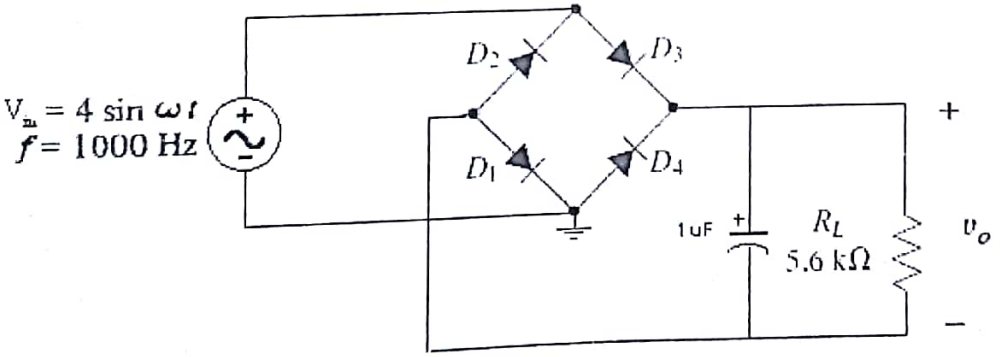

Fig.8: Filtered Bridge Rectifier

Note: It is extremely important to observe proper polarity when working with electrolytic capacitors. If installed backwards, they will fail and may explode.

9. Use the oscilloscope to observe and measure the ripple voltage. (*Note:* The Channel 1 input must be AC coupled to measure the ripple voltage.) Draw the ripple waveform, and record its measured peak-to-peak value.

10. Change the filter capacitor from 1 μF to 10 μF. Power up, and repeat Steps (8) and (9). Draw the ripple voltage waveform, and record its measured peak-to-peak value.

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Part 4: The Shunt Clipper

11. Construct the clipping circuit shown in Figure 9. Record the measured value of the resistor. Note that the input signal is 10 V_{p-p} sine wave at a frequency of 1KHz.

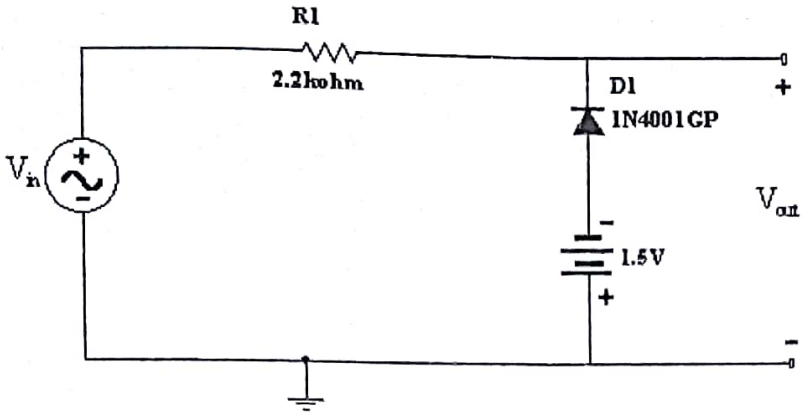

Fig.9: A shunt Clipper with DC Battery

12. Using the oscilloscope with the AC-DC coupling switch in the DC position, obtain the input voltage and the output voltage V_{out} and sketch their waveforms. Before viewing V_{out} be sure to set the V_{out} = 0 V line using the GND position of the coupling switch.

Part 5: Clampers with DC Battery

13. Construct the circuit shown in Figure 10. Connect a 2 KHz, 10 V_{p-p} sine wave to the input and use the oscilloscope to observe the input and output signals.

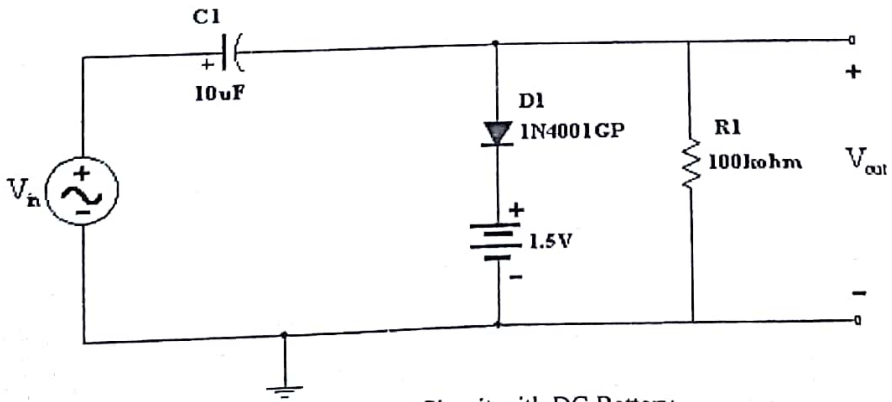

Fig.10: Clamper Circuit with DC Battery

14. Repeat step (12) for Figure10.

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QUESTIONS & PROBLEMS:

1. Using the results of step (2), calculate the peak values of the current i(t) and sketch its waveform.

2. Refer to Figure7. Explain how you would modify this circuit to obtain a negative load voltage.

3. Refer to the circuit shown in Figure 8, how would you decrease the ripple in the output voltage?

4. Refer to the circuit shown in Figure 9, how can you limit the output at a voltage different than the threshold voltage (V_γ) of the diode, for example at around $\pm 5V$?

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Lab Session 3

BJT Characteristics and DC Biasing

OBJECTIVES:

After performing this experiment, you should be able to:

- Determine the transistor type (NPN, PNP), terminals, and material using a digital multimeter (DMM).
- Determine the parameters for the small signal transistor model of a Bipolar Junction Transistor (BJT) and use these parameters to plot the DC load line.
- Investigate the operation of the two types of Bipolar Junction Transistor.

SUMMERY OF THEORY:

A bipolar junction transistor (BJT) is a three-terminal semiconductor device, made of either silicon (Si) or germanium (Ge). Their structure consists of two layers of n-type material separated by a layer of p-type material (NPN) or of two layers of p-material separated by a layer of n-material (PNP). In either case, the center layer forms the base of the transistor, while the external layers form the collector and the emitter of the transistor. It is the structure that determines the polarities of any voltages applied and the direction of the electron or conventional current flow. With regard to the latter, the arrow at the emitter terminal of the transistor symbol for either type of transistor points in the direction of conventional current flow and thus provides a useful reference as shown in Figure 1. One part of this experiment will demonstrate how you can determine the type of transistor, its material, and identify its three terminals.

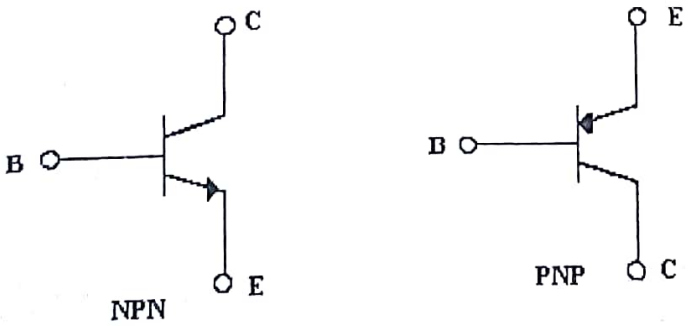

Fig.1: Transistor Symbols

A bipolar junction transistor (BJT) is very versatile. It can be used in many ways, as an amplifier, a switch or an oscillator. Before an AC input signal is applied to the transistor, its DC operating conditions need to be set.

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When looking at the curved face of the typical package of the BJT transistor as shown in Figure 2, the emitter (E) is on the right, the base (B) is in the middle and the collector (C) is on the left side of the package.

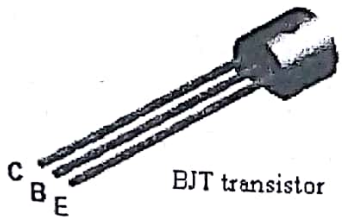

Fig.2: Typical Package of the BJT Transistor

There are three regions of operation for the transistor: Active Region, Saturation Region and Cutoff Region. To bias a BJT transistor for operation in the active region, the base-emitter junction must be forward biased and the collector-base junction reverse biased. Thus, in the active region, current will flow through the collector and will be related to the base current by:

$$I_C = \beta\, I_B \qquad (1)$$

Where:

I_C : The collector current,

I_B : The base current,

β : The DC current gain.

$\beta = \frac{I_C}{I_B}$

$\alpha = \frac{I_C}{I_E}$

The active region is the desired region of operation for a linear amplifier.

If the collector voltage falls below the base voltage by an amount that exceeds the threshold voltage of that junction, the collector-base junction will become forward biased and the transistor will enter the saturation region. . Transistor switching circuits are generally driven into saturation for the ON state. However, for application requiring rapid switching the distance driven into saturation must be limited to prevent long charge storage time in order to reduce switching time.

In addition to the active and saturation regions, the transistor will enter the cutoff region if both the base-emitter and base-collector junctions become reverse biased. In this case, all terminal currents are extremely small and the transistor is said to be off. Switching circuits are driven into cutoff when the desired state of the switch is OPEN.

In order to use a transistor in an amplifying circuit it has to be biased. In other words, a Q-point has to be set in order to place the device in the active region of operation. There are several methods which can be used to bias a transistor. Figures 3 and 4 demonstrate two possibilities.

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The first scheme (Figure 3) is called a fixed bias scheme. In a fixed biasing the base current is set through a base resistor and the emitter of the transistor is grounded. This scheme is not used in practice since the Q-point depends very strongly on β.

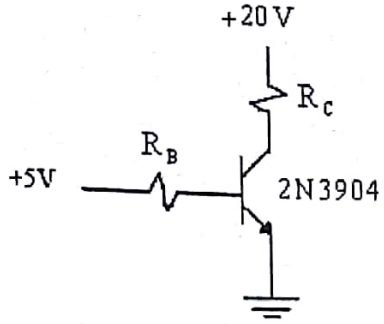

Fig.3: Fixed Biasing Scheme.

A second possibility, which is commonly used, is the self biasing scheme. Here the base voltage is set through a voltage divider and the emitter is tied to ground through a resistor. If designed correctly, this scheme is relatively independent of β.

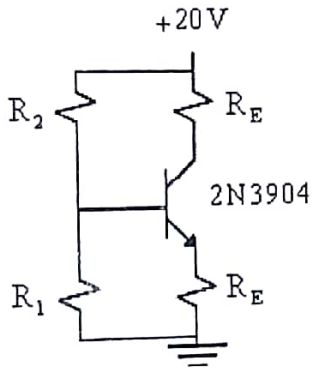

Fig.4: Self-Biasing Voltage Divider Scheme.

PreLab:

Read the specification sheet for the 2N3904 NPN BJT transistor and determine the typical and maximum values for each parameter listed in Table 2.

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PROCEDURE:

Pert 1: Checking Transistors

It is often necessary to perform a quick check on a transistor to determine the transistor's type, terminals, material and if it is working. Bipolar transistors are either NPN or PNP depending on the arrangement of materials as in Figure 5.

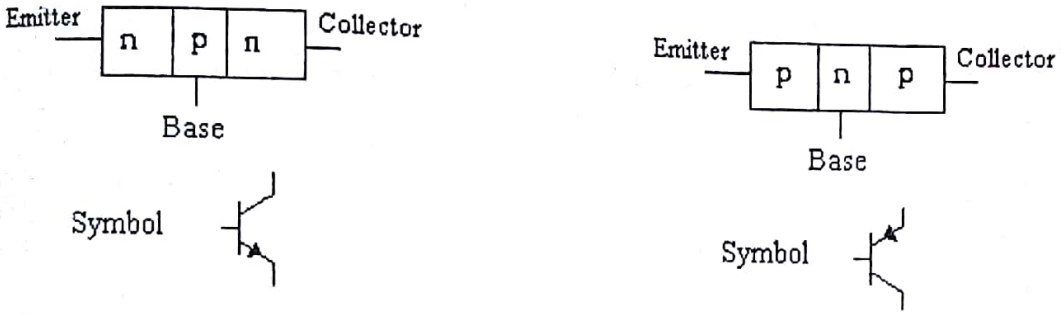

Fig.5: Arrangement of Transistor's Materials Depending on its Type

For purposes of quick testing only, a transistor can be thought of as two back to back diodes as in Figure 6 and hence the following procedure will determine the type, terminals, and material of a transistor and it can be tested in the same manner as a diode. The procedure will utilize the diode testing scale found on many modern multimeters. If no such scale is available, the resistance scales of the meter may be used.

Fig.6: Simple Transistor Model for Testing Purpose

1. Label the transistor terminals of Figure 7 as 1, 2, and 3.
2. Set the selector switch of the millimeter to the diode scale.
3. Connect the positive lead of the meter to terminal 1 and the negative lead to terminal 2. Record your reading in Table 1.
4. Reverse the leads and record your reading.

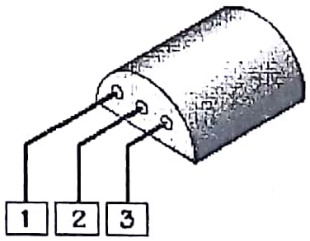

Fig.7: Determination of the Identities of BJT Leads

5. Repeat steps (3) and (4) using the other terminal to complete Table 1.

Step	Mate leads connected to BJT		Diode check reading	
	Positive	Negative	NPN	PNP
1.	1	2		
2.	2	1		
3.	1	3		
4.	3	1		
5.	2	3		
6.	3	2		

Table 1: Testing Transistor

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Part 2: Determining Transistor Parameters and The DC Load Line

1. Connect the circuit as shown in Figure 8 using NPN transistor. Switch on the power supply.

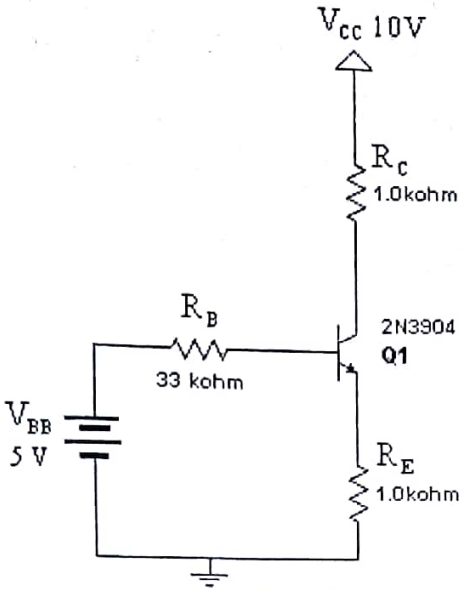

Fig.8: Biasing of NPN Transistor

2. Using the DMM: measure the collector, base and emitter voltages with respect to ground and measure the collector, base and emitter currents. Recording these values in the Table 2.

Parameter	Measured	Calculated	Percentage error %
V_C			
V_B			
V_E			
I_{CQ}			
I_{BQ}			
I_{EQ}			
β_{DC}			
V_{CEQ}			
V_{BEQ}			

Table 2: Transistor Parameters

3. Determine the DC current gain or beta (ß) and the parameter (α) for this transistor so that:

$$\beta_{DC} = \frac{I_{CQ}}{I_{BQ}} \quad (2)$$

$$\alpha = \frac{\beta}{\beta + 1} \quad (3)$$

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4. Measure the collector-emitter voltage V_{CE} and the base-emitter voltage V_{BE}. Record these values in Table 2.

5. Determine the saturation ($I_{C(short)}$) and cutoff ($V_{CE(off)}$) points on the DC load line for this circuit using the following equations:

$$I_{C(short)} = \frac{V_{CC}}{R_C + R_E} \quad (4)$$

$$V_{CE(off)} = V_{CC} \quad (5)$$

6. Plot the DC load line using the calculated values of step (5) as end points of the DC load line. Locate the Q point based on the measured values of I_{CQ} and V_{CEQ}.

7. Connect the circuit as shown in Figure 9 using PNP transistor. Switch on the power supply.

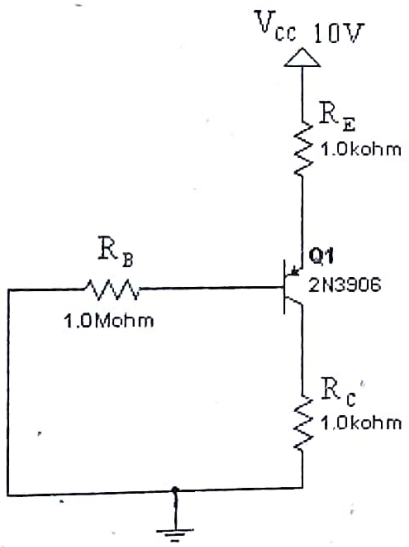

Fig.9: Biasing of PNP Transistor

8. Repeat the steps from (2) to (5) for Figure 9. Tabulate your records.

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Part 3: Transistor Switch

9. Build the following circuit shown in Figure 10 using the NPN transistor. Be sure to include the current limiting resistor R_C in series with the Light Emitting Diode (LED) or it may be damaged.

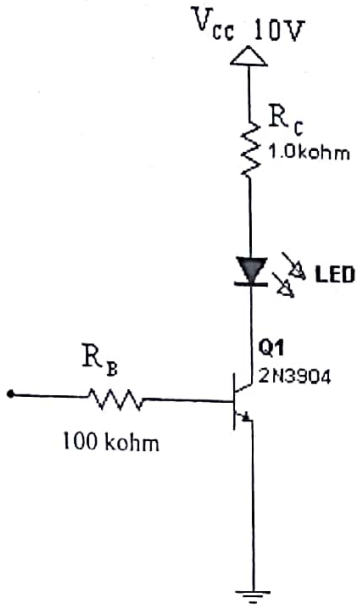

Fig.10: Transistor as a Switch

10. Make sure that one end of R_B is connected to ground as shown in Figure10. Measure and record the voltages at the Base (V_B), Emitter (V_E), and Collector (V_C). What do you observe?

11. Connect the Base resistor (R_B) to +10 V instead of ground. What do you observe?

12. For this configuration measure the Base (V_B), Emitter (V_E) and Collector (V_C) voltages. What mode of operation is the transistor in? Explain.

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QEUSTIONS & PROBLEMS:

1. Calculate the DC parameters listed in Table 2 of the NPN transistor in the circuit shown in Figure 8. (Show your calculations)

2. Compare the measured values of steps from (2) to (4) with expected values obtained from Question (1), using the value of ß determined in step (3) and a typical base-emitter voltage of 0.7 V. Record these values in Table 2.

3. For Part 3: What is the operating mode of the NPN transistor when connecting:

   (a) R_B to the ground?

   (b) R_B to +10 volt ?

4. For Part 4: Calculate the DC parameters obtained from step (14) and compare them with measured values. What is the operating mode of the NPN transistor?

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Lab Session 4
The Common Emitter Amplifier

Supervised by: Dr. Osama Al-Oquili

OBJECTIVES:

After performing this experiment, you should be able to:

- Determine the voltage gain of a common-emitter (CE) amplifier.
- Determine the input impedance of a CE amplifier.
- Determine AC resistance of the emitter (r_e) for a CE amplifier.
- Explain the role of coupling and bypass capacitors in a CE amplifier.
- Demonstrate the effect that a load has on the voltage gain of a CE amplifier.

SUMMARY OF THEORY:

In a common-emitter (CE) amplifier, the input signal is applied between the base and emitter, and the output signal is developed between the collector and emitter. The transistor's *emitter* is common to both the input and output circuit; hence, the term common emitter. The *common-emitter (CE) amplifier* is the most common BJT amplifier configuration. This amplifier has the following characteristics:

1. High voltage gain.
2. High current gain.
3. Moderate input resistance.
4. Moderate output resistance.
5. 180° voltage phase shift between the input and output waveforms.

To make any transistor circuit amplify AC signals, the base-emitter junction must be forward biased, and the base-collector junction must be reverse-biased. The purpose of bias circuits is to establish and maintain the proper DC operating conditions for the transistor. There are several ways to apply DC bias. The simplest method, called base bias or fixed bias, is frequently unsatisfactory due to manufacturing variations between transistors and sensitivity to temperature changes. Base bias is recognized by a single resistor connected from V_{CC} to the transistor base. A much more widely used bias circuit is called voltage-divider bias. Voltage-divider bias is not as sensitive to transistor variations and temperature changes. Voltage-divider bias is shown in Figure1(a).

To analyze any amplifier, start with the DC parameters. The steps to solve for the DC parameters for the CE amplifier with voltage-divider bias illustrated in Figure 1(a) are:

1. Mentally remove capacitors from the circuit since they appear open to DC. This causes the load resistor, R_L, to be removed. Solve for the base voltage, V_B, by applying the voltage divider rule to R_1 and R_2, as illustrated in Figure 1(b).

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RE reduce AV remove RL AI↑ AV↑
increase AI remove CL
increase Ri نفس الباقي

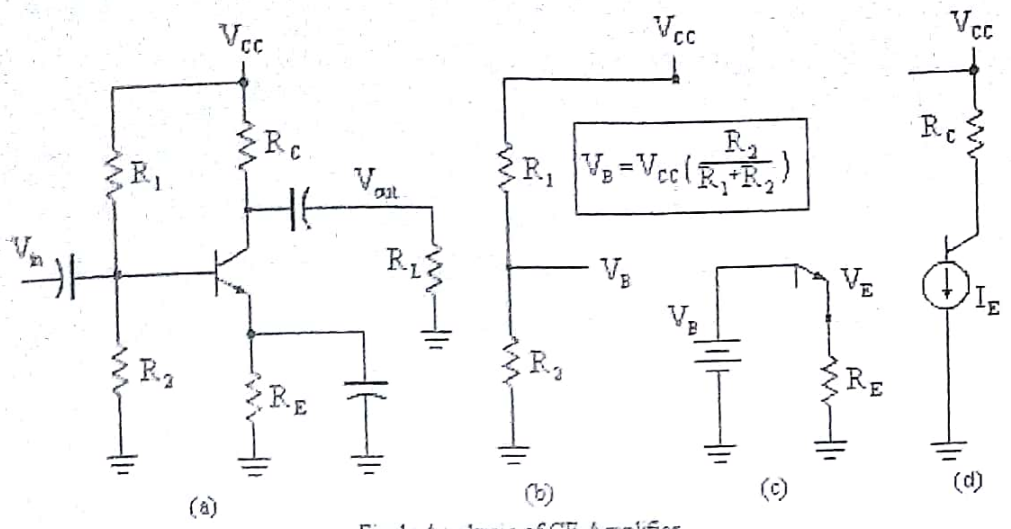

Fig.1: Analysis of CE Amplifier

2. Subtract the 0.7 V forward-bias drop across the base-emitter diode from V_B to obtain the emitter voltage, V_E, as illustrated in Figure 1(c).
3. The DC current in the emitter circuit is found by applying Ohm's law to R_E. The emitter current, I_E, is approximately equal to the collector current, I_C. The transistor appears to be a current source of approximately I_E into the collector circuit, as shown in Figure 1(d).

The AC parameters for the amplifier can now be analyzed. The AC equivalent circuit is shown in Figure 2. The capacitors appear to be an AC short. For this reason, the AC equivalent circuit does not contain R_E. Using the superposition theorem, V_{CC} is replaced with a short, placing it at AC ground. The analysis steps are:

1. Replace all capacitors with a short and place V_{CC} at AC ground. Compute the AC resistance of the emitter, r_e, from the equation:

$$r_e = \frac{26\ mV}{I_E} \qquad (1)$$

2. Compute the amplifier's voltage gain. Voltage gain is the ratio of the output voltage divided by the input voltage. The input voltage is across the AC emitter resistance to ground which, in this case, is r_e. The output voltage is taken across the AC resistance from collector to ground which, in this case, is R_C. For the circuit in Figure 2, the output voltage divided by the input voltage can be written:

With R_E bypassed:
$$|A_V| = \frac{V_{out}}{V_{in}} = \frac{i_C R_C}{i_e r_e} \cong \frac{R_C}{r_e} \qquad (2)$$

With R_E unbypassed:
$$|A_V| = \frac{V_{out}}{V_{in}} = \frac{i_C R_C}{i_e (r_e + R_E)} \cong \frac{R_C}{R_E} \qquad (3)$$

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3. Compute the total input resistance seen by the AC signal:

With R_E bypassed: $$R_{in} = R_1 \| R_2 \| \beta r_e \quad (4)$$

With R_E unbypassed: $$R_{in} = R_1 \| R_2 \| \beta (r_e + R_E) \quad (5)$$

4. Compute the total input resistance seen by the AC signal: (Assuming $r_o = \infty$)

$$R_{out} \cong R_C \quad (6)$$

5. Compute the voltage gain from the source to the load:

$$\frac{V_L}{V_S} = \frac{R_{in}}{r_S + R_{in}} A_V \frac{R_L}{R_L + R_{out}} \quad (7)$$

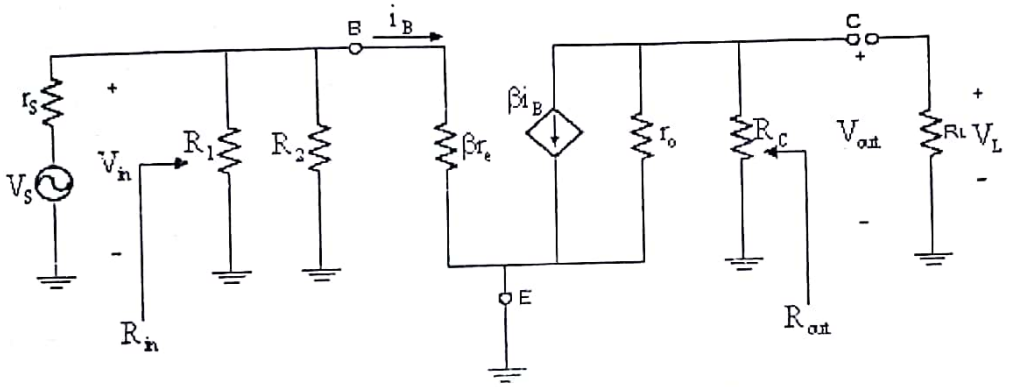

Fig.2: AC Equivalent Circuit of CE Amplifier.

EQUIPMENTS:

- Variable DC Power Supply
- Dual-Trace Oscilloscope
- Breadboard
- Resistors
- Capacitors
- Potentiometer
- 2N3904 NPN Transistor

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PROCEDURE:

Part 1: DC Measurements

1. Measure and record the values of the resistors.

2. Construct the amplifier shown in Figure 3. The signal generator should be turned off. Measure and record the DC voltages listed in Table 1.

3. Using the measured resistances and the value of ß determined in step (2). compute the DC parameters listed in Table 1 for the CE amplifier shown in Figure 3. Your measured and computed values should agree within 10%. (Show your calculations)

DC Parameter	Computed Value	Measured Value
V_B		
V_E		
I_E		
V_C		
V_{CE}		
β		

Table.1: DC Parameters of CE Amplifier

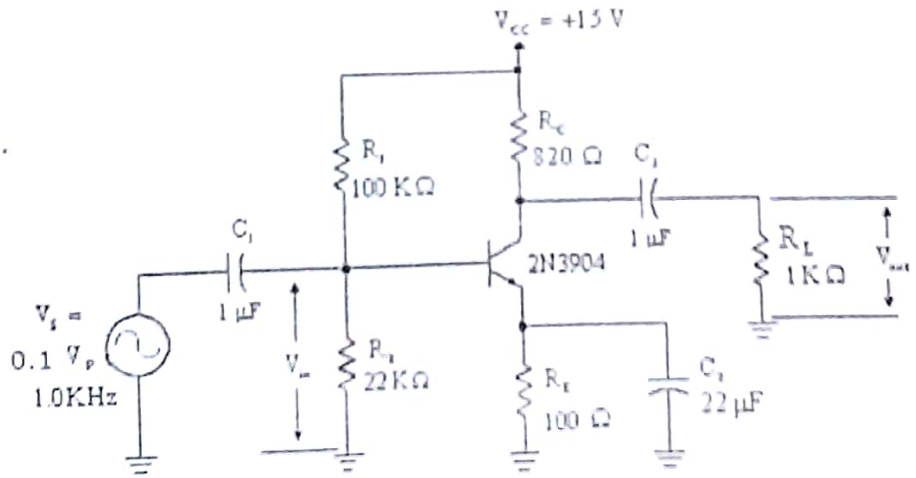

Fig.3: CE Amplifier

Part 2: AC Measurements

4. Compute the AC parameters listed in Table 2 (show your calculation). The AC base voltage, v_b, represents the signal input to the amplifier, V_{in}. Multiply the input signal by the computed voltage gain to obtain the output signal.

5. Disconnect the load resistance R_L. Turn on the signal generator and adjust V_s for a 0.1 V_p sine wave at 1.0 kHz. Measure the peak-to peak values of the input and output waveforms, and record these values in Table 2. Use the measured signal voltages to calculate the voltage gain of the amplifier.

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6. Carefully sketch the input and output waveforms showing the phase shift between them.

7. Restore the circuit to its original configuration shown in Figure 3. Set R_L to 1kΩ, and measure the peak-to peak value of the output waveform. Record your measured and calculated values. Use this measured voltage to calculate the voltage gain from the input to the load V_L/V_{in}. Record it in Table 2.

8. Using the basic laws of voltage division, you can easily determine the input impedance of this amplifier as follows:
   - Insert a 47 kΩ potentiometer between the signal generator and the input coupling capacitor.
   - Adjust the potentiometer until V_{out} drops to one-half the value noted prior to insert the potentiometer.
   - Power down, and remove the pot from the circuit *without disturbing its setting*.
   - Measure the adjusted resistance of the potentiometer, and record this value in Table 2. This value equals the input impedance of the amplifier.

9. Remove C_2 from the circuit. Measure the AC signal voltage at the transistor's base, emitter, and collector. Measure the voltage gain of the amplifier.

10. With C_2 open (R_E unbypassed): repeat steps (7) and (8). Compare the result values with the calculated values obtained from step (4).

11. To measure the output resistance R_{out} of the CE Amplifier connect a 1 KΩ potentiometer connected between the output coupling capacitor and ground. Adjust the potentiometer until V_{out} drops to one-half the previous value. Remove the potentiometer and measure its resistance. By the voltage divider role, the resistance of the potentiometer equals the output resistance of the amplifier.

AC Parameter	Computed Value		Measured Value	
	R_E byp.	R_E unbyp.	R_E byp.	R_E unbyp.
$v_b = V_{in}$				
r_e				
A_V				
$v_C = V_{out}$				
V_L				
R_{in}				
R_{out}				

Table 2. AC Parameters of CE Amplifier

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QUESTIONS & PROBLEMS:

1. Refer to Table 1: How close are your calculated values of the DC parameters to the measured value? Explain any discrepancies.

2. Refer to the waveforms that you drew from Figure 3. Explain why the output signal is 180° out of phase with the input.

3. Refer to Table 2: How close are your calculated value of AC parameters to the measured value? Explain any discrepancies.

4. Refer to Step (7): What happened to the voltage gain of the circuit when the load resistance was connected? Explain why you think this happened.

5. Refer to Step (9): What happened to the voltage gain of the circuit when the bypass capacitor was removed? Explain why you think this happened.

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Lab Session 5
Multistage Amplifiers

OBJECTIVES:

After performing this experiment, you should be able to:

- Construct a two-stage transistor amplifier.
- Measure the DC and AC parameters including the input resistance, output resistance, voltage gain, and power gain.

SUMMARY OF THEORY:

A single stage of amplification is often not enough for a particular application. The overall gain can be increased by using more than one stage. Practical transistor amplifiers usually consist of a number of stages connected in cascade. In addition to provide gain, the *first* (or input) stage is usually required to provide a high input resistance in order to avoid loss of signal level when the amplifier is fed from a high resistance source. In a differential amplifier the input stage must also provide large common mode rejection. The function of the *middle* stage of an amplifier cascade is to provide the bulk of the voltage gain. In addition, the middle stage provides such other functions as the conversion of the signal from differential mode to single ended mode and the shifting of the DC level of the signal. Finally, the main function of the *last* (or output) stage of an amplifier is to provide a low output resistance in order to avoid loss of gain when a low-valued load resistance is connected to the amplifier. Also, the output stage should be able to supply the current required by the load in an efficient manner.

The two-stage linear amplifier is shown in Figure 1. It uses two common emitter (CE) circuits, with the PNP and NPN transistors connected in a cascade Amplifier. R_A and R_B are not considered part of the amplifier, but are only used to attenuate the input signal from the function generator by a known factor. To analyze the amplifier, start with the DC parameters. Use measured values of components in your calculations. The steps to solve for the DC parameters for this amplifier are:

1. Mentally remove (open) capacitors from the circuit since they appear open to DC. Solve for the base voltage, V_B of Q_1. By inspection, the DC base voltage is zero; however if the resistors are not equal, the base voltage can be found by applying the voltage-divider rule and the superposition theorem to R_1 and R_2.

2. Add the 0.7 V forward-bias drop across the base-emitter diode of Q_1 from V_B to obtain the emitter voltage, V_E of Q_1.

3. Find the voltage across the emitter resistors and apply Ohm's law to solve for the emitter current I_E of Q_1.

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4. Assume the emitter current (step 3) is equal to the collector current, I_C, of Q_1. Find the voltage across R_{C1} and the voltage drop across Q_1. Solve for the DC voltage drop across the equivalent resistance to find the voltage at the collector of Q_1.

5. Compute the base voltage of Q_2 by applying the superposition theorem and voltage divider rule to R_3 and R_4. Subtract 0.7 V from the base voltage of Q_2 to find the emitter voltage of Q_2. Find the voltage across the emitter resistors and apply Ohm's law to determine the emitter current in Q_2.

6. Assume the emitter current (step 5) is equal to the collector current I_C, of Q_2. Find the voltage across R_{C2} and the voltage drop across Q_2.

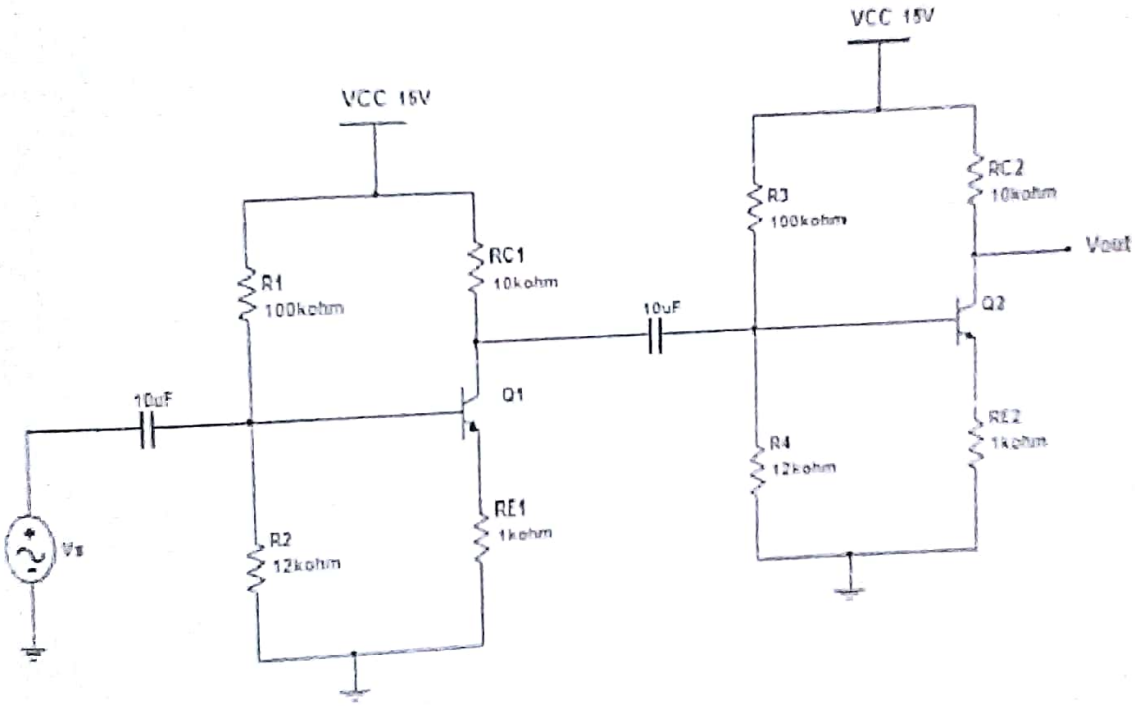

Fig.1: Two-Stage Linear Amplifier

The AC parameters for the amplifier can now be analyzed. The AC analysis steps are:

1. Replace all capacitors with a short. The AC resistance in the emitter circuit includes the unbypassed emitter resistor and the AC resistance of the transistor. Compute the AC emitter resistance of each transistor, r_e, from the equation:

$$r_e = \frac{25\text{mV}}{I_E} \qquad (1)$$

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2. Compute the input and output resistance of Q_1. The input resistance includes the bias resistors in parallel with the AC resistance of the emitter circuit reflected into the base circuit. The output resistance is simply the value of the collector resistor.

$$R_{in(Q1)} = R_1 \| R_2 \| \{\beta (r_e + R_{E2})\} \tag{2}$$

3. Compute the input and output resistance of Q_2. As before, the input resistance includes the bias resistors and the AC emitter resistance reflected to the base circuit. The output resistance is again the collector resistor.

$$R_{in(Q2)} = R_3 \| R_4 \| \{\beta r_e\} \tag{3}$$

4. Compute the unloaded gain, $A_{V(NL)}$ of each stage. The unloaded voltage gain for the common-emitter transistors can be written:

$$\left|A_{v(NL)}\right| = \frac{V_{out}}{V_{in}} = \frac{I_C R_C}{I_e (r_e + R_{e(ac)})} = \frac{R_C}{(r_e + R_{e(ac)})} \tag{4}$$

5. Compute the overall gain of the amplifier. It is easier to calculate the voltage gain of a multistage amplifier by computing the unloaded voltage gain for each stage, then including the loading effect by computing voltage dividers for the output resistance and input resistance of the following stage. This idea is illustrated in Figure 2. Each transistor is drawn as an Amplifier consisting of an input resistance, R_{in}, an output resistance, R_{out}, along with its unloaded gain, $A_{V(NL)}$. Then, the overall loaded gain. A_V, of this amplifier can be found by:

$$A_V = A_{V1}\left(\frac{R_{in2}}{R_{out1} + R_{in2}}\right)A_{V2} \tag{5}$$

Note that if a load resistor was added across the output, an additional voltage divider consisting of the output resistance of the second stage and the added load resistor is used to compute the new gain.

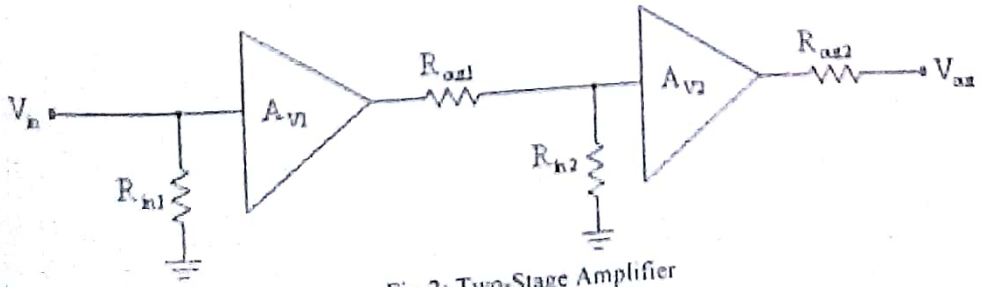

Fig.2: Two-Stage Amplifier

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PROCEDURE:

1. Connect the circuit shown in Fig.1. Compute the DC parameters for the amplifier listed in Table 2.

DC Parameter	Computed Value	Measured Value
$V_{B(Q1)}$		
$V_{E(Q1)}$		
$I_{E(Q1)}$		
$V_{C(Q1)}$		
$V_{CE(Q1)}$		
$V_{B(Q2)}$		
$V_{E(Q2)}$		
$I_{E(Q2)}$		
$V_{C(Q2)}$		
$V_{CE(Q2)}$		

Table 1: DC Parameters of the Multi-Stage Amplifier

2. Construct the two-stage bipolar transistor amplifier shown in Figure 1. The function generator should be turned off. Measure and record the DC voltages listed in Table 2 Your measured and computed values should agree within 10%.

3. Compute the AC parameters listed in Table 3. The gains for each stage are not loaded. The output resistance of Q_1 ($R_{out(Q1)}$) is simply the collector resistor; the input resistance of Q_2 is determined by the procedure given in the Summary of Theory.

4. Compute the overall gain of the amplifier using the computed gains from Table 3 and the input and output resistance between the stages (see step 5 of the AC analysis in the Summary of Theory). Enter the computed overall gain, A_v, on the first line of Table 4. Using this value. Compute the expected output voltage and record the computed output voltage on the last line of T able 4.

5. Connect the function generator voltage to the divider composed of R_A and R_B as shown in Figure 1. (Note: The purpose of these resistors is to attenuate the generator signal by a known amount; they will not be considered part of the amplifier). Turn on the function generator and set V_s for a 0.5 Vpp sine wave at 10 KHz. (Check voltage and frequency with the oscilloscope). Measure the AC signal voltage at the amplifier's output ($V_{out(Q2)}$) and record the value on the last line of Table 4. Then use V_{in} and V_{out} to find the measured overall gain, A_v. Record the measured overall gain in the first line of Table 4.

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AC Parameter	Computed Value
$r_{e(Q1)}$	
$r_{e(Q2)}$	
$A_{V(NL)_{Q1}}$	
$A_{V(NL)_{Q2}}$	
$R_{out(Q1)}$	
$R_{in(Q2)}$	

Table 3: Computed AC Parameters

AC Parameter	Computed Value	Measured Value
$V_{in(Q1)}$		
$V_{out(Q2)}$		
$R_{in(Q1)}$		
$R_{out(Q2)}$		
A_V		

Table 4: Computed & Measured AC Parameters

6. The measurement of the total input resistance, $R_{in(tot)}$, is done indirectly by using a potentiometer as shown in Figure 3. The output signal (V_{out}) set by V_s to a convenient level with the amplifier operating normally (no clipping or distortion). Using the basic laws of voltage division, you can easily determine the input impedance of this amplifier as follows:
   - Insert a 100 kΩ potentiometer in series between the base of the transistor Q_1 and the input coupling capacitor.
   - Adjust the potentiometer until V_{out} drops to one-half the value noted prior to insert the potentiometer.
   - Power down, and remove the pot from the circuit *without disturbing its setting*.
   - Measure the adjusted resistance of the potentiometer, and record this value in Table 4. This value equals the input impedance of the amplifier.

7. In this step you will measure the output resistance of the amplifier. The computed output resistance is the same as R_{C2}, the load resistor of Q_2. To measure the output resistance R_{out} connect a 10 KΩ potentiometer connected between the output coupling capacitor and ground. Adjust the potentiometer until V_{out} drops to one-half the previous value. Remove the potentiometer and measure its resistance. By the voltage divider role, the resistance of the potentiometer equals the output resistance of the amplifier.

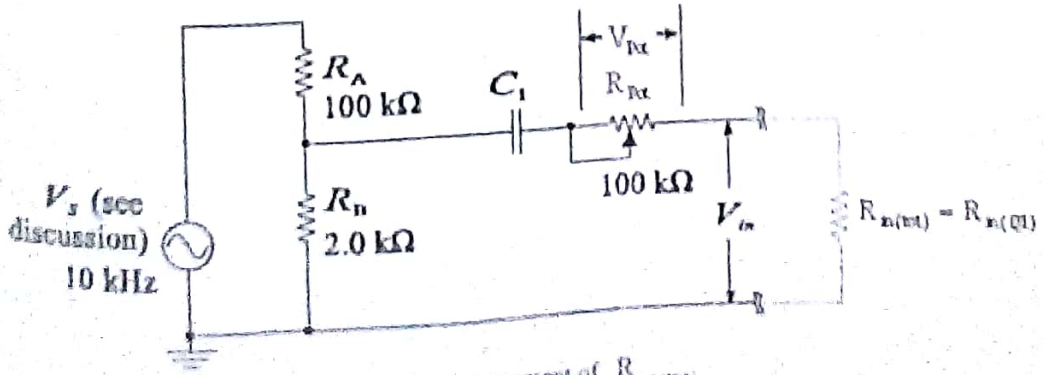

Fig 3: Measurement of $R_{in(tot)}$

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VALUATION AND REVIEW QUESTIONS:

1. Explain the principle used to measure the input and output resistance.

2. What is the phase between the input and output signal? Explain your answer.

3. What is the general characteristic of the multistage circuit shown in figure.1

4. What happened to the voltage gain of the circuit if you add a bypass capacitor (Paralle to R_{E1} and parallel to R_{E2})? Explain why.

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Lab Session 6

Op-Amp Applications 1:Inverting, Non-inverting and Summing OpAmp Circuits

OBJECTIVES:

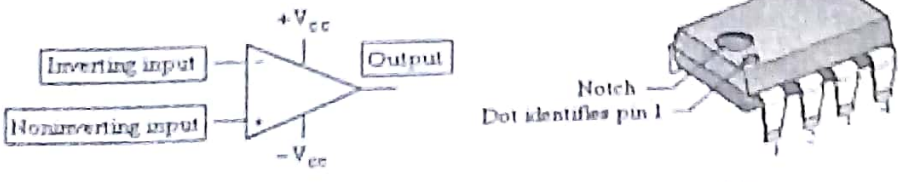
After performing this experiment, you should be able to:

- Analyze the operation of the inverting, non-inverting and summing amplifier.
- Determine and measure the closed-loop voltage gain of an inverting and a noninverting amplifier.
- Demonstrate the effects of load resistance on amplifier gain.
- Demonstrate the relationship between the gain and the bandwidth for operational amplifiers.

SUMMARY OF THEORY:

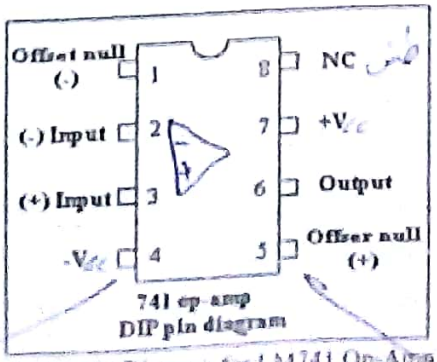
An operational amplifier (*op-amp*) is a linear integrated circuit that incorporates a DC-coupled, high-gain differential amplifier and other circuitry that give it specific characteristics. The ideal op-amp has certain unattainable specifications, but hundreds of types of operational amplifiers are available, which vary in specific ways from the ideal op-amp. Important specifications include very large open-loop gain, high input impedance, and low output impedance.

The opamp chip that we are using in this lab is the 741A opamp. It comes in an 8-pin dual-inline package (DIP) (see fig.1). The connections for the pins are as follows: pins 2 and 3 are for v- and v+ , pin 4 is for negative supply voltage, pin 7 for positive supply voltage, and pin 6 is for the output.



(a) (b)

Fig.1: (a) The Symbol for an Op-Amp (b) Typical 8-pin DIP Op-Amp



c) The Pin Diagram for LM741 Op-Amp

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Operational amplifiers can be used to perform mathematical operations on voltage signals such as inversion, addition, subtraction, integration, differentiation, and multiplication by a constant. In this experiment we will introduce the inverting, non-inverting and summing amplifiers.

Inverting Amplifier

The basic inverting op-amp configuration is shown in Figure 2. The inverting amplifier produces a 180° voltage phase shift from its input to its output. Inverting amplifiers can also be designed for a wide range of voltage gains. At the same time, the inverting amplifier has many characteristics that are determined largely by the external biasing resistor, R_1(input resistor) and R_f (feedback resistor):

- Inverting amplifiers are capable of extremely high voltage gains.

$$A_v = -\frac{R_2}{R_1} \quad (1)$$

- The gain of an inverting amplifier is extremely stable and easy to calculate.
- Input resistance: $R_i = R_1$ (2)

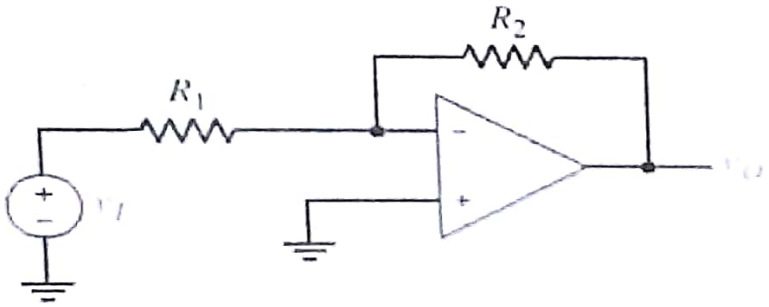

Fig.2: Inverting Amplifier

- Output resistance: $R_o = 0\ \Omega$ (3)
- Inverting amplifiers are easier to design and troubleshoot than common emitter or common source amplifiers.

Non-inverting Amplifier

Another configuration of op-amp is the noninverting amplifier as shown in Figure 3. The non-inverting amplifier shares many characteristics with the inverting amplifier (R_o =0Ω , high voltage gain …), with some exceptions:

- As the name implies, the output of this amplifier is in phase with its input.
- The noninverting amplifier has significantly higher input impedance than a comparable inverting amplifier: $R_i = \infty\ \Omega$ (4)
- Closed voltage gain: $A_v = 1 + \frac{R_f}{R_1}$ (5)

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As shown in Figure 2, the input is connected directly to the non-inverting terminal of the op-amp. As a result, the circuit input impedance is equal to (or greater than) the input impedance of the op-amp itself.

When compared to discrete amplifier circuits (like the emitter or source follower), the non-inverting amplifier shares some of their characteristics as well. It has high input impedance and low output impedance, and the input and output signals are in phase. The major difference is that non-inverting amplifiers can have high voltage gain, whereas emitter and source followers are limited to voltage gains of slightly less than unity.

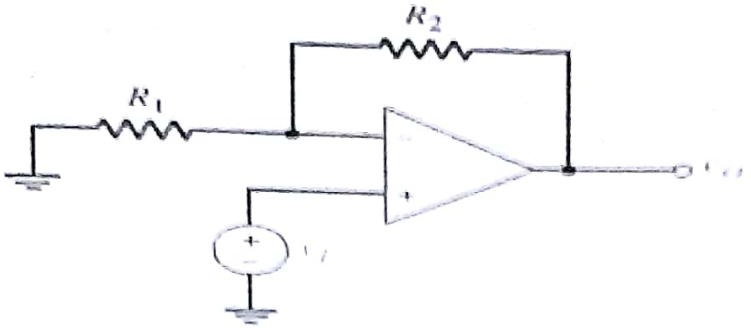

Fig 3: Non-inverting Amplifier

Summing OpAmp Circuit

The inverting amplifier can be modified to accommodate multiple input signals as in Figure 4.

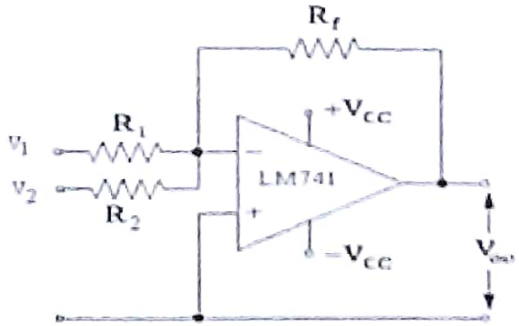

Fig.4: Summing Amplifier

With this configuration, the output signal is the sum of the two input signals and determined by the following equation:

$$V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 \right) \quad (6)$$

The amplifier can be extended to any number of inputs. For this reason, it can be used to build a digital-to-analog converter (DAC).

Equipments:

- Variable DC power supply
- Function generator
- Dual-trace oscilloscope
- LM741 op-amp (or equivalent)

Never apply an input signal to an op-amp unless both supply voltages are connected to the IC.

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PROCEDURE:

Part 1: Inverting Amplifier

1. Construct the circuit shown in Figure 5. Connect a 500 Hz, 1 V_{p-p} sine wave to the input and use the oscilloscope to observe the input and output signals.

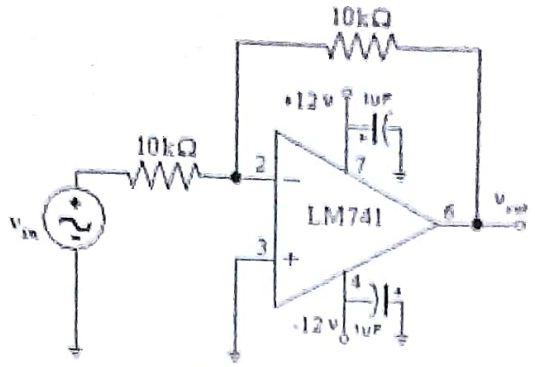

Fig.5: Inverting Amplifier

2. Measure the peak-to-peak values of the input and output waveforms, and record their values. Then, sketch both waveforms.
3. Use your results from Step (2) to calculate the closed-loop voltage gain for the circuit.
4. Table 1 lists a series of resistance values to be used in place of R_f. For each value listed, repeat the measurements and calculations in Steps (2) and (3).

R_f	V_{in}	V_{out}	A_v (Calculated)	A_v (Measured)
27 kΩ				
33 kΩ				

Table.1: Resistance Values

5. Measure the inverting amplifier circuit's input impedance by adding a 10 kΩ potentiometer in series with the input. Adjust the pot such that the gain reduces to the 50% of the value you measured in step (2).
6. Return R_f to 10 kΩ. Connect a 10 kΩ resistor as a load, and increase the input signal to 5 V_{p-p}. Power up, and measure the output voltage across the load. Use this value to calculate A_v. Record these values in Table 2.
7. Repeat Step (6) for the other load value in Table 2.

R_L	V_{in}	V_{out}	A_v
10 kΩ			
100 Ω			

Table 2: Resistance Values

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Part 2: Non-inverting Amplifier

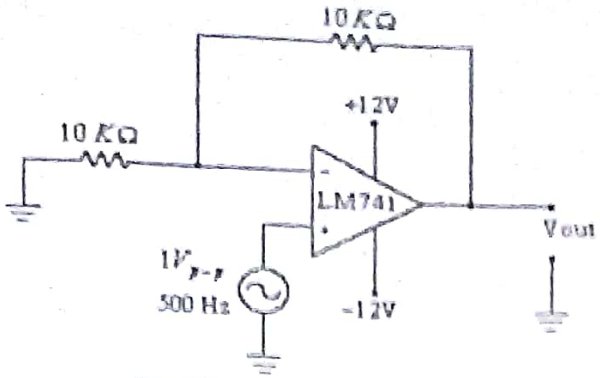

Fig.6: Non-inverting Amplifier

8. Construct the circuit shown in Figure 6. Connect a 500 Hz, 1 V_{p-p} sine wave to the input and use the oscilloscope to observe the input and output signals.
9. Repeat steps (2) and (3) for Figure 6.
10. Increase the input signal frequency from 1 KHZ to 600 KHz and measure the amplitude of V_{in} and V_{out}. Calculate the gain in dB, where dB is $20\ Log_{10}\left(\frac{V_{out}}{V_{in}}\right)$. Record your results in the Table 3. Reduce the amplitude of V_{in} if waveform of V_{out} begins to distort.

Frequency KHz	$\lvert V_{in}\rvert$ volt	$\lvert V_{out}\rvert$ volt	$\left\lvert\frac{V_{out}}{V_{in}}\right\rvert$	$\left\lvert\frac{V_{out}}{V_{in}}\right\rvert_{dB}$
1				
10				
100				
200				
600				

Table 3: Resistance Values

11. Plot the results on semi-log paper. You may need to make more measurements around frequencies where the changes occur more rapidly in order to find the -3 dB corner frequencies.

Part 3: Summing Amplifier

12. Construct the circuit shown in Figure 7. Note that the signal generator is supplying both inputs to the summing amplifier, which is op-amp 2. Note that op-amp1 in Figure 7 is included simply as a buffer; that is, it is being used to provide isolation between the two summing amplifier inputs.

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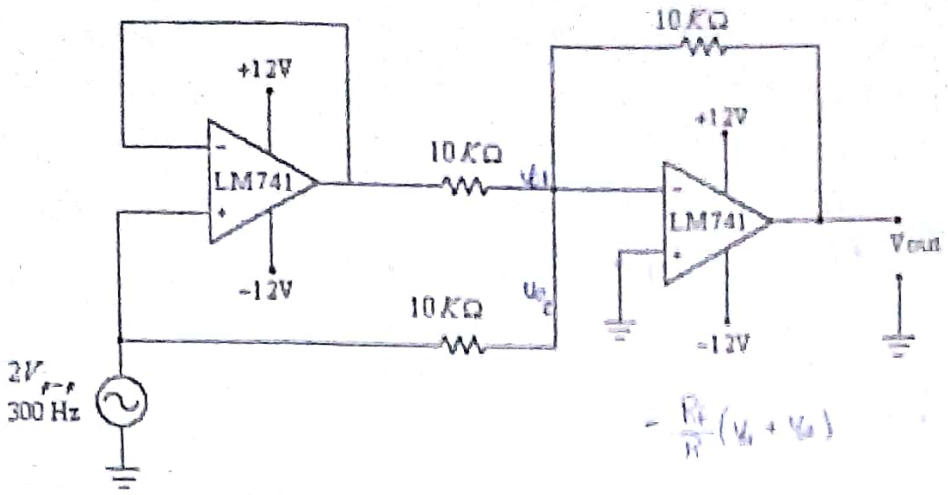

Fig.7: A Two-Input Summing Amplifier.

13. Measure and record the peak-to-peak output voltage.

14. Change R_1 to 22 kΩ, and measure the peak-to-peak output voltage.

15. Restore R_1 to 10 kΩ, and change R_f to 22 kΩ. Measure the peak-to-peak output voltage.

QUESTIONS & PROBLEMS:

1. Refer to Figure 5. What was the phase relationship between the input and the output signals? Explain this phase relationship.

2. Refer to your results from Step (3). Compare your measured value of A_v to the calculated value? Explain the reasons for any significant difference between these two values?

3. Refer to Table 2: What effect did a change in load have on the voltage gain of the amplifier?

4. Refer to Step (6): Based on your knowledge of op-amp output impedance, explain why the output waveform began to change at this value of R_L.

5. Refer to Step (11): Calculate the maximum operating frequency using the op-amp's slew rate (from the spec sheet). How does this value compare with your measured value? Explain any difference between your calculated and measured values.

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Lab Session 7

Op-Amp Applications 2: Comparator, Integrator and Differentiator

OBJECTIVES:

After performing this experiment, you should be able to:

- Construct and test comparator, integrator and differentiator circuits.
- Determine the response of these circuits to various waveforms.

SUMMARY OF THEORY:

A nonlinear application of an op-amp is the comparator. A comparator is a circuit used to compare two input voltages and to provide a DC output that indicates which of the two inputs is greater. A comparator circuit is essentially a very high gain op-amp having a plus (+) and a minus (-) inputs. The output of the comparator is a logic level that provides an indication of when the plus input voltages is greater than the minus input or when the plus input is less than the minus input. Although an op-amp can be used for this purpose, special comparator ICs are available which are better suited for the operation.
Figure 1 shows an inverting 741op-amp used as a level detector. If a LED is connected at the output, the indicator LED goes on whenever the input V_{in} goes below V_{ref} and goes off whenever V_{in} goes above V_{ref}.

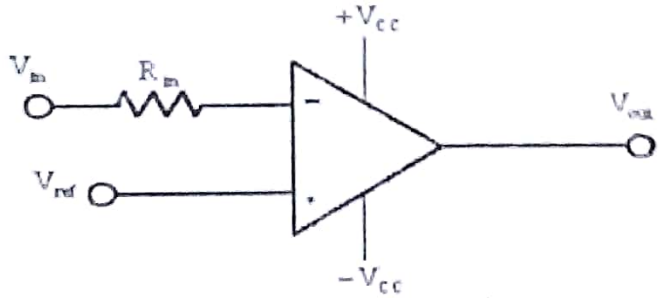

Fig 1: Comparator Circuit

Inverting comparator output:

$V_{out} = +V_{sat}$ when $V_{in} < V_{ref}$ (1)

$V_{out} = -V_{sat}$ when $V_{in} > V_{ref}$ (2)

There are two other nonlinear circuits that have application in waveform generation and signal processing - the integrator and the differentiator. An integrator produces an output voltage that is proportional to the integral (sum) of the input voltage waveform over time.

A simple integrator circuit can be constructed as shown in Figure 2 using an operational amplifier, a resistor and a capacitor. It can be shown that:

$$V_{out} = -\frac{1}{R_{in} C_f} \int_0^t V_{in}(t)\, dt \quad (3)$$

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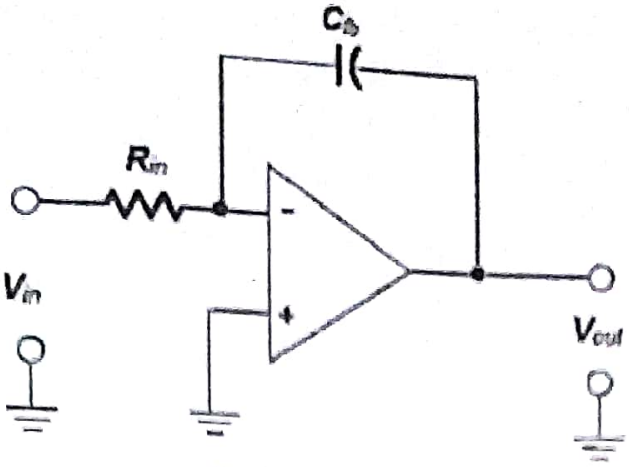

Fig.2: Integrator Circuit

Unfortunately this integrator is often unstable and hence not very practical. This is because even the slightest DC offset in the input voltage will drive the output into saturation. For this reason, a resistor R_{fb} as shown in Figure 3 is added in parallel to the capacitor to limit this effect and to limit the minimum input frequency allowed. With R_{fb} in place, the circuit is known as a leaky integrator (also known as a running average or Miller integrator).

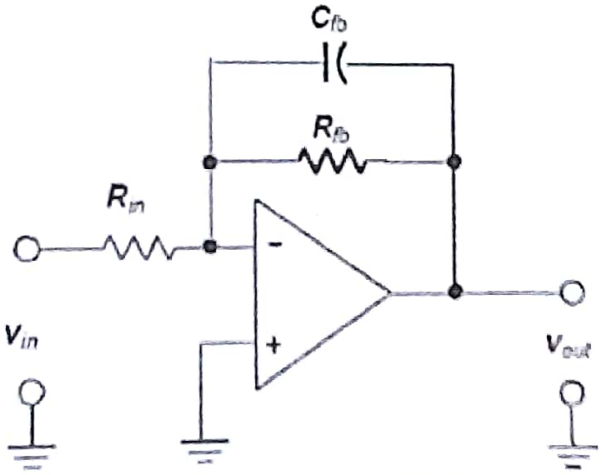

Fig.3: Leaky Integrator Circuit

Integration will be performed only at frequencies above the break frequency caused by the feedback resistor:

$$f_B = \frac{1}{2\pi R_{fb} C_{fb}} \qquad (4)$$

The opposite of integration is differentiation. A differentiator circuit produces an output that is proportional to the derivative or rate of change of the input voltage over time. Differentiator circuit can be constructed as shown using an operational amplifier, a resistor, and a capacitor. Unlike an ideal integrator circuit where the slightest DC offset in the input eventually drives the output into saturation, for the differentiator we need not be concerned about a DC offset in the input since the derivative of a constant is always zero.

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For this circuit, it can be shown that:

$$V_{out} = -RC\frac{dV_{in}}{dt} \qquad (5)$$

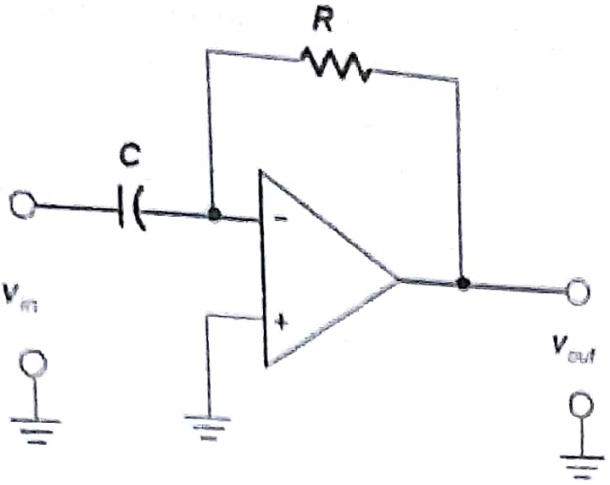

Fig 4: Differentiator Circuit

Since the output voltage of a differentiated is proportional to the input frequency, high frequency signals (such as electrical noise) may saturate or cutoff the amplifier. For this reason: a resistor is placed in series with the capacitor in the input as shown in Figure 5. This establishes high frequency limit beyond which differentiation no longer occurs:

$$f_B = \frac{1}{2\pi R_{in} C_{in}} \qquad (6)$$

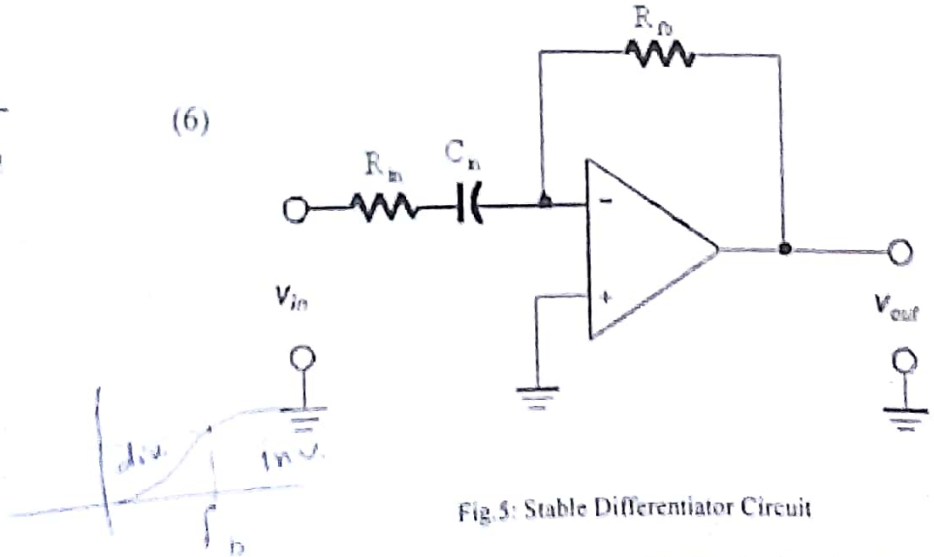

Fig.5: Stable Differentiator Circuit

To achieve greater attenuation at higher frequencies (or prevent oscillation), a feedback capacitor is added in parallel with the feedback resistor. This establishes another break frequency that can be calculated as in the integrator.

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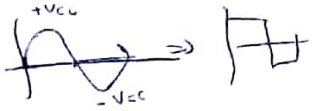
PROCEDURE:



Part 1: Comparator with 741 IC Used as a Level Detector

1. Construct the circuit of Figure 6. Adjust the function generator to produce a 5-V_{p-p} sine wave at a frequency of 1 KHz. Measure and record the resistor values.

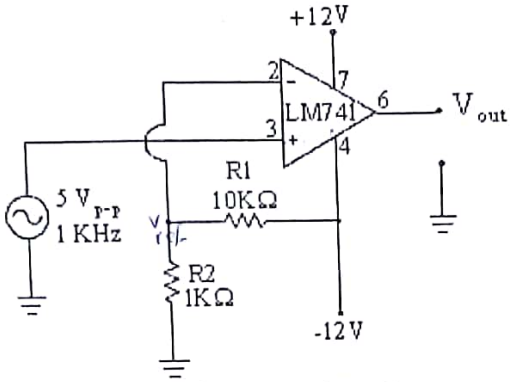
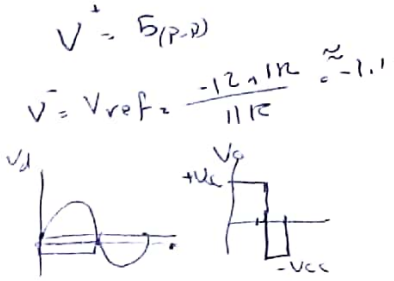


Fig.6: Comparator Circuits



2. Set up your oscilloscope so that both channels are ground-referenced to the center of the Osc. Screen. (This will enable you to use the oscilloscope to measure the value of input voltage that causes the op-amp output to change states). To establish the center of the grid as the ground reference:

   - Set GND switch to the ground (GND) position.
   - Move both channels to the center of the CRT display.
   - Set both switches to the DC position to provide dc coupling.

3. Observe the circuit input and output for the same vertical sensitivity (V/Div). Determine the magnitude of the input voltage at which the output changes state, and record this value.

4. Sketch both waveforms.

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Part 2: Integrator

5. Connect the circuit shown in Figure 7.

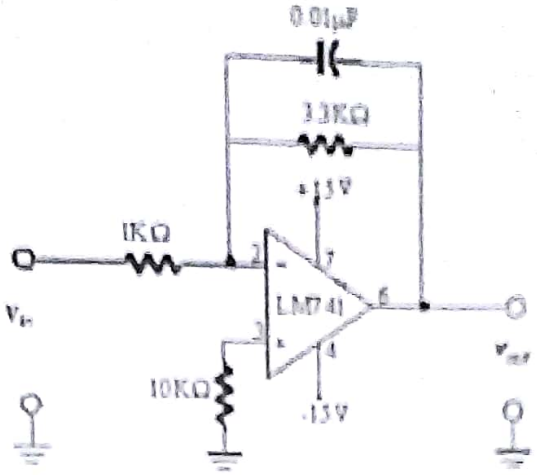

Fig.7: Integrator Circuit

6. Apply a $3V_{p-p}$ of 500Hz sine wave to the integrator and sketch the observed V_{in} and V_{out} on the same time scale. Note any phase shift of the output voltage with respect to the input voltage.

7. Vary the frequency of V_{in} frown 500Hz to 50KHz. Calculate the gain in dB.

8. Record the results in the Table 1 and plot the gain vs. frequency on semi-log graph paper.

Frequency (Hz)	V_{in} (Volt)	V_{out} (Volt)	$\left\lvert \frac{V_{out}}{V_{in}} \right\rvert_{dB}$	Phase Shift
500				
1K				
5K				
10K				
50k				

Table 1: Frequencies Values

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Part 3: Differentiator

9. Connect the circuit shown in Figure 8.

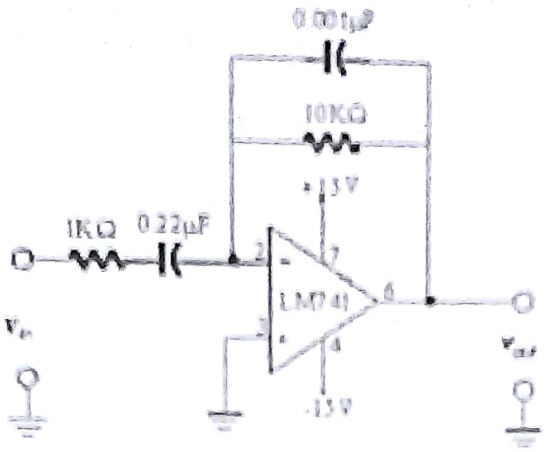

Fig 8: Differentiator Circuit

10. Apply a 1 V_p sine wave at 500 Hz to the differentiator and sketch the observed V_{in} and V_{out} on the same time scale. Note any phase shift of the output voltage with respect to the input voltage.

11. Vary the frequency of V_{in} as shown in the Table 2 and record the results. Calculate the gain in dB.

Frequency (Hz)	V_{in} (Volt)	V_{out} (Volt)	$\left\lvert \frac{V_{out}}{V_{in}} \right\rvert_{dB}$	Phase Shift
500				
200				
1000				

Table 2: Frequencies Values

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QUESTIONS & PROBLEMS:

1. Using the nominal values of the resistors shown in Figure 6, calculate V_{ref}. Compare this value to the voltage measured in Step (3)? Explain any discrepancy between the two values.

2. Refer to the waveforms you recorded in Figure 6. Explain the input/output relationship that you observed for these two circuits.

3. Refer to Figure 7: What is the cutoff frequency with R_s connected?

4. In step (8), explain why the output peak-to-peak value decreases as the frequency is increased.

5. Refer to Figure 8: What are the theoretical break frequencies for the differentiator?

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Lab Session 8

JFET Amplifiers

OBJECTIVES:

After performing this experiment, you should be able to:

- Measure and graph the drain characteristic curves for a junction field-effect transistor (JFET).
- Measure $V_{GS(off)}$ and I_{DSS} for a JFET.
- Measure the DC and AC parameters for self-biased common-source and common-drain amplifiers.
- Explain the differences between the AC operating characteristics of typical common source and common-emitter amplifiers.
- Test a common-drain amplifier with current-source biasing.

SUMMARY OF THEORY:

The bipolar junction transistor (BJT) uses base current to control collector current. Unlike the BJT, the field-effect transistor (FET) is a voltage-controlled device that uses an electrostatic field to control current. The FET begins with a doped piece of silicon called a channel. On one end of the channel is a terminal called the source and on the other end of the channel is a terminal called the drain. Current in the channel is controlled by a voltage applied to a third terminal called the gate.

Field-effect transistors are classified as either junction-gate (JFET) or insulated-gate (IGFET) devices. The JFET has a reverse-biased diode at the gate whereas the IGFET uses a thin glass-insulting layer. Since the gate circuit of either type of FET draws almost no current, the input resistance is extremely high. Both types have similar AC characteristics but differ in biasing methods.

The gate of a JFET is made of the opposite type of material than the channel, forming a PN junction between the gate and channel. Application of a reverse-bias on this junction decreases the conductivity of the channel, reducing the source-drain current. The gate diode should never be forward-biased. The JFET comes in two forms, n-channel and p-channel. The n-channel is distinguished on drawings by an inward arrow on the gate connection while the p-channel has an outward pointing arrow on the gate as shown in Figure 1. A typical JFET package is shown in Figure 1(c).

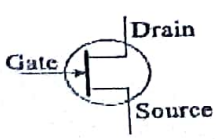
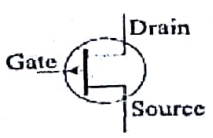
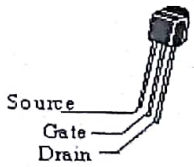


Fig.1: (a) n-Channel JFET



(b) p-Channel JFET



(c)Typical JFET Package

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The characteristic drain curves for a JFET exhibit several important differences from the BJT. In addition to the fact that the JFET is a voltage-controlled device, the JFET is a normally ON device. In other words, a reverse-bias voltage must be applied to the gate-source PN junction in order to close off the channel and prevent drain-source current. When the gate is shorted to the source, there is maximum allowable drain-source current. This current is called I_{DSS} for Drain-Source current with gate shorted. Another important difference is that the JFET exhibits a region on its characteristic curve where drain current is proportional to the drain- source voltage. This region, called the *ohmic region*, has important applications as a voltage- controlled resistance.

A useful specification for estimating the gain of a JFET is called the transconductance, which is abbreviated g_m. Recall that conductance is the reciprocal of resistance. Since the output current is controlled by an input voltage, it is useful to think of any FET as a transconductance amplifier. The transconductance can be found by dividing a small change in the output current by a small change in the input voltage.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \qquad (1)$$

As you know, bias is the application of DC voltages to set up the proper quiescent conditions for circuit operation. A satisfactory bias circuit for a FET depends on its type. With depletion-mode devices, which include all JFETS and some D-MOSFETS, the gate must be reverse biased (or zero biased) with respect to the source. These devices are normally on - they are turned off by applying reverse bias to the gate. Most MOSFETS operate as enhancement mode devices (all E-MOSFETS and some D-MOSFETS) and require bias to turn them on.

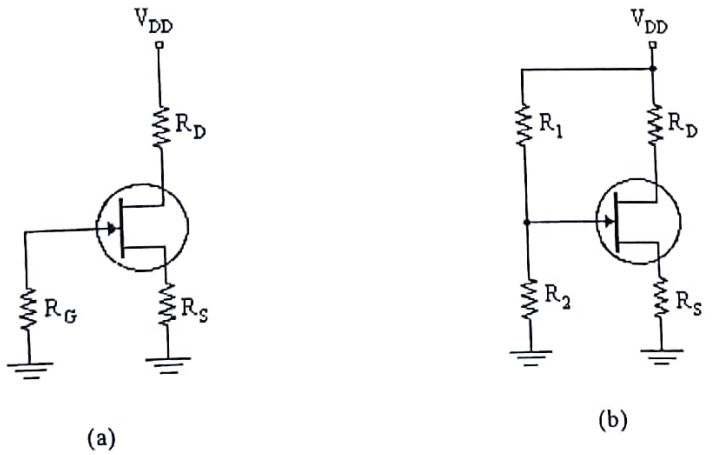

Fig.2: (a) Self-Bias (b) Voltage Divider Bias

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Self-bias is the most common type of bias for JFETs and is illustrated in Figure 2(a). The drain current, I_D, is in the source resistor, creating a voltage $V_S = I_D R_S$ at the source terminal. Since the gate is at ground potential (0 V), the gate-source voltage must have the same magnitude but opposite sign to the voltage drop across R_S (by Kirchhoff's voltage law). For an n-channel device, $V_{GS} = -V_S$. This provides the required reverse bias on the gate. Self-bias tends to compensate for different device characteristics between various FETs. For example, if a device with higher transconductance is put in the circuit, the drain current increases along with the voltage drop across R_S. This increased voltage tends to bias the FET off, compensating for the higher transconductance.

An even more stable form of bias combines self-bias with voltage-divider bias as illustrated in Figure 2(b). The voltage-divider connected to the gate biases the gate at some positive voltage. Unlike bipolar transistors, the JFET draws almost no input current, so the divider resistors can be much larger. The source voltage must still be more positive than the gate in order to establish the proper gate-source reverse bias. To accomplish this, the source resistor is made large enough to develop a positive voltage with respect to the gate (much larger than in self-bias). The net result is that transistor variations have less effect on the operating point than self-bias, producing a more stable form of biasing. The drain current is fairly Independent of the transistor; however, the drain-source voltage must be large enough to assure that the transistor is operating in the constant-current region.

There are several similarities between common-source (CS) and common-emitter (CE) amplifiers. Both provide a measurable amount of voltage gain, and both have a 180° voltage phase shift between their input and output signals. At the same time, however, they also have several differences.
Perhaps the biggest difference is that JFETs are voltage-controlled devices and BJTs are current-controlled devices. Also, the CS amplifier typically has much higher input impedance than the CE amplifier. Finally, the voltage gain calculation for a CS amplifier is very different from that of a CE amplifier.

In this experiment, you will test AC configurations of JFET amplifiers, beginning with a self-biased common-source amplifier as illustrated in Figure 3(a), then a self-biased common-drain amplifier as illustrated in Figure 3(b).

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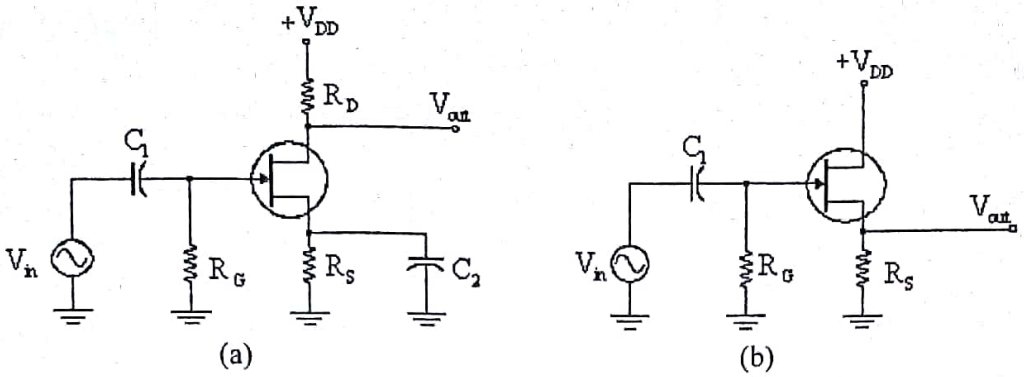

Fig.3: (a) Common Source Amplifier (b) Common Drain Amplifier

The DC bias of a JFET is determined by the device transfer characteristic (V_p and I_{DSS}) and the DC self-bias determined by the source resistor. The AC voltage gain at this DC bias point is then dependent on the device parameters (g_m) and circuit drain resistance.

AC Voltage Gain: The voltage gain of the amplifier as in Figure 1 is calculated from

$$A_V = \frac{V_{out}}{V_{in}} = -g_m R_D \qquad \left[-g_m (R_D \| R_L) \right] \tag{1}$$

Where:

$$g_m = g_{m0}\left(1 - V_{GS}/V_P\right) \quad \text{with } g_{m0} = \frac{2I_{DSS}}{V_P} \tag{2}$$

$$V_P = \frac{V_{GS}}{1 - \sqrt{\frac{I_D}{I_{DSS}}}}$$

AC Input Impedance: The AC input impedance is

$$R_{in} = R_G \tag{3}$$

AC Output Impedance: The AC output impedance is

$$R_{out} = R_D \tag{4}$$

EQUIPMENTS:

- Variable DC power supply
- Function generator
- Dual-trace oscilloscope
- Breadboard
- Resistors, Capacitors
- 2N3819A JFET Transistor (or equivalent)

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PROCEDURE:

Part 1: Current Voltage characteristic

1. Measure and record the value of the resistors listed in Table 1. R_1 is used for protection in case the JFET is forward-biased accidentally. R_2 serves as a current-sensing resistor.

Resistor	Listed Value	Measured Value
R_1	10 kΩ	
R_2	100 Ω	

Table.1

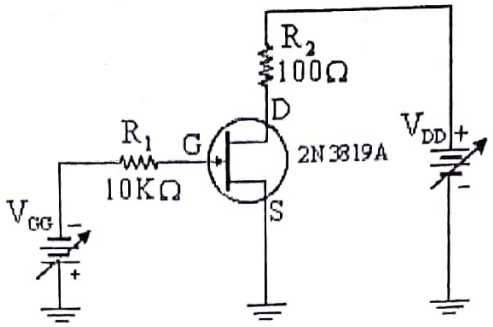

Fig.4: JFET Circuit

2. Construct the circuit shown in Figure 4. Start with V_{GG} and V_{DD} at 0 V. Connect a voltmeter between the drain and source. Keep V_{GG} at 0 V and slowly increase V_{DD} until V_{DS} is 1.0 V. (V_{DS} is the voltage between the transistor's drain and source).

3. With V_{DS} at 1.0 V, measure the voltage across R_2 (V_{R2}). Compute the drain current, I_D, by applying Ohm's law to R_2. Note that the current in R_2 is the same as I_D for the transistor. Use the measured voltage, V_{R2}, and the measured resistance, R_2, to determine I_D. Enter the measured value of V_{R2} and the computed I_D in Table 2 under the columns labeled Gate Voltage = 0 V.

4. Without disturbing the setting of V_{GG}, slowly increase V_{DD} until V_{DS} is 2.0 V. Then measure and record V_{R2} for this setting. Compute I_D as before and enter the measured voltage and computed current in Table 2 under the columns labeled Gate Voltage = 0 V.

	Gate Voltage = 0 V		Gate Voltage = -1.5 V	
V_{DS} (measured)	V_{R2} (measured)	I_D (computed)	V_{R2} (measured)	I_D (computed)
1.0 V				
2.0 V				
3.0 V				
4.0 V				

Table.2: Data of Drain Characteristics Curves for JFET Transistor

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5. Repeat step (4) for each value of V_{DS} listed in Table 2.

6. Adjust V_{GG} for -0.5 V. This applies -0.5 V between the gate and source because there is almost no gate current into the JFET and almost no voltage drop across R_1. Reset V_{DD} until V_{DS} = 1.0 V. Measure V_{R2} and compute I_D as before. Enter the values in Table 2 under the columns labeled Gate Voltage = -0.5 V.

7. Without changing the setting of V_{GG}, adjust V_{DD} for each value of V_{DS} listed in Table 2 as before. Compute the drain current at each setting and enter the voltage and current values in Table 2 under the columns labeled Gate Voltage = -0.5 V.

8. Adjust V_{GG} for -1.5 V. Repeat step (7), entering the data in the columns labeled Gate Voltage = -1.0 V.

9. The data in Table 2 represent four drain characteristic curves for your JFET. The drain characteristic curve is a graph of V_{DS} versus I_D for a constant gate voltage. Plot the four drain characteristic curves. Choose a scale for I_D that allows the largest current observed to fit on the graph. Label each curve with the gate voltage it represents.

10. In this step you will determine the value of $V_{GS(off)}$. Set V_{DD} for +12 V and V_{GG} for 0 V. Monitor the voltage across R_2 and slowly increase the negative gate voltage. When the voltage across R_2 reaches zero, note the gate voltage. Record this value as $V_{GS(off)}$. Record I_{DSS} from reading Plot obtained from step (10). These are the key parameters for your JFET.

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Common-Source JFET Amplifier

1. Measure and record the resistance value of the resistors listed in Table 3.

Resistor	Listed Value	Measured Value
R_S	1.0 KW	
R_D	3.3 KW	
R_G	1.0 MW	
R_L	10 KW	

Table.3: Values of Used Resistors

2. Construct the circuit shown in Figure 5.
3. Restore the initial settings and turn on the function generator as shown in Figure.5. Set the signal generator for 500 mV_{pp} sine wave at 1.0 kHz. Check the amplitude and frequency with your oscilloscope.

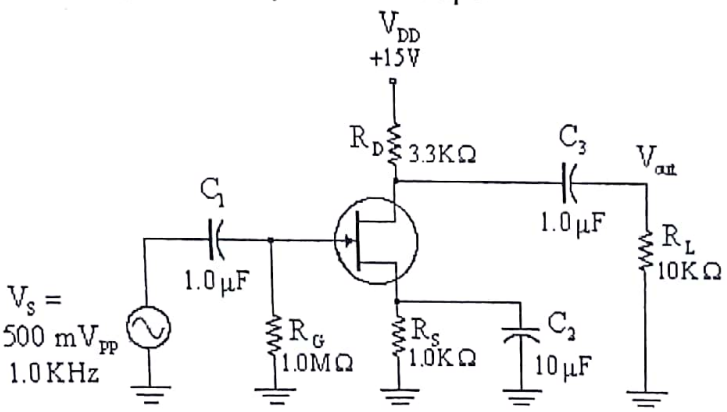

Fig.5: Common Source Amplifier

4. Measure the DC voltage at the drain, source, and gate. Use the source voltage and source resistance to compute I_D. Enter the data in Table 4. Compare the input and output AC voltage by viewing V_{in} and V_{out} simultaneously on a two-channel oscilloscope. Measure the voltage gain and note the phase difference (0 or 180°) between the input and output signals. Record these values in Table 4.

DC & AC Parameters	DC Values	AC Values
Gate Voltage, V_G		
Source Voltage, V_S		
Drain Voltage, V_D		
Drain Current, I_D		
Input Voltage, V_{in}		
Output Voltage, V_{out}		
Voltage Gain, A_V		
Phase Difference		

Table.4: Data for Common Source Amplifier

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Common-Drain Self-Biased JFET Amplifier

5. Change the circuit to the self-biased common-drain configuration as shown in Figure 6. The drain is connected directly to +15 V. Observe the input and output AC voltages with the oscilloscope. Measure the voltage gain and note the phase. Enter the data in Table 5.

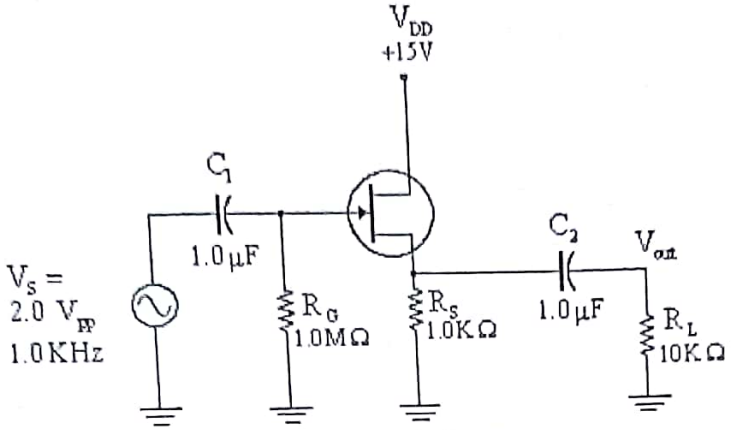

Fig.6: Common Drain Amplifier

DC & AC Parameters	DC Values	AC Values
Input Voltage, V_{in}		
Output Voltage, V_{out}		
Voltage Gain, A_V		
Phase Difference		

Table.5: Data for Common Drain Self-Biased Amplifier

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EVALUATION AND REVIEW QUESTIONS:

1. (a) Explain how to find I_{DSS} from the characteristic curves of a JFET.

2. Look up the meaning of pinch-off voltage, V_P, when $V_{GS} = 0$. Note that the magnitude of V_{GS} is equal to the magnitude of V_P so we can use the characteristic curve for $V_{GS} = 0$ to determine V_P. Using the data from this experiment, determine the pinch-off voltage for your JFET.

3. (a) What advantage does a common-drain amplifier have compared to a common-emitter amplifier?

   (b) What disadvantage does a common-drain amplifier have compared to a common- emitter amplifier?

4. Compare the common-source and common drain amplifiers tested in this experiment. What are the significant differences between them? What things do they have in common?

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Lab Session 9
Amplifier Frequency Response

OBJECTIVES:

After performing this experiment, you should be able to:

- Compute the three lower break frequencies for a CE amplifier and use them to compute the overall lower critical frequency, f_{CL}.
- Measure the overall low-frequency response of the CE amplifier.
- Measure the phase difference between the input and output signals at the critical frequency.
- Compute the upper break frequencies for a CE amplifier and the overall upper critical frequency, f_{CU}.
- Measure the overall upper critical frequency of the CE amplifier.

Summary of Theory:

The frequency response of an amplifier is the variation in the output as the frequency is varied. The analysis of the frequency response of an amplifier can be considered in three frequency ranges: the low-, mid-, and high-frequency regions. In the low-frequency region the capacitors used for DC isolation (AC coupling) and bypass operation affect the lower cutoff (lower 3-dB) frequency. In the mid- frequency range only resistive elements affect the gain, the gain remaining constant. In the high-frequency region of operation, stray wiring capacitances and device inter-terminal capacitances will determine the circuit's upper cutoff frequency.

Amplifier Low Frequency Response: If a capacitor is in series with the signal path, a high-pass filter is formed causing low signal frequencies to be attenuated at the output. The input and output coupling capacitors are examples of series capacitors. In performing their intended job of blocking DC, they also attenuate low signal frequencies, causing an AC signal to be developed across them. Also, a phase shift is introduced by the coupling capacitors because C_1 forms a lead circuit with R_{in} of the amplifier, and C_3 forms a lead circuit with R_L and R_C as shown in Figure 1.

The effect of the coupling capacitors is illustrated in Figure 1. Looking into the amplifier, as illustrated in Figure 1(a), you see an equivalent capacitor in series with the input resistance of the amplifier, forming the high-pass filter shown in Figure 1 (b).

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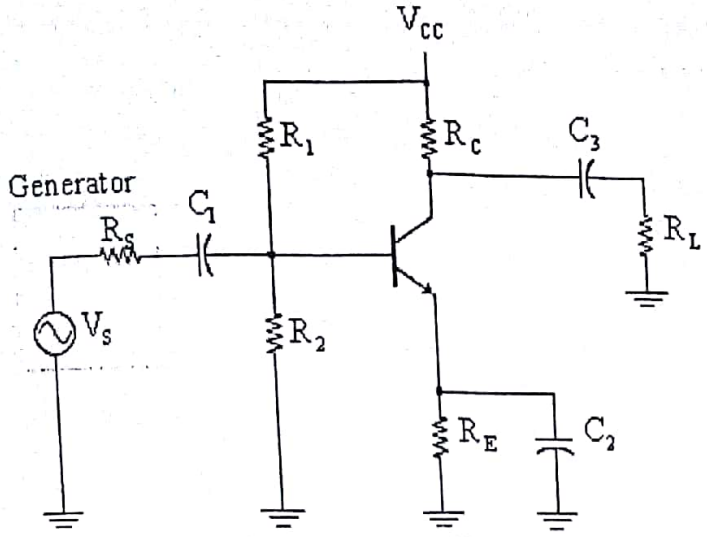

Fig.1 (a): CE Amplifier

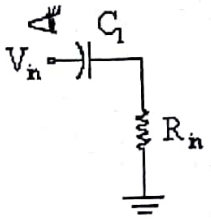

Fig.1 (b): Input High Pass Filter

The cutoff frequency due to the input coupling capacitor is:

$$f_{C1} = \frac{1}{2\pi\,(R_i + R_S)C_1}\ \text{Hz} \qquad \text{With: } R_i = R_1 \| R_2 \| \beta r_e \tag{1}$$

The phase shift introduced due to the input coupling capacitor is:

$$\theta = \tan^{-1}\left(\frac{X_{C1}}{R_{in} + R_S}\right) \tag{2}$$

The output coupling capacitor forms the same type of network. The cutoff frequency due to the output coupling capacitor is:

$$f_{C3} = \frac{1}{2\pi\,(R_C + R_L)C_3}\ \text{Hz} \tag{3}$$

The phase shift introduced due to the output coupling capacitor is:

$$\theta = \tan^{-1}\left(\frac{X_{C3}}{R_C + R_L}\right) \tag{4}$$

Another RC circuit that affects the low frequency response is when a parallel bypass capacitor is across the emitter resistor, R_E. Recall that the gain of a CE amplifier is determined by the ratio of the AC collector resistance to the AC emitter resistance. When a bypass capacitor is placed across R_E, the AC resistance in the emitter circuit is much lower for frequencies above the critical frequency, causing the gain to be higher. Below the critical frequency, the bypass capacitor looks open, causing the gain of the amplifier to be reduced. The cutoff frequency due to the emitter bypass capacitor is:

$$f_{C2} = \frac{1}{2\pi\,R_e C_2}\ \text{Hz} \qquad \text{With: } R_e = R_E \| (r_e + R_{th}/\beta) \tag{5}$$

$$\text{Where: } R_{th} = R_1 \| R_2 \| R_S$$

Lower Cutoff (lower 3-dB) Frequency: Each capacitor used will result in a lower cutoff frequency. The overall lower cutoff frequency at the network is then the largest of these lower cutoff frequencies.

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Amplifier High Frequency Response: The upper frequency response of an amplifier is typically controlled by the parallel (shunt) capacitances that are internal capacitances formed between each pair of terminals of a transistor. Capacitance that is in parallel with the signal path forms a low pass filter causing higher signal frequencies to be attenuated at the output. The frequency at which the internal capacitance becomes important is dependent on the circuit and the device, but it is typically well above 1 MHz. To reduce these frequencies, so they can be measured more accurately we will add additional capacitance in this experiment between the various leads of the transistor.

A typical transistor amplifier, showing the various shunt capacitances, is illustrated in Figure 2(a). At high frequencies, the coupling capacitors have very low reactance, so they can be ignored (placed with shorts). The equivalent high-frequency circuit is shown in Figure 2(b). The Thevenin resistance of the generator is part of the RC network, forming the low-pass filter. Notice that C_{bc} in the original circuit is shown as two Miller capacitances, $C_{in(Miller)}$ and $C_{out(Miller)}$ in the equivalent circuit.

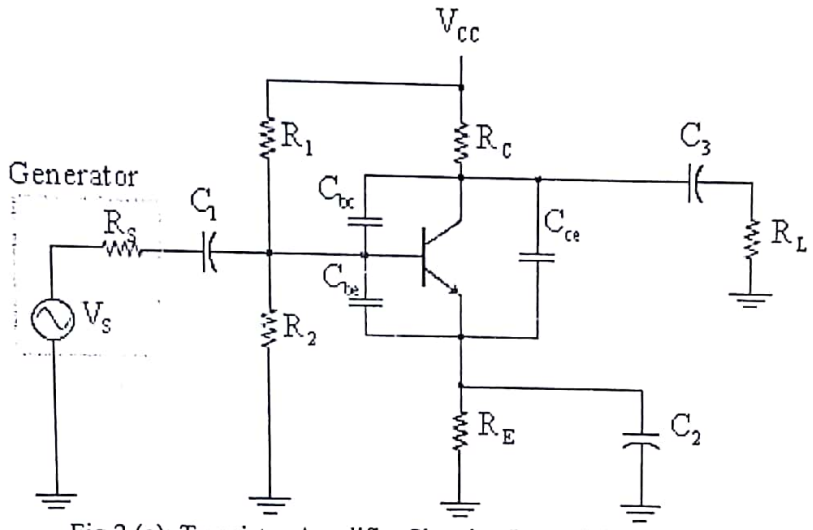

Fig.2 (a): Transistor Amplifier Showing Internal Capacitances

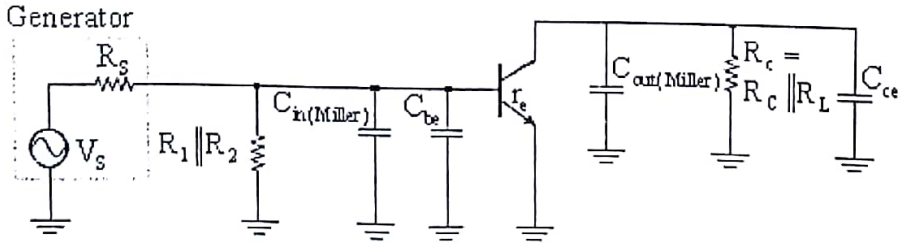

Fig.2 (b): Equivalent High Frequency Circuit

We can find the upper cutoff frequency by tracing the discharge path for the capacitors. On the input side, the equivalent capacitance is $C_{eq(in)} = C_{be} + C_{in(Miller)}$. Where $C_{in(Miller)} = C_{bc}\left(1+|A_V|\right)$. These capacitors can discharge through the parallel combination consisting of $R_{eq(in)} = (R_1 \| R_2) \| R_S \| (\beta r_e)$ as shown in the equivalent circuit. The cutoff frequency for the input circuit can be found from the equation:

$$f_{Hi} = \frac{1}{2\pi R_{eq(in)} C_{eq(in)}} \qquad (6)$$

Because the output voltage of a high- frequency input RC circuit is across the

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capacitor, the output of the circuit lags the input. The phase angle is expressed as:

$$\theta = \tan^{-1}\left(\frac{R_{eq(in)}}{X_{Ceq(in)}}\right) \tag{7}$$

At output connection of the circuit, the cutoff frequency can be found as:

$$f_{Ho} = \frac{1}{2\pi\, R_{eq(out)}\, C_{eq(out)}} \tag{8}$$

Where: $C_{eq(out)} = C_{ce} + C_{out(Miller)}$, $C_{out(Miller)} = C_{bc}\left(\frac{1+|A_V|}{|A_V|}\right)$

$$R_{eq(out)} = R_C \| R_L$$

The phase shift introduced by the output RC circuit is:

$$\theta = \tan^{-1}\left(\frac{R_{eq(out)}}{X_{Ceq(out)}}\right) \tag{9}$$

The most important parameter for high-frequency analysis with inverting amplifiers is the Miller capacitance. Other internal characteristics (such as varying β, internal base resistance, and stray capacitance) also affect the response, so the calculated cutoff frequency may differ from the measured one.

Upper Cutoff (upper 3-dB) Frequency: Each of the two capacitances used will result in an upper cutoff frequency. The overall upper cutoff frequency at the network is then the lower of the two critical high frequencies.

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PROCEDURE:

Part 1: Amplifier Low Frequency Response

1. Measure and record the values of the resistors listed in Table 1.

Resistor	Listed Value	Measured Value
R_S	620 Ω	
R_1	68 KΩ	
R_2	10 KΩ	
R_E	560 Ω	
R_C	3.9 KΩ	
R_L	10 KΩ	

Table.1: Resistors Values

Parameter	Computed Value	Measured Value
V_B		
V_E		
V_C		
V_{CE}		
I_E		
r_e		
A_V		
V_{out}		

Table.2: DC and AC Parameters of CE Amplifier

2. Compute the DC and AC parameters for the CE amplifier shown in Figure 3. Tabulate your calculations in Table 2 (the first five are DC parameters; the last three are AC).

3. Construct the amplifier shown in Figure 3. Then measure and record the parameters listed in Table 2 (in the open boxes) and confirm your calculations. Recheck your work if the calculated and measured values differ significantly.

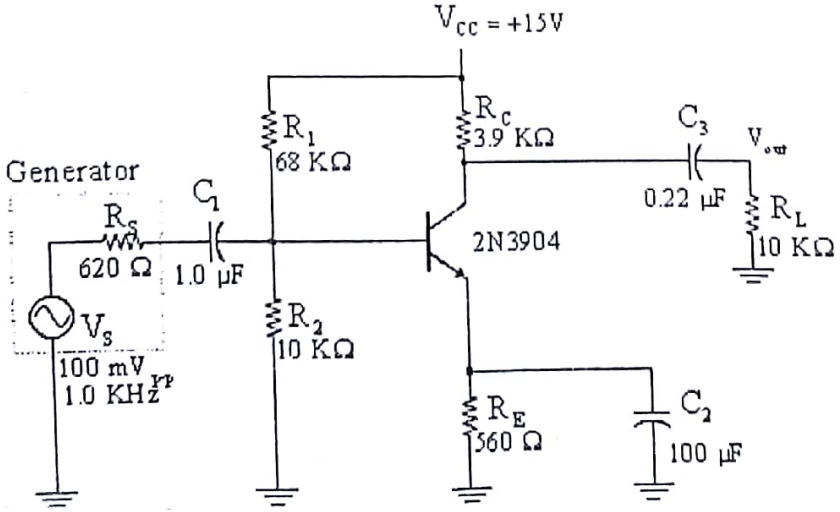

Fig.3: CE Amplifier

4. To compute the low-frequency response, it is necessary to find the equivalent resistance, R_{eq}, that represents the AC charge and discharge path for each capacitor. From the Summary of Theory, you find that R_{eq} for C_1 is $R_{eq} = (R_1 \| R_2 \| \beta r_e) + R_S$. Enter the computed value in Table 3.

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Capacitor	R_{eq}	$f_{critical}$
C_1		
C_2		
C_3		

Table.3: R_{eq} seen by Each Capacitor and their Lower Critical Frequencies

5. In the same manner as in step (4), you can trace the charge/discharge path for C_2 and C_3. For C_2, R_E is in parallel with the capacitor, and the combination consisting of r_e and the reflected resistance of the base circuit. (The reflected resistance of the base circuit is only 4 ohm to 6 ohm because it is divided by β to move it to the emitter circuit). Note that for C_3, the collector resistance appears to be in series with the load resistance. Compute the equivalent resistance seen by C_2 and C_3. Enter the computed values in Table 3.

6. Compute the critical frequency for each capacitor (C_1, C_2, and C_3). Use Eq(1), Eq(3) and Eq(5) from the Summary of Theory. Use the R_{eq} from Table 3 for each capacitor. Enter the computed critical frequency for each capacitor in Table 3. The overall lower cutoff frequency at the network is then the largest of these lower cutoff frequencies.

7. Measure the overall lower critical frequency of the amplifier. Observe the output signal in midband (around 10 KHz) and adjust the signal for 5.0 vertical divisions on the Osc. Screen. The output should appear undistorted. Reduce the generator frequency until the output falls to 70.7% (approximately 3.5 divisions) of the voltage in midband. This frequency is the low critical frequency of the amplifier. Measure and Record this value.

8. Maintaining the input voltage at the level set above, vary the frequency and measure and record V_{out} to complete Table 4.

Frequency (Hz)	V_{in} (Volt)	V_{out} (Volt)	$\left\lvert \frac{V_{out}}{V_{in}} \right\rvert_{dB}$	Phase Shift
50				
400				
800				
2 K				
5 K				
10 K				

Table.4: Voltage Gain vs Frequency

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Part 2: Amplifier High Frequency Response

9. Compute the DC and AC parameters for the CE amplifier shown in Figure 4. The purpose of C_4, C_5, and C_6 is to reduce the high-frequency response (as discussed in the Summary of Theory) to make it easier to measure; they do not affect any other parameter. Calculate the parameters in Table 5.

Parameter	Computed Value	Measured Value
V_B		
V_E		
V_C		
V_{CE}		
I_E		
r_e		
A_V		
V_{out}		

Table.5: DC and AC Parameters of CE Amplifier

10. Construct the amplifier shown in Figure 4. Measure and record the parameters listed in Table 5 (in the open boxes) and confirm your calculations. Recheck your work if the calculated and measured values differ significantly.

11. In this step, and in steps (12) and (13), you will compute the upper critical frequency due to the input network. First, determine the equivalent input capacitance, C_{in}, as illustrated in Figure 2. Assume C_{be} is equal to C_6 since the added capacitor is much larger than the actual base-emitter capacitance. This capacitance is in parallel with $C_{in(Miller)}$. The input capacitance is found from:

$$C_{eq(in)} = C_{be} + C_{in(Miller)}$$
$$= C_6 + C_4\left(1 + |A_V|\right) \qquad \text{(Use absolute value of gain)}$$

The base-collector capacitance, C_{bc}, is represented by C_4. In a small-signal transistor such as the 2N3904, this capacitance is small (3 pF to 5 pF). The added 100 pF capacitance in parallel is sufficiently large that you can ignore the actual internal capacitance of the transistor. Record the input capacitance on the first line (Step 11) of Table 6.

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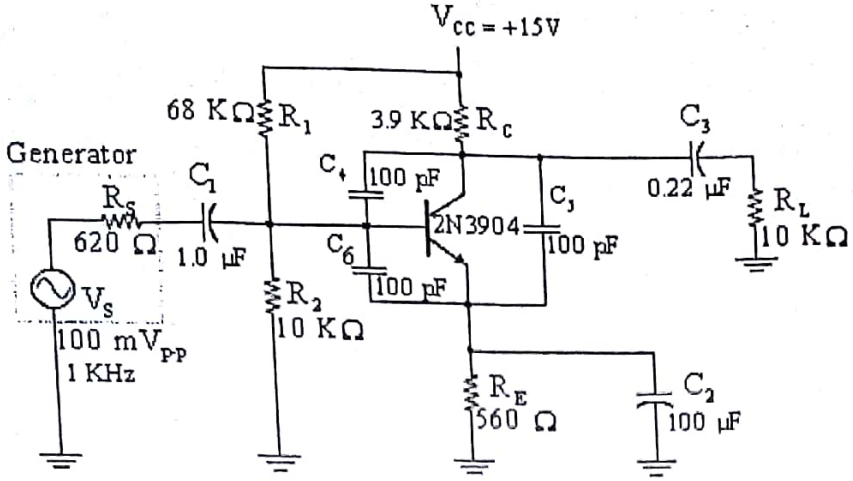

Fig.4: Measurement of High Frequency Response

12. Compute the equivalent resistance, $R_{eq(in)}$, seen by $C_{eq(in)}$ (illustrated in Figure 2 and described in the Summary of Theory). Enter the computed value in Table 6.

13. Compute the upper critical frequency due to the input network, f_{Hi}. Enter the computed value in Table 6.

Step	Parameter	Computed Value	Measured Value
11	$C_{eq(in)}$		
12	$R_{eq(in)}$		
13	f_{Hi}		
14	$C_{eq(out)}$		
15	R_c		
16	f_{Ho}		
17	f_{CU}		

Table.6: High-frequency Parameters

14. In this step, and in steps (15) and (16), you will compute the upper critical frequency due to the output network. Start by finding the equivalent output capacitance, $C_{eq(out)}$, as illustrated in Figure 2. Assume C_{ce} is equal to C_5 since the added capacitor is much larger than the actual collector-emitter capacitance. This capacitance is in parallel with the output Miller capacitance. The total output capacitance, $C_{eq(out)}$, is found from:

$$C_{eq(out)} = C_{ce} + C_{out(Miller)}$$

$$= C_5 + C_4\left(\frac{1+|A_V|}{|A_V|}\right) \qquad \text{(Use absolute value of gain)}$$

Record the output capacitance in Table 6.

15. Compute the equivalent resistance, R_c, seen by $C_{eq(out)}$, Since the transistor represents a current source, the capacitor charge/discharge path is only through $R_c \parallel R_L$ Enter the computed value in Table 6.

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16. Compute the upper critical frequency due to the output network, f_{Ho}. Enter the computed value in Table 6.

17. The overall upper critical frequency of the amplifier will be the lower of the two critical high frequencies. Enter the computed overall upper frequency, f_{CU}, in Table 6. Then, observe the output signal in midband (about 1 kHz) and adjust the signal for 5.0 vertical divisions on the scope face. The output should appear undistorted. Increase the generator frequency until the output falls to 70.7% (approximately 3.5 divisions) of the voltage observed in midband. This frequency is the upper critical frequency, f_{CU}. Measure and record this frequency in Table 6.

18. Apply an input that provides undistorted output voltage and complete Table 7.

Frequency (KHz)	V_{in} (Volt)	V_{out} (Volt)	$\left\lvert \frac{V_{out}}{V_{in}} \right\rvert_{dB}$	Phase Shift
10				
100				
500				
700				
1000				
2000				

Table.7: Voltage Gain vs Frequency

19. Using the semi-log paper, plot the gain versus frequency over the full frequency range obtained from steps (8) and (18). Plot the actual points and connect to obtain the actual plot. Use straight-line approximation curves to obtain the Bode plot.

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EVALUATION AND REVIEW QUESTIONS:

1. The critical frequency occurs at the frequency at which the output voltage drops to 70.7% of the midband voltage. Prove that this is also the half-power frequency.

2. Assume capacitor C_2 was open. How would this affect:
   (a) The gain of the amplifier?
   (b) The low critical frequency of the amplifier?
   (c) The high critical frequency of the amplifier?

3. Assume the measured lower cutoff frequency was much higher than it should be but other parameters (AC and DC) were normal. You assume one of the capacitors is the wrong size. How could you use another capacitor to quickly isolate which capacitor was incorrect?

4. Assume the amplifier shown in Figure 4 contained an unbypassed 10-ohm resistor in the emitter circuit. What effect does this have on the:
   (a) Gain?
   (b) Miller capacitance?
   (c) Upper critical frequency?

5. Consider the three capacitors that were placed between the transistor leads (C_4, C_5, and C_6). Which had the greatest effect on the upper critical frequency? Explain your answer.

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