The Hashemite University

Department of Electrical Engineering

Electronics.1 Laboratory Manual

Table of Content

General Lab Rules

- Be **PUNCTUAL** for your laboratory session.
- Foods, drinks and smoking are NOT allowed.
- Open-toed shoes are NOT allowed.
- The lab timetable must be strictly followed. Prior permission from the Lab Supervisor must be obtained if any change is to be made.
- Experiment must be completed within the given time.
- Respect the laboratory and its other users. Noise must be kept to a minimum.
- Workspace must be kept clean and tidy at all time. Points might be taken off on student/group who fail to follow this.
- Handle all apparatus with care.
- All students are liable for any damage to equipment due to their own negligence.
- At the end of your experiment make sure to switch off all the instruments.
- Students are strictly PROHIBITED from taking out any items from the laboratory without permission from the Lab Supervisor.
- Students are NOT allowed to work alone in the laboratory.
- Please consult the Lab Supervisor if you are not sure on how to operate the laboratory equipment.
- Report immediately to the Lab Supervisor if any injury occurred.
- Report immediately to the Lab Supervisor any damages to equipment, hazards, and potential hazards.
- Please refer to the Lab Supervisor should there be any concerns regarding the laboratory.

Grading Policy

The total mark for this lab is distributed as follows

Lab Report	20%
Quizzes	10%
Prelab	5%
Attendance	5%
Mid-term Exam	20%
Final Exam	40%

Guidelines for Writing Lab Report

The most effective way to acquire the practical skills in engineering studies is usually by experimenting in a laboratory. The process of experimentation involves organization, observation, familiarization with various pieces of equipment, working with others, writing, and communicating ideas and information. These are the skills required of an engineer.

In a practical situation, such as that in the industry or university research, experiments are designed for the purpose of clarifying research questions or conflicting theories by means of collecting a series of data. The conclusions drawn from that data can be used to validate a theory or sometimes to develop a theory that explains the behavior of an engineering object. The report for this kind of experiments must includes an introduction to the topic and purpose of the experiment, the theory, method, procedure, equipment used in the experiment, the data presented in an organized manner, and the conclusions based on the data gathered.

In engineering education, lab experiments are usually designed to enhance the understanding in engineering topics. Students are supposed to "dirty their hand" in preparing the experiment setup, organize the experiment flow, and learn to observe the salient features as well as to spot any unexpected occurrence as part of the training to acquire the practical skill to become an engineer. Although the introduction and the procedure are usually given in the lab handouts, students should practice writing a proper lab report which includes all the necessary sections, targeting at a reader who does not have any prior knowledge about the experiment. This is to develop the skill in documenting the laboratory work and communicating that experience to others. This write-up gives some guidelines on what to write in each section in preparing laboratory reports for engineering curricula.

Title Page

The title page should contain the title of the experiment, the code and title of the course, the name of the writer, the date when the experimental work was performed, submission date of the lab report, and the name of lecturer for whom the report is prepared for.

Introduction or Objectives

An introduction is necessary to give an overview of the overall topic and the purpose of the report. The motivation to the initialization of the experimental work can be included. Its content should be general enough to orientate the reader gracefully into the subject materials.

Theoretical Background

This section is to discuss the theoretical aspects leading to the experiment. Typically, this involves the historical background of the theories published in the research literature and the questions or ambiguities arose in these theoretical work. Citations for the sources of information should be given in one of the standard bibliographic formats (for example, using square brackets with the corresponding number [2] that points to the List of References). Explore this background to prepare the readers to read the main body of the report. It should contain sufficient materials to enable the

readers to understand why the set of data are collected, and what are the salient features to observe in the graph, charts and tables presented in the later sections.

Depending on the length and complexity of the report, the introduction and the theoretical background may be combined into one introductory section.

Experimental Method, Procedure and Equipment

This section describes the approach and the equipment used to conduct the experiment. It explains the function of each apparatus and how the configuration works to perform a particular measurement. Students should not recopy the procedures of the experiment from the lab handout, but to summarize and explain the methodology in a few paragraphs.

Observations, Data, Findings, Results

The data should be organized and presented in the forms of graphs, charts, or tables in this section, without interpretive discussion. Raw data which may take up a few pages, and most probably won't interest any reader, could be placed in the appendices.

Calculations and Analysis

The interpretation of the data gathered can be discussed in this section. Sample calculations may be included to show the correlation between the theory and the measurement results. If there exists any discrepancy between the theoretical and experimental results, an analysis or discussion should follow to explain the possible sources of error.

The experimental data and the discussions may also be combined into one section, for example, under the heading called "Discussion of Experimental Results".

Conclusions

The conclusions section closes the report by providing a summary to the content in the report. It indicates what is shown by the experimental work, what is its significance, and what are the advantages and limitations of the information presented. The potential applications of the results and recommendations for future work may be included.

Appendices

The appendices are used to present derivations of formulae, computer program source codes, raw data, and other related information that supports the topic of the report.

List of References

The sources of information are usually arranged and numbered according to the order they are cited in the report. The reference materials may be entered in the following formats:

[1] Author, "Title of the book", 2nd edition, New York: Publisher, 1989.
[2] Author, "Title of the paper", Journal name, Vol. 2, No. 3, Jan 1990, pg. 456-458.
[3] Author, "Title of the paper", Proceedings of Conference 1991, pg. 5-6.
[4] Author, "Title of the thesis", Ph.D. thesis, Rice University, Houston, May 1973.

Electronics.1 Lab Experiments

Lab Session 1
Diode Characteristics

OBJECTIVES:

After completing this experiment, you should be able to:

- Measure the forward voltage across a diode, and determine if the component is faulty.
- Demonstrate the forward current and voltage characteristics of *pn*-junction and zener diodes.
- Demonstrate the reverse current and voltage characteristics of *pn*-junction and zener diodes.

SUMMARY OF THEORY:

The diode is a semiconductor device that conducts currents much more readily in one direction than in the other. The voltage across the diode terminals determines whether or not the diode will conduct. If the anode is more positive than the cathode, the diode will conduct currents and is said to be forward-biased. As *forward current* (I_F) increases, so does *forward voltage* (V_F) across the device. However, V_F increases at a much lower rate than I_F, because the forward resistance of a diode *decreases* as the I_F increases. Hence, V_F increases at a very low rate when a diode is operated above its *knee voltage* (V_γ). This is true of *pn* junction diodes, zener diodes, and even LEDs.

The following formula is used to calculate the dynamic or AC resistance of the diode:

Where:

$$r_D = \frac{\Delta V}{\Delta I} \quad (1)$$

ΔV: The small change in voltage across the diode.
ΔI: The corresponding change in current through the diode.

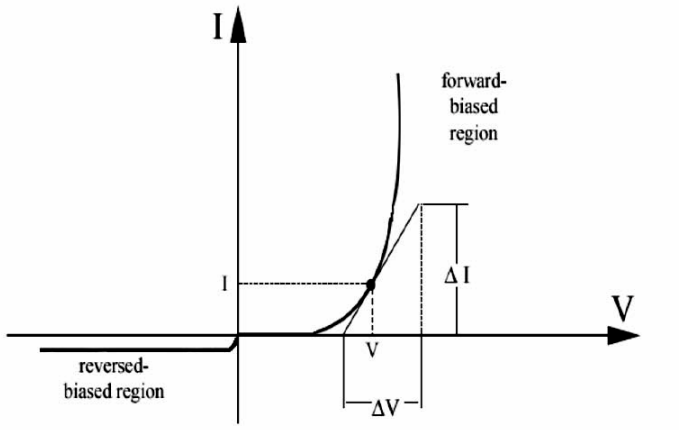


Fig.1: I-V Characteristic of Normal Diode.

The static or DC resistance at any point along the characteristic curve is calculated using Ohm's law:

$$R_D = \frac{V}{I} \quad (2)$$

Where:

V: The voltage across the diode.
I: The current through the diode.

These relationships can be seen in the characteristic curve shown in Figure1.

If the cathode is more positive than the anode, the diode will conduct only an extremely small leakage current and is said to be reversed-biased. When a *pn*-junction diode is reverse biased, the *reverse current* (I_R) through the device is extremely low, even with a significant reverse voltage applied. This is not necessarily the case with a *zener diode.* Zener reverse current remains low until V_R reaches the *zener voltage* (V_Z) rating of the component. When the magnitude of V_R reaches V_Z, I_R increases abruptly. The forward and reverse characteristics of *pn*-junction and zener diodes are the focus of the second part of this experiment.

A diode can be tested using a simple ohmmeter, but this is not a very accurate test. Most modern multimeters have a diode-checker function, which allows you to determine the actual voltage across a forward-biased diode. If the forward voltage falls within its expected range, the diode is considered good. If the diode test indicates the component is shorted or open, then the diode should be replaced.

MATERIALS:

1. Function Generator
2. Variable DC Power Supply
3. Digital Multimeter, DMM (with diode-check function)
4. Breadboard
5. 1N4001 Small Signal Diode
6. 1N5240 Zener Diode
7. Resistors

PROCEDURE:

Part 1: Diode Testing

Note: The schematic and component symbols for *pn*-junction and zener diodes are shown in Figure 2. Note that the indicator band on the component is always closest to the cathode terminal.

1. Set your DMM to the diode test position.

2. Connect the DMM to the 1N4001 diode as shown in Figure 2a. Measure the forward voltage (V_F) across the diode, and record your measurement in Table1.

Diode	V_F	V_R
1N4001 Normal Diode		
1N5240 Zener Diode		

Table1: Diode Test Measurements

3. Reverse the diode as shown in Figure 2a. Measure its reverse voltage (V_R), and record this reading in Table 1.

4. Repeat Steps (2) and (3) for the 1N5240 zener diode. Record the meter readings in Table 1.

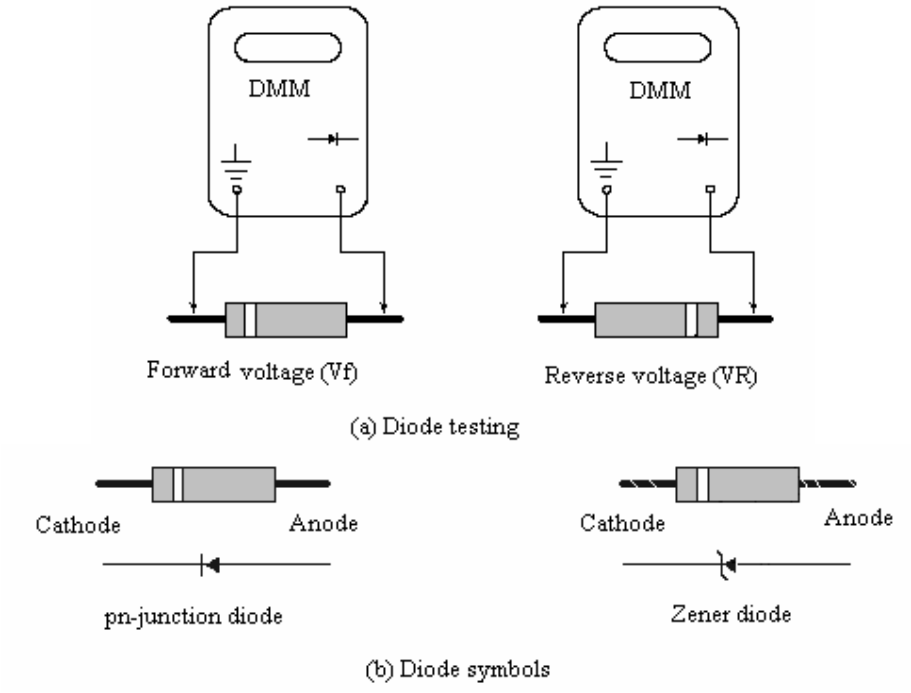


Fig.2: (a) Diode Testing (b) Diode Symbols

Part 2: Diode Voltage and Current Characteristics:

5. Construct the circuit shown in Figure 3. The voltage source should be set initially to 0.0 V. R_1 limits the diode current to a value lower than the rated maximum forward current.

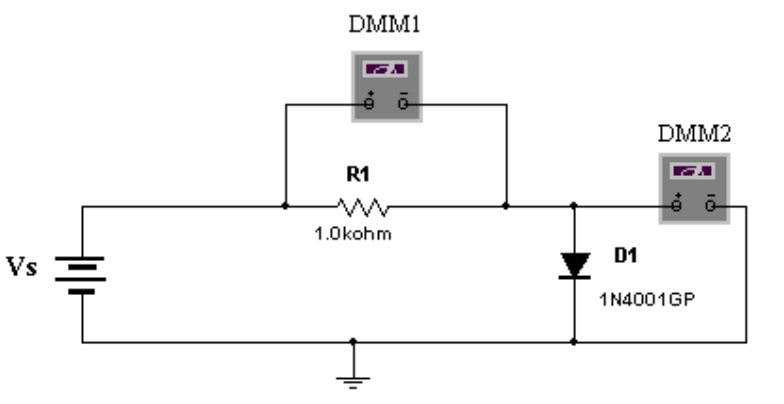


Fig.3: Measurement of the Forward Characteristics of Diode.

6. Measure V_F, V_{R1}, and compute I_F. Record these values in Table 2.

7. Repeat Step (6) for all the voltage values listed in Table 2.

8. Replace the normal diode with a zener diode. Repeat Steps (6) and (7) for the 1N5240 zener diode.

V_S (volt)	V_{R1} (volt)		V_F (volt)		$I_F = V_R / R$ (mA)	
	Normal	Zener	Normal	Zener	Normal	Zener
0.0						
0.2						
0.4						
0.6						
1.0						
3.0						
5.0						
7.0						
9.0						
11.0						
13.0						

Table2: Diode Forward Currents and Voltages

9. Use your results from Table 2 to plot the I_F versus V_F curve for both diodes in Figure 4.

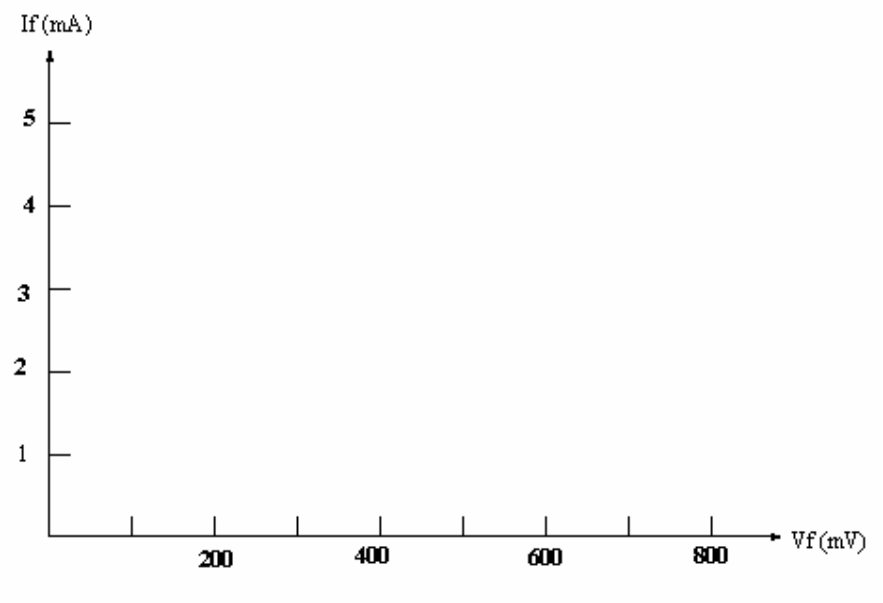


Fig.4: I_F versus V_F

10. Determine the static resistance of the normal diode at 1, 3, 5 and 10 volts using values obtained for I_F and V_F from Table l.

11. Graphically determine the dynamic resistance of the normal diode at 1, 3, 5, 7, and 13 volts using the I-V characteristic curve obtained in Figure 4.

12. To obtain the I-V characteristics of the diode using the oscilloscope, connect the circuit shown in Figure 5 below. Set the function generator to 10 V_{P-P}, 1KHz sinusoid input signal.

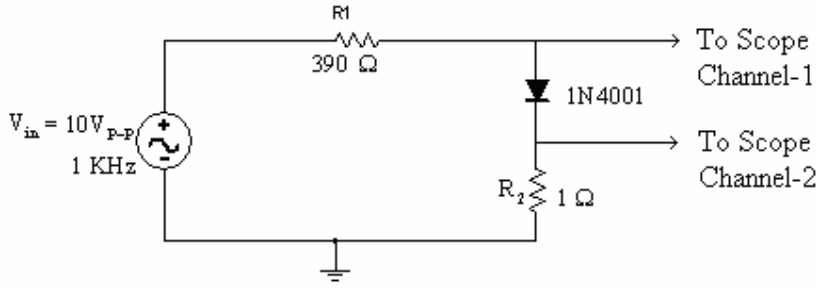


Fig.5: Measurement of I-V Characteristics using Oscilloscope

13. Set the oscilloscope to the x-y mode. Connect the horizontal input of the oscilloscope channel-l to the anode of the diode and the vertical input channel_2 to the cathode. Set the sensitivity of the vertical input to l0 mV/division and set the horizontal sensitivity at l mV/division. Draw the curve shown on the screen of the oscilloscope and find the junction potential.

14. Compare these results with the table you made.

15. Construct the circuit shown in Figure 6. Note that the 1N4001 diode is now reverse biased.

16. Measure and record V_{R1}. Use this value (and the measured value of R_1) to calculate I_{R1}. This equals the reverse current through the diode.

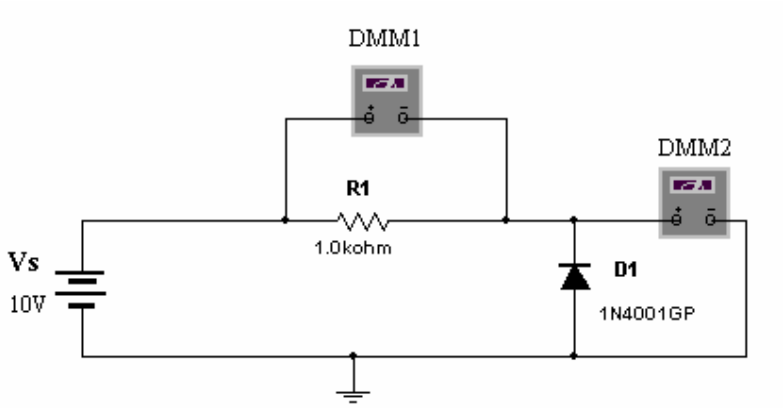


Fig.6: Measurement of I_{R1}

17. Construct the circuit shown in Figure 7.

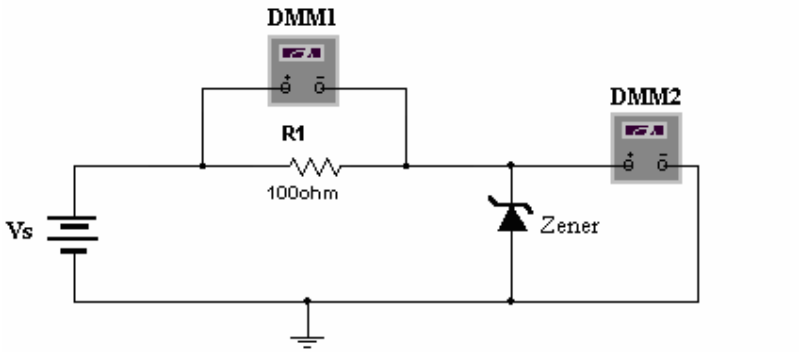


Fig.7: Zener Diode Test Circuit

18. Measure the voltage across the zener diode, and record this value in Table 3. Repeat this procedure for all the voltage values listed in the table.

V_S (volt)	V_{R1} (volt)	Vz (volt)	$I_Z = V_{R1} / R_1$ (mA)
0			
0.2			
0.4			
0.6			
1.0			
3.0			
5.0			
7.0			
9.0			
10.0			
12.0			
14.0			

Table.3: Measurement of V_{R1} and Vz

19. Use the values from Table 3 to plot the I_Z versus V_Z curve in Figure 8.

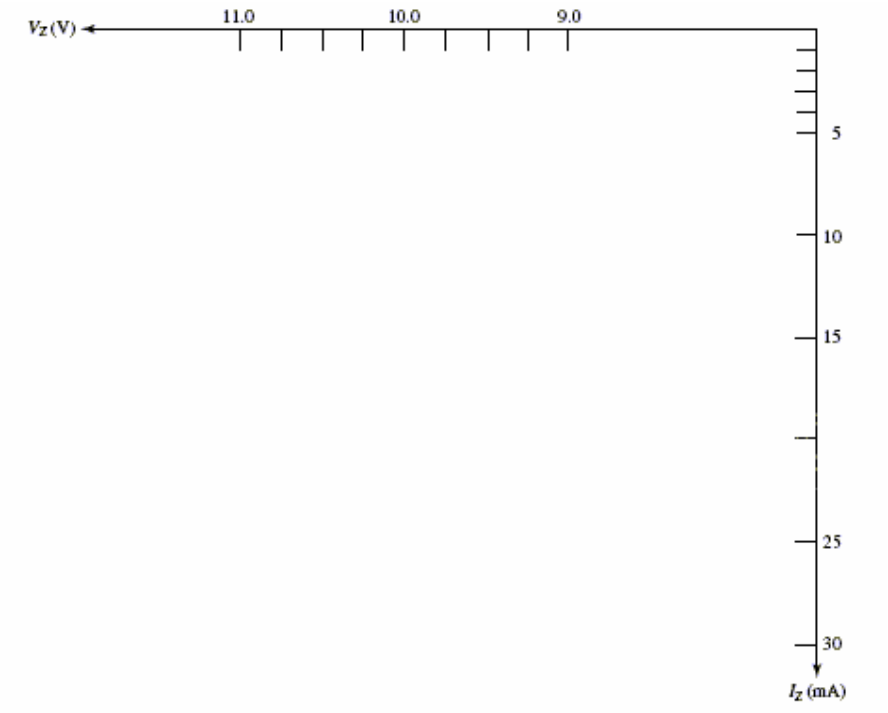


Fig.8: Zener Reverse Operating Curve.

20. Determine the internal DC resistance R_Z of your zener diode by taking the change in zener voltage, V_Z, divided by the corresponding change in current, I_Z.

QUESTIONS & PROBLEMS:

1. Refer to your graphs in Figure 4. Compare the forward characteristics of the two diodes. Explain why they are so similar (or dissimilar).

2. Refer to your results in Step 16. Was the reverse current in the range that you expected? What would happen to the reverse current if the diode was heated to 50°C? Explain your reasoning.

3. Refer to your results in Table 3. Explain how you could use these results to calculate the zener impedance of this 1N5240 zener diode.

4. From step (18), what is the difference between this Zener diode and the normal diode you measured previously? Can you tell the difference between a normal diode and a Zener diode by looking to their characteristic charts?

Lab Session 2
Rectifiers and Filters

OBJECTIVES:

After performing this experiment, you should be able to:

- Demonstrate the strengths and weaknesses of the two basic rectifier circuits.
- Draw the output waveforms for the two basic rectifier circuits.
- Demonstrate the effect and benefit of filtering on rectifier circuits.

SUMMARY OF THEORY:

The most popular application of the diode is the *rectification*. Rectification is simply defined as: the conversion of alternating current (AC) to direct current (DC). This almost always involves the use of some devices that conduct in only one direction, so one polarity of an AC signal, which has zero average (DC) level, can be eliminated resulting in net DC component. As we have seen in the previous experiment, this is exactly what a semiconductor diode does. This process can be used to make power supplies, peak detectors, and amplitude modulators.

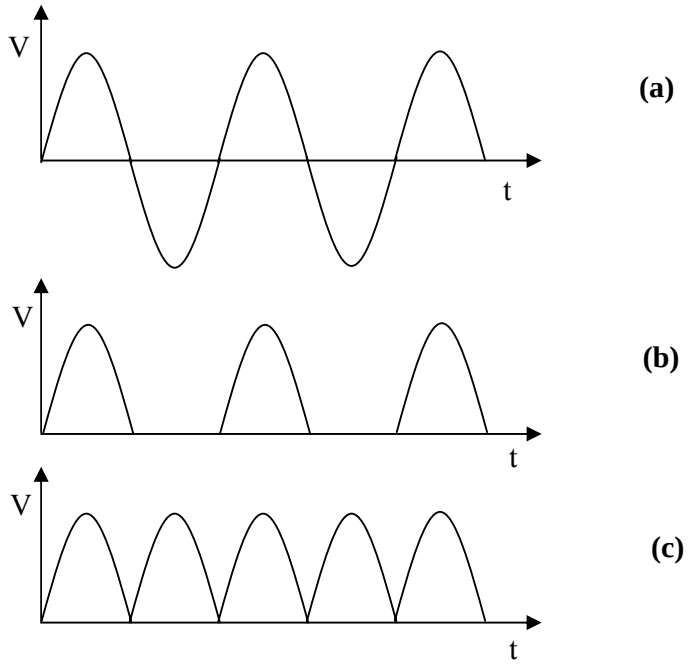


Fig. 1: (a) Input Waveform, (b) Half-Wave Rectified Waveform and
(c) Full-Wave Rectified Waveform

The three basic rectifier configurations are the half-wave, full-wave, and bridge rectifiers. The output of a positive half-wave rectifier is shown in Figure1(b). Figure1(c) shows the output of a positive full-wave, or bridge rectifier.

In any case of rectification the amount of AC voltage mixed with the rectifier's DC output is called *ripple voltage*. In most cases, since "pure" DC is the desired goal, ripple voltage is undesirable or unwanted. If the power levels are not too great, filtering networks that are composed of suitably connected capacitors and inductors may be employed to reduce the amount of ripple in the output voltage. We will be discussing and using only the simple capacitor filter. A measure of the effectiveness of a filter is given by *ripple factor* (r), which is defined as the ratio of the peak-peak value of the AC component to the DC or average value. That is

$$r = \frac{V_r}{V_{avg}} \quad (1)$$

It is desirable and important to make ripple factor as small as possible.

The capacitor filter is the simplest filter circuit with a capacitor in parallel to the load resistor R_L. The capacitor is charged to the peak value of the rectified voltage V_p and begins to discharge through load resistance R_L after the rectified voltage decreases from the peak value. The rate of decrease in the capacitor voltage between charging pulses depends upon the relative values of time constant *RC* and the period of the input voltage. The large time constant results in slower decrease and hence smaller ripple component. The concept of capacitor filter is illustrated in Figure 2. The disadvantages of the capacitor filter lies in: (a) poor regulation and (b) increased ripple at large loads.

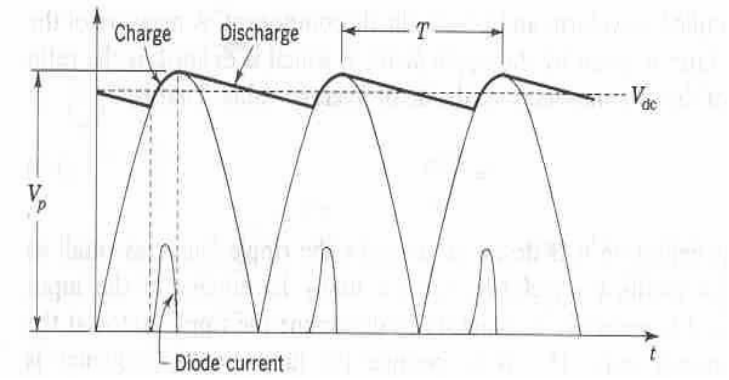


Fig. 2: Output Voltage Capacitor Filter is a DC Voltage and Small Triangular Ripple Voltage.

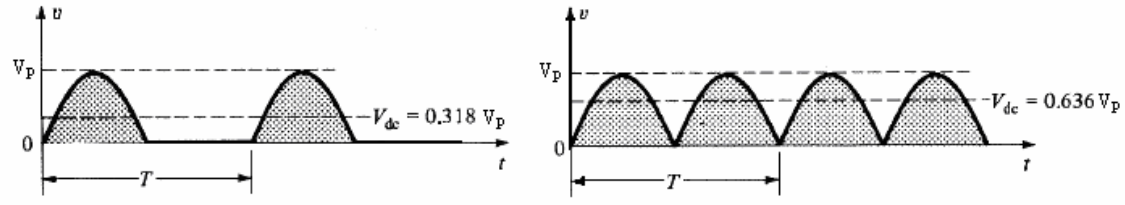
For most power applications, half-wave rectification is insufficient for the task. The harmonic content of the rectifier's output waveform is very large and consequently difficult to filter. Furthermore, AC power source only works to supply power to the load once every half-cycle, meaning that much of its capacity is unused. Half-wave rectification is, however, a very simple way to reduce power to the resistive load.

The half-wave voltage signal of Figure 3(a) normally established by a network with a single diode has an average or equivalent DC voltage level equal to 31.8% of the peak voltage V_p.
That is,

$$V_{avg} = \frac{V_p}{\pi} = 0.318\ V_{peak}\ \text{Volts}\big|_{\text{Half-wave}} \quad (2)$$

The full-wave rectified signal of Figure 3(b) has twice the average or DC level of the half-way signal, or 63:6% of the peak value V_p.
That is,

$$V_{avg} = \frac{2\ V_p}{\pi} = 0.636\ V_{peak}\ \text{Volts}\big|_{\text{Full-wave}} \quad (3)$$



(a) (b)

Fig.3: (a) Half-Wave Rectifier (b) Full-Wave Rectifier.

In rectification systems the peak inverse voltage (PIV) or Zener breakdown voltage parameter must be considered carefully. The PIV voltage is the maximum reverse-bias voltage that a diode voltage can handle before entering the Zener breakdown region. For ideal single-diode half-wave rectification systems, the required PIV level is equal to the peak value of the applied sinusoidal signal. For the four-diode full-wave bridge rectification system, the required PIV level is again the peak value, but for a two-diode center- tapped configuration, it is twice the peak value of the applied signal.

Equipments:

- Dual-Trace Oscilloscope
- Digital Multimeter DMM
- Bread Board
- Resistors
- Electrolytic Capacitors: 10 µF and 100 µF
- 1N4001 Rectifier Diodes

PROCEDURE:

Part 1: Half-Wave Rectification

1. Construct the half-wave rectifier circuit shown in Figure 4. Record the measured value of the resistor. Set the function generator to a 1 KHz, $8 V_{P-P}$ sinusoidal voltage using the oscilloscope.

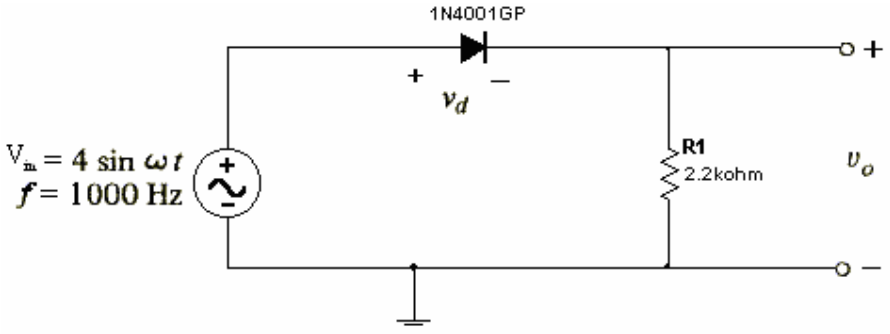


Fig.4: Half-wave Rectifier.

2. Using the oscilloscope with the AC-DC coupling switch in the DC position, obtain the input voltage V_{in} and the output voltage V_O and sketch their waveforms. Before viewing V_O be sure to set the $V_O = 0$ V line using the GND position of the coupling switch.

3. Determine the theoretical output voltage V_O for the circuit of Figure 4 and sketch its waveform for one full cycle using the same sensitivities employed in step (2). Indicate the maximum and minimum values on the output waveform. Compare the results of step (2) and (3)?

4. Set your oscilloscope to X-Y setting. This will display channel-1 (your input) on the horizontal axis and channel-2 (the output of the circuit) on the vertical axis. The X-Y mode will display the transfer characteristic of your circuit. Sketch the transfer characteristic you observed and commit.

5. Measure the DC value of V_O using the DC scale in the DMM.

6. Calculate the DC level of the half-wave rectified signal of step (2). Find the percent difference between the measured value (from step 5) and the calculated value.

7. Reverse the diode of Figure 4 and sketch the output waveform obtained using the oscilloscope. Be sure the coupling switch is in the DC position and the $V_O = 0$ V line is preset using the GND position.

8. Measure and calculate the DC level of the resulting waveform. Insert the proper sign for the polarity of V_{avg} as defined by Figure 4.

Part 2: Half-Wave Rectification (continued)

9. Construct the circuit of Figure 5. Record the measured value of the resistor R_1.

This circuit is another configuration of half-wave rectifier. In the positive half cycle, the diode will be reverse bias (open circuit) and V_O will equal the input voltage $V_{in}(t)$. In the negative half cycle, the diode will conduct (short circuit) and V_O will be near the zero volt.

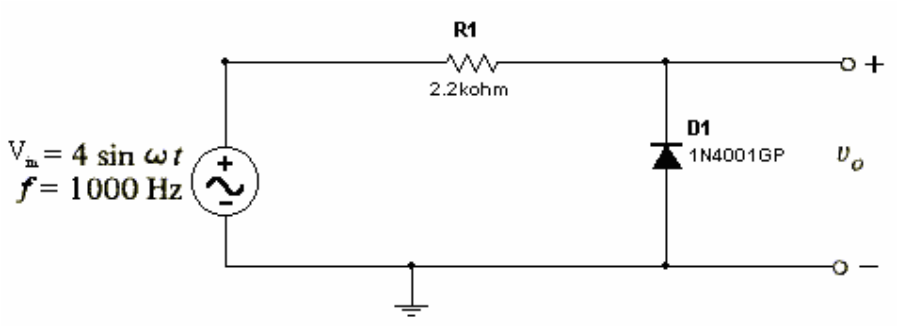


Fig.5: Half-Wave Rectification

10. Repeat steps (2) and (3) for Figure 5.

11. What is the most noticeable difference between the waveform of output voltage V_O obtained in part 2 and that obtained in step (2).

12. Measure the DC value of V_O using the DC scale in the DMM.

13. Calculate the DC level of the output waveform V_O using the following equation:

$$V_{avg} = \frac{V_p}{\pi} - V_\gamma/2 \text{ volts} \qquad (4)$$

Where:

V_p : The peak value of the output voltage.

V_γ : The threshold voltage of the diode.

Part 3: Full-Wave Rectification

14. Construct the circuit shown in Figure 6. Sketch the input and output waveforms. Then, measure the DC load voltage using DMM.

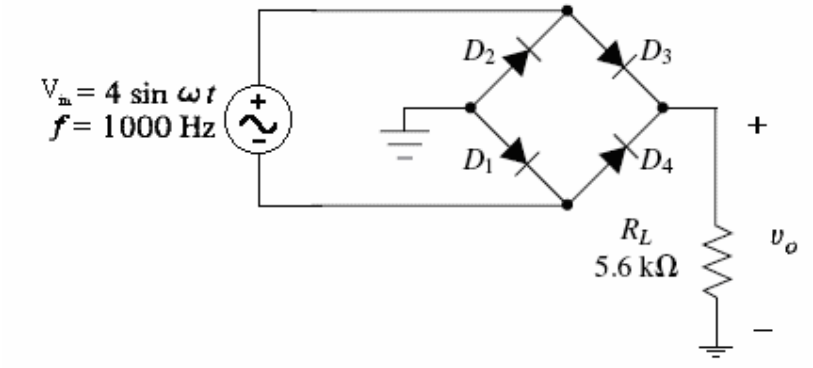


Fig.6: Bridge Rectifier.

Part 4: Rectifier Filtering

As you have seen in the previous parts of this experiment, the output from a rectifier is a pulsating DC voltage. The filter in a linear power supply is designed to reduce the variations in this DC voltage. As you will see shortly, the value of the filter capacitor determines how effective the filter is. No filter is perfect, however, so the variations in the DC voltage are never completely eliminated. The remaining variations in the DC voltage are referred to as the *ripple voltage* (V_r).

15. Add a 1 μF capacitor in parallel with the bridge rectifier load as shown in Figure 7. Use the DMM to measure V_O, and record this value.

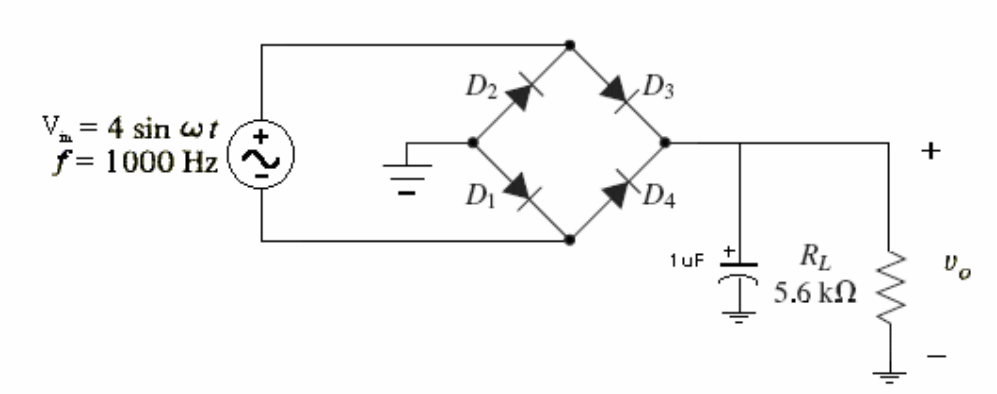


Fig.7: Filtered Bridge Rectifier

Note: It is extremely important to observe proper polarity when working with electrolytic capacitors. If installed backwards, they will fail and may explode.

16. Use the oscilloscope to observe and measure the ripple voltage. (*Note:* The Channel 1 input must be AC coupled to measure the ripple voltage.) Draw the ripple waveform, and record its measured peak-to-peak value.

17. Change the filter capacitor from 1 μF to 10 μF. Power up, and repeat Steps (15) and (16). Draw the ripple voltage waveform, and record its measured peak-to-peak value.

QUESTIONS & PROBLEMS:

1. Use the appropriate relationships to calculate V_O for each circuit. Compare these values with your results in Steps (2,) (10), and (14). Explain any differences between the measured and the calculated values.

2. Using the results of step (2), calculate the peak values of the current i(t) and sketch its waveform.

3. At part (2), you used eq(4) to calculate the DC level of the output waveform V_O. Derive this equation.

4. Refer to Figure 6. Explain how you would modify this circuit to obtain a negative load voltage.

5. Refer to your answer to Question 4. What precaution would be required when adding a filter capacitor to this circuit?

Lab Session 3
Clippers, Clampers, and Voltage Multipliers

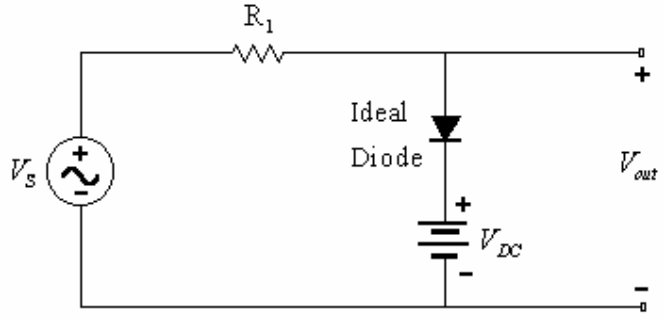
OBJECTIVES:

After performing this experiment, you should be able to:

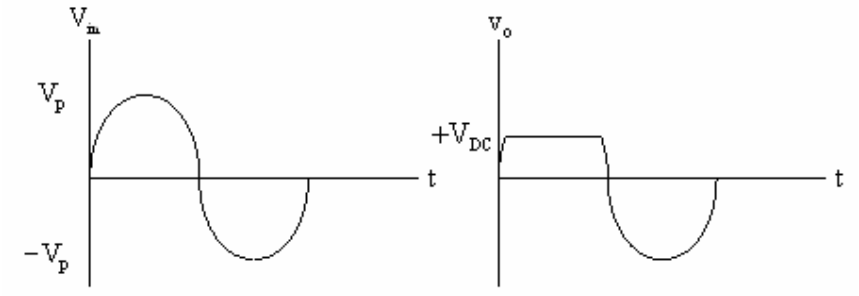
- Demonstrate the operation of the shunt clipper circuit.
- Demonstrate the operation of the diode clamper circuit.
- Demonstrate the operation of a half-wave voltage multiplier.

SUMMARY OF THEORY:

The primary function of clippers is to "clip" away a portion of an applied alternating signal. The process is typically performed by a resistor-diode combination. DC batteries are also used to provide additional shifts or "cuts" of the applied voltage. The half-wave rectifier is a simple *series* clipper. It "clips" either the positive or the negative alternation of its input waveform, depending on the polarity of the diode. Since we examined series clipper operation in the rectifier experiment, we will focus on the *shunt* clipper in this experiment.



(a)



(b)

Fig.1: (a) Clipping Circuit (b) Input and Output Waveforms.

A typical clipper circuit is shown in Figure 1(a). In this circuit the output voltage can never be greater than the value of V_{DC}. The ideal diode becomes forward biased at V_S equal to V_{DC} and this ties the output directly to the V_{DC} supply as shown in Figure1(b). Often in the development of electronic circuits it is required that voltages be limited in some manner to avoid circuit damage. Furthermore, the limiting or clipping of voltages can be very useful in the development of wave-shaping circuits.

The *clamper* is a diode circuit used to change the *DC reference* of a waveform *without significantly altering the shape of that waveform.* The *positive* clamper shifts its input waveform in the positive direction; the *negative* clamper shifts it in the negative direction. The negative clamper is identical to the positive clamper except for the polarity of the diode and capacitor. Clampers are easily distinguished from clippers in that they include a capacitive element. A typical clamper as shown in Figure 2(a) includes a capacitor, diode, and resistor with some also having a DC battery. This circuit works by allowing the capacitor to charge up and act like a battery. This is the voltage across the capacitor depends on the input waveform, the output maximum (or the minimum depending on the orientation of the diode) will be clamped to a fixed reference point. The only design constraint is that $2\pi RC$ be five times larger than the period of the input waveform.
Observe that the output voltage is simply the input voltage shifted by the value of steady state offset (V_{DC}) as shown in Figure 2(b).

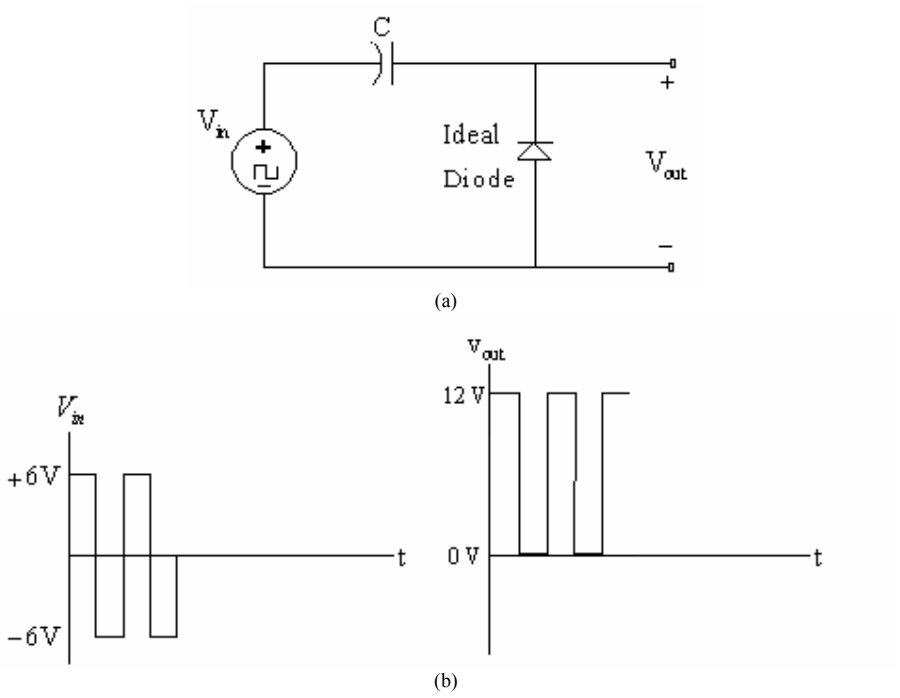


Fig.2: (a) Clamping Circuit (b) Input and Output Waveforms

A *voltage multiplier* is a diode circuit used to provide a DC output that is a specified multiple of the peak value of its input signal voltage. For example, the DC output from a voltage *doubler* is approximately two times its peak input voltage. The voltage *tripler* provides a DC output that is approximately three times its peak input voltage, and so on. There is a slight voltage across each diode in the multiplier circuit, so the output voltage cannot truly reach the design multiple of the peak input voltage. In this experiment, we will investigate a simple half-wave voltage doubler as shown in Figure 3.

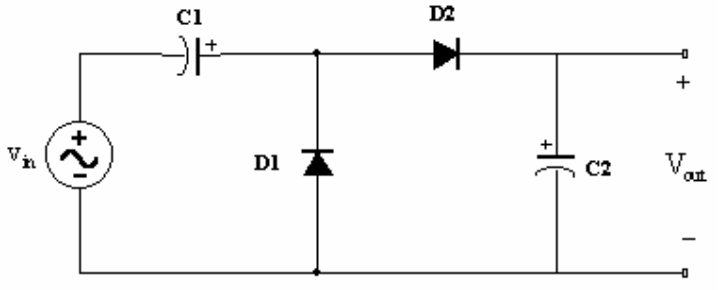


Fig.3: Half-Wave Voltage Doubler

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Equipments:

- Dual-trace oscilloscope
- Function generator
- Digital Multimeter (DMM)
- Breadboard
- Resistors
- Capacitors
- 1N4001 Diodes

PROCEDURE:

Part 1: The Shunt Clipper

1. Construct the circuit shown in Figure 4. Connect a 2 KHz, 10 V_{p-p} sine wave to the input and use the oscilloscope to observe the input and output signals.

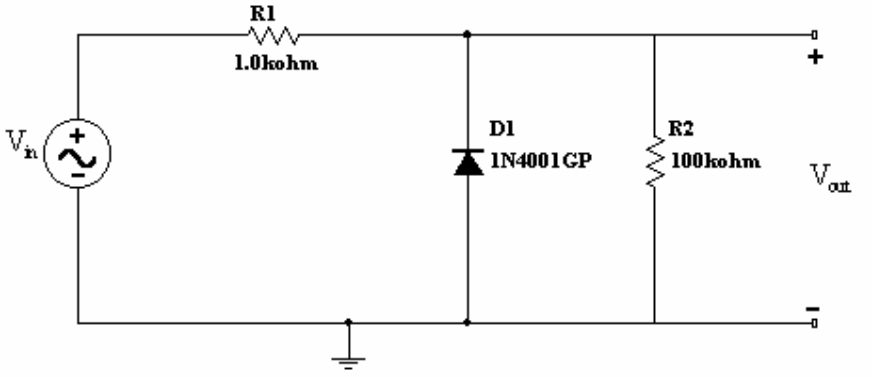


Fig.4: A shunt Clipper

2. Sketch the input and output waveforms.

3. Reverse the direction of D_1 and repeat Step (2).

Part 2: The Shunt Clipper with a DC Battery

4. Construct the clipping circuit shown in Figure 5. Record the measured value of the resistor. Note that the input signal is 10 V_{p-p} sine wave at a frequency of 1KHz.

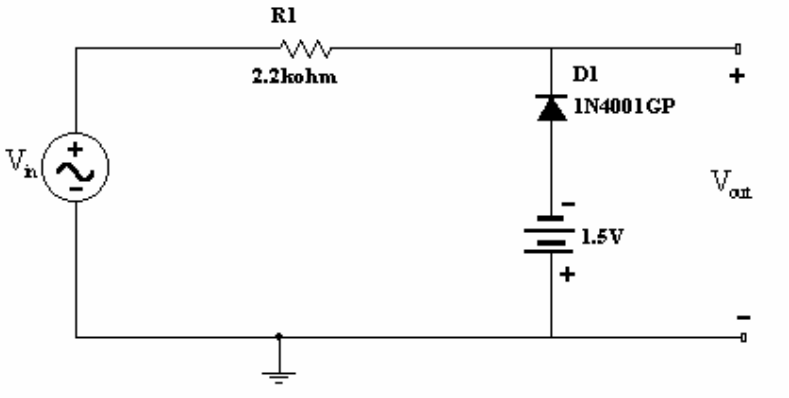


Fig.5: Clipping Circuit

5. Using the oscilloscope with the AC-DC coupling switch in the DC position, obtain the input voltage and the output voltage V_{out} and sketch their waveforms. Before viewing V_{out} be sure to set the V_{out} = 0 V line using the GND position of the coupling switch.

6. Determine the theoretical output voltage V_{out} for the circuit of Figure 5 and sketch its waveform for one full cycle using the same sensitivities employed in step (5). Indicate the maximum and minimum values on the output waveform. Compare the results of step (5) and (6)?

7. Reverse the polarity of the DC power supply and repeat Step (5).

Part 3: The Double Clipper (Limiter)

8. Construct the clipping circuit shown in Figure 6. Record the measured value of the resistor. Set the function generator to a 1 KHz, 0.8-V_{P-P} sine wave.

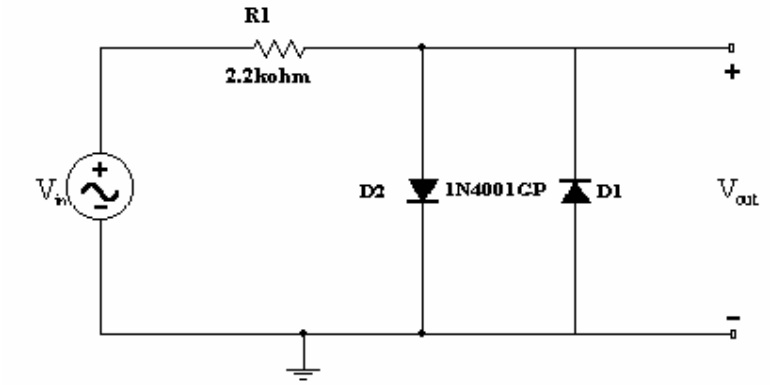


Fig.6: Double Limiter

9. Sketch the input and output waveforms. Can you see the difference between the two waveforms?

10. Increase the amplitude of the input signal to 1V and record the input/output signals. What has happened?

11. Increase the amplitude of the input signal to 4V and record the input/output signals. What has happened?

12. Determine the theoretical output voltage V_{out} for the circuit of Figure 6 and sketch its waveform for one full cycle using the same sensitivities employed in step (11). Indicate the maximum and minimum values on the output waveform. Compare the results of step (11) and (12)?

Part 4: Clampers

13. Construct the circuit shown in Figure 7. Note the direction of the diode and the polarity of the capacitor. Use the oscilloscope to display the input and output signals. Channel 1 is connected to display V_{in}, and Channel 2 is connected to display V_{out}. Both channel inputs should be DC coupled.

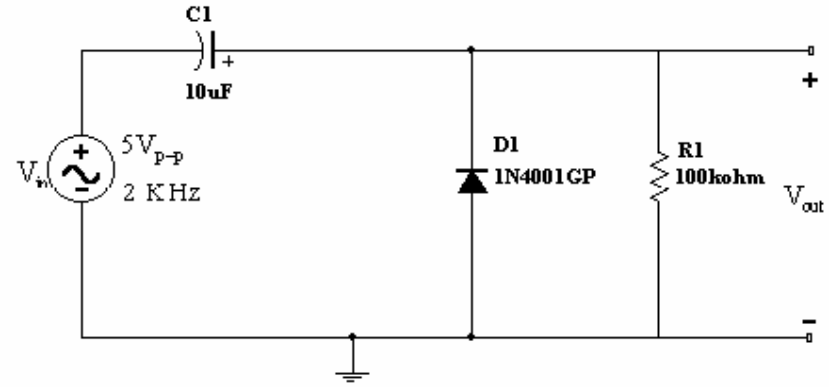


Fig.7: Clamper Circuit

14. Draw the input and output waveforms.

15. Reverse the diode and the capacitor (if it is an electrolytic), and repeat Step (14).

16. There is an easy way to measure the *DC average* (DC offset) of any waveform using the oscilloscope:

    - Set the Channel 2 input to AC coupling. Note the position of the positive (or negative) peak of the waveform.
    - While viewing the waveform, switch the channel input to DC coupling. Note the direction of the shift in the position of the waveform and the number of divisions by which it shifts. If it shifts *up* on the display, it is a *positive* offset. If it shifts *down,* it is a *negative* offset.
    - Multiply the number of divisions by the vertical sensitivity (V/div) setting.
      The result is the DC average (DC offset) of the waveform.

Use this technique on the circuit from Step (13), and record the DC average of the output waveform.

Part 5: Clampers with DC Battery

17. Construct the circuit shown in Figure 8. Connect a 2 KHz, 10 V_{p-p} sine wave to the input and use the oscilloscope to observe the input and output signals.

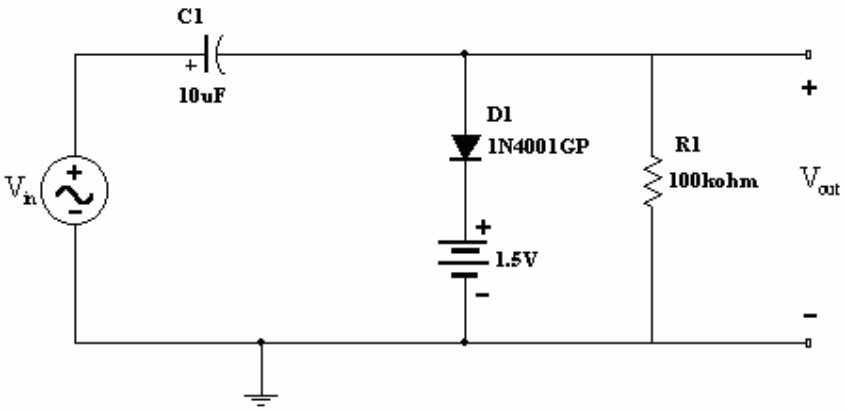


Fig.8: Clamper Circuit with DC Battery

18. Repeat step (14) for Figure 8.

Part 6: Voltage Multipliers

19. Construct the circuit shown in Figure 9. Set the function generator to 1 KHz 10 V_{P-P} square voltage using the oscilloscope.

It is very important that the polarity of the two capacitors be correct.

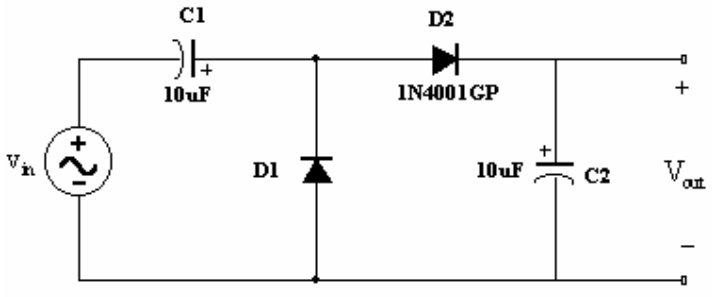


Fig.9: Half-wave Voltage Doubler

20. Use your DMM to measure the DC output voltage (V_{DC}), and record this value. Then, set the oscilloscope to AC coupling, and measure the output ripple voltage. Record this value as well.

QUESTIONS & PROBLEMS:

1. What purpose does R_1 serve in the circuit shown in Figure 4?

2. Refer to Figure 4, was the input waveform clipped at *exactly* 0 V? If not, explain why.

3. Refer to the circuit shown in Figure 6, how can you limit the output at a voltage different than the threshold voltage (V_γ) of the diode, for example at around $\pm$ 5V?

4. Refer to Step (16), there is a relationship between the DC offset of a positive clamper and the *positive* peak value of the output waveform. Based on your results, state and explain this relationship.

5. Refer to the circuit shown in Figure 9, how would you decrease the ripple in the output of the voltage doubler?

6. Refer to the V_{DC} value that you measured in Step (20), was this value *exactly* twice the peak input voltage? If not, explain why.

7. Refer to the circuit shown in Figure 9, this is a *positive* voltage doubler. Sketch a *negative* half-wave voltage doubler.

Lab Session 4
Zener Diode as Voltage Regulator

OBJECTIVES:

After performing this experiment, you should be able to:

- Use an oscilloscope to plot the characteristic curve of a zener diode.
- Study zener diode as voltage regulator against a changing source and a changing load.
- Compute, from measurements, the line and load regulation of a zener regulator circuit.

SUMMARY OF THEORY:

A zener diode is a special type of diode where the diode has been optimized for operation in the reverse or avalanche region. This is completely the opposite of normal diodes or rectifiers where every effort is made to keep the diode from breaking down in the reverse direction. The breakdown voltage can be well controlled and yields a device which exhibits a constant breakdown voltage over a wide range of currents. There is always a series resistor to limit the avalanche current and the zener finds great use as a voltage regulator. In the forward direction, the zener diode acts as a normal forward biased diode as shown in the characteristic curve in Figure 1.

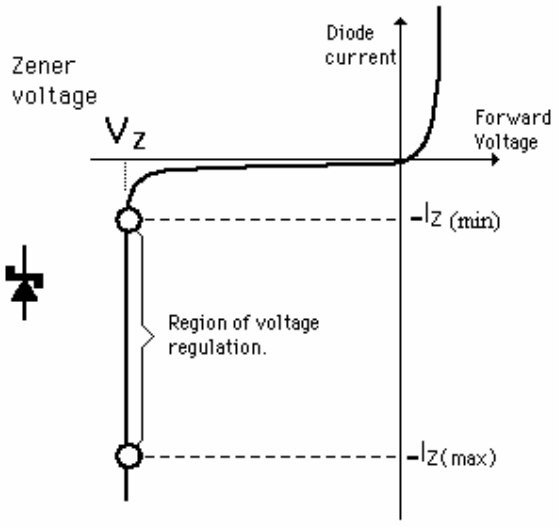


Fig.1: Zener Characteristic

Voltage Regulator: A voltage regulator circuit is required to maintain a constant DC output voltage across the load terminals in spite of the variation:

• Variation in input mains voltage

• Change in the load current

• Change in the temperature

For the purpose of regulating the voltage, zener diode is operated always in reverse biased condition. Here, zener is operated in break down region and it is used to regulate the voltage across a load when there are variations in the supply voltage or load current.

The Figure 2 shows the zener voltage regulator. It consists of a current limiting resistor R_S connected in series with the input voltage V_{in} and zener diode is connected in parallel with the load R_L in reverse biased condition. The output voltage is always selected with a breakdown voltage V_Z of the diode.

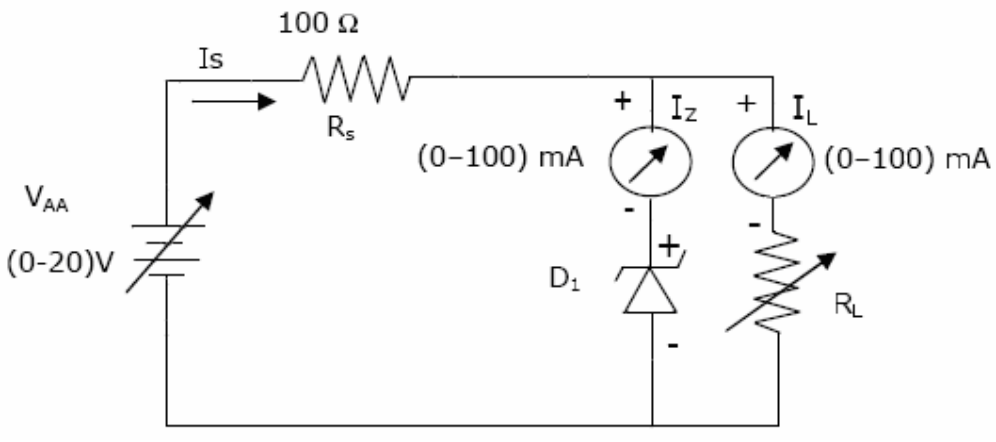


Fig.2: Zener Voltage Regulator

The input source current, $I_S = I_Z + I_L$ …….. (1)

The drop across the series resistance, $V_{R_S} = V_{in} - V_Z$ …… (2)

And current flowing through it, $I_S = (V_{in} - V_Z) / R_S$…….. (3)

From equation (1) and (2), we get, $(V_{in} - V_Z) / R_S = I_Z + I_L$ …… (4)

Regulation with a varying input voltage (line regulation):

It is defined as the change in regulated voltage with respect to variation in line voltage. In this, input voltage varies but load resistance remains constant hence, the load current remains constant. As the input voltage increases, form equation (3) I_S also varies accordingly. Therefore, zener current I_Z will increase. The extra voltage is dropped across R_S. Since, increased I_Z will still have a constant V_Z and V_Z is equal to V_{out}. The output voltage will remain constant.

If there is decrease in V_{in}, I_Z decreases as load current remains constant and voltage drop across R_S is reduced. But even though I_Z may change, V_Z remains constant hence, output voltage remains constant.

Regulation with the varying load (load regulation):

It is defined as change in load voltage with respect to variations in load current. To calculate this regulation, input voltage is constant and output voltage varies due to change in the load resistance value.
Consider output voltage is increased due to increasing in the load current. The left side of the equation (4) is constant as input voltage V_{in} , I_S and R_S is constant. Then as load current changes, the zener current I_Z will also change but in opposite way such that the sum of I_Z and I_L will remain constant. Thus, the load current increases, the zener current decreases and sum remain constant. Form reverse bias characteristics even I_Z changes, V_Z remains same and hence, output voltage remains fairly constant.

Equipments:

- Dual-trace oscilloscope
- Function generator
- Digital Multimeter (DMM)
- Breadboard
- Resistors
- BZX85 Zener Diodes

PROCEDURE:

Part 1: Zener Characteristic Curve

1. Measure and record the values of the resistors listed in Table 1.

Resistor	Listed Value	Measured Value
R_S	220 Ω	
R_1	1 KΩ	
R_L	2.2 KΩ	

Table.1

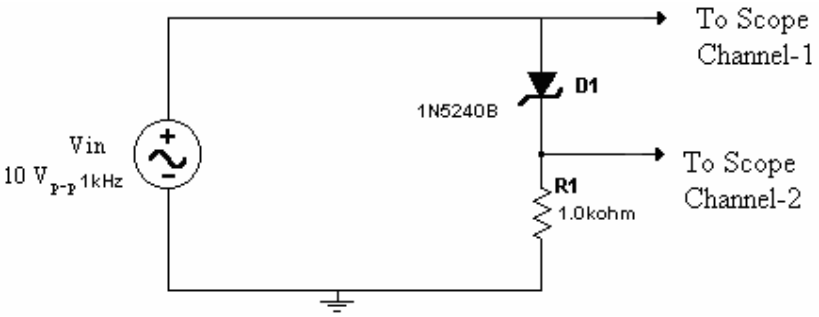


Fig.3: Measuring Zener Characteristic

2. Observe the zener characteristic curve by setting up the circuit shown in Figure 3. Put the oscilloscope in the X-Y mode. Sketch the I-V curve. The 1.0kΩ resistor changes the scope's y-axis into a current axis (1 mA per volt). Label your plot for current and voltage.

Part 2: Line Regulation

3. As we know a common application of zener diodes is in regulators. In this step, you will investigate a zener regulator as the source voltage is varied. Connect the circuit shown in Figure 4.

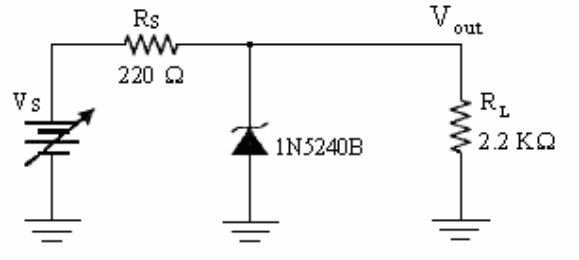


Fig.4: Line Regulation

4. Set V_S to each voltage listed in Table 2 and measure the output (load) voltage, V_{out}.

V_S	V_{out} (measured)	I_L (computed)	V_{R1} (measured)	I_S (computed)	I_Z (computed)
2.0 V					
4.0 V					
6.0 V					
8.0 V					
10.0V					

Tabel.2

5. From the measurements in step (4), complete Table 2. Apply Ohm's law to compute the load current, I_L, for each sitting of the source voltage. Note that I_S is thorough R_S and can be found using ohm's law. Find the zener current, I_Z, by applying Kirchhoff's Current Law (KCL) to the junction at the top of the zener diode.
   What happens to the zener current after the breakdown voltage is reached?

6. Line regulation of a zener regulator is normally expressed as a percentage and is given by the equation:

$$\text{Line regulation} = \frac{\Delta V_{out}}{\Delta V_{in}} \times 100\% \qquad (5)$$

Compute the line regulation expressed as a percentage for the circuit in Figure 4 using the data for the last two rows of Table 2, (Note that V_{in} in the equation is equivalent to V_S in the table).

Part 3: Load Regulation

In this step, you will test the effect of a zener regulator working with a fixed source voltage with a variable load resistance. Often, the load is an active circuit (such as a logic circuit) in which the current changes because of varying conditions .We will simulate this behavior with a variable load resistor.

7. Construct the circuit shown in Figure 5. Set the power supply to a fixed + 6 V output and set the load resistor (R_L) to1 KΩ .

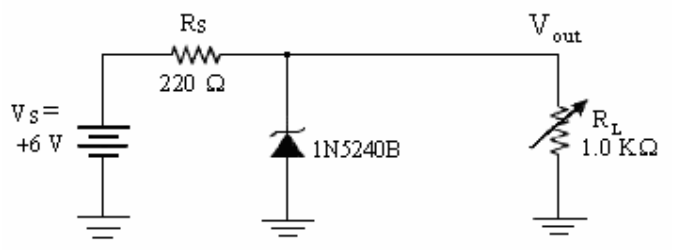


Fig.5: Load Regulation

8. With the load resistor (R_L) set to 1 KΩ (maximum), measure the load voltage (V_{out}) and record the voltage in Table 3. Compute the other parameters listed on the first row as before.

9. Set the load resistor (R_L) to each value listed in Table 3 and repeat step (8).

10. From the data in Table 3, plot the output voltage as a function of load resistance. Choose a reasonable scale factor for each axis and add labels to the plot.

R_L	V_{out} (measured)	I_L (computed)	V_{RS} (measured)	I_S (computed)	I_Z (computed)
1.0 KΩ					
620 Ω					
470 Ω					
270 Ω					
100Ω					

Table.3

From your results, what is the smallest load resistor can be used and still maintain regulation? (Use 1 KΩ potentiometer).

11. Load regulation of a zener regulator, expressed as a percentage, is given by the equation:

$$\text{Load regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\% \qquad (6)$$

Compute the load regulation for the circuit in Figure 5. (Assume V_{out} for the 1.0 KΩ resistor = V_{NL} and V_{out} for the 100 Ω resistor represents V_{FL}).
Note that: no load voltage 'V_{NL}' for maximum load resistance value and full load voltage 'V_{FL}' for minimum load resistance value.

12. Modify the regulator circuit by adding a second zener diode as shown in Figure 6 and changing the source to a 15 V_{p-p} sine wave at 1.0 KHz. Set the 1 KΩ potentiometer to its maximum resistance. Sketch the output waveform and label voltage and time on your sketch.

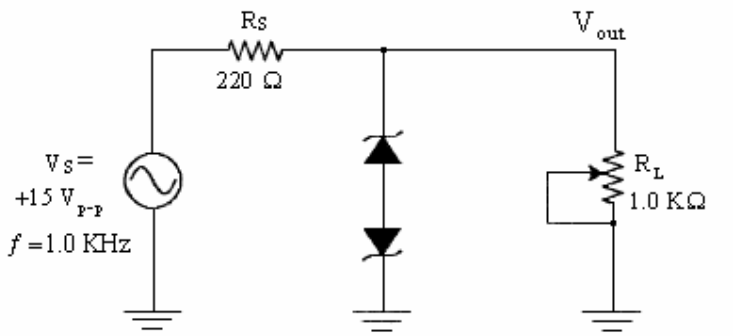


Fig.6: Modified Zener Voltage Regulator

QUESTIONS & PROBLEMS:

1. Observe the characteristic curve obtained for a zener from step (2).

   (a) What portion of the curve is approximated by an open circuit?

   (b) What portion of the curve is approximated by a short circuit?

2. From the data in Table 2, compute the AC resistance of the zener diode when the source voltage changed from 8.0 V to 10.0 V.

3. From the data in Table 3, sketch the Zener Voltage vs Load. Check out any anomalies and comment.

Lab Session 5
BJT Characteristics and DC Biasing

OBJECTIVES:

After performing this experiment, you should be able to:

- Determine the transistor type (NPN, PNP), terminals, and material using a digital multimeter (DMM).
- Determine the parameters for the small signal transistor model of a Bipolar Junction Transistor (BJT) and use these parameters to plot the DC load line.
- Investigate the operation of the two types of Bipolar Junction Transistor.

SUMMERY OF THEORY:

A bipolar junction transistor (BJT) is a three-terminal semiconductor device, made of either silicon (Si) or germanium (Ge). Their structure consists of two layers of n-type material separated by a layer of p-type material (NPN) or of two layers of p-material separated by a layer of n-material (PNP). In either case, the center layer forms the base of the transistor, while the external layers form the collector and the emitter of the transistor. It is the structure that determines the polarities of any voltages applied and the direction of the electron or conventional current flow. With regard to the latter, the arrow at the emitter terminal of the transistor symbol for either type of transistor points in the direction of conventional current flow and thus provides a useful reference as shown in Figure 1. One part of this experiment will demonstrate how you can determine the type of transistor, its material, and identify its three terminals.

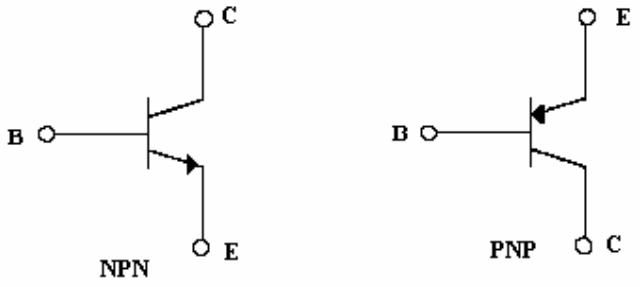


Fig.1: Transistor Symbols

A bipolar junction transistor (BJT) is very versatile. It can be used in many ways, as an amplifier, a switch or an oscillator. Before an AC input signal is applied to the transistor, its DC operating conditions need to be set.

When looking at the curved face of the typical package of the BJT transistor as shown in Figure 2, the emitter (E) is on the right, the base (B) is in the middle and the collector (C) is on the left side of the package.

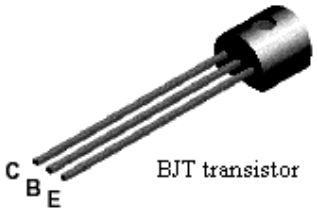


Fig.2: Typical Package of the BJT Transistor

There are three regions of operation for the transistor: Active Region, Saturation Region and Cutoff Region. To bias a BJT transistor for operation in the active region, the base-emitter junction must be forward biased and the collector-base junction reverse biased. Thus, in the active region, current will flow through the collector and will be related to the base current by:

$$I_C = \beta\ I_B \tag{1}$$

Where:

I_C : The collector current,

I_B : The base current,

β : The DC current gain.

The active region is the desired region of operation for a linear amplifier.

If the collector voltage falls below the base voltage by an amount that exceeds the threshold voltage of that junction, the collector-base junction will become forward biased and the transistor will enter the saturation region. . Transistor switching circuits are generally driven into saturation for the ON state. However, for application requiring rapid switching the distance driven into saturation must be limited to prevent long charge storage time in order to reduce switching time.

In addition to the active and saturation regions, the transistor will enter the cutoff region if both the base-emitter and base-collector junctions become reverse biased. In this case, all terminal currents are extremely small and the transistor is said to be off. Switching circuits are driven into cutoff when the desired state of the switch is OPEN.

In order to use a transistor in an amplifying circuit it has to be biased. In other words, a Q-point has to be set in order to place the device in the active region of operation. There are several methods which can be used to bias a transistor. Figures 3 and 4 demonstrate two possibilities.

The first scheme (Figure 3) is called a fixed bias scheme. In a fixed biasing the base current is set through a base resistor and the emitter of the transistor is grounded. This scheme is not used in practice since the Q-point depends very strongly on β.

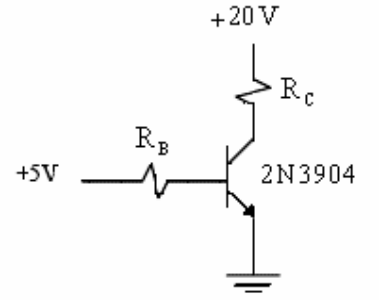


Fig.3: Fixed Biasing Scheme.

A second possibility, which is commonly used, is the self biasing scheme. Here the base voltage is set through a voltage divider and the emitter is tied to ground through a resistor. If designed correctly, this scheme is relatively independent of β.

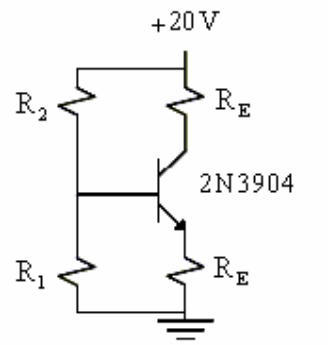


Fig.4: Self-Biasing Voltage Divider Scheme.

PreLab:

Read the specification sheet for the 2N3904 NPN BJT transistor and determine the typical and maximum values for each parameter listed in Table 2.

PROCEDURE:

Pert 1: Checking Transistors

It is often necessary to perform a quick check on a transistor to determine the transistor's type, terminals, material and if it is working. Bipolar transistors are either NPN or PNP depending on the arrangement of materials as in Figure 5.

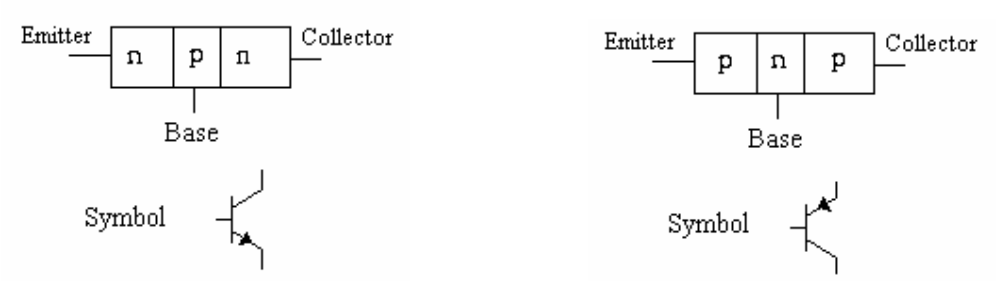


Fig.5: Arrangement of Transistor's Materials Depending on its Type

For purposes of quick testing only, a transistor can be thought of as two back to back diodes as in Figure 6 and hence the following procedure will determine the type, terminals, and material of a transistor and it can be tested in the same manner as a diode. The procedure will utilize the diode testing scale found on many modern multimeters. If no such scale is available, the resistance scales of the meter may be used.

Fig.6: Simple Transistor Model for Testing Purpose

1. Label the transistor terminals of Figure 7 as 1, 2, and 3.
2. Set the selector switch of the millimeter to the diode scale.
3. Connect the positive lead of the meter to terminal 1 and the negative lead to terminal 2. Record your reading in Table 1.
4. Reverse the leads and record your reading.

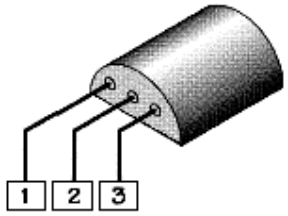


Fig.7: Determination of the Identities of BJT Leads

5. Repeat steps (3) and (4) using the other terminal to complete Table 1.

Step	Mate leads connected to BJT		Diode check reading	
	Positive	Negative	NPN	PNP
1.	1	2		
2.	2	1		
3.	1	3		
4.	3	1		
5.	2	3		
6.	3	2		

Table 1: Testing Transistor

Part 2: Determining Transistor Parameters and The DC Load Line

1. Connect the circuit as shown in Figure 8 using NPN transistor. Switch on the power supply.

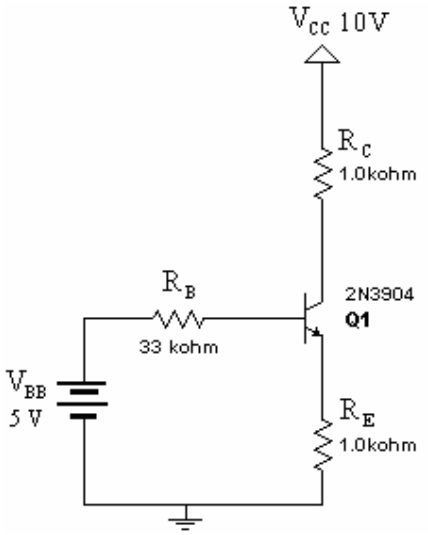


Fig.8: Biasing of NPN Transistor

2. Using the DMM: measure the collector, base and emitter voltages with respect to ground and measure the collector, base and emitter currents. Recording these values in the Table 2.

Parameter	Measured	Calculated	Percentage error %
V_C			
V_B			
V_E			
I_{CQ}			
I_{BQ}			
I_{EQ}			
β_{DC}			
V_{CEQ}			
V_{BEQ}			

Table 2: Transistor Parameters

3. Determine the DC current gain or beta (ß) and the parameter (α) for this transistor so that:

$$\beta_{DC} = \frac{I_{CQ}}{I_{BQ}} \quad (2)$$

$$\alpha = \frac{\beta}{\beta + 1} \quad (3)$$

4. Measure the collector-emitter voltage V_{CE} and the base-emitter voltage V_{BE}. Record these values in Table 2.

5. Determine the saturation ($I_{C(short)}$) and cutoff ($V_{CE(off)}$) points on the DC load line for this circuit using the following equations:

$$I_{C(short)} = \frac{V_{CC}}{R_C + R_E} \quad (4)$$

$$V_{CE(off)} = V_{CC} \quad (5)$$

6. Plot the DC load line using the calculated values of step (5) as end points of the DC load line. Locate the Q point based on the measured values of I_{CQ} and V_{CEQ}.

7. Connect the circuit as shown in Figure 9 using PNP transistor. Switch on the power supply.

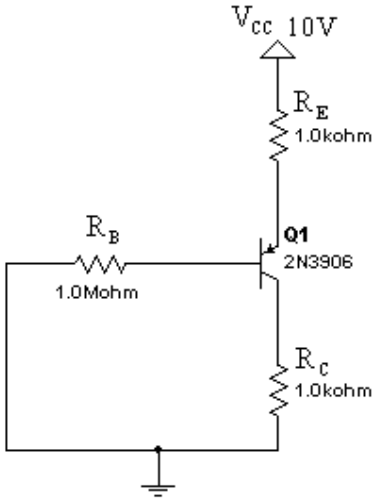


Fig.9: Biasing of PNP Transistor

8. Repeat the steps from (2) to (5) for Figure 9. Tabulate your records.

Part 3: Transistor Switch

9. Build the following circuit shown in Figure 10 using the NPN transistor. Be sure to include the current limiting resistor R_C in series with the Light Emitting Diode (LED) or it may be damaged.

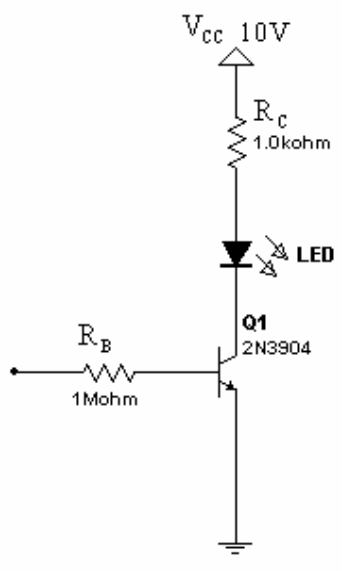


Fig.10: Transistor as a Switch

10. Make sure that one end of R_B is connected to ground as shown in Figure10. Measure and record the voltages at the Base (V_B), Emitter (V_E), and Collector (V_C). What do you observe?

11. Connect the Base resistor (R_B) to +10 V instead of ground. What do you observe?

12. For this configuration measure the Base (V_B), Emitter (V_E) and Collector (V_C) voltages. What mode of operation is the transistor in? Explain.

Part 4: Transistor Amplifier

13. Build the following circuit shown in Figure 11 using the NPN transistor.

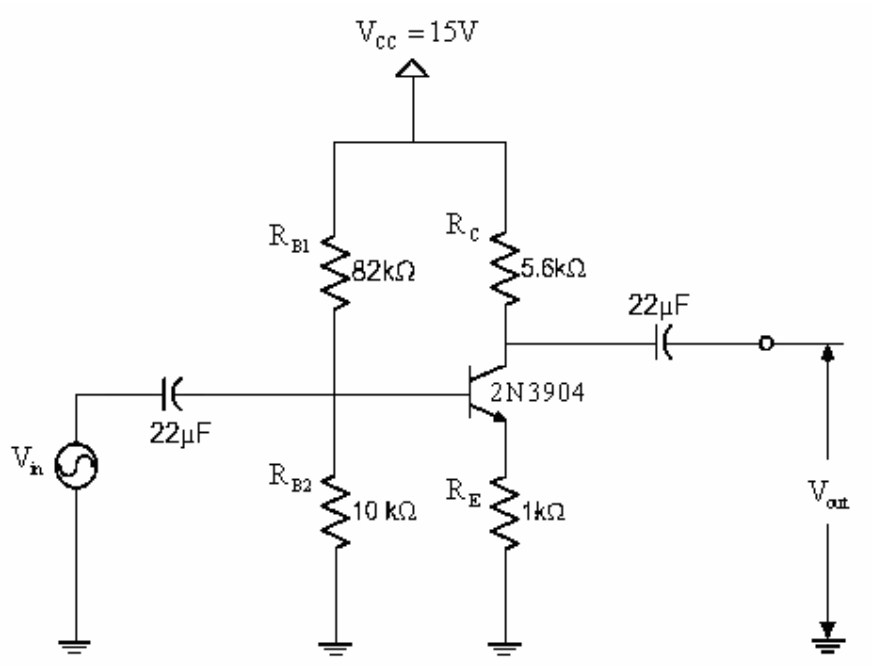


Fig.11: Transistor Amplifier

14. First determine the DC operating point of this circuit. Disconnect the input signal (function generator). Measure and record the DC voltages at the Base (V_B), Emitter (V_E) and Collector (V_C).

15. Connect the input signal. Use the function generator to generate a sinusoidal signal with 0.5 Volt amplitude and 1 kHz frequency. Use the oscilloscope to observe the input and output signals.

16. Sketch the input and output waveforms, show the phase of both signals with respect to each other.

17. Determine the voltage gain:

$$A_V = \frac{V_{out}}{V_{in}} \qquad (6)$$

By measuring the peak amplitudes of input and output voltages.

18. Increase the input signal voltage amplitude until you observe a significant change in the shape of the output waveform. Describe what you observe.

QEUSTIONS & PROBLEMS:

1. Calculate the DC parameters listed in Table 2 of the NPN transistor in the circuit shown in Figure 8. (Show your calculations)

2. Compare the measured values of steps from (2) to (4) with expected values obtained from Question (1), using the value of ß determined in step (3) and a typical base-emitter voltage of 0.7 V. Record these values in Table 2.

3. For Part 3: What is the operating mode of the NPN transistor when connecting:

   (a) R_B to the ground?

   (b) R_B to +10 volt ?

4. For Part 4: Calculate the DC parameters obtained from step (14) and compare them with measured values. What is the operating mode of the NPN transistor?

Lab Session 6
The Common Emitter Amplifier

OBJECTIVES:

After performing this experiment, you should be able to:

- Determine the voltage gain of a common-emitter (CE) amplifier.
- Determine the input impedance of a CE amplifier.
- Determine AC resistance of the emitter (r_e) for a CE amplifier.
- Explain the role of coupling and bypass capacitors in a CE amplifier.
- Demonstrate the effect that a load has on the voltage gain of a CE amplifier.

SUMMARY OF THEORY:

In a common-emitter (CE) amplifier, the input signal is applied between the base and emitter, and the output signal is developed between the collector and emitter. The transistor's *emitter* is common to both the input and output circuit; hence, the term common emitter. The *common-emitter (CE) amplifier* is the most common BJT amplifier configuration. This amplifier has the following characteristics:

1. High voltage gain.
2. High current gain.
3. Moderate input resistance.
4. Moderate output resistance.
5. 180° voltage phase shift between the input and output waveforms.

To make any transistor circuit amplify AC signals, the base-emitter junction must be forward biased, and the base-collector junction must be reverse-biased. The purpose of bias circuits is to establish and maintain the proper DC operating conditions for the transistor. There are several ways to apply DC bias. The simplest method, called base bias or fixed bias, is frequently unsatisfactory due to manufacturing variations between transistors and sensitivity to temperature changes. Base bias is recognized by a single resistor connected from V_{CC} to the transistor base. A much more widely used bias circuit is called voltage-divider bias. Voltage-divider bias is not as sensitive to transistor variations and temperature changes. Voltage-divider bias is shown in Figure1(a).

To analyze any amplifier, start with the DC parameters. The steps to solve for the DC parameters for the CE amplifier with voltage-divider bias illustrated in Figure 1(a) are:

1. Mentally remove capacitors from the circuit since they appear open to DC. This causes the load resistor, R_L, to be removed. Solve for the base voltage, V_B, by applying the voltage divider rule to R_1 and R_2, as illustrated in Figure 1(b).

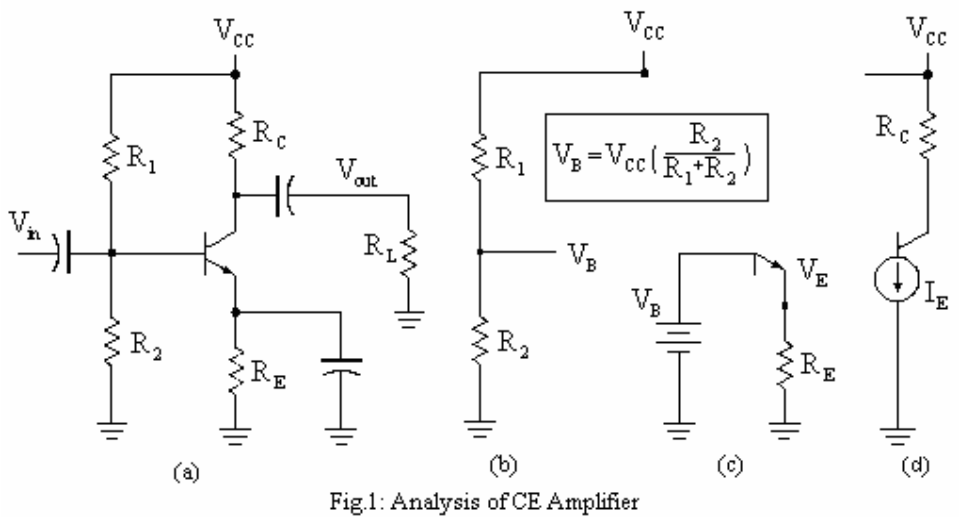


Fig.1: Analysis of CE Amplifier

2. Subtract the 0.7 V forward-bias drop across the base-emitter diode from V_B to obtain the emitter voltage, V_E, as illustrated in Figure 1(c).
3. The DC current in the emitter circuit is found by applying Ohm's law to R_E. The emitter current, I_E, is approximately equal to the collector current, I_C. The transistor appears to be a current source of approximately I_E into the collector circuit, as shown in Figure 1(d).

The AC parameters for the amplifier can now be analyzed. The AC equivalent circuit is shown in Figure 2. The capacitors appear to be an AC short. For this reason, the AC equivalent circuit does not contain R_E. Using the superposition theorem, V_{CC} is replaced with a short, placing it at AC ground. The analysis steps are:

1. Replace all capacitors with a short and place V_{CC} at AC ground. Compute the AC resistance of the emitter, r_e, from the equation:

$$r_e = \frac{26\ mV}{I_E} \tag{1}$$

2. Compute the amplifier's voltage gain. Voltage gain is the ratio of the output voltage divided by the input voltage. The input voltage is across the AC emitter resistance to ground which, in this case, is r_e. The output voltage is taken across the AC resistance from collector to ground which, in this case, is R_C. For the circuit in Figure 2, the output voltage divided by the input voltage can be written:

With R_E bypassed:
$$|A_V| = \frac{V_{out}}{V_{in}} = \frac{\iota_C R_C}{\iota_e r_e} \cong \frac{R_C}{r_e} \tag{2}$$

With R_E unbypassed:
$$|A_V| = \frac{V_{out}}{V_{in}} = \frac{\iota_C R_C}{\iota_e (r_e + R_E)} \cong \frac{R_C}{R_E} \tag{3}$$

3. Compute the total input resistance seen by the AC signal:

With R_E bypassed: $$R_{in} = R_1 \| R_2 \| \beta r_e \quad (4)$$

With R_E unbypassed: $$R_{in} = R_1 \| R_2 \| \beta (r_e + R_E) \quad (5)$$

4. Compute the total input resistance seen by the AC signal: (Assuming $r_o = \infty$)

$$R_{out} \cong R_C \quad (6)$$

5. Compute the voltage gain from the source to the load:

$$\frac{V_L}{V_S} = \frac{R_{in}}{r_S + R_{in}} A_V \frac{R_L}{R_L + R_{out}} \quad (7)$$

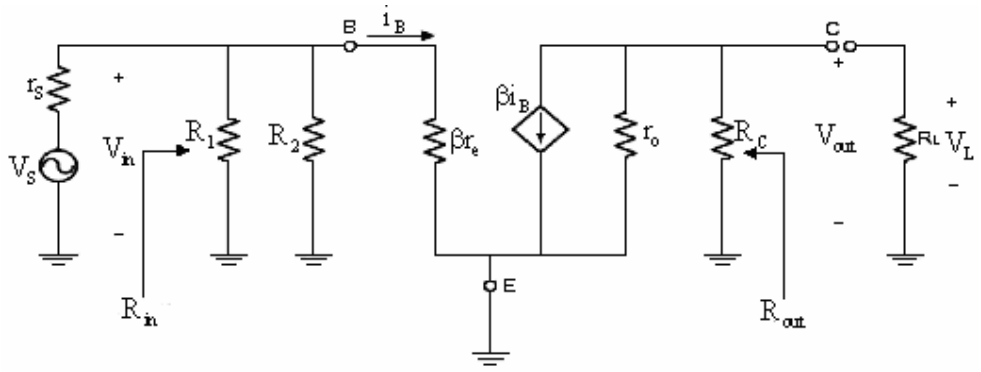


Fig.2: AC Equivalent Circuit of CE Amplifier.

EQUIPMENTS:

- Variable DC Power Supply
- Dual-Trace Oscilloscope
- Breadboard
- Resistors
- Capacitors
- Potentiometer
- 2N3904 NPN Transistor

PROCEDURE:

Part 1: DC Measurements

1. Measure and record the values of the resistors.

2. Construct the amplifier shown in Figure 3. The signal generator should be turned off. Measure and record the DC voltages listed in Table 1.

3. Using the measured resistances and the value of ß determined in step (2), compute the DC parameters listed in Table 1 for the CE amplifier shown in Figure 3. Your measured and computed values should agree within 10%. (Show your calculations)

DC Parameter	Computed Value	Measured Value
V_B		
V_E		
I_E		
V_C		
V_{CE}		
β		

Table.1: DC Parameters of CE Amplifier

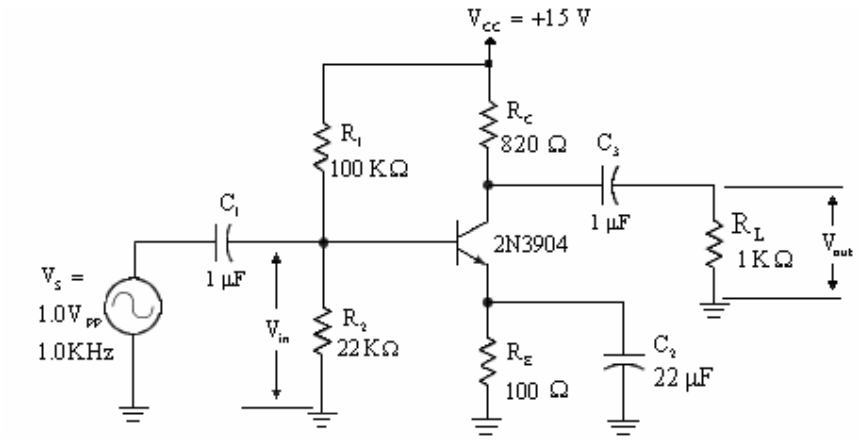


Fig.3: CE Amplifier

Part 1: AC Measurements (Optional)

4. Compute the AC parameters listed in Table 2 (show your calculation). The AC base voltage, v_b, represents the signal input to the amplifier, V_{in}. Multiply the input signal by the computed voltage gain to obtain the output signal.

5. Disconnect the load resistance R_L. Turn on the signal generator and adjust V_S for a 0.1 V_P sine wave at 1.0 kHz. Measure the peak-to peak values of the input and output waveforms, and record these values in Table 2. Use the measured signal voltages to calculate the voltage gain of the amplifier.

6. Carefully sketch the input and output waveforms showing the phase shift between them.

7. Restore the circuit to its original configuration shown in Figure 3. Set R_L to $1k\Omega$, and measure the peak-to peak value of the output waveform. Record your measured and calculated values. Use this measured voltage to calculate the voltage gain from the input to the load V_L/V_{in}. Record it in Table 2.

8. Using the basic laws of voltage division, you can easily determine the input impedance of this amplifier as follows:
   - Insert a 47 $k\Omega$ potentiometer between the signal generator and the input coupling capacitor.
   - Adjust the potentiometer until V_{out} drops to one-half the value noted prior to insert the potentiometer.
   - Power down, and remove the pot from the circuit *without disturbing its setting*.
   - Measure the adjusted resistance of the potentiometer, and record this value in Table 2. This value equals the input impedance of the amplifier.

9. Remove C_2 from the circuit. Measure the AC signal voltage at the transistor's base, emitter, and collector. Measure the voltage gain of the amplifier.

10. With C_2 open (R_E unbypassed): repeat steps (7) and (8). Compare the result values with the calculated values obtained from step (4).

11. To measure the output resistance R_{out} of the CE Amplifier connect a 1 $K\Omega$ potentiometer connected between the output coupling capacitor and ground. Adjust the potentiometer until V_{out} drops to one-half the previous value. Remove the potentiometer and measure its resistance. By the voltage divider role, the resistance of the potentiometer equals the output resistance of the amplifier.

AC Parameter	Computed Value R_E byp. | R_E unbyp.		Measured Value R_E byp. | R_E unbyp.	
$v_b = V_{in}$				
r_e				
A_V				
$v_C = V_{out}$				
R_{in}				
V_L/V_{in}				

Table.2: AC Parameters of CE Amplifier

QUESTIONS & PROBLEMS:

1. Explain a simple test to determine if a transistor is saturated or cut off.

2. Refer to Table 1: How close are your calculated values of the DC parameters to the measured value? Explain any discrepancies.

3. Is the amplifier shown in Figure 3 midpoint biased? Support your answer using values from Step (3).

4. Refer to the waveforms that you drew from Figure 3. Explain why the output signal is 180° out of phase with the input.

5. Refer to Table 2: How close are your calculated value of AC parameters to the measured value? Explain any discrepancies.

6. Refer to Step (7): What happened to the voltage gain of the circuit when the load resistance was connected? Explain why you think this happened.

7. Refer to Step (9): What happened to the voltage gain of the circuit when the bypass capacitor was removed? Explain why you think this happened.

Lab Session 7
The Common Collector Amplifier

OBJECTIVES:

After performing this experiment, you should be able to:

- Compute and measure the DC parameters of Common Collector (CC) Amplifier.
- Compute and measure the AC parameters of (CC) amplifier including the voltage gain, input resistance and power gain.
- Test the effect of different load resistors on the AC parameters of the (CC) amplifier.

SUMMARY OF THEORY:

The *common-collector (CC) amplifier* is the second most common BJT amplifier configuration. The common-collector (CC) amplifier (also called the emitter-follower) has the input signal applied to the base and the output signal is taken from the emitter.
This amplifier has the following characteristics:

6. Almost unity voltage gain.
7. High current gain.
8. High input resistance.
9. Low output resistance.
10. 0° voltage phase shift between the input and output waveforms.

Figure 1(a) illustrates a (CC) amplifier using a PNP transistor with voltage-divider bias. Frequently, a (CC) amplifier follows a voltage amplifier. Instead of having separate bias resistor bias may be obtained through a DC path connected from the previous stage as illustrated in Figure 1(b). This technique is common in power amplifiers.

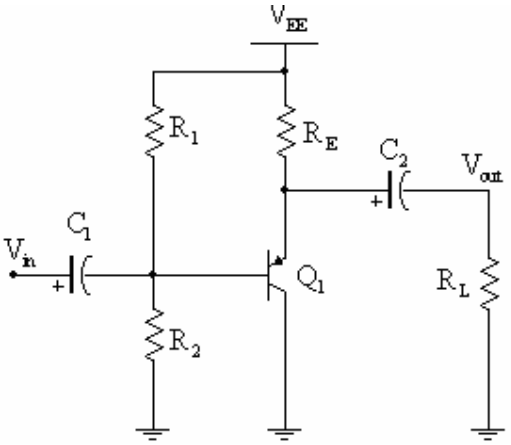
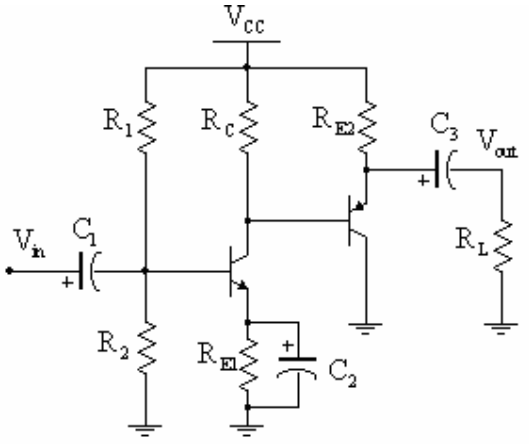


Fig.1: (a) CC with PNP Transistor



(b) CE and CC Amplifiers

Analysis of the amplifier begins with the DC parameters. These procedures are described in Experiment 6 and summarized here for the PNP transistor shown in Figure 1(a).

1. Mentally remove the capacitors from the circuit since they appear open to DC. This causes the load resistor, RL to be removed.
2. Solve for the base voltage. V_B, by applying the voltage-divider rule to R_1 and R_2.
3. Add the 0.7 V forward-bias drop across the base-emitter diode from V_B to obtain the emitter voltage, V_E. (Note that the emitter is at a higher voltage in the PNP case.)
4. The DC current in the emitter circuit is found by applying Ohm's law to R_E. The voltage across the emitter resistor is the difference between the supply voltage (V_{EE}) and V_E. The collector current is nearly equal to the emitter current, and the collector voltage is Zero.

The AC parameters for the amplifier can now be analyzed. The equivalent AC circuit is illustrated in Figure 2. The analysis steps are:

1. Replace all capacitors with a short. Compute the AC resistance of the emitter, r_e, from the equation:

$$r_e = \frac{25\ \text{mV}}{I_E} \tag{1}$$

2. Compute the amplifier's voltage gain. Voltage gain is the ratio of the output voltage divided by the input voltage. The input voltage is applied across r_e and the AC emitter resistance, whereas the output voltage is taken only across the AC emitter resistance. Thus, the voltage gain is based on the voltage divider equation:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{\imath_e \left(R_E \| R_L \right)}{\imath_e \left(r_e + R_E \| R_L \right)} = \frac{R_E \| R_L}{r_e + R_E \| R_L} \simeq 1 \tag{2}$$

3. Compute the total input resistance seen by the AC signal:

$$R_{in} = R_1 \left\| R_2 \right\| \left\{ \beta \left(r_e + R_E \| R_L \right) \right\} \tag{3}$$

4. Compute the total output resistance seen by the AC signal:

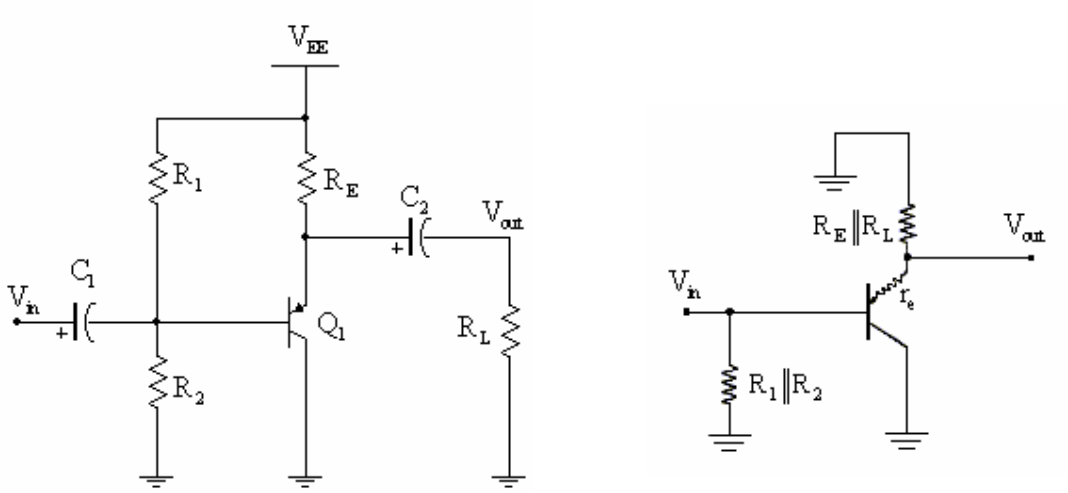
$$R_{out} = R_E \left\| R_L \right\| \left(r_e + \frac{R_1 \| R_2}{\beta} \right) \simeq r_e \tag{4}$$

5. Compute the amplifier's power gain. In this case, we are only interested in the power delivered to the load resistor. The output power is V_{out}^2/R_L. The input power is V_{in}^2/R_{in}. Since the voltage gain is approximately 1, the power gain can be expressed as a ratio of R_{in} to R_L.

$$A_P = \frac{\frac{V_{out}^2}{R_L}}{\frac{V_{in}^2}{R_{in}}} = A_V^2 \left\{ \frac{R_{in}}{R_L} \right\} = \frac{R_{in}}{R_L} \qquad (5)$$

These formulas were derived for the particular (CC) amplifier shown in Figure 2. You should not assume that these equations are valid for other configurations.

One common application of the CC amplifier is as a *buffer*. A buffer is used to compensate for an impedance mismatch between a load and a source. Because the emitter follower has relatively high input impedance and low output impedance, it is commonly used to couple a high-impedance source to a low-impedance load. You will look at this application in this experiment.



(a) (b)

Fig.2: (a) CC Amplifier (b) AC Equivalent Circuit

PROCEDURE:

Part 1: DC Measurements

1. Measure and record the resistance value of the resistors listed in Table 1.

Resistor	Listed Value	Measured Value
R_1	33 KΩ	
R_2	10 KΩ	
R_E	1.0 KΩ	
R_L	1.0 KΩ	

Table.1

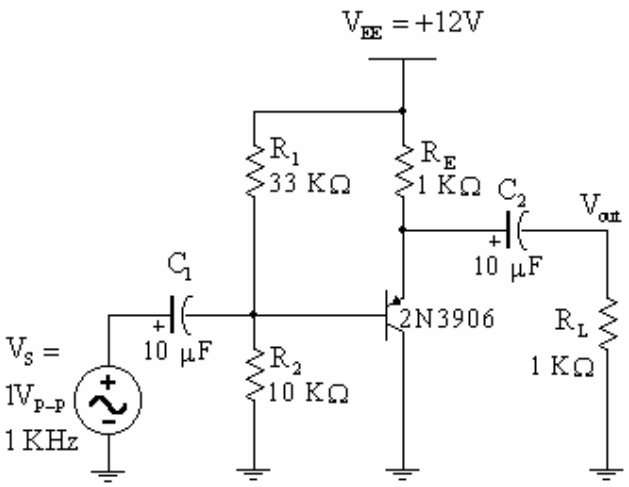


Fig.3: (CC) Amplifier

2. Construct the amplifier shown in Figure 3. The signal generator should be turned off. With the power supply on, measure and record the DC voltages listed in Table 2.

3. Using the measured resistances and the value of ß determined in step (2), compute the DC parameters listed in Table 2 for the (CC) amplifier shown in Figure 3. Your measured and computed values should agree within 10%. (Show your calculations)

DC Parameter	Computed Value	Measured Value
V_B		
V_E		
I_E		
V_C		
β		

Table.2: DC Parameters of CC Amplifier

Part 1: AC Measurements (Optional)

4. Compute the AC parameters listed in Table 3. Assume υ_b is the same as the source voltage, V_S. Use the procedure outlined in the Summary of Theory to compute these parameters. Show your calculations.

AC Parameter	Computed Value	Measured Value
υ_b		
υ_e		
r_e		
A_V		
R_{in}		
R_{out}		
A_P		

Table.3: AC parameters of CC Amplifier

5. Turn on the signal generator and set V_S for 1.0 V_{p-p} at 1.0 KHz. Use the oscilloscope to set the proper voltage and check the frequency. Measure the peak to peak input and output signal voltages, and determine the voltage gain, A_V.

6. With a two-channel oscilloscope, compare the input and output waveforms. What is the phase relationship between V_{in} and V_{out} ?

7. Measure R_{in} using the method employed for the CE amplifier in Experiment6:

   - Insert a 47 KΩ potentiometer between the signal generator and the input coupling capacitor.
   - Connect the oscilloscope and adjust the potentiometer until the output signal displayed on the oscilloscope is exactly half the input voltage.
   - Power down and carefully remove the potentiometer from the circuit without disturbing its setting.

   Measure the resistance of the potentiometer and record this value in Table 3. This value is approximately equal to the amplifier input impedance.

8. To measure the output resistance R_{out} of the (CC) amplifier, connect a 1KΩ potentiometer between the output coupling capacitor and ground. Adjust the potentiometer until V_{out} drops to one half its previous value. Remove the potentiometer and measure its resistance. By the voltage divider rule, this resistance equals the output resistance of the amplifier.

9. Replace R_L with a 10 KΩ variable resistor set to 1.0 KΩ. Connect an oscilloscope probe to the emitter. Raise the signal amplitude until you just begin to observe clipping. If the positive peaks are clipped, you are observing cutoff because the transistor is turned off. If the negative peaks are clipped, this is called saturation clipping because the transistor is fully conducting. What type of clipping is first observed?

10. Vary R_L while observing the output waveform. Describe your observations.

11. To demonstrate the load effect on a common emitter amplifier, connect the circuit shown in Figure 4:

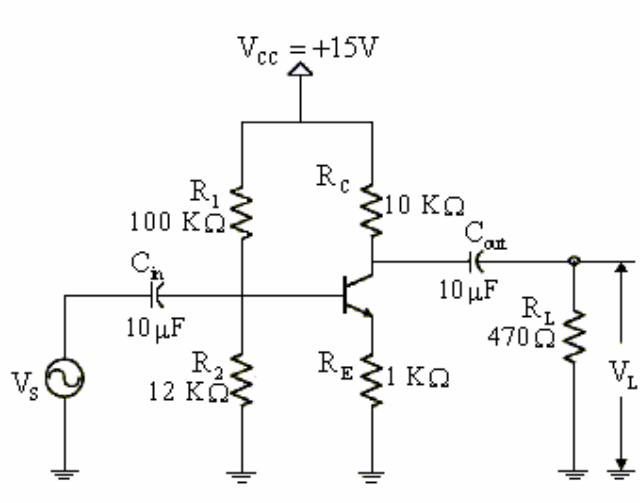


Fig.4: CE Amplifier

12. Set $V_S = 0.1\ V_{p\text{-}p}$ at 10 KHz. Measure and record V_L. Calculate the voltage gain from source to load, V_L / V_S.

13. To demonstrate the use of a common collector amplifier stage to buffer a low impedance load from a high output resistance of the common emitter amplifier, connect the circuit shown in Figure 5:

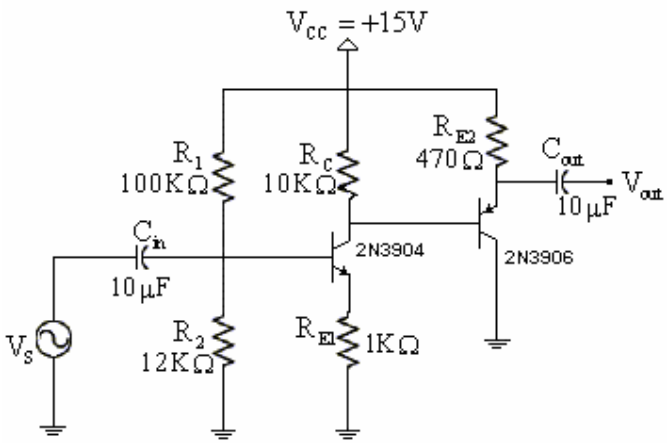


Fig.5: CE and CC Amplifiers

14. Repeat step (12) for the circuit of Figure 5. Set the oscilloscope to the AC coupling.

QUESTIONS & PROBLEMS:

1. In step (6), you observed the phase relationship between the input and output waveforms. Is the phase relationship you observed the same for an NPN circuit? Explain.

2. In step (9), you observed the effect of clipping due to saturation or cutoff of the transistor. The statement was made that if the positive peaks are clipped, you are observing cutoff clipping because the transistor is turned off. Is this statement true if the CC circuit had been constructed with an NPN transistor? Why or why not?

3. The circuit used in this experiment used voltage-divider bias.

   (a) Compared to base bias, what is the advantage?

   (b) What disadvantage does it have?

4. Common-collector amplifiers do not have voltage gain but still provide power gain. Explain.

5. Explain the results of steps (10) and (12). Did the emitter follower stage have a noticeable effect on the voltage gain from source to load, V_L/V_S .

Lab Session 8
JFET Characteristics & DC Biasing

OBJECTIVES:

After performing this experiment, you should be able to:

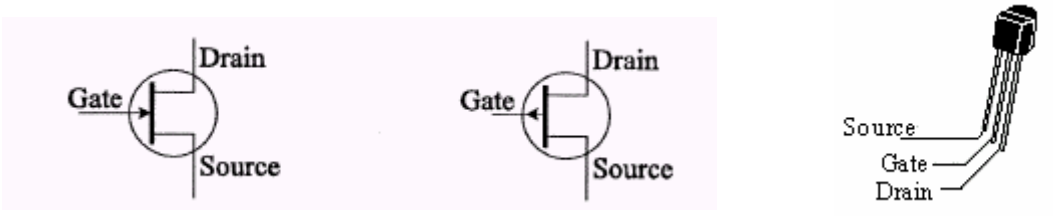
- Measure and graph the drain characteristic curves for a junction field-effect transistor (JFET).
- Measure $V_{GS(off)}$ and I_{DSS} for a JFET.
- Connect a JFET as a two-terminal constant-current source to maintain constant illumination in a LED.

SUMMARY OF THEORY:

The bipolar junction transistor (BJT) uses base current to control collector current. Unlike the BJT, the field-effect transistor (FET) is a voltage-controlled device that uses an electrostatic field to control current. The FET begins with a doped piece of silicon called a channel. On one end of the channel is a terminal called the source and on the other end of the channel is a terminal called the drain. Current in the channel is controlled by a voltage applied to a third terminal called the gate.

Field-effect transistors are classified as either junction-gate (JFET) or insulated-gate (IGFET) devices. The JFET has a reverse-biased diode at the gate whereas the IGFET uses a thin glass-insulting layer. Since the gate circuit of either type of FET draws almost no current, the input resistance is extremely high. Both types have similar AC characteristics but differ in biasing methods.

The gate of a JFET is made of the opposite type of material than the channel, forming a PN junction between the gate and channel. Application of a reverse-bias on this junction decreases the conductivity of the channel, reducing the source-drain current. The gate diode should never be forward-biased. The JFET comes in two forms, n-channel and p-channel. The n-channel is distinguished on drawings by an inward arrow on the gate connection while the p-channel has an outward pointing arrow on the gate as shown in Figure 1. A typical JFET package is shown in Figure 1(c).



(a) (b) (c)

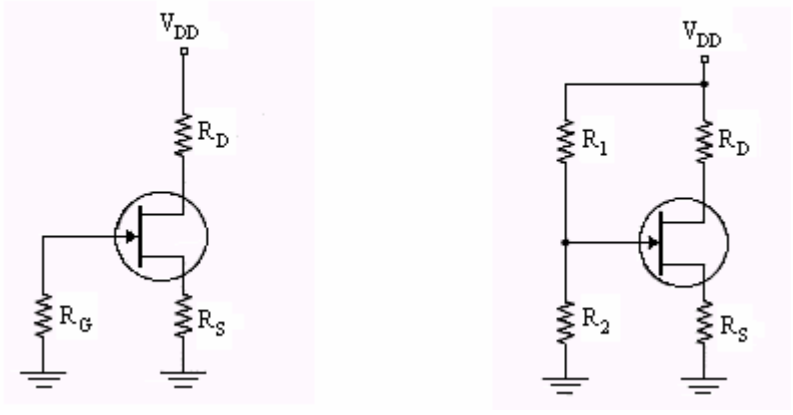
Fig.1: (a) n-Channel JFET (b) p-Channel JFET (c) Typical JFET Package

The characteristic drain curves for a JFET exhibit several important differences from the BJT. In addition to the fact that the JFET is a voltage-controlled device, the JFET is a normally ON device. In other words, a reverse-bias voltage must be applied to the gate-source PN junction in order to close off the channel and prevent drain-source current. When the gate is shorted to the source, there is maximum allowable drain-source current. This current is called I_{DSS} for Drain-Source current with gate shorted. Another important difference is that the JFET exhibits a region on its characteristic curve where drain current is proportional to the drain- source voltage. This region, called the *ohmic region*, has important applications as a voltage- controlled resistance.

A useful specification for estimating the gain of a JFET is called the transconductance, which is abbreviated g_m. Recall that conductance is the reciprocal of resistance. Since the output current is controlled by an input voltage, it is useful to think of any FET as a transconductance amplifier. The transconductance can be found by dividing a small change in the output current by a small change in the input voltage.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \qquad (1)$$

As you know, bias is the application of DC voltages to set up the proper quiescent conditions for circuit operation. A satisfactory bias circuit for a FET depends on its type. With depletion-mode devices, which include all JFETS and some D-MOSFETS, the gate must be reverse biased (or zero biased) with respect to the source. These devices are normally on - they are turned off by applying reverse bias to the gate. Most MOSFETS operate as enhancement mode devices (all E-MOSFETS and some D-MOSFETS) and require bias to turn them on.



(a) (b)

Fig.2: (a) Self -Bias (b) Voltage Divider Bias

Self-bias is the most common type of bias for JFETs and is illustrated in Figure 2(a). The drain current, I_D, is in the source resistor, creating a voltage $V_S = I_D R_S$ at the source terminal. Since the gate is at ground potential (0 V), the gate-source voltage must have the same magnitude but opposite sign to the voltage drop across R_S (by Kirchhoff's voltage law). For an n-channel device, $V_{GS} = -V_S$. This provides the required reverse bias on the gate. Self-bias tends to compensate for different device characteristics between various FETs. For example, if a device with higher transconductance is put in the circuit, the drain current increases along with the voltage drop across R_S. This increased voltage tends to bias the FET off, compensating for the higher transconductance.

An even more stable form of bias combines self-bias with voltage-divider bias as illustrated in Figure 2(b). The voltage-divider connected to the gate biases the gate at some positive voltage. Unlike bipolar transistors, the JFET draws almost no input current, so the divider resistors can be much larger. The source voltage must still be more positive than the gate in order to establish the proper gate-source reverse bias. To accomplish this, the source resistor is made large enough to develop a positive voltage with respect to the gate (much larger than in self-bias). The net result is that transistor variations have less effect on the operating point than self-bias, producing a more stable form of biasing. The drain current is fairly Independent of the transistor; however, the drain-source voltage must be large enough to assure that the transistor is operating in the constant-current region.

PROCEDURE:

1. Measure and record the value of the resistors listed in Table 1. R_1 is used for protection in case the JFET is forward-biased accidentally. R_2 serves as a current-sensing resistor.

Resistor	Listed Value	Measured Value
R_1	10 kΩ	
R_2	100 Ω	

Table.1

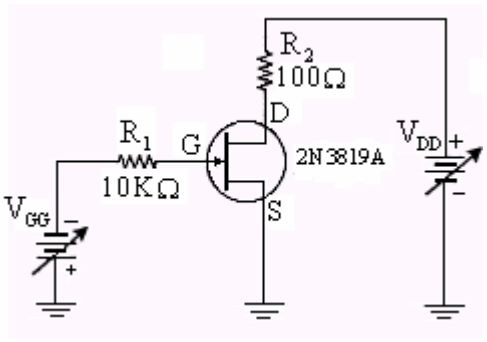


Fig.3: JFET Circuit

2. Construct the circuit shown in Figure 3. Start with V_{GG} and V_{DD} at 0 V. Connect a voltmeter between the drain and source. Keep V_{GG} at 0 V and slowly increase V_{DD} until V_{DS} is 1.0 V. (V_{DS} is the voltage between the transistor's drain and source).

3. With V_{DS} at 1.0 V, measure the voltage across R_2 (V_{R2}). Compute the drain current, I_D, by applying Ohm's law to R_2. Note that the current in R_2 is the same as I_D for the transistor. Use the measured voltage, V_{R2}, and the measured resistance, R_2, to determine I_D. Enter the measured value of V_{R2} and the computed I_D in Table 2 under the columns labeled Gate Voltage = 0 V.

4. Without disturbing the setting of V_{GG}, slowly increase V_{DD} until V_{DS} is 2.0 V. Then measure and record V_{R2} for this setting. Compute I_D as before and enter the measured voltage and computed current in Table 2 under the columns labeled Gate Voltage = 0 V.

	Gate Voltage = 0 V		Gate Voltage = -0.5 V		Gate Voltage = -1.0 V		Gate Voltage = -1.5 V	
V_{DS} (measured)	V_{R2} (measured)	I_D (computed)	V_{R2} (measured)	I_D (computed)	V_{R2} (measured)	I_D (computed)	V_{R2} (measured)	I_D (computed)
1.0 V								
2.0 V								
3.0 V								
4.0 V								
6.0 V								
8.0 V								

Table.2: Data of Drain Characteristics Curves for JFET Transistor

5. Repeat step (4) for each value of V_{DS} listed in Table 2.

6. Adjust V_{GG} for -0.5 V. This applies -0.5 V between the gate and source because there is almost no gate current into the JFET and almost no voltage drop across R_1. Reset V_{DD} until V_{DS} = 1.0 V. Measure V_{R2} and compute I_D as before. Enter the values in Table 2 under the columns labeled Gate Voltage = -0.5 V.

7. Without changing the setting of V_{GG}, adjust V_{DD} for each value of V_{DS} listed in Table 2 as before. Compute the drain current at each setting and enter the voltage and current values in Table 2 under the columns labeled Gate Voltage = -0.5 V.

8. Adjust V_{GG} for -1.0 V. Repeat step (7), entering the data in the columns labeled Gate Voltage = -1.0 V.

9. Adjust V_{GG} for -1.5 V. Reset V_{DD} until V_{DS} = 1.0 V. Repeat step (7), entering the data in the columns labeled Gate Voltage = -1.5 V.

10. The data in Table 2 represent four drain characteristic curves for your JFET. The drain characteristic curve is a graph of V_{DS} versus I_D for a constant gate voltage. Plot the four drain characteristic curves. Choose a scale for I_D that allows the largest current observed to fit on the graph. Label each curve with the gate voltage it represents.

11. In this step you will determine the value of $V_{GS(off)}$. Set V_{DD} for +12 V and V_{GG} for 0 V. Monitor the voltage across R_2 and slowly increase the negative gate voltage. When the voltage across R_2 reaches zero, note the gate voltage. Record this value as $V_{GS(off)}$. Record I_{DSS} from reading Plot obtained from step (10). These are the key parameters for your JFET.

12. In this step, you can observe a JFET connected as a two-terminal constant current source. Construct the circuit shown in Figure 4. Monitor the drain voltage while you increase the drain power supply from 0 V to +15 V. Notice the drain voltage where constant current begins (this point is imprecise but about the same as the absolute value of $V_{GS(off)}$).

    Compare the ammeter reading with the maximum current found in step (3).

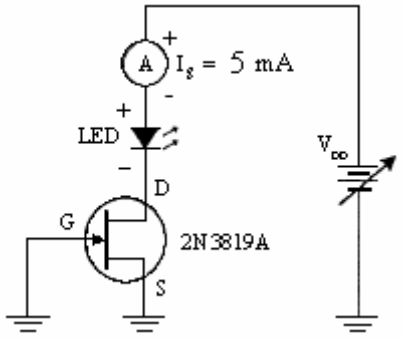
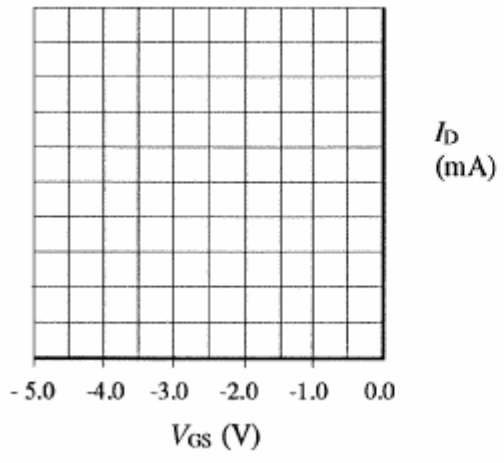


Fig.4: JFET connected as a two-terminal constant current source

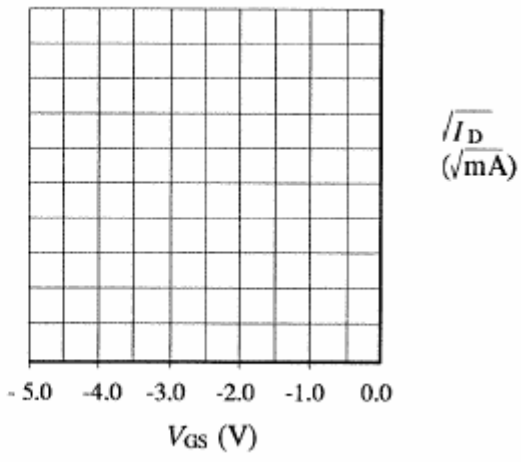
13. Using the test circuit shown in Figure 3, test the effect of varying V_{GS} with V_{DD} held at constant +12 V. Tabulate a set of data of I_D as a function a of V_{GS} (Table.3). Start with V_{GS} = 0.0 V and take data every - 0.25 V until there is no appreciable drain current. Then graph the data on Plot 1. This curve is the transconductance curve for your JFET. The result is nonlinear because the gate-source voltage is proportional to the square root of the drain current. To illustrate this, compute the square root of I_D and record in Table 3. Plot the square root of the drain current, ($\sqrt{I_D}$), as a function of the gate-source voltage on Plot 2.

V_{GS} (measured)	I_D (measured)	$\sqrt{I_D}$ (computed)
0.0 V		
-0.25 V		
-0.5 V		
-0.75 V		
-1.0 V		
-1.25 V		
-1.5 V		
-1.75 V		
-2.0 V		
-2.25 V		
-2.5 V		

Table.3: Drain Current Vs. The Gate-Source Voltage



Plot 1



Plot2

QUESTIONS & PROBLEMS:

1. (a) Explain how to find I_{DSS} from the characteristic curves of a JFET.

   (b) What was the maximum current in the LED in Step (12)?

2. (a) Does the experimental data indicate that the transconductance is a constant at all points?

   (b) From your experimental data, what evidence indicates that a JFET is a nonlinear device?

3. Look up the meaning of pinch-off voltage, V_P, when $V_{GS} = 0$. Note that the magnitude of V_{GS} is equal to the magnitude of V_P so we can use the characteristic curve for $V_{GS} = 0$ to determine V_P. Using the data from this experiment, determine the pinch-off voltage for your JFET.

4. Why should a JFET be operated with only reverse bias on the gate source?

5. Compare the characteristic curve observed for bipolar transistor with the characteristic curve obtained in this experiment for a JFET transistor.

Lab Session 9
Darlington Transistor Pair

OBJECTIVES:

After performing this experiment, you should be able to:

- Calculate and measure the DC parameters for a Darlington transistor pair.
- Determine the input and the output impedance of a Darlington transistor pair.
- Determine the current gain of a Darlington transistor pair.

SUMMARY OF THEORY:

Darlington transistors contain two transistors connected in an emitter-follower configuration, while sharing the same collector contact as shown in Figure 1. The key advantage of the Darlington configuration is that the total current gain of the circuit equals the product of the current gain of the two devices. The disadvantage is the larger saturation voltage. Since the two devices share the same collector, the saturation voltage of the Darlington pair equals the forward bias voltage of transistor Q_2 plus the saturation voltage of transistor Q_1. Since the forward bias voltage is much larger than the saturation voltage, the saturation voltage of the Darlington pair is also significantly larger. This larger voltage results in larger on-state power dissipation in the device.

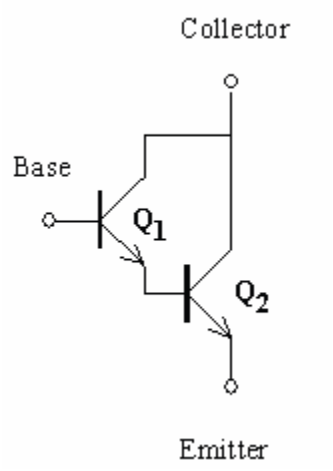


Fig.1: Darlington Transistor Pair

A Darlington Connection provides a pair of BJT transistors with effective beta (β_D) equal to the product of the individual transistor betas.

$$\beta_D = \beta_1 \beta_2 \tag{1}$$

The Darlington emitter-follower has higher input impedance than that of an emitter-follower. The Darlington emitter-follower input impedance is:

$$R_{in} = R_B \left\| (\beta_D R_E) \right. \tag{2}$$

The output impedance of the Darlington emitter-follower is:

$$R_{out} = r_e \tag{3}$$

The voltage gain of the Darlington emitter-follower is:

$$A_V = \frac{R_E}{(R_E + r_e)} \tag{4}$$

EQUIPMENTS:

- Variable DC Power Supply
- Dual-Trace Oscilloscope
- Breadboard
- Resistors
- Capacitors
- 2N3904 NPN Transistor

PROCEDURE:

Part 1: Darlington Emitter-Follower Circuit

1. For the circuit of Figure 2, calculate the DC bias voltages and currents.

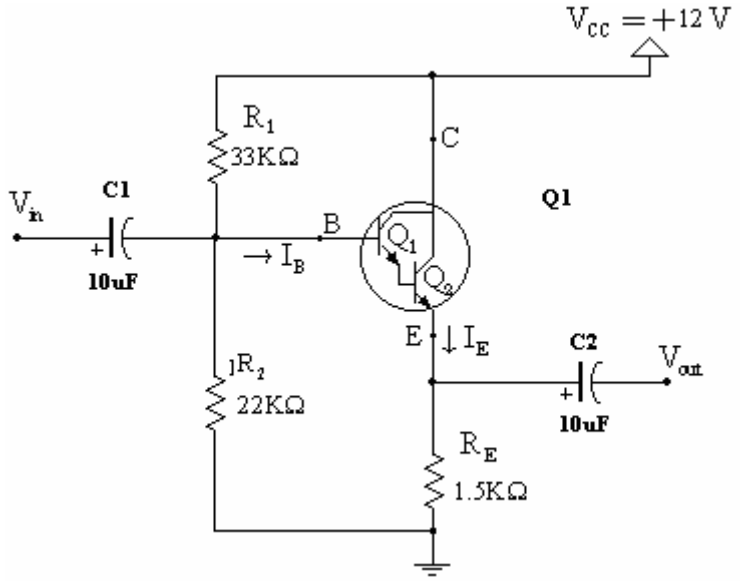


Fig.2: Darlington Emitter-Follower Circuit

2. Calculate the theoretical values of voltage gain, input and output impedance.

3. Construct the Darlington circuit of Figure 2. Using a DMM, measure and record the DC bias voltages.

4. Calculate the base and emitter DC currents, and then calculate the value of the transistor beta at this Q-point.

5. Apply an input signal $V_{in} = 1V_P$ at $f = 10$ KHz. Using the oscilloscope, observe and record the output voltage to assure that the signal is not clipped or distorted. (Reduce the input signal amplitude if necessary).

6. Measure the peak-to peak voltages of the input and output waveforms, and record these values. Use the measured signal voltages to calculate the voltage gain of the amplifier.

7. Carefully sketch the input and output waveforms showing the phase shift between them.

Part 2: Darlington Input and Output Impedance

8. Calculate the input and output impedance of the Darlington Pair of Figure 2.

9. Using the basic laws of voltage division, you can easily determine the input impedance of the Darlington pair as follows:

    - Insert a 100 $k\Omega$ potentiometer between the signal generator and the input coupling capacitor.
    - Adjust the potentiometer until V_{out} drops to one-half the value noted prior to insert the potentiometer.
    - Power down, and remove the pot from the circuit *without disturbing its setting*.
    - Measure the adjusted resistance of the potentiometer, and record this value. This value equals the input impedance of the Darlington pair.

10. To measure the output resistance R_{out} of the Darlington pair: connect a 1 $K\Omega$ potentiometer connected between the output coupling capacitor and ground. Adjust the potentiometer until V_{out} drops to one-half the previous value. Remove the potentiometer and measure its resistance. By the voltage divider role, the resistance of the potentiometer equals the output resistance of the Darlington transistor pair.