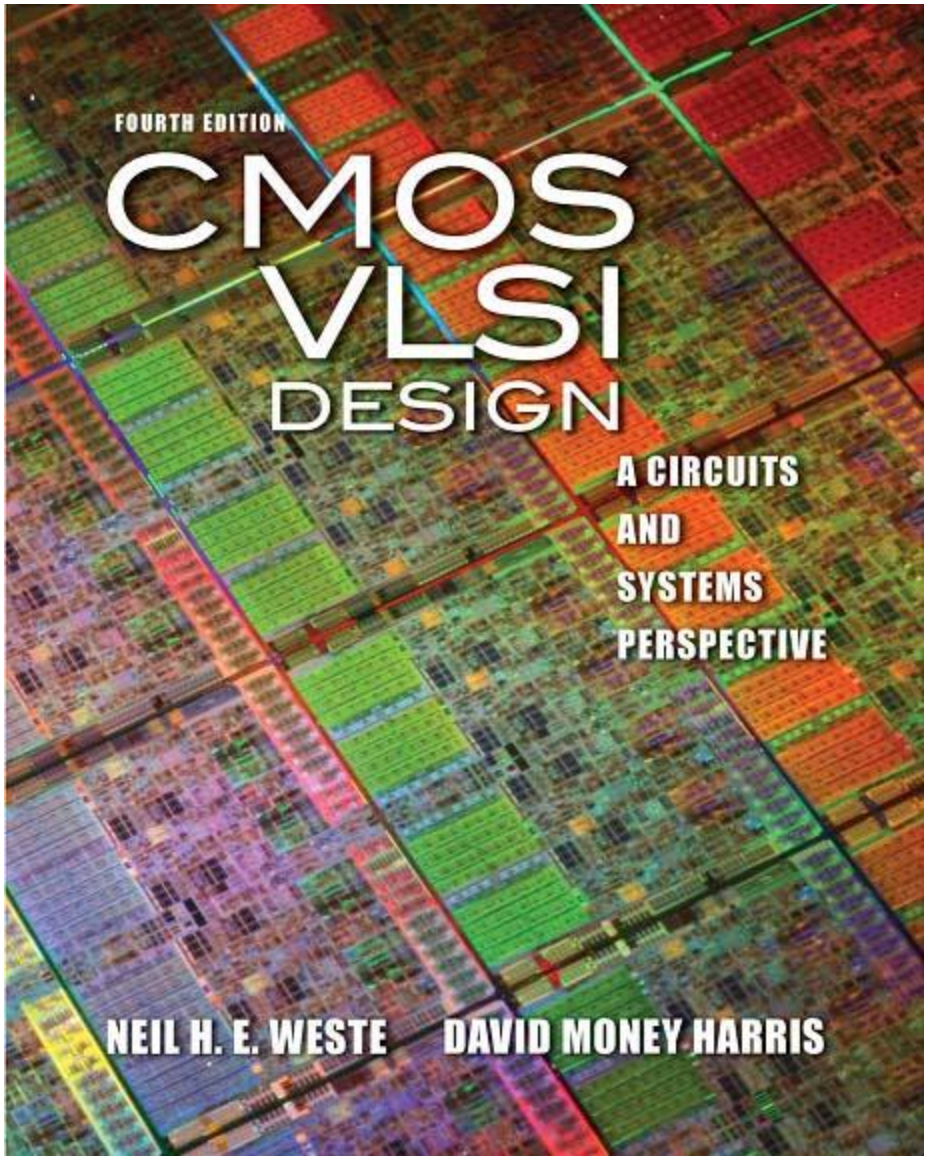


Transistor Theory and DC Characteristics

Dr. Bassam Jamil

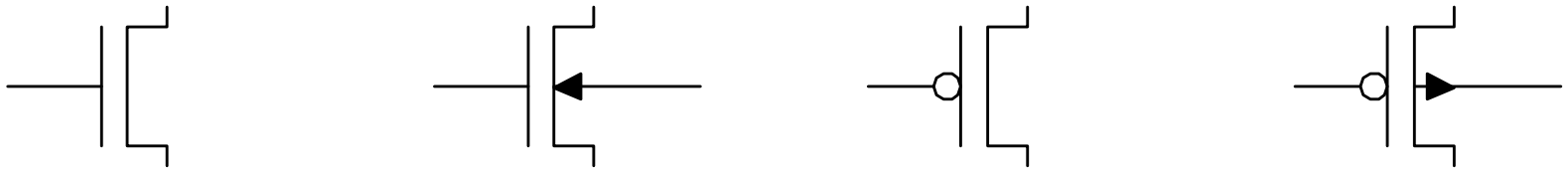
Adopted from slides of the textbook

Outline

- Transistor Theory
  - Channel Formation and operation Regions
  - I-V Characteristics
  - C-V Characteristics
    - Gate and Diffusion Capacitance
- Nonideal characteristics
- DC Response
  - DC Response
  - Logic Levels and Noise Margins

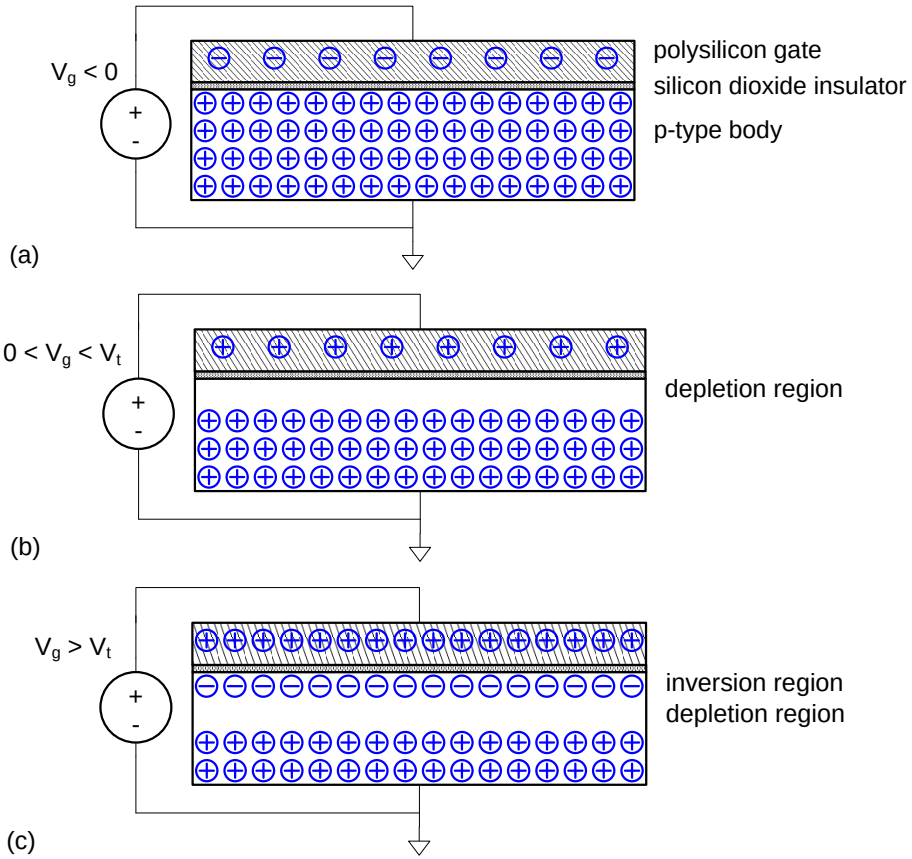
Introduction

- So far, we have treated transistors as ideal switches
- An ON transistor passes a finite amount of current
  - Depends on terminal voltages
  - Derive current-voltage (I-V) relationships
- Transistor gate, source, drain all have capacitance
  - $I = C (\Delta V/\Delta t) \rightarrow \Delta t = (C/I) \Delta V$
  - Capacitance and current determine speed



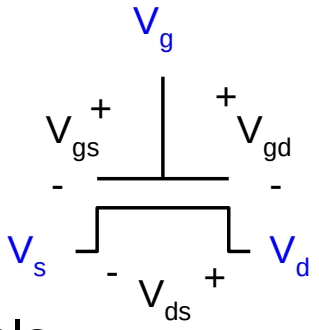
MOS Device Channel Formation

- Gate and body form MOS capacitor
- Operating modes
  - Accumulation
  - Depletion
  - Inversion



Terminal Voltages

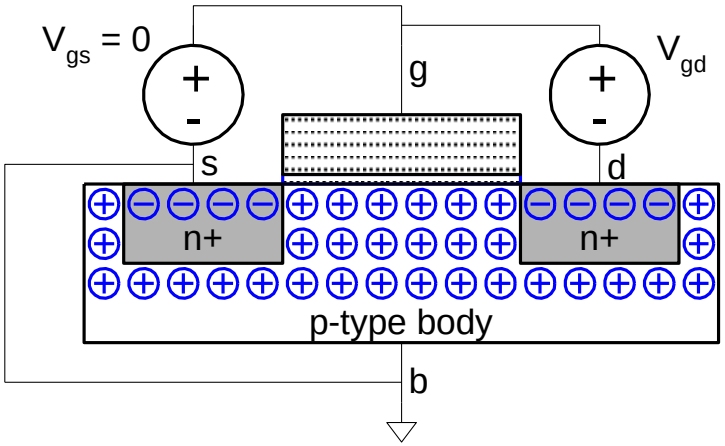
- Mode of operation depends on V_g, V_d, V_s
  - $V_{gs} = V_g - V_s$
  - $V_{gd} = V_g - V_d$
  - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$



- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence $V_{ds} \geq 0$
- nMOS body is grounded. First assume source is 0 too.
- Three regions of operation
  - *Cutoff*
  - *Linear*
  - *Saturation*

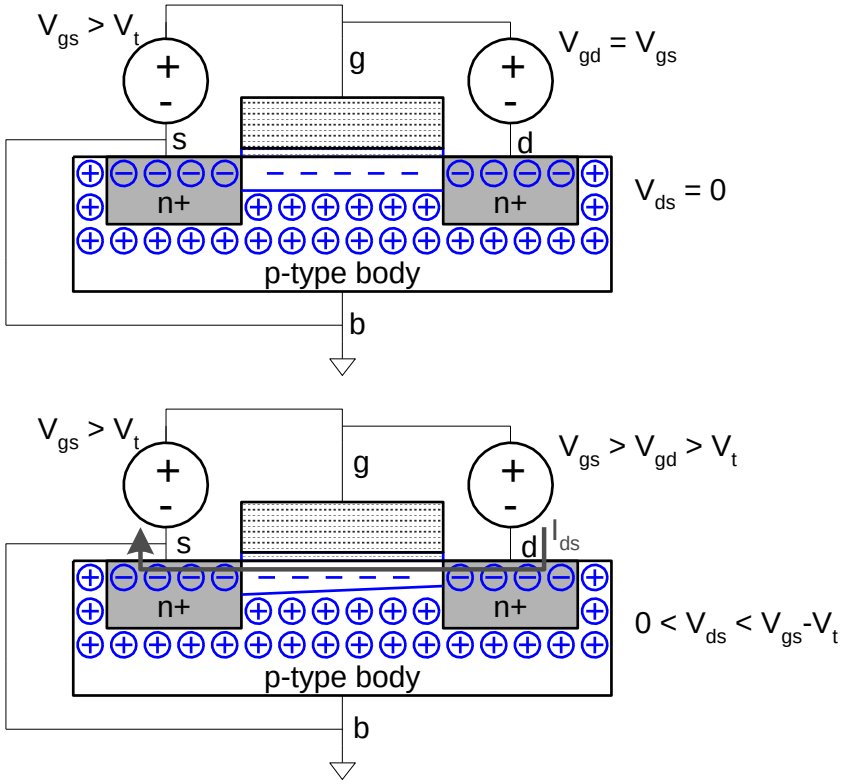
nMOS Cutoff

- No channel
- $I_{ds} \approx 0$



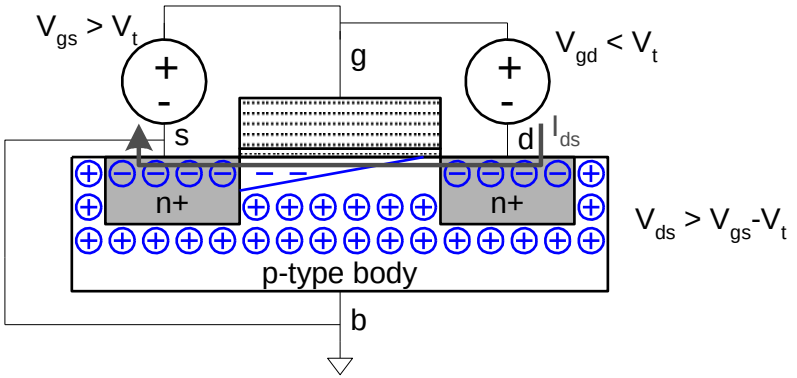
nMOS Linear

- Channel forms
- Current flows from d to s
  - e^- from s to d
- I_{ds} increases with V_{ds}
- Similar to linear resistor



nMOS Saturation

- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current *saturates*
- Similar to current source

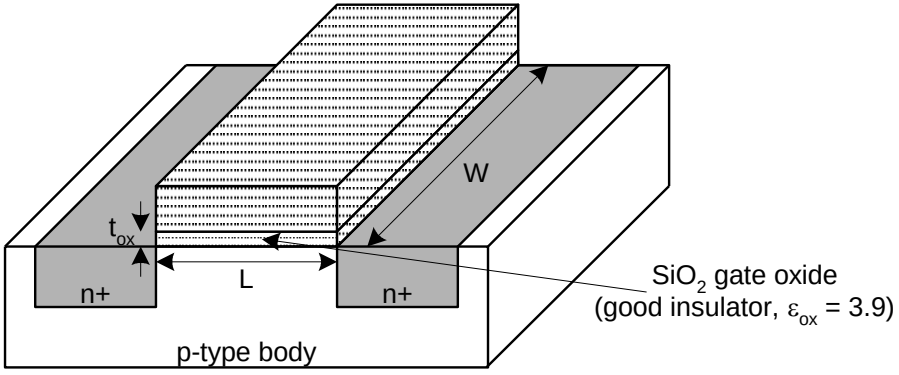


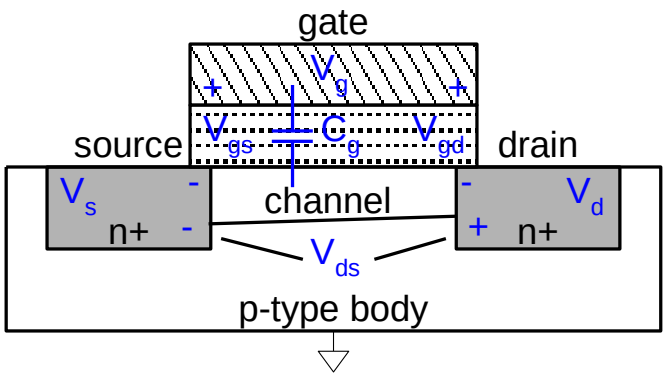
I-V Characteristics

- In Linear region, I_{ds} depends on
  - How much charge is in the channel?
  - How fast is the charge moving?

Long Channel I-V

- MOS structure looks like parallel plate capacitor while operating in inversions
  - Gate – oxide – channel
- $Q_{channel} = CV$
- $C = C_g = \varepsilon_{ox} WL/t_{ox} = C_{ox} WL$ $\quad C_{ox} = \varepsilon_{ox} / t_{ox}$
- $V = V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t$





Long Channel I-V

Ids = Qchannel / Time

$$Q_{channel} = C_g\left(V_{gc} - V_t\right)$$

$$C_g = k_{ox}\varepsilon_0\frac{WL}{t_{ox}} = \varepsilon_{ox}\frac{WL}{t_{ox}} = C_{ox}WL$$

Time= L/v

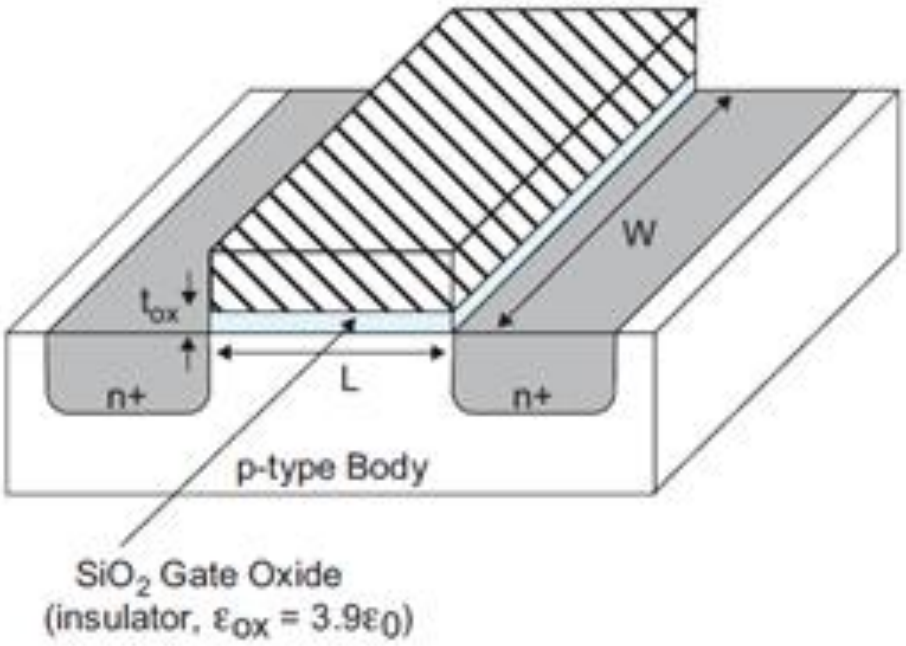
$$v = \mu E \qquad \text{Where,} \quad E = \frac{V_{ds}}{L}$$

$$I_{ds} = \frac{Q_{channel}}{L/v}$$

$$= \mu C_{ox}\frac{W}{L}\left(V_{gc} - V_t - V_{ds}/2\right)V_{ds}$$

$$= \beta\left(V_{GT} - V_{ds}/2\right)V_{ds}$$

$$\beta = \mu C_{ox}\frac{W}{L};\ V_{GT} = V_{gc} - V_t$$



nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} = \frac{\beta}{2} V_{GT}^2$$

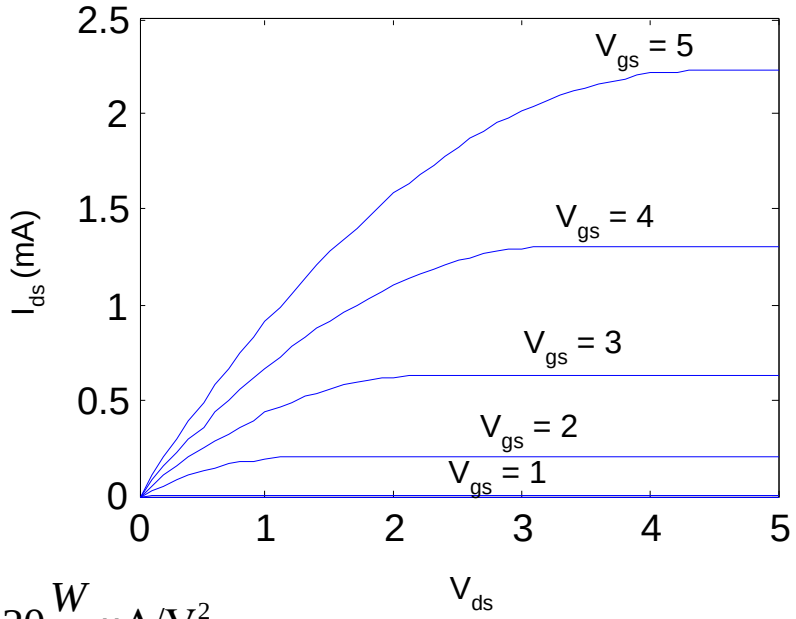
nMOS I-V Summary

- *Shockley* 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

Example

- The following is a 0.6 μm process:
  - t_{ox} = 100 Å
  - μ = 350 $cm^2/V*s$
  - V_t = 0.7 V
- Plot I_{ds} vs. V_{ds}
  - V_{gs} = 0, 1, 2, 3, 4, 5
  - Use W/L = 4/2 λ



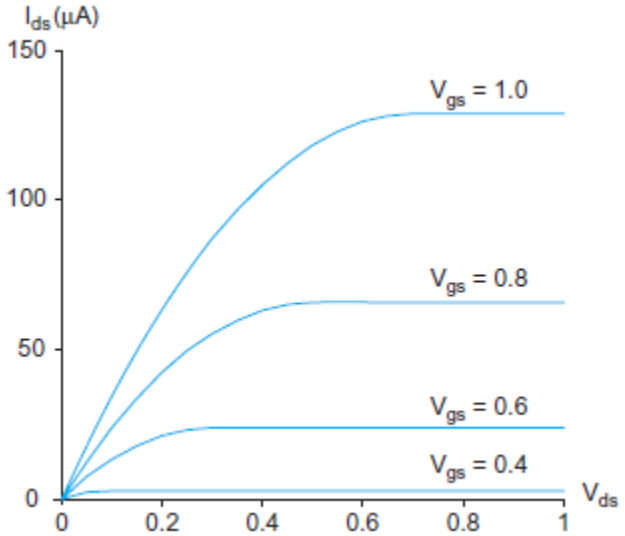
$$\beta = \mu C_{ox}\frac{W}{L} = (350)\left(\frac{3.9\times 8.85\cdot 10^{-14}}{100\cdot 10^{-8}}\right)\left(\frac{W}{L}\right) = 120\frac{W}{L}\,\mu A/V^2$$

Another Example

Consider an nMOS transistor in a 65 nm process with a minimum drawn channel length of 50 nm ($\lambda = 25$ nm). Let $W/L = 4/2\ \lambda$ (i.e., 0.1/0.05 μm). In this process, the gate oxide thickness is 10.5 Å. Estimate the high-field mobility of electrons to be 80 $cm^2/V \cdot s$ at 70 °C. The threshold voltage is 0.3 V. Plot I_{ds} vs. V_{ds} for $V_{gs} = 0$, 0.2, 0.4, 0.6, 0.8, and 1.0 V using the long-channel model.

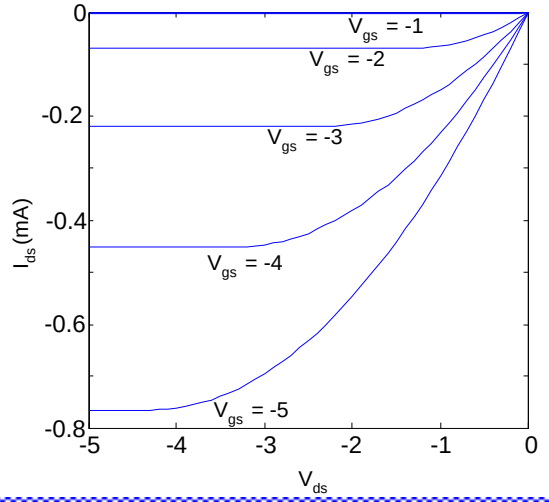
SOLUTION: We first calculate β.

$$\beta = \mu C_{ox}\frac{W}{L} = \left(80\frac{\text{cm}^2}{\text{V}\cdot\text{s}}\right)\left(\frac{3.9\times 8.85\times 10^{-14}\ \frac{\text{F}}{\text{cm}}}{10.5\times 10^{-8}\ \text{cm}}\right)\left(\frac{W}{L}\right) = 262\frac{W}{L}\frac{\text{A}}{\text{V}^2} \qquad (2.11)$$



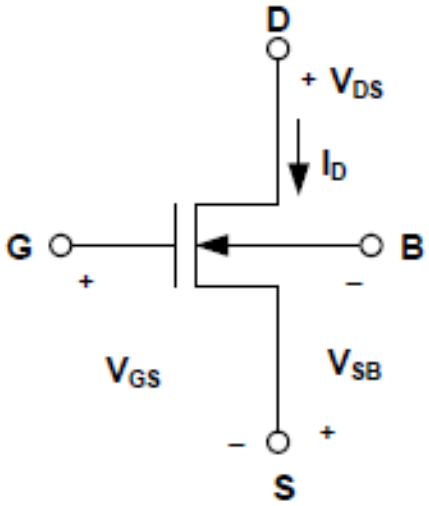
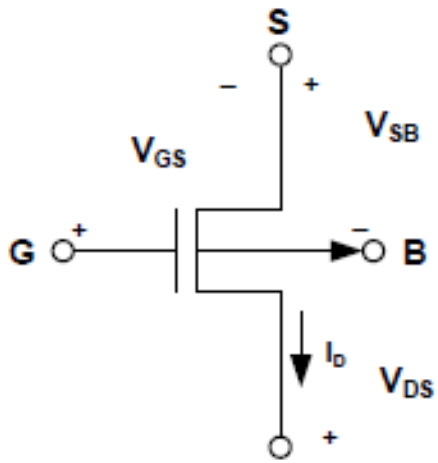
pMOS I-V

- All dopings and voltages are inverted for pMOS
  - Source is the more positive terminal
- Mobility μ_p is determined by holes
  - Typically 2-3x lower than that of electrons μ_n
  - 120 $cm^2/V \cdot s$ in AMI 0.6 μm process
- Thus pMOS must be wider to provide same current
  - In this class, assume $\mu_n / \mu_p = 2$



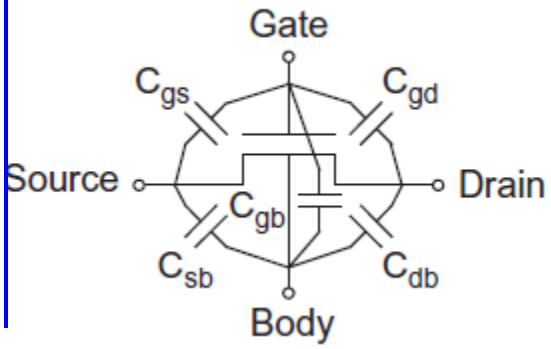
Reverse Voltages Terminals

Change > to <
Positives to negatives

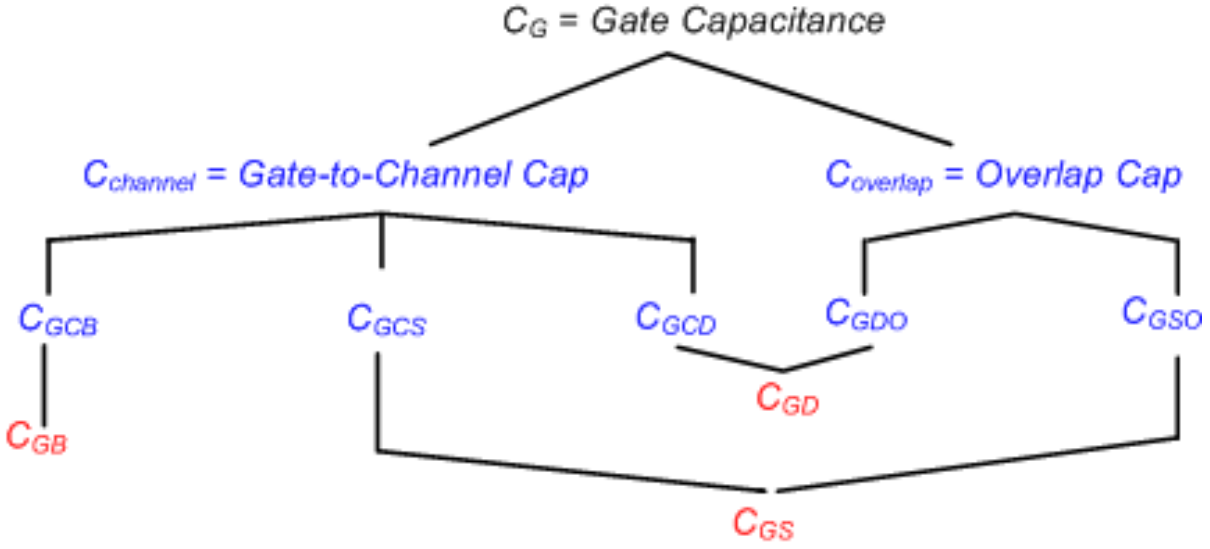
Term	nMOS	pMOS
Voltages and Currents		
V_{GS}, V_{DS}, V_{SB}, V_T	Positive	Negative
Cut-off	When $V_{GS} < V_T$ $I_D=0$	When $V_{GS} > V_T$ $I_D=0$
Linear	When $V_{GS} \geq V_T$ $V_{DS} < V_{GS} - V_T$ $I_D = k_n [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$	When $V_{GS} \leq V_T$ $V_{DS} > V_{GS} - V_T$ $I_D = k_p [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$
Saturation	When $V_{GS} \geq V_T$ $V_{DS} \geq V_{GS} - V_T$ $I_D = (k_n/2) [(V_{GS} - V_T)^2] (1 + \lambda V_{DS})$	When $V_{GS} \leq V_T$ $V_{DS} \leq V_{GS} - V_T$ $I_D = (k_n/2) [(V_{GS} - V_T)^2] (1 + \lambda V_{DS})$
k	$k_n = k'_n W/L$ $k'_n = \mu_n C_{ox} = \mu_n \varepsilon_{ox}/t_{ox}$	$K_p = k'_n W/L$ $k'_p = \mu_p C_{ox} = \mu_p \varepsilon_{ox}/t_{ox}$
Fermi potential ϕ_F	Negative	Positive
Depletion region charge densities Q_{B0} and Q_B	Negative	Postitive
Substrate bias coefficient γ	Positive	Negative

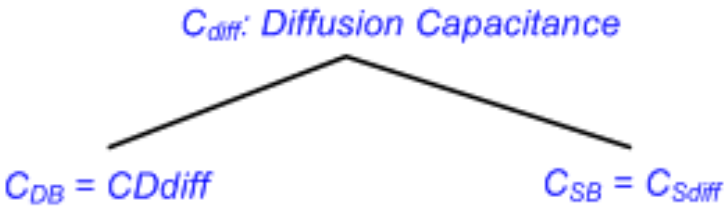
Capacitance

- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor is very important
  - Creates channel charge necessary for operation
- Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called diffusion capacitance because it is associated with source/drain diffusion



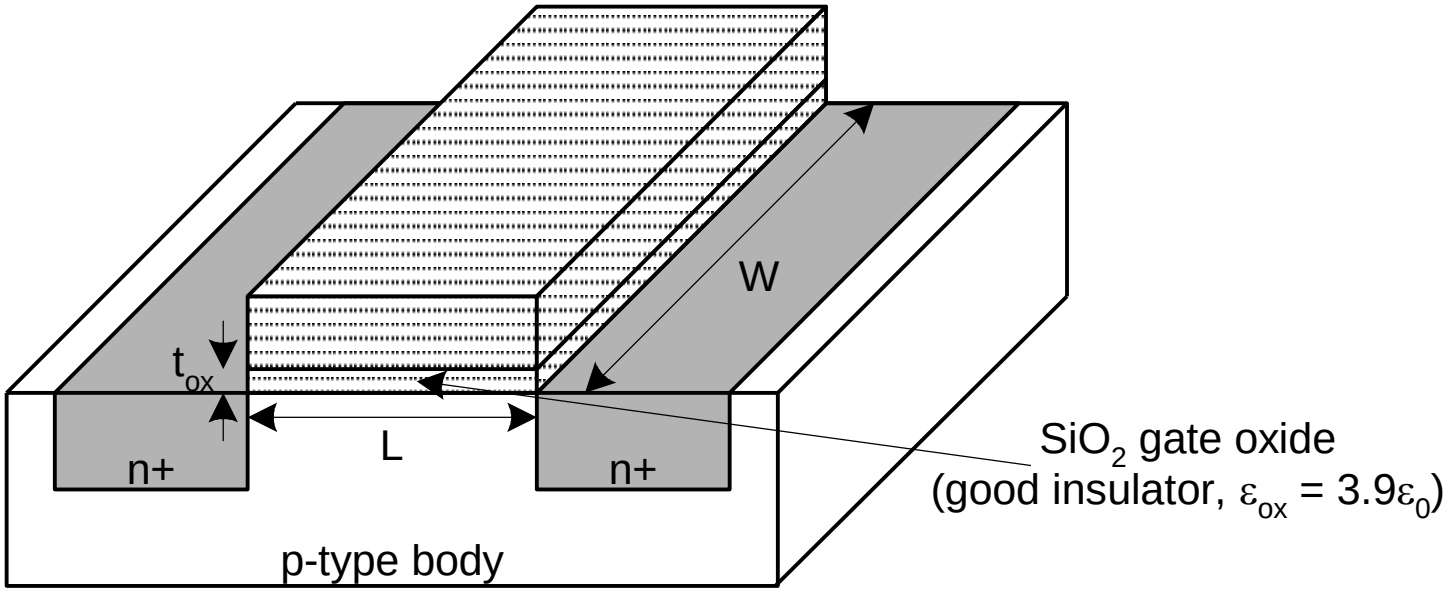
MOS Device Capacitances





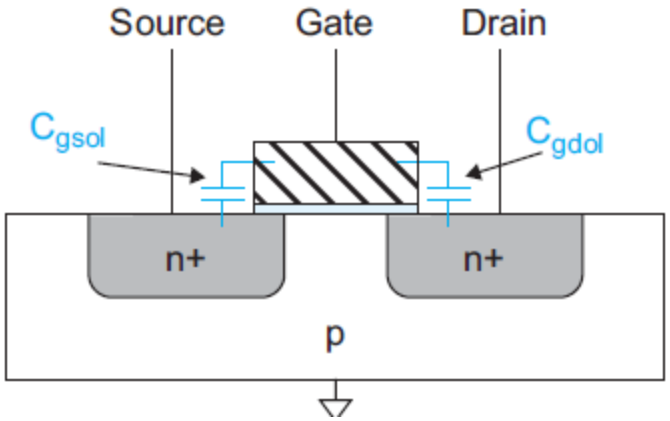
Gate Capacitance

- Approximate channel as connected to source
- $C_{gs} = \varepsilon_{ox} WL/t_{ox} = C_{ox} WL = C_{permicron} W$
- $C_{permicron}$ is typically about 2 fF/μm

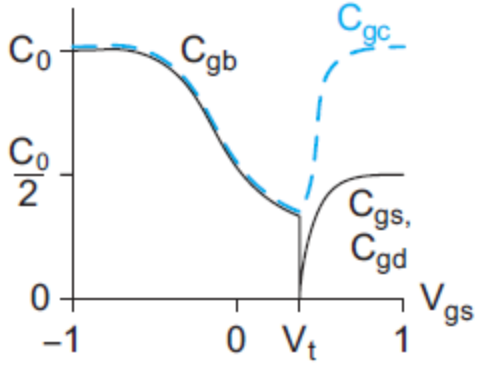


Gate Overlap Capacitance

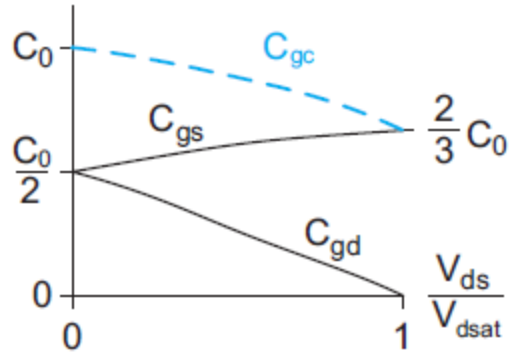
The gate overlaps the source and drain in a real device and also has fringing fields terminating on the source and drain. This leads to additional overlap capacitances, as shown in Figure 2.10. These capacitances are proportional to the width of the transistor. Typical values are $C_{gsol} = C_{gdol} = 0.2 - 0.4$ fF/μm. They should be added to the intrinsic gate capacitance to find the total.



Approximation of Intrinsic Gate Capacitance



(a)



(b)

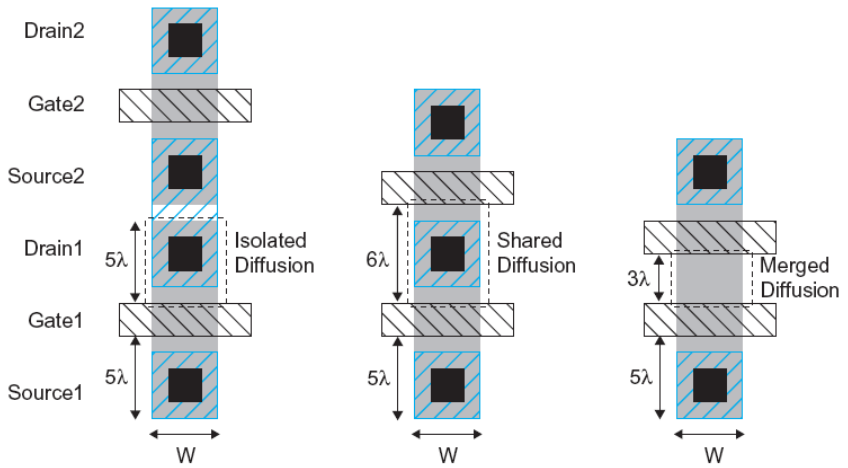
FIGURE 2.9 Intrinsic gate capacitance $C_{gc} = C_{gs} + C_{gd} + C_{gb}$ as a function of (a) V_{gs} and (b) V_{ds}

TABLE 2.1 Approximation for intrinsic MOS gate capacitance

Parameter	Cutoff	Linear	Saturation
C_{gb}	$\leq C_0$	0	0
C_{gs}	0	$C_0/2$	$2/3\ C_0$
C_{gd}	0	$C_0/2$	0
$C_g = C_{gs} + C_{gd} + C_{gb}$	C_0	C_0	$2/3\ C_0$

Diffusion Capacitance

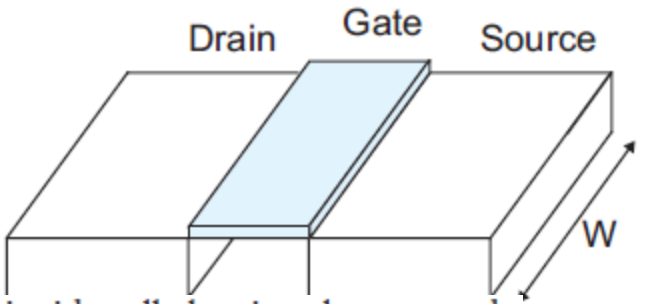
- C_{sb}, C_{db}
- Undesirable, called *parasitic* capacitance
- Capacitance depends on area and perimeter
  - Use small diffusion nodes
  - Comparable to C_g for contacted diff
  - ½ C_g for uncontacted
  - Varies with process



Diffusion Cap Calculations

- Total source diff capacitance

$$C_{sb} = AS \times C_{jbs} + PS \times C_{jbssw}$$



significant. In some SPICE models, the capacitance of this sidewall abutting the gate and channel is specified with another set of parameters:

$$C_{jbsswg} = C_{JSW}\left(1+\frac{V_{sb}}{\psi_{SWG}}\right)^{-M_{JSWG}} \qquad (2.20)$$

ometry

$$C_{jbssw} = C_{JSW}\left(1+\frac{V_{sb}}{\psi_{SW}}\right)^{-M_{JSW}}$$

* **The side wall capacitance abutting the channel is:**

$$C_{jbsswg} = C_{JSW}\left(1+\frac{V_{sb}}{\psi_{SWG}}\right)^{-M_{JSWG}}$$

- Source area (AS) = W D
- Source Perimeter (PS) = W + 2D

Diffusion Cap Example

Example 2.2

Calculate the diffusion parasitic C_{db} of the drain of a unit-sized contacted nMOS transistor in a 65 nm process when the drain is at 0 V and again at $V_{DD} = 1.0$ V. Assume the substrate is grounded. The diffusion region conforms to the design rules from Figure 2.8 with $\lambda = 25$ nm. The transistor characteristics are $CJ = 1.2$ fF/μm^2, $MJ = 0.33$, $CJSW = 0.1$ fF/μm, $CJSWG = 0.36$ fF/μm, $MJSW = MJSWG = 0.10$, and $\psi_0 = 0.7$ V at room temperature.

SOLUTION: From Figure 2.8, we find a unit-size diffusion contact is $4 \times 5\ \lambda$, or $0.1 \times 0.125\ \mu$m. The area is 0.0125 μm^2 and perimeter is 0.35 μm plus 0.1 μm along the channel. At zero bias, $C_{jbd} = 1.2$ fF/μm^2, $C_{jbdsw} = 0.1$ fF/μm, and $C_{jbdswg} = 0.36$ fF/μm. Hence, the total capacitance is

$$C_{db}(0\text{ V}) = (0.0125\mu\text{m}^2)\left(1.2\frac{\text{fF}}{\mu\text{m}^2}\right) + (0.35\mu\text{m})\left(0.1\frac{\text{fF}}{\mu\text{m}}\right) + (0.1\mu\text{m})\left(0.36\frac{\text{fF}}{\mu\text{m}}\right) = 0.086\,\text{fF} \quad (2.21)$$

At a drain voltage of V_{DD}, the capacitance reduces to

$$C_{db}(1\text{ V}) = (0.0125\mu\text{m}^2)\left(1.2\frac{\text{fF}}{\mu\text{m}^2}\right)\left(1+\frac{1.0}{0.7}\right)^{-0.33} + \left[(0.35\mu\text{m})\left(0.1\frac{\text{fF}}{\mu\text{m}}\right) + (0.1\mu\text{m})\left(0.36\frac{\text{fF}}{\mu\text{m}}\right)\right]\left(1+\frac{1.0}{0.7}\right)^{-0.10} = 0.076\,\text{fF} \quad (2.22)$$

For the purpose of manual performance estimation, this nonlinear capacitance is too much effort. An effective capacitance averaged over the switching range is quite satisfactory for digital applications. In this example, the effective drain capacitance would be approximated as the average of the two extremes, 0.081 fF.

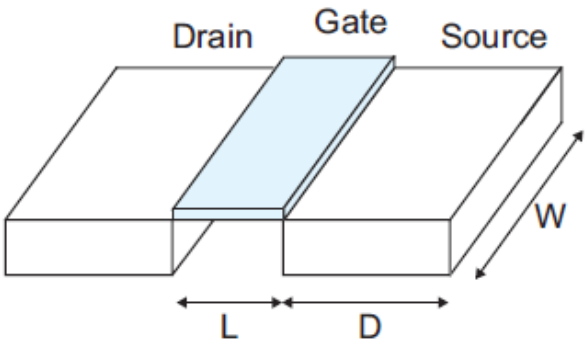
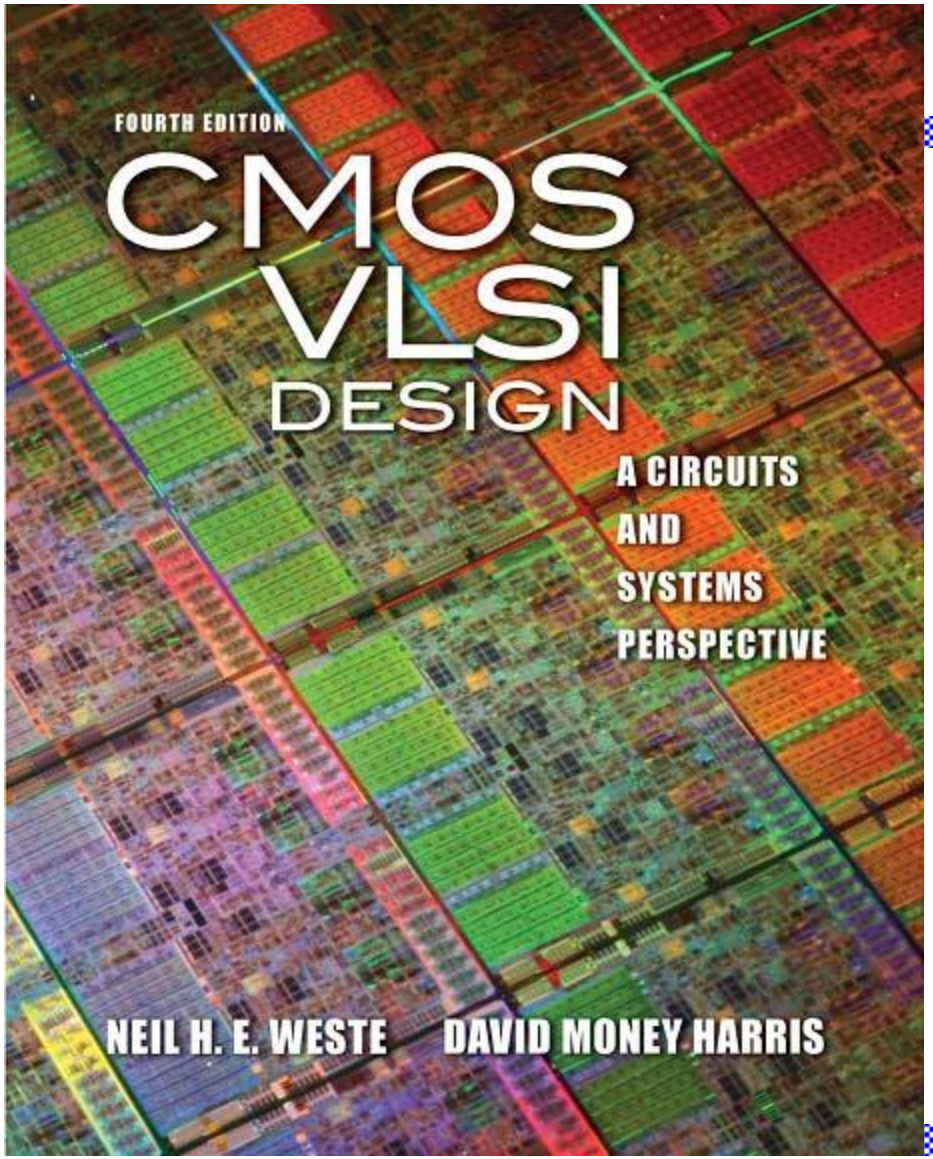


FIGURE 2.12 Diffusion region geometry

$\lambda = 25$ nm
$W = 4\ \lambda = 0.1\mu$m
$D = 5\ \lambda = 0.125\mu$m



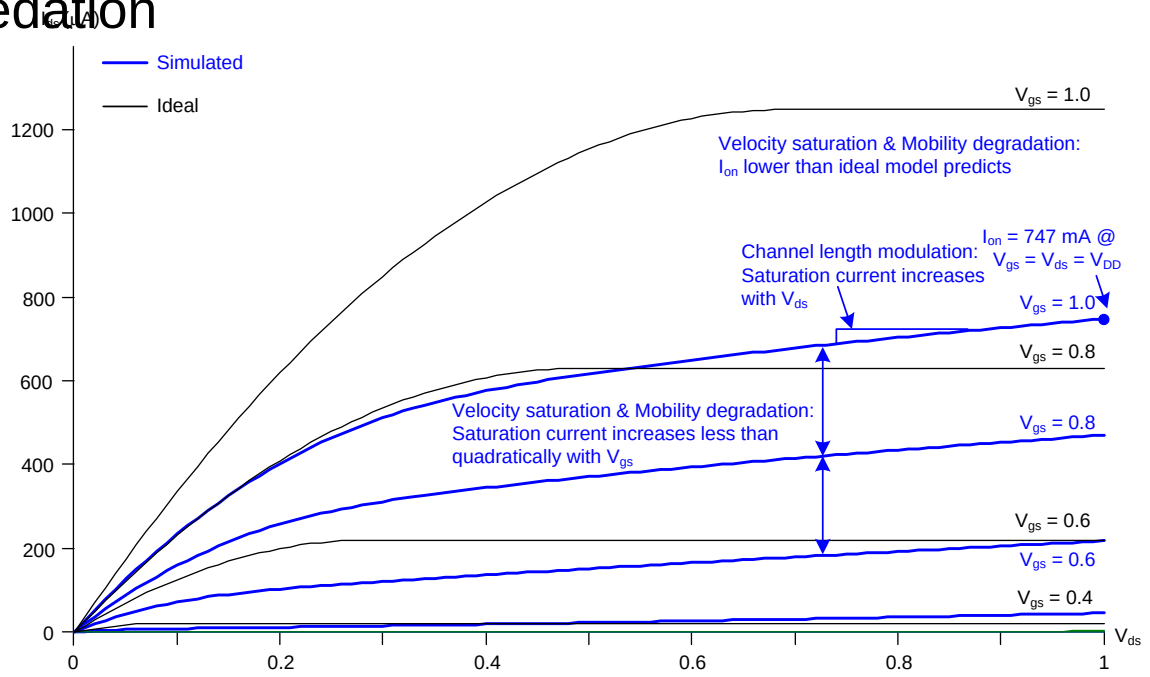
Nonideal Transistor Theory

Outline

- Nonideal Transistor Behavior
  - High Field Effects
    - Mobility Degradation
    - Velocity Saturation
  - Channel Length Modulation
  - Threshold Voltage Effects
    - Body Effect
    - Drain-Induced Barrier Lowering
    - Short Channel Effect
  - Leakage
    - Subthreshold Leakage
    - Gate Leakage
    - Junction Leakage
- Process and Environmental Variations

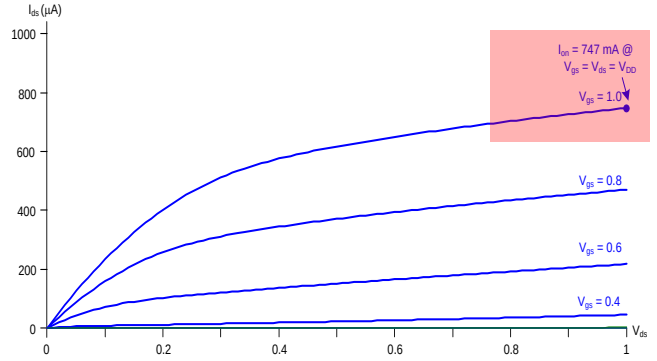
Ideal vs. Simulated nMOS I-V Plot

- 65 nm IBM process, V_{DD} = 1.0 V
- This is due to:
  - Velocity Saturation
  - Mobility depredation

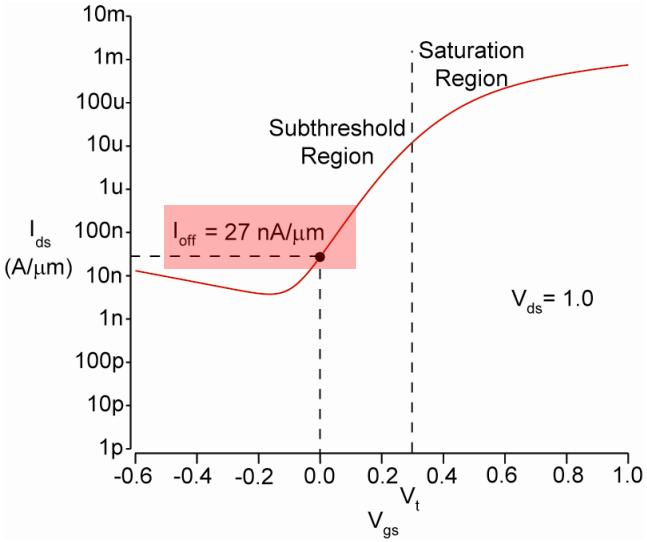


ON and OFF Current

- $I_{on} = I_{ds}$ @ $V_{gs} = V_{ds} = V_{DD}$
  - Saturation



- $I_{off} = I_{ds}$ @ $V_{gs} = 0$, $V_{ds} = V_{DD}$
  - Cutoff



Nonideal Transistor Behavior: High Field Effects

- The saturation current increases less than quadratically with increasing Vgs because of:
  - velocity saturation
  - mobility degradation.
- At high **lateral** field strengths (V_{ds} /L), carrier velocity ceases to increase linearly with field strength. This is called **velocity saturation** and results in lower I_{ds} than expected at high V_{ds} .
- At high **vertical** field strengths (V_{gs} /t_{ox}), the carriers scatter off the oxide interface more often, slowing their progress. This **mobility degradation** effect also leads to less current than expected at high V_{gs}

Nonideal Transistor Behavior: Other Effects

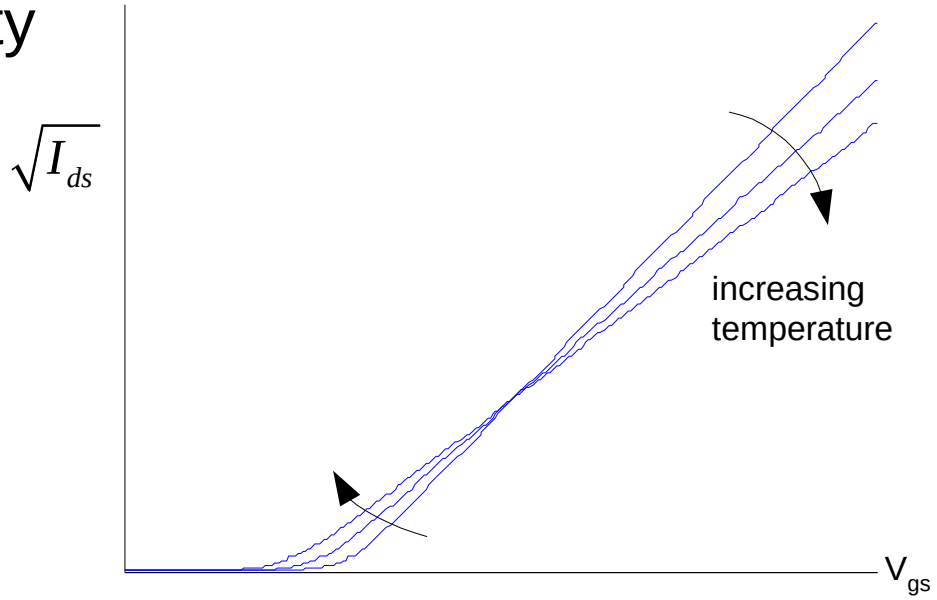
- The saturation current of the nonideal transistor increases somewhat with V_{ds} . This is caused by **channel length modulation**, in which higher V_{ds} increases the size of the depletion region around the drain and thus effectively shortens the channel.
- There are other fields in the transistor have some effect on the channel, effectively modifying the threshold voltage.
  - Increasing the potential between the source and body raises the threshold through the **body effect**.
  - Increasing the drain voltage lowers the threshold through **drain-induced barrier lowering.**
  - Increasing the channel length raises the threshold through **the short channel effect**.

Nonideal Transistor Behavior: Leakage & Temperature

- Sources of leakage result in current flow in nominally OFF transistors:
  - **Subthreshold** conduction: when $V_{gs} < V_t$, the current drops off exponentially rather than abruptly becoming zero.
  - **Gate leakage**: The current into the gate I_g is ideally 0. However, as the thickness of gate oxides reduces to only a small number of atomic layers, electrons tunnel through the gate, causing some gate leakage current.
  - **Diffusion leakage**: The source and drain diffusions are typically reverse-biased diodes and also experience junction leakage into the substrate or well.
- Both mobility and threshold voltage decrease with rising temperature. The mobility effect tends to dominate for strongly ON transistors, resulting in lower Ids at high temperature. The threshold effect is most important for OFF transistors, resulting in higher leakage current at high temperature. **In summary, MOS characteristics degrade with temperature.**

Temperature Sensitivity

- Increasing temperature
  - Reduces mobility
  - Reduces V_t



The mobility effect tends to dominate for strongly ON transistors, resulting in lower Ids at high temperature. The threshold effect is most important for OFF transistors, resulting in higher leakage current at high temperature.

Electric Fields Effects

- Vertical electric field: $E_{vert} = \mathbf{V_{gs} / t_{ox}}$
  - Attracts carriers into channel
  - Long channel: $Q_{channel} \propto E_{vert}$
- Lateral electric field: $E_{lat} = \mathbf{V_{ds} / L}$
  - Accelerates carriers from drain to source
  - Long channel: $v = \mu E_{lat}$

Mobility Degradation

- High E_{vert} effectively reduces mobility
  - Collisions with oxide interface

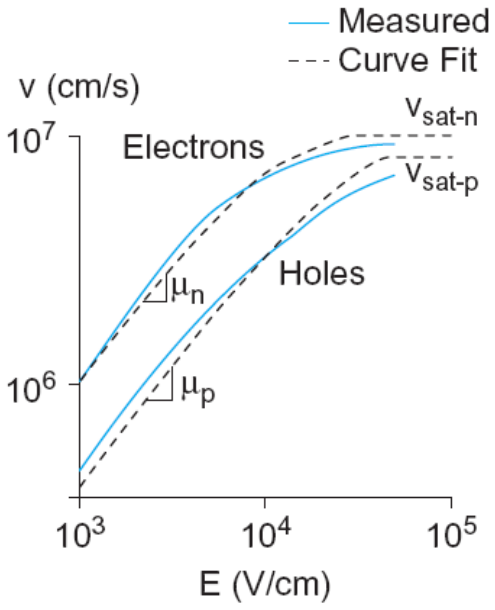
$$\mu_{\text{eff}-n} = \frac{540\frac{\text{cm}^2}{\text{V}\cdot\text{s}}}{1+\left(\frac{V_{gs}+V_t}{0.54\frac{\text{V}}{\text{nm}}t_{\text{ox}}}\right)^{1.85}}$$

$$\mu_{\text{eff}-p} = \frac{185\frac{\text{cm}^2}{\text{V}\cdot\text{s}}}{1+\frac{\left|V_{gs}+1.5V_t\right|}{0.338\frac{\text{V}}{\text{nm}}t_{\text{ox}}}}$$

Velocity Saturation

- At high E_{lat}, carrier velocity rolls off
  - Carriers scatter off atoms in silicon lattice
  - Velocity reaches v_{sat}
    - Electrons: 10^7 cm/s
    - Holes: 8 x 10^6 cm/s
  - Better model

$$v = \begin{cases} \dfrac{\mu_{\text{eff}} E}{1 + \dfrac{E}{E_c}} & E < E_c \\ v_{\text{sat}} & E \geq E_c \end{cases} \qquad E_c = \frac{2 v_{\text{sat}}}{\mu_{\text{eff}}}$$



Vel Sat I-V Effects

- Ideal transistor ON current increases with V_{DD}^2

$$I_{ds} = \mu C_{ox} \frac{W}{L} \frac{\left(V_{gs} - V_t\right)^2}{2} = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

- Velocity-saturated ON current increases with V_{DD}

$$I_{ds} = C_{ox} W \left(V_{gs} - V_t\right) v_{max}$$

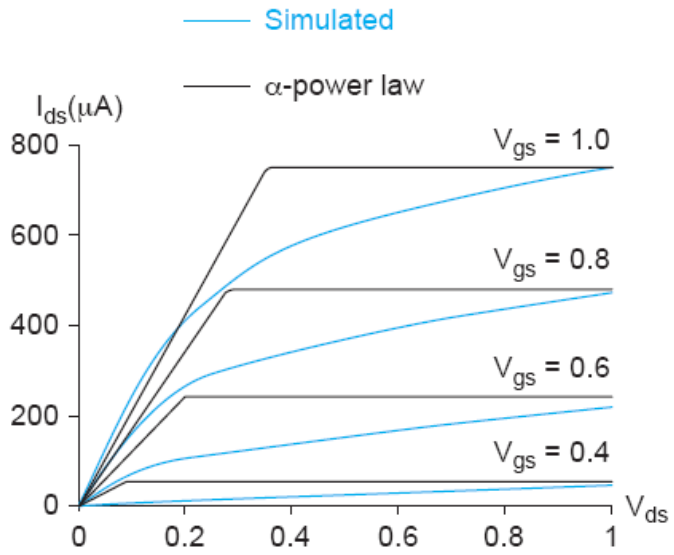
- Real transistors are partially velocity saturated
  - Approximate with α-power law model
  - $I_{ds} \propto V_{DD}^{\alpha}$
  - $1 < \alpha < 2$ determined empirically (≈ 1.3 for 65 nm)

α-Power Model

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ I_{dsat}\dfrac{V_{ds}}{V_{dsat}} & V_{ds} < V_{dsat} \quad \text{linear} \\ I_{dsat} & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

$$I_{dsat} = P_c \frac{\beta}{2}\left(V_{gs} - V_t\right)^{\alpha}$$

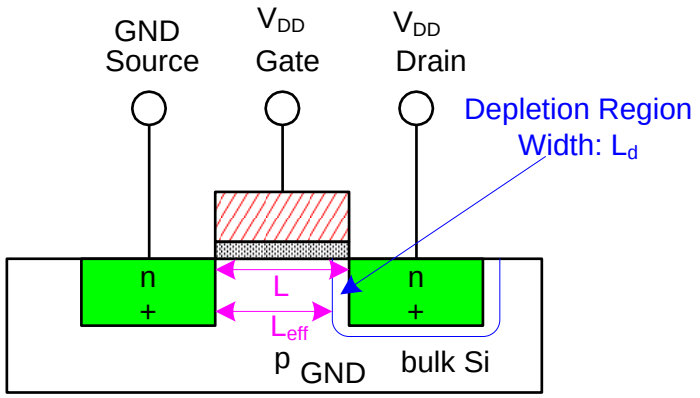
$$V_{dsat} = P_v \left(V_{gs} - V_t\right)^{\alpha/2}$$



Channel Length Modulation

- Reverse-biased p-n junctions form a *depletion region*
  - Region between n and p with no carriers
  - Width of depletion L_d region grows with reverse bias
  - $L_{eff} = L - L_d$

$$I_{ds} = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2\left(1 + \lambda V_{ds}\right)$$



λ = *channel length modulation coefficient*

- not feature size
- Empirically fit to I-V characteristics

Threshold Voltage Effects

- V_t is V_{gs} for which the channel starts to invert
- Ideal models assumed V_t is constant
- Really depends (weakly) on almost everything else:
  - Body voltage: *Body Effect*
  - Drain voltage: *Drain-Induced Barrier Lowering*
  - Channel length: *Short Channel Effect*

Body Effect

- Body is a fourth transistor terminal
- V_{sb} affects the charge required to invert the channel
  - Increasing V_s or decreasing V_b increases V_t

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$$

- ϕ_s = *surface potential* at threshold

$$\phi_s = 2v_T \ln\frac{N_A}{n_i}$$

  - Depends on doping level N_A
  - And intrinsic carrier concentration n_i
- γ = *body effect coefficient*

$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{si}N_A} = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

Body Effect Cont.

- For small source-to-body voltage, treat as linear

$$V_t = V_{t0} + k_\gamma V_{sb}$$

$$k_\gamma = \frac{\gamma}{2\sqrt{\phi_s}} = \frac{\sqrt{\frac{q\varepsilon_{si}N_A}{v_T \ln\frac{N_A}{n_i}}}}{2C_{ox}}$$

Body Effect Example

Example 2.5

Consider the nMOS transistor in a 65 nm process with a nominal threshold voltage of 0.3 V and a doping level of 8×10^{17} cm^{-3}. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 0.6 V instead of 0?

SOLUTION: At room temperature, the thermal voltage $v_T = kT/q = 26$ mV and $n_i = 1.45 \times 10^{10}$ cm^{-3}. The threshold increases by 0.04 V.

$$\phi_s = 2(0.026\ \text{V}) \ln \frac{8 \times 10^{17}\ \text{cm}^{-3}}{1.45 \times 10^{10}\ \text{cm}^{-3}} = 0.93\ \text{V}$$

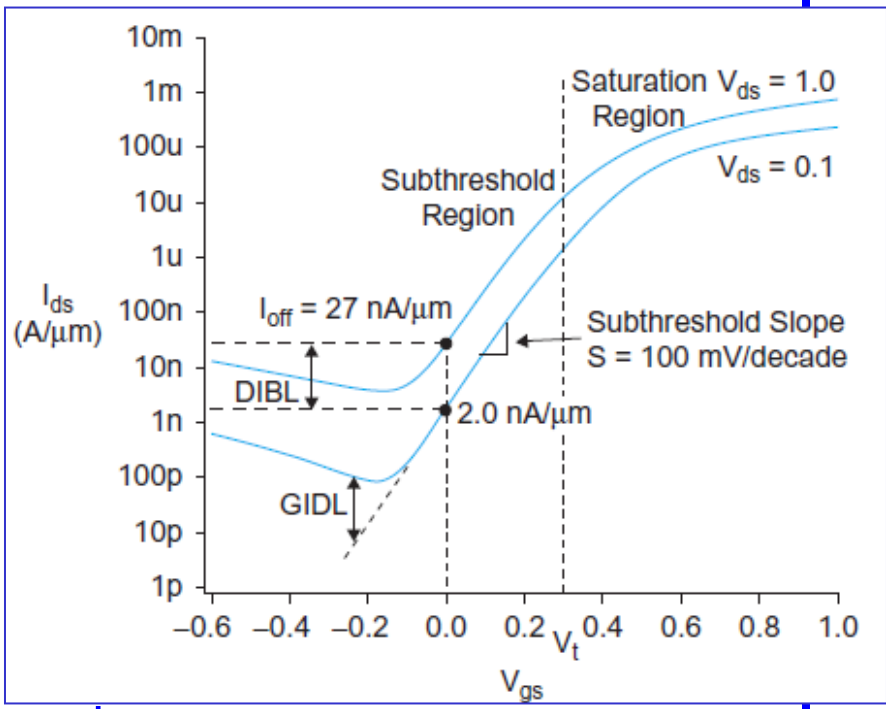
$$\gamma = \frac{10.5 \times 10^{-8}\ \text{cm}}{3.9 \times 8.85 \times 10^{-14}\ \frac{\text{F}}{\text{cm}}} \sqrt{2\left(1.6 \times 10^{-19}\ \text{C}\right)\left(11.7 \times 8.85 \times 10^{-14}\ \frac{\text{F}}{\text{cm}}\right)\left(8 \times 10^{17}\ \text{cm}^{-3}\right)} = 0.16$$

$$V_t = 0.3 + \gamma\left(\sqrt{\phi_s + 0.6\ \text{V}} - \sqrt{\phi_s}\right) = 0.34\ \text{V}$$

DIBL

- Electric field from drain affects channel
- More pronounced in small transistors where the drain is closer to the channel
- Drain-Induced Barrier Lowering
  - Drain voltage also affect V_t

$$V_t' = V_t - \eta V_{ds}$$



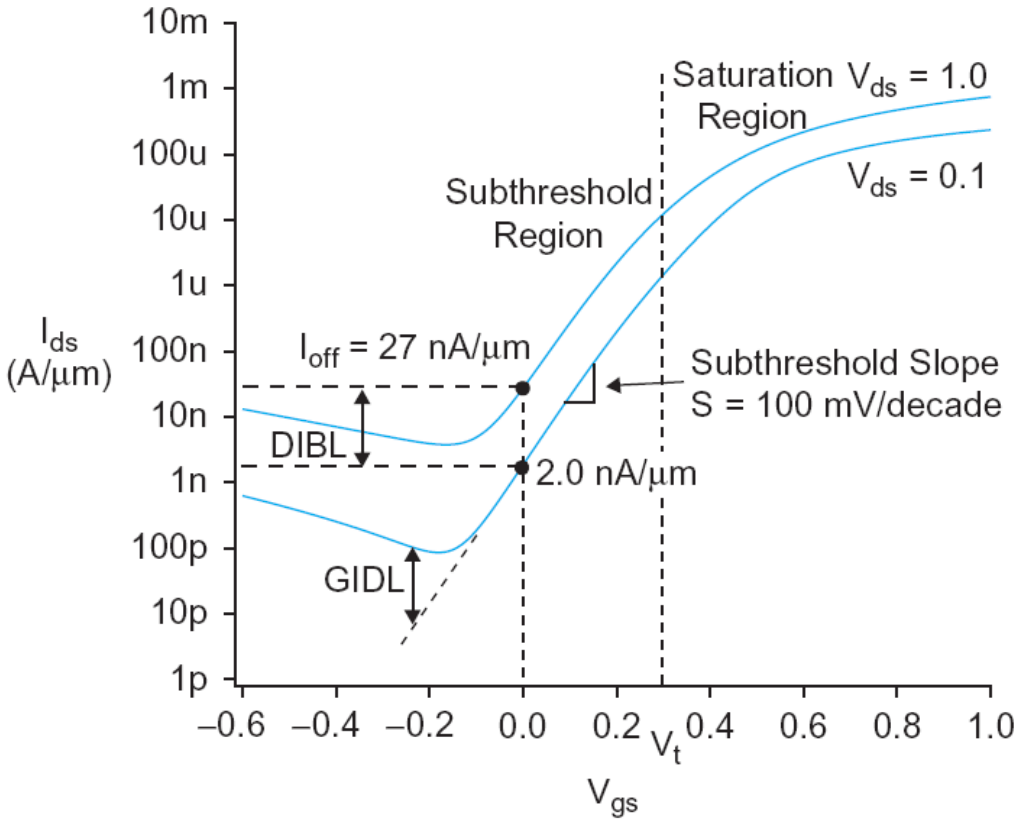
- High drain voltage causes current to increase.

Short Channel Effect

- In small transistors, source/drain depletion regions extend into the channel
  - Impacts the amount of charge required to invert the channel
  - And thus makes V_t a function of channel length
- Short channel effect: V_t increases with L
  - Some processes exhibit a reverse short channel effect in which V_t decreases with L

Leakage

- What about current in cutoff?
- Simulated results
- What differs?
  - Current doesn't go to 0 in cutoff



Leakage Sources

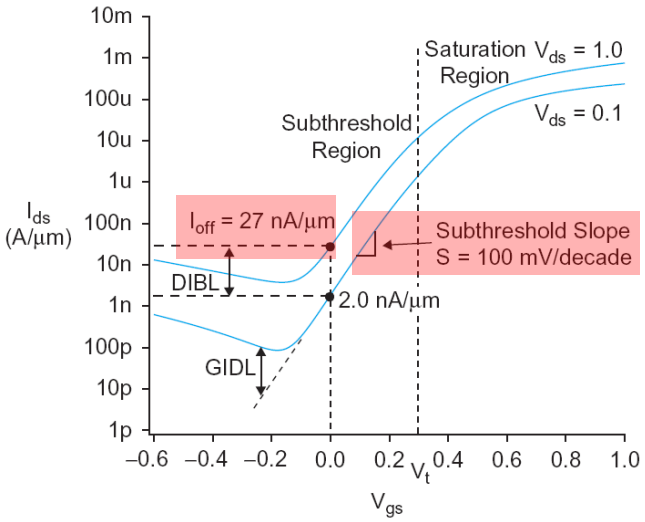
- Subthreshold conduction
  - Transistors can't abruptly turn ON or OFF
  - Dominant source in contemporary transistors
- Gate leakage
  - Tunneling through ultrathin gate dielectric
- Junction leakage
  - Reverse-biased PN junction diode current

Subthreshold Leakage

- Subthreshold leakage exponential with V_{gs}

$$I_{ds} = I_{ds0} e^{\frac{V_{gs} - V_{t0} + \eta V_{ds} - k_\gamma V_{sb}}{n v_T}} \left(1 - e^{\frac{-V_{ds}}{v_T}}\right)$$

- n is process dependent
  - typically 1.3-1.7
- Rewrite relative to I_{off} on log scale



$$I_{ds} = I_{off} 10^{\frac{V_{gs} + \eta(V_{ds} - V_{dd}) - k\gamma V_{sb}}{S}} \left(1 - e^{\frac{-V_{ds}}{v_t}}\right)$$

$$S = \left[\frac{d\left(\log_{10} I_{ds}\right)}{dV_{gs}}\right]^{-1} = n v_T \ln 10$$

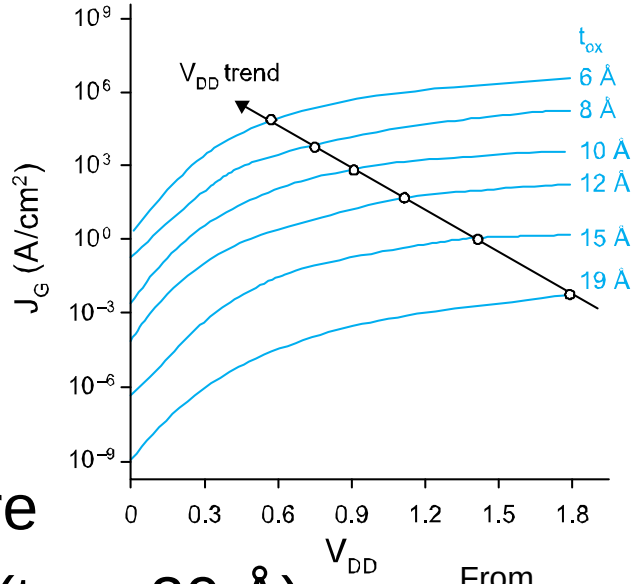
- S ≈ 100 mV/decade @ room temperature

Gate Leakage

- Carriers tunnel thorough very thin gate oxides
- Exponentially sensitive to t_{ox} and V_{DD}

$$I_{gate} = WA\left(\frac{V_{DD}}{t_{ox}}\right)^2 e^{-B\frac{t_{ox}}{V_{DD}}}$$

  - A and B are tech constants
  - Greater for electrons
    - So nMOS gates leak more



From [Song01]

- Negligible for older processes (t_{ox} > 20 Å)
- Critically important at 65 nm and below (t_{ox} ≈ 10.5 Å)

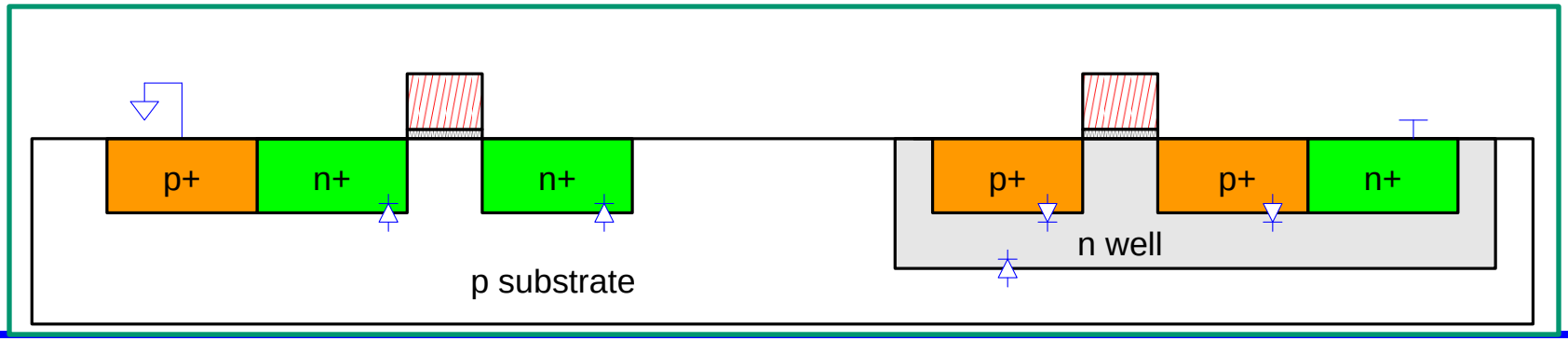
Junction Leakage

- Reverse-biased p-n junctions have some leakage
  - Band-to-band tunneling (BTBT)

BTBT occurs across the junction between the source or drain and the body when the junction is reverse-biased. It is a function of the reverse bias and the doping levels.

  - Gate-induced drain leakage (GIDL)

GIDL occurs where the gate partially overlaps the drain. This effect is most pronounced when the drain is at a high voltage and the gate is at a low voltage. GIDL current is proportional to gate-drain overlap area and hence to transistor width. It is a strong function of the electric field and hence increases rapidly with the drain-to-gate voltage.

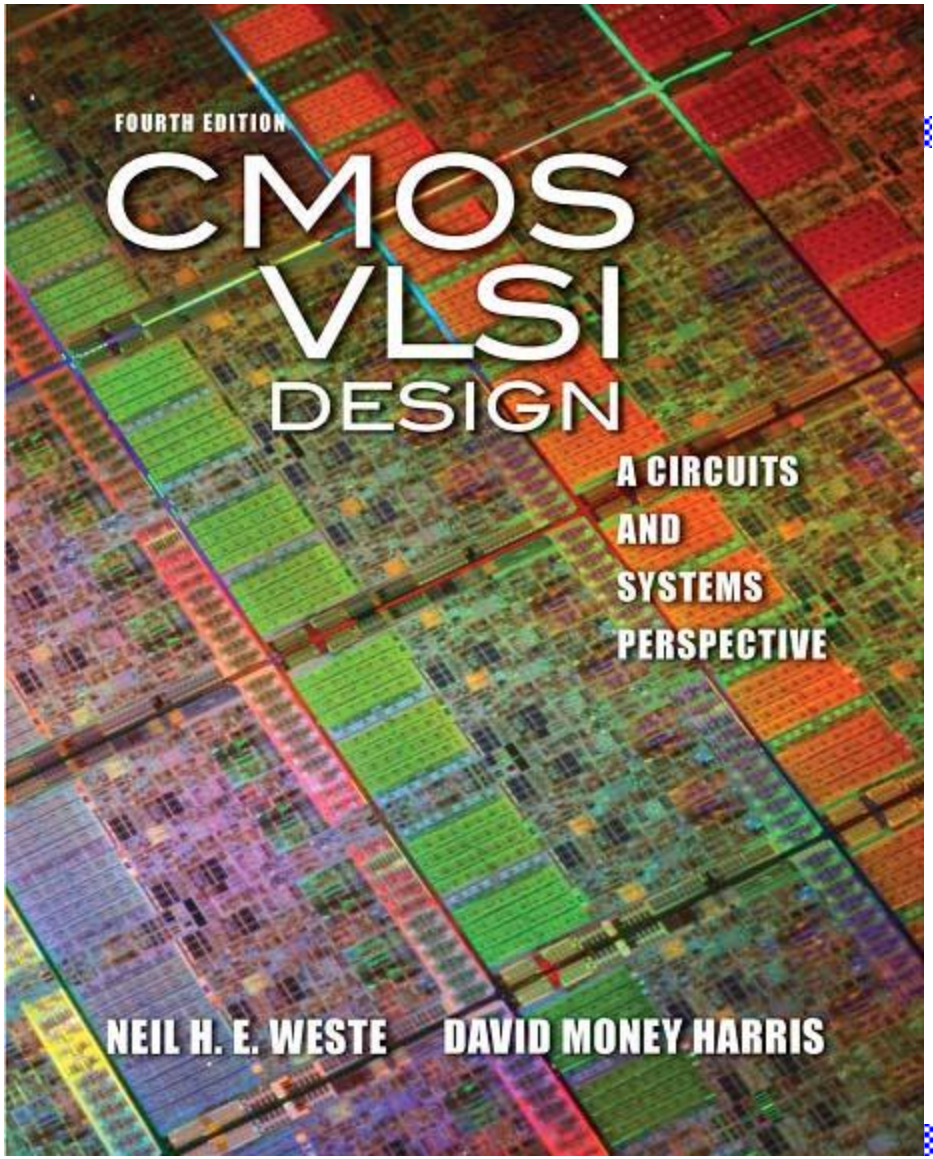


Diode Leakage

- Reverse-biased p-n junctions have some leakage

$$I_D = I_S \left(e^{\frac{V_D}{v_T}} - 1 \right)$$

- At any significant negative diode voltage, $I_D = -I_s$
- I_s depends on doping levels
  - And area and perimeter of diffusion regions
  - Typically < 1 fA/μm^2 (negligible)



DC Characteristics

Dr. Bassam Jamil

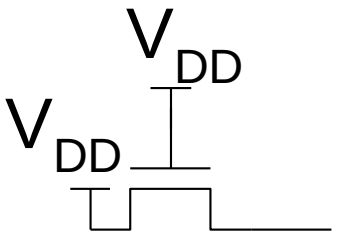
Adopted from slides of the textbook

Outline

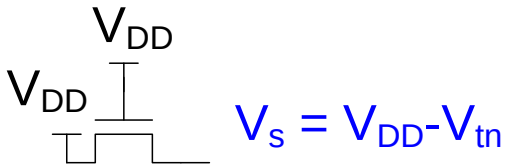
- Pass Transistors
- DC Response
- Logic Levels and Noise Margins
- Transient Response
- RC Delay Models
- Delay Estimation

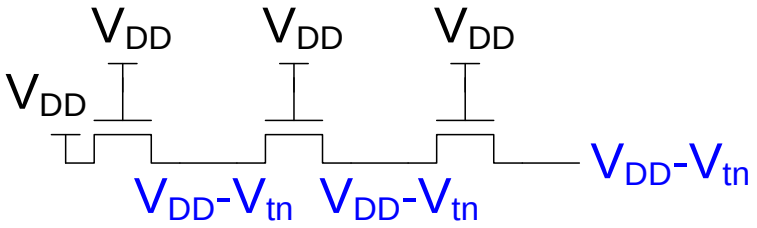
Pass Transistors

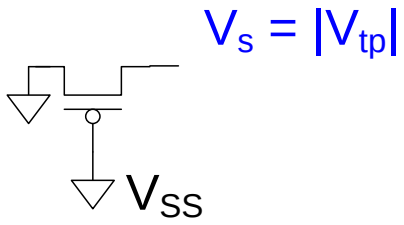
- We have assumed source is grounded
- What if source > 0?
  - e.g. pass transistor passing V_{DD}
- $V_g = V_{DD}$
  - If $V_s > V_{DD}-V_t$, $V_{gs} < V_t$
  - Hence transistor would turn itself off
- nMOS pass transistors pull no higher than $V_{DD}-V_{tn}$
  - Called a degraded "1"
  - Approach degraded value slowly (low I_{ds})
- pMOS pass transistors pull no lower than V_{tp}
- Transmission gates are needed to pass both 0 and 1

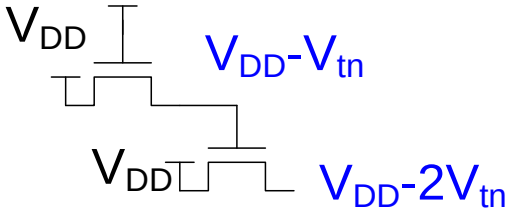


Pass Transistor Ckts



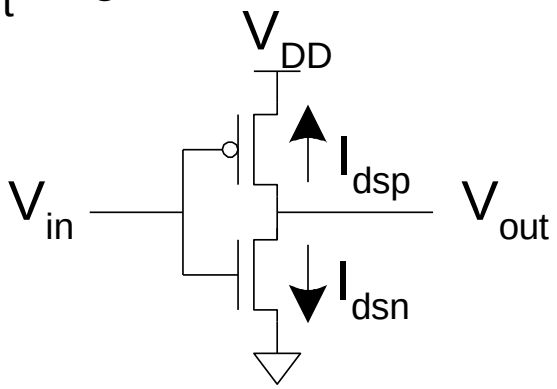






DC Response

- DC Response: V_{out} vs. V_{in} for a gate
- Ex: Inverter
  - When $V_{in} = 0$ -> $V_{out} = V_{DD}$
  - When $V_{in} = V_{DD}$ -> $V_{out} = 0$
  - In between, V_{out} depends on transistor size and current
  - By KCL, must settle such that $I_{dsn} = |I_{dsp}|$
  - We could solve equations
  - But graphical solution gives more insight

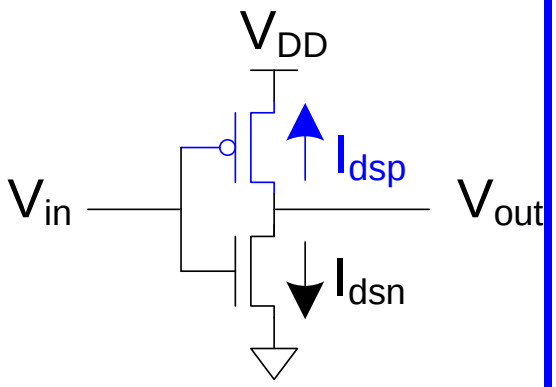


pMOS Operation

For PMOS: $V_{tp} < 0$

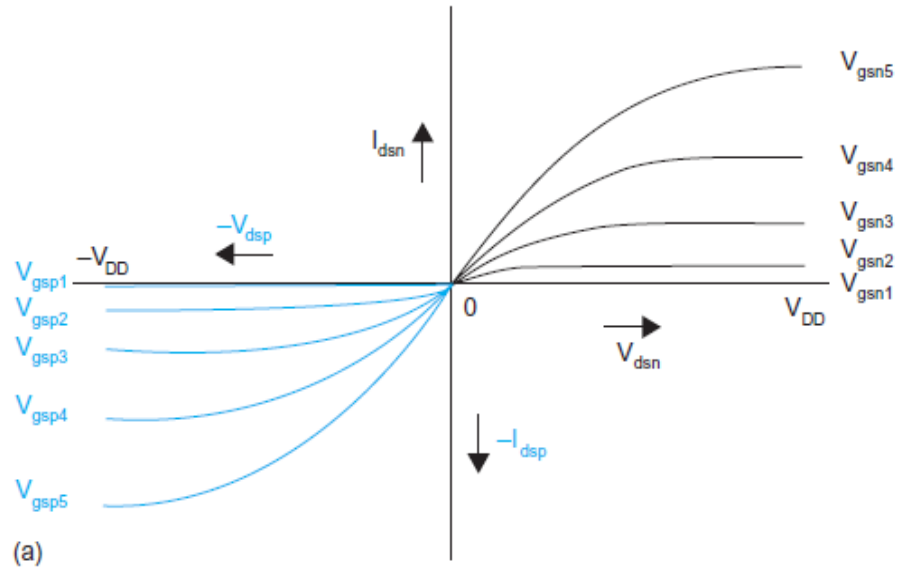
$$V_{gsp} = V_{in} - V_{DD} \quad , V_{dsp} = V_{out} - V_{DD}$$

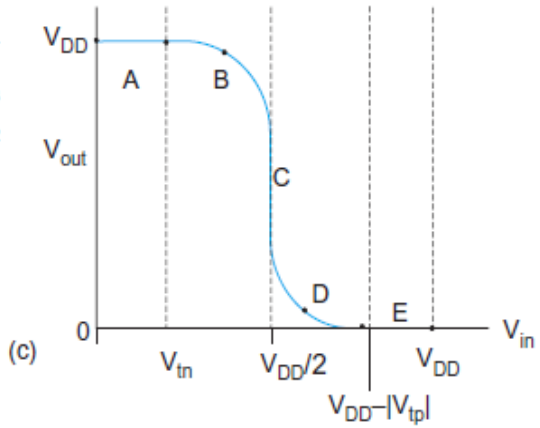
For NMOS: $V_{gsp} = V_{in}$, $V_{dsp} = V_{out} - V_{DD}$

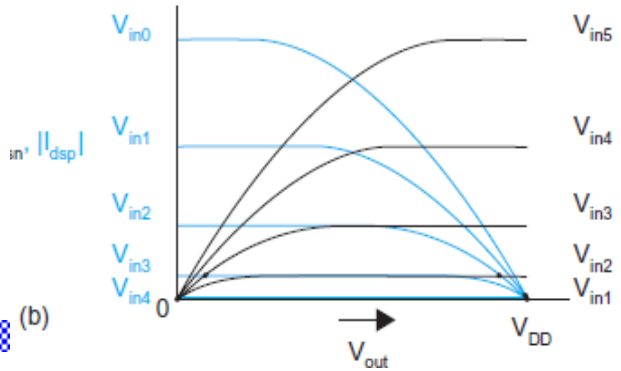


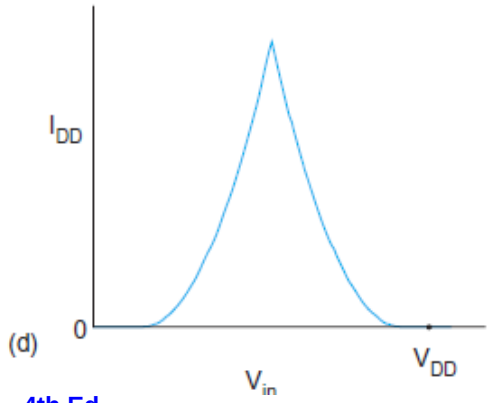
	Cutoff	Linear	Saturated
nMOS	$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$	$V_{gsn} > V_{tn}$
	$V_{in} < V_{tn}$	$V_{in} > V_{tn}$	$V_{in} > V_{tn}$
		$V_{dsn} < V_{gsn} - V_{tn}$	$V_{dsn} > V_{gsn} - V_{tn}$
		$V_{out} < V_{in} - V_{tn}$	$V_{out} > V_{in} - V_{tn}$
pMOS	$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$	$V_{gsp} < V_{tp}$
	$V_{in} > V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$
		$V_{dsp} > V_{gsp} - V_{tp}$	$V_{dsp} < V_{gsp} - V_{tp}$
		$V_{out} > V_{in} - V_{tp}$	$V_{out} < V_{in} - V_{tp}$

DC Characteristic



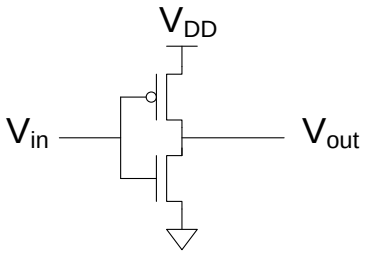




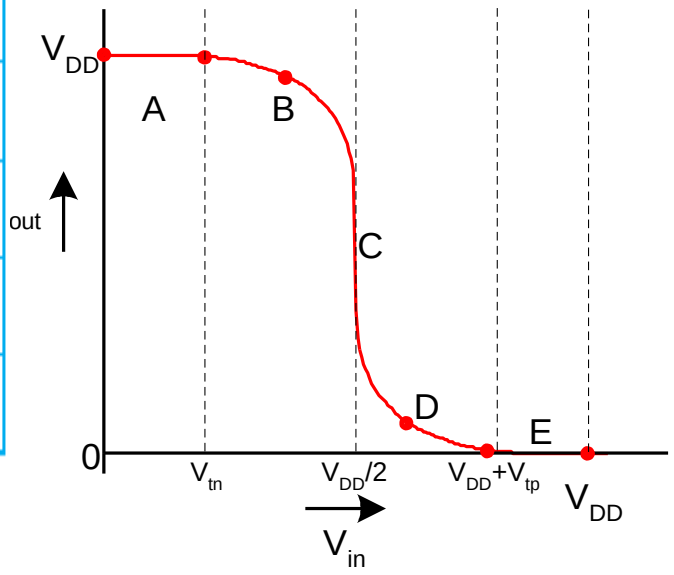


Operating Regions

- Revisit transistor operating regions
- Define input threshold (Vinv) as when
  Vinv=Vin=Vout



Region	Condition	p-device	n-device	Output
A	$0 \le V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \lvert V_{tp} \rvert$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \lvert V_{tp} \rvert$	cutoff	linear	$V_{out} = 0$



Calculate Vinv

$$I_{dn} = \frac{\beta_n}{2}\left(V_{\text{inv}} - V_{tn}\right)^2$$
$$I_{dp} = \frac{\beta_p}{2}\left(V_{\text{inv}} - V_{DD} - V_{tp}\right)^2 \qquad (2.54)$$

By setting the currents to be equal and opposite, we can solve for V_{inv} as a function of r:

$$V_{\text{inv}} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{1}{r}}}{1 + \sqrt{\frac{1}{r}}} \qquad (2.55)$$

In the limit that the transistors are fully velocity saturated, EQ (2.29) shows

$$I_{dn} = W_n C_{\text{ox}} v_{\text{sat}-n}(V_{\text{inv}} - V_{tn})$$
$$I_{dp} = W_p C_{\text{ox}} v_{\text{sat}-p}(V_{\text{inv}} - V_{DD} - V_{tp}) \qquad (2.56)$$

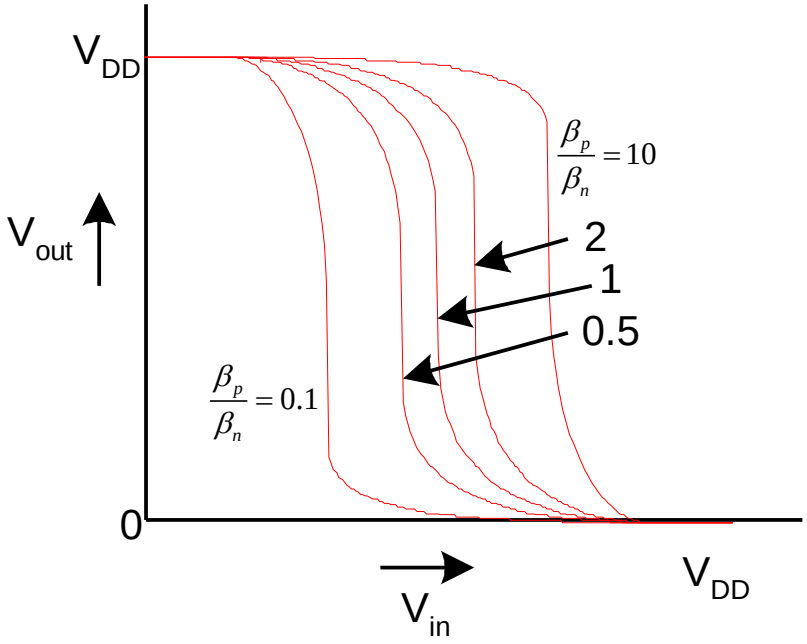
Redefining $r = W_p v_{\text{sat-}p} / W_n v_{\text{sat-}n}$, we can again find the inverter threshold

$$V_{\text{inv}} = \frac{V_{DD} + V_{tp} + V_{tn}\frac{1}{r}}{1 + \frac{1}{r}} \qquad (2.57)$$

In either case, if $V_{tn} = -V_{tp}$ and $r = 1$, $V_{\text{inv}} = V_{DD}/2$ as expected. However, velocity sat-

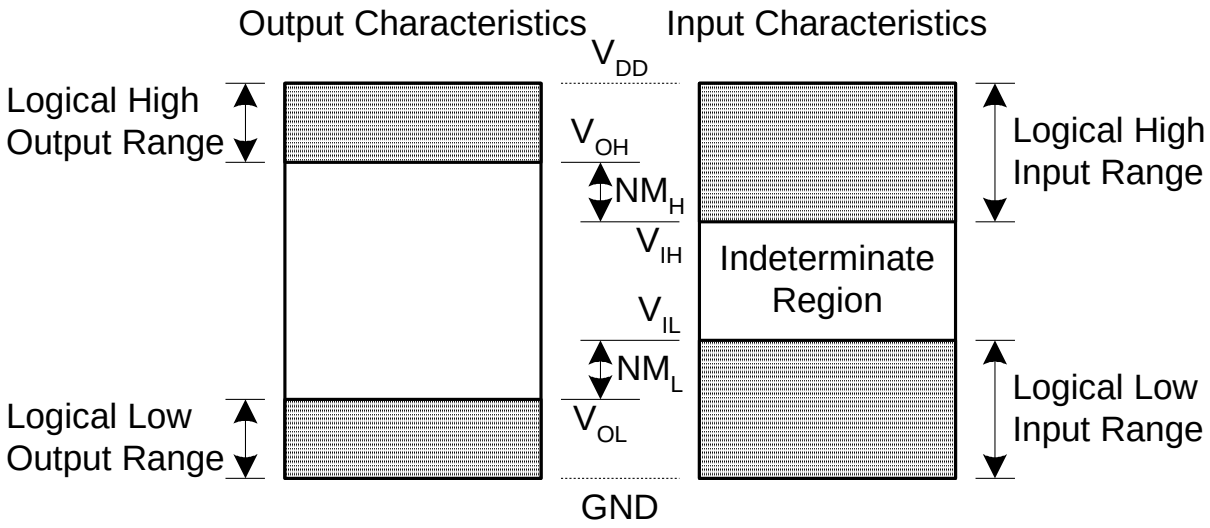
Beta Ratio

- If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed* gate
- Other gates: collapse into equivalent inverter



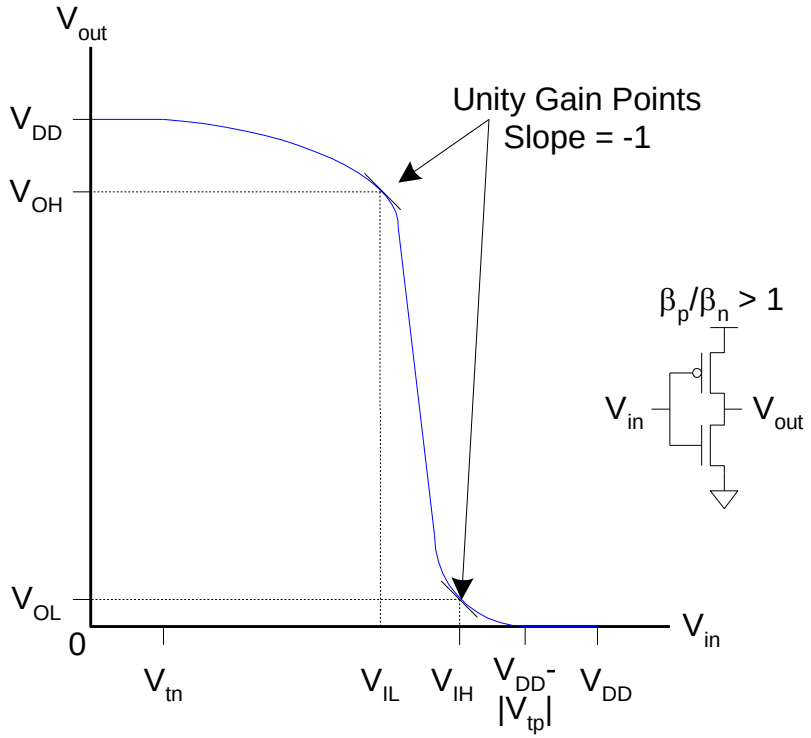
Noise Margins

- How much noise can a gate input see before it does not recognize the input?



Logic Levels

- To maximize noise margins, select logic levels at
  - unity gain point of DC transfer characteristic



$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$