Building Gates with Diodes and BJTs

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Introduction

- Acknowledgement: Most of the following slides were adopted from Dr. Anas Al-Trabsheh lecture notes.
- Topics
  - Basics of logic gates
  - Diodes and Diode-Resistor Logic
  - BJT
  - Resistor-Transistor Logic (RTL)
  - Transistor-Transistor Logic (TTL)
  - Emitter-Coupled Logic (ECL)

Logic Gates

The objective of digital electronics is to "build/implement logic gates" using basic circuit components.

Recall from digital logic class, the basic logic gates are: inverter, AND, OR, NAND, NOR.

Inverter

Vin	Vout
L	H
H	L

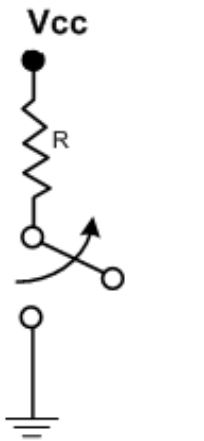
AND

Vin1	Vin2	Vout
L	L	L
L	H	L
H	L	L
H	H	H

OR

Vin1	Vin2	Vout
L	L	L
L	H	H
H	L	H
H	H	H

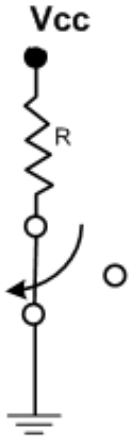
The Basics of Digital Gate Implementation



When : $V_I < V_{IL}$

$V_O = V_{OH}$

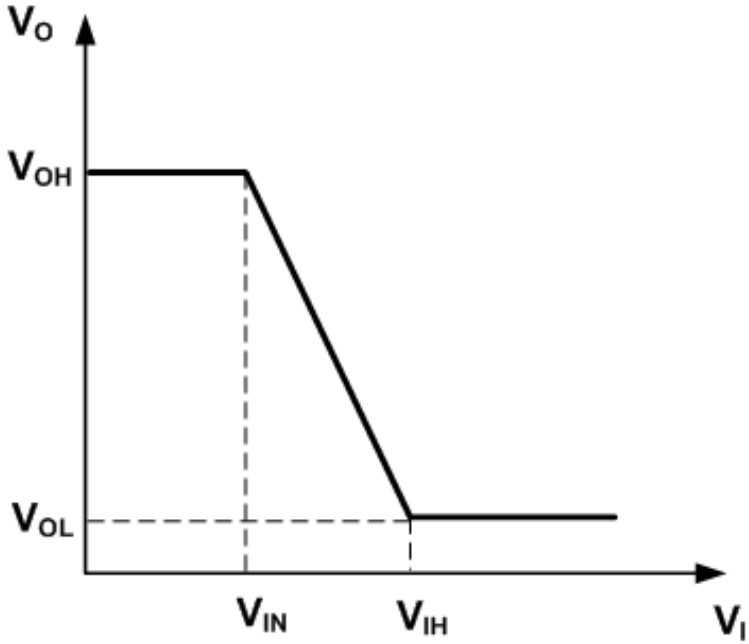
Usually: $V_{OH} = V_{cc}$



When : $V_I > V_{IH}$

$V_O = V_{OL}$

Usually: $V_{OL} \cong 0V$

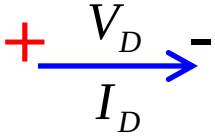


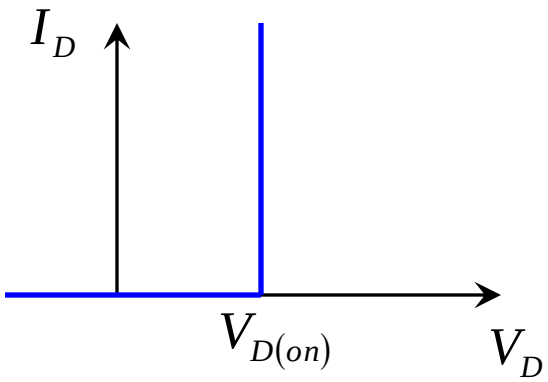
Transfer Characteristic

Diodes

- Allows current to pass in one direction
- Piecewise linear model:
  - Cutoff: $I_D = 0$ for $V_D < V_{D(on)}$
  - Conducting: $V_D = V_{D(on)}$ for $I_D > 0$

$V_{D(on)} = 0.7\,V$





Diode-Resistor Logic

- Consists only of diodes and resistors
- Performs AND and OR logic functions

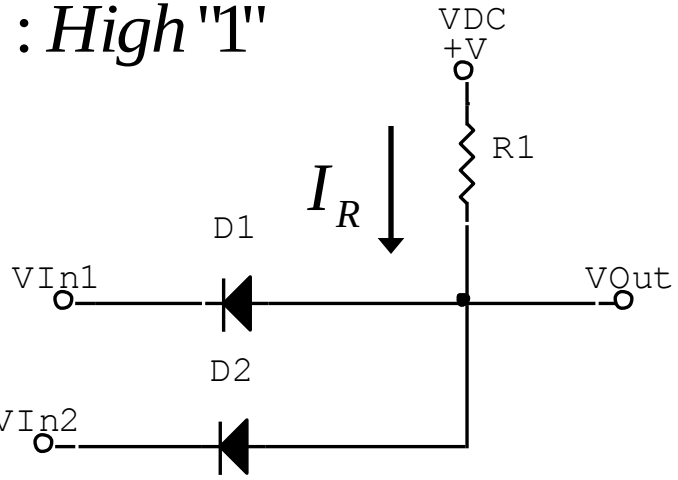
1. DRL AND gate

For $V_{in(1,2)} > V_{DC} - V_{D(ON)} \Rightarrow D_{(1,2)}$ is "OFF"

$$V_{in(1\&2)} : High\ "1" \Rightarrow V_{Out} = V_{DC} : High\ "1"$$

$$I_R = \begin{cases} 0; & \\ \text{when } \underline{\text{both}}\ \mathrm{D}_1 \text{ and } \mathrm{D}_2 \text{ are } OFF & \\ \left(V_{DC} - V_{D_{ON}} - V_{In}\right)/R_1; & \\ \text{when } \underline{\text{either}}\ \mathrm{D}_1 \text{ or } \mathrm{D}_2 \text{ is } ON & \end{cases}$$

V1	V 2	V o
L	L	L
L	H	L
H	L	L
H	H	H



Diode-Resistor Logic

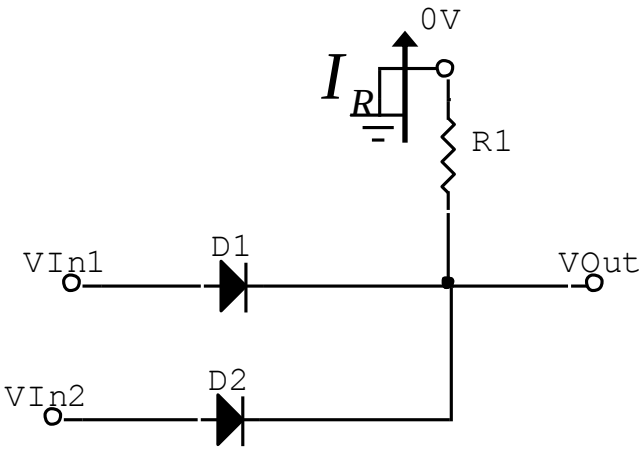
2. DRL OR gate

V1	V2	Vo
L	L	L
L	H	H
H	L	H
H	H	H

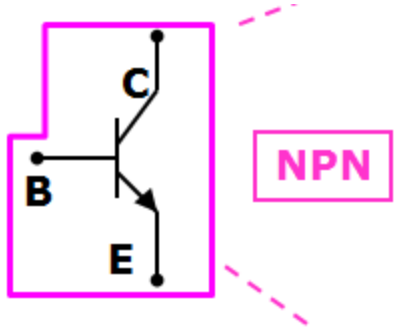
For $V_{in(1,2)} > V_{D(ON)} \Rightarrow D_{(1,2)}$ is "ON"

$V_{in(1\&2)} : Low"0" \Rightarrow V_{Out} = 0 : Low"0"$

$$I_R = \begin{cases} 0; \\ \text{when both } D_1 \text{ and } D_2 \text{ are } OFF \\ \left(V_{In} - V_{D_{ON}}\right)/R_1; \\ \text{when either } D_1 \text{ or } D_2 \text{ is } ON \end{cases}$$

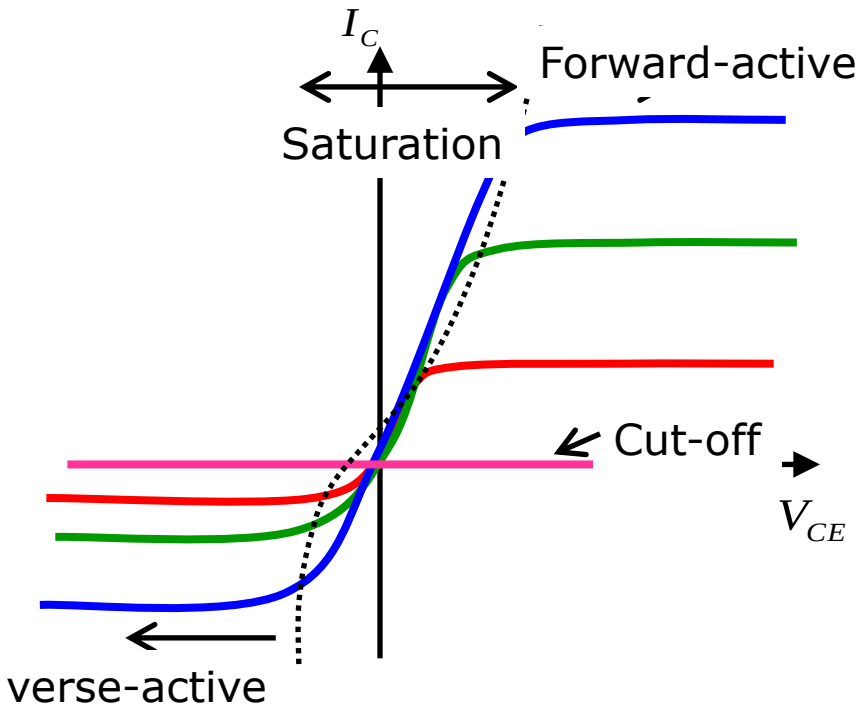


Bipolar Junction Transistor

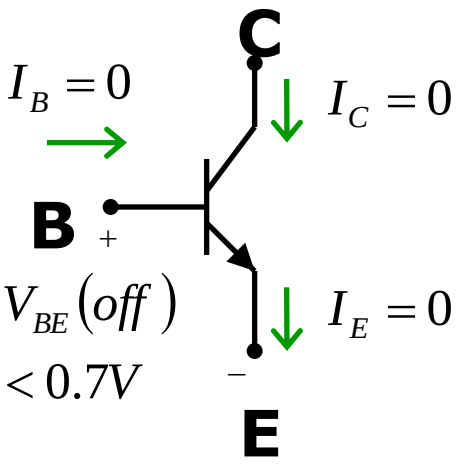


❑ MODES of operation

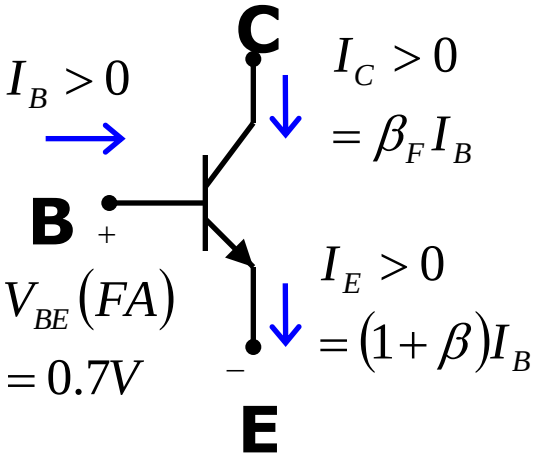
1. Cut-off mode:
   a) $V_{BE} < 0.7$ V
   b) transistor is off
   c) $I_B=I_C=I_E=0$
2. Forward-active mode:
   a) $V_{BE} = 0.7$ V
   b) $I_E= I_B+I_C$
   c) $I_C = \beta \times I_B$
3. Inverse-active mode
   a) $V_{BE} = 0.7$ V
   b) (see next slide)
4. Saturation mode
   a) $V_{BE} = 0.8$ V
   b) $V_{CE} = 0.2$ V
   c) $I_E= I_B+I_C$
   d) $I_C = \sigma\times \beta \times I_B$



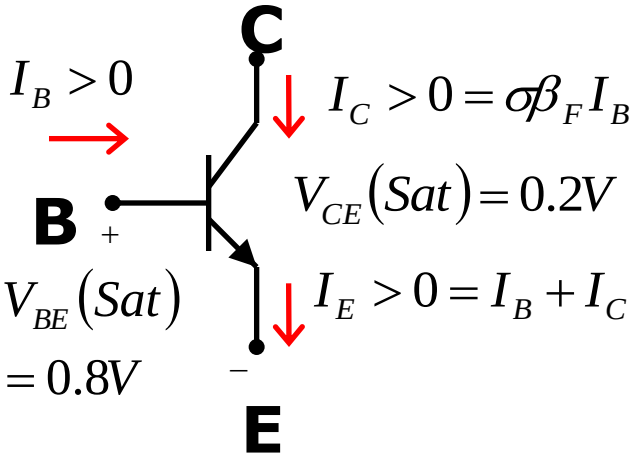
BTJ currents and voltages



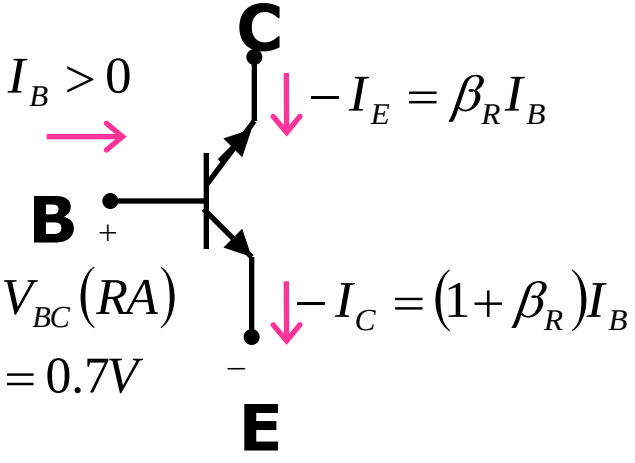
Cut-off Mode



Forward-Active Mode



Saturation Mode



Inverse-Active Mode

Resistor Transistor Logic (RTL) Inverter

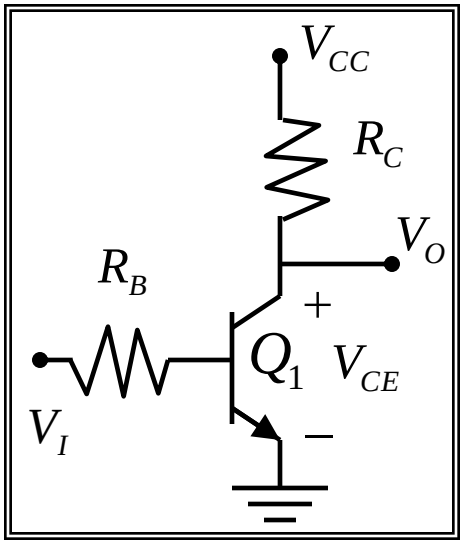
- Voltage-Transfer Characteristics

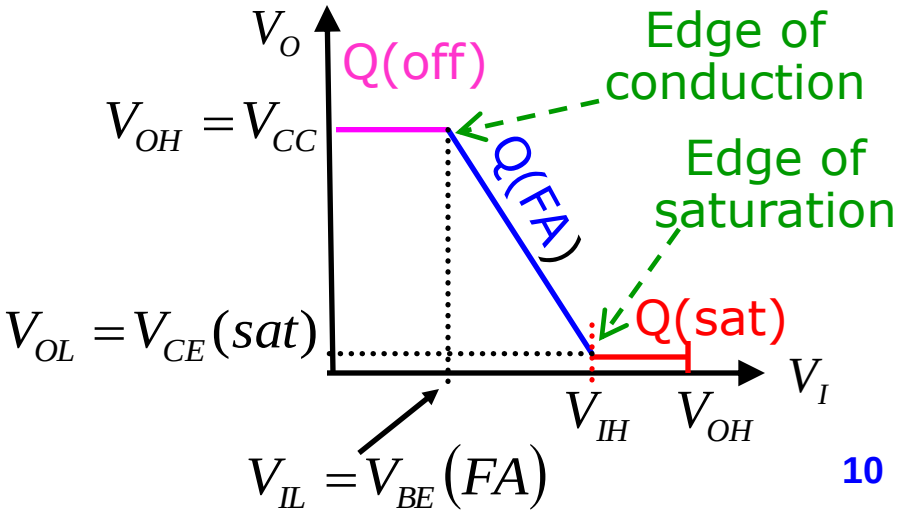
For $V_I - GND < V_{BE}(OFF)$ ⇒ $I_B=0, I_C=0, V_O=V_{CC}=V_{OH}$

For $V_I - GND \geq V_{BE}(FA)$ ⇒ $I_B=(V_I-V_{BE}(FA))/R_B, I_C=\beta_F I_B, V_O=V_{CC}-I_C R_C$

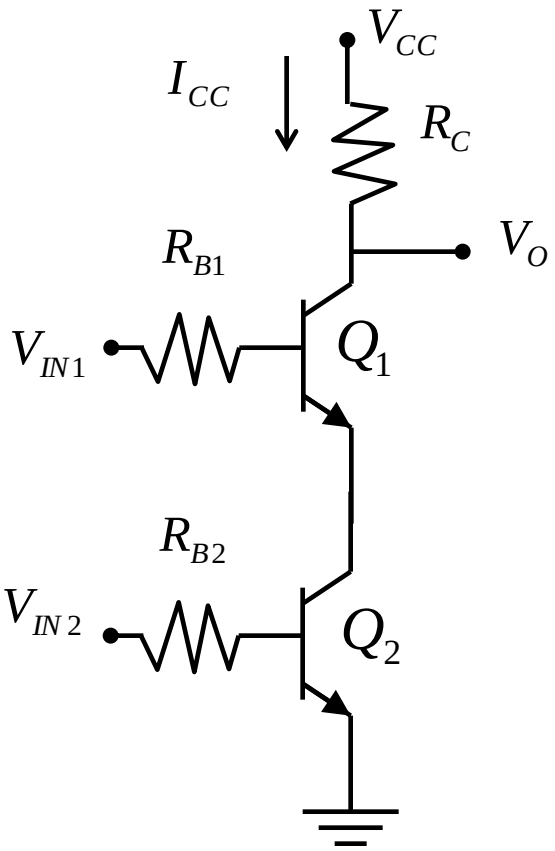
For $V_I - GND \geq V_{IH}$ ⇒

$I_B=(V_I-V_{BE}(sat))/R_B$
$I_C=(V_{CC}-V_{CE}(sat))/R_C$
$V_O=V_{CE}(sat)=V_{OL}$

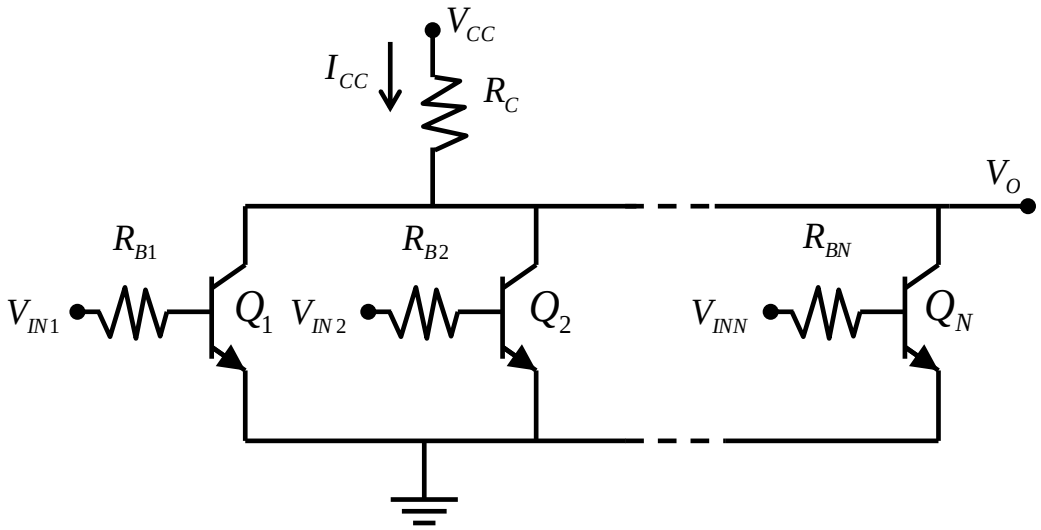




RTL : NAND and NOR Gates



NAND



NOR

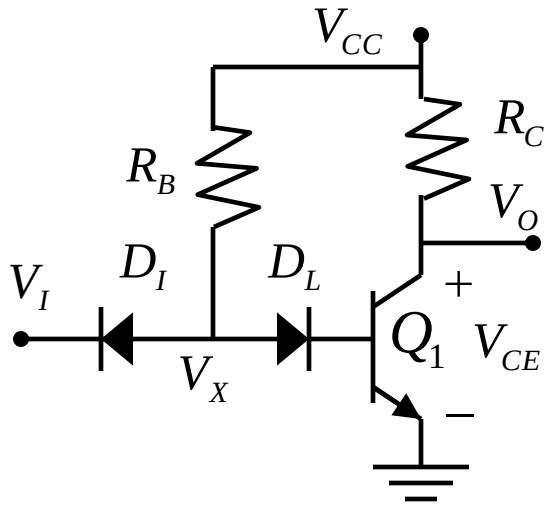
Diode-Transistor Logic (DTL)

For $V_I - V_{DI}(ON) + V_{DL}(ON) < V_{BE}(FA)$

$V_I < V_{BE}(FA)$ $\Rightarrow$ $V_X < V_{BE}(FA) + V_{DI}(ON)$

$V_{IL} = V_{BE}(FA)$ $\quad V_{OH} = V_{CC}$

D_I is ON,
D_L & Q_1 are OFF



For $V_I = V_{BE}(FA)$ $\Rightarrow$ D_I & D_L & Q_1 are ON (FA)

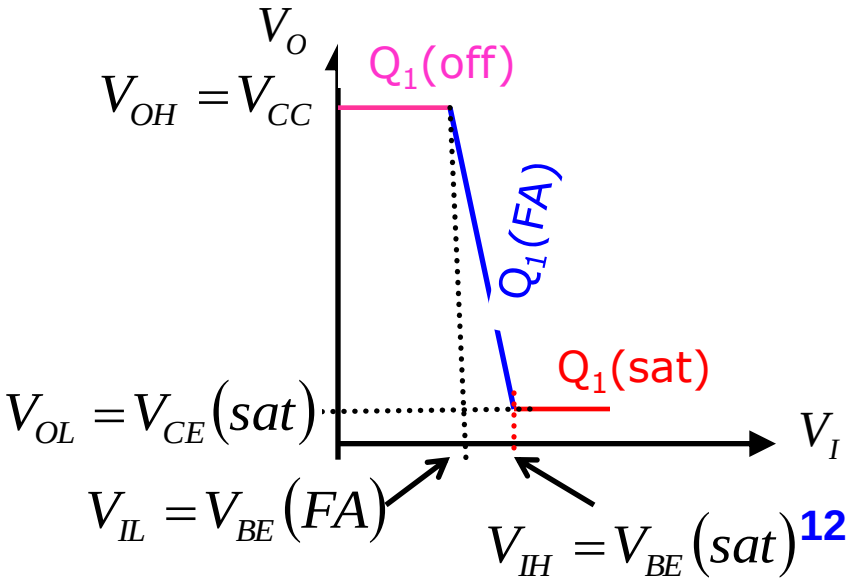
$V_X = V_{BE}(FA) + V_{DL}(ON)$

For $V_I - V_{DI}(ON) + V_{DL}(ON) = V_{BE}(sat)$

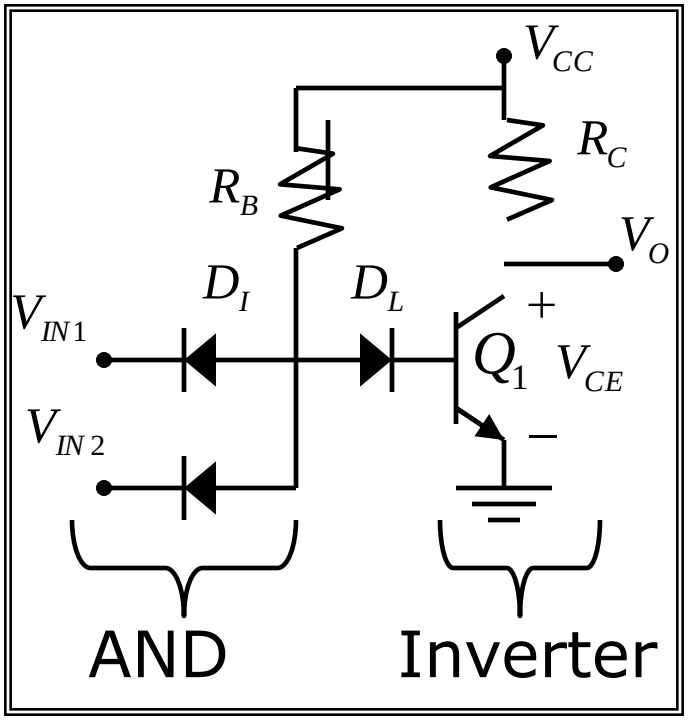
$V_{IH} = V_{BE}(sat)$

$V_I \geq V_{IH}$ $\Rightarrow$ D_I is OFF, D_L is ON, Q_1 is sat

$V_{OL} = V_{CE}(sat)$



DTL NAND Gate



If at <u>least one input</u> less than V_{BE}(FA), then Q_1 is off. i.e. I_{CC}=0

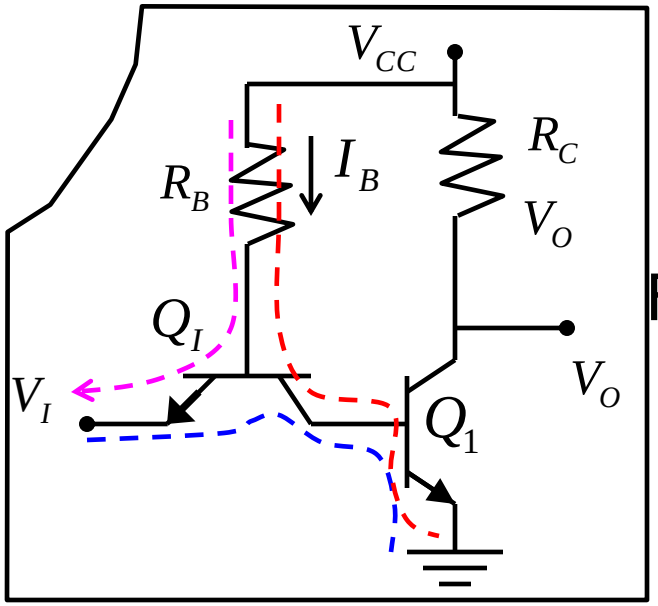
$$V_{OH} = V_{CC}$$

Transistor-Transistor Logic (TTL) Inverter

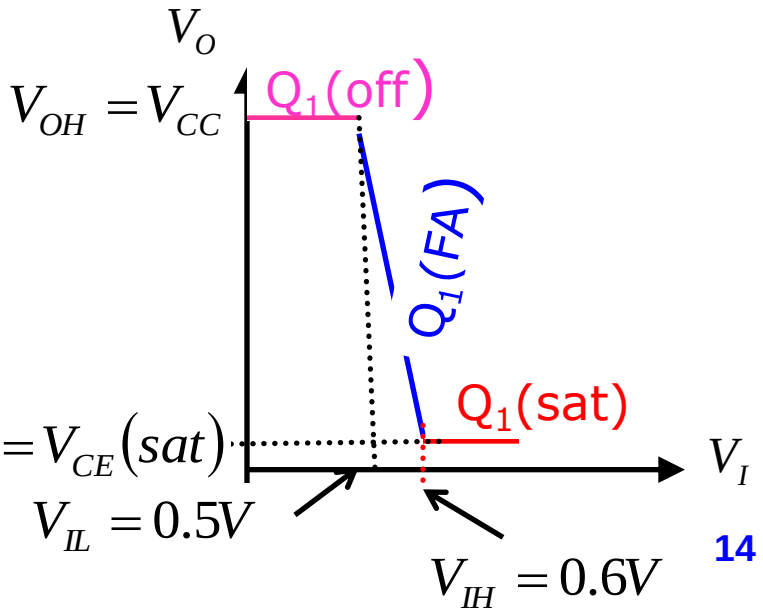
For
$V_I \le V_{IL} = V_{BE,1}(FA) - V_{CE,I}(sat)$ ⇒ BE of Q_I is forward-biased

$I_B = \dfrac{V_{CC} - V_{BE,I} - V_I}{R_B}$ For typical values of R_B, I_B is in mA, Q_I is sat.

$V_{BE,1} = V_{CE,I}(sat) + V_{IL}$ Q_1 is cut-off $\boxed{V_{OH} = V_{CC}}$



For $V_I \ge V_{IL}$ ⇒ Q_I is sat& Q_1 is FA

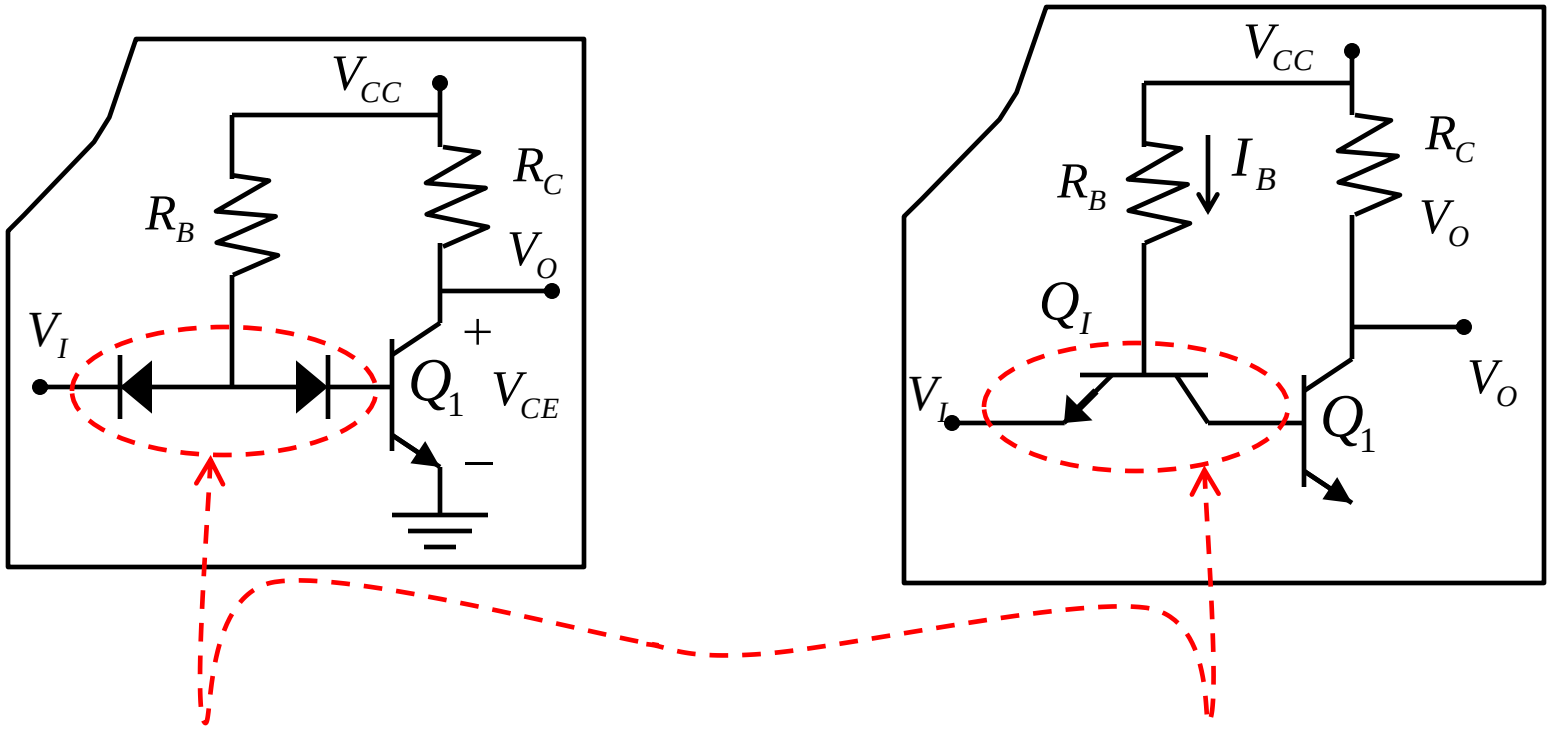


For
$V_I = V_{IH} = V_{BE,1}(sat) - V_{CE,I}(sat)$

$\boxed{V_{OL} = V_{CE}(sat)}$ ⇒ Q_1 is sat

For $V_I > V_{IH}$ BE of Q_I is reverse-biased
Inverse-active mode (RB)

DTL vs. TTL



- The input and level-shifting diodes are replaced by Q_I
- The Q_I BJT requires less area than the two diodes

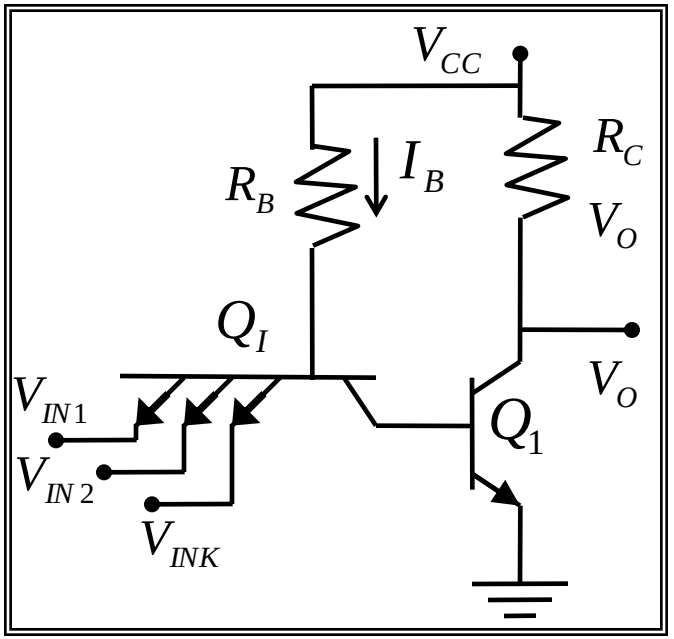
TTL NAND Gate

If at least one input is less than V_{IL}, then the Q_1 is off.

$$V_{OH} = V_{CC}$$

If all inputs are greater than V_{IH}, then the Q_1 is sat.

$$V_O = V_{CE}(sat)$$



Multiple-emitter BJT requires much less chip area than using individual transistors for each input

Emitter-Coupled Logic (ECL)

Emitter-Coupled Logic (ECL)

The BJTs in ECL circuits do not operate in saturation mode, but either in cut-off or forward-active modes

The ECL circuits are the fastest switching time of commercially digital circuits.

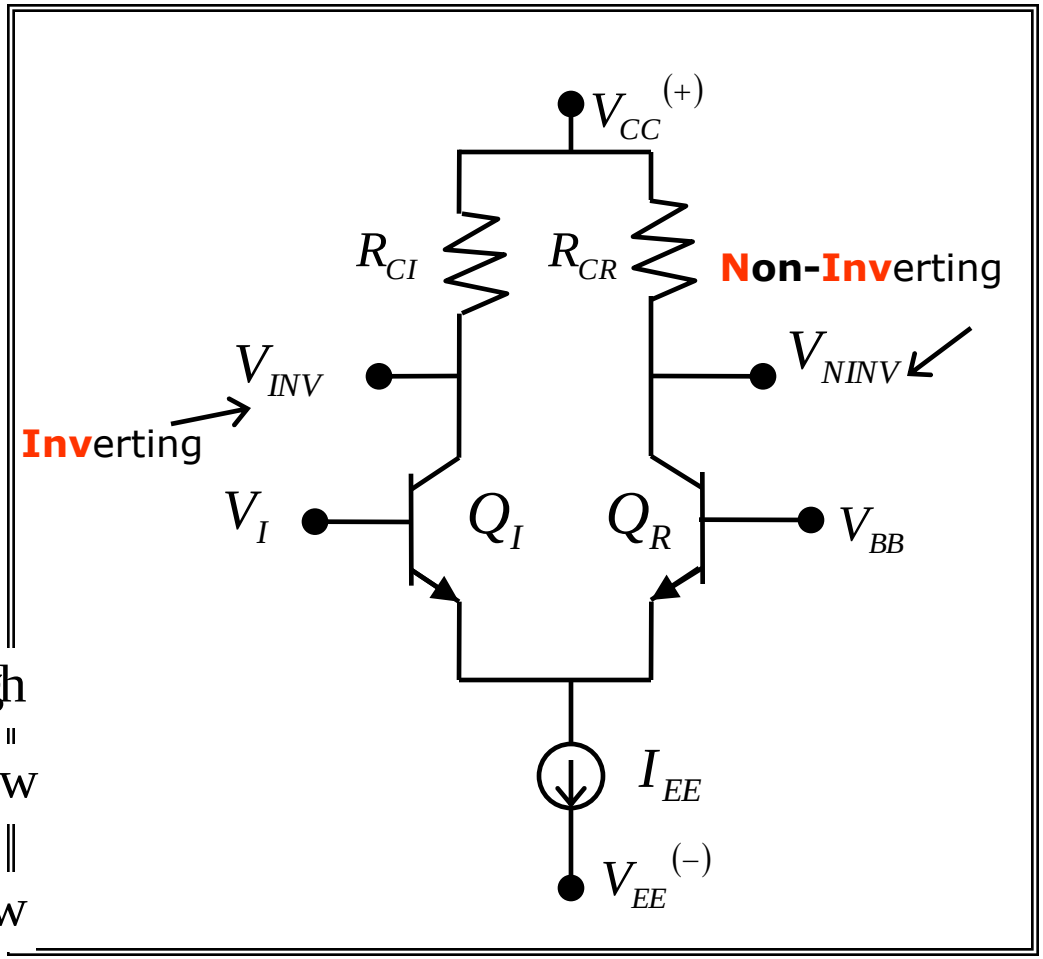
Typical propagation delay times are on the order of 1ns, allowing for clock frequencies up to 1GHz.

However, ECL circuits have the highest power dissipation of all logic families, typically 25mW per gate.

Basic ECL Current Switch

This figure shows an ideal BJT current switch

- The input is at the base of Q_I , and V_{BB} is a constant reference voltage
- The coupled emitters are ideally connected to a constant current source I_{EE}.



$V_I < V_{BB} \Rightarrow Q_I$ is OFF $\Rightarrow V_{INV}$ is High

Q_R is FA $\Rightarrow V_{NINV}$ is Low

$V_I > V_{BB} \Rightarrow Q_I$ is FA $\Rightarrow V_{INV}$ is Low

Q_R is OFF $\Rightarrow V_{NINV}$ is High

Resistor EC Current Switch

This figure shows an early ECL implementation

$$I_{RE} = \frac{V_E - V_{EE}}{R_E}$$

Outputs are taken at the collectors of Q_I and Q_R.

$$V_{O,1} = V_{INV} = V_{C,I} = V_{CC} - I_{C,I} R_{CI}$$

and

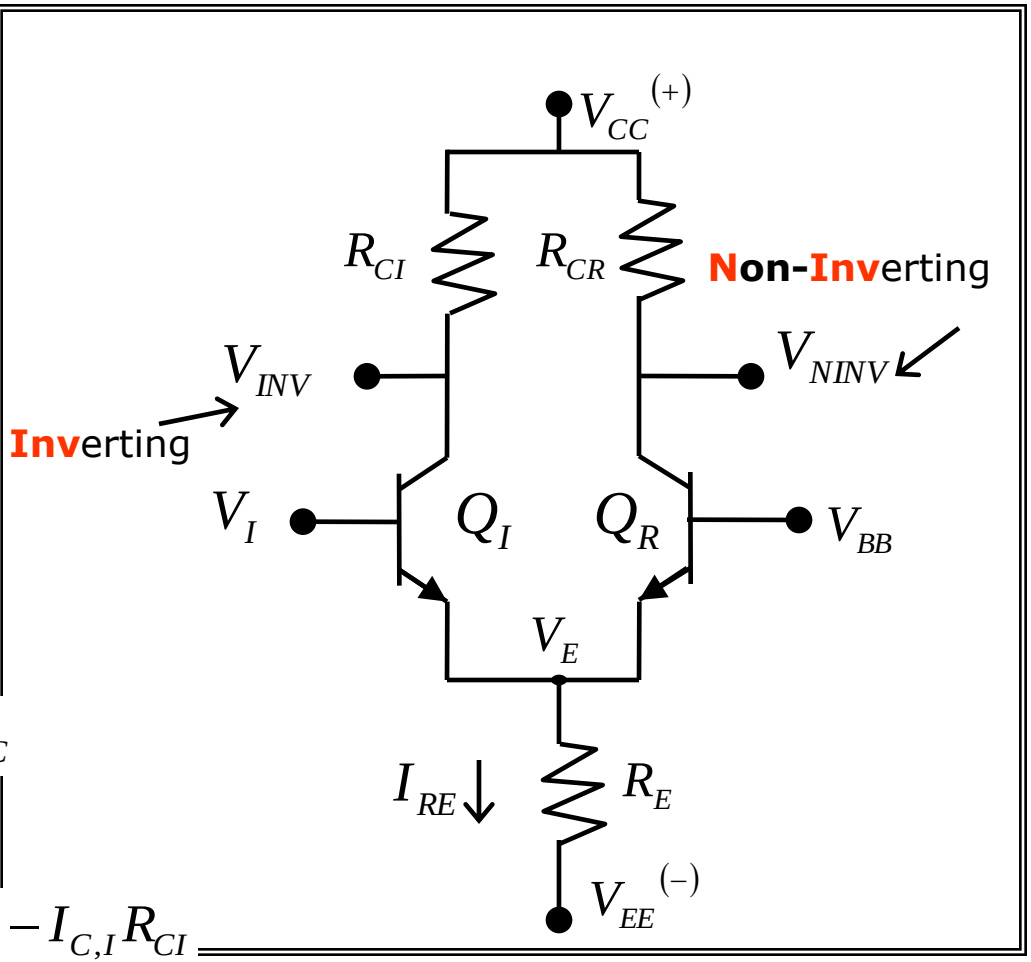
$$V_{O,2} = V_{NINV} = V_{C,R} = V_{CC} - I_{C,R} R_{CR}$$

$V_I < V_{BB} \Rightarrow Q_I$ is OFF $\Rightarrow$ $V_{INV} = V_{CC}$

$$V_{NINV} = V_{CC} - I_{C,R} R_{CR}$$

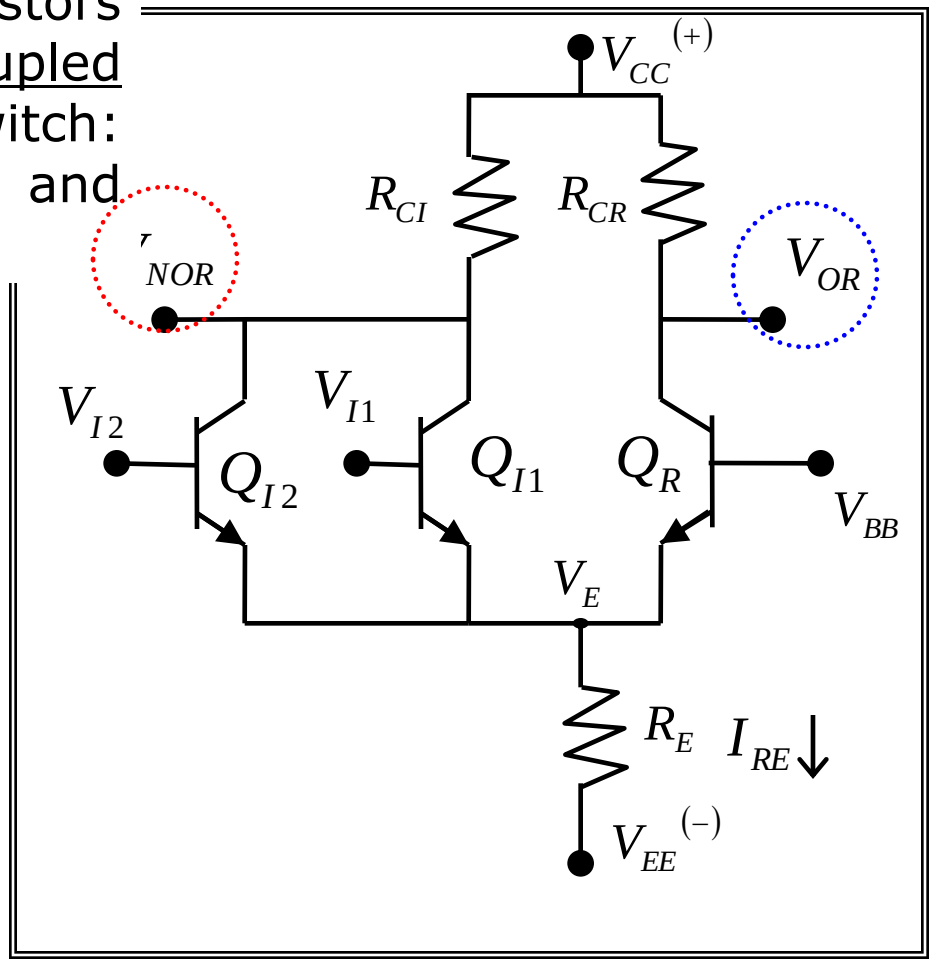
$V_I > V_{BB} \Rightarrow Q_I$ is FA $\Rightarrow$ $V_{INV} = V_{CC} - I_{C,I} R_{CI}$

$$V_{NINV} = V_{CC}$$



ECL NOR/OR Gate

Adding additional input transistors with coupled collectors and coupled emitters to the ECL current switch: V_{INV} becomes NOR output and V_{NINV} becomes OR output.



For any high-state input, the corresponding transistor is forward-active and then the corresponding collector current flows through R_{CI} and

$$V_{NOR} = V_{INV} = V_{CC} - I_{C,I} R_{CI} \quad (Low)$$

$$V_{OR} = V_{NINV} = V_{CC} \quad (High)$$

If all inputs are low, then all the corresponding transistors are cut-off and then

$$V_{NOR} = V_{INV} = V_{CC} \quad (High)$$

$$V_{OR} = V_{NINV} = V_{CC} - I_{C,R} R_{CR} \quad (Low)$$