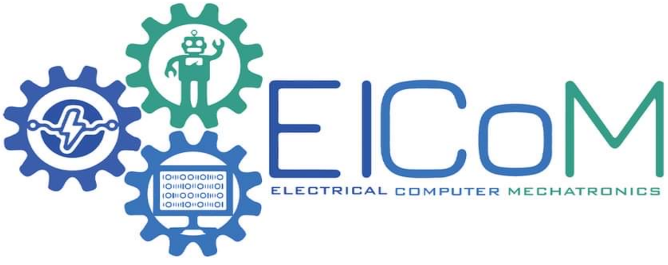

تقدم لجنة ElCoM الاكاديمية

دفتر لمادة:

الالكترونيات الرقمية والدوائر المتكاملة

من شرح:

بيان الخوالدة

جزيل الشكر للطالب:

بيان الخوالدة

Section 8.3.4 discusses SPICE perimeter capacitance models further.

The drain diffusion has a similar parasitic capacitance dependent on *AD*, *PD*, and V_{db}. Equivalent relationships hold for pMOS transistors, but doping levels differ. As the capacitances are voltage-dependent, the most useful information to digital designers is the value averaged across a switching transition. This is the C_{sb} or C_{db} value that was presented in Section 2.3.1.

Example 2.2

Calculate the diffusion parasitic C_{db} of the drain of a unit-sized contacted nMOS transistor in a 65 nm process when the drain is at 0 V and again at V_{DD} = 1.0 V. Assume the substrate is grounded. The diffusion region conforms to the design rules from Figure 2.8 with $\lambda = 25$ nm. The transistor characteristics are $CJ = 1.2\ \text{fF}/\mu\text{m}^2$, $MJ = 0.33$, $CJSW = 0.1\ \text{fF}/\mu\text{m}$, $CJSWG = 0.36\ \text{fF}/\mu\text{m}$, $MJSW = MJSWG = 0.10$, and $\psi_0 = 0.7$ V at room temperature.

SOLUTION: From Figure 2.8, we find a unit-size diffusion contact is $4 \times 5\ \lambda$, or $0.1 \times 0.125\ \mu\text{m}$. The area is $0.0125\ \mu\text{m}^2$ and perimeter is $0.35\ \mu\text{m}$ plus $0.1\ \mu\text{m}$ along the channel. At zero bias, $C_{jbd} = 1.2\ \text{fF}/\mu\text{m}^2$, $C_{jbdsw} = 0.1\ \text{fF}/\mu\text{m}$, and $C_{jbdswg} = 0.36\ \text{fF}/\mu\text{m}$. Hence, the total capacitance is

$$C_{db}(0\text{ V}) = \left(0.0125\mu\text{m}^2\right)\left(1.2\frac{\text{fF}}{\mu\text{m}^2}\right) + \left(0.35\mu\text{m}\right)\left(0.1\frac{\text{fF}}{\mu\text{m}}\right) + \left(0.1\mu\text{m}\right)\left(0.36\frac{\text{fF}}{\mu\text{m}}\right) = 0.086\text{ fF} \tag{2.21}$$

At a drain voltage of V_{DD}, the capacitance reduces to

$$C_{db}(1\text{ V}) = \left(0.0125\mu\text{m}^2\right)\left(1.2\frac{\text{fF}}{\mu\text{m}^2}\right)\left(1+\frac{1.0}{0.7}\right)^{-0.33} + \left[\left(0.35\mu\text{m}\right)\left(0.1\frac{\text{fF}}{\mu\text{m}}\right) + \left(0.1\mu\text{m}\right)\left(0.36\frac{\text{fF}}{\mu\text{m}}\right)\right]\left(1+\frac{1.0}{0.7}\right)^{-0.10} = 0.076\text{ fF} \tag{2.22}$$

For the purpose of manual performance estimation, this nonlinear capacitance is too much effort. An effective capacitance averaged over the switching range is quite satisfactory for digital applications. In this example, the effective drain capacitance would be approximated as the average of the two extremes, 0.081 fF.

Diffusion regions were historically used for short wires called *runners* in processes with only one or two metal levels. Diffusion capacitance and resistance are large enough that such practice is now discouraged; diffusion regions should be kept as small as possible on nodes that switch.

In summary, an MOS transistor can be viewed as a four-terminal device with capacitances between each terminal pair, as shown in Figure 2.13. The gate capacitance includes an intrinsic component (to the body, source and drain, or source alone, depending on operating regime) and overlap terms with the source and drain. The source and drain have parasitic diffusion capacitance to the body.

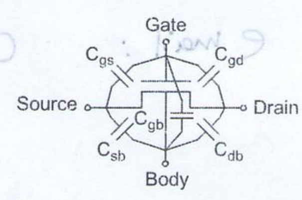

FIGURE 2.13 Capacitance of an MOS transistor

12

هام

ترتيب المادة حسب السلايدات
وليس حسب ترتيب الدكتور بسام
لأنه رح يعطي Ch.6 قبل Ch.5

تنصح بتصوير ورقة القوانين Cheatcheet
فقط اللازم نقلها بخط اليد أو تلخيصها
بنفسك عا ورقة واحدة بوجهين

٣. التركيز فقط عا أسئلة السلايدات لأنه بتيجي
بنفس تغيير الأرقام والتركيز عا الخط
والمفاهيم والمكونات.

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دعواتكم

BH

بيان الخالدي 1032945

nMos

linear $V_{gs} \geq V_t$ $\quad V_{ds} \leq V_{gs} - V_t$

sat $V_{gs} > V_t$ $\quad V_{ds} > V_{gs} - V_t$

$$I = \beta\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right] \text{ linear}$$

$$I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2 = \frac{\beta}{2}(V_{gt})^2$$

→ saturation pinches off $V_{gd} < V_t$

$V_{ds} > V_{dsat} = V_{gs} - V_t$

$Q = C \cdot V \Rightarrow I = C \frac{\Delta V}{\Delta t}$

pMos

$V_{gs} > V_t \Rightarrow$ off

$V_{gs} < V_t$ on

$V_{ds} > V_{gs} - V_t$. linear

$V_{ds} \leq V_{gs} - V_t$ saturation

$C_g = \frac{\varepsilon_{ox}}{t_{ox}} WL \Rightarrow$ gate capac.

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \Rightarrow$ $\boxed{C_g = C_{ox} WL}$

$\beta = \mu \frac{\varepsilon_{ox}}{t_{ox}} \frac{W}{L} = \mu C_{ox} \frac{W}{L}$

Voltage cross channel $= V_{gc} - V_t$

$= \left(V_{gs} - \frac{V_{ds}}{2}\right) - V_t$

$\mu = \frac{cm^2}{V \cdot s} = 350$

$\varepsilon_{ox} = 3.9 \times 8.85 \times 10^{-14}$ F/cm

$F = A/V$

$\lambda = 25\,nm$ $\quad$ $Å = 10^{-10}\,m = 10^{-8}\,cm$

$t_{ox} = 10.5\,Å$

short channel $L < 0.25\,\mu m$

$V_{ds\,sat} < V_{gs} - V_t$

long $\geq 0.25\,\mu m$ $\quad V_{dsat} = V_{gs} - V_t$

$M_p = \frac{M_n}{2}$ $\quad V_{tp}$ = negative

gate Capacitance :

$C_0 = C_{ox} WL$

Cut off

$C_{gb} = C_0$

linear $= S + D = C_{gs} + C_{gd} = C_0$

saturation $= \frac{2}{3} C_0$

$C_{gs} = \frac{\varepsilon_{ox}}{t_{ox}} WL = C_p W$ $\quad C_p = \frac{\varepsilon_{ox}}{t_{ox}} L$

$C_p = 2\,fF/\mu m$

C_{sb} = bottom + body + sidewall

$= AS * C_{jbs} + P C_{jbssw} + W C_{jbsswg}$

A: area

$A = W * D / W \times S = 20\lambda^2 = 0.0125\,\mu m^2$

$C_{jbss} = C_{jb}\left[1 + \frac{V_{sb}}{\Psi_0}\right]^{-M_j}$

$\Psi_0 =$

$C_{jbssw} = C_{jsw}\left(1 + \frac{V_{sb}}{\Psi}\right]^{-M_{jsw}}$

$P = \left.\begin{matrix} W + 2D \\ W + 2S \end{matrix}\right] = 14\lambda = 0.35\,\mu m$

$C_{jbsswg} = C_{jswg}\left(1 + \frac{V_{SB}}{\Psi_{swg}}\right]^{-M_{jswg}}$

$W = 4\lambda = 0.1\,\mu m$

$W = 4\lambda$ $\quad D = S = 5\lambda$

$L = 2\lambda$

non Ideal

$$I = \frac{\beta}{2}(V_{gs} - V_t)^2(1 + \lambda V_{ds})$$

$\lambda = 0.09$

$V_t = f\sqrt{V_{SB}}$

nominal → $V_{SB} = 0$

$E = \frac{V}{L} = \frac{V_{gs}}{t_{ox}} = \frac{V_{ds}}{L}$

$K = \beta = \frac{W}{L} K' = \frac{W}{L} \beta'$

ratio $= \frac{\beta_p}{\beta_n}$

First اولى

1032945 بيان الخوالدة

tempreture / body effect

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{SB}} - \sqrt{\phi_s}\right)$$

ϕ : surface potential

$$\phi = 2 v_t \ln \frac{N_A}{n_i}$$

N_A : doping level

$n_i = 1.45 \times 10^{10}\ cm^{-3}$

$v_t = 26\,mV$

$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}} \sqrt{2 q \varepsilon_{si} N_A}$$

DIBL

$$V_{t\,new} = V_{t_{old}} - n V_{ds}$$

$$I_{dn} = \frac{\beta_n}{2}(V_{inv} - V_{tn})^2$$

$$I_{dp} = \frac{\beta_p}{2}(V_{inv} - V_{DD} - V_{tp})^2$$

$$r = \frac{W_p\, V_{sat}}{W_n\, V_{sat\text{-}n}}$$

$$V_{inv} = \frac{V_{DD} + V_{tp} + V_{tn}\frac{1}{r}}{\frac{1}{r} + 1}$$

$V_{inv} = \frac{V_{DD}}{2}$ $\quad r = 1 \quad V_{tn} = -V_{tp}$

$$I_p = I_s\left(e^{\frac{V_D}{V_t}} - 1\right)$$

$$I_{ds} = I_0\left(e^{\frac{-V_t}{n v_t}}\right)$$

$NM_H = V_{OH} - V_{IH}$ $\quad V_{DD} - V_{IH}$

$NM_L = V_{IL} - V_{OL}$ $\quad V_{OL} = 0$

delay = RC

$$V_{out} = V_{DD}\, e^{-t/\tau}$$

$\ln 2 = 0.69$

$t_{pd} = RC \ln 2 = RC$

$t_{pd} = (3 + 3m) RC$ inverter

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Second ثاني

Ch.5

$\frac{W}{L} = \frac{4\lambda}{2\lambda}$

$V_{out} = V_{DD} e^{-t/\tau}$

$t_{pd} = RC$

$d = f + P$

$f = g \cdot h$

$h = \frac{C_{out}}{C_{in}}$

$g = \frac{\text{Capacitance of 1 input}}{\text{Inverter capac}}$

$\tau = 3RC$

Nand $= \frac{n+2}{3}$, NOR $= \frac{2n+1}{3}$

Ring

$T = 2Nd$ N: stages $h=1$

$d=2$

$f = \frac{1}{T \cdot \tau}$ $T = 2Nd$

FO4 inverter

delay $= d * \tau$ = second

Ring :

$T = 2Nd$

$= 4N\tau$ $\because d = 2\tau$

multi-stage

$G = \prod g_i$

$H = \frac{C_{out}}{C_{in}}$

$P = P_1 + P_2 + \cdots P_N$

$d_i = f_i + P_i$

$F = \prod g_i h_i = \prod \hat{f}_i = (\hat{f}_i)^N$

$F = GHB$

$HB = \prod h_i$

$D = N\hat{f} + P = D(F)^{1/N} + P$

Branch

$B = \prod B_i$

$F = GHB \Rightarrow H = \frac{C_{out\ final}}{C_{first}}$

$BH = \prod h_i$

effort delay $= N\hat{f}$

intrinsic delay $= \sum P_i$

Total $= N\hat{f} + P$

---

sizing :

$\hat{f} = g \cdot h \Rightarrow$

$\hat{f} = g \cdot \frac{C_{out}}{C_{in}}$

---

best number :

$\hat{f} = 4$

$F = (\hat{f})^N$ by log assume $N = 3$

$D = 3 \times \hat{f} + (NP)$ N if inv

$N = \log_4 F$

Ch.6

$t_{pdf} = P + 1$

$t_{pdr} = (P+1)\frac{(\mu)}{P}$

least $P_{delay} = \sqrt{\mu}$

$\mu = \frac{\mu_p}{\mu_n} = 2$

Ch.7

Total power = dynamic + static

$P = I \cdot V$

$P = \frac{E}{Time}$

$E = Area = \int_0^T p(t)\, d(t)$

$P_{avg} = \frac{1}{T}\int_0^T p(t)\, dt$

$P = I^2 R = \frac{V^2}{R}$

$E_C = \frac{1}{2} C V_C^2$, $E_{diss} = C \cdot V_{DD}^2$

↓ stored

$P = \frac{E}{T} = E \cdot f$

$P_{switching}$: dynamic

$P = \alpha\, C \cdot V_{DD}^2 \cdot f$

$E = [P \cdot T]$

* dynamic power =

$\left[\alpha C_{mem} + \alpha C_{Logic}\right] V_{DD}^2\, f$

Probability: α

$P_i = 1 - \overline{P_i}$

$\alpha_i = P_i * \overline{P_i}$

$AND_2 = P_A P_B$

$Nand_2 = 1 - and_2 = 1 - P_A P_B$

$NOR_2 = \overline{P_A}\,\overline{P_B}$

$OR_2 = 1 - NOR = 1 - \overline{P_A}\,\overline{P_B}$

$XOR_2 = P_A \overline{P_B} + \overline{P_A} P_B$

Static power

W → high / normal

$W = no. \times \lambda \times 0.025 \times 10^{-6} \times \%$ (النسبة)

$I_{sub} = W \times V_{t_{sub}} \times off\ \%$

$I_{gate} = W_{total} \times V_{t_{gate}} \times ON\ \%$

$I_{junct} = W_{total} \times V_{t_{junc}}$

Total $Leakage = I_{sub} + I_{gate} + I_{jun.}$

power = Leakage $\times V_{DD}$

Digital electronic
Digital integreted ccts

DIC

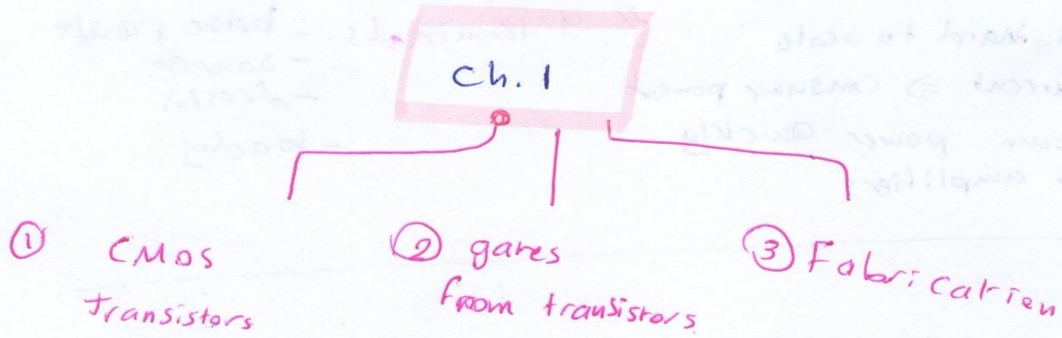
Ch.1 + Ch.2

Ch. 1
+ Ch. 2

⇒ integrated ccts: ⇒ many transistors on one chip.

VlSI : Very large Scale integration

Metal oxide Semiconductor : - Fast, cheap
SiO_2 - low power transistors



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miniaturization :
↳ most important achievement in DIC

تصغير ، تقليل الحجم

- Faster
- Smaller
- Cheap : less cost
- less power
- more transistors per chip

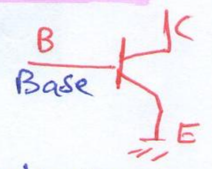
⇒ enhance performance

Moore's low : # transistors double every 18 months
⇒ every 1 year & half

Transistors Types

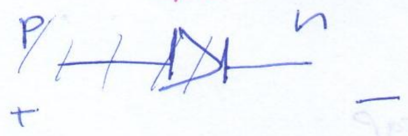
BJT

or Bipolar — Bipolar



npn
pnp

→ old technology
→ Current driven
depenet on Current to perform operation



→ C
→ E

* 2 terminals

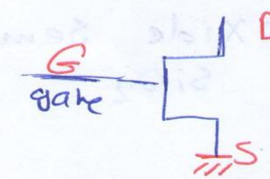
→ The 2 devices hard to scale
→ consume current ⇒ consume power
→ consume / burn power Quickly
∴ Excellent amplifiers

MOSFET

metal oxide Semiconductor
MOS

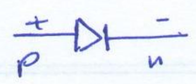
depend on The voltage to perform operation

→ new technology
→ voltage driven
→ low power
→ very high integration

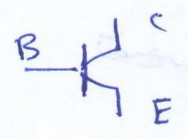


* 4 terminals
- base, gate
- source
- drain
- body

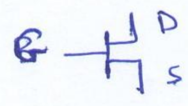
Bipolar



BJT

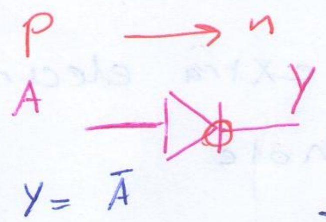


CMOS



if short cc v = 0.2

CMOS gates



$Y = \bar{A}$

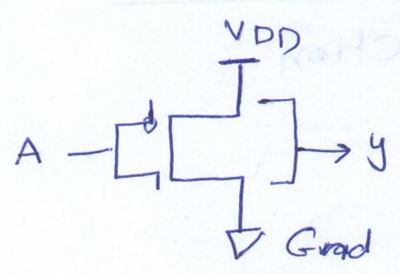
A	Y
0	1
1	0

① The Inverter

⇒ NOT gate

using 2 Moss transistor → nMos, → pMOS

T VDD ▽ ground



when A = 0 ⇒ base is off

no voltage on the base

⇒ no current

∴ Mos is off

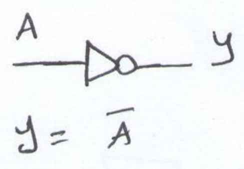
∴ nMos : off

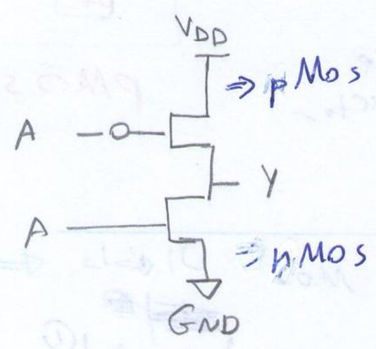
Then V_y = VDD ⇒ y is on

① when A = 0 (off)

pMos → on

nMos → off





mores law

transistors // يتضاعف

كل 18 شهر

كل سنه ونص بتضاعف

- n Type = extra electron
+ p Type = hole

⟹ silicon is poor Conductivity ⟹ so we add Dopants To increase Conductivity

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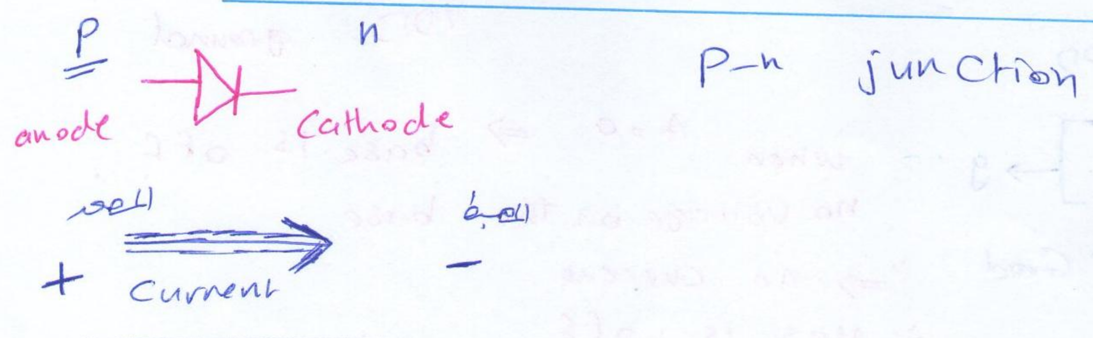
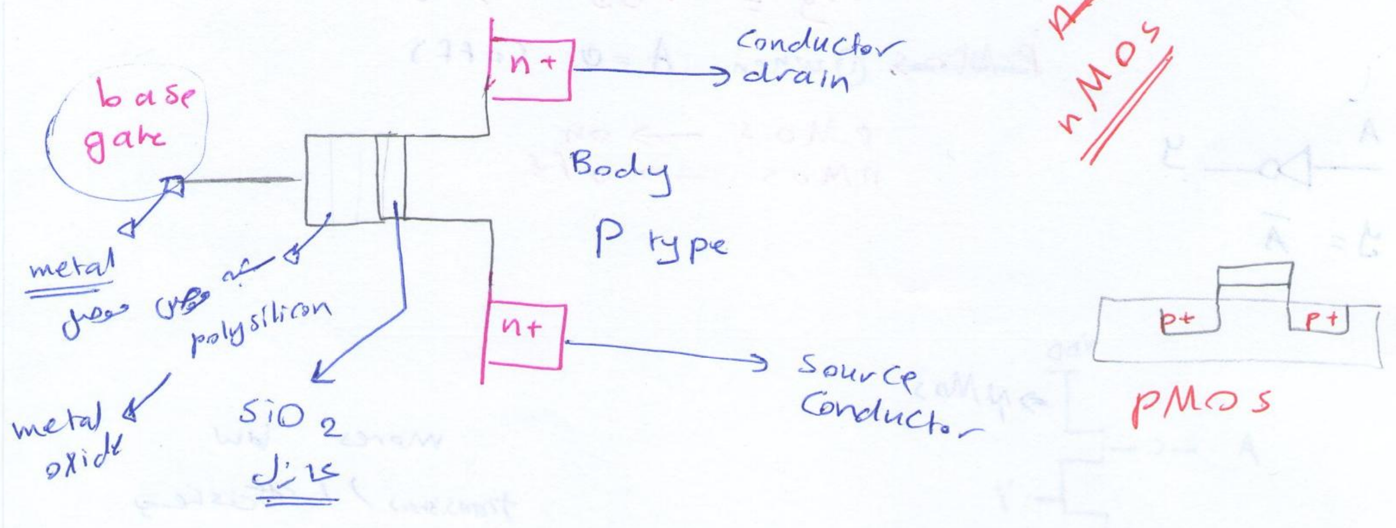
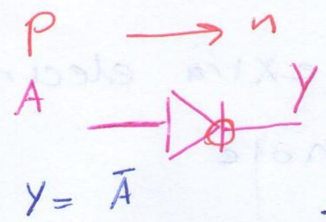


MOS transistors



⇐ داخل ال MOS الفولتية ال base او ال gate هي من يحدد
① الوضعية (موصول أو off)
② اتجاه التيار، منه D ← S

CMOS gates



$Y = \bar{A}$

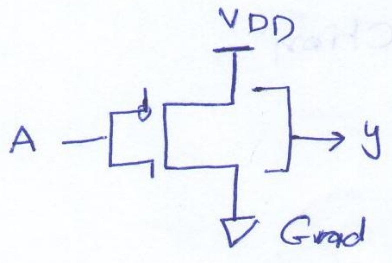
A	Y
0	1
1	0

① The Inverter

⇒ NOT gate

using 2 Mos transistor → nMos / → pMos

T VDD   ▽ ground



when A = 0 ⇒ base is off

no voltage on the base

∴ ⇒ no current

∴ Mos is off

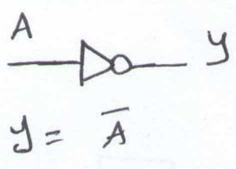
∴ nMos : off

Then V_y = VDD ⇒ y is on

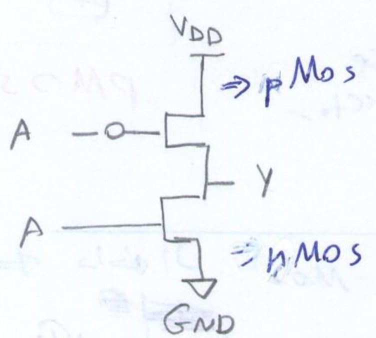
① when A = 0 (off)

pMos → on

nMos → off



$y = \bar{A}$



mores law

transistors // بتضاعف الـ

كل 18 شهر

كل سنة ونص بتضاعف

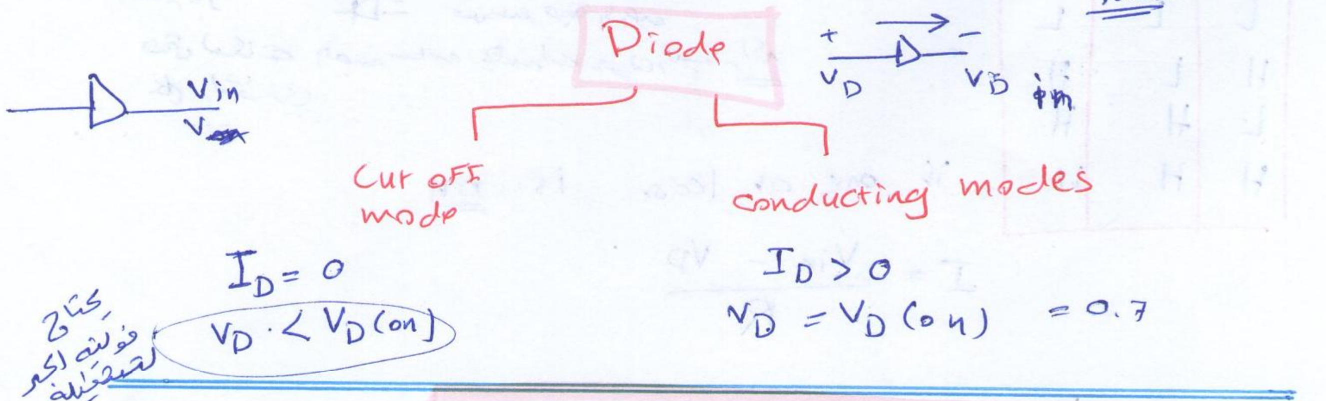
⟹ logic Gates in Digital electronics

① not inverter ② and, ③ OR, ④ NAND ⑤ NOR

⟹ **Diodes:** BJT transistor allows current passing in one Direction

→ Current Driven

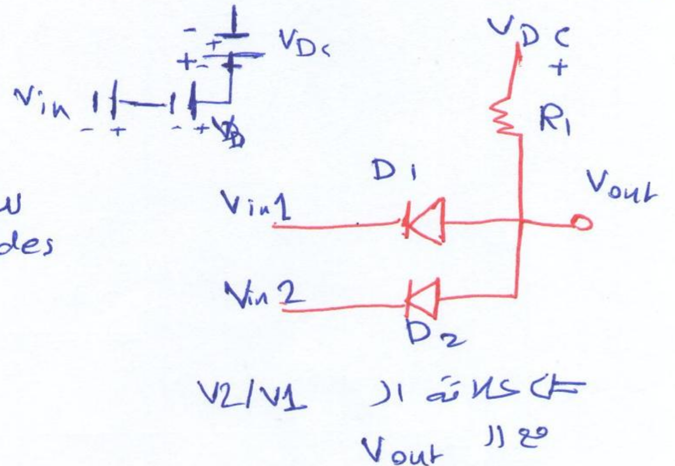
Diode ⟸ القيز بين Diode دار Mos



Diode – transistor logic

⟹ Diode-transistor logic performs only AND / OR Functions

① AND



V2/V1 ⟸ كلما قلّ الـ V2/V1 مع الـ Vout

if

$V_{in} > V_{DC} - V_{D(on)}$ } كلها للـ 2 diodes

∴ + —|◁— − ⟹ OFF

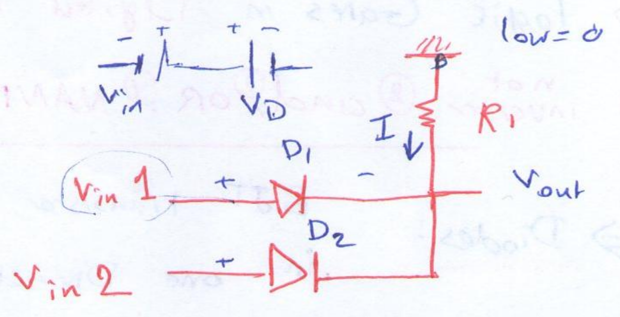
OFF واحدة الاقل يجب ان يكون OFF

1	2	out
L	L	L → off
L	H	L
H	L	L
H	H	H

① if both are off ⟹ $I = 0$

if either one is on $I = \frac{V_{DC} - V_D - V_{in}}{R_1}$

2 OR gate



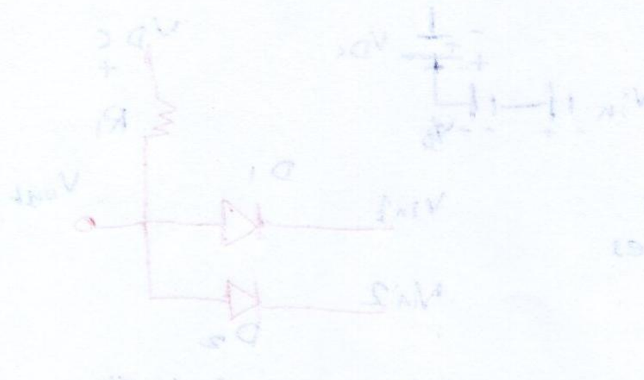
$V_{in} > V_D \Rightarrow$ ON

1	2	out
L	L	L
H	L	H
L	H	H
H	H	H

التحكم بال $^{+}D^{-}$ من عند جهة الموجب
حتى لو كانت الجهة سالبة بالشدات تحول الجهد اكبر
على التوازي

if one at least is on

$$I = \frac{V_{in} - V_D}{R}$$



Bipolar Junction Transistor

① Cut off

$V_B - V_E < 0.7$

$I = 0$

Forward inverse

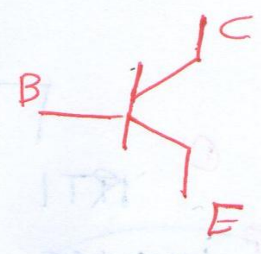
$V_{BE} = 0.7$

Saturation

$V_{BE} > 0.7$

$= 0.8$

$V_{CE} = 0.2$



$I_E = I_B + I_C = (\beta + 1)(I_B)$

1 Resistor Transistor logic (RTL)

→ Inverter

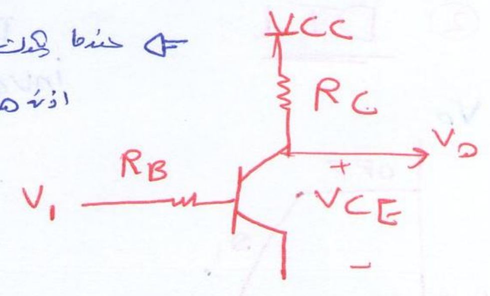
Bipolar

شرط يكون ال V_i كبير ⇐ بال Saturation ⇐

اذا هناك تيار فتطلع ال V_o

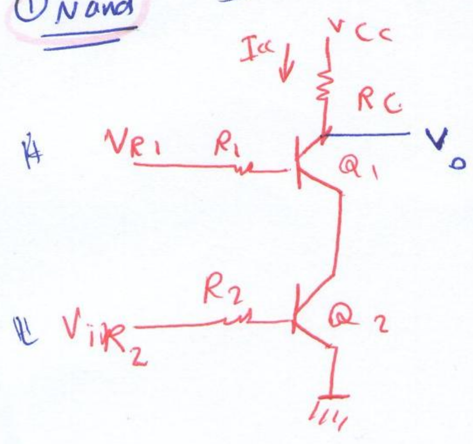
$V_1 - GND \geq 0.7$

V_1	V_o
L	H
H	L



2 RTL : NAND / NOR gates

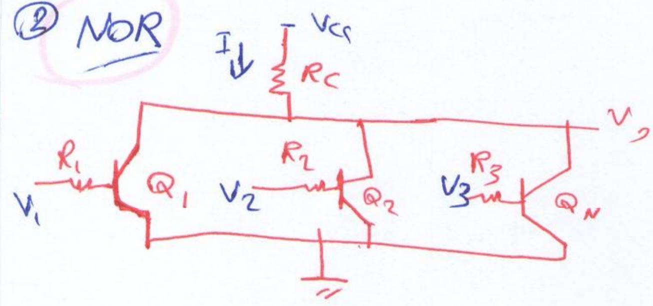
① Nand

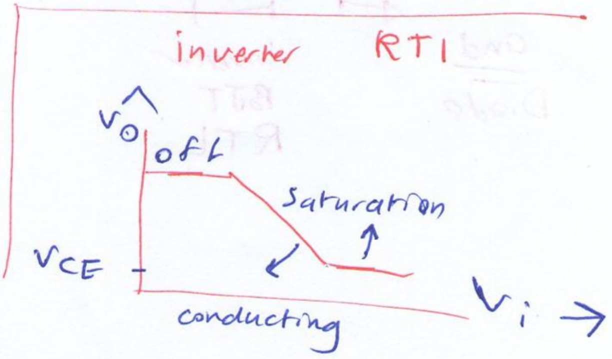


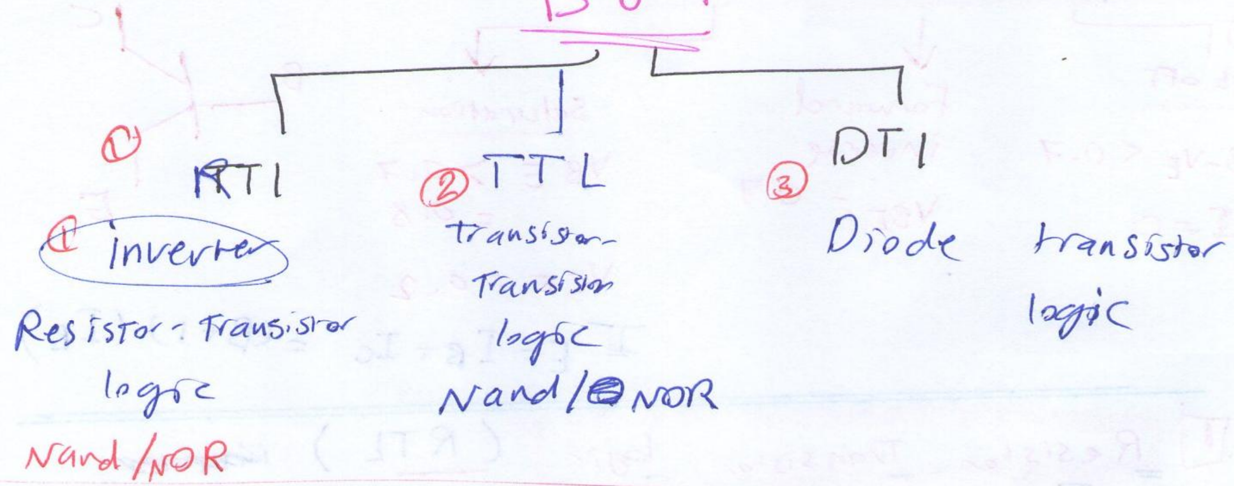
1	2	V_o
L	L	H
H	H	L
L	H	H
H	L	

⇒ كيف صارت

② NOR

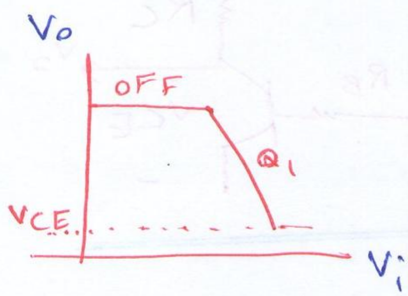


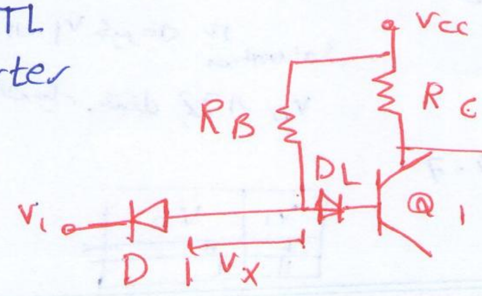




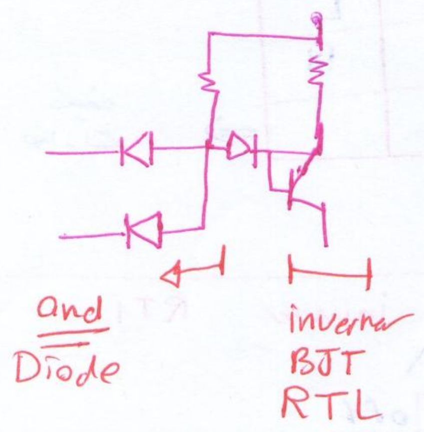
② DTL :

DTL
inverter



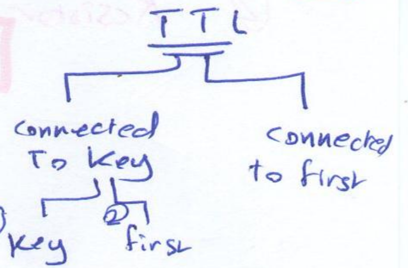


⇒ DTL /NAND

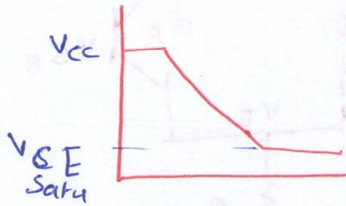


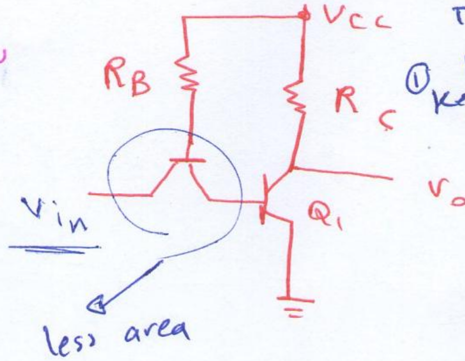
TTL → forward / reverse   Key → oFF / saturation

3 TTL : transistor - transistor logic



1. TTL inverter : → Safe → but slow





2. TTL NAND Gate

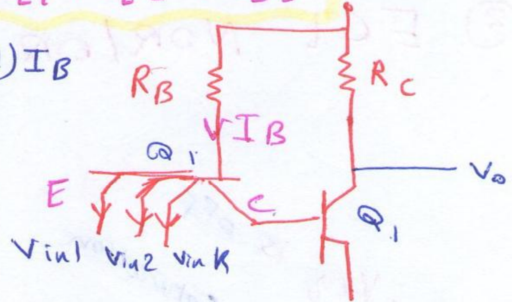
$I_B + I_C = I_{E1} + I_{E2} + I_{E3}$

$\sum I_{Ei} = (\beta + 1) I_B$

if one input $< V_{iL}$

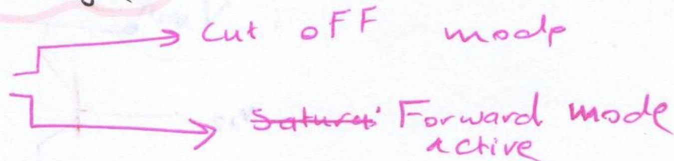
$Q_1 \Rightarrow$ oFF

all $> V_{iH} \Rightarrow$ Q : saturation



Emitter_Coupled logic

1. 2 modes only : → cut oFF mode → ~~Saturat~~ Forward active mode

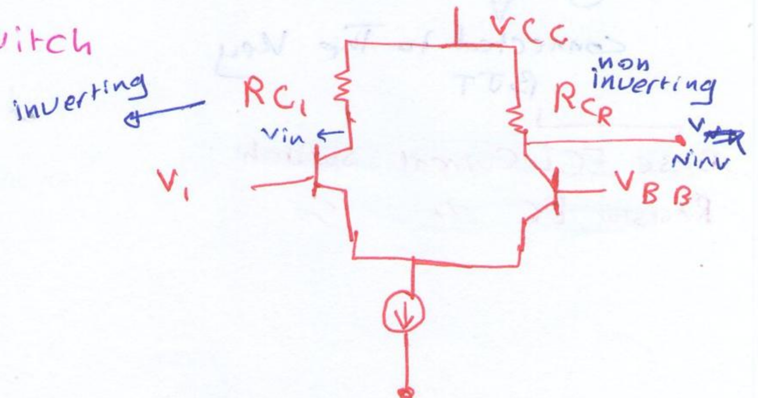


2. fastest switching   TTL عكس

3. highest power dissipation of all logic families

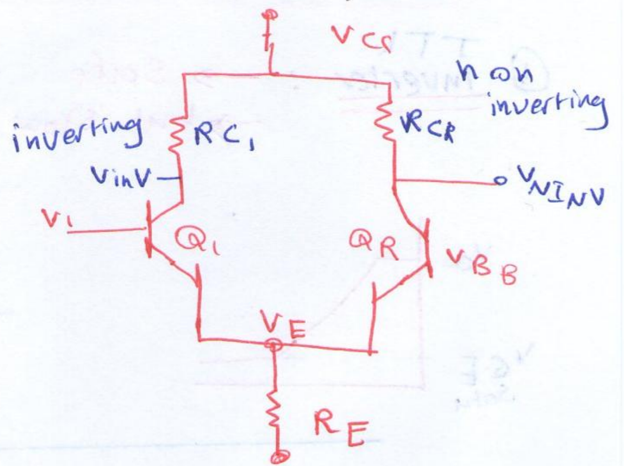
fast but sensitive

1. Basic ECL Current Switch

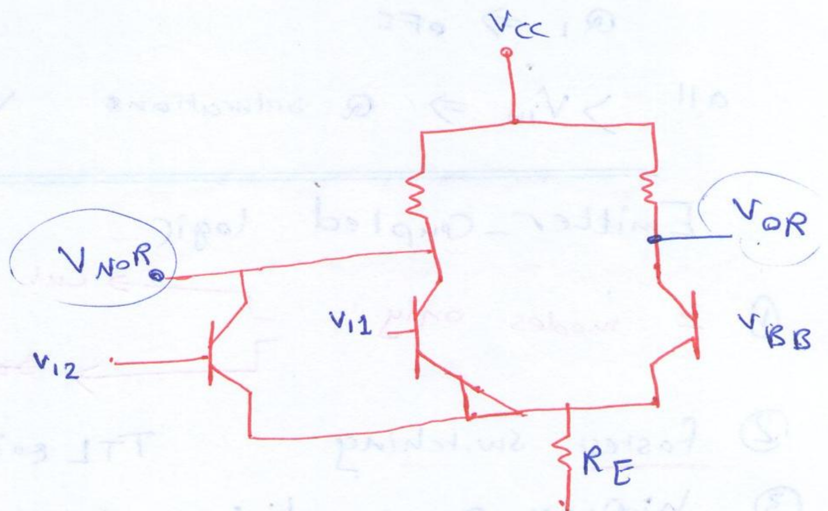


TTL	ECl
- Safe	- sensitive
- Slow	- fast

② Resistor EC Current Switch



③ ECL NOR/OR ~~Switch~~ Gate



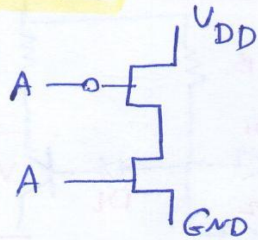
TTL

① Connected to The Key BJT

② Connected to The first BJT

Gates ال gaيت

[1] CMOS inverter — CMOS



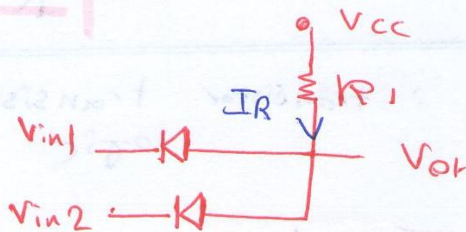
[2] Diodes (Bipolar transistor) — DRL

AND — DRL — OR

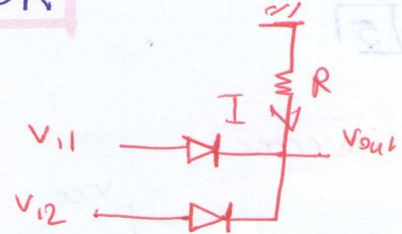
Diode-Resistor logic

DRL: Diode / Resist فقط

① AND

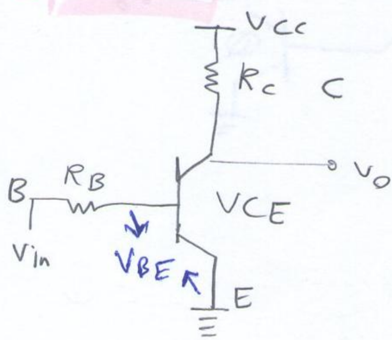


② OR

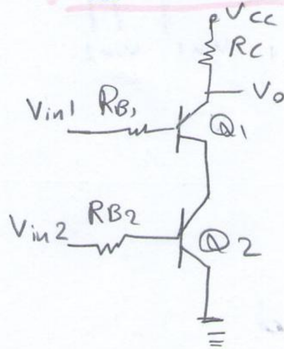


[3] BJT RTL ① Resistor ② transistor logic

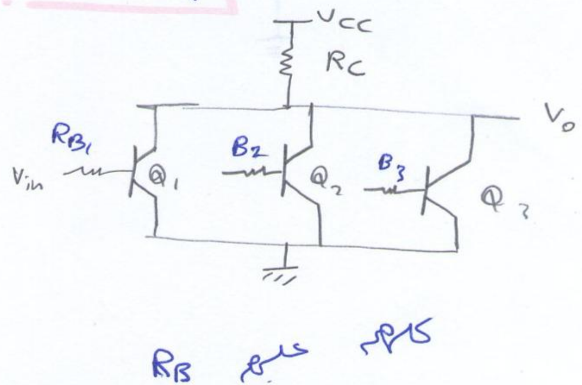
① inverter



② NAND



③ NOR



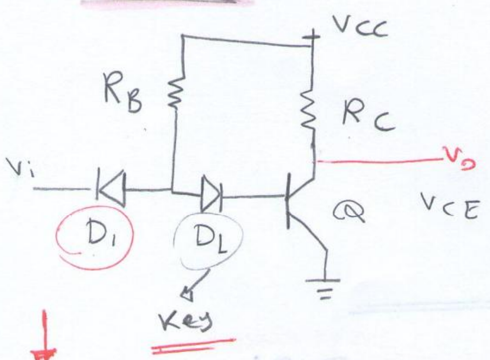
RB علم كالرم

4 DTL

Diode - transistor logic

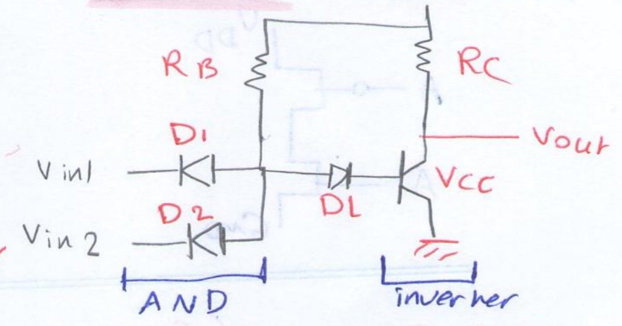
ترانزیستور دیود .

① inverter



D1 is connected to The Key
↓
first Diode

② NAND Gate



D2 is connected to the first Diode D1

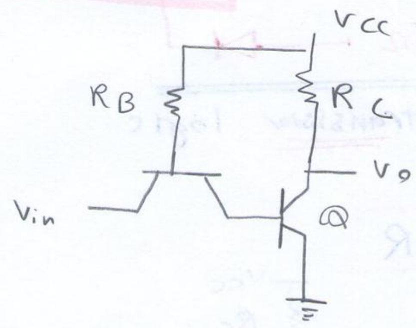
NAND = AND + inverter

DTL = AND DRL + inverter RTL

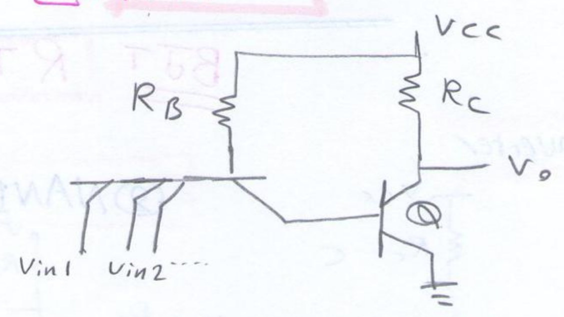
5 TTL

: transistor transistor logic

① inverter



② NAND

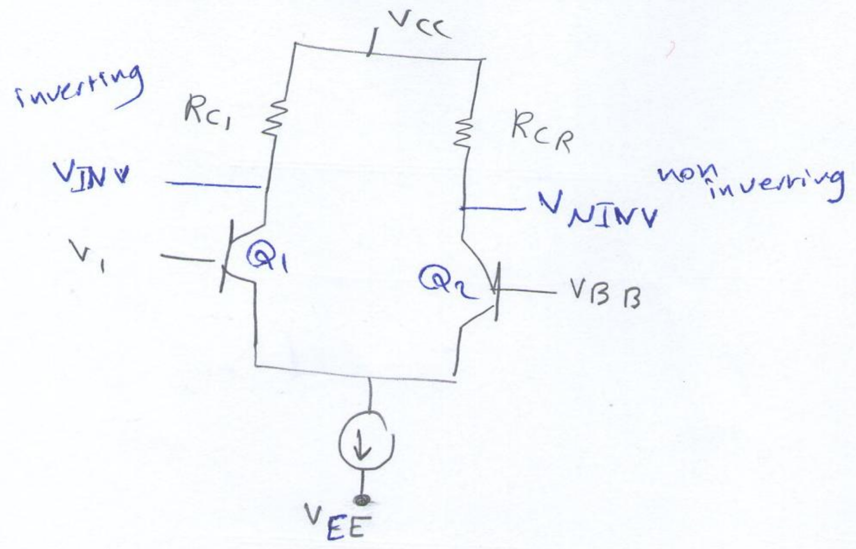


(5)

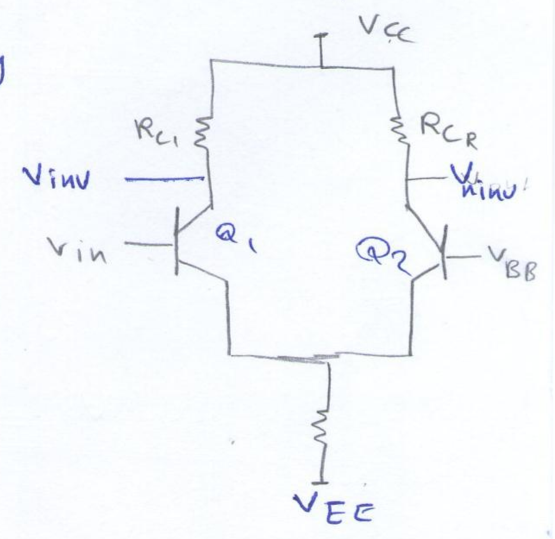
ECL

Emitter - Coupled logic

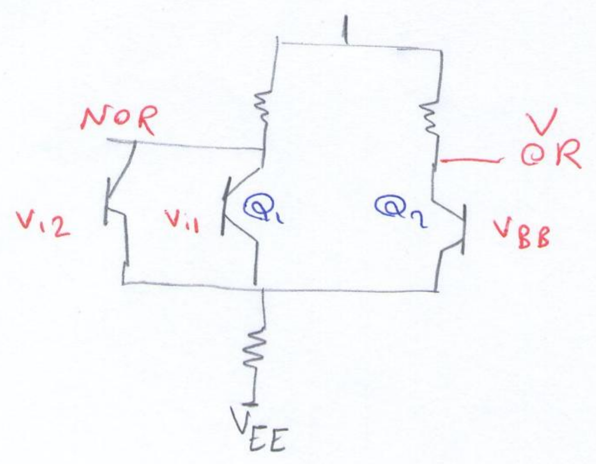
(1) Base ECL Current Switch



(2) Resistor EC current switch



(3) ~~NAND~~ NOR/OR



EICoM
ELECTRICAL COMPUTER MECHATRONICS

Lecture 3

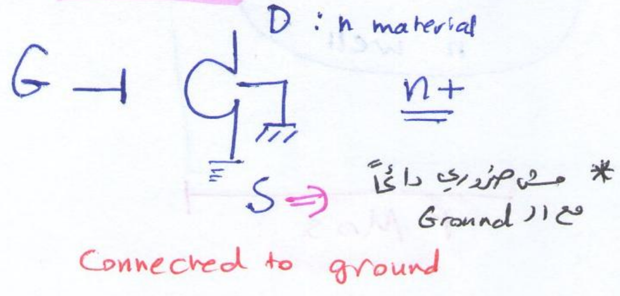
3 terminals
/ Gate / Drain / Source

CMOS

Lecture 3 : Steps

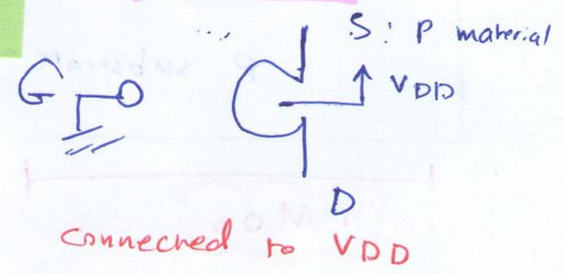
G D S

nMOS



Connected to ground

PMOS



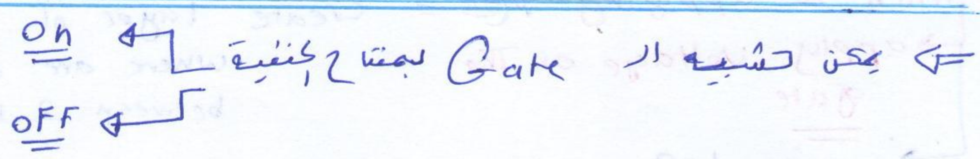
Connected to VDD

Vcc ↑ VDD

Vss ↓ ground

heavy

always in Reverse Bias

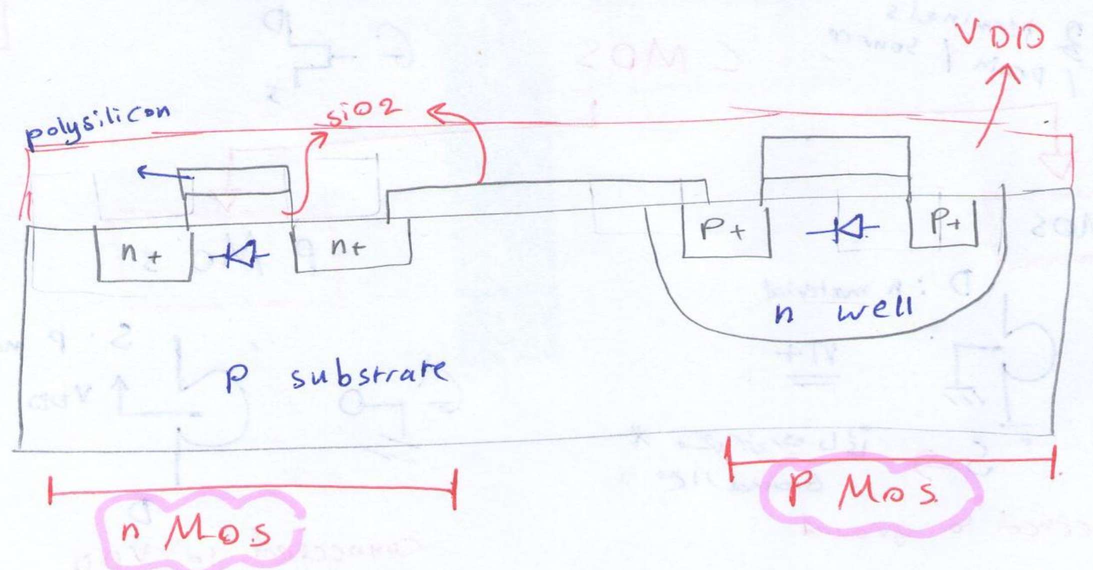


⇒ Current flow Controlled by Gate

⇒ Current Source ⟶ Drain

SiO_2 : Very good insulation material

VDD



⇒ n+, n+ source and The Drain are separated by p material

عادةً الـ Diodes تكون في حالة الـ Reverse Bias

*Reverse :: يعني ⇒ no conduction between The 2 terminals
∴ no Current

* n MOS

⇒ When applying VG = Create layer of electrons where are conducting between 2 terminals
- ↳ apply voltage on The gate
- ↳ open tap
  مثل فتح الكنفية

⇒ Cannot build [n+][n+][n+] : Then will be short CCt always
but we only need to allow / stop electrons

① ⇒ Voltage on Gate ⇒ eleerons ⇒ Short CCt ⇒ Conducting mode فتح الكنفية

→ P Substrate material : material of silicon which holds CCt but Contain of p material
↳ only for n Mos

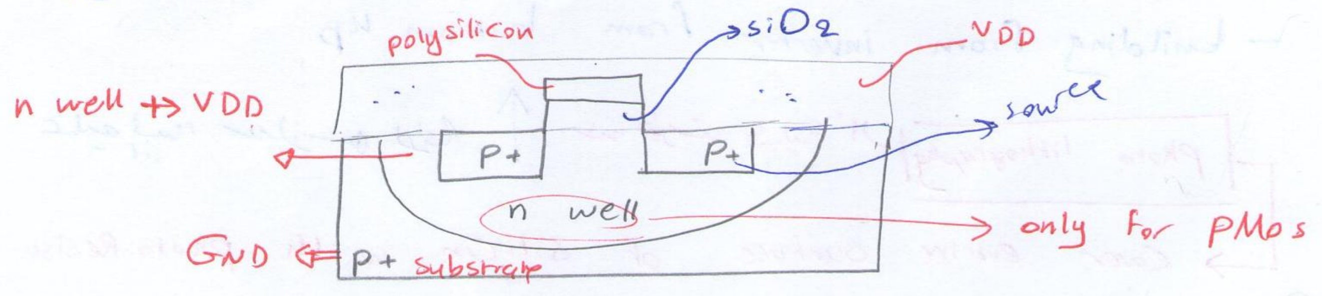
but in p Mos must be a well off n type material in order not to build short CCt.

* electrons : n+ (−)
* holes : p+ (+)

* pMos

⇒ عكس عملية ال nMos.

The source & The Drain are p material



⇒ applying U_g on The Gate: Create layer of holes between The 2 terminals

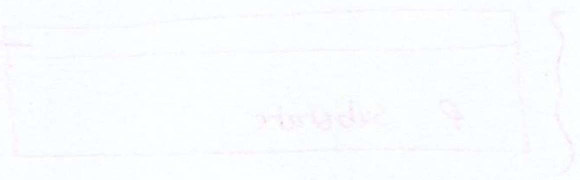
→ but make sure that b substrate is only for nMos

- NMos connected ⇒ ground (p substrate)
- PMos connected ⇒ Udd (n well)
  - why: to Keep Diode in reverse mode

mask: alayer of some material

⇐ كلما صغر حجم ال S وال D كلما اصبحت اسرع.

*wafer: slide of silicon



Fabrication Steps

- Start with blank wafer
- building from inverter from buttom up

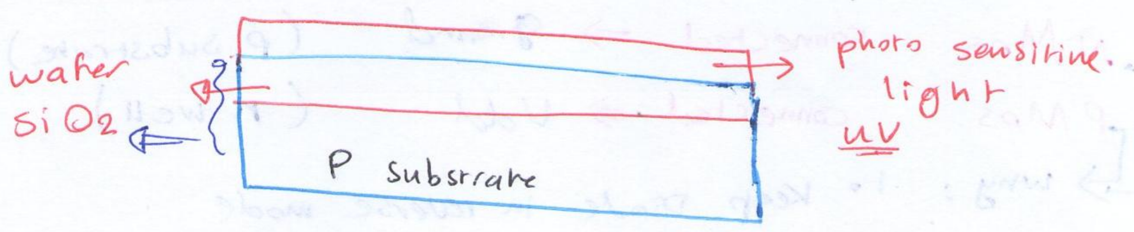
عملية البناء من الأسفل للأعلى ↑

photo lithography حنة طريقة عملية ال

→ Cover entire surface of silicon with photo Resist

① material or photo sensetive material

② phace a mask



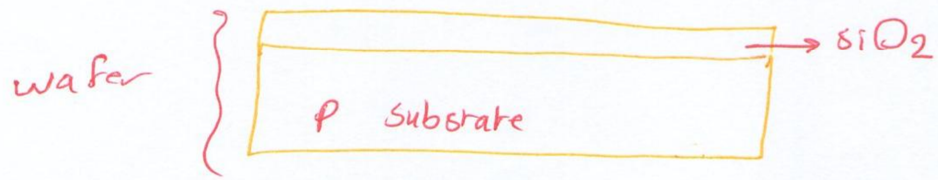
Steps بالتفصيل

① Silicon wafer on P substrate is covered with O_2

⇒ oxidation : SiO_2 Growing on the top of wafer

الأكسدة عن طريق O_2 أو ال H_2O

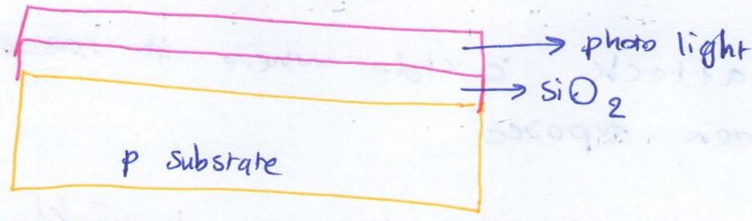
∴ we get



Step 2

[2] photoresist : photo sensitive light-sensetive material

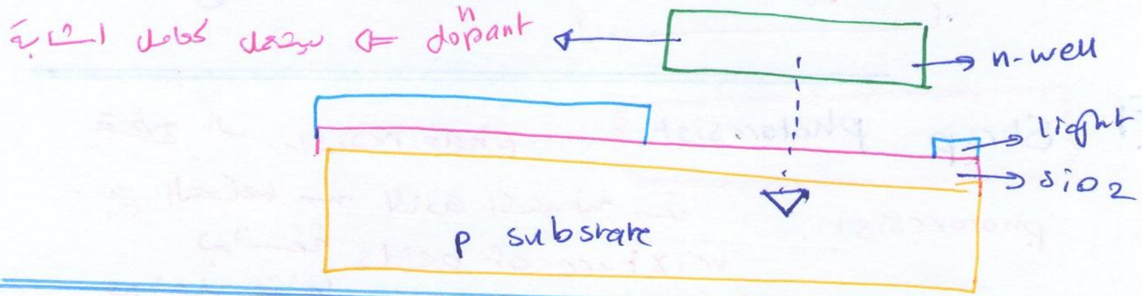
covers wafer with light-sensetive material



Step 3

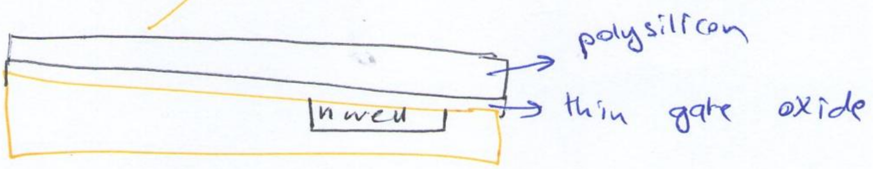
remove soft ~~light~~ photo

[3] Lithography remove light-sensetive where n-well mask should be built



[4] polysilicon : شبه موصل
- after n-well is built inside wafer
- very thin layer of gate oxide

by chemical vapor Deposition CVD polysilicon material covers thin gate oxide



4 step 4 : **Etch** الحفر

كيف ملاحظة ان ازالة ال hard لها محبة يختلف عن acid ازالة ال soft فيما سبق

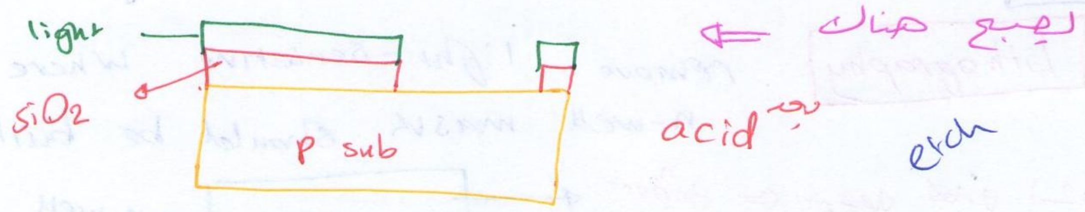
after The light-sensetive material is removed but SiO_2 will resist the n-well ..

SiO_2 (oxide) is etched with acid

نتخلص منه حتى نستطيع ادخال ال n-well بسهولة

⇒ only attack oxide where ~~resist~~ resist has been exposed

الهدف من هذه الطريقة وال lithography حفر ال SiO_2 بجزء محدد فقط



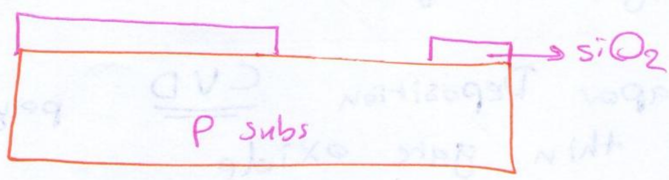
5 **Strip photoresist** قطع ال photo resist

يتم التخلص من المادة المتبقية من photoresist بواسطة mixture of acids

مع العلم ان ~~الحفر~~ البقاء SiO_2 بدون photor. مهم

لل Resistance و انها لا تتحلل

ليصبح

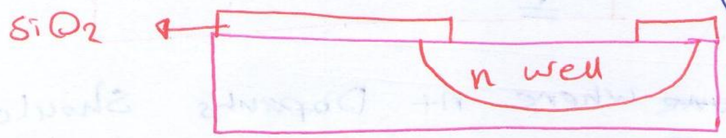


Step 6 | n-well

ال n-well تدخل وتتحول لجزء خاصة

n-well is formed with - Diffusion (gas) ← بالانتشار / بالحرارة
- old
- cheap

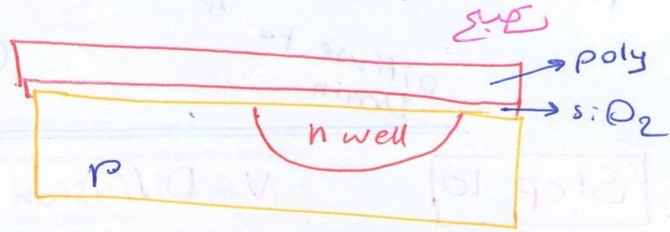
- Ion implanation ← بالزرع
  - as
  - more accurate
  - more expensive
  - new technology



Step 7 | poly silicon

1- deposite Thin layer of gate oxide

The Gate is made of polysilicon but in order not to make short cct between drain & and the source ⇒ gate oxide (SiO_2) must be deposited

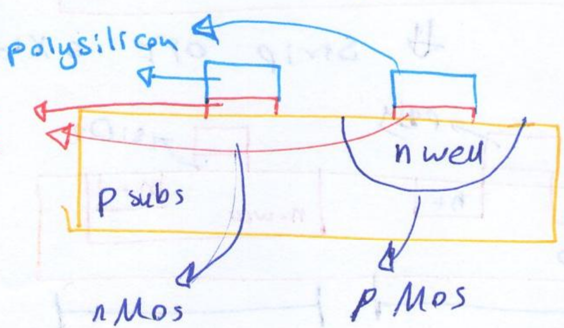


Step 8 | polysilicon patterning

زخرفة ال poly يعني نزيد اشياء Gate poly لل n Mos وال pMos

Pattern polysilicon for
- nMos gate
- pMos gate

← نفس خرطة ال lithography السابقة نزيد نتشكل حواف ال poly لازالة ال poly وال oxide



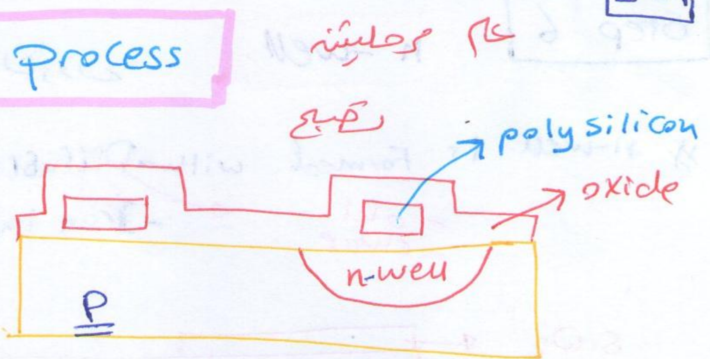
⇒ we get 2 Gates

عمودين

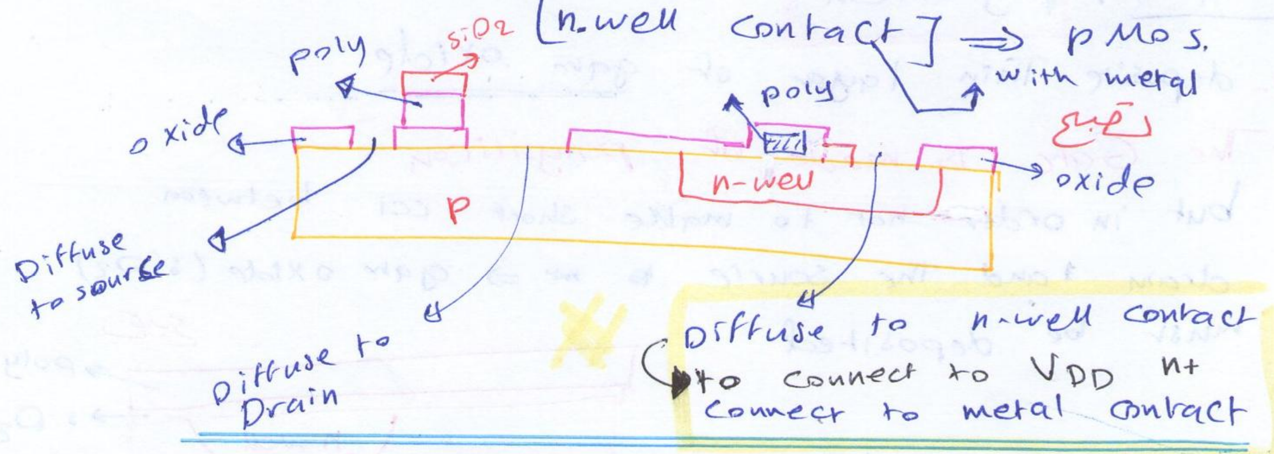
Step 9 : Self-aligned Process

عام رصاصيّة

1. Cover with oxide



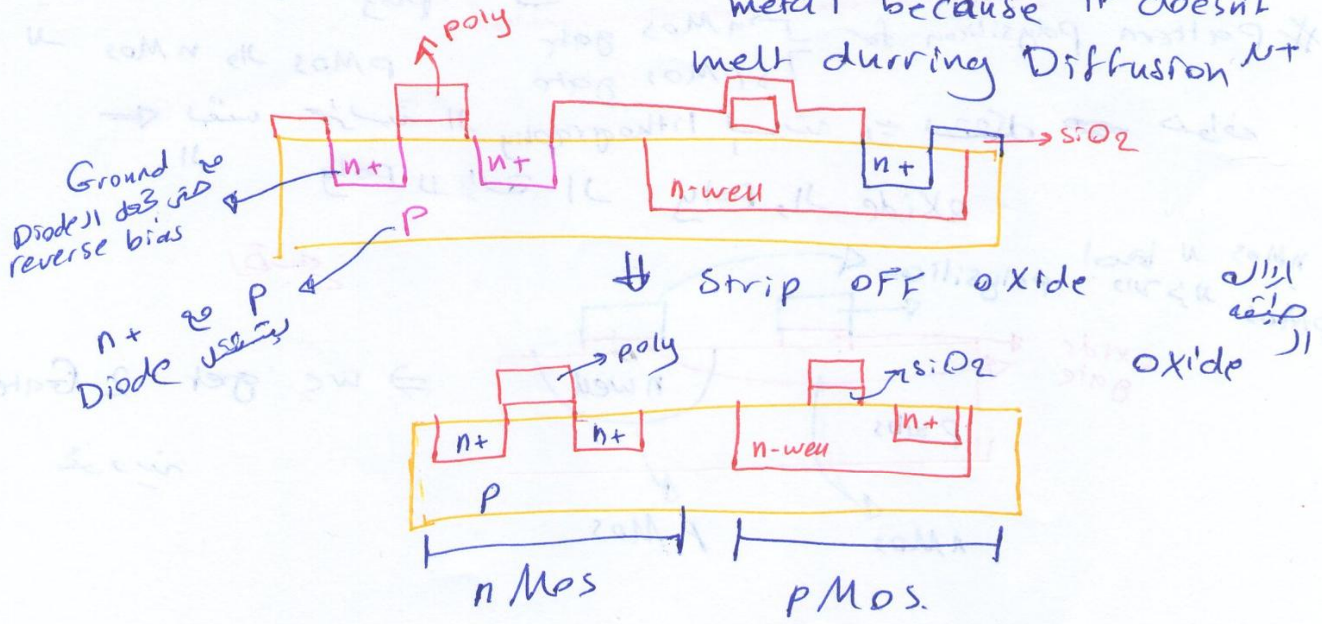
2. mask to expose where n+ Dopants Should be Diffused to [Drain, source] ⇒ n Mos
[n-well contact] ⇒ p Mos. with metal



Diffuse to n-well contact
to connect to VDD n+
connect to metal contact

Step 10 N - Diffusion

- form n+ regions
- Gates are not Diffused ⇒ polysilicon better than metal because it doesn't melt durring Diffusion n+

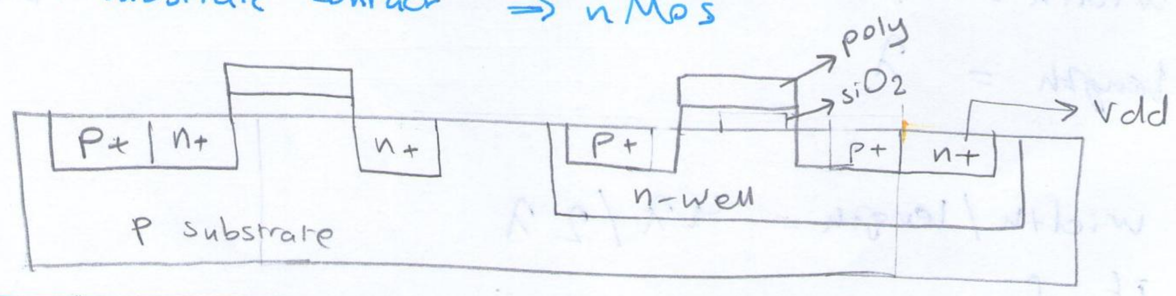


Step 11 : P_Diffusion

Same steps → Oxidation, → Etch, → Diffusion } ⇒ for P+ regions

⇒ for P+ source, drain ⇒ PMos

P substrate contact ⇒ nMos



Step 12 : Contacts

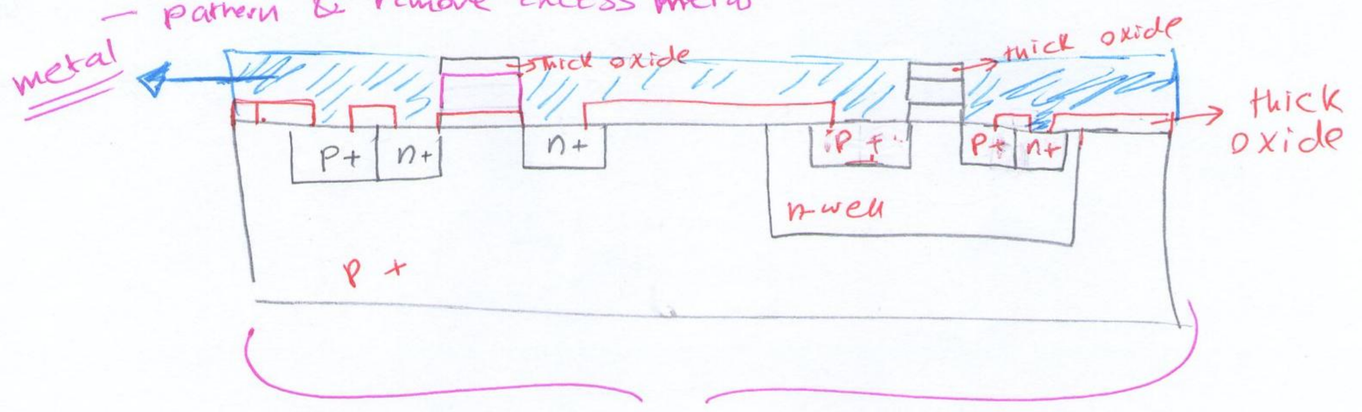
1. deposite layer of oxide   oxide [illegible]

layer of oxide is thick fied

2. etch oxide regions where contacts are needed

~~length~~ Step 13 : metalization

- covers metal over the wafer
- pattern & remove excess metal

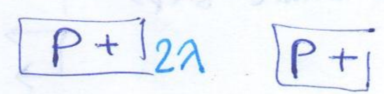


Complete chip

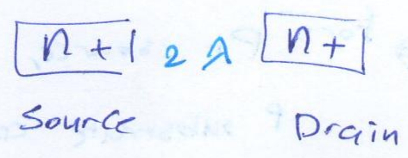
∴ chip: set of masks

Distance between source & drain ⇒ length of channel

feature size ⇒ $2\lambda = F$



$\lambda = \frac{F}{2}$

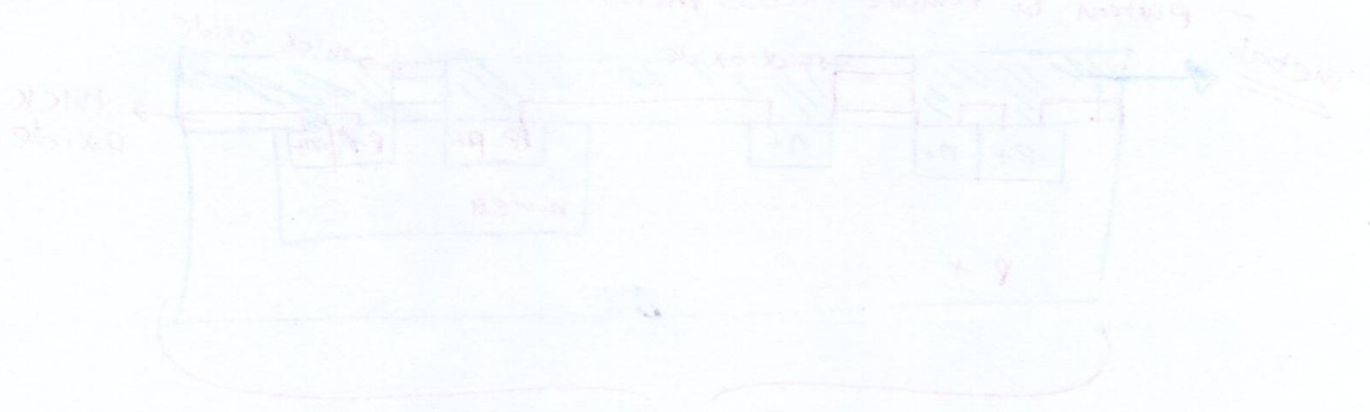


width = f

length = λ

width / length = $4\lambda / 2\lambda$

if $f =$

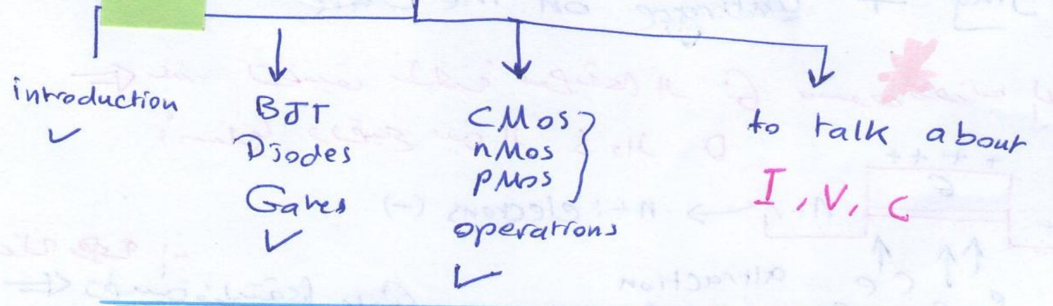


$L = 2\lambda$

Theory

Transistor Theory and DC characteristics

PE - DIC



analysis

DS

* voltage is constant in The cct
- Simpler
→ value of The voltage of Current in constant condition

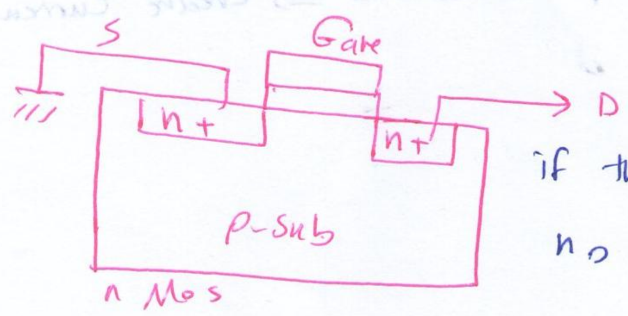
* حركة الالكترونات عكس اتجاه حركة التيار

Transient

→ Voltage is dynamic
→ focus on delays:
#how does it take to change input or output for certain value
e.g: inverter : invert value
this change needs delay

low → high
→ delay: how long it take to make this transition

① How delays
② How power

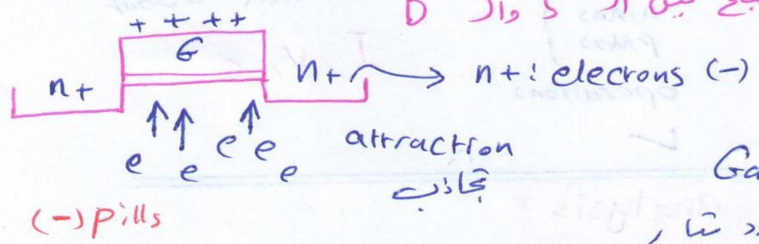


if there is volt on the gate: tap is on
no voltage: channel is off

⇒ in nMos ⇒ normal mode is idle

⇒ but Conduction happens by establishing a channel by create layer of electrons under the Gate by applying + charge on the Gate

⇐ عند تطبيق شحنة موجبة على الـ G سوف تنجذب الإلكترونات أسفلها وتتجمع بين الـ S والـ D



* ملاحظة هامة :-

⇐ تطبيق فولتية على Gate
هذا يعني السماح بوجود تيار ،
ولكنه لا يعني اجبار وجود تيار ،
يجب أن يكون هناك فرق جهد يسمح بتوليد تيار كهربائي
السوط

* Conditions to Create Conduction Channel :-

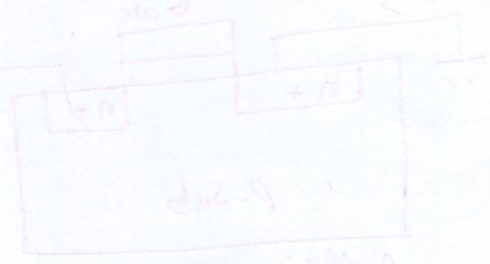
1. positive charge on Gate which create Virtical pills electrons
2. voltage difference (differintial voltage) to create current ⇒ pressure

لنفس مثال الحنفية :
① الحنفية : فتح الحنفية
② الضغط : فرق الجهد : التيار : مجال كهربائي

Voltage difference by 2 electrical fields :

Virtical
builds Channel

Horizontal
later
Sweep electrons ⇒ create current
تدفع



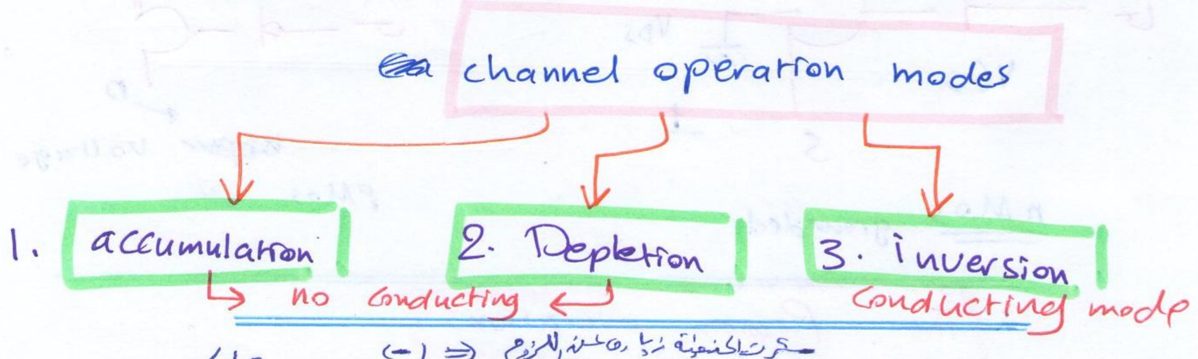
Current : + ⇒ −
electrons : − ⇒ +

$$Q = C \cdot V$$

(Q → charge, C → capacitor)

$$\frac{dQ}{dt} = C \cdot \frac{dV}{dt} \Rightarrow I = C \cdot \frac{V}{\Delta T}$$

channel = Gate + body (capacitor) ⇒ p substrate



① accumulation : The Gate connected to Low Voltage (−) or to ground (0V) and the Diode is Reverse Bias
→ OFF state ⇒ only holes in absence of electrons

② Depletion : when applying positive charge on the gate
→ repels the holes ⇒
$V_t > V_g > 0$
hole
electron
⇒ still no conducting mode
The positive charge not strong

③ Inversion : positive charge is strong
→ invert type of material

$V_G \geq V_t$ ⇒ Threshold
→ voltage when device is conducting

electrons

Voltage controls only ON/OFF modes on The Gate

↳ MOS ⇒ VG

⇓

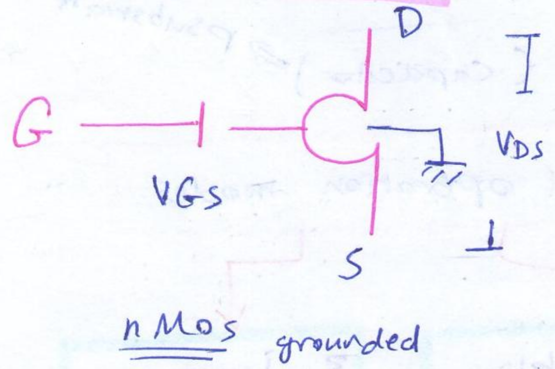
Consume power less Than BJT

I_B — BJT عكس ال

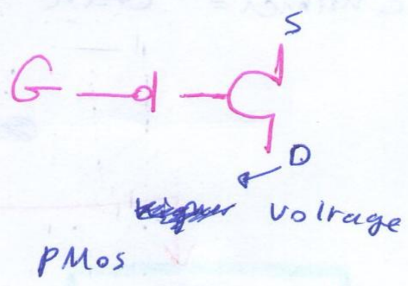
الي فقط بتحدد ال وجود/عدم وجود I_B

Consume more power

MOS Terminals



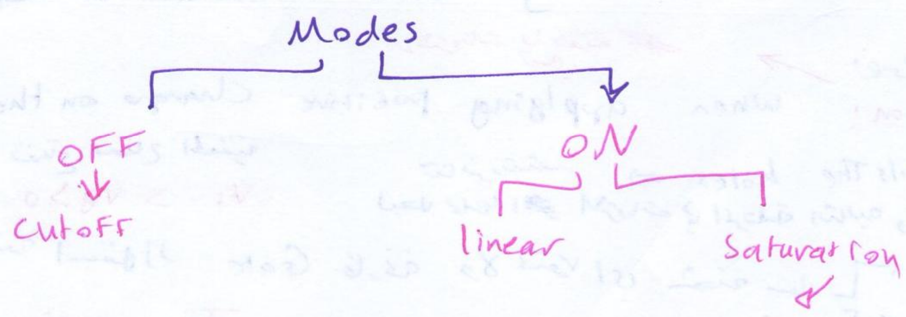
nMOS grounded



PMOS

The Region operations

1. CutOFF
2. linear
3. Saturation



1. Cut OFF region : region where There is no Channel

↳ The Tap Key is OFF switch : open

diode : reverse bias

Current between Drain & source = 0

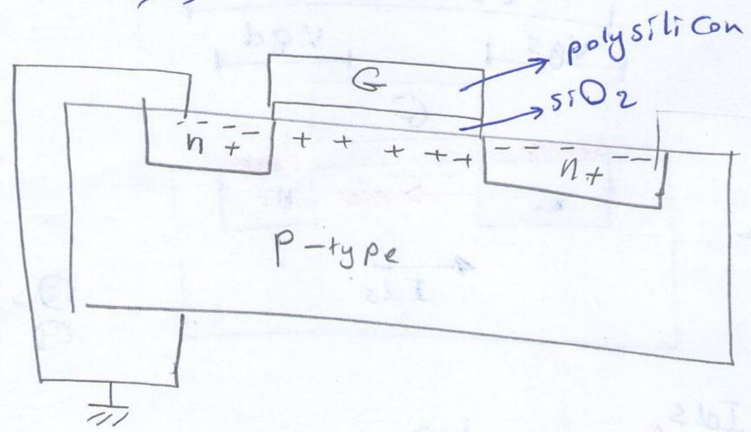
كلمة Channel تعني وجود : * وجود ال Gate

* وجود فرق الجهد

* وجود تيار

1

Cut-OFF mode



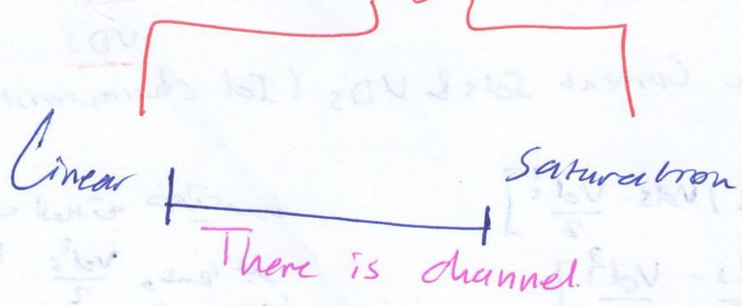
$V_{gs} < V_t$

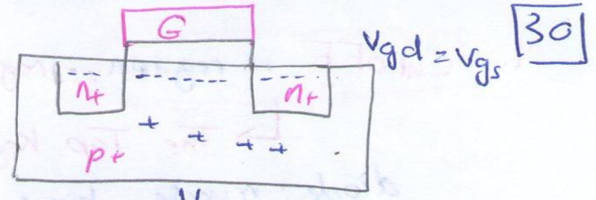
$I_{ds} = 0$

عبارة عن ال accumulation operation mode

Cut OFF : non-Conducting mode

Conducting modes





$V_{gd} = V_{gs}$

2 Linear — Conducting mode

→ Depletion + inversion

$V_d > V_s$ المفروض

التيار من الجهد العالي

d → s

electrons : s → d

1. $V_{gs} > V_{gd} > V_t$
2. $V_{ds} > 0$ && $V_{ds} \le V_{gs} - V_t$
3. $V_{gd} > V_t$
4. $V_{gs} \geq V_t$ أو هيك

$V_{ds} = V_d - V_s$

V_{gs} , V_{gd}

G
source
drain
n+
n+
e⁻ e⁻
Ids

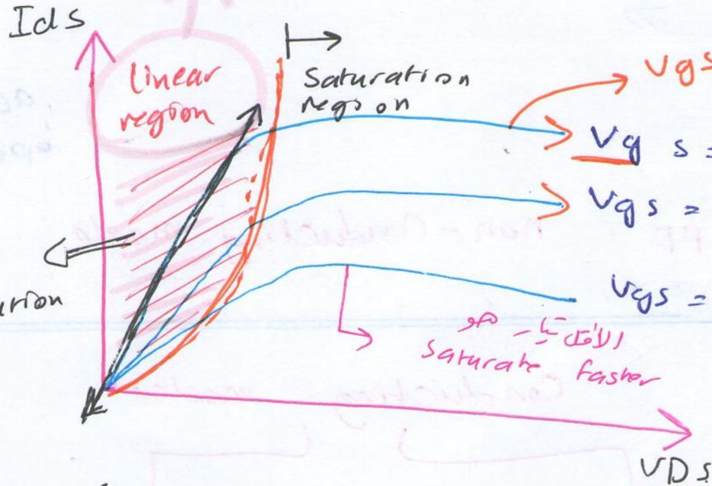
V_t : $V_{threshold}$

العتبة اللي رح تحرك مفتاح الحنفية .

Ids increases with Vds

$I \uparrow \; V_{DS} \uparrow$ عند ثبوت R

⇒ more voltage on the gate = more current in the channel
علاقة طردية



⇒ more voltage on gate more electrons in channel

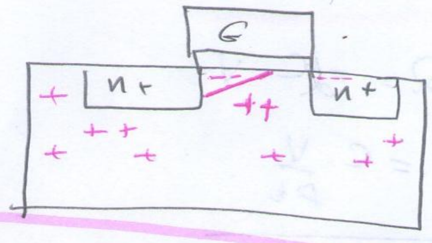
Relation between Current Ids & VDs (Id characteristics)

$$I = \beta \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

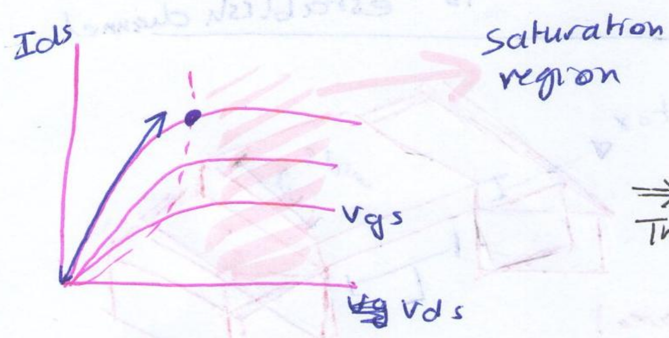
$$I_{ds} = \beta \left[V_{gt} V_{ds} - \frac{V_{ds}^2}{2} \right]$$

* توضيح !-
المفروض تكون العلاقة خطية دون وجود التربيع $\frac{V_{ds}^2}{2}$ ولكنها غير ما صدات بعين الاعتبار فقط تدخل في الحساب وقيمتها صغيرة جداً عشان يبين انها تعتمد ولو بمقدار قليل ع V_{ds}

3 Saturation Conducting mode



- Channel pinches off
- Ids indep. Vds
- Current saturates



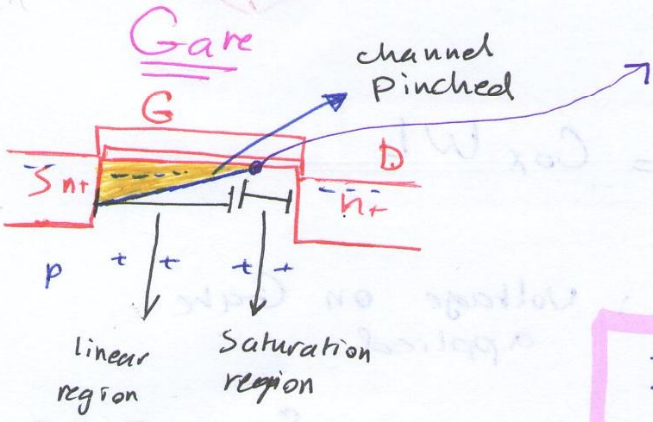
Saturation region

1. $V_{gd} < V_t$
2. $V_{ds} > V_{gs} - V_t$
3. $V_{gs} > V_t$

⇒ Voltage at drain will be larger Than gate voltage $- V_t$

at moment when channel pinched

Gate



$V_{ds} = V_{gs} - V_t$

if $V_d > V_g$

كأنه نعتبرها Source هو ground

In saturation region Same Current no change

$$I_{ds} = \beta \frac{(V_{gs} - V_t)^2}{2}$$

$$I_{ds} = \beta \frac{(V_{gt})^2}{2}$$

independent of Vds ⇐

$V_{gt} = V_{gs} - V_t$
$= V_g - V_t$

في الامتحان يطلب تحليل ال cct أو ال Graph

Time $= \frac{L}{V} = \frac{L}{\mu \cdot E}$ = لإيجاد الوقت

السرعة ف

$\varepsilon_{ox} = 3.9 * 8.85 * 10^{-14}$

نبدأ بالاشتقاق للمعادلة الي اللي

معلومات Channel

linear region

$d\,Q = dC \cdot V$

$I = C \cdot \frac{V}{Dt}$

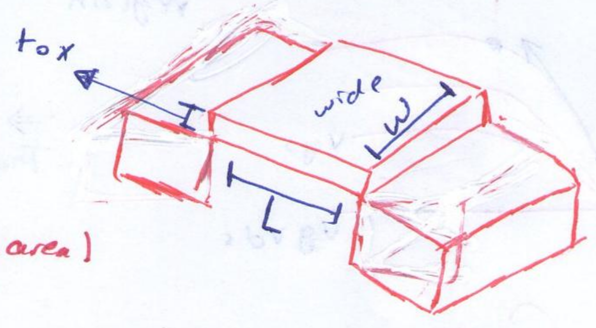
$V = V_{gc} - V_t$

Voltage cross Channel

لانه مفقود ⇐ V_t

V_t lost to establish channel

$C = C_g$: vertical Capacitor cross Channel



$$C_g = \frac{\varepsilon_{ox} W L}{t_{ox}}$$

t_{ox} : Thickness of oxide (isolation area)

ε_{ox} : permitivity of space ⇒ السماحية الكهربائية

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \Rightarrow C_g = C_{ox} W L$$

$V = V_{gc} - V_t$ ($V_g - V_t$)

V_{gc} : Voltage on Gate applied

$= \left(V_{gs} - \frac{V_{ds}}{2}\right) - V_t$

$\varepsilon_{ox} = 3.9\,\varepsilon_0$

$v = \mu \cdot E$ → elecrical field

velocity, constant

$V_{gt} = V_{gs} - V_t$

$\beta = \mu C_{ox} \frac{W}{L}$

∴ Current equation for Linear region

$$I_{linear} = \beta \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

($V_{gs} - V_t$ = V_{Gt})

$$\therefore I = \beta \left[V_{Gt} V_{ds} - \frac{V_{ds}^2}{2} \right]$$

- هذا يطلب اهامك في الامتحان
- يظهر تأثيره في آخر الـ linear region

Cutoff	linear	Saturation
$V_{gs} < V_t$	$V_{gs} > V_{gd} > V_t$	$V_{gd} < V_t$
	$V_{gs} \geq V_t$	$V_{gs} \geq V_t$
		$\therefore V_{gd} < V_{gs}$
	$V_{ds} \leq V_{gs} - V_t$	$V_{ds} > V_{gs} - V_t$
$I_{ds} = 0$	$I_{ds} = \beta\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right]$	$I_{ds} = \beta \frac{(V_{gs} - V_t)^2}{2}$
	$I_{ds} = \beta\left(V_{gt} V_{ds} - \frac{V_{ds}^2}{2}\right)$	$I_{ds} = \beta \frac{V_{gt}^2}{2}$

---

e.g $t_{ox} = 100 Å$

$\mu = 350 cm^2 / V \cdot s$ (volt, second)

$V_t = 0.7$

$\frac{W}{L} = \frac{4}{2} \lambda$

$\beta = \mu C_{ox} \frac{W}{L}$

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

$\varepsilon_o = 3.9 \times 8.85 \times 10^{-14}$

$\frac{W}{L} = \frac{4}{2} \lambda$

$L = 2\lambda$

$$\beta = 350 \frac{cm^2}{V \cdot S} \cdot \frac{3.9 \times 8.85 \times 10^{-14} \frac{F}{cm}}{100 \times 10^{-8} cm} \frac{W}{L}$$

$$= 12080 \times 10^{-6} \cdot \frac{W}{L} \cdot \frac{F}{V \cdot S}$$

$$= 120 \frac{\mu A}{V^2} \cdot \frac{W}{L}$$

$Å = 10^{-8} cm$

$\varepsilon_o = 3.9 * 8.85 * 10^{-14} \frac{F}{cm}$

$A = F \cdot V$

$F = \frac{A}{V}$

mobolity $= cm^2 / V.s$ (volt)

$Q = C \cdot V$

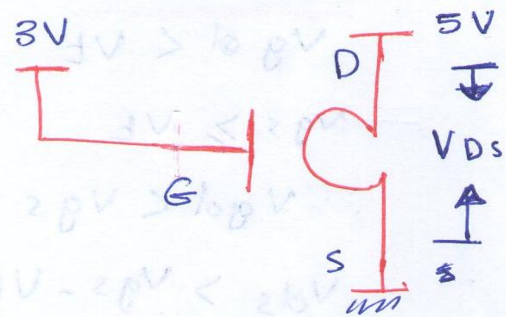
$I = C \cdot \frac{V}{s}$

$A = F \cdot \frac{V}{s}$

$F = \frac{A \cdot s}{V}$

$$\frac{\mu F}{V \cdot s} = \mu \frac{\frac{A \cdot s}{V}}{V \cdot s} = \frac{A}{V^2}$$

example :



assume

$V_t = 1$ volt

① if $V_{gs} \geq V_t$

$3 \geq 1$ ✓

∴ in conducting mode either linear or saturation

$V_{gs} = V_g - V_s$
$= 3 - 0 = 3$

$V_{DS} = 5$ V

$V_{DS} \overset{?}{>} V_{GS} - V_t$

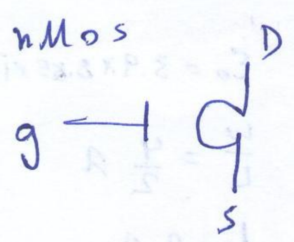
$5 > 3 - 1$

$5 \overset{?}{>} 2$ ✓

② ∴ Saturation mode

---

nMos



if $V_{gs} < V_t \Rightarrow$ off state

in n Mos

Vd sat

by default long

① long channel

$L = 0.25\ \mu m$

$V_{dsat} = V_{gs} - V_t$ مهم

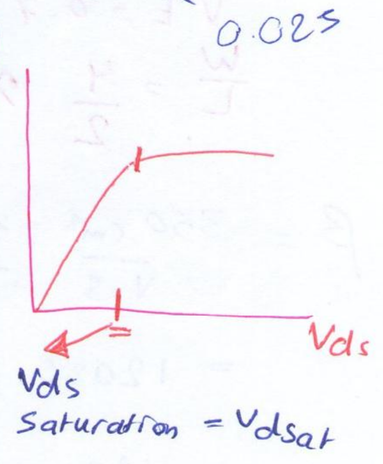
② Short channel

$L < 0.25\ \mu m$

$V_{dsat} < V_{gs} - V_t$ → linear بس

⇒ يعطيك اياها

Vd sat = Value



Vd sat: depend on technology of transistor

Channel pinches off in saturation if

$V_{gd} < V_t$

example /15

process = 65 nm (actual length of process)

length between 2n+ = 25 nm (minimum drawn length)

$\lambda = 25\ nm$

$w = 4\lambda \Rightarrow 100\ nm = 0.1\ \mu m$

$L = 2\lambda \Rightarrow 50\ nm = 0.05\ \mu m$

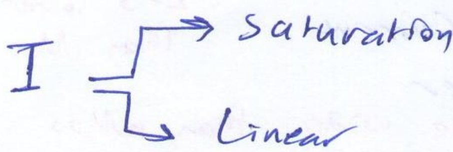
$\beta = \mu\ C_{ox} \frac{W}{L}$

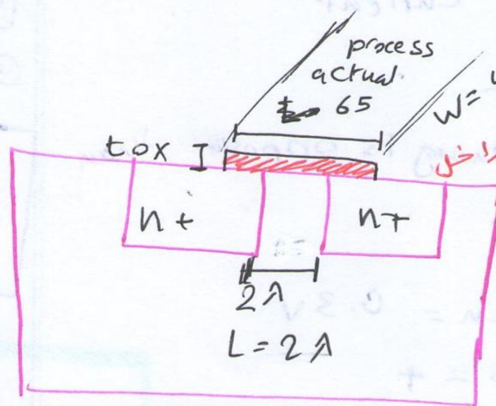
$C_{ox} = \frac{\varepsilon_o}{t_{ox}}$

$A^o = 10^{-8}\ cm$

$f = \frac{A}{V}$ Amper / Volt

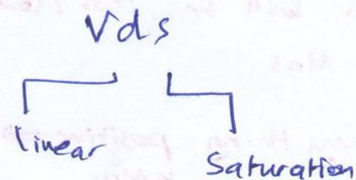
$\varepsilon_o = 3.9 \times 8.85 \times 10^{-14} \frac{f}{cm}$



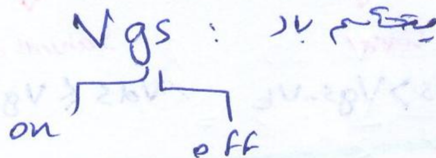


long channel

$\frac{W}{L} = \frac{4\lambda}{2\lambda} = 2$



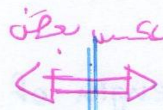
Vgs : يتحكم بال



EICoM
ELECTRICAL COMPUTER MECHATRONICS

الترتيب

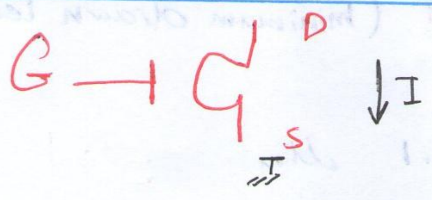
nMos

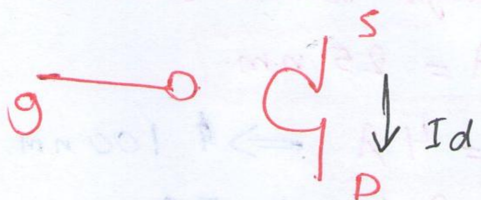


pMos

electrons

holes





nMos:

① The higher voltage is Drain and lower is Source

② Current D ⟹ S

③ μ_n : larger mobolity

④ larger Current

⑤ faster

⑥ everything is opposite than pMos

if $V_{tn} = 0.3\,V$

$V_{GS} = +$

pMos:

① higher is Source and lower is Drain

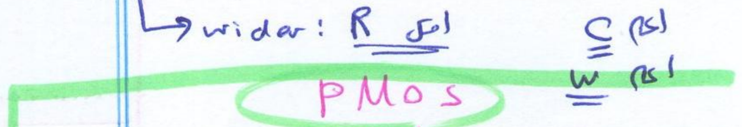
② Current S ⟹ D

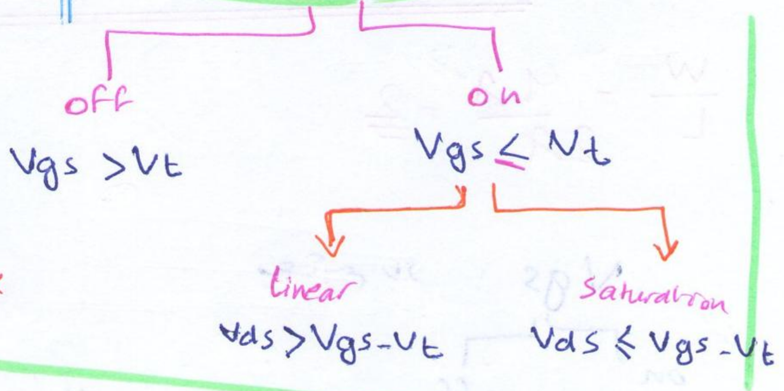
③ μ_p : Mobility of holes is lower Than Mobility of electrons

④ less Current — 2-3 lower Than μ_n

⑤ Slower — must be wider than nMos To provide same current

⑥ $V_{tp} = -0.3\,V$





nMos عكس كل الإشارات بـ

every thing greater in nMos will be less / lower in pMos

every thing positive ⟹ negative
nMos pMos

عكس الـ d / s والإشارات

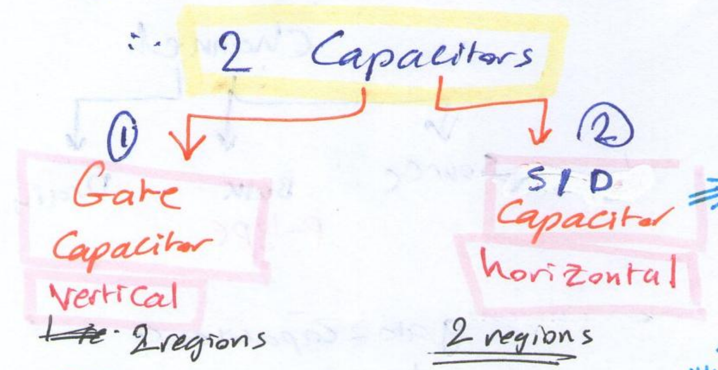
$$\frac{\mu_n}{\mu_p} = 2$$

Capacitance in nMos

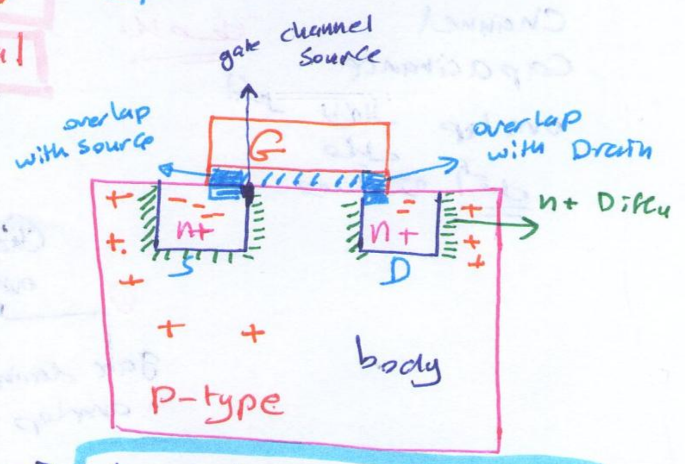
any 2 conductors separated by insulator = capacitance

When There is a Channel : ON state

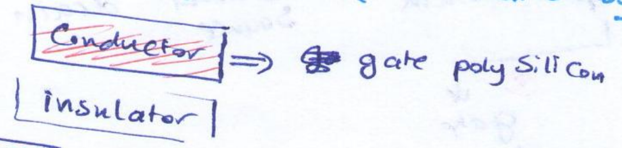
∴ 2 Capacitors



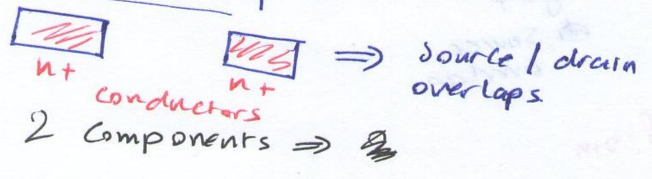
① Gate Capacitance :



Vertical Capacitance created by



⟹ gate polysilicon



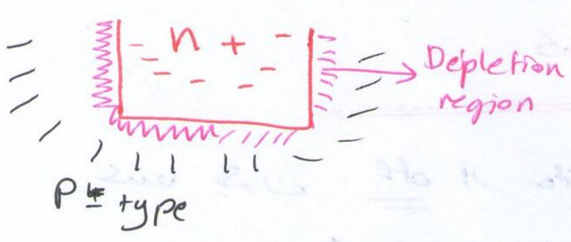
⟹ Source/drain overlaps ⟹ Channel with overlaps

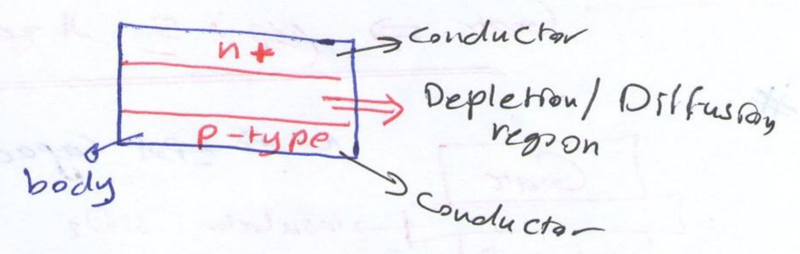
overlap : SiO_2 over n+ material

2 Components ⟹

② diffusion Capacitance : S/D region Source/drain Capacitance with body

horizontal capacitance when Ther Thin n+ material with p-type Then There is Diffusion region around source & drain will caused capacitance

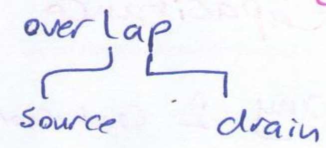


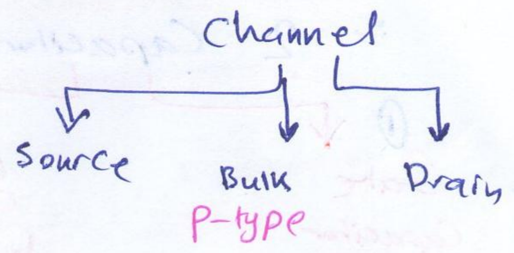


$C_o = C_{ox} WL$

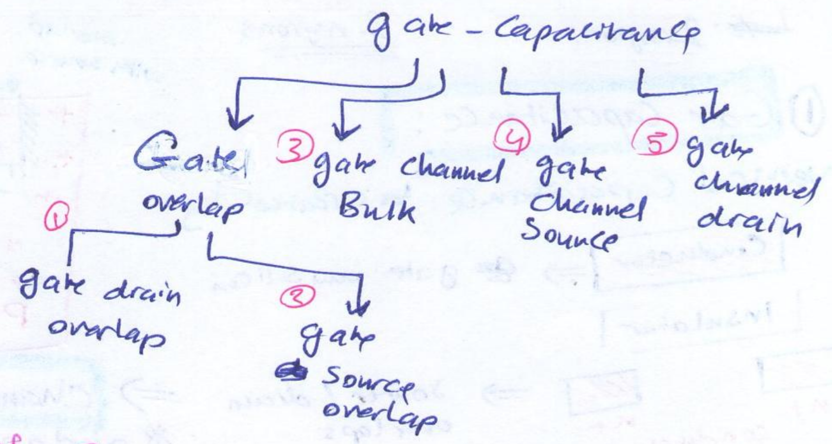
Channel Components :

1- gate channel source
2- " " Bulk
3- " " drain
4- gate drain overlap
5- " source "





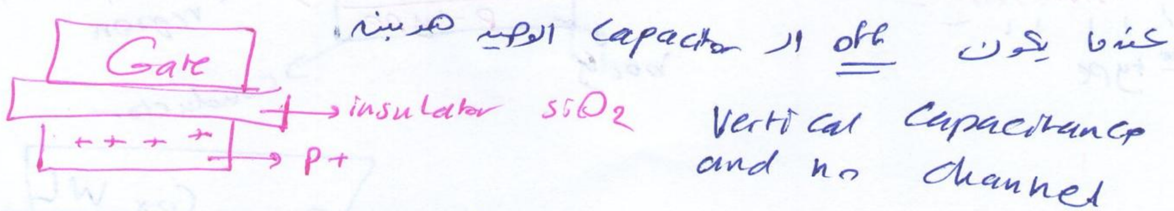
ملاحظة:
Channel capacitance الأكبر
overlap الأقل
مساحته أقل



Total capacitance of gate from drain = Channel component + overlap component

∴ Total = gate drain overlap capacitance + gate channel drain capacitance

Total capacitance of Gate ⇒ اذا طلب ⇐ بجمع ال 5 في الحل



عندما يكون ال off capacitor الوحيد هو vertical capacitance and no channel

gate capacitance : gate & channel component

at Cut-off state : Capacitance Created by bulk Component by holes

all Capacitance between Gate & bulk

⟸ عند تطبيق V_t على ال gate فإن ال Bulk capacitance

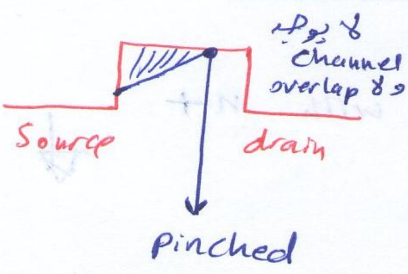
تختفي وتقل قيمتها لأن مفصول ال

ويبدأ ينشأ ال

↑ drain / Source Capacitance increases

يبقى الكلي نفسه

⟸ في حالة ال Saturation



لا يوجد drain Component

لأن ال Channel تصبح pinched

فقط كتب ال Source.

يبقى لدينا ٣ =
1 ← Channel-Source
٢ ← Channel-Bulk
٣ ← Source-gate-overlap

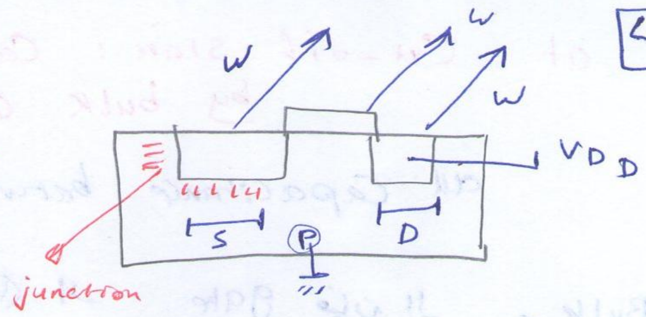
\# Capacitor in Saturation region = $\frac{2}{3}$ max value $\frac{2}{3} C_0$

Linear = C_0

Cut off = C_0

Saturation = $\frac{2}{3} C_0$

- ~~have~~ wall away from channel has special capacitance
- wall next to channel has special capa.
- bottom has....



⟹ assume channel with source..

$$C_{gs} = \frac{\varepsilon_{ox}}{t_{ox}} WL = C_{permicon} \, W$$ per unit

Diffusion Capacitance

[1] bottom capacitance (floor): P-type with n+

= junction capacitance * Area S/D

per unit area — ال bottom يتعامل مع وحدة المساحة

Area = W * D or W * S

Generally: bottom capacitance = factor * Area

factor = C_{JBS} Capacitance
↳ junction body to source capacitance

↳ in drain lets use C_{JBD}

V_{SB} = deferential voltage (source & body)

[2] Side wall capacitance

Total source diff capacitance

$$C_{sb} = AS * C_{jbs} + PS * C_{jbssw}$$

AS → bottom, per length

PS → walls side, perimeter per length

$A = WD$ or $A = WS$

$(PS) = W + 2D$ or $= W + 2S$

$$C_{jbs} = C_{jsw}\left(1 + \frac{V_{SB}}{\psi_0}\right)^{-M_j}$$

$$C_{jbssw} = C_{jsw}\left(1 + \frac{V_{SB}}{\psi_{sw}}\right)^{-M_{jsw}}$$

$n = 10^{-9}$
$P = 10^{-12}$
$F = 10^{-15}$
$\lambda = 0.25\,nm$
$W = 4\lambda$
$L = 2\lambda$
$D = 5\lambda$
$S = 5\lambda$

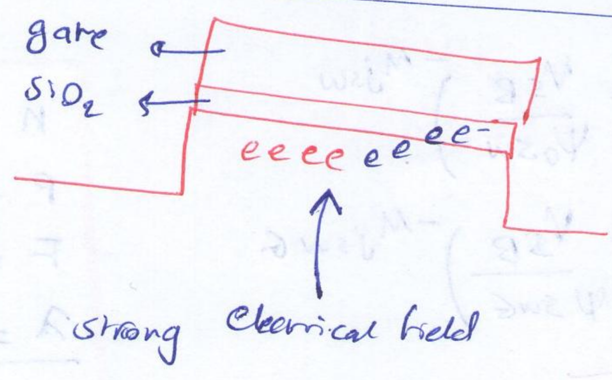
side wall abutting (كتب) Channel

$$C_{jbsswg} = C_{jsw}\left(1 + \frac{V_{SB}}{\psi_{swG}}\right)^{-M_{jswG}}$$

= Short channel enters saturation region very quickly

= Current has value but @ cut off stait is useless

⟹ ~~shrink~~ if transistors ~~are~~ shrinked
⟹ they will saturates quickly
and t_{ox} very small



الالكترونات بسبب تعرضها
لمجال كهربائي قوي
إما أن تحبس في
ال SiO_2 أو تختلط داخل
ال gate

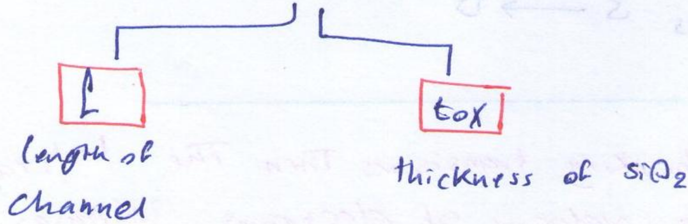
⟹ electrons which are trapped in SiO_2 will change the threshold of device
Then we need higher V_t : need higher voltage to establish channel

⟹ Shrink distance ⟹ larger electrical field
electrons will collide with SiO_2 atoms

Non Ideal Transistor Theory

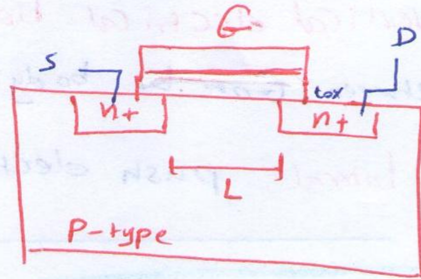
⇒ what happens when we shrink transistor ! nMos
using super technology

Shrinking transistor ; shrink physical dimensions of device

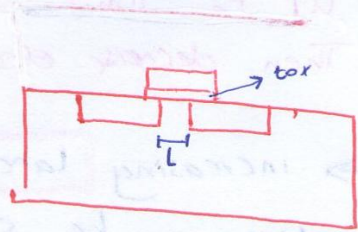


length of channel

thickness of SiO_2



after shrinking



⇒ ① lateral electrical field

$$E_H = \frac{V_{ds}}{L}$$

$v = \mu E_{lat}$ (v: velocity)

⇒ ② Vertical electrical field

$$E_V = \frac{V_{gs}}{t_{ox}}$$

⇒ Shrinking using super technology with same behaviour and same parameters to get smaller devices and faster

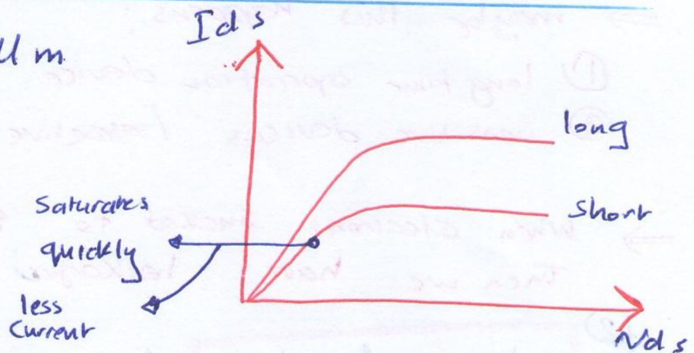
⇒ we want to get super technology

Shrinking tox & L ⇒ lateral & vertical $\underline{E}$ goes ↑ علاقة عكسية

---

long channel ≥ 25 nm = 0.25 μm

long channel is better because The current is greater ~~where The~~ since The current is The blood of The Transistor base of conduction



we don't Prefer short channel

- Velocity saturation ↑
- mobility depreciation

⇒ vertical electrical field: to establish channel between Gate & body

⇒ lateral: push electrons S ⟶ D

---

1 # Velocity saturation: Shrinking transistors Then The lateral electrical field Then The velocity of electrons increases UP to limit ⇒ electrons collides with SiO_2 Then decrease electrons speed in SiO_2 ⟹ saturates quickly

⟶ increasing lateral electrical field causes electrons be sucked by Gate (+ charge) and some electrons be trapped in SiO_2 causing increasing V_t because if we want to establish a channel we need higher voltage front of a layer of electrons in SiO_2
$I_{ds} <$ expected

⇒ maybe this happens:
① long time operation device
② sensitive devices / sensitive ccts

⇒ when electrons sucked to gate not drain Then we have leakage current

② ⇒ mobility degradation: decreasing t_{ox} & increasing vertical E causing increasing V_{gs} when electrons be sucked to gate and go out oxide and slowing their velocity.

increasing V_{gs} increases Current saturation :-

because of :

1. velocity saturation ⇒ lateral E
2. mobility degradation ⇒ vertical E

] → reduce Current in The device

Channel length modulation

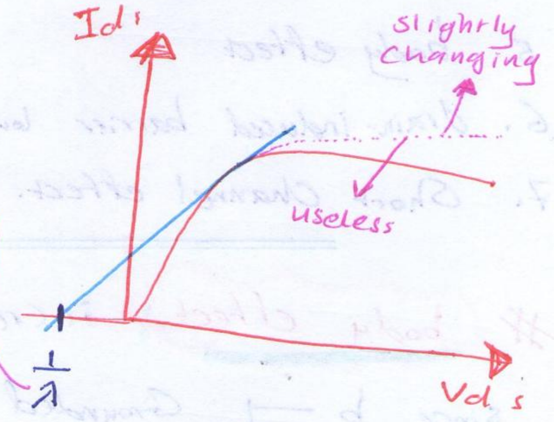
Current does change with ~~Vgs~~ Vds but slightly (useless change)

λ : Channel length modulation

$\lambda = 0.09$

$$I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2 (1 + \lambda V_{ds})$$ ⇒ non ideal

→ (saturation current)



نتحدث عند منطقة ال saturation فقط

⇒ Short Channel by increasing The Depletion region ⇒ increasing Vds

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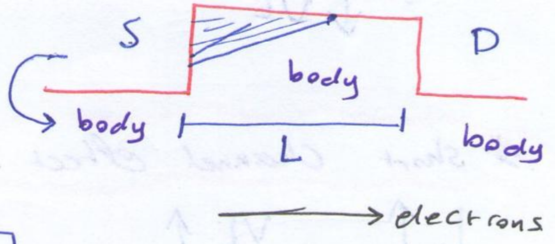
body effect

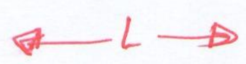
⇒ body affects on (1) Channel Through depletion region & affects on (2) V_t



1 → increasing V_{bs} (V_{SB}) increases V_t → نحتاج Vt أعلى لتحريك الالكترونات منا كـ

2 → increasing V_d V_t ↓
لإنه رح يصير حركة الالكترونات اسهل وبالتالي Vt أقل

3 → increasing L ⇒ V_t ↑
لأنه بدنا أكبر Vt لتحريك الالكترونات على طول أعلى وأكبر



Summary of Effects

non-Ideal effects

1. Shrinking Transistor
2. Velocity Saturation
3. mobility degradation
4. Channel length modulation.
5. body effect
6. drain-induced barrier lowering
7. Short Channel effect.
8. Leakage Current
9. temprature
10. Depletion region
11. electrical field

---

body effect: increasing $\underline{V_{sb}}$ but

since b — ⏚ Grounded ∴ $V_s \uparrow$ $V_t \downarrow$

increasing $\underline{V_s}$ ⟹ need higher V_t

more work to establish channel

↳ increase Δ between S & b

$V_t = f(\sqrt{V_{sb}})$ function

drain-induced barrier lowering:

increasing V_d ⟹ making Creating channel easier

∴ $\downarrow V_t$ $V_d \uparrow$ $V_t \downarrow$

← D goes to S

short channel effect: ⟹ increasing Depletion region

$L \uparrow$ $V_t \uparrow$

increasing length of channel making Creating it

need higher $\underline{V_t}$

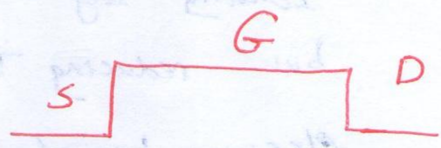
لأنه إحنا رح نزيد عدد ال electrons

ع طول ال $\underline{L}$

leakage Current : When transistor in OFF

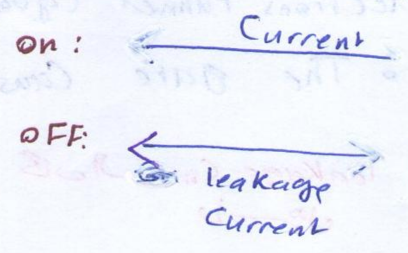
happens when transistor is in off-state

from [illegible] to [illegible]



and This because of 3 reasons (sources):

1. SubThreshold Current.
2. leakage Gate.
3. Diffusion leakage.

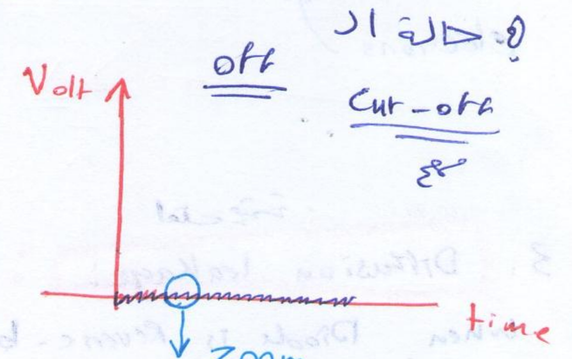


① subThreShold Current: will be partially on

at $V_{gs} = 0$ $V_s = 0$

في حالة ال off
Cut-off

because of The activity of surrounded ccts ⇐
activity of other circuits
and no actual activity in This transistor
-GND is switching



Gnd is switching due to other ccts

ON لحظة أن ال transistor هو توقع
لكنه اصلًا كان off

SubThreshold Conduction: $V_{gs} < V_t$ ⇒ off state

Current drops off exponentially.

⇐ اعتماد خارجي فقط وال GND

⟵ ال Sub اصعب والمرجح. لانه عم استعملها بحوت هناك Volt ويصبح هناك leakage.

When Channel is <u>ON</u>

2. Gate leakage in <u>on</u>-state

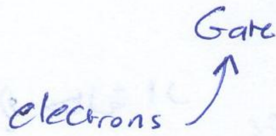
Ideally $I_g = 0 \Rightarrow$ non ideal $\Rightarrow$ slightly changing

but reducing Thickness of oxide $\Rightarrow$ reducing number of atomic layers

electrons tunnel (goes through) or sucked to The gate Causing leakage Current

كل ما كانت صغيرة ال tox اقل ⇐ كان ال leakage Current اكبر وأسهل.

هذه ,حالة تحضيريا



Vertical field —

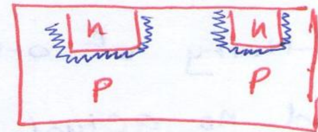
tox —

اقل حجة.

3. Diffusion leakage: off-state

When Diode is Reverse-biased

$(P + n) \Rightarrow$ Diode in RB

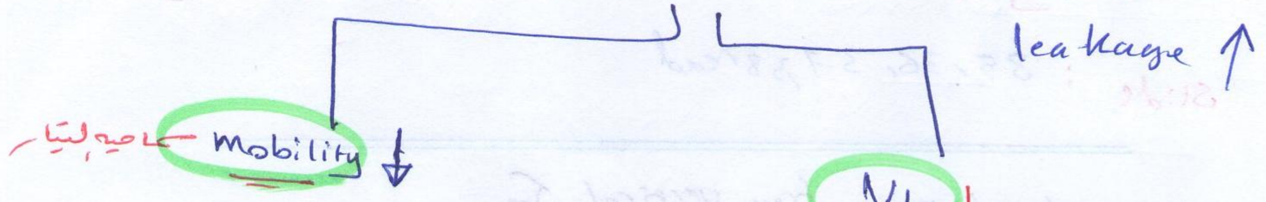


$\Rightarrow$ any Diode in reverse biased has a leakage Current

Small Value

Temprature affects on Transistor

as temprature goes up ↑



leakage ↑

Mobility ↓ — عاميليتيا

V_t ↓

makes I ↓

علاقة طردية

$I = \beta ...$

$\beta = \mu ...$

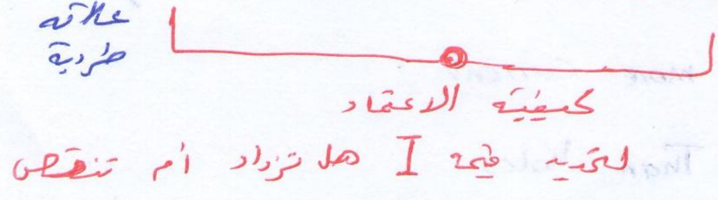
علاقة طردية

makes I ↑

علاقة عكسية

$I = V_{gs} - V_t$

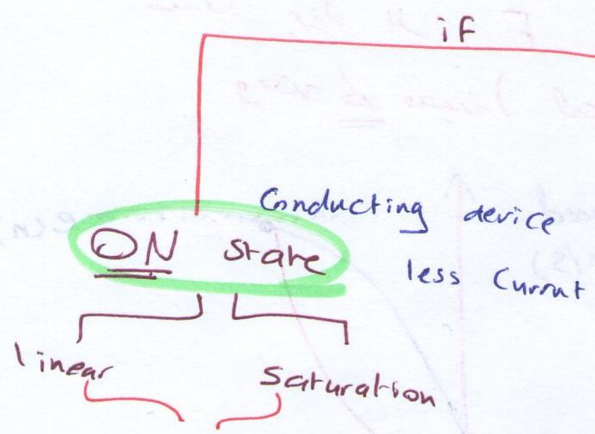
عكسية



كيفية الاعتماد

التيار فيه I هل تزداد أم تنقص

if — if



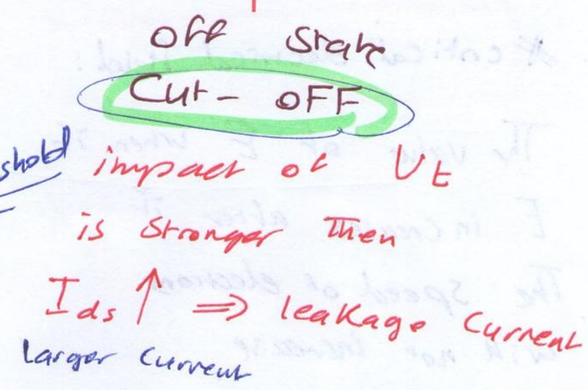
Conducting device

ON state — less Current

linear — saturation

impact (effect) of μ is stronger Then I_{ds} ↓ with increasing Temprature

SubThreshold OFF



off state

Cut-OFF

impact of V_t is stronger Then I_{ds} ↑ ⇒ leakage Current

Larger Current

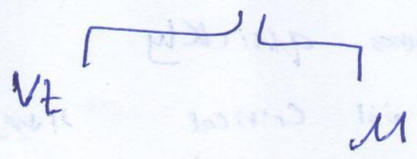
عشان كده بنحتاج Cooling Center عشان ما تنقل رحمة التيار

not to waste power & slow current

مهم جداً :

هذا الكلام كله فقط للـ nMos

اذا طلب منا pMos عكس الصدور فقط



V_t — μ

Vertical electrical field attracts electrons

To open (Create) channel

⇒ modeling is needed to reduce The Complexity

Slide : 35, 36, 37, 38 read

---

mobility degradation: from vertical E

⇒ lateral : accelerates The electrons : The more Voltage The higher Current

→ faster electrons : more current

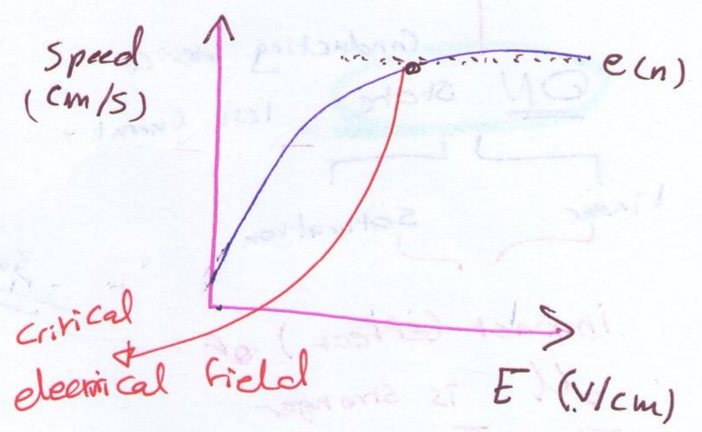
electrons faster Than holes

عندما يزداد ال E فإن حركة ال e أو P تزداد

وعند حد معين (Critical) بحيث لا يمكن أن تزيد عند هذا الحد.

critical electrical field:

The value of E when it E increases after it The speed of electrons will not increase



long channel better Than short channel

Since we need more current

short saturates quickly

$$E = \frac{V}{L}$$

الفولت

اذا كانت L كبيرة مش ح توصل ال Critical اذن # افضل

Current In Saturation region it does has dependency on Vds but its weak and usually neglected

not entirely ind on Uds

λ: Channel length modulation

$$I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2 (1 + \lambda V_{ds})$$

λ = 0.09 small

تختلف حسب الرسومة. Vds

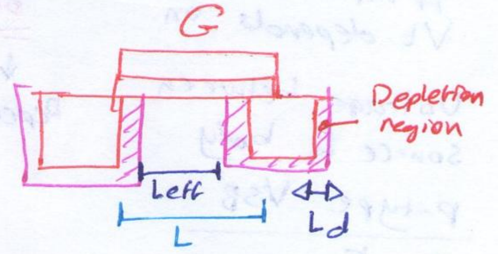
L = 2λ

Depletion Region: region between n & p where There is no any Carrier.

width of DR ↑ as Reverse bias ↑

Depletion region increases as Vd increases

$$L_{eff} = L - L_d$$



Threshold effects V_t — non ideal

V_t: The needed Voltage to be applied on The gate to Create a channel and allowing The Current to Start from S to D

⟹ ideal: V_t is Constant

V_t: has weak depends on:

3 depends

- **Body Voltage (Body effect)**
- **Drain Voltage D-I B L effect**
- **Channel length — Short channel effect**

Body Voltage (Body effect)

V_t depends on Voltage between source & body p-type V_{SB}

If S not grounded Then $V_{SB} > 0$ but There is dependency

$$V_t = f(\sqrt{V_{SB}})$$

علاقة طردية.

Nominal Threshold

∴ $V_{SB} = 0$

Source: grounded

e.g.: increasing V_{SB} $0 \to 0.6$

V_t increasing by 0.04

Drain Voltage — D-I B L effect

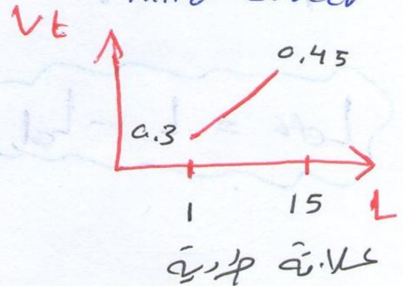
- off → Depletion
- on → Channel length modulation in Saturation

53 رح نشرحه

2 ص

Channel length — Short channel effect

Third effect



علاقة طردية

as length of channel becomes longer ⟹ V_t be larger

if long channel we need large V_t to establish long channel with large number of electrons need larger work ≈ potential

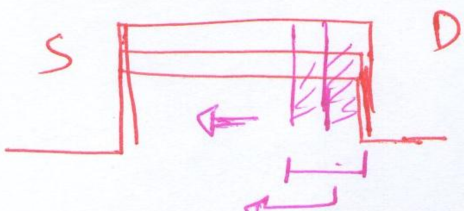
second effect

Drain Voltage effects of DIBL

V_t by 2 modes / ways

off — in Cut-off mode

applying more voltage on Drain Then more Depletion area
L_d be larger
an L_{eff} be Smaller
⇒ Drain is moving toward source



Depletion region

D داخلة الزيادة على الفولت عند الجهاز

Then $V_t \downarrow$ why:
The channel Creation will be easier since L_{eff} is smaller

$$V_{t_{new}} = V_{t_{old}} - n\, V_{ds}$$

n ⇒ factor

on — in Saturation mode

Through channel length modulation
⇒ I_{ds} increases sligtly in saturation with V_d increases

⇒ Depletion region in long channel is ignored because because depletion region is so small size compared with long channel it can be ignored

it has more effects on Short Channel

slide 43 السؤال

13 صوت منه

36 → 40

leakage Current:

* type of current happens in off state and its not desirable... it happens due to 3 effects causing it:

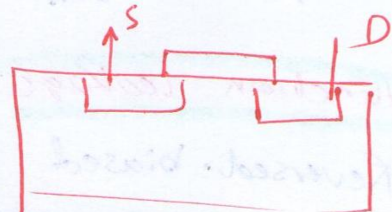
① SubThreshold current → its The Killer and its The main effect because it will switch The value of Ground Causing channel on and cause Gate & Drift

② ~~Lea~~ Gate leakage

③ Diffusion leakage

→ Sources of leakage Current

leakage S ⟹ D



⇒ in SubThreshold: transistor: gate not exactly at 0 volt is partially turned ON

20 → 30% of current

⇒ Gate: when channel is ON high potential between Gate & ~~b~~ body. electrons escape to Gate as they flow S ⟹ D

⟹ Diffusion Junction: very slight ignored created

SubThreshold: ~~Killed~~ Killer and high

we reduce Vt to speed up transistor

Then Vt↓ SubThreshold current ↑ عكسية.

لانه مو يصير أي مشكلة طول ال transistor رح تأثر فيه وتحركوا وصوبار off

⇒ SubT current كلما قلت ال Vt يصبح اكثر مشكلة ونزداد ال

Sub Threshold conduction:

less than Vt → when channel is off

- transistors Can't be abruptly ON / off (~~Dimer~~) (Dimmer)

  بشكل مفاجئ

- Dominant source in contemporary transistors

  المسيطر — المعاصرة، الحديثة

Gate leakage ⇒ on: high potential between g & body

Tunneling through ultrathin gate dielectric because tox is thin.

as tox is thin current will escape through

if tox is thiner ⇒ Gate leakage is larger

important tox 65 nm   tox = 10.5 Å

ignore tox > 20 Å

Junction leakage:

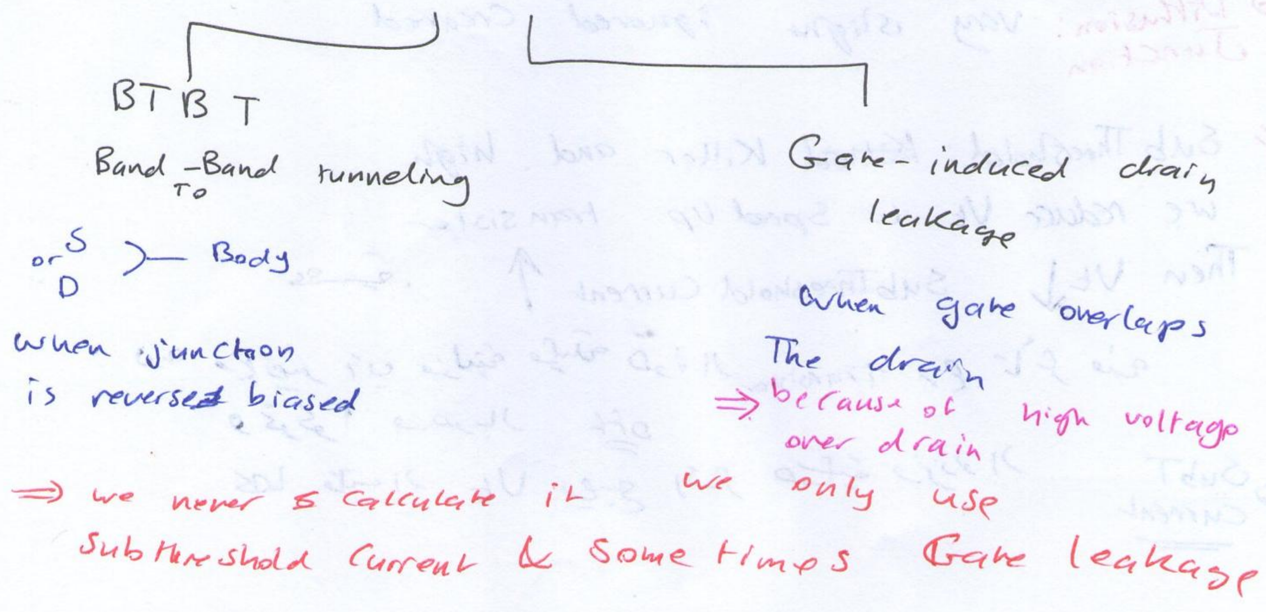
Reversed-biased PN junction diode Current

Junction leakage

$\text{Å} = 10^{-10}$

⇒ reverse-biased:

$V_p \leq V_{n+}$



⇒ we never calculate it we only use Subthreshold current & sometimes Gate leakage

Gate leakage: at 19 Å tox

if tox ↓ ⇒ Gate leakage ↑
Current

because it will be easier to escape

$Å = 10^{-10}$

$$I_D = I_s \left(e^{\frac{V_D}{V_t}} - 1 \right)$$

$$I_D = -I_s$$

I_s depends on doping level

exam:
Vds = __
Vgs = __
① find I
② find W given acct

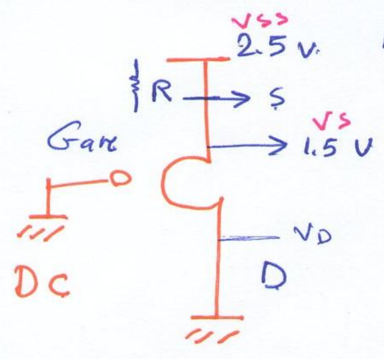
---

example: find W of transistor

Channel length = 0.25 μm
→ long channel

⇒ ignore CLM (λ)
Channel length modulation

$R_S = 20\ K\Omega$



$K' = \beta' = \frac{W}{L} \beta'$

pMos

① $\because I_s = \frac{2.5 - 1.5}{20 K\Omega} = \frac{1}{20 \times 10^3} = 50\ \mu A$

$V_d = 0$
$V_s = 1.5$
$V_{ds} = -1.5$
$V_{gs} = 0 - 1.5 = -1.5$
$V_{tp} = -V_{tn} = -0.4$
$30\ \frac{\mu}{V^2}$

② V_{ds} ☐ $V_{gs} - V_t$
-1.5 $-1.5 - (-0.4)$

$\because V_{ds} < V_{gs} - V_t \Rightarrow$ Saturation

$$\therefore I = \frac{\beta}{2} (V_{gs} - V_t{}^2) = \frac{W}{L} \beta' \frac{(V_{gs} - V_t)^2}{2}$$

$$50\ \mu m = \frac{W}{2 \times 0.25 \mu} \cdot 30 \frac{\mu}{V^2} (-1.5 + 0.4)^2$$

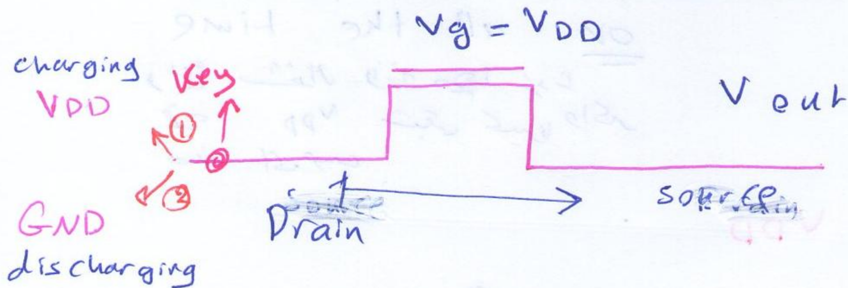
DC Characteristics

we ever assumed $V_s = 0$ (grounded) — nMOS

now what if $V_s > 0$ (or $V_D > 0$ in pMOS)

nMOS: will charge till $V_{DD} - V_{tn}$, no higher

pMOS: no lower than V_{tp}



nMOS

$V_{gs} > V_t$

$V_{DD} - V_{out} > V_t$

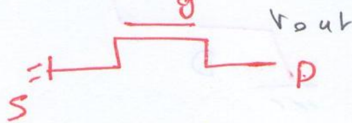
$V_{out} < V_{DD} - V_t$

$V_{gs} > V_t$

nMOS

① Charge untill $V_{DD} - V_{out} > V_t$ (Bad)

in discharging



$V_{gs} > V_t$

$V_{DD} \rightarrow V_t$

discharge untill $V_{DD} > V_t$

~~Vout~~ in charging:

تزداد كل $V_{out} < V_{DD} - V_t$ ⟹ لأنه مغطيا الفترة الزمنية طالما أن $v_{gs} \le V_t$

$V_{DD} - V_t$

---

charge to $V_{DD} - V_t$

discharge down to 0

discharging

$V_{gs} > V_t$

$V_{DD} - 0 > V_t$

$V_{DD} > V_t$ → قيمة ثابتة لا تتغير طالما أنها ال gate

good discharge

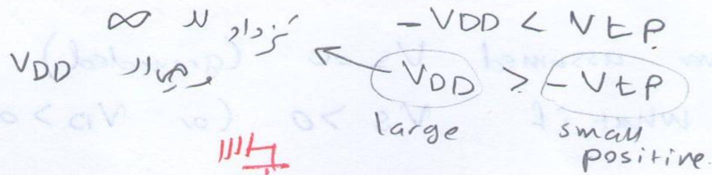
bad charger

V_{gs} alway = V_{DD}

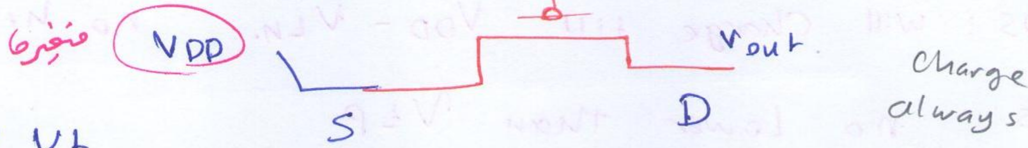
will not change so it will discharge all time

← كيف التميز أن ال VDD gate لا تتغير بينما ال VDD key تتغير

P Mos



① charging



$V_{gs} \leq V_t$

$-V_{DD} \leq V_{tp}$ always

$V_{DD} > -V_{tp}$

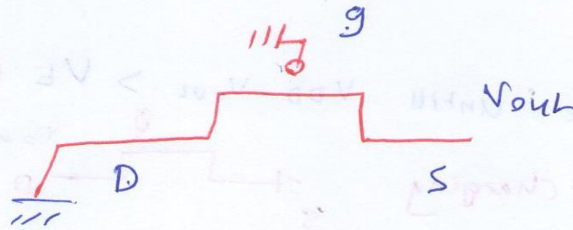
<u>on</u> all the time

واذا شغال وانه هيا زدنا
جهد VDD شبقى كبيرة واكبر
من المطلوب

∴ good charger

charging till V_{DD}

② discharging



$V_{gs} < V_t$

$-V_{out} < V_{tp}$

$V_{out} > -V_{tp}$

positive — positive but very tiny

discharge until $V_{out} = V_{tp}$

شغال طالما ان Vout
اكبر من -Vtp

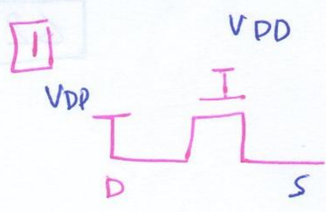
∴ bad discharger

تقل لحد معينة

V_{tn} : positive

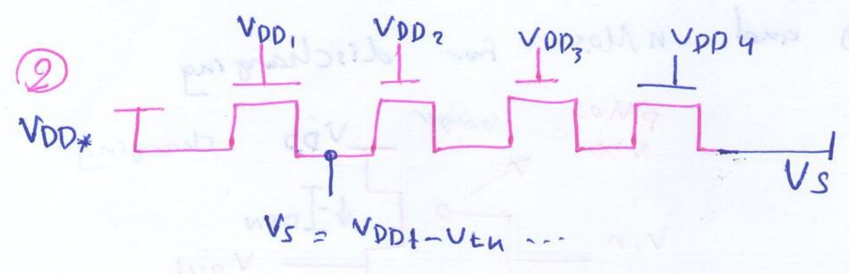
V_{tp} : negative — $-V_{tp}$: positive value

1



Charging $V_S = V_{DD} - V_{tn}$

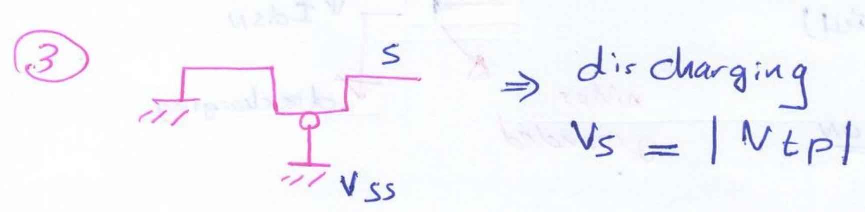
2



$V_S = V_{DD4} - V_{tn}$

بغض النظر عن الـ قبلها

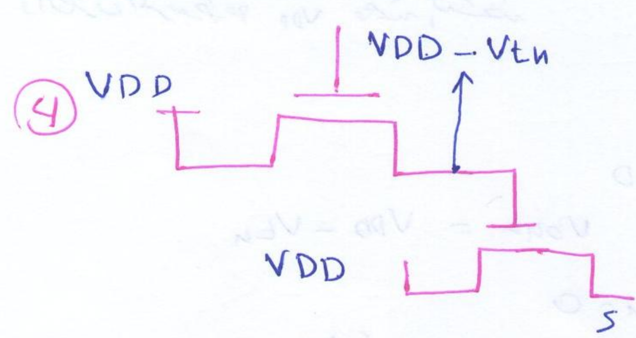
3



$\Rightarrow$ discharging

$V_S = |V_{tp}|$

4



Charging

والمهم فولت الـ Key

$V_S = (V_{DD} - V_{tn}) - V_{tn}$

$V_S = V_{DD} - 2V_{tn}$

$\therefore$ pMos : good charger
Bad Dis charger

$\therefore$ N Mos : Bad charger
good Dis charger

EICoM
ELECTRICAL COMPUTER MECHATRONICS

Inverter

Consists of 2 Transistors → p, → n.

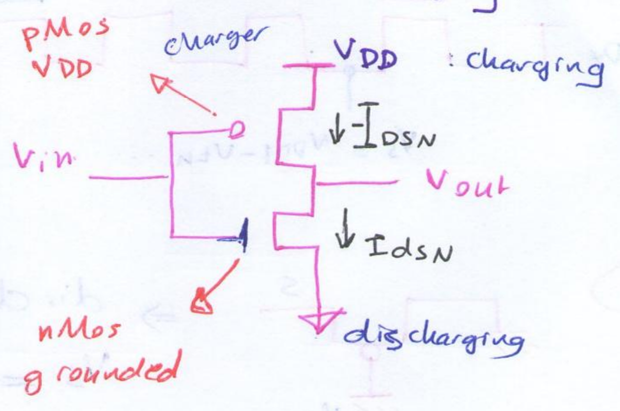
P mos for charging and n Mos for discharging

when $V_{in} = V_{DD}$

The nMos is ON

Then it will discharge

$V_{out} = 0$ (GND الترفع)

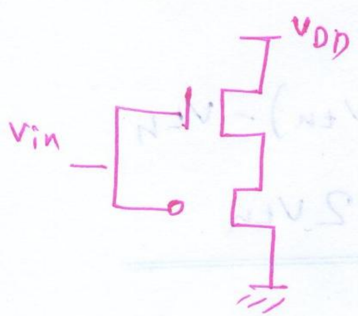


if $V_{in} = 0$ PMos ON

Charging until $V_{out} = V_{DD}$ ⇒ inverses The Value of Vin

الارتفاع GND يعمل كالمفرغ
والطرف المربوط VDD معتبر الشحن

What if



if $V_{in} = V_{DD}$
charge until $V_{out} = V_{DD} - V_{tn}$

and when $V_{in} = 0$
discharge until $V_{out} = (-V_{tp})$

So its not good

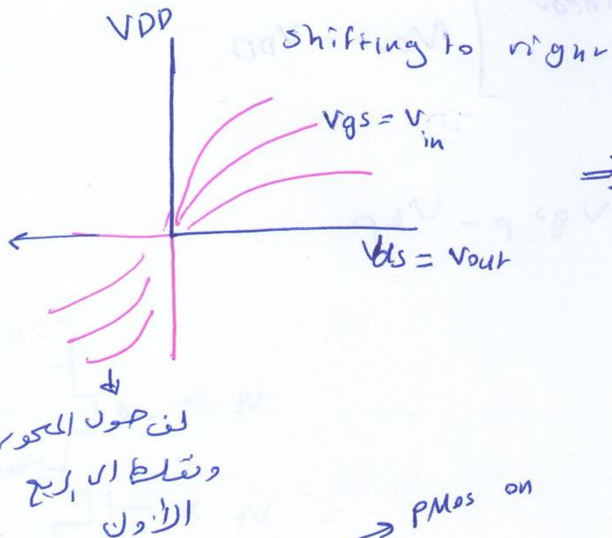
⇒ both above cases depend on:

① Transistor size
② Current

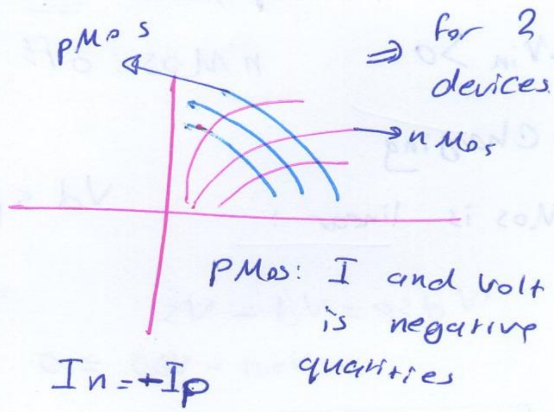
We will start talking about inverters

Vin : changing ⇒ transient analysis

* operating points → cut off / linear / saturation ⇒ regions



⇒



→ pMos on

for ← $V_{out_p} = V_{dd} + V_{dsp}$

$V_{dsp} = V_{out} - V_{DD}$

for pMos ← $V_{out} = V_{dsp} + V_{DD}$

⇒ pMos.

right to shift

⇒ intersections: operating regions for the inverter

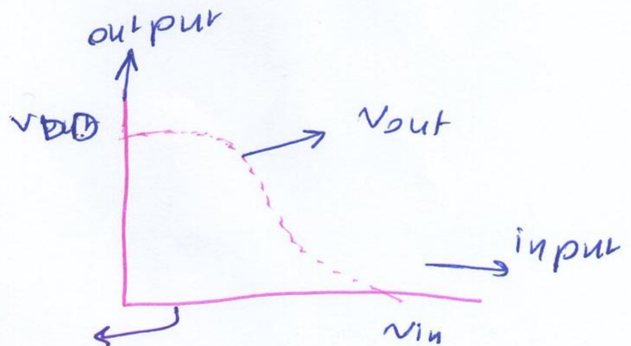
I max in the middle

⇒ Characteristics Curve

describes function of device

Vout inverter plot

~~when~~



as we change V_{in} ~~cha~~ ⇒ change region
change output

Characteristics curve for inverter is divided into 5 regions

① region A

$V_{tn} > V_{in} > 0$

pMos: on & linear
nMos: off
] $V_{out} = V_{DD}$

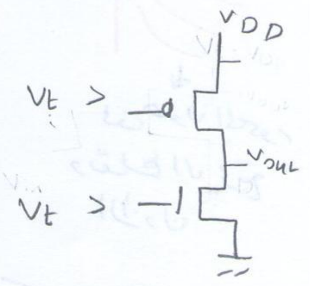
⇒ Charging

pMos is linear : V_{dsp} [ ] $V_{gsp} - V_{tp}$

$V_{dsp} = V_d - V_s$

$= V_{out} - VDD = 0$

$V_{gs} = V_g - V_s$ large negative



(V_{tp}) negative

0 [ ] large negative + small positive

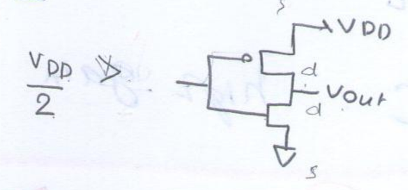
0 [>] negative ⇒ Linear

② region B

now nMos will be on

$V_{out} > \frac{V_{DD}}{2}$
Vin

$\frac{V_{DD}}{2} > V_{in} > V_{tn}$



$\frac{V_{DD}}{2} >$

nMos ⇒ on

V_{dsn} ☐ $V_{gsn} - V_{tn}$

$V_d - V_s$ ☐ $V_g - V_s - V_{tn}$

large ☐ smaller

saturation

PMos : ON

V_{dsp} ☐ $V_{gsp} - V_{tp}$

$\frac{V_{DS}}{2} <$ [>] أكبر سالب
أقل (-)

linear

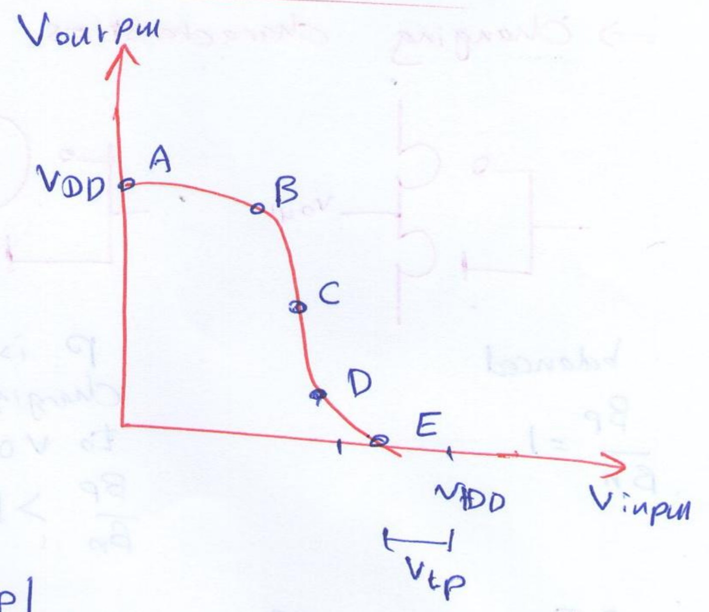
A $V_t > V_{in} > 0$

B $\frac{V_{DD}}{2} > V_{in} > V_{tn}$

C $V_{in} = \frac{V_{DD}}{2}$

D $V_{DD} - |V_{tp}| > V_{in} > \frac{V_{DD}}{2}$

E : $V_{in} > V_{DD} - |V_{tp}|$



A : off(n) on linear (P) — $V_{out} = V_{DD}$

B : on linear (P) on saturation (n) — $V_{out} > \frac{V_{DD}}{2}$

C : on saturation n, P — Vout sharply $V_{out} = \frac{V_{DD}}{2}$

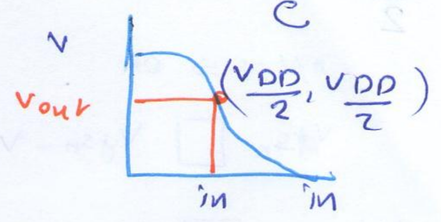
D : (saturation P) (linear n) — $V_{out} < \frac{V_{DD}}{2}$

E : off P (on linear n) — $V_{out} = 0$

A : n off

E : P off

C : high gain both saturation

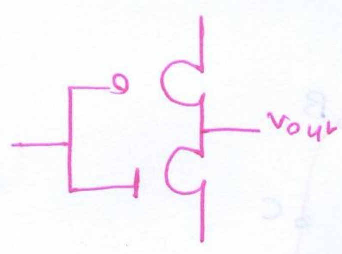


$$Gain = \frac{\Delta\ output}{\Delta\ input}$$

C : saturation region when $V_{in} = V_{out}$

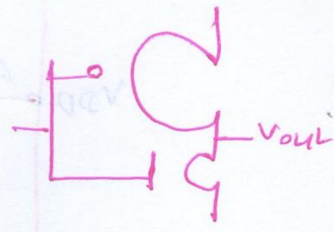
$V_{in} = V_{out} = V_{inv}$ at C region

⟹ changing characteristics curve



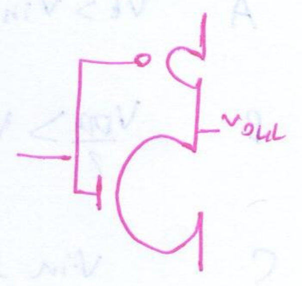
balanced

$\frac{\beta p}{\beta n} = 1$



p is stronger
charging quickly
to VDD

$\frac{\beta p}{\beta n} > 1$



n stronger
discharging
faster

$\frac{\beta p}{\beta n} < 1$

⟹ These cases shifting plot but same shape

⟶ shifting to right
β larger
P Mos stronger & larger
ratio larger

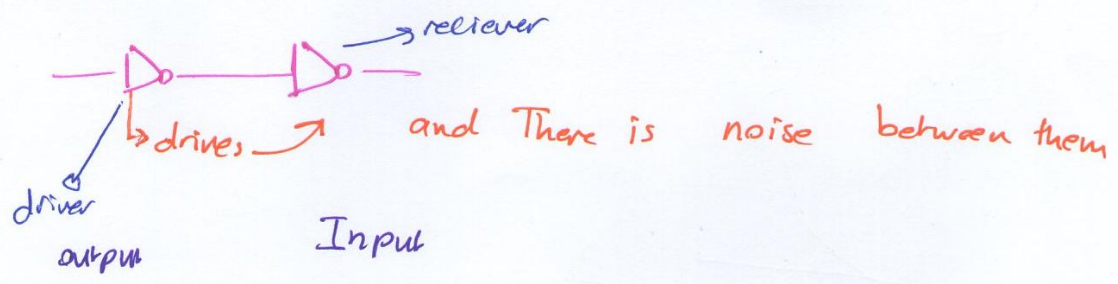
skewed gate

Noise Margin:

مناعة / اوزمتن

كلما كان ال margin قليل كان اكثر مناعة حتى لو كان ال noise قليل

specially in GND

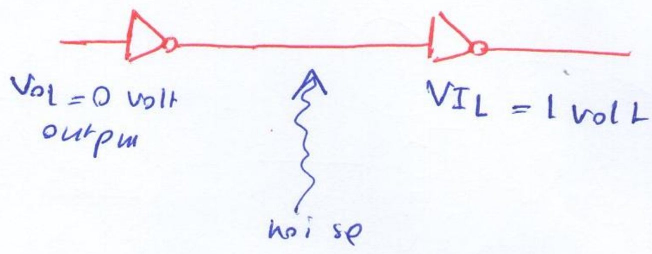


and There is noise between them

noise margin = $V_{OH} - V_{IH} = NM_H$ Logic high input

$V_{IL} - V_{OL} = NML$ Logic low

example



if noise = 0.5 volt ⇒ take it as 0

اي حاجة صفر

$NM_H = V_{OH} - V_{IH}$ (V_{OH} = VDD)

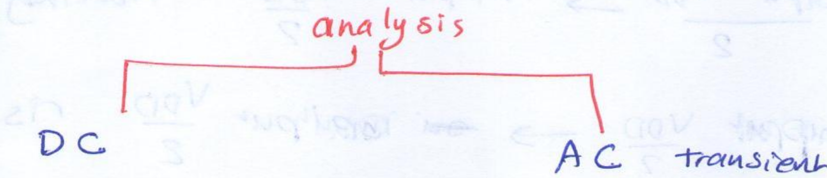
~~$NM_L = V_{OL} - V_{IL}$~~ (0)

NML = input low − output low

Ch.5

Response- delay

Transient Response: Delay



DC: I and V constraints

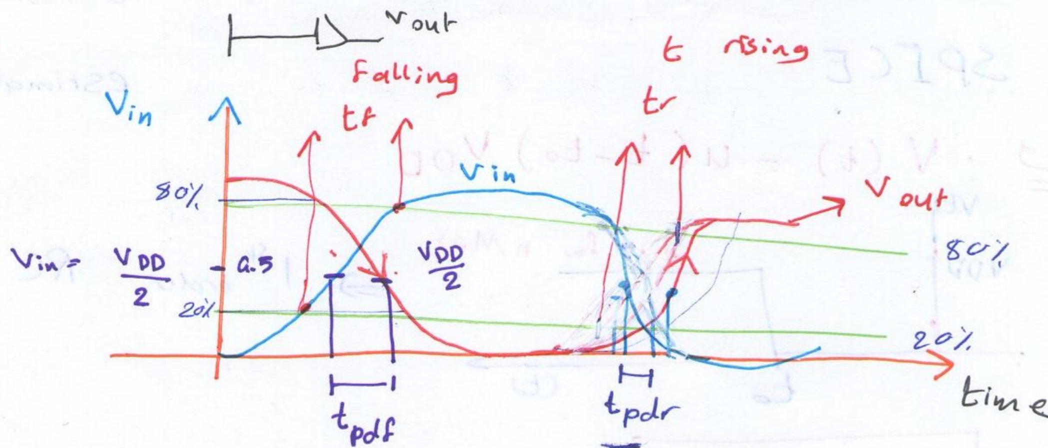
AC transient:
- delay
- power
- energy
- sizing

$\Rightarrow$ $I(t)$, $P(t)$, $V(t)$ is time variant function of Time

$\Rightarrow$ how we are going to go from DC $\longrightarrow$ AC

Delay

for inverter



tpdf: propogation delay to falling

tpdr : prop. delay rising

tr = rising time from 0.2 to 0.8 VDD
tf = falling time 0.8 to 0.2 VDD

: how to up $\Rightarrow$ in output curve

كلما قل ال time
كان اكثر sharp
واكثر سرعة.

$$\text{average propogation delay } t_{pd} = \frac{t_{pdf} + t_{pdr}}{2}$$

$\Rightarrow$ 2 types of delays

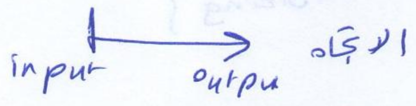
Delay Definitions

t_{pdf} Input $\frac{V_{DD}}{2}$ → output $\frac{V_{DD}}{2}$ falling ~~bedr~~

t_{pdr} Input $\frac{V_{DD}}{2}$ → ~~ou~~ output $\frac{V_{DD}}{2}$ rising

⇒ delay is due to V_{out} → falling t_{pdf} / → rising t_{pdr} — البداية من input

الاتجاه

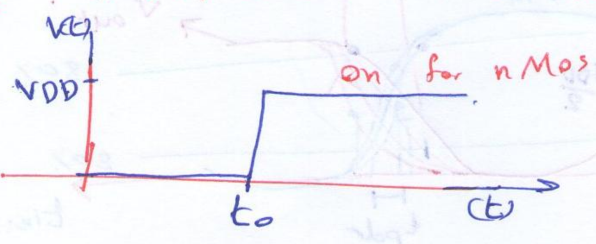


Simulated Inverter Delay

simulators to fasten work

SPICE — estimate delay

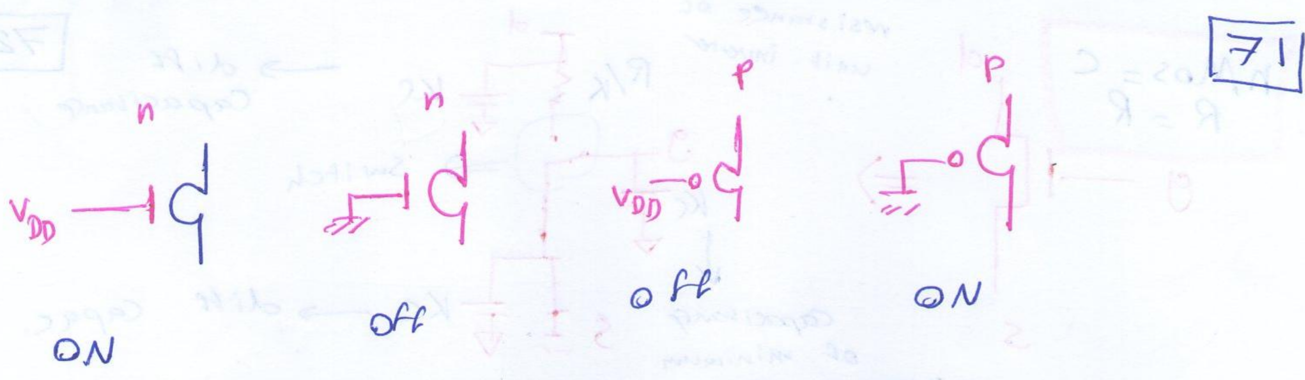
e.g: $V(t) = u(t - t_o) V_{DD}$



⇒ 1st order RC response

$$t_{pd} = RC$$

$$Q = CV$$



$Q = C_o V$ $\quad\quad$ $I = C \dfrac{dV_{out}}{dt}$

$\dfrac{dV_{out}}{dt} = \dfrac{I}{C_{load}}$ → function ⟶ off, linear, Saturation

C_{load} → Constant

⟹ if transistor replaced by Resistor & capacitor its very good RC cct

$t_{pd} = RC$

How ??

every transistor has a $\underline{R}$

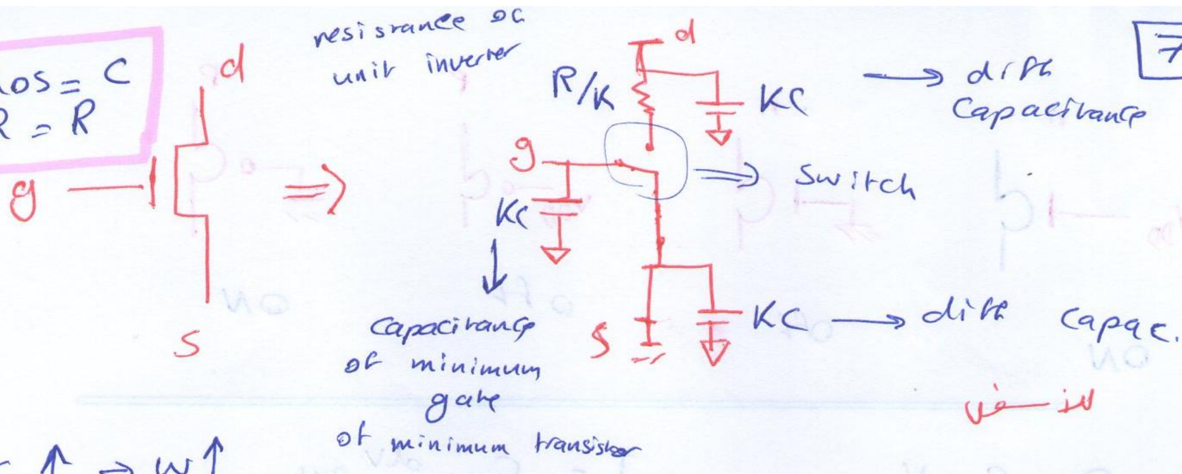
K: is The minimum size

minimum $\frac{W}{L} = \frac{4\lambda}{2\lambda}$

$K \cdot \frac{W}{L} = K \cdot \frac{4\lambda}{2\lambda}$ K: any number above 1

$R_{eff} = \frac{R}{K}$

nMos = C
R = R



$C \uparrow \Rightarrow W \uparrow$

$W \uparrow \Rightarrow R \downarrow$ علاقة عكسية

$L \uparrow \Rightarrow R \uparrow$

$I \propto \frac{W}{L}$

$I \propto \beta$

$I \propto \frac{1}{R}$

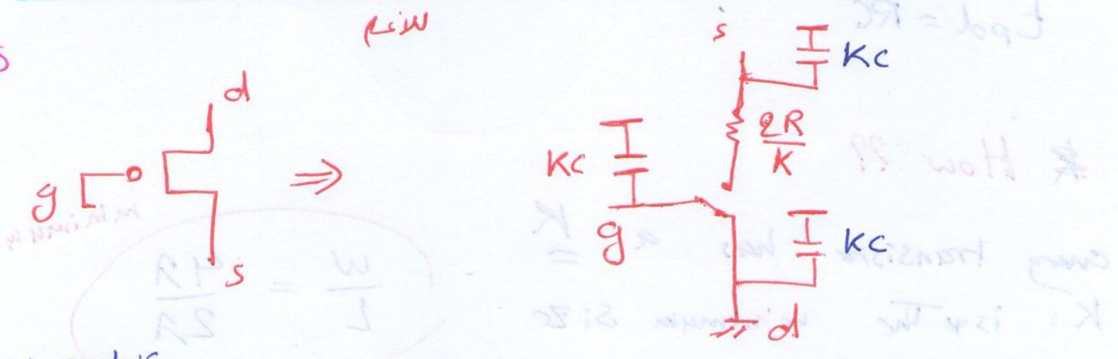
$I \propto \frac{1}{L}$

L : alway untouched

دائماً اللي نزيد هو W عشان هيك الـ R تقل بمقدار K

للأعلى

PMos
C
2R



C : W تزداد مع
R : W تقل مع

Why 2R : $\mu_p = \frac{\mu_n}{2}$

اذن نضاعف الـ R عشان نثبت الحجم

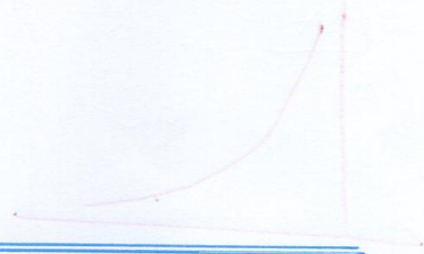
C : Capacitance of unit size $\frac{W}{L}$ $\frac{4\lambda}{2\lambda}$

R : Resistivity " " "

$C = 2fF/\mu m$ $W = 0.6\ \mu m$ $1fF/65nm$

$R = 10K\Omega$ $L = 0.6\ \mu m$

$1.25K$ $L = 65nm$



Transistor in RC: is just like switch

effective Resistance: ratio $V_{ds} \rightarrow I_{ds}$ cross switch

---

fanout of 1- inverter

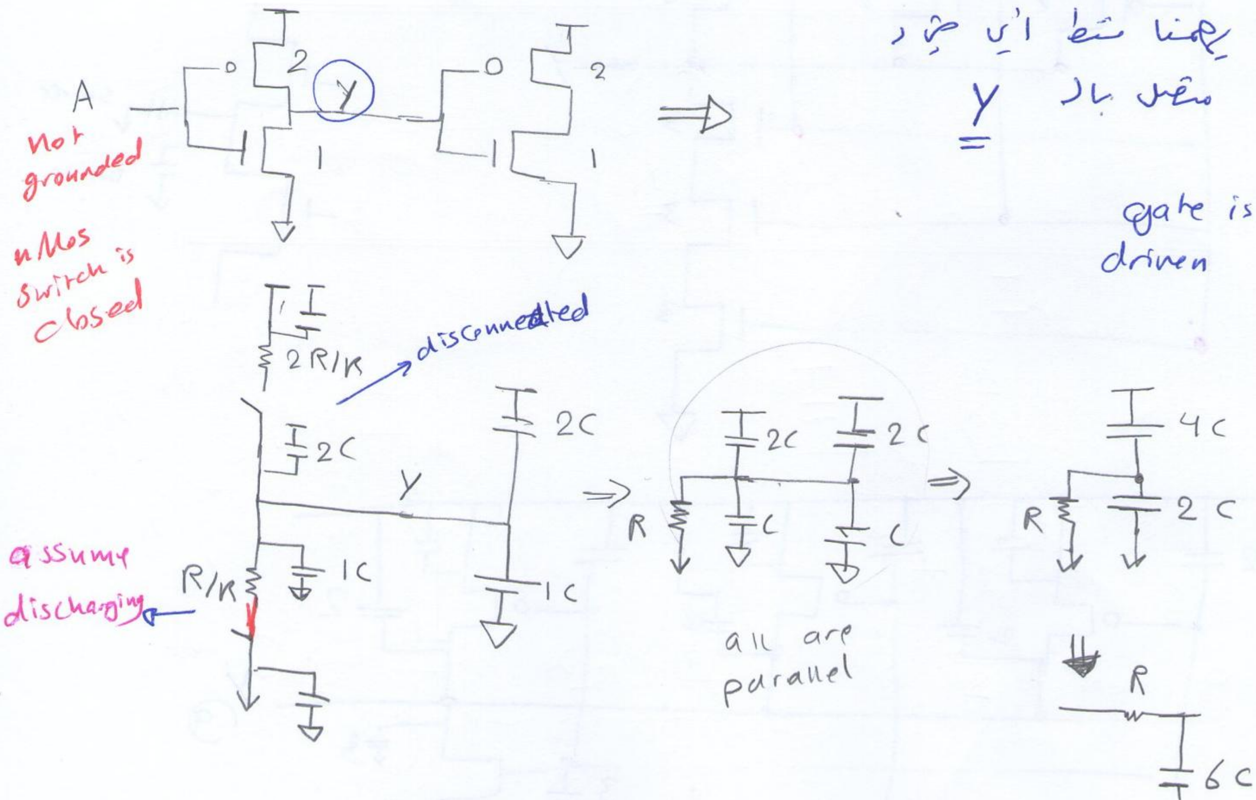
Y: out

assume only one switch is on other is off

نقطه تحت ای چیز

متصل بار Y

gate is driven

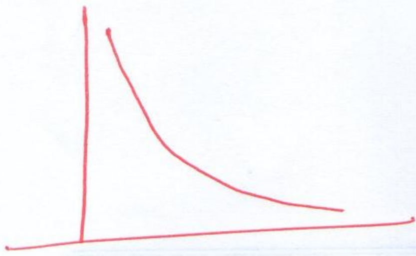


d (output) = 6 RC

delay = 6 RC = R(6C) Reff = R

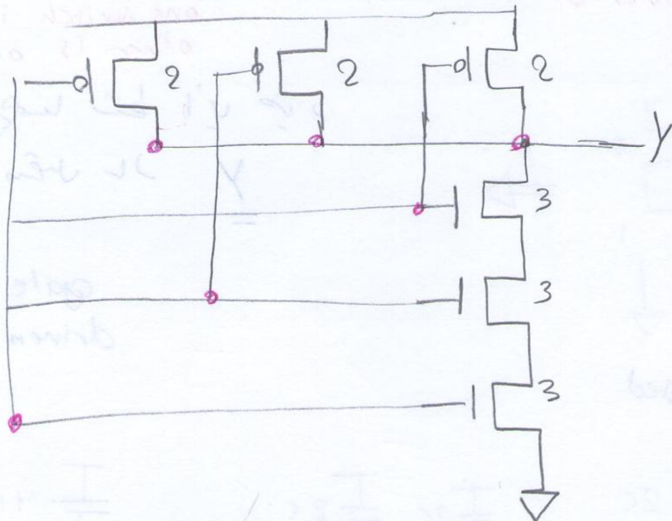
$\Rightarrow$ remove any device connected to V_{DD} or GND in both terminals

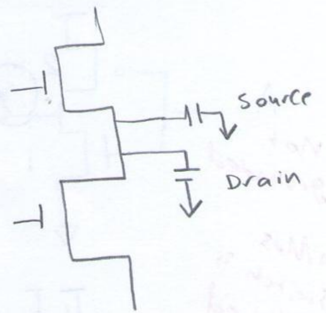
Discharging

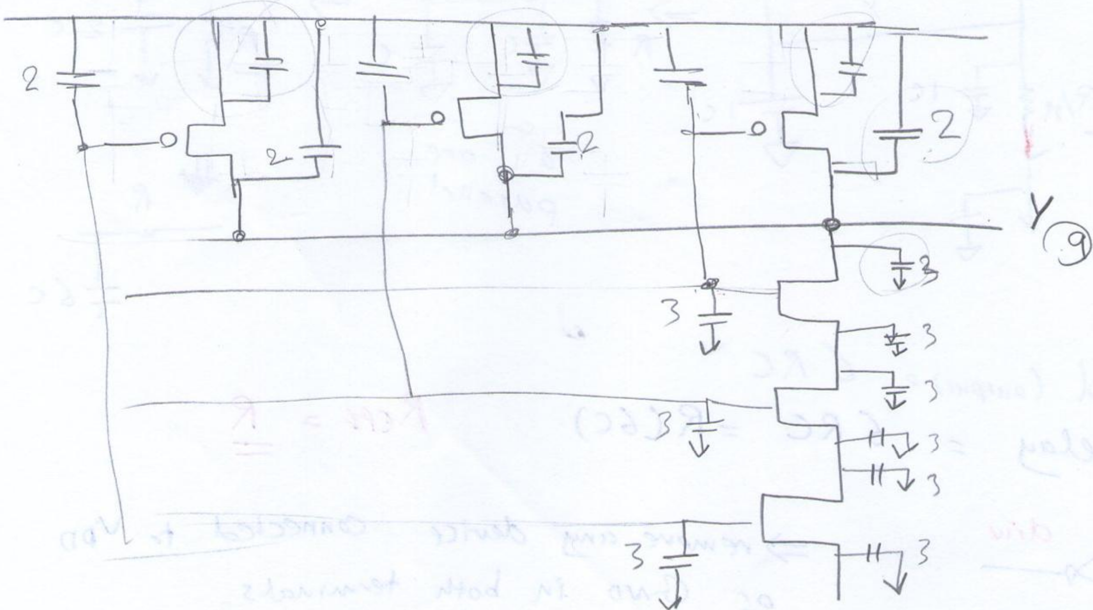


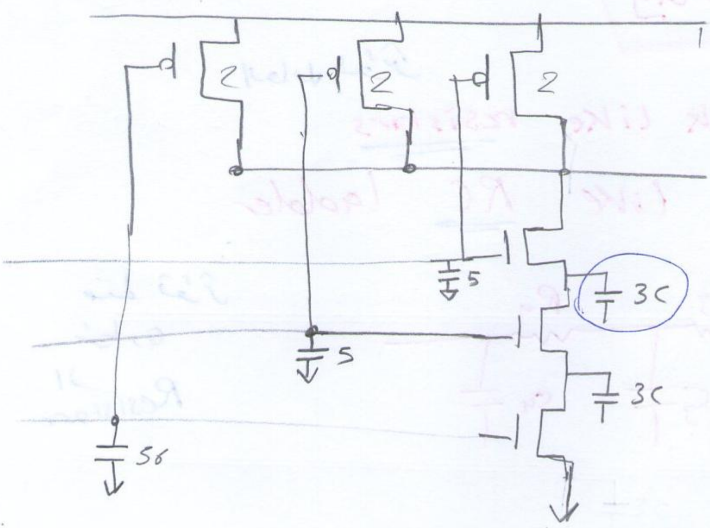
(3- Input Nand Gate) P vs n us

replace nMos & pMos with RC ccts









: can be shared
1 diffusion (over lapped)

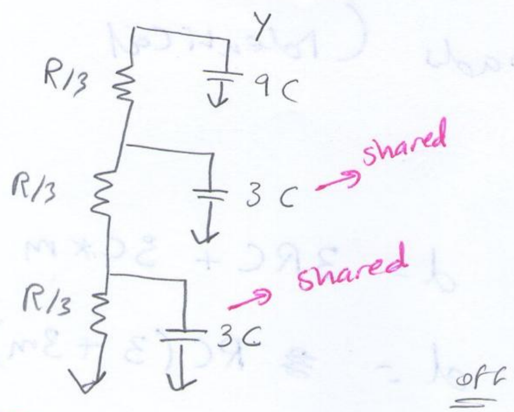
الشروط

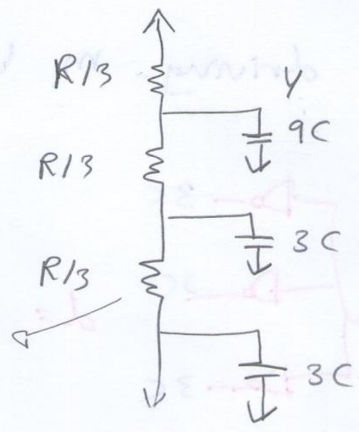
① Same type
nMos + nMos
pMos + pMos

② Same size

③ in Series

how lets add R_s
for falling & rising





falling

rising

R عم بتوازي كم effective R = R

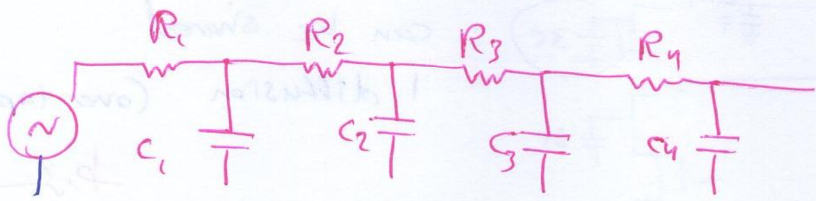
$$R_{eff} = \frac{R}{3} + \frac{R}{3} + \frac{R}{3}$$

Elmore Delay

العامل المؤثر

ON transistors look like resistors

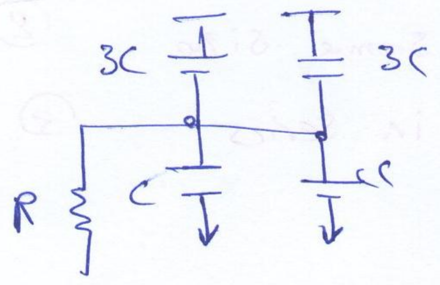
pullup & pulldown like RC ladder



مقط مؤثر
زي ال
Resistors

$t_{pd} = RC_1 + C_2(R_1+R_2) + C_3(R_1+R_2+R_3) + \cdots$

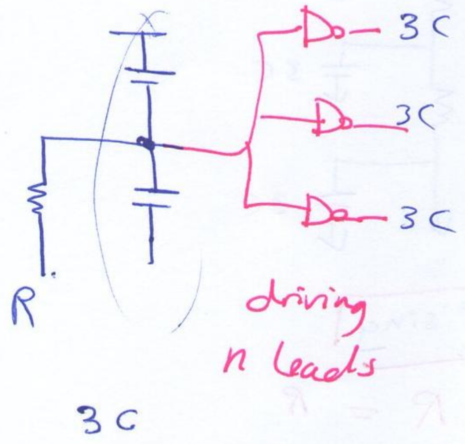
$d =$,,



$d = 6RC$ if

if driving 1 load

⟹ what if driving m loads (identical



3C

$d =$

$d = 3RC + 3C * m$

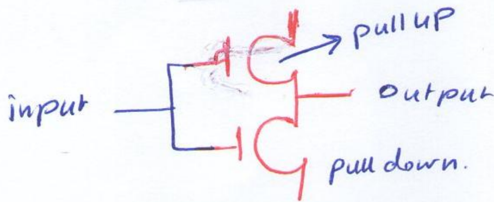
$d = RC(3 + 3m)$

Lecture 6
Combinitional

Complementary CMos

Complementary

Inverter



nMos : pull down
pMos : pull up network

up : Charging VDD
down : disch Vss

up / down	off	ON
off	Z	1
ON	0	X → Crowbar

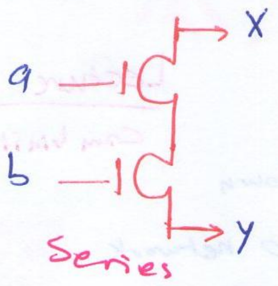
on: must be a path

Z State : "float output"
high impedence isolated from pMos & nMos
↳ not connected to niether VDD or Vss (GND)

1 state : Connected only to VDD and isolated from Vss so state is up (high) = 1

0 state disconnected from VDD and connected to Vss

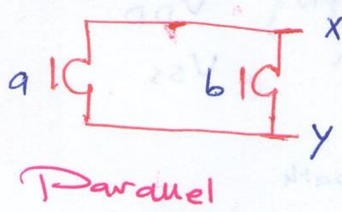
Crowbar State : Connected to both VDD and Vss in same time then its short cct from VDD → Vss and its not desirable



⇒ to transform from $x \to y$

"a" and b must be both ON

Series



$X \to y$

a or b must be on

one ON at least

Parallel

Series	⇒	and
parallel	⇒	OR

⇒ nMos

تكلم عن ذلك بالنسبة للـ nMos لكن الـ pMos عكس ذلك التوصيل

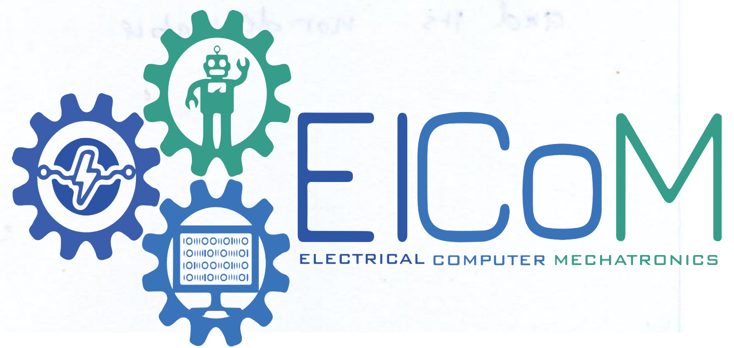
⇒ path to VDD ⇒ 1

" " Vss ⇒ 0

⇒ what ever is series in nMos ⇒ its Parallel in pMos والعكس صحيح

⇒ pullup is complement of pulldown

⇒ in CMos we cannot build OR or and without inverter



A	B	1 $\overline{A.B}$	2 $\overline{A+B}$
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	0

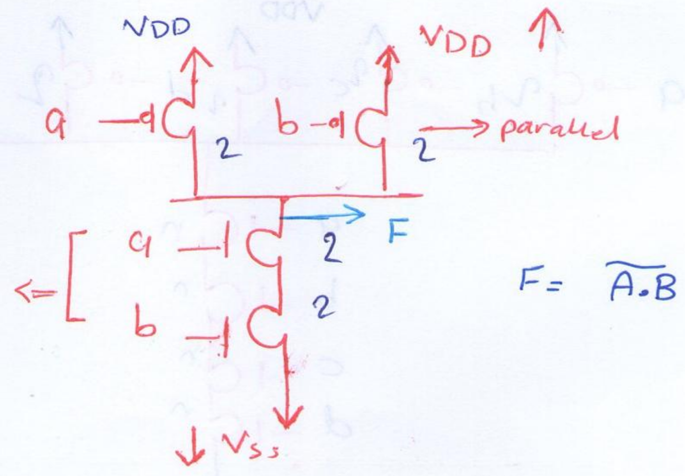
Nand

① اولاً عندما تكون $\overline{A.B}$ (and)

نفصل الـ nMos على التوالي لأنه and

ونفصل الـ pMos على الـ

1= Construction Nand gate



$F = \overline{A.B}$

① if $a = 0$, $b = 0$

nMos ⇒ OFF

pMos ⇒ ON

∴ output is VDD

∴ $\overline{A.B} = 1$ → charging

② if $a = 1$, $b = 1$ — nMos on, pMos off] ⇒ $\overline{A.B} = 0$ — path to VDD is blocked discharging

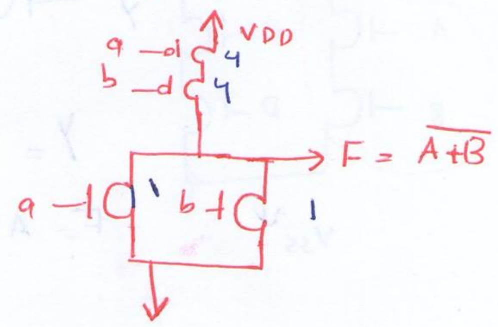
③ if $a = 0$, $b = 1$] ⇒ connected to VDD ⇒ charging

2= Construction NOR Gate

② عندما تكون $\overline{A+B}$ (OR)

نفصل nMos على التوازي

pMos = التوالي



① if $a = 0$, $b = 0$

nMos OFF

pMos ON

F = 1 VDD charging

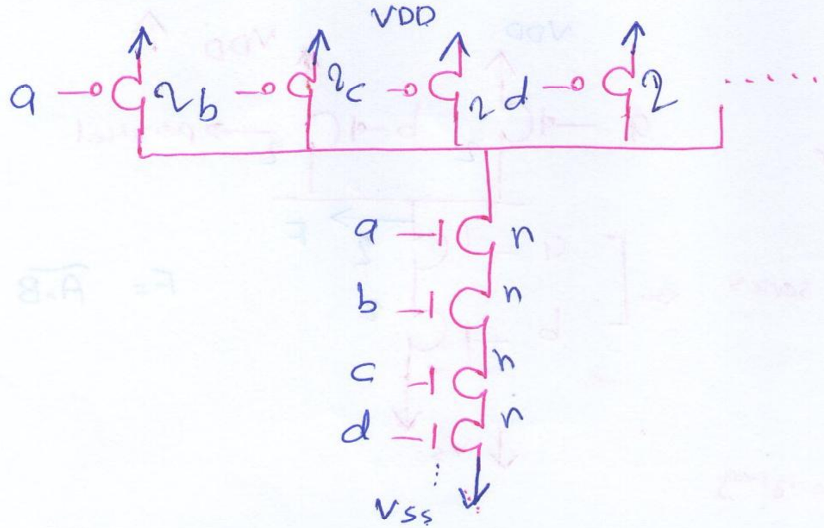
② $a = 1$, $b = 1$

F = 0 Vss discharging

③ $a = 1$, $b = 0$ — pMos off, connected to Vss — F = 0 discharging

→ expanding Nand Gate

adding other inputs C, D, E, ... to series nMos and C, D, E to Parallel pMos



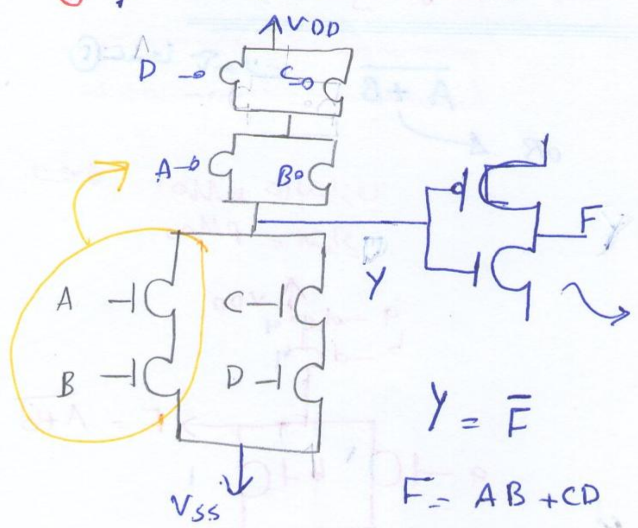
Compound Gates

make sure OR = inversion of NOR
and = " "

e.g ① $Y = \overline{(AB + CD)}$

← أولاً نبدأ برسم كل العلاقات بالـ nMos
ثم نعكس كل شيء بالـ pMos

OR = Parallel
and = Series



فقط لنفيها اذا طلب OR

عكس كل شيء
توصيل P

$AB + CD = \overline{AB} \cdot \overline{CD}$

$= (\bar{A} + \bar{B}) \cdot (\bar{C} + \bar{D})$

= حلقة الوصل الرئيسة

! ⇐ الانتباه لموضوع الـ inverter أما في حال يطلب الـ inverter نضع هنا مثال $Y = AB + CD$

مع

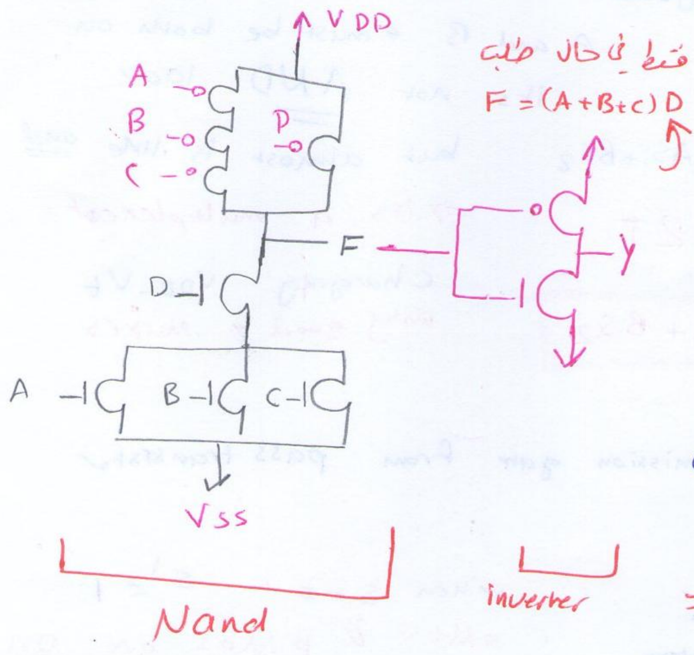
اذا طلب OR أو and نحتفظ بـ inverter لأن نفي النفي إيجاب

2 $Y = [(A+B+C)D]'$ => O3AI

$((A+B+C)D)'$

$\overline{(A+B+C)} + \overline{D}$

$\overline{A}.\overline{B}.\overline{C} + \overline{D}$



O3AI (الاسم)

OR 3 and Input

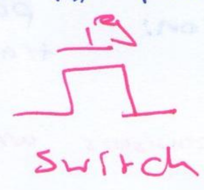
Nand — inverter = and

Strength of signal: قوة الاشارة

How its close to ideal voltage source

nMos pass strong 0 → dis : best for pull-down
degraded or weak 1

pass Gates : as switches



pMos pass strong 1 → charging
degraded or weak 0

g = 0 ——→ on   VDD 1 strong (if input 1)

g = 1 —/— off   Vss 0 degraded (if input 0)

→ pass transistors produce degraded outputs

→ but transmission gates pass 0 & 1 well ✓

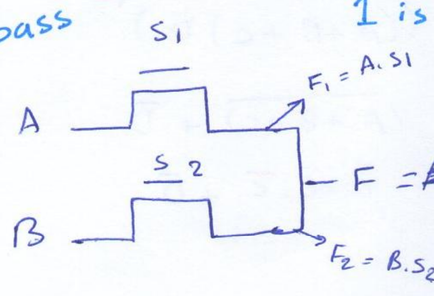
produce degraded value unlike transmission gate produce well values

no any degraded

Transmission gates

pass

1 is not good



F = $AS_1 + BS_2$

2T

العلاقة بين S وال A

A and B must be both on

its not AND 100%

but almost is like and

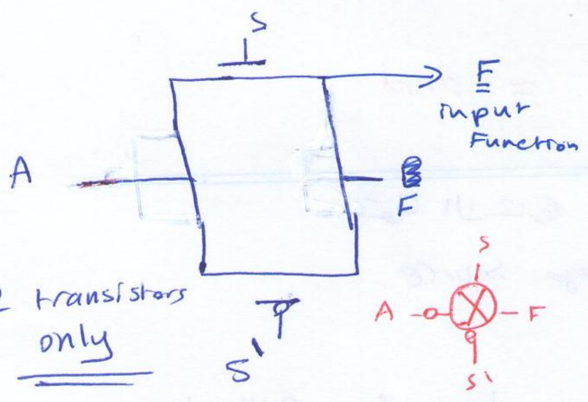
=> its a multiplexed

Charging $V_{DD} - V_t$

Only good in Muxes

pass transistor = $AS_1 + BS_2$

→ How to build transmission gate from pass transistor

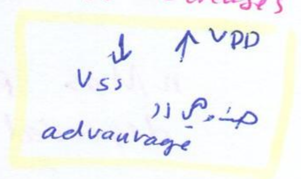


2 transistors only

when S = 0   S' = 1

∴ nMos & pMos are ON in The same time but not short cct ($V_{DD} \to GND$)

but here are on same time to make 0 increases to V_{DD} and V_{DD} decreases To 0



transmission: جات كل مشكلة ال pass transistors in Muxes

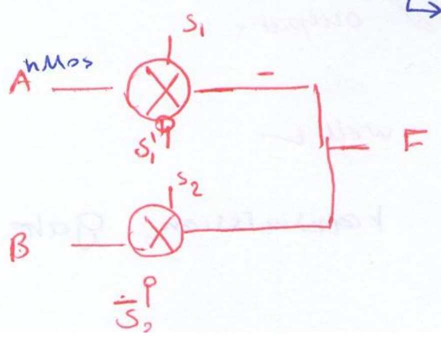
in pass transistors we only use nMos but in Transmission Gates we use pMos & nMos in parallel

=> nMos continue Charging to $V_{DD} - V_{tn}$ then pMos continue to V_{DD}

pMos discharge to $-V_{tp}$ then nMos discharge to 0

تعاون بنفس الوقت لتحقيق نتائج افضل.

both are well in → 0, → 1

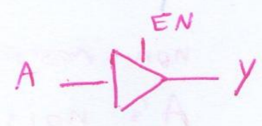


F = $S_1 \cdot A + S_2 \cdot B$

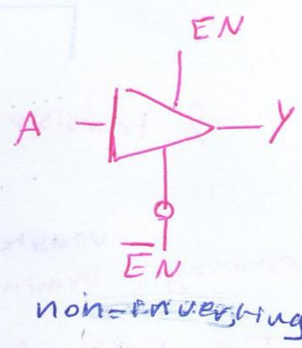
كل input له nMos / pMos بنفس الوقت

Tristates

produce Z when not enabled



≡



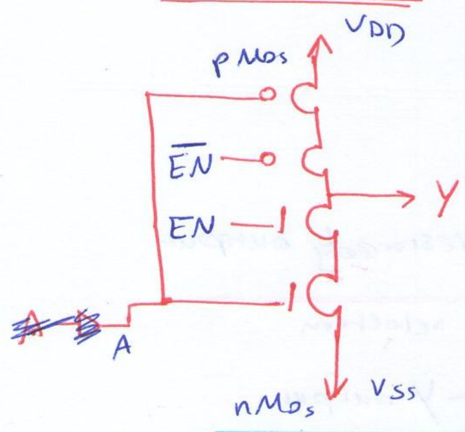
EN	A	y
0	0	Z
0	1	Z
1	0	0
1	1	1

not enabled

⊣ EN = $\overline{EN}$ ⊸

→ not connected to V_{DD} (pMos) or Vss (nMos)

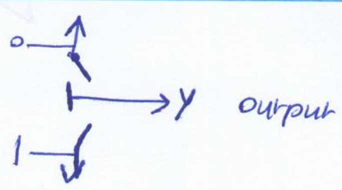
tristate inverter restoring



if EN = 0 ⇒ Y = Z

EN = 1 ⇒ inverter

Z-state like (floating)



Tristate
3 terminals
3 nods
~~3~~ 4 transistors

non-inverting

A	y
0	0
1	1

inverting

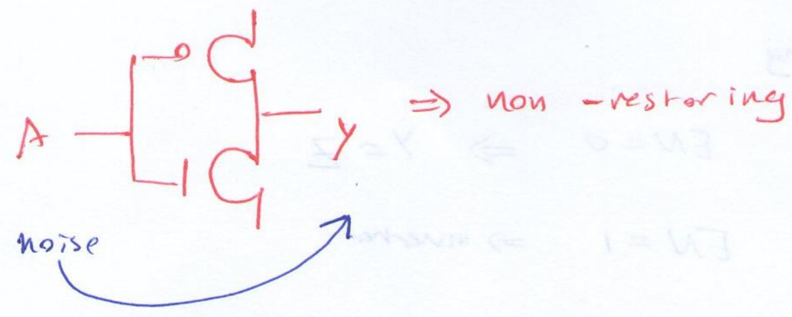
A	y
0	1
1	0

transmission Gates acts as tristate buffer

2 transistors

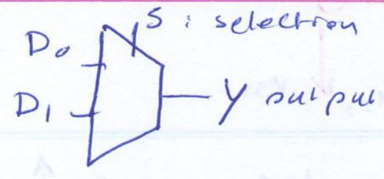
non-restoring
A's noise copied to Y

restoring : terminate noise of input in order not (violate) to pass / copy it to output



⟹ but tristate inverter is restored output

Multiplexers

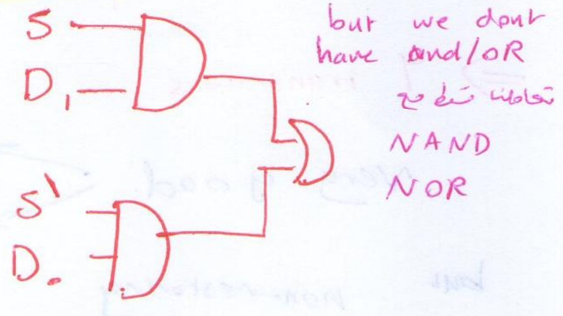


S	D0	D1	Y
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

Gate-level Mux Design

$Y = SD_1 + \bar{S} D_0$ How many transistors ??

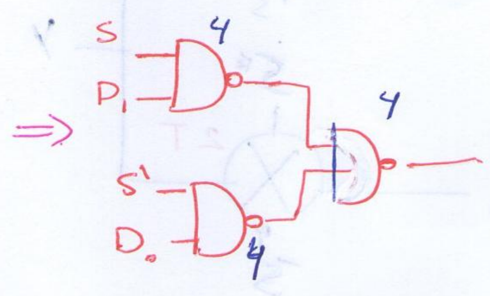
① using gates



but we dont have and/OR

NAND
NOR

⟹



$\overline{(SD_1 + \bar{S} D_0)} = \overline{SD_1} \bar{+} \overline{S' D_0}$

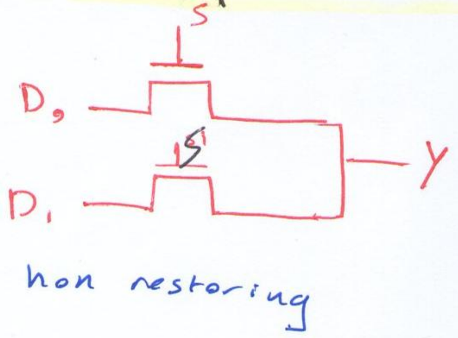
NAND → NOR, NAND

- restoring
⟹ 12 T
good but large number of transistors

draw mux using gate ——

using
1. gates
2. Transmission gates
3. pass gate
4. Tristate

② using pass transistor

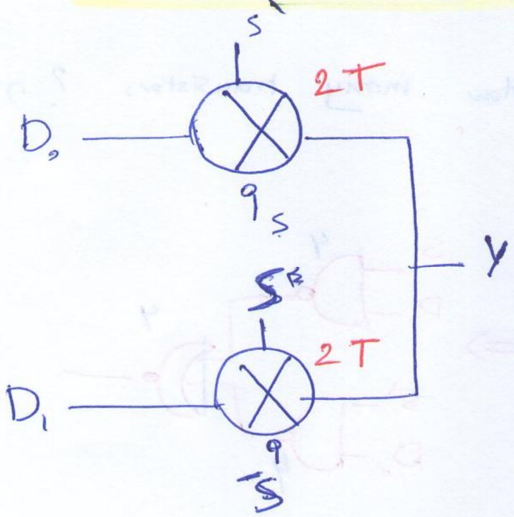


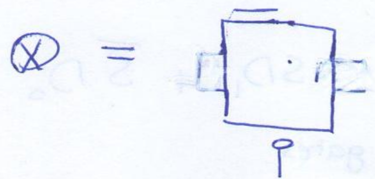
⟹ 2 Transistors

→ problem in VDD & Vss noise copied to Y

non restoring

3. Transmission Gates = pass + pMos X2 = 2+2 = 4



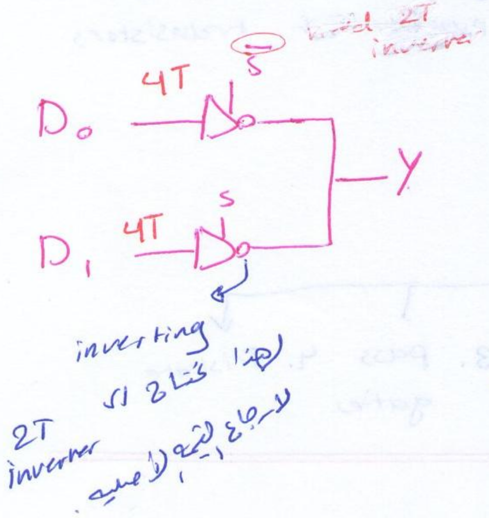


$\Rightarrow$ 4 transistors

Very good → VDD → 0

but non-restoring

4. using Tristate



= 4+4+2 = 8 T + 2 = 10 T

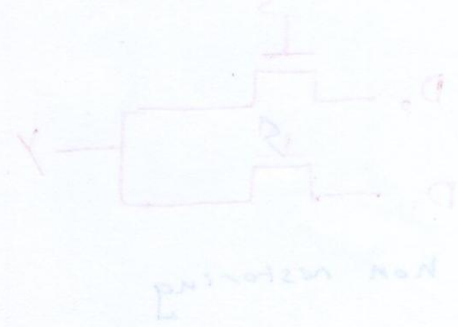
restoring

good Design

S = 1 S' = 0

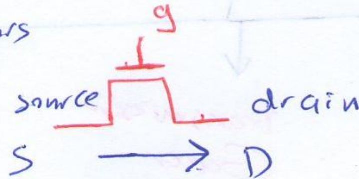
D_1 is connected

it give The value inverter



Transistors

① pass ~~gates~~ transistors



or

1 input

1 transistor

charge to $V_{DD} - V_t$

non-restoring

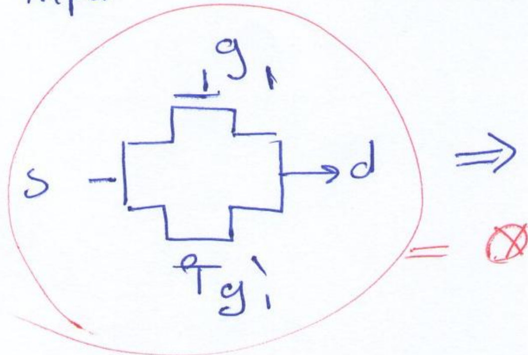
② Transmission Gates

2 transistors → n, → p

2 inputs

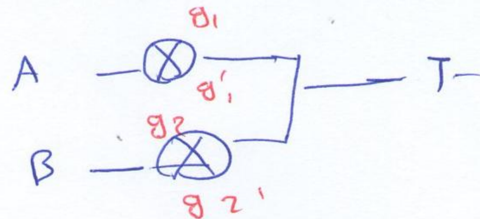
Charge to VDD

1 input → 2 transistor



⇒ = ⊗

for 2 inputs : 4 transistors



⇒ non restoring

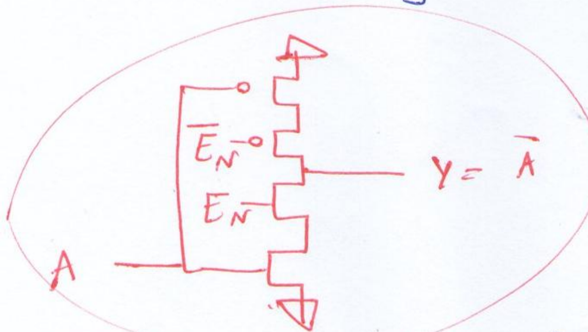
③ Tri state

restoring

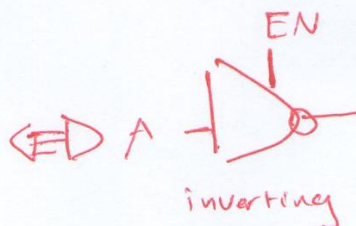
inverter restoring

EN = 0 $\bar{A}$ Y = Z-state

EN = ϕ $Y = \bar{A}$



⟺



④ ~~sim~~ basic gates

restory

inverter : 2

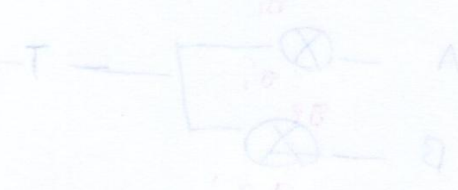
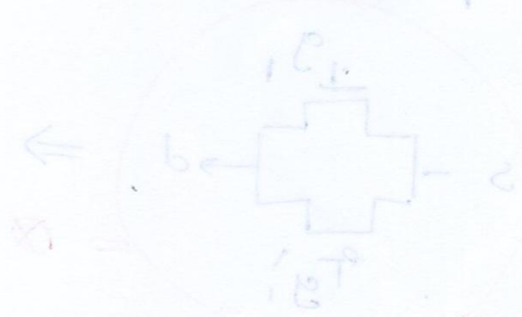
Nand : 4

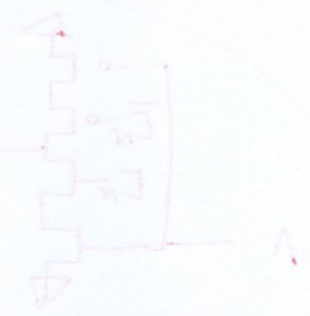
NOR : 4

E21

4 types

pass transistors	gates basic	Transmission Gates	Tristate
non	Res	non	Res
$V_{DD} - V_t$ V_t	many Transistors	better VDD 0	gives the value inverting so we need inverter

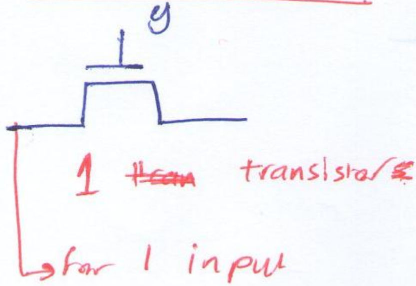





A1

85

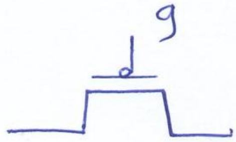
① Pass transistors



0 ⟶ 1 strong 0

1 ⟶ 1 degraded 1

- فقط نوع واحد مستخدم في التصميم



0 ⟶ 1 degraded 0

1 ⟶ 0 strong 1

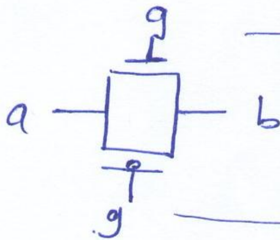
---

② Transmission Gates:

1- not produce any degraded value → acts as tristate buffer

2- any value is well strong

3- 2 transistors → n MOS, → p MOS → non restoring



→ 0,1 ⟶ 1,0 : strong 0

~~1 ⟶ 1 : strong 1~~

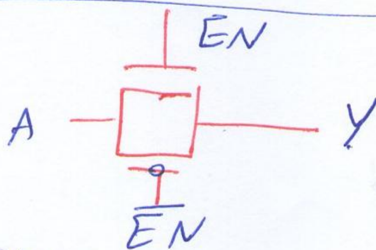
→ 1,0 ⟶ 0,0 : strong 1

~~0 ⟶ 0 strong 0~~

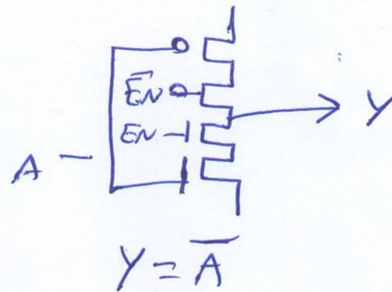
2 transistors per input

③ Tristate

- restoring



its as transmission Gates

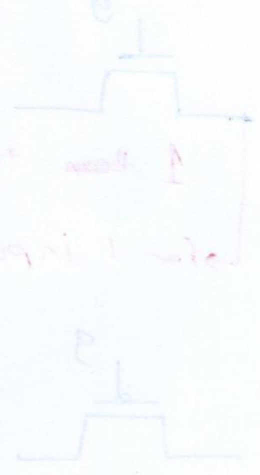


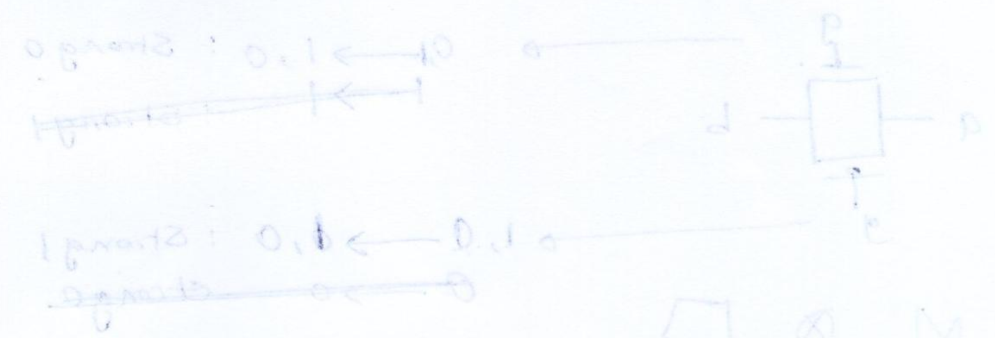
$Y = \overline{A}$

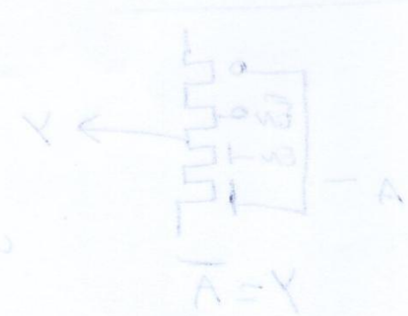
4 transistors

$Y = SD_1 + \bar{S}D_0$

using
1. ~~tea~~ CMOS transistors — static
2. pass transistors
3. logical Gate
4. tri state
5. transmission Gate

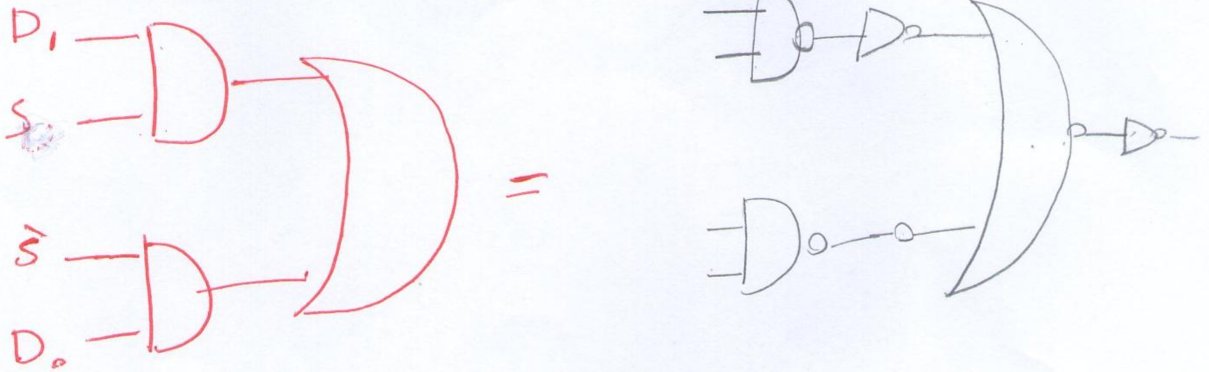


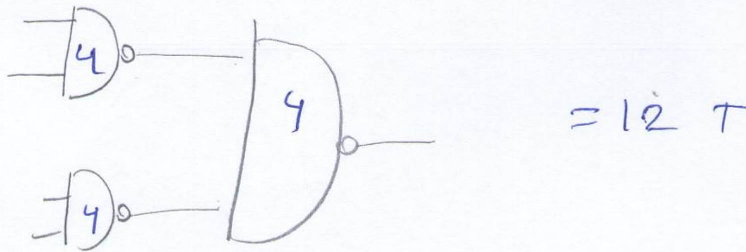




$Y = S D_1 + \bar{S} D_0$

How many gates → with simplification
→ without





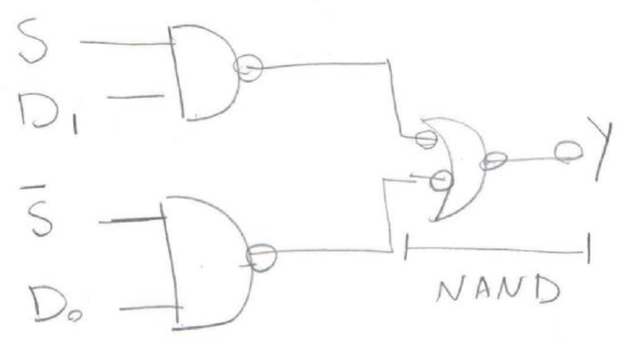
$\bar{A} + \bar{B} = \overline{A \cdot B}$

E3

85

$Y = SD_1 + \bar{S}D_0$

① using Gates



$SD_1 \Rightarrow$

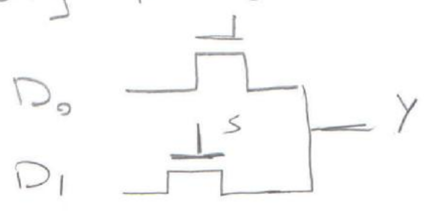
$\overline{\bar{A} + \bar{B}} = \overline{A \cdot B}$

→ restoring

but many transistors

$= \underline{12}$ transistor

② using pass - gates $\underline{2}$ transistors



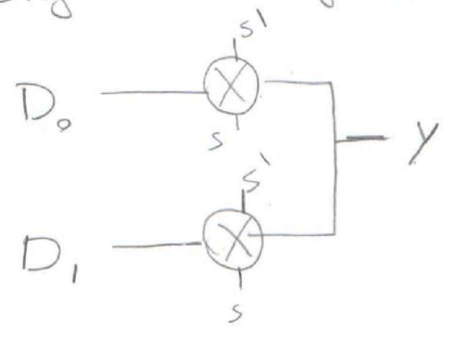
→ VDD - Vt ↑

→ Vt ↓

→ non restoring

→ only one type

③ using transmission gates



$\underline{4}$

VDD ↑

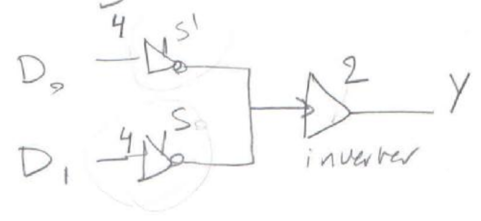
↓ Ø

vere good

2 types of tran

non R

④ using Tristate

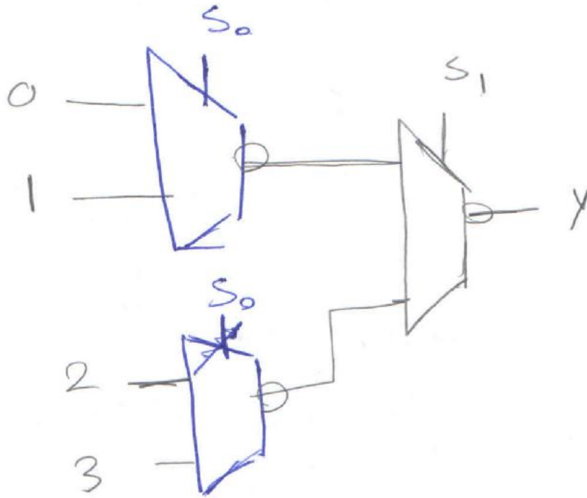


10 T - restoring

R -

E4

building 4:1 mux using 2:1 mux



S_1	S_0
0	0
0	1
1	0
1	1

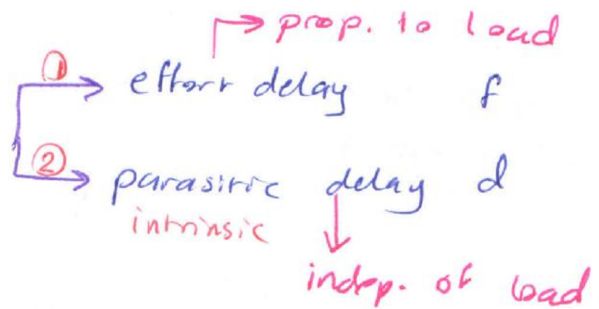
linear Delay model and Logical effort

linear Delay mo

logical effort method to make decisions
- delay
- calculations
- alternatives
- symmetries

Independent-Process : to have independent Design of technology

Delay has 2 Components



$\therefore d = f + p$

⇒ effort delay has 2 Components $f = g \cdot h$

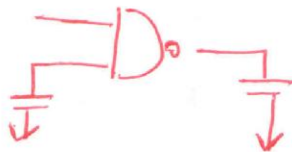
fanout ← h = electrical effort = $\frac{C_{out}}{C_{in}}$ ⇒ relative size of load

g = logical effort ⇒ depends on nature of gate logical effort

Effort delay : external load

intrinsic : delay of no load (unloaded body)
internal
DC level

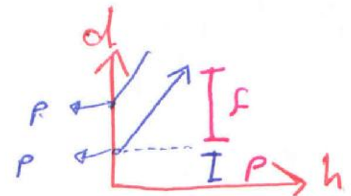
delay of gate when no load driven



$d = f + p$

$f = g \cdot h$

$h = \frac{C_{out}}{C_{in}}$



$d = p \big|_{h=0}$

P = intersection when $h = 0$

but nand $p = 2$

$g = \frac{4}{3}$

$d = (\frac{4}{3}) h + 2$

$\tau = 3RC$

for inverter

if $h = 1$

Then $d = 2$

$g = 1$

if $p = 1$

$h = 0$

$\therefore d = h + 1$

gate ability to deliver Current

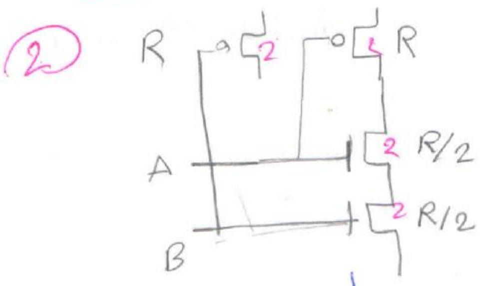
logical effort : ratio of input capacitance of gate to the input capacitance of unit inverter

unit inverter = nMOS size 1 & pMOS size 2

$\uparrow \frac{W}{L} \Rightarrow R \downarrow$

(2 inputs)
NAND

(2)



input = 4 capacitance per input

$A = 4 \quad C$

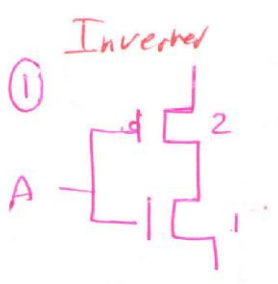
$g = \frac{4}{3}$

more gate to deliver same inverter work

مقلوب القيم

(3) NOR 2 inputs.

(1) Inverter

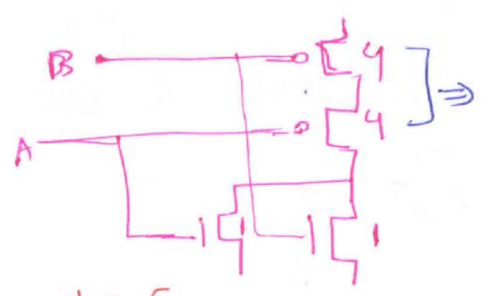


$C_{in} = 3$

$g = 1$ for inverter

~~Cout = 3~~

1 input



نزيد المساحة حتى تعمل نفس Work

لأنه R

1/2 تقل

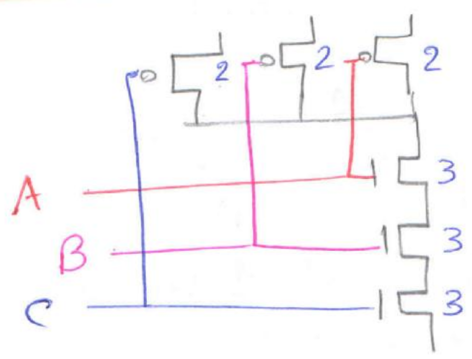
W نزيد

عشان R تقل وما تزيد

input = 5

$g = \frac{5}{3}$

Nand 3inputs



3 inputs

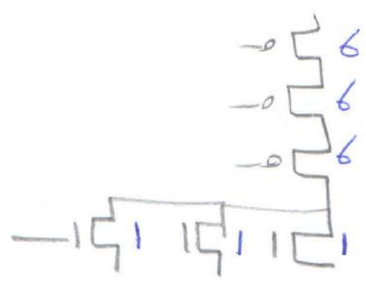
input = 5

$g = \frac{5}{3}$

$\left(\frac{n+2}{3}\right)$

اولاً نرسم ال Nand ثم ال NOR

NOR 3 inputs

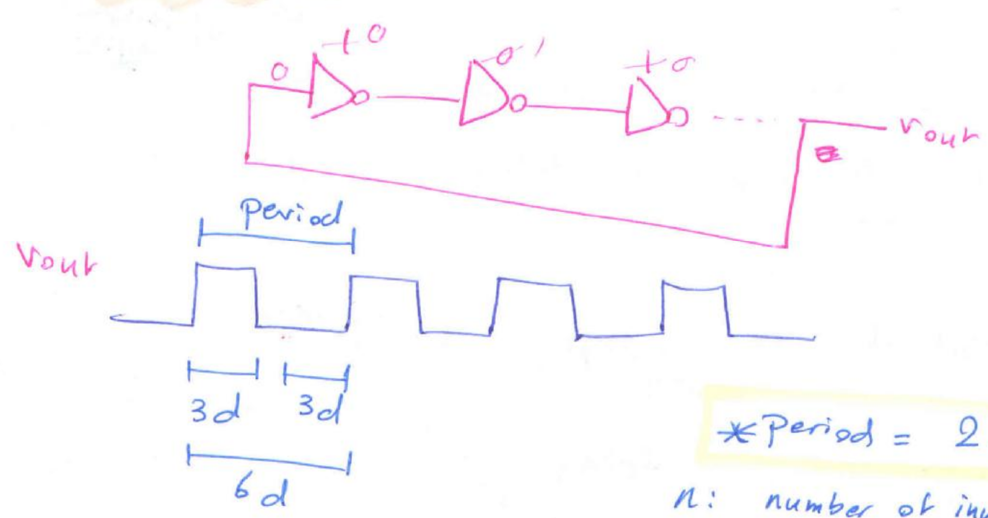


input = 7

$g = \frac{7}{3}$

$\left(\frac{2n+1}{3}\right)$

Ring Oscillator



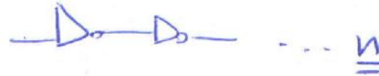
$*$Period = $2 \cdot n \cdot d$

n: number of inverters

d: delay of unit inverter

$f = \frac{1}{T}$ frequency $= \frac{1}{\text{period}} = \frac{1}{2 \cdot n \cdot d}$

Example 1:



$g = 1$
$h = 1$
$p = 1$
$d = 2$

assume $n = 31$

$\tau = 3ps$: delay of 1 inverter

$T =$ when $d = 2\tau = 4N\tau$

$\therefore f = \frac{1}{2 \cdot n \cdot d}$ but $f_{osc} = \frac{1}{T} = \frac{1}{4N\tau}$

$\therefore f_{osc} = \frac{1}{4 \times 31 \times 3 \times 10^{-12}} = 2.69$ GHZ

---

example 2

delay $= d * \tau$ (العدد ← d ; τ ↓ of 1 inverter)

(FO4 inverters) fount of 4 inverters

$g = 1$
$h = 4$
$p = 1$
$d = 5$ مش شرط معطاة

$d = g \cdot h + p = 1 \times 4 + 1$
$d = 5$ inverter units

① 65n Process $\tau = 3ps$ ⇒ delay = 15 ps

② 0.6 μm process $\tau = 60ps$ ⇒ delay = 300 ps

$\therefore$ Delay calculations indep of process

لنقدر نحسب ال delay بشكل مستقل عن نوع ال Process

if delay = 5 = 5 times delay of inverter

Logical Effort for multi-stage paths

h : electrical Effort = $\frac{C_{out}}{C_{in}}$ → $\frac{\text{آخر وحدة}}{\text{اول وحدة}}$

g : Logical effort = $\frac{C_{in} \text{ for 1 input}}{\text{Capacitance for inverter}}$

g for inverter = $\frac{3}{3} = 1$ always

t = delay of 1 inverter (unit is in time)

d = delay in inverter unit

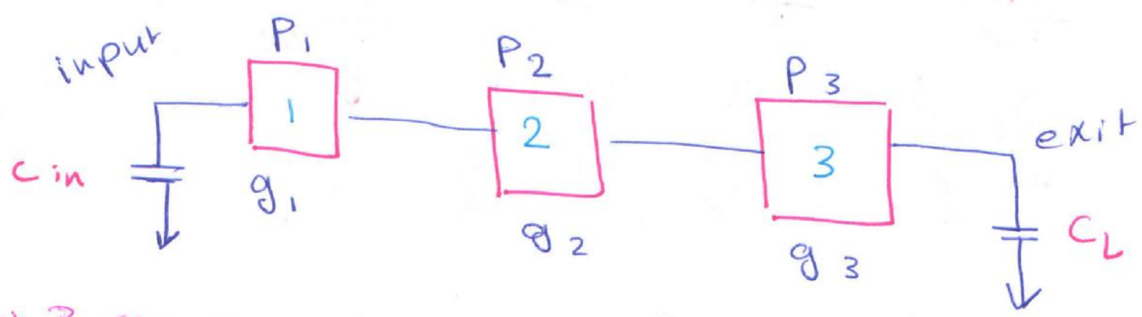
path :-

gate connected to another gate and so on...

more than 1 stage

more than one single gate

⟹ if we have multi stage path



3 stages

Total delay = $d_1 + d_2 + d_3$ entire D

G for whole path = $g_1 \cdot g_2 \cdot g_3 = \prod g_i$ G

H = $\frac{C_L}{C_{in}} = \frac{\text{exit Load}}{\text{Input load}}$ H

P = $P_1 + P_2 + P_3$ P

$D = F + P$

$F = H \cdot G \cdot B$

$F = (g_1 \cdot h_1)(g_2 h_2)(g_3 h_3)$ | $B = 1$

B : number of Branches for now assume $B = 1$

$\hat{f}$ = optimum stage effort

$\hat{f} = \sqrt[N]{(F)} = (F)^{\frac{1}{N}}$ ⇒ gates متساوية لكل ال

$F = H \cdot G \cdot B$

$H \to \frac{C_{out}}{C_{in}}$, $G \to \prod g_i$, $B \to 1$

$\hat{f} = g \cdot h$

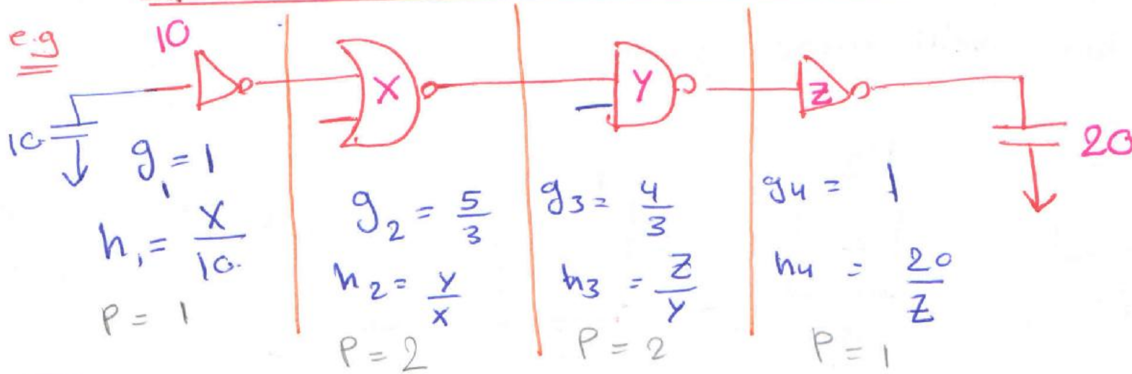
$F = \prod \hat{f}_i = \prod g_i h_i$

$F_{\text{for entire path}} = N\hat{f}$

$$D = NF^{\frac{1}{N}} + P = N\hat{f} + P$$

N : number of stages

e.g



$G = g_1 \cdot g_2 \cdot g_3 \cdot g_4 = 1 * \frac{5}{3} \times \frac{4}{3} \times 1 = \frac{20}{9}$

$H = \frac{C_{out}}{C_{in}} = \frac{20}{10} = 2$

B = 1 (given or no any Branches)

$F = G \cdot H \cdot B = \frac{20}{9} \times 2 \times 1 = \frac{40}{9}$

$\therefore \hat{f} = \sqrt[4]{\frac{40}{9}} = 1.45$, $P = P_1 + P_2 + P_3 + P_4 = 6$

$D = N\hat{f} + P = (4 \times 1.45) + 6 = 11.8$ inverter unit

① effort delay for each stage = $\hat{f}$

Total effort delay = $\sum \hat{f} = N\hat{f}$

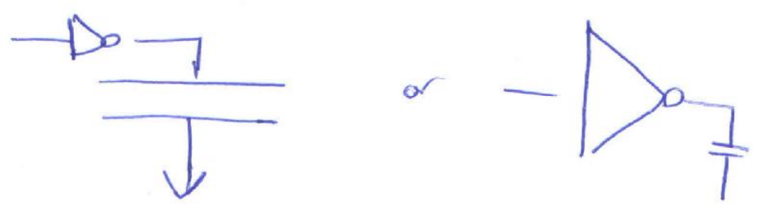
② intrinsic delay for each = P_i

Total = $\sum P_i = P$ (total intrinsic only)

③ Total Delay = Total effort + Total intrinsic = $n\hat{f}_i + P = D$

⇒ $\hat{f}$ same for each gate ⇒ Smallest delay

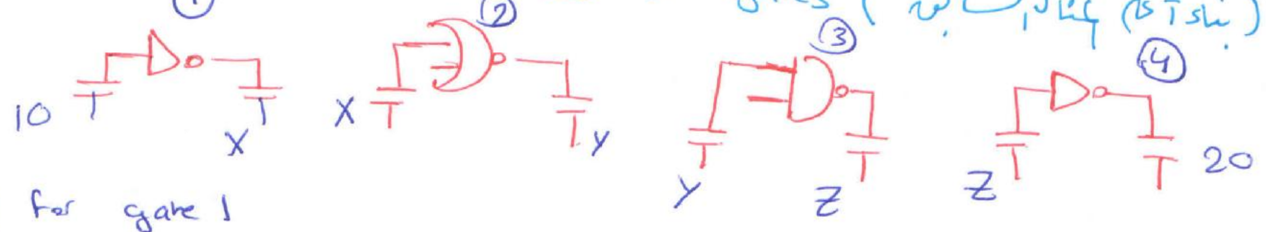
Gate Sizes



⇒ both are bad Designs

gates don't match each other

⇒ now how to find sizes of gates (بناءً على المثال السابق)



① for gate 1

$\hat{f} = 1.45$ (معطى أو يتم إيجاده سريعة)

$h = \frac{C_{out}}{C_{in}}$

$\hat{f} = h \cdot g \Rightarrow$

$h = \frac{\hat{f}}{g} \Rightarrow \frac{C_{out}}{C_{in}} = \frac{\hat{f}}{g}$

$g = 1$ (معروفة)

$C_{out} = \frac{C_{in}\hat{f}}{g} = \frac{10 \times 1.45}{1}$

$X = 14.52$

① مثلاً من اليسار

※ مهم : يجب تطبيق الإجابة في اكل من اليمين واليسار للتأكد ان القيم صحيحة حسب الوقت المعطى بالامتحان

For gate 2

$g = \frac{5}{3}$

$C_{out} = \frac{14.5 \times 14.5}{\frac{5}{3}}$

$Y = 12.64$

For gate 3

$C_{out} = \frac{12.64 \times 1.45}{\frac{4}{3}}$

$Z = 13.75$

For gate 4

$C_{out} = 20 \ ???$

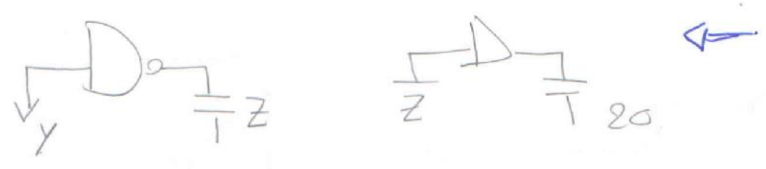
$= \frac{(13.7)(1.45)}{1}$

19.9 ≈ 20

g, h, p, $\hat{f}$ — لكل gate نحتاج

حتى نبدأ الحل

(من اليمين) يتم الحل بالاتجاه العكسي ⇐



$g = \frac{4}{3}$

$\frac{C_{out}}{C_{in}} = \frac{\hat{f}}{g}$

$C_{in} = \frac{C_{out} \cdot g}{\hat{f}}$

① inverter

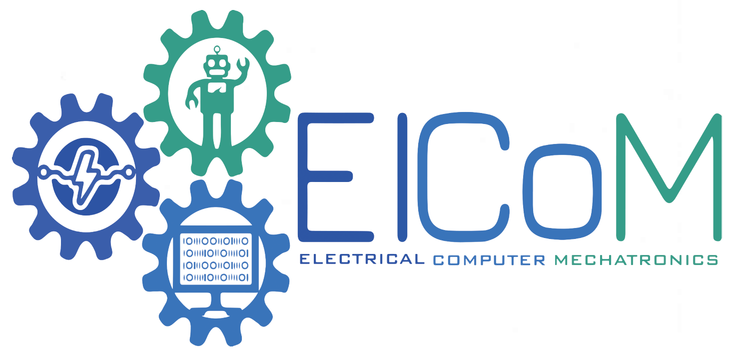
$Z = \frac{(20)(1)}{1.45}$

$Z = 13.77$ ✓

② Nand

$Y = \frac{(13.77)(\frac{4}{3})}{1.45}$

$Y = 12.6$ ✓



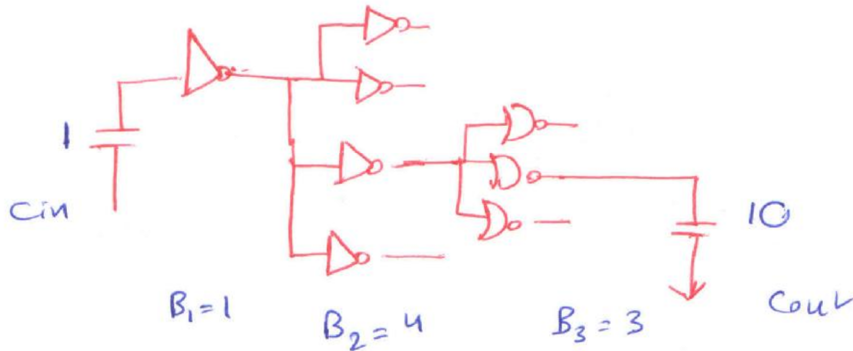
Branching Effort

$B = \prod b_i$ $\qquad b = \frac{C_{on} + C_{off}}{C_{on}}$

$F = G\,BH$

$BH = \prod h_i$

e.g

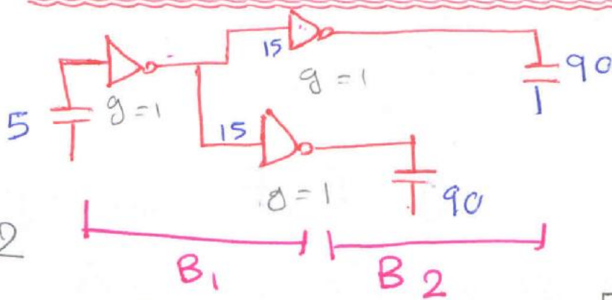


3 stages

$B = B_1 * B_2 * B_3 = \underline{12}$

$*$ gates $= \sum B_i = 1 + 4 + 3 = 8$

e.g



Find effort delay

$B = 2$ $\qquad B_1 \quad B_2$

$F = H \cdot B G$

$H = \frac{90}{5} = \underline{18}$

$G = 1$

$F = \underline{36}$

$F = \prod h g = H \cdot B \cdot G$

$HB = \pi h_i$

Branch 1

$h_1 = \frac{(15 + 15)}{5} = 6$

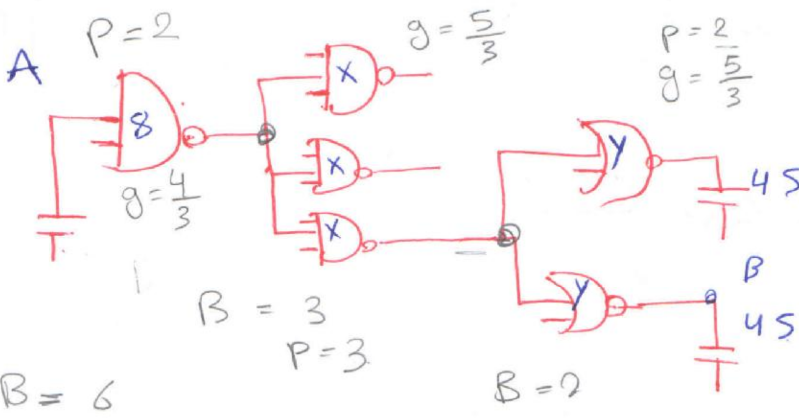
$h_2 = \frac{90}{15} = 6$

$\therefore F = G(HB)$ $\quad HB = \prod B_i$
$= \prod g_i h_i$

$F = (6 \times 1)(6 \times 1) = 36$

$F = GHB = (1)(36)$
GH

FO4



مهم P تغير
حسب عدد ال
inputs

$N = 3$ $N = 3$ stages

$$F = GHB = (6)\left(\frac{45}{8}\right)\left(\frac{100}{27}\right)$$

$$= 125$$

$$P = 2 + 3 + 2 = 7$$

$$\hat{f} = \sqrt[3]{125} = 5$$

$$\hat{f} = g \cdot h$$

$$5 = \frac{4}{3} \frac{C_{out}}{C_{in}}$$

$$\frac{15}{4} \times C_{in} = 3X$$

$$30 = 3X$$

$$X = 10$$

$$\Rightarrow$$

$$5 = \frac{5}{3} \frac{2y}{10}$$

$$y = 15$$

$$D = N\hat{f} + P$$

$$= 3 \times 5 + 7 = 15 + 7 = 22$$

\# stages ≠ gates

مهم: بال g, $\hat{f}$, P
حسب ال stage وليس لكل gate
فقط بال $\frac{C_{out}}{C_{in}}$ ننظر الى عدد ال gates
بالنسبة لل Branches

gate = stages

② حالة واحدة فقط
اذا كان
Path = 1 Branch

من اليمين

① $5 = \frac{5}{3} \frac{45}{y}$

② $5 = \frac{5}{3} \frac{2y}{X}$

③ $5 = \frac{4}{3} \frac{3X}{8}$

Sizing

حفظ ومعرف

Cin = 8

size = 8

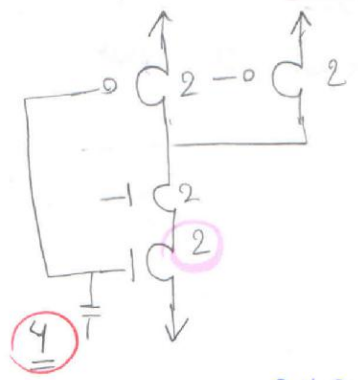
if inverter

$-\circ C\ 2 = 2R$

$-| C\ 1 = R \Rightarrow$

1 : 2

n : p

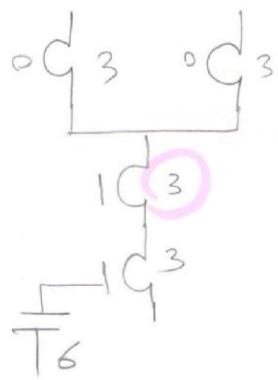


pMos ⇒ parallel $\frac{2 \times 2}{2+2} = 1$

nMos شرط تتعامل بالاتساع

على ال pMos عكس كل ذلك

OR



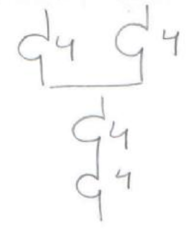
$2 * f = 3$

$2 * 1.5 = 3$

$\therefore 4 \times 1.5 = 6$

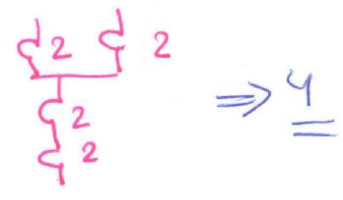
$4 \Rightarrow 6$

$2 \Rightarrow 3$



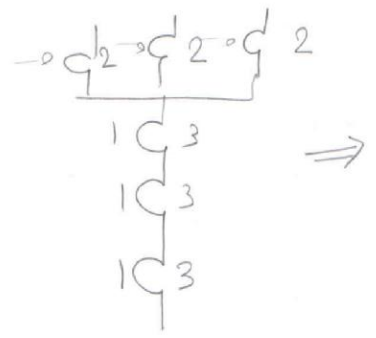
size = 8

2 input nand gate =

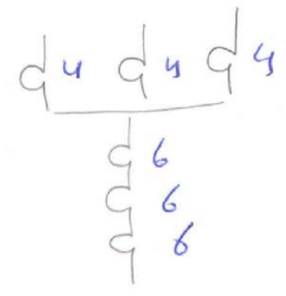


$\Rightarrow 4$

if 3 input Nand gate



$\Rightarrow$



input = 5

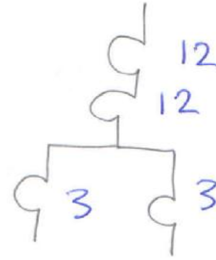
but x (size) = 10

multiply 2

NOR

عم المتوازي بنضاعف القيمة

basic 2 input



5 but y = 15 (multiply 3)

⇒ Relationship between size is same

Best number of stages

number of stages that path should use to be fastest and mini delay

n is unknown

$\hat{f} = \sqrt[N]{F}$ $F = GBH$ $D = N\hat{f} + P$

$\hat{f}$, F is known

$H = \frac{64}{1} = 64$

$B = 1$

$g = 1$

$\hat{f} = \sqrt[N]{64}$

(1) if

$\Rightarrow \hat{f} = \sqrt[1]{64} = 64$

$D = N\hat{f} + P$

$P = 1$ for inverter $\therefore D = 65$

First we must know F to know N & $\hat{f}$

Solve it using Try & error

$N = 3$

$\hat{f} = 4$

(2) Try if $N = 2$

$N = 2$
$P = P_1 + P_2$

$\hat{f} = \sqrt[2]{64} = 8$

$D = 2 \times 8 + 1 \times 2 = 18$

\## اساس العملية اي، اول رقم وهو عندنا $N = 1$ عندنا $F = HBG$

(3) $N = 3$

$\hat{f} = \sqrt[3]{64} = 4$

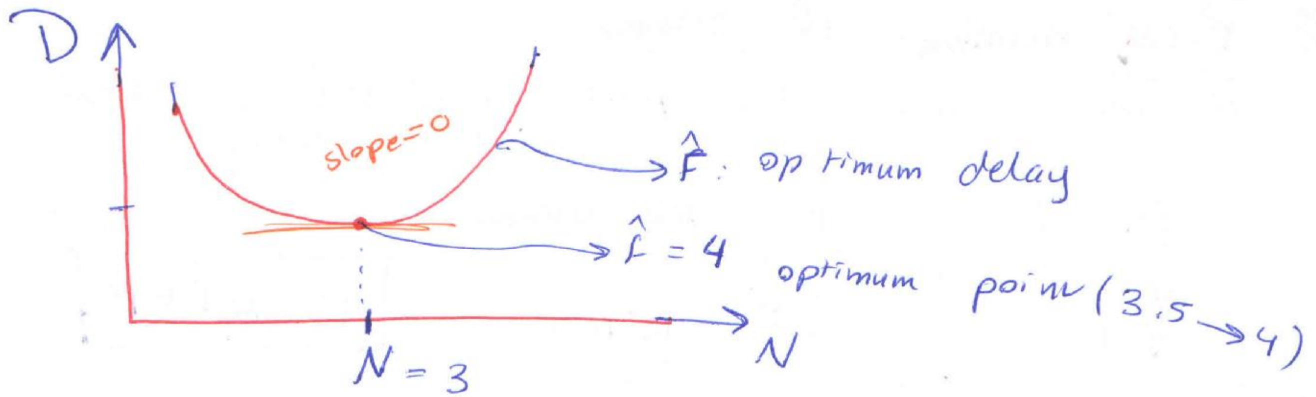
$D = 3 \times 4 + 3 = 15$

\## عند كل رقم لل $\hat{f}$ وال N نقوم بحساب ال D لمقارنتها مع الباقي

(4) $N = 4$

$\hat{f} = \sqrt[4]{64} = 2.83$

$D = 15.3$



∴ best number for $N = 3$

in exam best values for $\hat{f} = \{3, 4, 5\}$

or start with ← ... 3 ← (4) → 5 ... →

اول بداية

$\hat{f}$ is around 4

الانتباه لنوع gates
اذا كانت Not , Nand , Nor
يختلف ال H , P , G

$\log \hat{f} = \frac{\log F}{N}$

مهم جداً : التمييز بين N و $\hat{f}$

اذا $\hat{f}$ كانت معروفة

نستطيع ايجاد ال N عن طريق log

① اول خطوة بالامتحان نفرض ان $\hat{f} = 4$

$\hat{f} = 3$

$\hat{f} = 5$

2 Methods

جدول 53
مهم بالامتحان

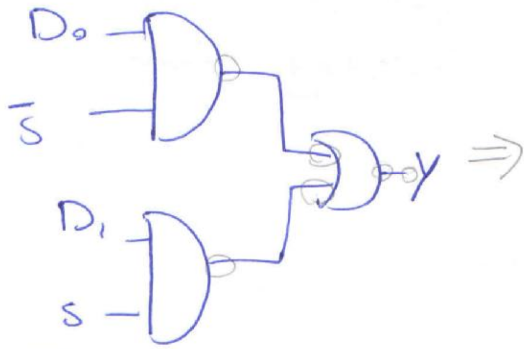
② Try & error

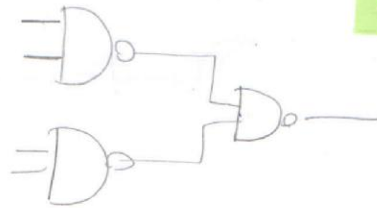
Lecture 6 : chapter 9

Combinational ccr Design

Combinational ccr

Design using NAND, NOR, Not

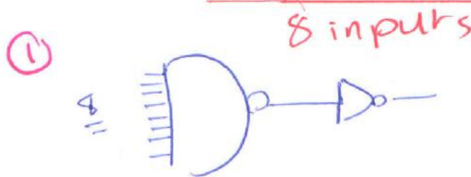




$\overline{\overline{\bar{A} + \bar{B}}} = \overline{A \cdot B}$ Nand

$= \overline{A+B}$

① 8 inputs



$N = 2$ stages

$G = \frac{n+2}{3} = \frac{10}{3}$

$B = 1$

$H = 64$

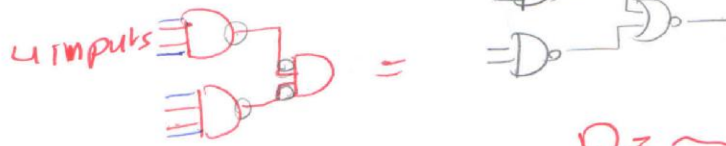
$F = \frac{646}{3}$

$\hat{f} = \sqrt[2]{\frac{646}{3}}$

$D = 2 \times \sqrt[2]{\ } + 8 + 1$

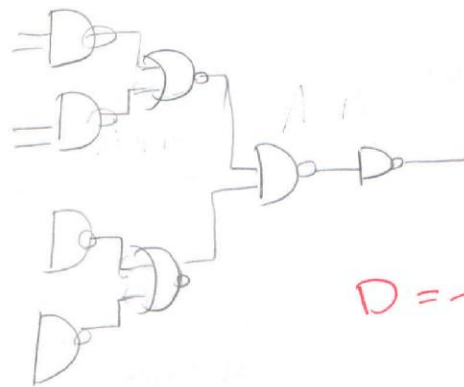
$= \bigcirc$

② Design following using 2, 4 stages



in 2 stages $D = \sim$

2 inputs



$D = \sim$

مع كل عدد input بتختلف معها

$\hat{f}, F, N, G, g, B^{-1}$

وبالتالي بنختار أقل D

minmum D

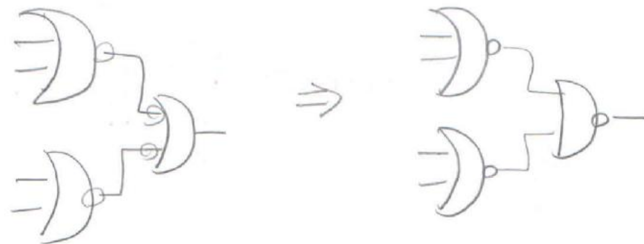
عكس الشكل وتغيير مكان ال Bubble

because we only ~~Dot~~ Deal with inverting Gates

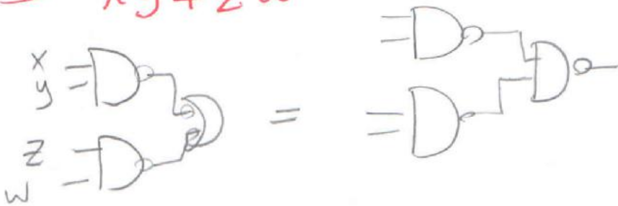
①

②

or



③ $xy + zw$

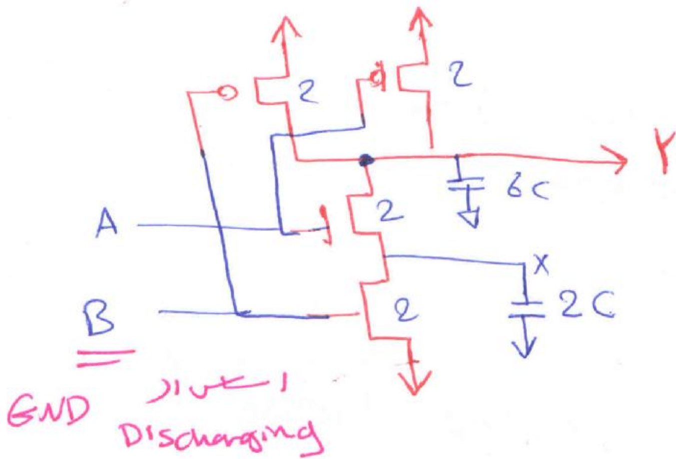


4 inputs ① either 4 input

or ② → 2, → 2

مش داخل
25 → 27

Input Order



Suttlepoint : نقطة مهمة

1 ※ faster to discharge output if

A : early

B : earled

discharge if A B بنفس

2 # if B is late

worst Case

because when A is early and B is late 6C & 2C cannot be discharged without B because its The path for ground so A (6C) is waiting for B Then 2C & 6C will be discharged as B is There (ON)

A need to wait B

6C is discharged to unknown value

3 ※ if B is very early

The 2C will be discharged and 6C is waiting for late A to be discharged

⇒ when A comes after B whole output will be discharged

↳ better case Than 2 because 6C is discharged

6C & 2C are discharged indep.

B not need to wait A

make Top latest

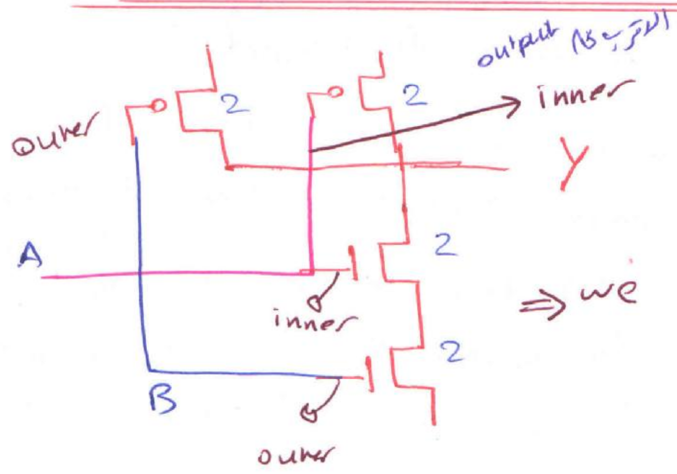
Diff. capac من شطلع من ①

make lower (bottom) earlier

not worst case'

each lower will eliminate diffusion Then latest one will discharge output Then its discharged

∴ Input order: make The top latest and lower earlier

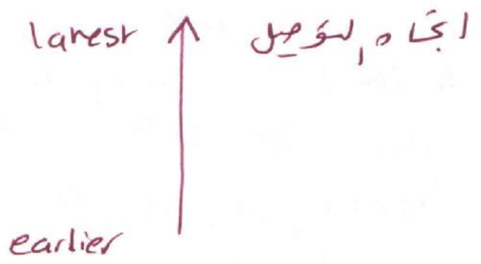


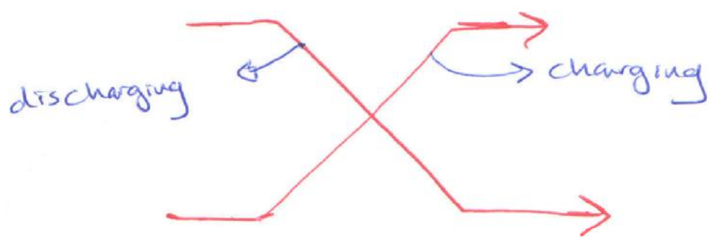
make inner latest

inner input to → A

outer input to → B

⇒ we Connect inner to latest

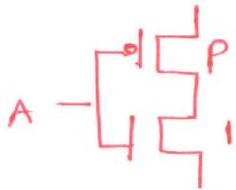




inner : Top

output الاقرب لل

Best P/N Ratio



previously we dealt with 2 : 1 Ratio
p : n

but now we need to choose ratio for This inverter to get
least average delay

$$\text{delay}_{avg} = \frac{\text{fall} + \text{raise}}{2}$$

$$\mu = \frac{\mu_p}{\mu_n} = 2$$

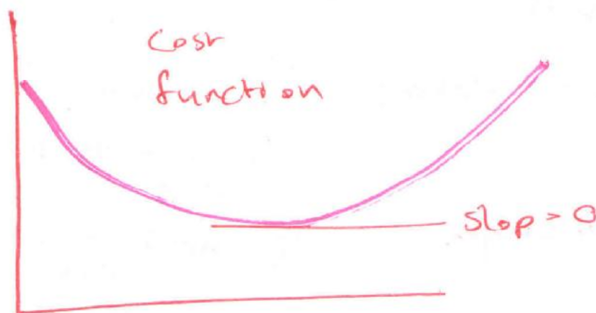
fall : $t_{pdf} = p + 1$

raise : $t_{pdr} = \frac{(p+1)\mu}{p}$

$$\text{delay} = \frac{(p+1) + \frac{(p+1)}{p}\mu}{2} \Rightarrow$$

* $p = \sqrt{\mu} = \sqrt{2} = 1.41$

$$p = \sqrt{\frac{\mu_p}{\mu_n}}$$



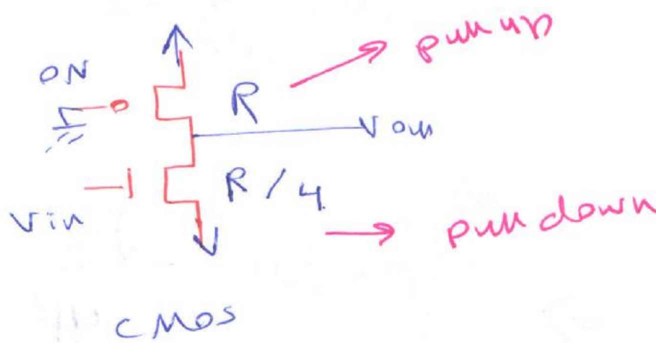
$$\frac{\mu_p}{\mu_n} = \frac{P}{N} = 2$$

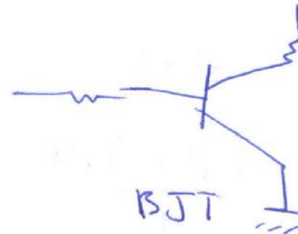
CCT Families

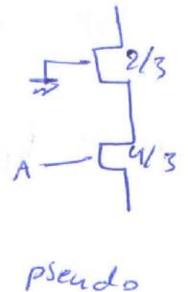
- * - Pseudo - nMos logic
- * - Dynamic
- * - pass Transistor Logic

pseudo - nMos logic :- Ratioed

something like but not exact







nMos stronger Than PMos 4 times

we need to make pMos stronger but not than nMos ⇒ to reduce delay

$PMos = \frac{1}{4}$ pull down Strength

problems :

1. wasting power it short ccl
2. need correct Ratio
3. consuming high energy

Ratioed Logic : psudo : if The sizes not Correct : it wont work "There is Condition"

normal CMOS : work at any size (non- Ratioed)
↳ better

static power When $Y = 0$

$p = V_{DD} I_{DD}$

Ratio example

ROM = 32 word x 48 bit

$I_{on\text{-}p} = 36\ \mu A$ $V_{DD} = 1\ V$

$P_{pull\text{-}up} = V_{DD} \cdot I_p = 36\ \mu W$

$P_{static} = (P_{pull})(31 + 24) = 2mW$

24 bit = high (48-24)

1 word = high (32-31)

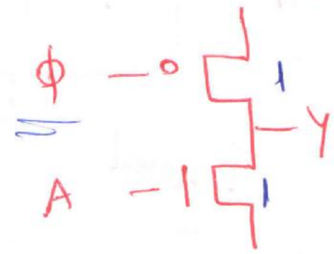
$P_{static} = V_{DD} \cdot I_{pullup}$

psuedo : static

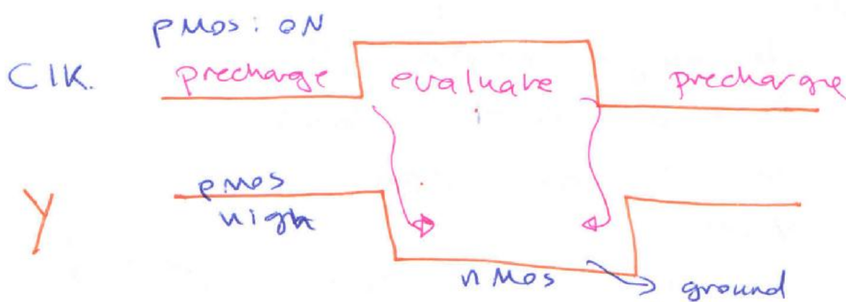
Dynamic Logic

Gates uses clocked pMos pull up

2 Modes → evaluate / → precharge



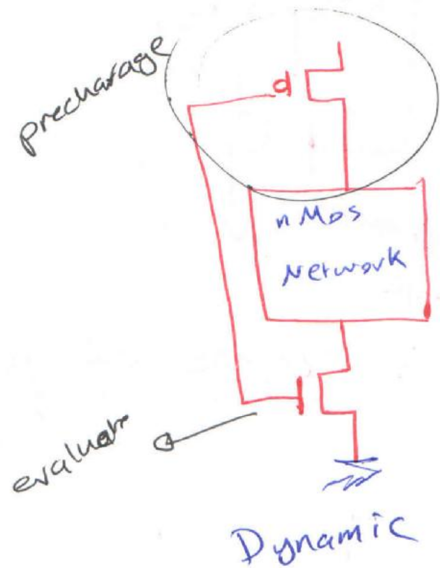
- Dynamic cct : has 2 Transistors



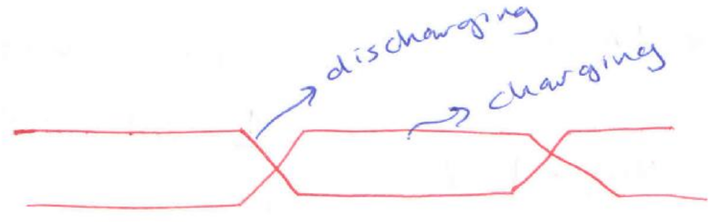
precharge: Clk = 0 pMos ON VDD

evaluate: clk ON → Connected to GND

⇒ when clk = 0 off
precharge and output is high



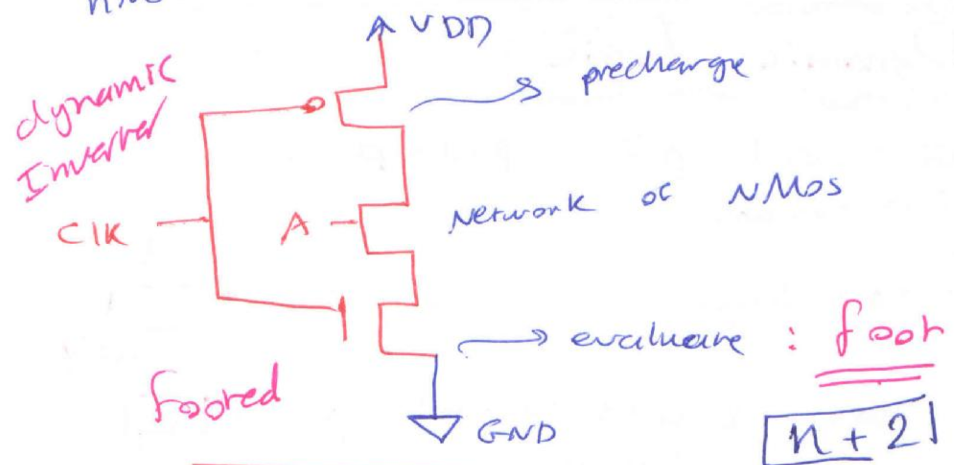
Make sure we only evaluate the value of output only when clk is On high

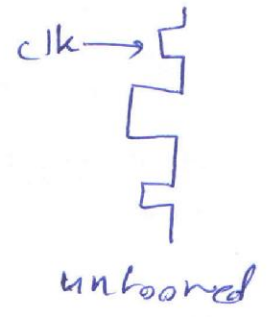


when clk is OFF

pMos: ON → connected to vdd and disconnected from Ground

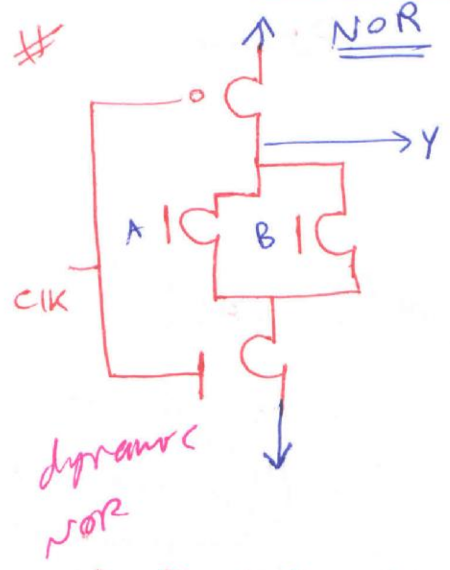
nMos: OFF





n: input

NOR Gate



discharge output if

A = 1 or B = 1 or both

Then evaluate output

Y = 0

n + 2 gate → 1 for precharge, 1 for evaluate

instead of 2n transistors

2n

Dynamic Cct: Synchronized with clk Signal

if clk = 1 evaluate function

footed ال شغلة

* during precharge when $Clk = 0$

Y is connected to V_{DD}

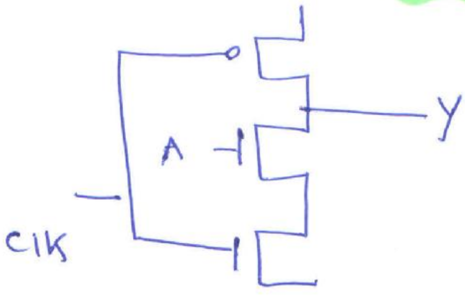
footed will cut path to ground to make sure that Y is high during $clk = 0$

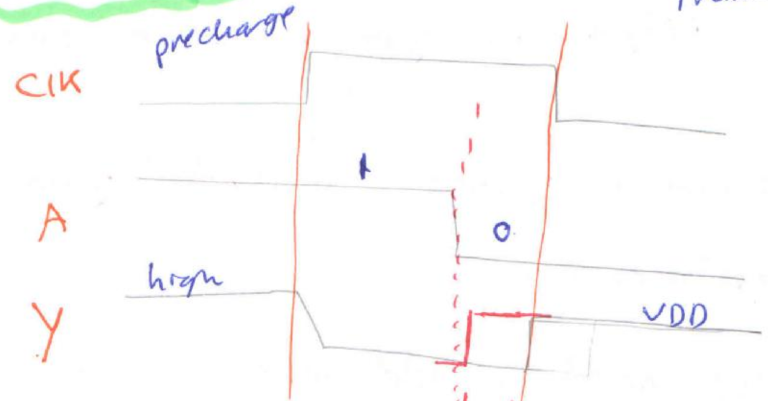
because we don't need electrons to escape to ground

if $A = 0$ & $B = 0$ we don't need

Dynamic inverter

n + 2 Transistors





⟹ if $clk = 0$ The A = don't care

$Y = 1$

⟹ $Clk = 1$

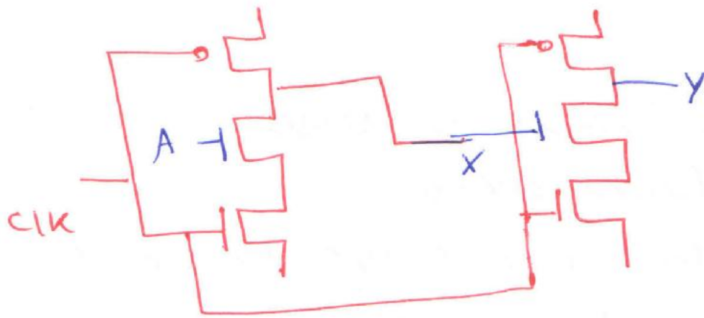
if $A = 1$ ⟹ $Y = 0$ (connected to ground

$A = 0$ ⟹ $Y = 1$

⟹ illegal: to change A value from 1 to 0 during evaluate $clk = 1$

because output will discharge to undetermined value

How to solve The illegal problem



output is connected to another gate

if A = 1
X ↓ ⟶ Y goes 0

\# output of first inverter 1 ⟶ 0
its illegal for X

Monotonicity solves

\# illegal for gate to drive another

Nand + inverter = and gate

\# Problems :

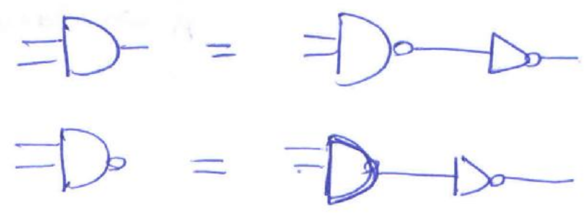
① need to add more transistors (price)
② And, OR not universal Gates

most problems are when $clk = 1$

Dual-Rail Domino

→ how to Design non-inverting gates and, OR : ⇒ only And, OR

→ Dual-Rail is The solution for This by producing complementary output



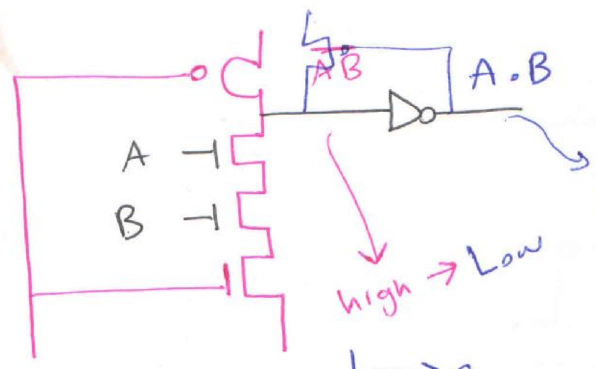
Function & it Complementary

inverter: to prevent illegal transition

---

1 2 inputs A, B

and



series : Nand

inver لازم بعدها
A·B عشان تطلع

high → Low

1 → 0

disch

low → high

0 → 1

inverter Transfer illegal Transition to legal one because maybe it will be input of another gate

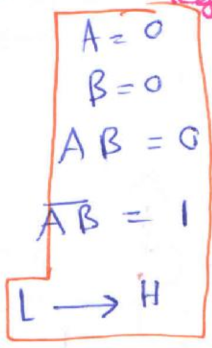
$A = 1$ $\bar{A} = 0$

$B = 1$ $\bar{B} = 0$

$AB = 1$

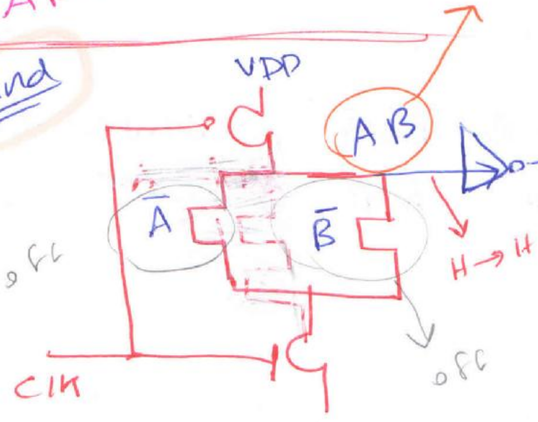
$\overline{AB} = 0$

output = high



output of dynamic cct

Nand



$\overline{AB} = \bar{A} + \bar{B}$

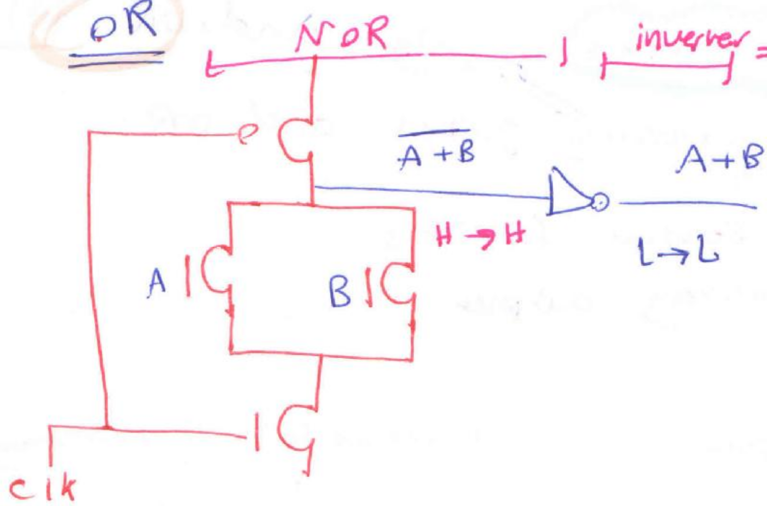
L → L

H → H

$\bar{A}, \bar{B}$ always off : no charge

off = Cannot discharge

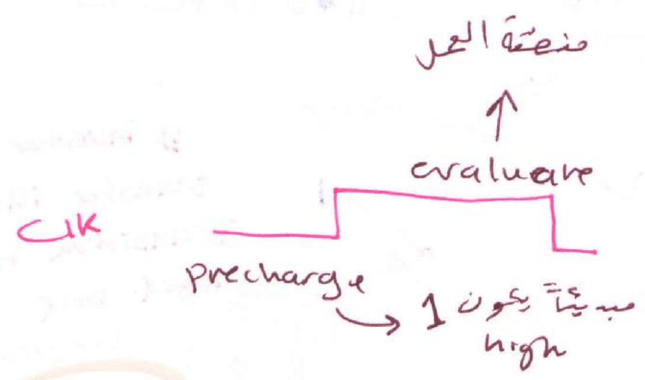
متوك
04
دقيقه 30

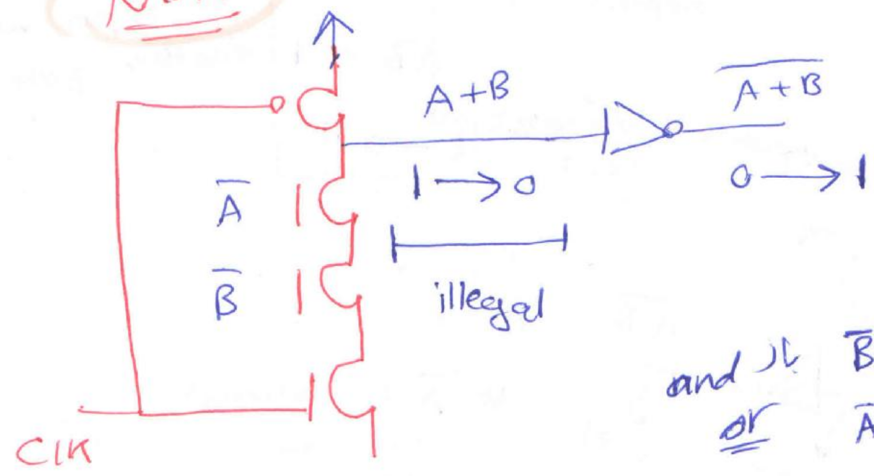


1 → 0 : disch
0 → 1 : charging

مهم : اذا موصولات توازي فتيمهم 0
$A \Rightarrow$ or
$\bar{A} \Rightarrow$ Nand

if $A=0$ $\bar{A}=1$
$B=0$ $\bar{B}=1$

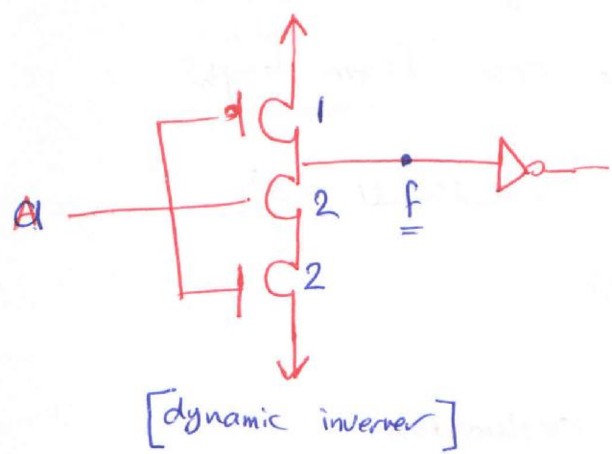


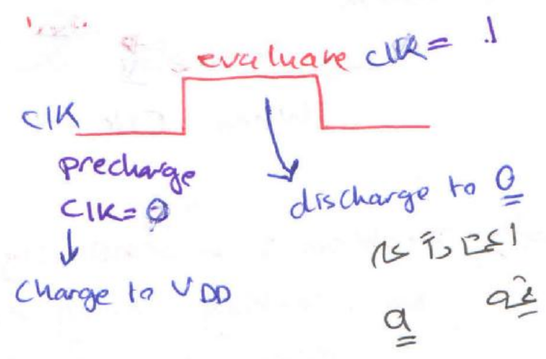


مهم: موصولات التوازي $\bar{B}$, $\bar{A}$ بال and
ع ع التوالي $\bar{A}$, $\bar{B}$ or

$A=0$ $\bar{A}=1$
$B=0$ $\bar{B}=1$

Leakage





Compact & faster
⇒ because n+2 instead of 2n

make sure that clk: not logical operand
Function لا يجوز ادخالها بال Function

≠ 0

Function above = $\overline{a}$ inverter

الاسرع : الأقل C , R

* Less load = less RC = less C ⇒ faster

---

* problem here is = Sensitivity

التغير على ال clk

during evaluation: Supply of charges is PMOS
evaluate based on value of a (input)
Suppose a = 0 (∴ Output still = VDD)
but clk slow

⇒ Supply of charges: PMOS but if clk = 1 PMOS OFF
So it won't stay at VDD ⇒ it will start leaking through nMOS.

but as leaking from nMOS ⇒ also leaking via pMOS
⇒ electrons faster than holes

during evaluation $Clk = 1$

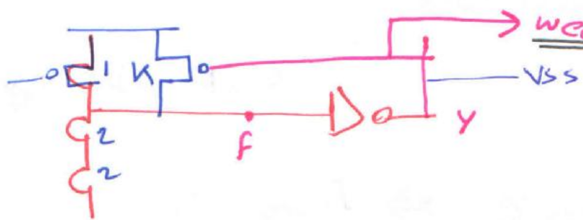
Charges will escaped and VDD get lower & lower until The inverter is flipped Then CCt float high

Problem

→ Sensitivity & leakage   = إذن المشكلة
when $Clk = 1$ & $a = 0$

⇒ Problem :- sensitivity in The evaluation
leaking during evaluation causes electrons to escaped and VDD gets lower & lower

Solution For problem!



→ weak keeper :- to compensate any loss of electrons escaped by leaking via nMos

∴ $I_{OFF} \neq 0$

why weak not strong: because not to fight evaluation

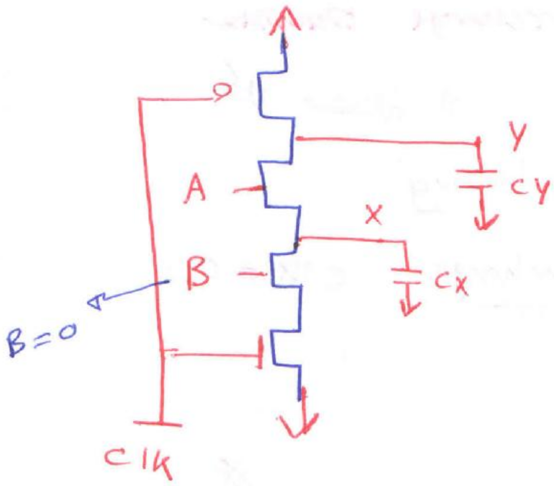
good but still have problem :- fighting evaluation it needs To be weak

$I = \frac{W}{L}$ to make it weakest L not mini

∴ $I = \frac{W}{2L_{mini}}$ weaker (2L)

اذن يجب ان يحقق الـ keeper الخاصية ←

1. Compensate leakage Through nMos
2. not fighting evaluation



$Y = \overline{A \cdot B}$

in precharge $Y = V_{DD}$

but X not precharged when $clk = 0$

اذن ال initial فقط من جهة ال Y

$\therefore Q_{X_{initial}} = 0$ nMos : OFF

$Q_{initial} = C_y V_{DD}$

⟹ Charge Sharing:

$Q = C.V$ الشحنة

but initial = final الشحنة بعد = قبل

$\therefore Q_{final} = (C_x + C_y) V_{final}$ ⟹ مجهول عادي.

$C_y V_{DD} = (C_x + C_y) V_{final}$

$V_x = V_y$

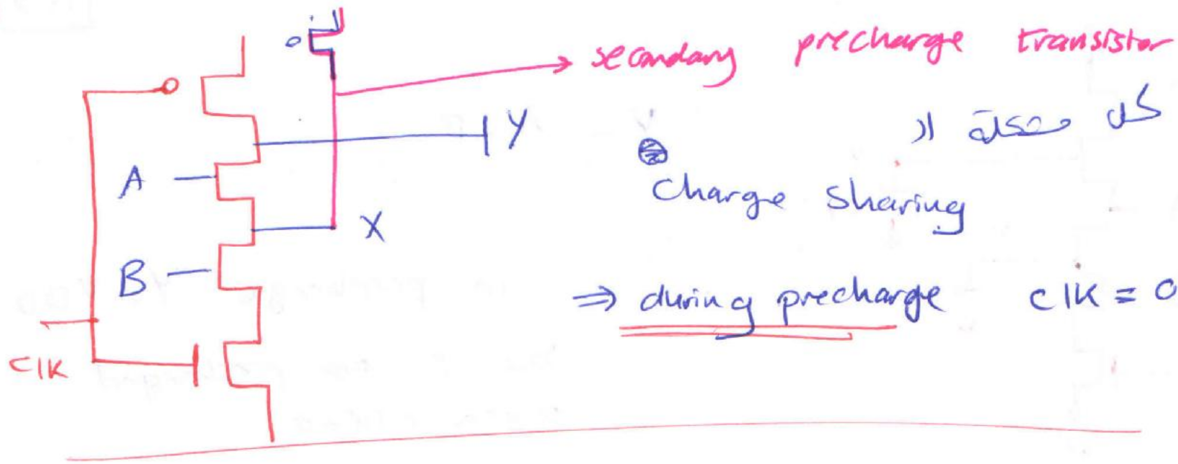
B=0 not discharged to Gound (discharged to V_{final})

$$\therefore V_{final} = \frac{C_y V_{DD}}{C_x + C_y} = V_x = V_y$$

if $C_x = C_y \Rightarrow V_{final} = \frac{V_{DD}}{2}$ its bad

So we have a problem in Charge Sharing: having $\frac{V_{DD}}{2}$

Solution: adding secondary precharg



number of transistors ≠ n + 2

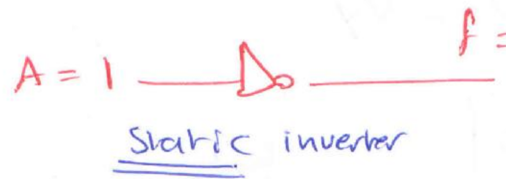
1- increasing number of transistors for leakage
2- 〃 〃 〃 〃 precharge

noise sources

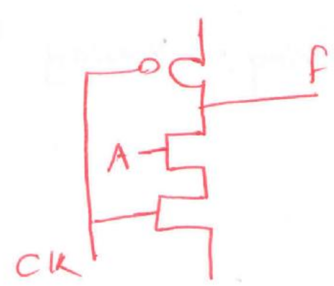
1- Capacitive Crosstalk
2- Charge sharing
3- power supply noise
4- Feed Through noise

another problem : power hungry

up & down of nodes makes power hungry



⇒ if A doesn't change : output doesn't change



dynamic

Charge f when clk = 0
The activity of dynamic is high
if A doesn't charge output charges depending on clk

⇒ wasting power

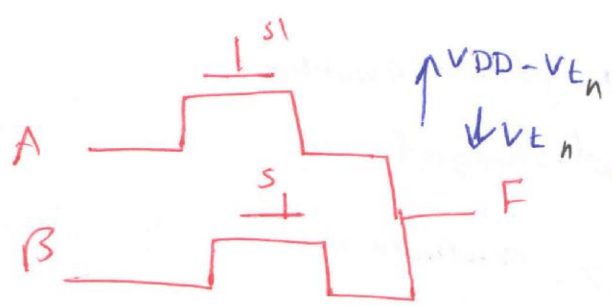
Leap cct

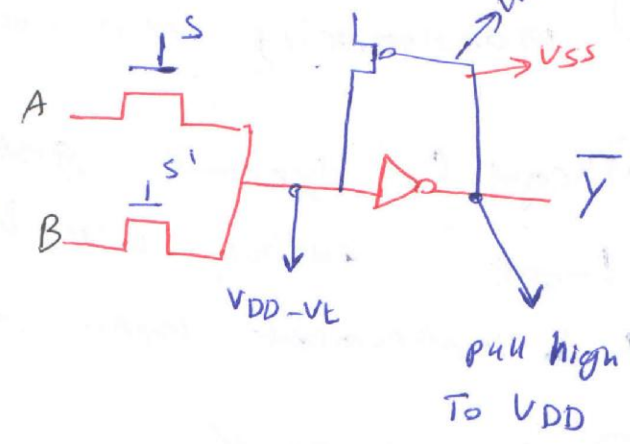
- lean integration with pass transistor
- pMos weak feedback to pull high
- Ratio constraint

"pass" Transistor problem

2-1 MUX

"Leap"

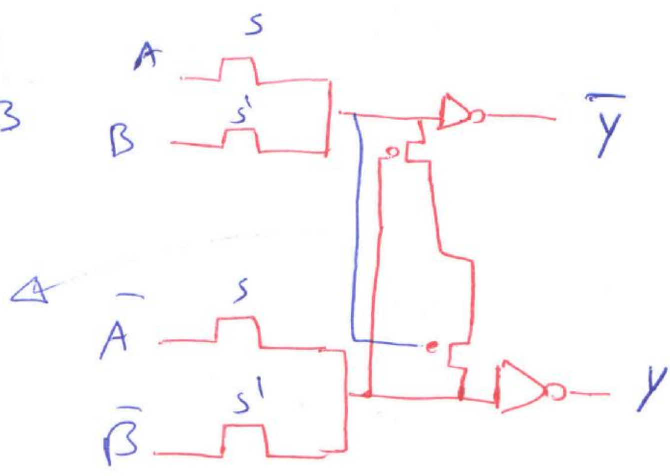




$f = A\bar{S} + BS$

CPL : Complementary pass-transistor logic

1. Dual-rail
2. avoid FB



⇒ fighting: lossing power

faster
stop fighting

\# to implement The Function & its complement

no Ratio needed

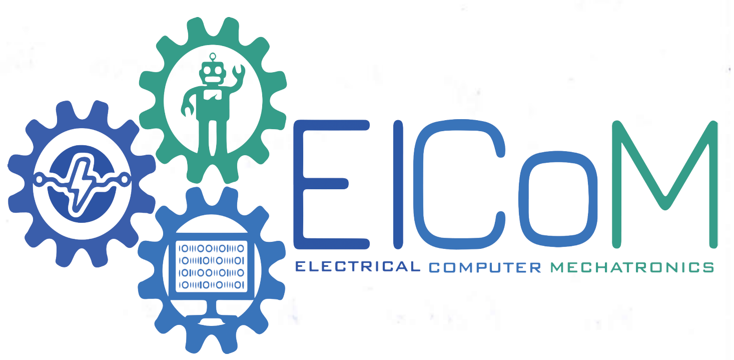
Challenges

1. noise
2. charge sharing
3. leakage & sensitivity
4. monotonicity monotonicity woes

→ illegal for dynamic gate to drive another

1 → 0 output will be discharged to undetermined value during evaluation

5. hungry power



lecture: 7 Power

Total Power = Dynamic + Static

Dynamic → Switching

Static → subth + gate leak + junc

Power

Power & energy

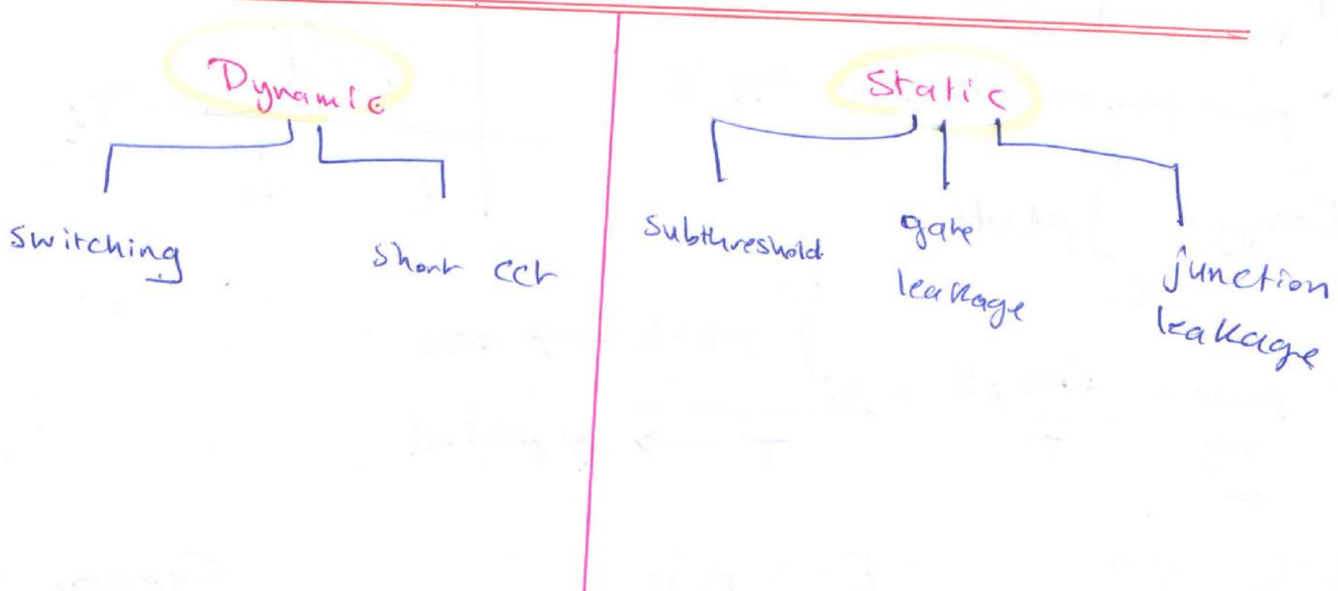
power: from source → V_{DD}

Dynamic like: NOR, XOR, NAND when output changes

instantaneous power = $p(t) = I(t)\,V(t)$

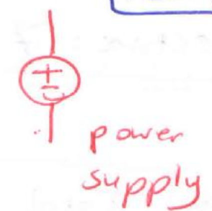
- energy = $E = \int_0^T p(t)\,d(t)$

- averagy power = $P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T p(t)\,dt$



power: how much consuming energy in the time unit

$P_{VDD}(t) = V_{DD} \cdot I_{DD} \Longrightarrow \frac{E}{T} = \frac{Q \cdot V}{T}$ ⟸



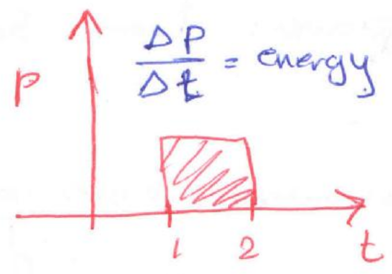
* $P = I \cdot V$

$$P_R = \frac{V_R^2}{R} = I_R^2 \cdot R$$ ⟸ R

$$E = \int p(t)\,dt = \int_0^\infty I(t)\,V(t)\,dt =$$

---

① $P = \frac{E}{T}$ power is Rate



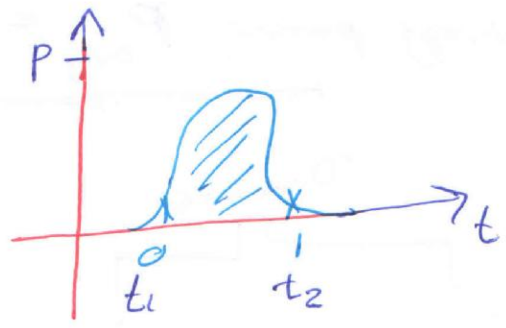
$\therefore E_{total} = P(t) \cdot \text{Time}$

instantaneous power calculated using $\int$

energy = Area = $\int$

② $P_{Diss} = I \cdot V_{DD}$

↳ power generated by power supply



$$\text{Energy} = \int_{t_1}^{t_2} p(t)\,dt$$

$$\therefore \text{power}_{avg} = \frac{\text{Energy}}{T} = \frac{\int_{t_1}^{t_2} p(t)\,dt}{T}$$ $\int p(t)dt$ → area, T → period

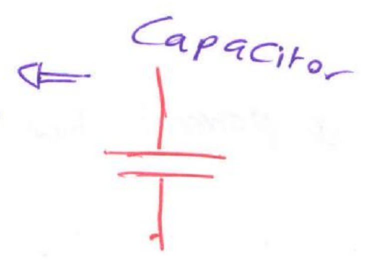
③ $Q = C\,V$

$I = C\frac{dV(t)}{dt}$

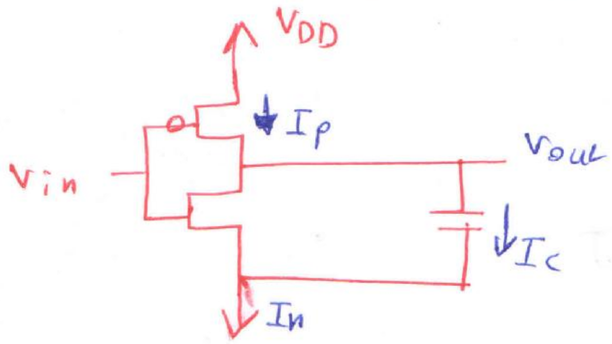
$$\therefore E = \int I \cdot V = \int C\,V(t)\,\frac{dV}{dt} \cdot dt = \int C\,V(t)\,dV = \frac{C\,V(t)^2}{2}$$

$$= \frac{1}{2} C V_c^2$$

⟸ Capacitor



$$P_{total} = P_{dynamic} + P_{static}$$



ملاحظة:
ال power مصدر ال Supply
دائماً الجهد لأنه VDD ثابت
لا يتغير

Energy Dissipated from power supply to C

$$\text{energy} = \int I\, V(t)\, dt$$

$$I = C\frac{dv_t}{dt} \qquad V(t) = V_{DD} \text{ Constant}$$

$$\therefore \text{energy} = \int_0^{V_{DD}} C \frac{dv_t}{dt} V_{DD}\, dt$$

$$\therefore E = C\, V_{DD} \int_0^{V_{DD}} dv_t$$

$$= C\, V_{DD}^2$$

not time - varient

energy Stored in C

$$E = \int I\, V_t\, dt$$

$$I = C\frac{dv}{dt}$$

$$\therefore E = \int C \frac{dv}{dt} v_t\, dt$$

$$= C\int_0^{V_c} v_t\, dv$$

$$= C\, \frac{V_c^2}{2}$$

Time_varient

Slide 7 ??

⇒ why Stored < dissp ??

⇒ because half of power energy from power supp[ly] ... in PMos as heat & other half is stored ... → سببه ال collision between atoms

if Vout falls:

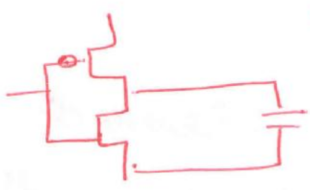
1- Ec goes to GND half
2- energy diss as heat in nMos half

$$\therefore \text{Power Stored} = \frac{1}{2}\ \text{Power Supply}$$

example

$V_{DD} = 1$. volt $f = 1\ GHz$

$C_L = 150\ fF$



مهم جداً التمييز بين power و energy

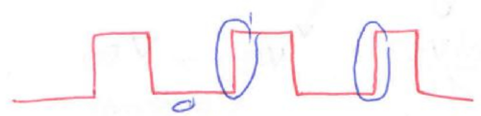
① energy ~~power~~ diss from power supply

$$E = C\ V_{DD}^2 = (1)^2 (150) = 150\ fJ$$

② power stored in C

$$E = \frac{1}{2} C\ V_C^2 = \frac{1}{2} \text{ power supply} = \frac{1}{2} (150) = 75\ fJ$$

Switching power



$$P_{switching} = \frac{1}{T} \int_0^T i_{DD} V_{DD}\, dt$$

0 → 1 energy from power supply
from battary

$$= \frac{V_{DD}}{T} \int_0^T i_{DD}\, dt = \frac{V_{DD}}{T} \left[T f_{sw} C\ V_{DD} \right]$$

$$\therefore \text{power}_{sw} = C\ V_{DD}^2 f_{sw}$$

$$P = \frac{E}{T}$$

$$\text{Energy}_{sw} = C \cdot V_{DD}^2 \cdot f_{sw} \cdot T = C\ V_{DD}^2$$

⇒ but if clock is dynamic and The transitions not = 1

activity factor = 1 = α
↳ how many transitions in The period

$\alpha = 0.5$

$$\therefore \text{power}_{sw} = \alpha\ C_L\ V_{DD}^2\ f_{sw} \Rightarrow P_{dynamic}$$

= short لأنها صغيرة متجاهلة

example slide 11

1 billion = 10^9

$V_{DD} = 1$

$f = 1\ GHz$

$\lambda = 25\ nm = 0.025\ \mu m$

① 50M Logic
$W = 12\lambda$
$\alpha = 0.1$

② 950M Memory
$W = 4\lambda$
$\alpha = 0.02$

المطلوب:
dynamic power Total

$C = 1\ fF/\mu m$ gate + 0.8 fF diff = 1.8

① for Logic ⇒ C_{Logic} = number of chips × width × C

$$C_{Logic} = (50 \times 10^6)(12)(0.025\ \mu m)(1.8)\frac{fF}{\mu m} =$$

$$= 27 \times 10^{-15} \times 10^{6}\ F = 27\ nF$$

② for memory $= (950 \times 10^6)(4)(0.025)(1.8) = 171\ nF$

$$\therefore P_{dynamic\ Total} = (\alpha C_{Logic} + \alpha C_{Memory})[1^2 * 1]$$

$$= [2.7\ nF + 3.42\ nF] \cdot 1 = 6.12\ W$$

energy = P · Time

$$P_{dy} = \alpha C V_{DD}^2 f$$

\# reduction by minimize
1. activity factor α
2. capacitance C
3. power supply VDD
4. frequency f

مهم جداً
الانتباه اذا طلب ال dynamic أم static

$\Rightarrow$ how to estimate $\underline{\alpha}$ activity factor

probability of node = P_i

$P_i = 1 - \overline{P_i} \Rightarrow \overline{P_i} = 1 - P_i$

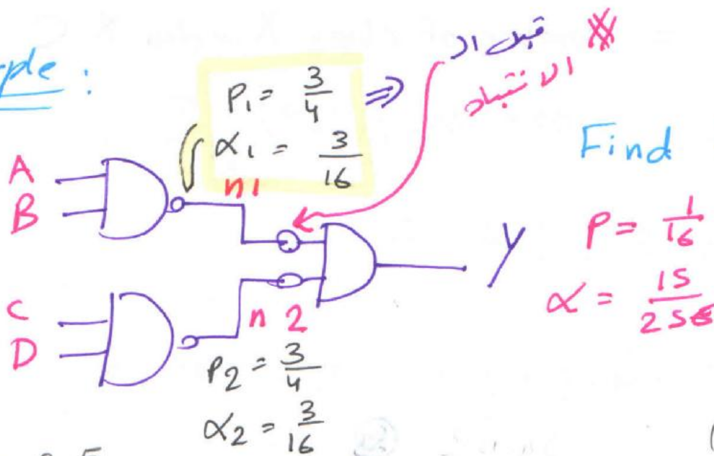
$\therefore \alpha_i = P_i \cdot \overline{P_i}$

$\Rightarrow$ e.g $P_i = 0.5 \Rightarrow \overline{P_i} = 0.5 \therefore \Rightarrow \alpha =$

Slide 14
مطابعة
+ كتابة
المشتقات

AND2 = P_y (output) = $P_A P_B$

example:



Find α if $P = 0.5$

$P = \frac{1}{16}$

$\alpha = \frac{15}{256}$

①

$P_A = 0.5$

$P_B = 0.5$

Nand = 1 - and

$P_A P_B = 0.25$

$\therefore$ Nand $= 1 - 0.25 = \frac{3}{4}$

$P_1 = \frac{3}{4}$

$\alpha_1 = (\frac{3}{4})(\frac{1}{4}) = \frac{3}{16}$

② $P_C = 0.5$

$P_D = 0.5$

Same

③ on $\underline{y}$

$P_1 = \frac{1}{4} = 0.25$

$P_2 = \frac{1}{4} = 0.25$

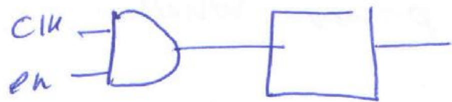
$P = \frac{1}{16}$

$\alpha = (\frac{1}{16})(\frac{15}{16}) = \frac{15}{256}$

مهم الانتباه لوجود ال D قبل ال D

Clock Gating : Killing Clock

- best way to reduce activity of clock in unused blocks
- saves activity $\alpha = 1$
- first must determine if block must be used or not



if clock is killed ⇒ no change & no energy : cct is asleep

$$P_{sw} = \alpha C V_{DD}^2 f$$

gate

- Fewer stages
- small gate sizes
- Smaller Design
- less Diffusion
- less capacitance

wire

long wires ⟶ higher R, higher C

Smaller Design ⟶ Slower Design

voltage scaling: adjust voltage and f according to workload

scaling voltage: ↓ voltage : ↓ freq : ↓ speed

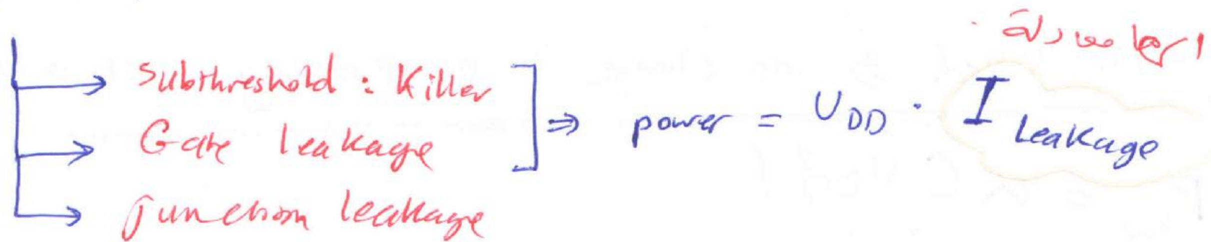
workload: how many to suck energy from Power supp.

~~less~~ & smaller transistors : less power : faster

Scalling device : make it faster with less energy

Smaller device: less $\underline{\underline{C}}$ → cct faster ⇒ less power
less delay

Static power : Consuming & burning power whether
The chip is on or off



Killer : leakage in smaller devices is higher because tox is smaller and allow more electrons.

⇒ Total static power = Total Leakage power

= Subthreshold + Gate + Junction

gate : off — when G = on — ignored

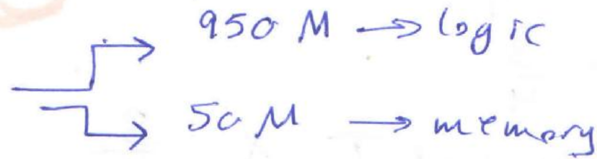
Vt تختلف
باختلاف ال speed

high Vt : slow

Low Vt : fast , high leakage , اكثر صابية , normal $\underline{\underline{Vt}}$

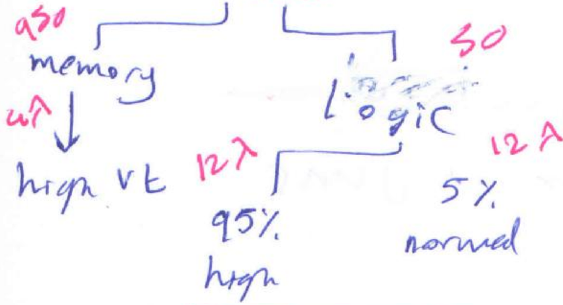
Static power example

$V_{DD} = 1$



1 billion transistors

① subthreshold:



normal 100 nA/μm

high 10 nA/μm

② Gate 5 nA/μm

③ I_{jun} : ignored

Static power = Sub + Gate = $I \cdot V_{DD}$

$= (I_{sub} + I_{Gate}) \cdot V_{DD}$

$I = * \times \lambda \times Vt$

gate : on

sub : off

① Subthreshold

$W_{memory\ high} = 950 \times 10^6 \times 4 \times 0.025 \times 10^{-6} = 95$ m

$W_{Logic\ high} = 50 \times 10^6 \times 12 \times 0.025 \times 0.95 = 14.25$ m

$W_{Logic\ n} = 50 \times 10^6 \times 12 \times 0.025 \times 0.05 \times 10^{-6} = 0.75$ m

$W_{high} = 109.25$ m

$\therefore I_{sub} = \left[\frac{10^{-6} \times 95 \times 10^6 \times 10\,nA}{\mu m} + \frac{10^{-6} \times 14.25 \times 10^6 \times 10\,nA}{\mu m} + \frac{10^{-6} \times 0.75 \times 10^6 \times 100\,nA}{\mu m} \right]$

$= 950 \times 10^6 + 142.5 \times 10^6 + 75 \times 10^6 = 1167.5 \times 10^6 \times 10^{-9}$ A

$= 1167.5\ mA \times \frac{1}{2}$ off $= 584$ mA

---

② Gate ⇒ W = Total = 95 + 14.25 + 0.75 = 110 m

$I_{gate} = \frac{110 \times 10^6 \times 10^{-6} \times 5\,nA \times 0.5}{\mu m} = 275$ mA

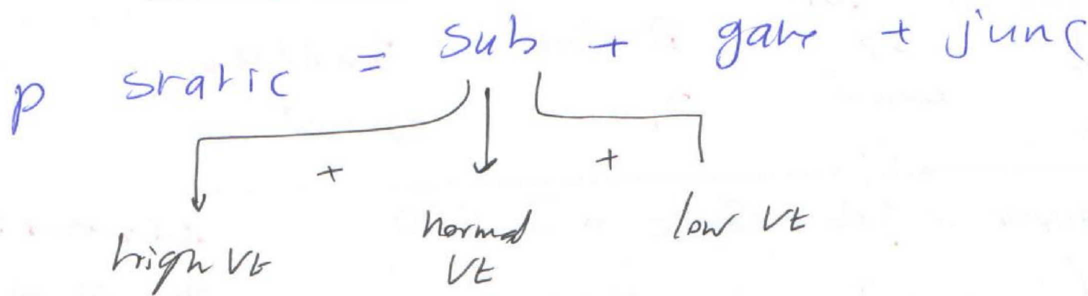
$P_{static} = I \cdot V_{DD} = (gate + sub) V_{DD} = 859$ mW

on = $\frac{1}{4}$

$\therefore$ off = $\frac{3}{4}$

$\therefore$ Subthreshold $I \times \frac{3}{4}$

gate $I \times \frac{1}{4}$



low Vt only when need high speed high Leakage

Speed
Leakage : Low V(t) > normal V(t) > high V(t)

but $P_{dynamic} = \alpha C V_{DD}^2 f$ ⇒ for ~~dynam~~ switching

decrease VDD to $\frac{1}{2}$ but $P = (V_{DD})^2$

$\therefore$ power decrease to $\frac{1}{4}$

اذا طلب ~~leak~~ jun نجمع عادي مع I total بدون تقسيم

كم اي حجم

W total

100 5

1000 50

Leakage Control

To reduce leakeage: ① increase V_t

② increase $\underline{V_s}$ stack effect

③ decrease V_B : body Reverse body bias

$V_t = f(V_{SB})$

$\underline{V_{SB}}$ عشان نزيد

نزيد $\underline{S}$ أو نقلل B

$\underline{\text{If}}$ $V_S = 0 \Rightarrow$ make it < 0 such negative

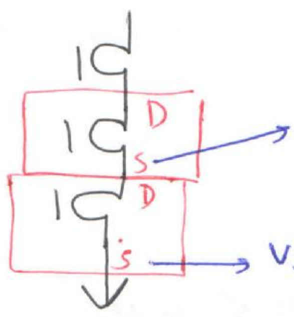
$\therefore V_{SB} \downarrow \Rightarrow V_t \downarrow$ high leakage

$\uparrow V_{DD} \Rightarrow \uparrow$ leakage $\Rightarrow$ make $V_{DD} \downarrow \Rightarrow$ slower

- Low V_{DD} & high $V_t \Rightarrow$ leakage أقل ما يمكن slow
- high V_{DD} & low $V_t \Rightarrow$ fast ccts high leakeage

$\Rightarrow$ trade off

Total power = dynamic + static إذا طُلِب ال



S connected to The drain of previous nMos.
$\therefore V_S > 0 \Rightarrow V_{SB} \neq 0$
$\therefore \downarrow$
V_t أعلى
أقل leakage

$\rightarrow V_S = 0 \Rightarrow V_{SB} = 0$
V_t small

$E = \frac{V_{gs}}{t_{ox}}$ electrons escaped to gate

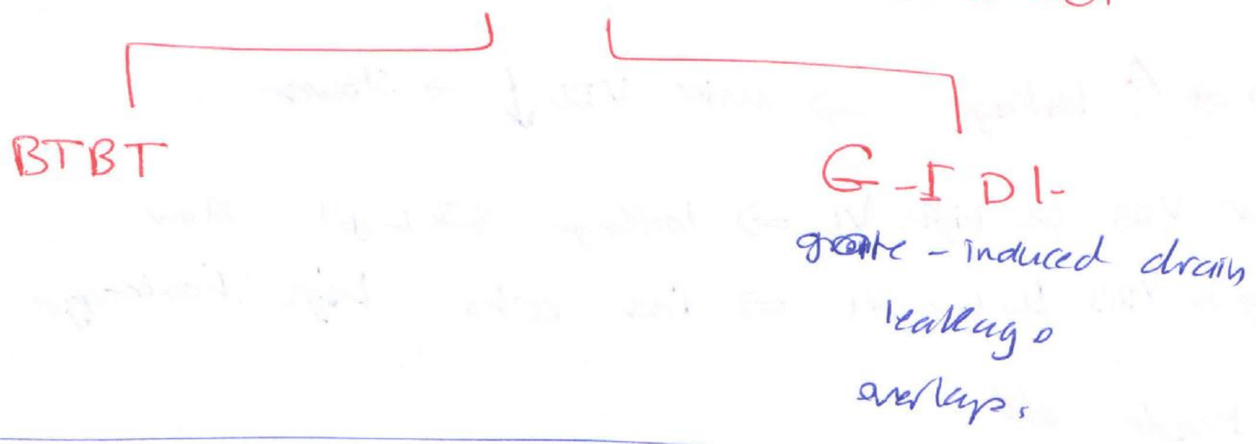
gate leakage gate $\Rightarrow$ S

$V\downarrow \Rightarrow E\downarrow$

max gate leakag when all the gates are ON

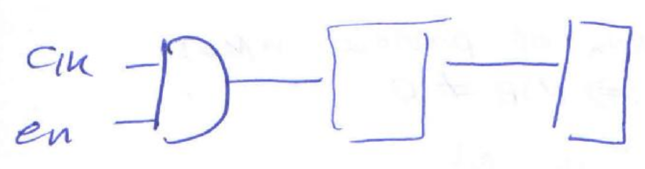
6.3 nA $I_{gp} = 0$
5.63 nA $I_{off} = 9.3$

junction: between Diff & substrate or well

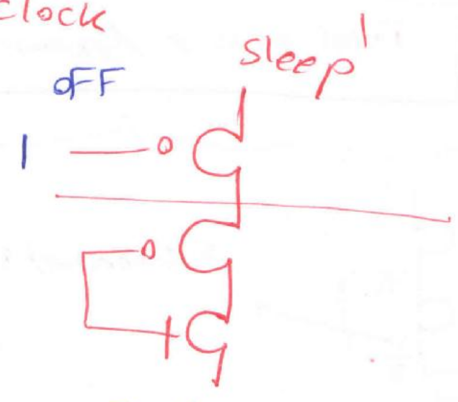


power Gating: shutting / killing clock
save power

power Reduction



dynamic



static
leakage in PMos < nMos
* if sleep=1 ⇒ off: stop leakage to happen
if sleep=0 ⇒ on & off burns power

Wires

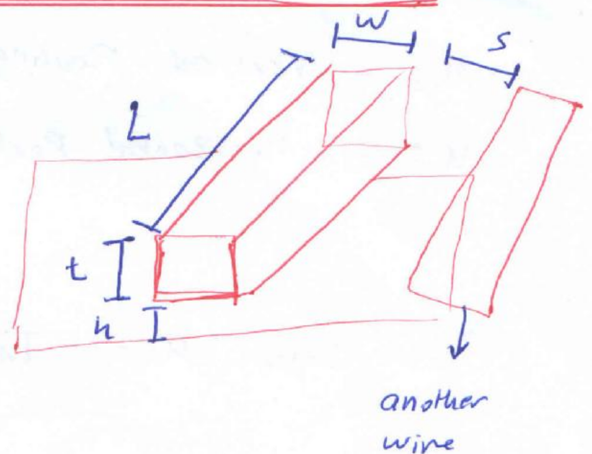
Wires

Wires in Chips = Inter Connect

- → important as transistors → Speed, power, noise
- → linking transistors together
- → play Major role in performance

if wires wide & Thick ⇒ Low Resistance.

Wire Geometry



S : spacing from nieghbors

h: between wire and Conducting Layer

pitch = sum of $W + S$

aspect ratio = $\frac{t}{w} = AR$

old processes ⇒ $AR \ll 1$

modern " ⇒ $AR \approx 2$

example on wires : Intel metal stack

Intel 90nm process

6 metal layers

intel 45nm process

8 metal layers

60nm

3 metal layers

M1 = within Cell - Routing

M2 = Vertical Routing between Cells

M3 = horizontal Routing between Cells

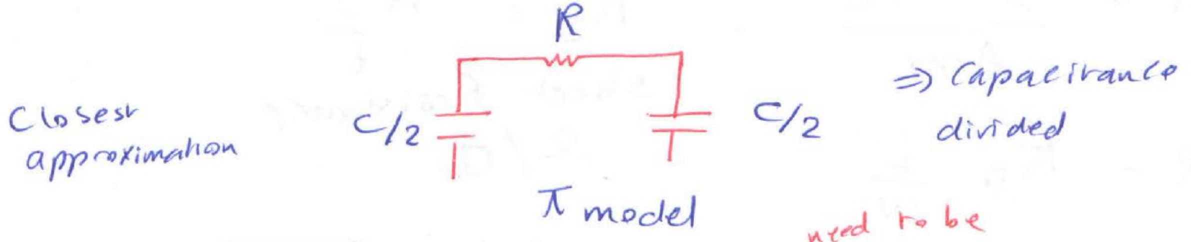
first layer M1 = Thin, narrow, high density

Mid Layers : Thicker & wider

Top layers : Thickest

π Model = Lumped element model

→ 3 segment π model accuracy 3% in sim

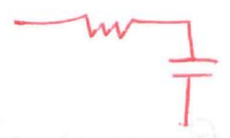


Closest approximation

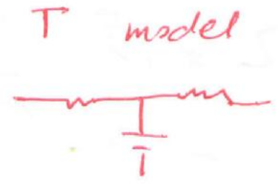
divide wire into (n) numbers parts — need to be large

and Replace each part by π model

L Model



T model



100 segments ⇒

⇒ single segment for elmore is no needed for excessive accuracy keep on π model

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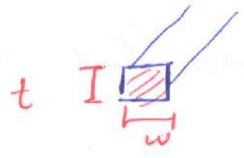
Wire Resistance

مساحة المقطع العرضي

$t * w$ = area



ρ = Resistivity = $\Omega * m$

$$R = \rho \frac{* L}{t * w}$$

$$R_{\square} = \Omega = \frac{\rho}{t}$$

بدون وحدة

⇒ wave of electrons in The wires
make C & R in wire piece by piece

$\therefore R = \frac{\rho * L}{Area}$ $R_{\square} = \frac{\rho}{t}$
sheet Resistance
$\Omega / \square$

$\therefore R = R_{\square} \frac{L}{W}$

$\Omega = \rho \frac{m}{m * m} \Rightarrow \rho = \Omega * m$

we need to decrease delay ⇒ ∴ decrease R and C

∴ we need Low ρ

Copper least Resistivity

more length ⇒ more Resistance

* Cupper must be surrounded by diffusion barrier (→ Low conductivity, high R)
because Cu atoms diffuse into silicon and damage FET's

→ to reduce cross sectional
→ increasing R

⇐ كدة تغير فقط L أو W
t لا تغير

* لأنه اول استي ادا اقرب السلي.

Metal 1

* Contact : metal touches silicon on The CMOS Chip
  (→ wire touches silicon)

many contacts ⟹ lower R

drain touches another drain or source

→ why layers : to shrink area

<u>Via</u> : points where 2 layers touching

- وجود طبقة عازلة barrier
- اذن ستقل مساحة المقطع (المقطع العرضي)
- فتزداد <u>R</u>

$$R = \frac{\rho\, L}{t \cdot W}$$

⇓

$$\underline{R} = \frac{\rho \cdot L}{(w - 2t_{barrier})(t - t_{dish} - t_{barrier})}$$

$(w - 2t_{barrier})$ ← العرض ، $(t - t_{dish} - t_{barrier})$ ← الطول

---

* R for 1mm = 800 Ω
* C for 1mm = 0.2 pF

example 12

Sheer Resisrance $R_{\square} = $ ~~0.22 µm~~

$t = 0.22\ \mu m$

$\rho = 2.2 \times 10^{-8}\ \Omega \cdot m$

$$R_{\square} = \frac{\rho}{t} = \frac{2.2 \times 10^{-6} \times 10^{-2}}{0.22 \times 10^{-6}} = 0.1\ \Omega/\square$$

$w = 0.125\ \mu m$

$L = 1\ mm$

$$R = R_{\square} \times \frac{L}{w} = \frac{0.1 \times 1 \times 10^{-3}}{0.125 \times 10^{-6}} = 800\,\Omega$$

WiRe Capacitance

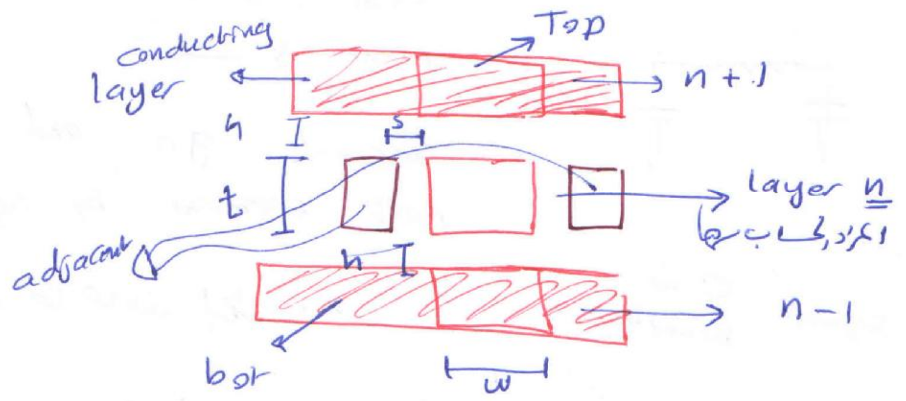
⇒ capacitance in wire include:

→ Top

→ bot

→ adjacent

S: between wire & it neighbor



$$C = \frac{A \cdot \epsilon}{t}$$

كثافة المساحة بين اللوحين الموصلات

$\underline{C}$ تزداد

$W \gg t$

⇒ increasing w, t ⇒ increase C

〃 h, S ⇒ decrease C

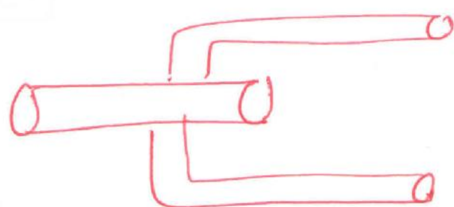
$$C_{total} = C_{Top} + C_{bot} + 2C_{adj}$$

$$\therefore C = \varepsilon_{ox} L \left[\frac{w}{h} + 0.77 + 1.06 \left(\frac{w}{h} \right)^{0.25} + 1.06 \left(\frac{t}{h} \right)^{0.5} \right]$$

C for $1\,\mu m = 0.2\ fF$ $\qquad 1\,\mu m = 0.001\ mm$

for $1\,mm = \frac{0.2}{0.001} = 0.2\ pF$

$\Omega = 800$



How to find R, C, Rent, Cent

Slide 20 From $S \rightarrow i$

π model

First : define the main path from point $S \rightarrow i$

Second: go and analysis the path segment by segment by π model

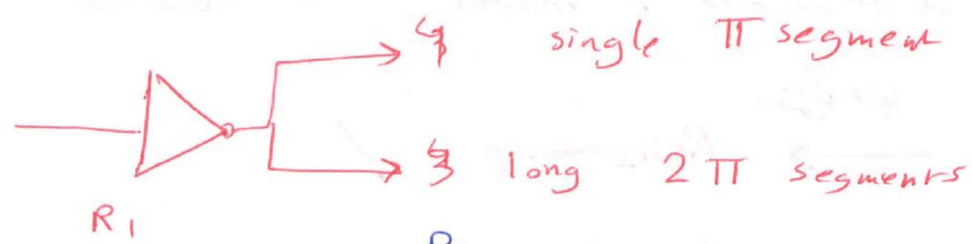
Segment : C on Branch

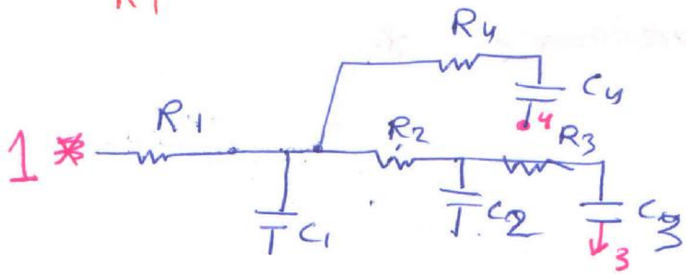
← يتم تصفير اي مقاومة ما بعد الرسمه

$$R_1 (C_1 + C_2) + (R_1 + R_3)(C_3 + C_4) + (R_1 + R_3 + R_i)(C_i)$$

EICoM
ELECTRICAL COMPUTER MECHATRONICS

example 21





مع: الانتباه للطريقة الرئيسية

From 1 → 3

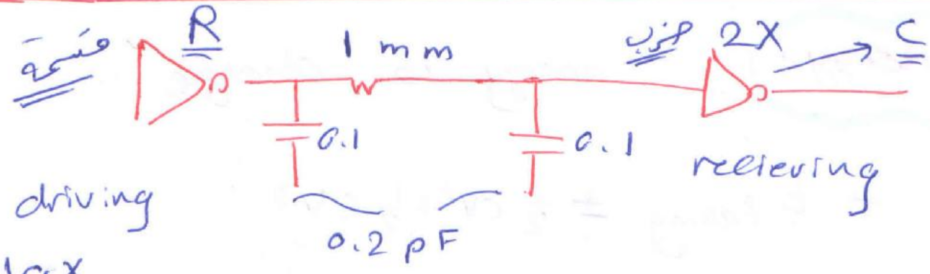
$$delay_3 = R_1C_1 + (R_1+R_2)C_2 + (R_1+R_2+R_3)C_3 + R_1C_4$$

from 1 → 4

$$delay_4 = R_1C_1 + R_1(C_2+C_3) + (R_1+R_4)C_4$$

---

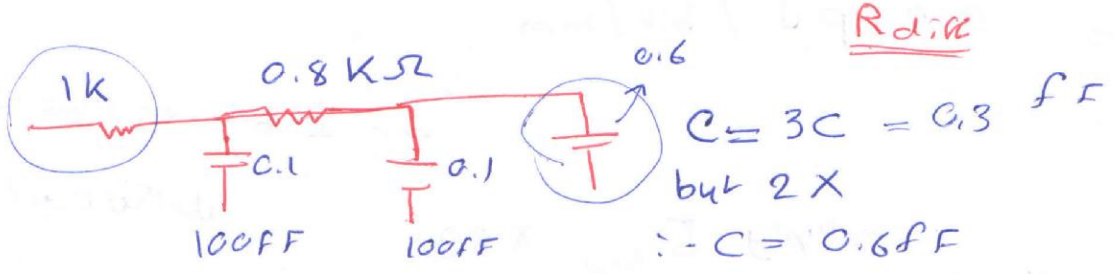
slide 18



$R = 800\Omega$
$C = 0.2pF$

10X → 10 Times size of inverter

⇓ to find RC



$R_1 = 10K$

$R_1 = \frac{10}{10} = 1K$

R_{diff}

$C = 3C = 0.3\ fF$

but 2X

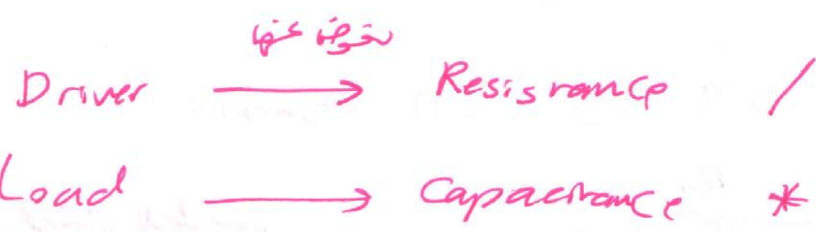
$\therefore C = 0.6fF$

$$Delay = RC = R_1(C_1) + (R_1+R_2)(C_2+C_3)$$

R_1 ← شو ال شحن

تعويض بالقيم فقط

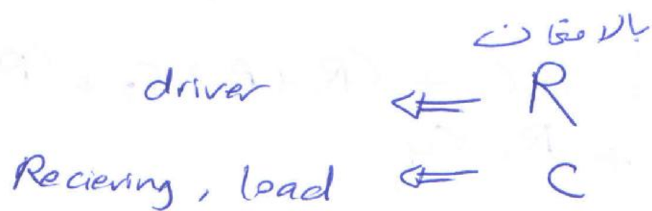
ملاحظة: ال π model مثل نعوض لل **wire**



Driver —(نعوض عنها)→ Resistance /

Load ——→ Capacitance *

we find intrinsic delay



بالاتفاق

driver ⇐ R

Recieving, load ⇐ C

Capacitance = 3C (2 for p Mos & 1 C for nMos)

E. **Wire energy:** energy to charge

$E = E_{rising} + E_{falling} \pm \frac{1}{2}CV^2 + \frac{1}{2}CV^2$

$= CV^2 = (0.2)(1\,V)^2$

$= 0.2\,mW$

$= 0.2\ mW/Gbps/mm$

$= 0.2\ pJ/bit/mm$

لانه نتعامل مع 1 bit فقط

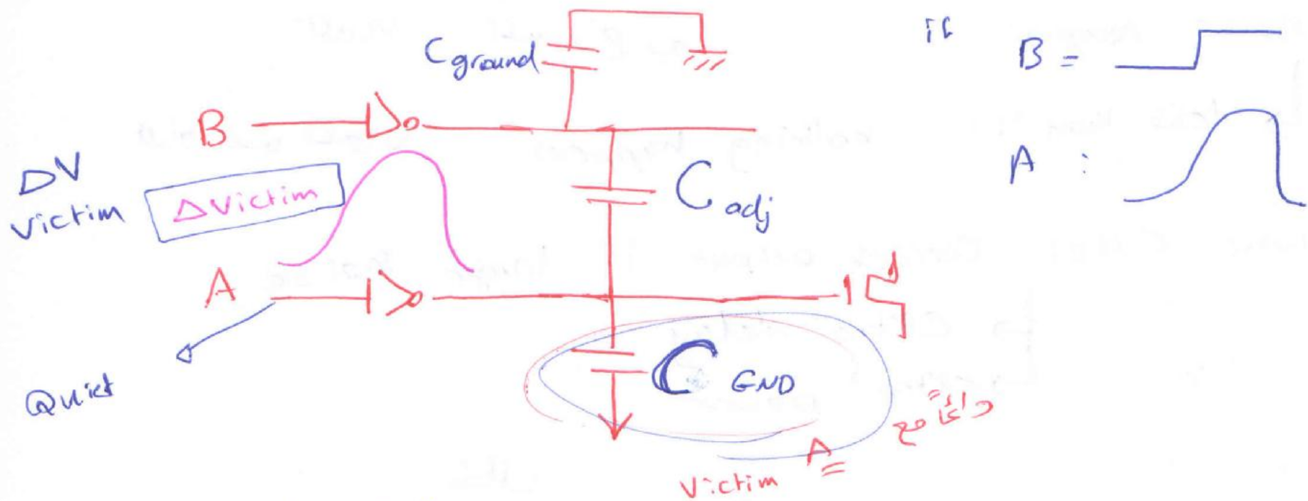
اذا بدنا الكامل

multiply $E_{total} \times 32$

$mW \cdot S = mJ$

$\frac{1}{G} \cdot mJ = n \times mJ = pJ$

Cross talk delay



Victim wire : A

ΔV_{agr} : How far it moves $0 \rightarrow V_{DD}$

$\hookrightarrow = V_{DD} - 0 = V_{DD}$

$$\Delta Victim = \frac{C_{adj}}{C_{gnd} + C_{adj}} \cdot \Delta V_{agr}$$

⇒ larger C_{adj} = larger ΔV victim

⇒ stronger agg = less $\underline{R}$: more adj

⇒ smaller C_{adj} = smaller ΔV victim

⇒ smaller / weaker aggresser = larger $\underline{R}$ ~~less~~ larger Δ Victim

Noise Implications

→ Noise margin: المجال المسموح به

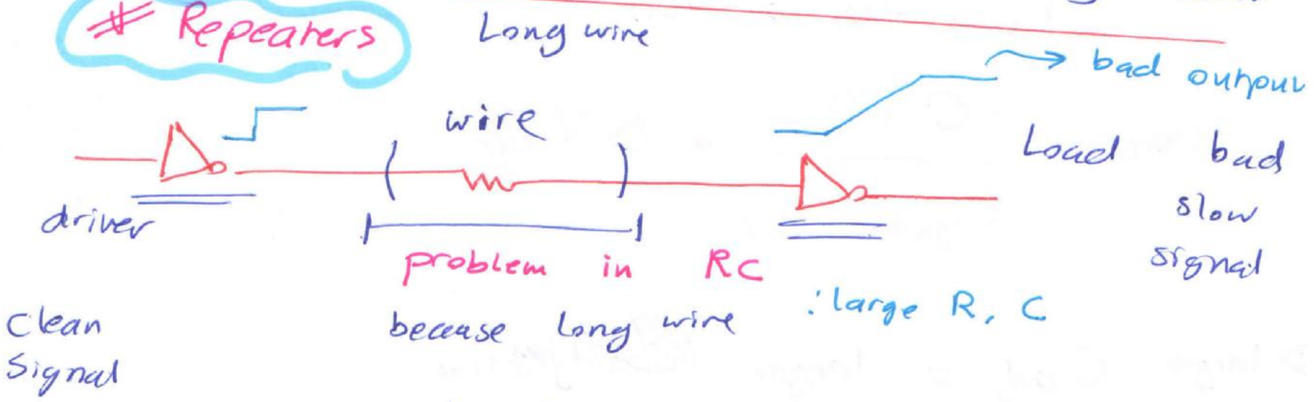
↳ less than it: nothing happens لانه ضمن المجال

Static CMOS: Correct output if large noise
- ↳ extra delay
- ↳ extra power

Dynamic: never recover from glitches (خلل)

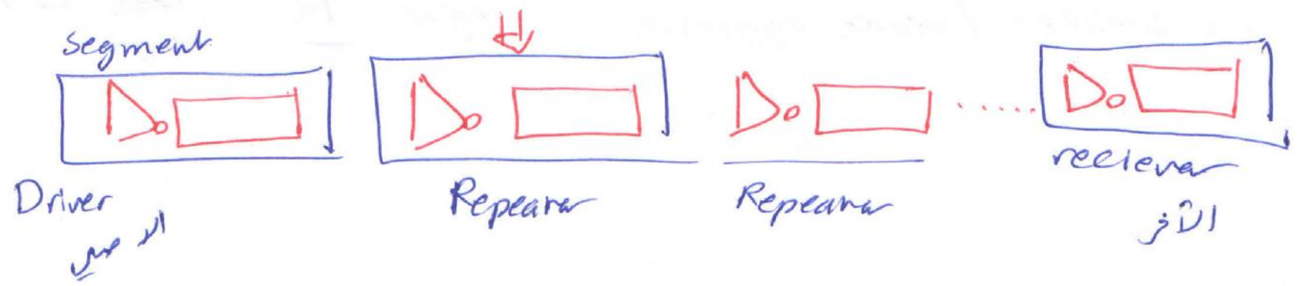
sensitive ccts such memories: produce wrong answer

Repeaters
Long wire



Solution: break wire into small segments and each previous segment work as Reapeater for The next segment

* Repeater: Repeats The Same signal   N Segments



but still There is problem

has a delay
with large energy
large C for gate bo diff

Then each segment length $= \frac{L}{N}$

$\therefore R_w = \frac{R}{N}$

width → nMos = W
→ pMos = 2W

gate capacitance $= C \cdot W$

Resistance $= \frac{R}{W}$

R_w, C_w } per unit length

multiply by $\underline{L}$ ⇒ for whole wire

Driver : Resistance

$R = \frac{R}{W}$

Reciever $= C = C \cdot W$

بالنسبة لـ W فقط

اما ال Segment فهي بالنسبة لـ N

$R_w = \frac{R_w}{N} \cdot L$

$\frac{C_w}{2} = \frac{C_w}{2N} \cdot L$ ↓ for whole wire

$C_w \cdot L$ ⇒ Total Capacitance

delay RC = delay for 1 segment * N

$$\frac{t_{pd}}{l} = 1.67\sqrt{FO4\ R_w C_w}$$

مهم (under FO4); per unit length (under R_w, C_w)

optimum delay of wire devided by length

$$\frac{s}{m} = \sqrt{(s)\left(\frac{\Omega}{m}\right)\left(\frac{f}{m}\right)}$$ but $RC = s$

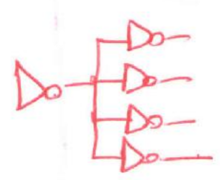
$$\frac{s}{m} = \sqrt{\frac{(s)(s)}{m^2}}$$

$$\text{energy / length} = \frac{1.87}{\text{repeaters}}\ C_w V_{DD}^2$$

example 33

width = 2X

$\therefore R = \frac{R}{2}$



1mm = 800 Ω
0.2 pF

FO4 = 15ps

$R_w = 200\ \Omega/mm$
$C_w = 0.2\ pF/mm$ ⇒ تعطى اذا

$$\frac{t_{pd}}{L} = 1.67\sqrt{FO4\ R_w C_w} = 1.67\sqrt{15 \times 0.2 \times 200}$$

(ps ← t_{pd}, mm ← L) مهم *

$$= 41\ ps/mm$$

مهم *

$$\frac{\text{energy}}{\text{Length}} = 1.87\ C_w V_{DD}^2$$

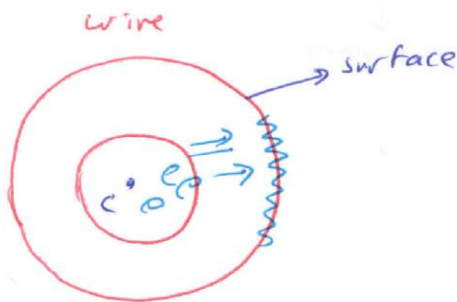
assume $V_{DD}^2 = 1$

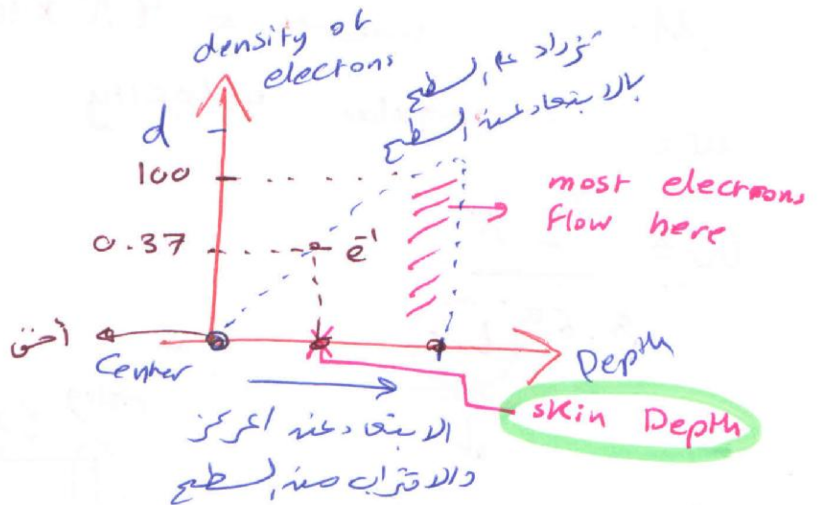
$$\frac{\text{energy}}{\text{length}} = (1.87)(0.2)(1)^2$$

Skin effect :-

at high frequency electrons in wire will be on The surface of Conductor

Then very high freq ... electrons are next to surface





density of electrons will be higher at Surface

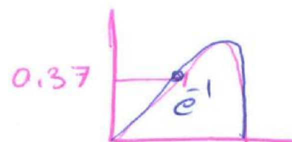
electrons crowded on Surface as well as area of Cross-section is smaller

كلما قلت مساحة المقطع العرضي ← زادت كمية الالكترونات على السطح وبالتالي زيادة R مما يجعل الـ wire طويل وكثيف.

→ rising Resistance

→ reducing Cross-section Area

Skin Depth :



at what point density of electrons $= \bar{e}^1 = 0.37$

most of electrons will flow in this Area

skin depth δ

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}}$$

ρ → Resistivity

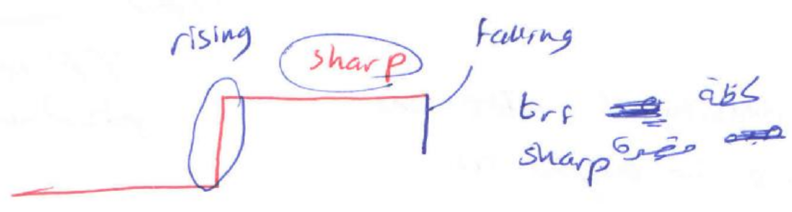
μ → permitivity

μ: النفاذية $= 4\pi \times 10^{-7}$ H/m

H ↓ henry

ω: angular velocity

$$\omega = \frac{2\pi}{8.65\, t_{rf}}$$

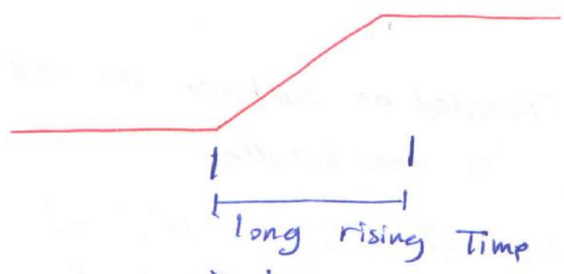


freq الاعلى ⇐ 1 ⇒

$freq = \frac{1}{t_{rf}}$ الادنى

t_{rf} قليلة

sharp مقعرة



2 ⇒

long rising Time

∴ longer period

∴ freq is slower

$$f = \frac{1}{t_{rf}} = \frac{1}{period}$$

$$\therefore \omega = \frac{2\pi f}{8.65}$$

example 35

ch. 9
lecture 9

Sequential ccts

Sequential cct Design

2 techniques types:

Static — dynamic

---

memory element can be used for 2 functions:
1 - Store part
2 - Read/write part

---

① Latches: CKT's Tech type

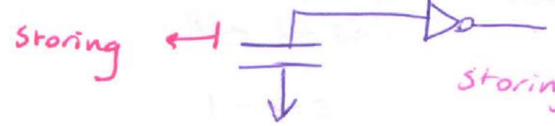
Static

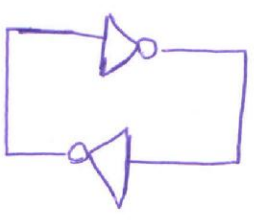
Feed back

- back to back inverters
- Saves data in static
- no lossing data as long as The power is on

dynamic

- data saved on Capacitor
- need to be refreshed each time (rewrite)





- will loss its value after some time because of leakage

we can use MUX

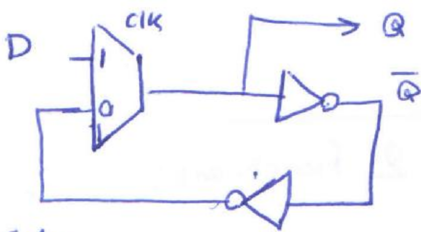
⇒ Fundamental job: store The data
storing independent of CLK value

using Mux in D latch

How to write anew value (write part)

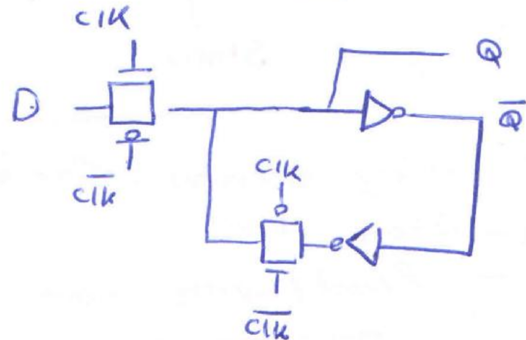
we use decoder in static and transmission gate in dynamic

static



decoder
MUX: keep saving the old data or allow new data to be written on the storage element depending on value of clk which determine selection of Mux

dynamic

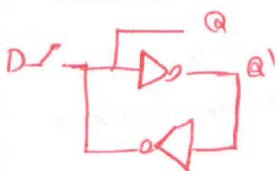


Transmission Gates:
allow new data to get in capacitor
* if its on: write
off: keep saving data
↳ storing part

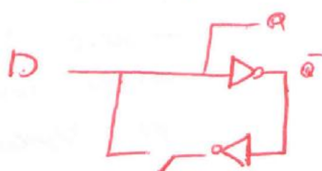
if clk = 0 storing part
D بغض النظر عن قيم ال

when clk = 1
اكتب القيم الجديدة بغض النظر عن القيم القديمة.

clk = 0



clk = 1

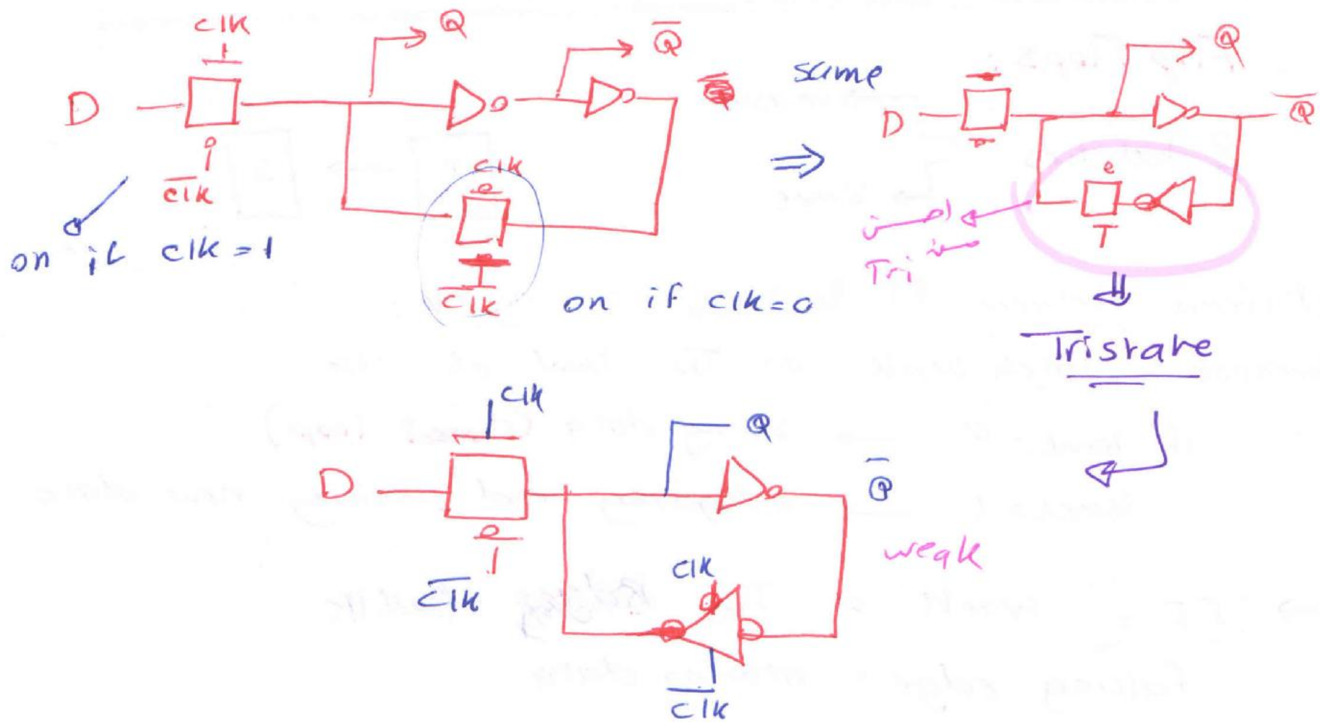


static latch

The multiplexer can be achieved ~~b~~ using pass Transistor or transmission Gate for better results

→ ~~…~~ can be achieved using tristate

→ better than dynamic latch and essential because ~~?~~ of ~~…~~ leakage in dynamic which causes loss of data



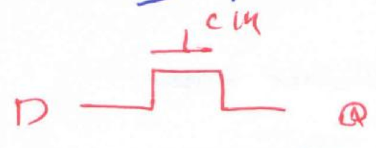
⇒ Static using transmission Gates or Tristate as multiplexer

→ static because

Transmission + inverter = tristate

Dynamic latch

- Store data on some kind of gate or diffusion
- using pass Transistor



if clk = 0 saves old value/OFF
if clk = 1 its on and accept new data

→ clk is using to store data on Capacitor

(1) using pass Transistor:
good because - Tiny
- low clock load (one transistor)

الايجابيات

السلبيات: - (1) max = $V_{DD} - V_t$

(2) non Restoring (The noise is Copied)

(3) back driving: if no well design The cct will be drived to other way
لأنه تم الـ D التاليه سوف تتغير وهذا خطأ

(4) output noise sensitive

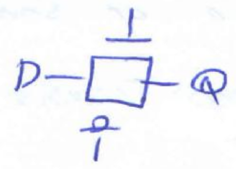
(5) diffusion input:
because D can be dropped at VDD or Vss

اخطر والهم نقطة ⇐ (6) Leakage: The data will be lost (= 0) after some time because of leakage Current

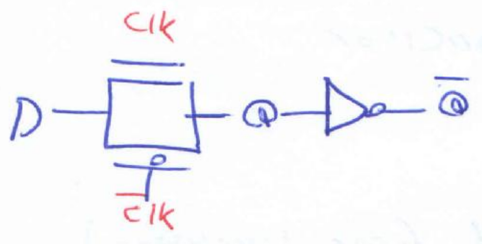
(7) need periodicly refreshing ⇒ need power

Dynamic using Transmission

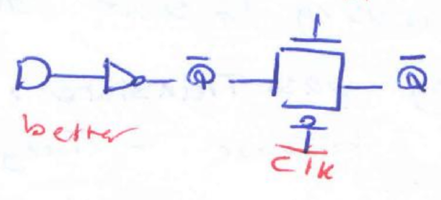
- max V_{DD}
- requires inverted Clock
- leakage : lose value after some time



يكون B كلا الطريقتين



or



→ Restoring ⇒ inverter will Kill The noise

→ no Back driving

→ Fix output noise sensitivity

→ Fix diffusion input

→ output is inverted

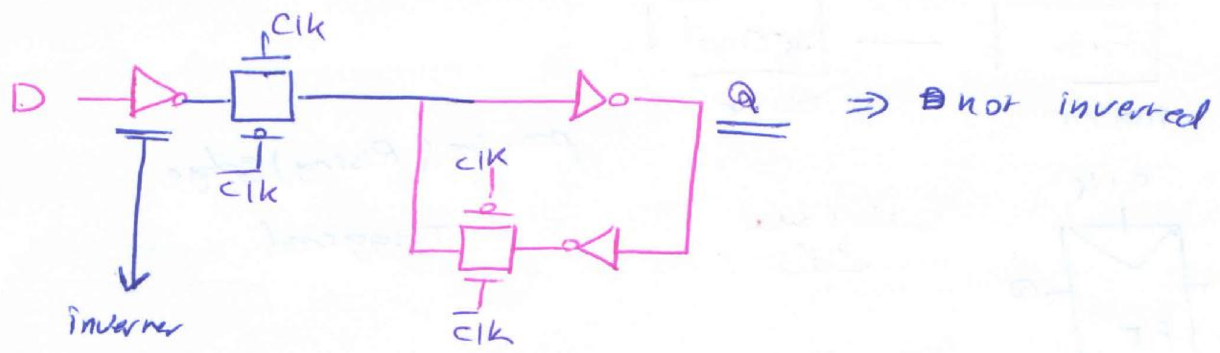
no feedback

مهم

مهم جدا : التمييز بين Dy وال static

non inverting static latch

= latch + inverter on input



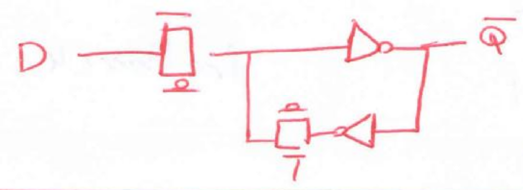
⇒ not inverted

→ noninverting
→ Fixes diff input
] ⇒ الإيجابيات

input is buffered

⇒ **best**
no leakage
no diff problem
no inverted output

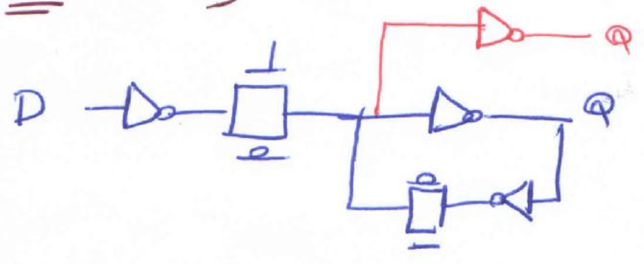
بالرغم من ان النوع ال inverting :-



Smaller
faster
no buffered input
→ diffusion input

---

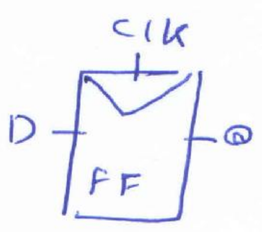
noninverting and buffered output



- output is buffered
- no back driving
- robust
- slow
- high clk load
- large
-

F.F : update The value only at Rising edge

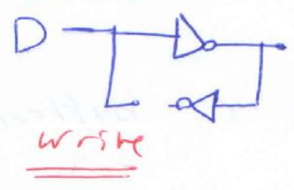
positive (Rising) edge
Triggered

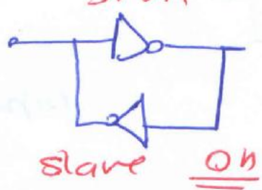


[illegible]

if clk = 0 master slave

Store

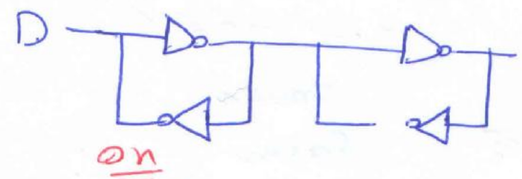




static

if clk = 0

if clk = 1



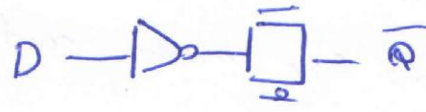
→ static لأنه في feedback

master on if clk = 1

store write

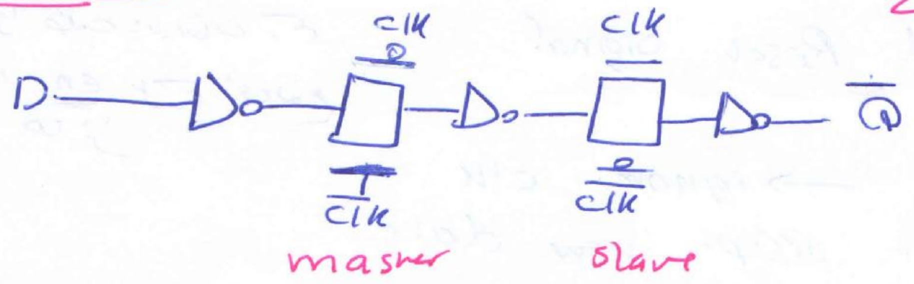
العمليات عكس بعض

dynamic latch :



Flip Flops

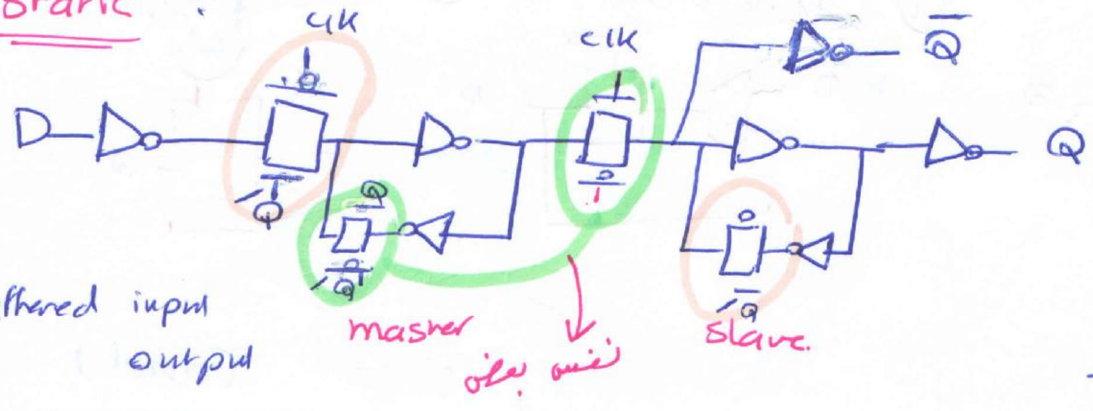
Dynamic :



** الانتباه للرسم يطلبه بالامتحان

البداية عندما
clk = 0
clk
0 → 1

static :



buffered input
& output

نفس بعض

If any master or slave is storing
The other is writing

مختلفات في العملية .
والعكس صحيح

if clk = 0

master : getting new data
slave : storing

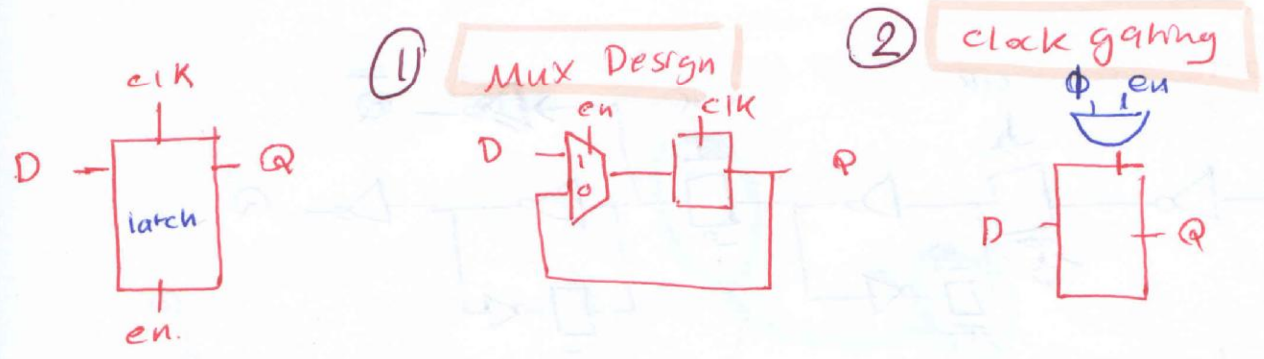
\# When clk goes 0 → 1

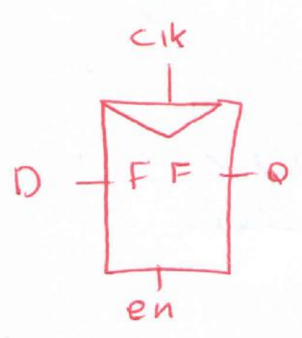
- writing ~~from~~ ends in master and starts in slave
- at Rise edge of clk
- befor Rising: writing on master
- after " : " " slave

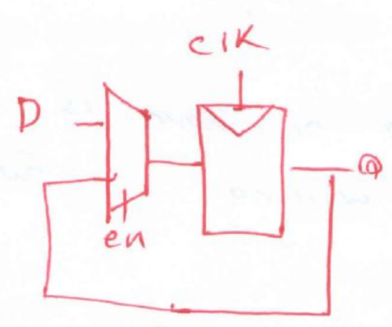
\# Enable and Reset Signal

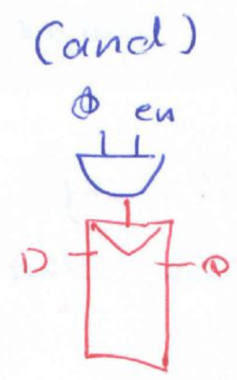
\# اذا طلب بالامتحان رسم بال en نرسم اي نوع جائز

if enable = 0 → ignore clk
↳ don't accept new data









en = 0 storing

en = 1 accept new data from D
تتغير قيمتها

⇒ Kill the clk

if en = 0 (store) don't see clk

if en = 1
- look to clk value
- ↳ take new data

Reset : enable تشتغل زي

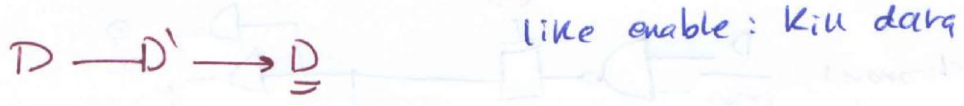
→ fundumental signal and more important than EN

- → synchronous
- → asynchronous

⇒ Sets output of FF to Zero

① synchronous : output changed based on value of clk

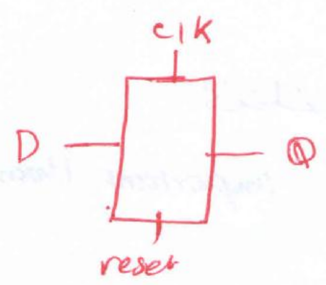
even number of inversions must be between D & Q



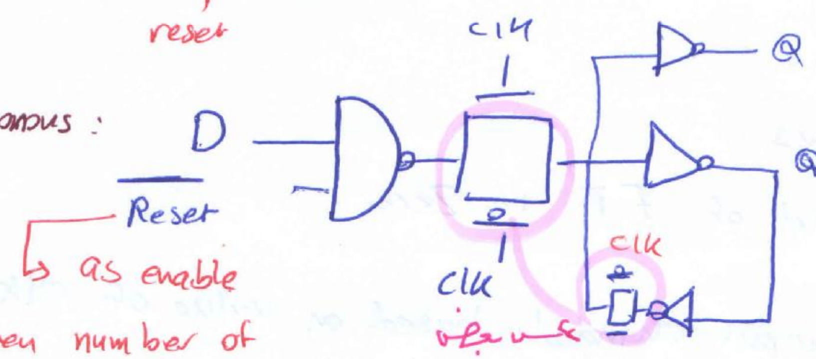
② ~~asy~~ Asy : ~~reset~~ ~~like~~ assert reset : Change Q immediately independently of clk in feedback

don't wait for clk

⇒ using static Design



① synchronous :

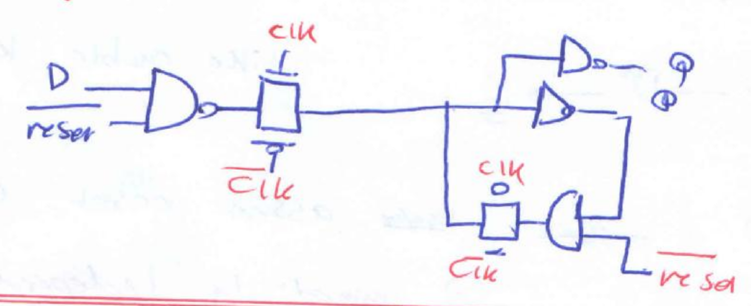


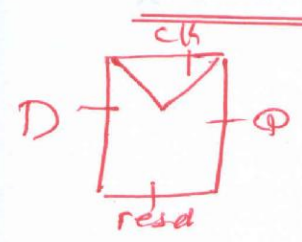
↳ as enable

→ even number of inverters

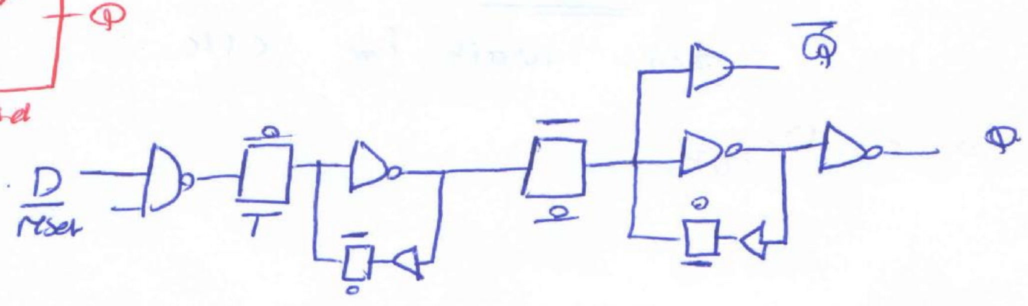
→ if Reset change output based on clk value

② asynchronous



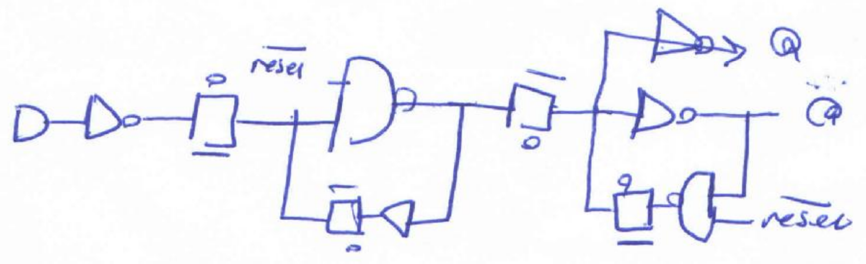


① synch.



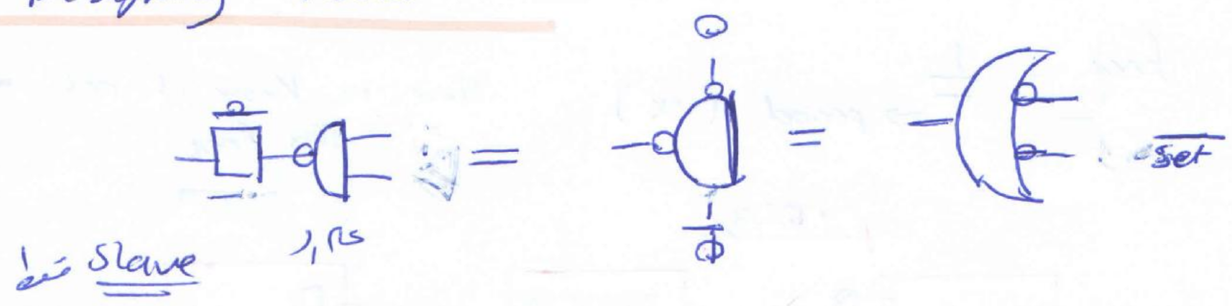
الأقرب

② asyn



$\overline{Reset}$: if logic = 1 (not activated) : normal operation

In Designing Reset (FF)

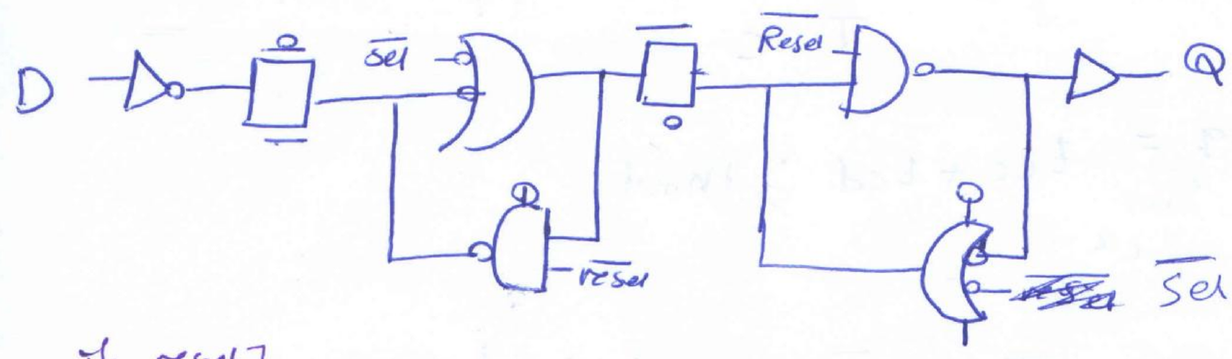


فقط Slave

$D\!\!\!\triangleright = $

Set

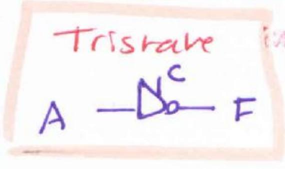
asynchronous FF



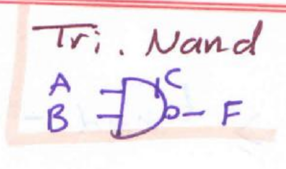
If reset] activated
set]

reset الدخل اولوية

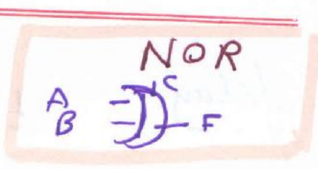
Tristate

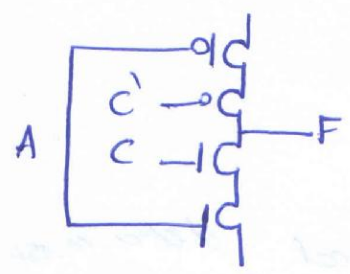


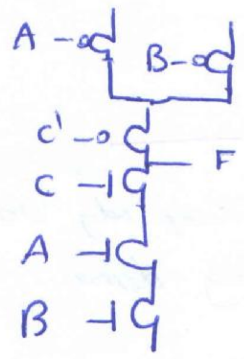
Tri. Nand

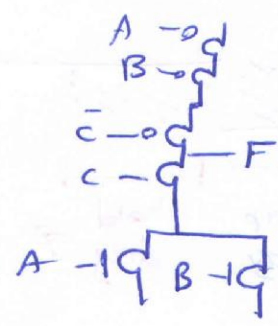


NOR





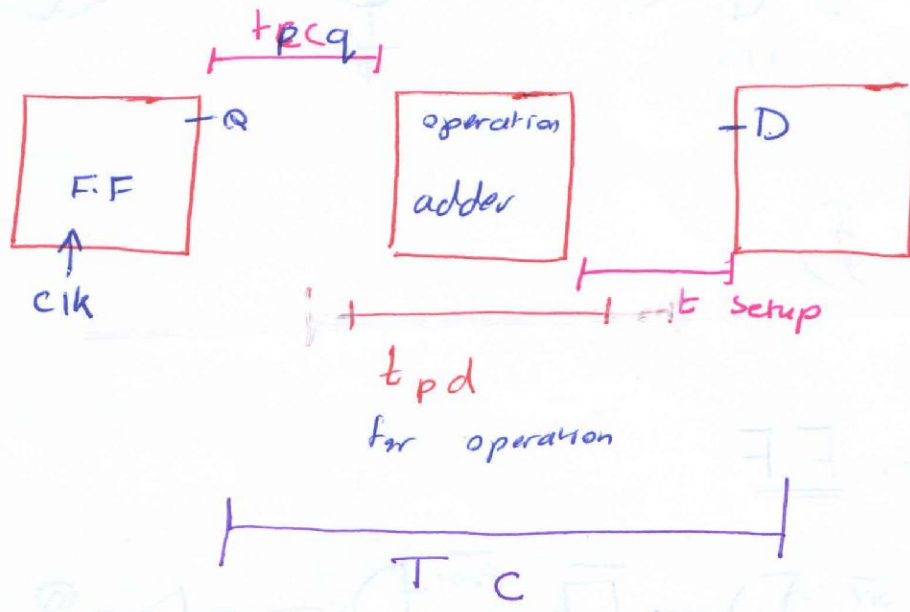




Timing

$freq = \frac{1}{T}$ → period (clk)

How to know if ccl works on This freq

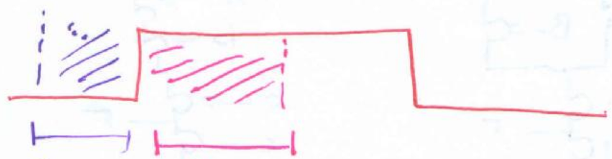


$t_{pcq} = t_{cc} + t_{cd} \geq t_{hold}$

(clk ↓, output of clk ↓)

max delay $T_C \geq T_{pcq} + t_{pd} + t_{setup}$

mini delay $t_{cd} \geq t_{hold} - t_{ccq}$



Setup delay — hold delay ⇒ not completely started, holding data not changed, data must be stable

$t_{hold} \leq t_{cd} + t_{cc}$

clk skew: اختلاف مواعيد وصول الـ clk سببه اختلاف ⇐ يجب مراعاة الـ skew في الحسابات.

Scaling

⇒ number of transistors is exponential with Time

Moore's law: number of transistors double's every 18 month and scaling transistors is The enabler for moore's law

---

Scaling: making transistors smaller (Shrinking)

∴ faster
∴ effect of Gate capacitance less.
∴ R ↓
∴ RC ↓

∴ more transistors per IC
∴ large die

⇒ Computer is faster:

1. Smaller & Faster transistors
2. fewer gate delay per cycle
3. better micro architecture.
4. more transistors per IC
5. lower power

shrink by 30% (2→3 years)

- smaller then faster
- Cheaper
- lower power
- wires not improved

shrinking (scaling) by factor S

$S = \sqrt{2} = 1.41$ (when move from tech to another)

assume every 2 years

2000	100 nm
2002	70 nm
2004	4 nm

⇒ Same tech

⇒ if moving to another tech use $\sqrt{2}$ (decrease)

تقل السلبيات (مثل البارزيتيات) وال delay
وتزداد الايجابيات (مثل الحجم) والتيار

$L = 130$ nm ↓ 65 nm — ضعف / مباشرة

$L = 130 \longrightarrow \frac{130}{\sqrt{2}} \approx 90$

$90 \longrightarrow \frac{90}{\sqrt{2}} = 65$

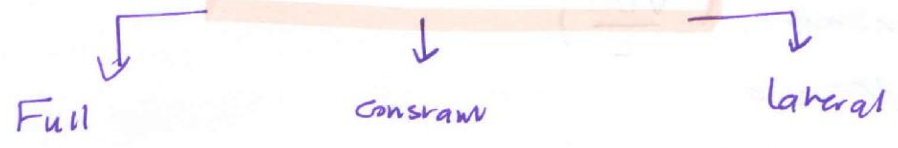
$65 \longrightarrow \frac{65}{\sqrt{2}} = 45$

45

⋮

going to The half (130 → 65) by 2 steps.
it's easier since The Configuration steps are good to new tech

Technology scaling Methods



Transistors

Physical

scale: L, t, w

قطع الحاجات الفيزيائية

if only This : Constraint

or if L only : lateral

Voltage

scale: VDD, Vt

تغيير الفولت

+ → if This plus physical called : Full

---

but it's difficult to scale Voltage

→ scaling physical Features without scaling voltage This will Cause very high electrical field

$$E = \frac{V}{\text{distance}} \rightarrow$$ تصغير, E تزداد

which will impact operations of device due to

- velocity saturation ↑ (lateral E)
- Leakage ↑ (vertical E)

(Donnard)

1 **Full Scalling**: physical + voltage

E : Constant ($\frac{VDD}{L}$)

delay: decrease

power, Area: decrease

But make sure not desirable to change voltages

example

L_1 = 90 nm L_2 = 65

V_{DD_1} = 1.4   ∴ V_{DD_2} must be 1.0

in order to keep $\frac{V\ DD}{L}$ constant for E

E: constant

Constant voltage

2 **Constant**: change physical features only

dimensions ↓

voltages —

E: ↑

power: ↑

suffers from power issues

leakage problem & velocity saturation

3 Lateral : Gate shrink

only shrink L

E: ↑

area: same

Device scaling: الجدول سلايد 7

N: تزداد

$S > 1$

$\frac{1}{S} < 1$

$S = \sqrt{2}$

$\frac{1}{S} =$

$\frac{1}{S^2} =$

$S^2 =$

$S^3 =$

مهم: في الامتحان يحدد نوع ال tech ويطلب ماذا يحصل عن القيم التي فيه وما قيمتها الجديدة.

Example Slide 8:

$L = 65\,nm \downarrow$ $f = 1\,GHz \uparrow$

$V_{DD} = 1.25$ $P = 1\,W \uparrow$

- تقل الابعاد
- وتزداد الطاقة المنتجة
- يزداد ال freq

new $L = 45\,nm$ using Constant Voltage

فقط تتغير القيم الفيزيائية بدون الفولتية

$S = \frac{old}{new} = \frac{65\,nm}{45\,nm} = 1.41 = \sqrt{2}$

$f = \frac{1}{t}$, $t = RC$

$C = \frac{W \cdot L}{t_{ox}}$, $C_{new} = \frac{1}{S}$

$R = \frac{V}{I}$ constant $= R_{new} = \frac{1}{S}$

$\beta (V_{DD} - V_t)^2$

$\therefore RC_{new} = \frac{1}{S^2}$

$S = \sqrt{2}$

$S^2 = 2$

$f = f \cdot S^2 = 1 \times 2 = 2\,GHz$

$P = \frac{E}{T} = C V_{DD}^2 = IV$

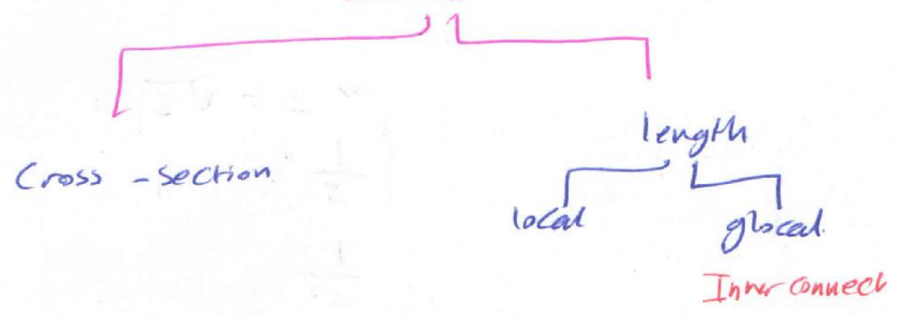
$= (S)$ constant

β تزداد، تتغير

$P = 1 \times \sqrt{2} = 1.41\,W$

Voltage: Constant

Wires Scaling



Global wire

length increased because the increasing of RC (delay)

" " by D_c

بجيه ملصقان

delay for whole wire itself = not change

only delay per unit length changed

⟹ shrinking wires: making them closer to each other

∴ increase C ↑

∴ RC ↑

∴ delay ↑