ElCoM
ELECTRICAL COMPUTER MECHATRONICS

تقدم لجنة ElCoM الاكاديمية

دفتر لمادة:

الكترونيات (١)

من شرح:

د. رلى طوالبة

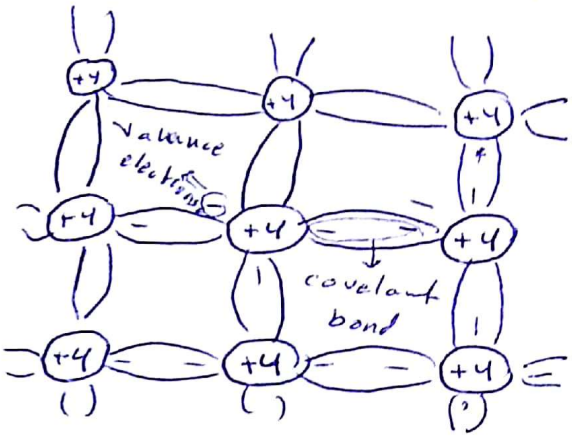
جزيل الشكر للطالب:

باسل البلوي

Energy levels cont:.

conductor — semi

Lattice structure (crystal structure)



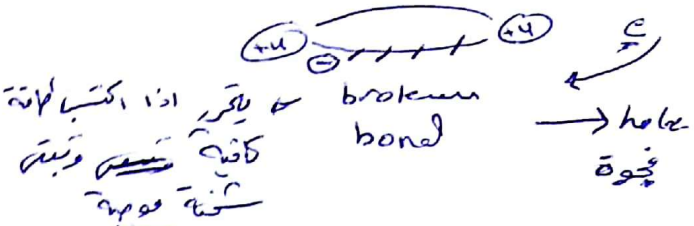
* Atoms are arranged in an orderly pattern.

* at 0k temperature there are no free electrons.

* If enough energy is applied to the semiconductor electrons are able to break free, and move to conduction band and a current.

conduction in semiconductor materials:

* no energy applied ⇒ no free electrons If energy is applied electrons will break free, leaving behind a broken bond and creating a hole that has a positive charge



* An only electron might have enough energy to break free from its atom, so that it can replace the electron mentioned in previous step This electron will leave behind another hole and so on.

In intrinsic semiconductors, the number of electrons = the number of holes

* electrons and holes have the same properties, but have opposite charges and more in opposite direction,

* if an electron is recaptured then an electron-hole pair will dissappear.

Si : (silicon) dop. I ⟶ e

+14, ? ⟶

at 0°k, no free electrons

at room tempreature ≅ 300°k

there are a few free electrons

Energy required for electrons to break free and create ~~a current~~ a current is

$E_g = 1.12 ev$

Example: for a "Si" the number of broken bonds is $10^{11}/cm^2$ for $10^{23}/cm^2$ atoms

$$\frac{10^{23}}{10^{11}} = 10^{12}$$

⇒ 1 electrons free for 10^{12} atom

Intrinsic semiconductors (n_i)

~~electron~~ ~~cond~~

⇒ electron concentration: n

hole concentration: p

$n = p = n_i \Rightarrow n_i^2 = np$

---

n_i depends on tempurature

$$n_i = BT^{3/2} e^{(-E_g/2kT)}$$

$$B = 5.23 \times 10^{15} \left[cm^{-3} k^{-3/2}\right]$$

T : temprature in kelvin

E_g : Energy gap for 1.12 ev

k : Boltzman Const:

1.38066×10^{-23} J/k

86×10^{-6} ev/°k

No.

Example:- At $T = 300^{\circ}K$ find intrinsic carrier concentration for an Si. ($E_g = 1.12$ ev) $K = 1.38066 \times 10^{-23}$ dep $K = 86 \times 10^{-6}$ ev

$$n_i^{\circ} = BT^{3/2} e^{(-E_g/2kT)}$$

$$= 5.22 \times 10^{15} (300)^{3/2} e^{(-1.12/2 \times 86 \times 10^{-6} \times 300)}$$

$$= 1.5 \times 10^{10} \ cm^{-3}$$

1.1.2 Extrinsic Semiconductors :-

* concentration of electrons and holes in an Intrinsic Semiconductor is not enough (to create charge & cond.) ⇒ Semiconductor will be doped by atoms from groups 3 and 5.

group 3 to increase number of holes

group 5 to = = = electron

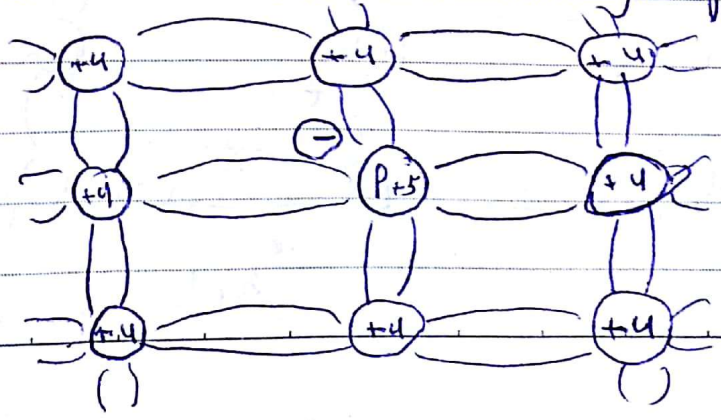
The process of adding holes and elec. is called doping

more electrons ⇒ donor impurity

= holes ⇒ acceptor impurity

Donor Impurity (n-type Semiconductor)

⇒ One Common element from group 5 is phosphorus (P)



No.

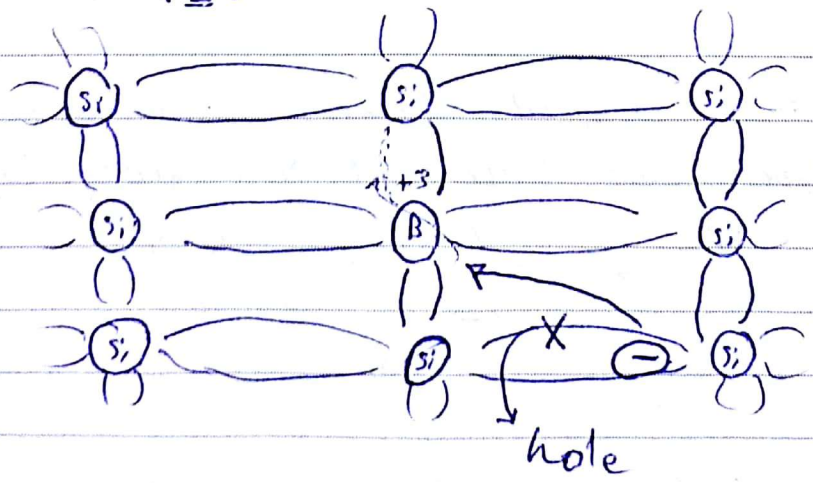
AP atoms has 5 Valance electrons 4 of them are part of the structure and ~~creat~~ creat Covelent bonds with nearby by Si atoms.

* the 5th electron remains Loose and at room temperature it might have enough energy to move away from the atom ⇒ no broken covelent bonds ⇒ no ~~increase~~ increase in number of holes. This causes a +ve charge atom although there is no increase in number of hole

This is called ~~a~~ donor ~~door~~ impurity because (P) ~~pro~~ provided the Semiconductor with extra electrons

~~Donor~~ Acceptor Impurity (P-type ~~Semiconductor~~ semiconductor)

One common element from group (3) is Boron (B)



No.

3 electrons from the B atom are part of covalent ~~Bonds~~ Bonds . One Bond is still empty. Anearby silicon electron has ~~enough~~ enough to break free and to fill the empty Bond, leaving behind a broken bond called hole ⇒ number of holes increases, but number of electrons ~~remains~~ remains the ~~same~~ Same although the B atom gained a (-ve) charge but this doesn't count as a free electrons since the electron is part of the newly created covalent bond.

* This type is called acceptor impurity because accepted a electron from anearly Si atom

Int : $n_i = n = p$

Ext Donor Concentration : N_d

Acceptor : N_a

Thermal ~~Equilibrium~~ Equilibrium :- الاتزان الحراري

no net & low of holes or electrons if Semiconductor is undisturbed in its thermal environment

At thermal equilibrium :- $n_i^2 = n_o p_o$

No.

* n-type material :-

Nd was added $n_o \cong N_d$

$p_o = \frac{n_i^2}{N_d}$

{ e : magority carriers
hole : minority

* p-type material

$p_o = N_a \Rightarrow N_o = \frac{n_i^2}{N_a}$

{ hole :- magority
e :- minority

Ex At T = 300°k, Si is doped with P, $N_d = 10^{16}\ cm^{-3}$ find n_o, p_o ??

$n_o = N_d = 10^{16}\ cm^{-3}$

$p_o = \frac{n_i^2}{10^{16}}$ from last example $n_i = 1.5 \times 10^{10}$

$p_o = \frac{(1.5 \times 10^{10})^2}{10^{16}} = 2.25 \times 10^{4}\ cm^{-3}$

Si & Ge are elemental Sami conductors compound Semiconductors can be created by combining elements from Groups 3 and 5, Such as ~~GaAs (Gallium Arsenid~~

GaAs (Gallium Arsenids)

InP (Indium Phosphide)

No.

Ex 1.2 part b (ii) :- For GaAs, it doped with acceptor Concentration find the concentration of minority and majority carries . $T = 300^{\circ}K$

$B = 2.1 \times 10^{14}$

$E_g = 1.4\ eV$

$N_a = 10^{15}\ cm^{-3}$

$n_i = B T^{3/2} e^{-E_g/2KT}$ $\qquad p_o = N_a = 10^{15}$

$n_i = 1.8 \times 10^{6}\ cm^{-3}$

$n_o = \frac{n_i^2}{p_o} = \frac{(1.8 \times 10^6)^2}{10^{15}} = 3.24 \times 10^{-3}\ cm^{-3}$

1.3 Drift & Diffusion Currents

* Carriers :- +ve charged holes and -ve charged electrons.

* processes that causes carriers to move in a semiconductor :-

① Drift :- due applying Electric to the Semiconductor

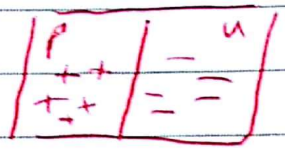
② Diffusion :- due concentration gradient => اختلاف التركيز

ⓐ non homogenous doping of holes and electrons غير متجانس

x electrons and holes move from spot with high Concentration spot with low conc--

No.

(b) injection of holes or electrons in one region and no injection in another like the Pn ~~j~~ junction.

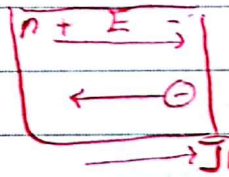


*** Drift Current density :-

$$\text{Current Density} = \frac{\text{Current}}{\text{Area}} \left(\frac{A}{cm^2}\right)$$

→ n-type Semiconductor :-

n-type has a large number of electrons



If electric is applied to Semiconductor electrons will move with avelocity V_{dn} and adirection opposite to that of the electric field.

$$V_{dn} = -\mu_n \mathcal{E}$$

μ_n :- electron mobility (cm^2/Vs)

mobility measure how well electrons can move in asemiconductor

silicon ← For Si → $\mu_n = 1350\ cm^2/Vs$

* Electron movement creates Density Current

(J_n)

No.

with ~~a~~ direction opposite to the direction of electron velocity

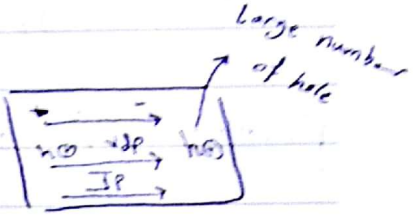
$J_n = -en v_{dn}$

$\Rightarrow$ J_n has the same direction as the electric field

$J_n = -en(-\mu_n E)$

$J_n = en\mu_n E$

P-type semiconductor



v_{dp} :- drift velocity of holes
J_p :- current density
μ_p for Si = 480 cm^2/Vs

$J_p = ep v_{dp}$
$= ep\mu_p E$

Total current density

$J_T = J_n + J_p$
$= en\mu_n E + ep\mu_p E$

$\Rightarrow J_T = \sigma E$

$\sigma \rightarrow$ conductivity $\frac{1}{\Omega cm}$ $\rho = \frac{1}{\sigma}$ (Ωcm)

$J_T = \frac{E}{\rho}$

** If electricfield is due applying voltage to the Semiconductor then this will be a form of Ohm's law

$J_T = \frac{E}{\rho} \Rightarrow \frac{A}{cm^2} = \frac{V/cm}{\Omega\, cm} \Rightarrow A = \frac{V}{\Omega}$

Examples : Find drift current density at $T = 300^{\circ}K$ if Si is doped with As $N_d = 8 \times 10^{15}\ cm^{-3}$

$\mu_n = 1350\ cm^2/Vs$, $\mu_p = 480\ cm^2/Vs$ $E = 100\ V/cm$

$n = N_d = 8 \times 10^{15}$

$p = \frac{n_i^2}{N_d} = \frac{(1.5 \times 10^{10})^2}{8 \times 10^{15}} = 2.81 \times 10^{4}\ /cm^3$

* $p \ll n$
p بنتجاهلها
=> ignore p
and ignore $ep\mu_p E$

$J_T \simeq J_n = 1.6 \times 10^{-19} \times 8 \times 10^{15} \times 1350 \times 100$

P. 1.14

a) $\sigma = 1.5\ (\Omega cm)^{-1}$ (n-type)

$\mu_n = 1000\ cm^2/Vs$, $\mu_p = 375\ cm^2/Vs$.

$N_d = ??$

$\sigma = e n \mu_n$

$n = N_d = \frac{\sigma}{\mu_n e} = \frac{1.5}{1.6 \times 10^{-19} \times 1000} = 9.375 \times 10^{15}\ cm^{-3}$

P: 1.11

a) $E = 10\ V/cm$ $\sigma = 1.5\ (\Omega cm)^{-1}$ $A = 10^{-5}\ cm^2$

$J = E\sigma = 10 \times 1.5 = 15\ A/cm^2$

$J = \frac{I}{A} \Rightarrow I = 15 \times 10^{-5}$

No.

Drift velocity Saturation:-

$v_d = \mu E$

if E increase, v_d increase, until velocity reaches a value of 10^7 cm/s than it reaches Saturation and velocity won't increase anymore

Mobility and impurity concentration

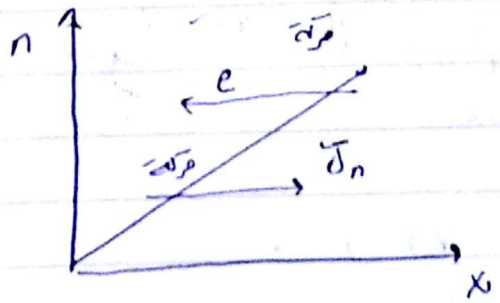
$\sigma = e m n$

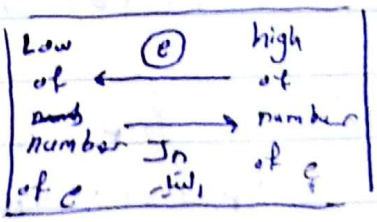
$\mu = \frac{\sigma}{en}$ if concentration decreases, mobility increases

⇒ Diffusion Current Density

Diffusion:- Particles flow from high concentration to low concentration.

n-type semiconductor:-





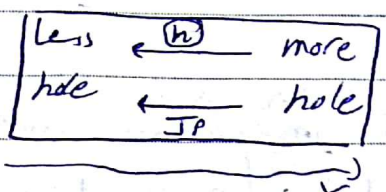
$J_n = e D_n \frac{dn}{dx}$

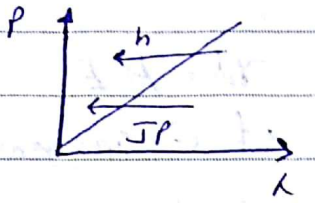
D_n : Diffusion coefficient for electrons

$\frac{dn}{dx}$:- gradient of electron concentration

No.

P - type material



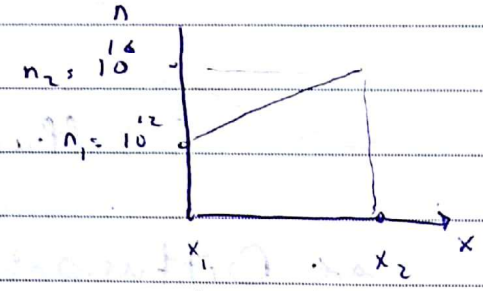


$$J_p = -e D_p \frac{dp}{dx}$$

Ex :- 1.4 Find J_n if $T = 300^0 K$ n changes from $n_1 = 10^{12}$ at $x_1 = 0$ to $n_2 = 10^{16} cm^{-3}$ at $x_2 = 3 \mu m = 3 \times 10^{-6}$

$D_n = 35 cm^2/s$

$x_2 = 3 \times 10^{-4} cm$



$$J_n = e D_n \cdot \frac{dn}{dx}$$

$$\frac{dn}{dx} = \frac{10^{16} - 10^{12}}{3 \times 10^{-4} - 0}$$

$$= 3.333 \times 10^{19}$$

$$J_n = 1.6 \times 10^{-14} \times 35 \times 3.333 \times 10^{19}$$

$$= 187 \ A/cm^2$$

Q 1.17 :- for p_n, $p(x) = 10^4 + 10^{15} \exp(-x/L_p)$ $x \geq 0$

$L_p = 10 \mu m = 10 \times 10^{-4} cm$

$D_p = 15 cm^2/s$

find J_p at a) $x = 0$

b) $x = 10 \mu$

c) $x = 70 cm$

No.

$J_p = -eD_p \frac{dp}{dx}$

$\left.\frac{dp}{dx}\right|_{x=0} = 10^{15}\left(\frac{-1}{L_p}\right)e^{-x/L_p}$ (0)

$\left.\frac{dp}{dx}\right|_{x=0} = \frac{1}{10 \times 10^{-4}} \times 10^{15} = -0.1 \times 10^{19}$

$J_p = -1.6 \times 10^{-19}(15)(-0.1 \times 10^{19})$

$= 2.4 \ A/cm^2$

Mobility Vs Diffusion Coefficient :-

Mobility from Drift current :
Diffusion coeff from different current

* Einstein Relation :-

$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{KT}{e}$ = Thermal Voltage = V_T or ϕ_T

we use if Bolte is given in J/K
If Bolts is given ev/K use

$V_T = KT$

$T = 300°$

At room temperature $\phi_T = 26 \ mV$

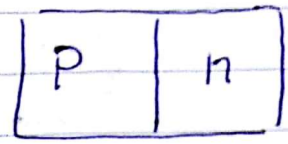
$= 0.026$

0.0258

No.

1.2 The PN Junction :—

P & n material adjacent to each other, forming a single semiconductor, one side doped with electrons and another with holes



① ⇒ in P-type :- magority holes N_A

minority electrons $n_{p0} = \frac{N_i^2}{N_A}$

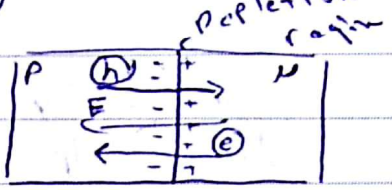
② ⇒ in N-type : magority electrons N_D

minority holes $p_{n0} = \frac{N_i^2}{N_D}$

③ ⇒ Assume :- Uniform doping

Thermal Equilibrium

minority carriers



* Large density gradiant occurs across the junction

① electrons more from N to P ⇒ creat -ve charged acceptor carriers

② holes cross the junction from P to N ⇒ creat +ve charged Donor carriers

* this movement of holes and electrons create a charge on the junction which is called depletion region (space charge region)

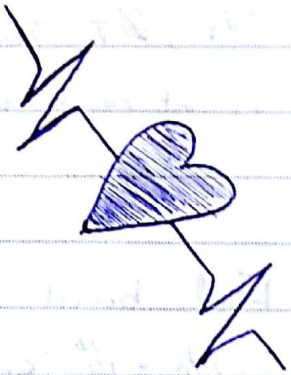
No.

↑ electric field appear across the junction from ℓ (N to P) once this electric field is ~~to~~ ~~sto~~ strong enough such that its force is equal to the force induced by diffusion gradient, it will fight off

holes moving from P to N & electrons ⇐ ⇐ N to P ⇒ charge flow will cease to exist and thermal equilbrium is reached.

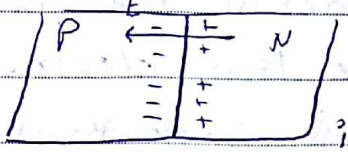
~~and~~ carrier flow will stop

the region around the junction is called Depletion region or space charge region



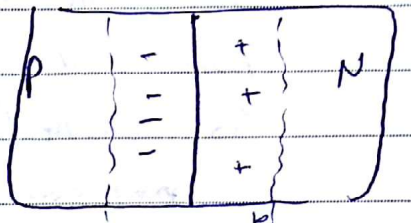
Saturation No. Current

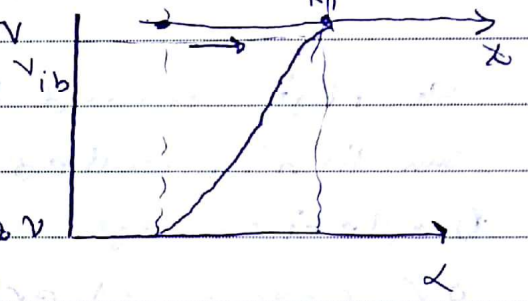
Leakage current, Drift current, since it exists due to electric field E (V. small)



Thermal equilibrium when force induced by Electric field equals force induced by diffusion due concentration gradient

Electric creates built-in barrier potential (V_{bi}).





$$V_{bi} = \frac{KT}{e} \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

V_T, ϕ_T Thermal voltage

V_T at room temp = 0.0259 V

$\simeq$ 2.6 mV

$\therefore$ V_{bi}

Ex: Find built-in barrier voltage Si, T = 300°K

$N_A = 10^{16}$ cm^{-3}

$N_D = 10^{17}$ cm^{-3}

$$V_{bi} = (2.6\text{ m}) \ln\left(\frac{10^{16} * 10^{17}}{(1.5 * 10^{10})^2}\right)$$

$= 0.757$ V.

* V_{bi} is "important" important when PN junction is forward biased

No

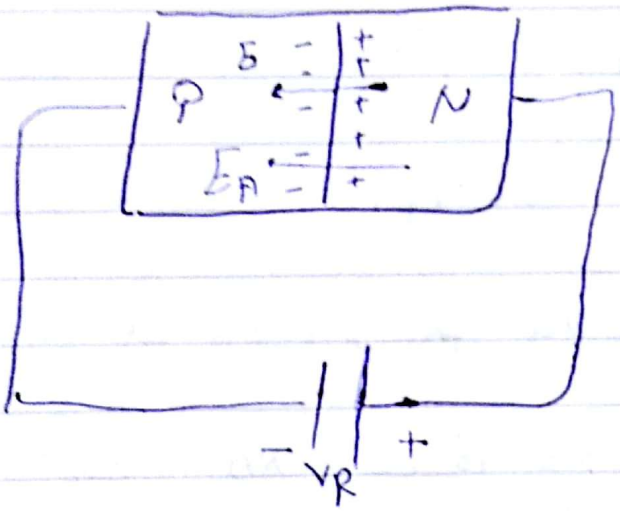
V_{bi} maintains thermal equilibrium

Biasing : Applying power source to PN - junction

1.2.2 Reverse biased PN junction

-ve terminal of source is connected to P-type

+ve " " " " = N-type



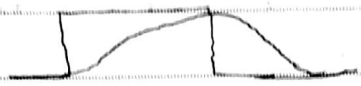
$E_{net} = E + E_A$

V_R (Reverse Voltage) create an electric field (E_A) across the PN junction. E_A and E are in the same Direction $\Rightarrow E_{net} > E \Rightarrow$ force induced by total E (E_{net}) is above thermal equilibrium $\Rightarrow E_{net}$ will keep preventing holes from moving from p to N and electrons from N to P, and no charge across Depletion regions Except for the leakage Current Due to E & E_A which is small $\Rightarrow$ ignorable

No.

Depletion region widens when pn junction is reverse biased. And if $V_R \uparrow$, the width ↑

⊣⊢ PN junction has an interval capacitor C_j that affects the switching capability of the diode



* Application external voltage will affect the capacitor

$$C_j = C_{j0}\left(1 + \frac{V_R}{V_{bi}}\right)^{-1/2}$$

C_{j0} = Capacitor at $V_R = 0$

ex 1.6" Find C_j for pn junction at (a) $V_R = 1V$

(b) $V_R = 5V$

$T = 300K$, $N_a = 10^{16}\ cm^{-3}$, $N_D = 10^{15}\ cm^{-3}$

$n_i = 1.5 \times 10^{10}\ cm^{-3}$ $C_{j0} = 0.5\ pF$

$$V_{bi} = V_T \ln\left(\frac{N_A N_D}{N_i^2}\right) = 26m \ln\left(\frac{10^{16} \times 10^{15}}{(1.5 \times 10^{10})^2}\right)$$

$$= 0.637V$$

a) $$C_j = 0.5 \times 10^{-12}\left(1 + \frac{1}{0.637}\right)^{\frac{-1}{2}}$$

$$= 0.312\ pF$$

b) $$C_j = 0.5 \times 10^{-12}\left(1 + \frac{5}{0.637}\right)^{\frac{-1}{2}} = 0.168\ pF$$

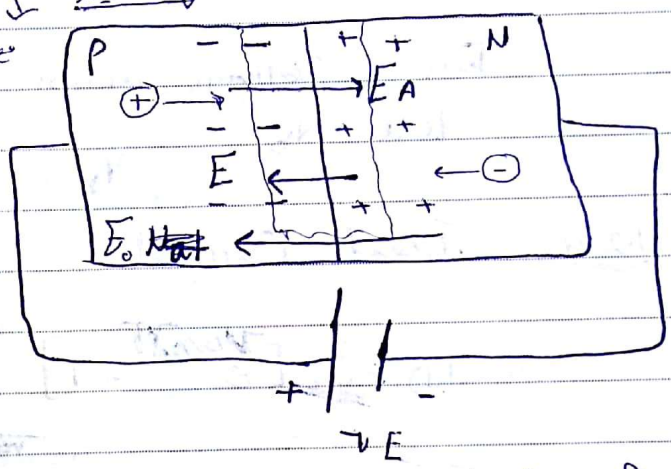
No.

* more V_R ⇒ less capacitor ⇒ V_R ↑ ⇒ width of depltion region ↑ ⇒ distance ~~between~~ between plates ↑ Capacitor ↓ (inversely)
* V_R ↑, E ↑, width ↑, cap ↓
* As V_R increase to acertain high value, E increases, breakdown occurs, creating large reverse current.

1.2.3 ~~Forward~~ Forward biased PN Junction

$E_A < E$

$E_{Ne} < E$ in the direction of E



If PN junction is forward biased, an electric field (E_A) will appear accross the junction due to the voltage source this E_A is less than E with a direction opposite to it.
Not electric field will be smaller than E, with the same direction.
The width of the space charge region will decrease compored to the width of the space charge region when PN junction is unbiased

No.

⇒ force of electric field will be less than force of diffusion gradiant ⇒ electric field can't prevent holes ~~from~~ moving from P to N and electrons from moving from N to P

⇒ this means that the semi-conductor is disturbed in its thermal environment (no thermal equilibrium) ⇒ charge flow, and current I_D moves from P to N

* Current will flow as long as V_F is applied

Forwal Voltage across PN junction V_p is less than V_{bi}

$$V_b < V_{bi}$$

1.2.4 Ideal Current Voltage relation

$$I_D = I_s\left[e^{V_D/\eta V_T} - 1\right] \qquad I_D = I_s\left[e^{V_D/\eta V_T} - 1\right]$$

I_s = reverse Saturation current small, due to electric field $E \Rightarrow$ Drift

if reverse biased, I_s will increase, but remains small, unless PN junction reaches breake down.

→ I_s depends on concentration & cross sectional area of junction

I_s has values between 10^{-18} & 10^{-12} A

For Si,

No.

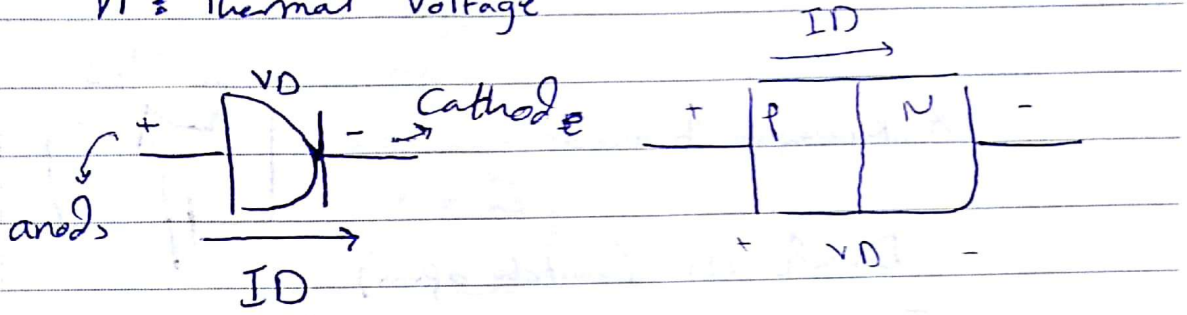
N: ideality factor (emission coefficient)

$1 \le n \le 2$

$n = 1 \rightarrow$ current high

$n = 2 \rightarrow$ ~~flow~~ low

V_T : Thermal Voltage



ex 1.7 $T = 300^\circ K$, $I_S = 10^{-14}$ A, $n = 1$ find I_D

I_D a) if $V_D = 0.7$ V

b) if $V_D = -0.7$ V

a) $I_D = I_S \left[e^{V_D / n V_t} - 1 \right]$

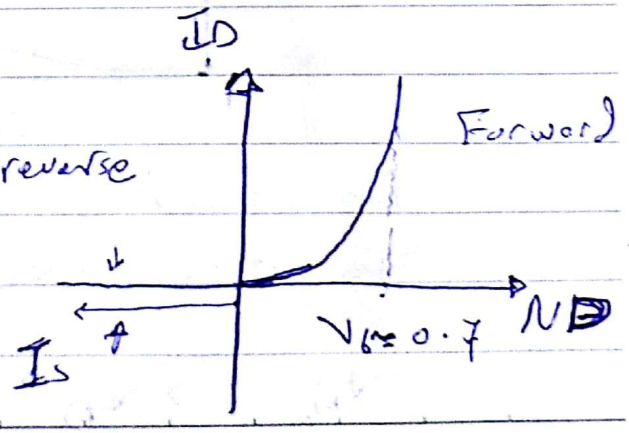
$= 10^{-14} \left[e^{0.7/(1 * 0.026)} - 1 \right] = 4.97$ mA

b) $I_D = 10^{-14} \left[e^{-0.7/(1 * 0.026)} - 1 \right] = -10^{-14}$ A $\simeq I_S$

1.8.5: PN Junction Diode

(cut in V) or (0 A - Voltage) reverse

V_γ : cut in voltage



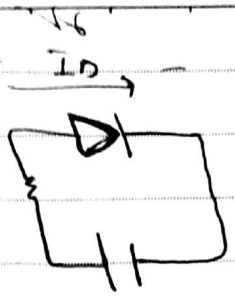
* I/V characteristic curve

* if ND > 0.1

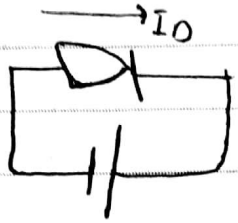
ignore (-1) in eq. $I_D = I_S e^{N_D / n V_T}$

No.

Diode as an Switch:-



* Forward biase
switch closed, dio on
$I_D > 0$ $\bar{I}D = V_\gamma$
Diode short

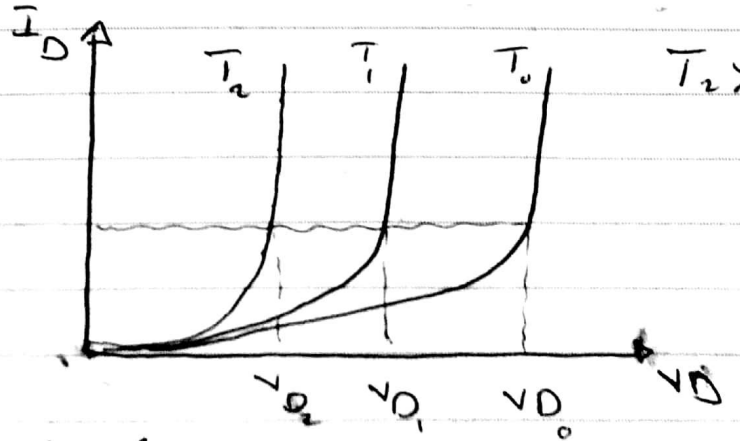


* Reverse biased

Diode off (switch open)
$I_0 = 0$, $VD = V_{oc}$
open cat.

Temporatur effects (on I/P characteristics current)

I_D depends I_s which depends on concentration and n depends on temp.



for a fixed I_0 as temperature increase
$T_0 \rightarrow T_2$, VD decrease

$V_{D_0} \rightarrow V_{D_1}$ $V_{D_2} < V_{D_1} < V_{D_0}$

No.

⇒ for every $5^{\circ}c$, I_s doubles

example $I_{s,0} = 10^{-10}$ $T_0 = 0^{\circ}c$

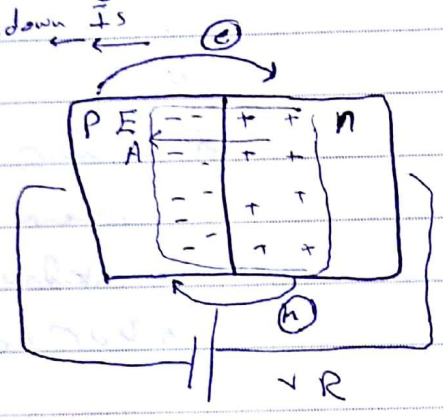
Find I_{s_1} at $T_1 = 15^{\circ}c$ $\frac{15}{5} = 3$

$I_s = I_{s0} * 2^{3}$

in general multiply by 2^{x}

where $x = \frac{T_1 - T_0}{5}$

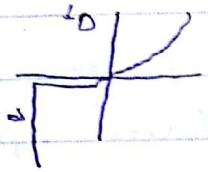
This is a problem for devices using Ge, Since I_s for Ge is around 10^{-6} A $I_{B\,down} \leftarrow I_s$



Break Down Voltage

If V_R is too high, break down occurs V_R v. high

⇒ E_A high



⇒ electrons gain enough energy to break free

⇒ new electron - hole pairs are created

creating large reverse current and the barrier on the PN junction will collapse

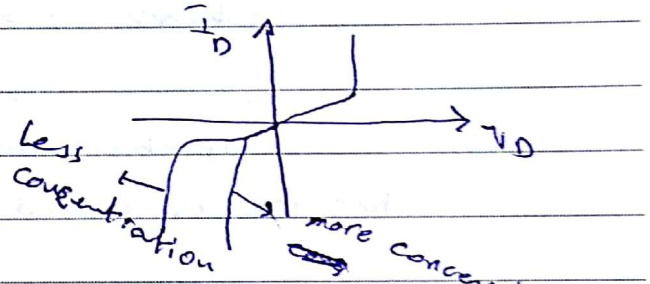
free electrons will collide with other particles causing more electrons and holes to break free

No.

this condition is called avalanche breakdown

* Breakdown Voltage is usuall high at Voltages between 50V - 200V

doping is inversely related to Breakdown Voltage. The higher the concentration the lower the breakdown Voltage



* Zener Breakdown :
when doping is very high So that breakdown occurs at voltages around 5V or less

⇒ Peak Inverse Voltage (PIV) :-
The highest allowed open cut Voltage on diode when it is reverse biased If Breakdown is to be avoided, the PIV should not be exceeded.

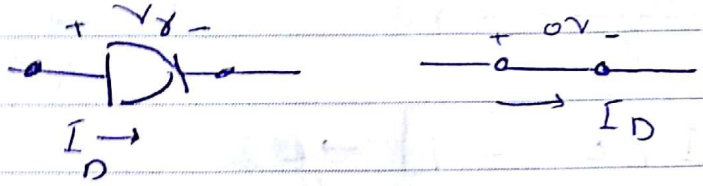
No.

1.3 Diode circuits: DC Analysis and Design:-

Ideal Diode:-

① when Diode is forward biased

$V_\gamma = 0$, $V_f = 0$, closed or shorted $I_D > 0$

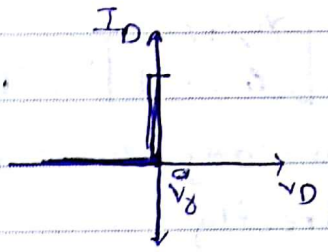


② Reverse Biased:

open ckt — ⊣⊢ — ≡ — / —

$I_D = 0$

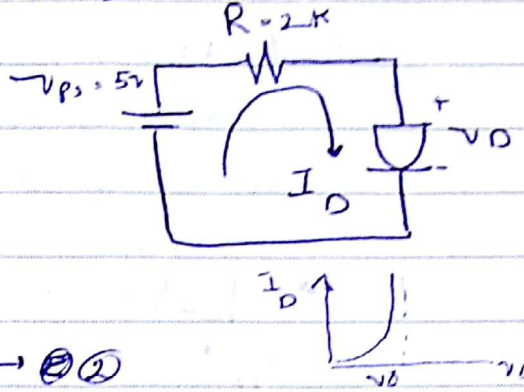
$V_D < 0$



No.

1.3.1 Iteration and Graphical Techniques

① Iteration:- trial and Error



$$V_{ps} = I_D R + V_D$$

$$I_D = \frac{V_{ps} - V_D}{R} \rightarrow ①$$

$$I_D = I_s \left[e^{V_D/\eta V_T} - 1 \right] \rightarrow ②$$

Diode eq^n - nonlinear device eqn exponential relation between V_D & I_D

$$\frac{V_{ps} - V_D}{R} = I_s \left[e^{V_D/\eta V_T} - 1 \right]$$

Solve for V_D

$$\left\{ V_{ps} = R I_s \left[e^{V_D/\eta V_T} - 1 \right] + V_D \right\} \Longrightarrow ③$$

⇒ this equation ③ has only one unknown, but can't be solved directly

⇒ use trial and error of eq ③

Try : V_D	P_s
0.6	2.7V ≠ 5V
0.65	15.1V ≠ 5V
⋮	
0.619	4.99V ≈ 5V

use eq ① or ② to find I_D

$$I_D = \frac{5 - 0.619}{2k} = 2.19\ mA$$

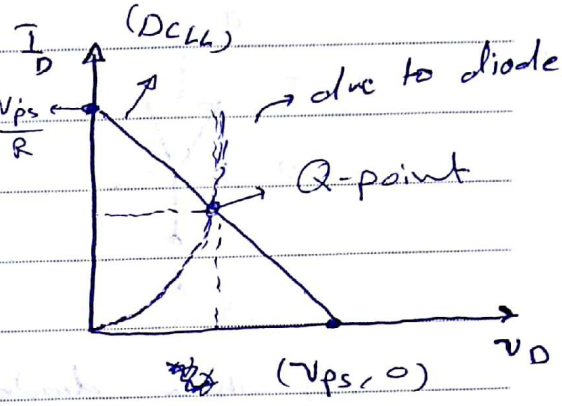
No.

(2) Graphical Analysis :-

$I_D = \frac{V_{PS}}{R} - \frac{V_D}{R}$ DC Load Line (DCLL) depends on R (linear Device)

* at $I_D = 0$ $\quad \frac{V_{PS}}{R} - \frac{V_D}{R} = 0 \Rightarrow V_{PS} = V_D$

* at $V_D = 0$ $\quad I_D = \frac{V_{PS}}{R}$



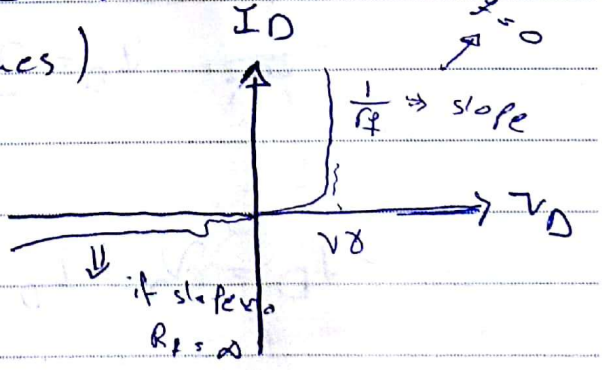
⇒ Q-Point :- when DCLL and I/V Diod curve intersect
Also called operation point because it is the point at which Diode operates
In our example Q-point is at $I_D = 2.19$ mA, $V_D = 0.62$ mV

* slope of DCLL :- $\quad$ slope $= \frac{\partial I_D}{\partial V_D} = \frac{-1}{R}$

$\frac{\Delta I_D}{\Delta V_D} = \frac{0 - V_{PS}/R}{V_{PS} - 0} = \frac{-1}{R}$

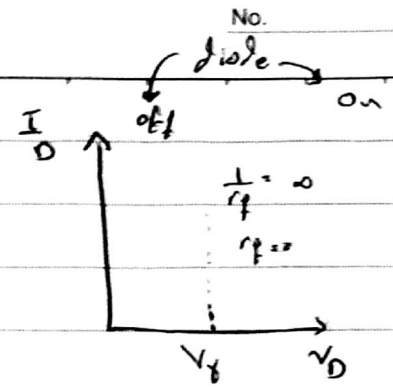
if vertical slope $\infty \Rightarrow R = 0$

12.2 Piecewise Linear Model :-
(segment of straight lines)

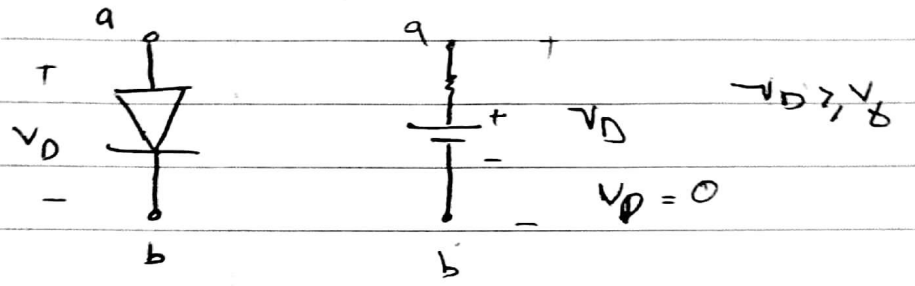


V_f : Cut in (on voltage)

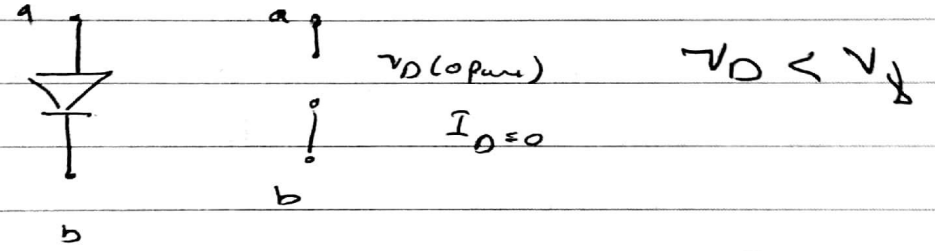
r_f : forward Resister R_f



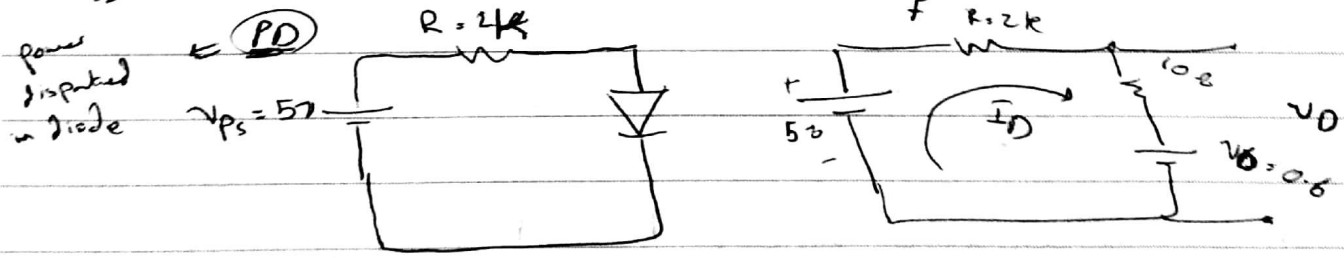
⇒ when diode is forward active :- (Diode ON)



⇒ when diode is reverse biased :- (Diode off)



Ex: Find I_D, V_D, $V_\gamma = 0.6$, $r_f = 10\,\Omega$



$$I_D = \frac{V_{PS} - V_\gamma}{r_f + R} = \frac{5 - 0.6}{10 + 2k} = 2.19\ mA$$

$$V_D = V_\gamma + I_D r_f = 0.6 + 2.19m \times (10)$$
$$= 0.622\ V$$

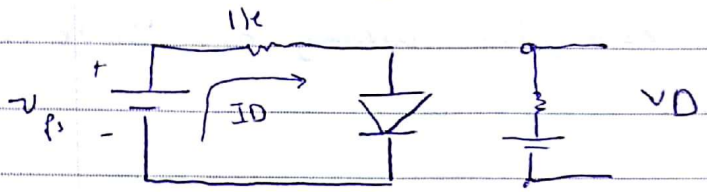
$$PD = I_D V_D = 0.622 \times 2.19m = 1.36m\ W$$

Note: If I_D → +ve → Diode ON
→ -ve → Diode ~~off~~

No.

Problems:-

(Q.) Find V_D, I_D and P_D for the following ckt



a) $V_{ps} = 5\,V$, $V_\gamma = 0.6\,V$

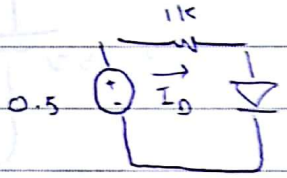
$$I_D = \frac{V_{ps} - V_\gamma}{1k} = \frac{5 - 0.6}{1k} = 4.4\,mA$$

$V_D = V_\gamma = 0.6\,V$

$P_D = I_D * V_D = 0.6 * 4.4\,m = 2.64\,mW$

(b) $V_f = 0.6$, $r_f = 20\,\Omega$, $V_{ps} = 5\,V$

c) $V_f = 0.6$, $V_{ps} = 0.5\,V$

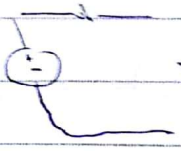


$$I_D = \frac{V_D - V_f}{1k} = \frac{0.5 - 0.6}{1k} = -0.1\,m$$

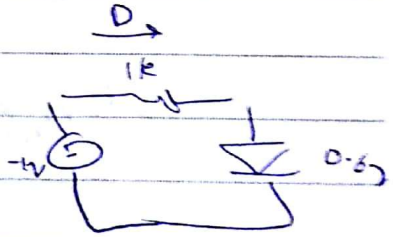
$I_D \ominus V_f \Rightarrow$ Diode off $\Rightarrow I_D = 0$

V_D (open ckt) = ~~5~~ 0.5 V

$P_D = 0\,W$



D)



$V_f = 0.6$ $V_{ps} = -1\,V$

⇒ Diode off

$I = 0$ $V_D = -1$

$P_D = 0$.

[illegible]

Q.5 No.

[illegible]

① ⇒ One way to test diode assume Diode on, find I_D

If I_D +ve ⇒ assumption correct and Diode on.

⇒ if I_D -ve ⇒ assumption wrong and Diode is off $I_D = 0$

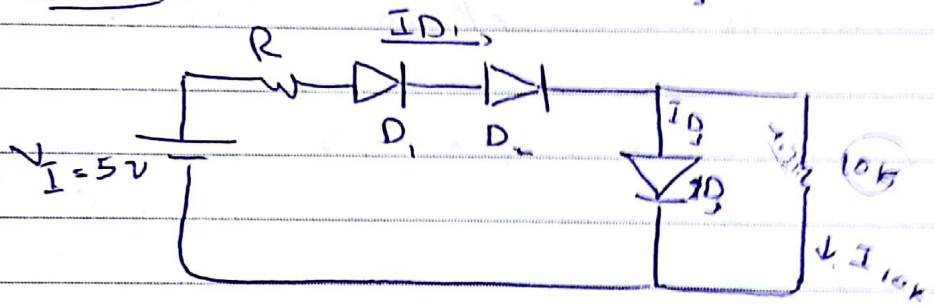
② another way: assume Diode off

find V_{open}:

if $V > V_\gamma$ ⇒ Diode is on $V_D = V_\gamma$

if $V < V_\gamma$ ⇒ Diode is off and $V_D = V_{open}$

ex $I_{D_1} = 2I_{D_2}$ - find R_1, I_{D_1}, I_{D_2} $V_\gamma = 0.65$ V



$I_{D_1} = I_{D_2} + I_{10k} = 2I_{D_2}$

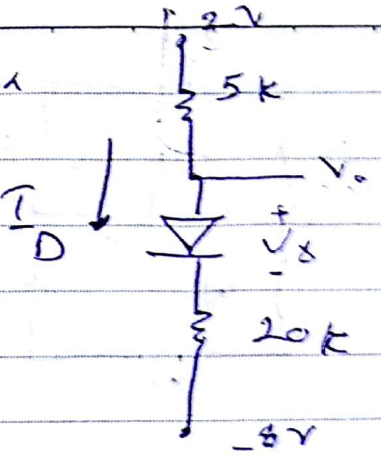
$I_{10k} = I_{D_2} = \frac{V_\gamma}{10k} = 0.065\,mA$

$I_{D_1} = 2I_{D_2} = 2(0.065) = 0.13\,mA$

$I_{D_1} = \frac{V_I - 7V_0}{R_1} \Rightarrow R_1 = \frac{5 - 7(0.65)}{0.13\,m} = 23.46\,k\Omega$

No.

ex



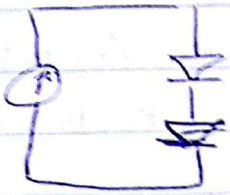
find I_D, V_o, $V_\gamma = 0.6V$

$$I_D = \frac{2 - \gamma - 0.6}{25k} = 0.376 mA$$

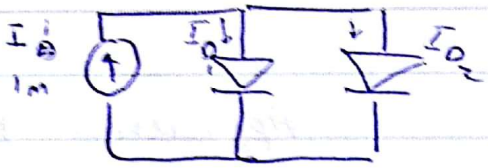
$$V_o = 2 - 0.376m\,(5k)$$
$$= 0.12\,V$$

Find I_{D_1}, I_{D_2}, V_{D_1}, V_{D_2} if $I_{S_1} = 5 * 10^{-14}$ A
$I_{S_2} = 5 * 10^{-7}$ A

(a)



b)



$I_i = I_{D_1} + I_{D_2} = 1m$

$V_{D_1} = V_{D_2} = V_D$

متساويان

$$\frac{I_{D_1}}{I_{D_2}} = \frac{I_{S_1}(e^{V_D/V_t} - 1)}{I_{S_2}(e^{V_D/V_t} - 1)}$$

$$1m = \frac{I_{S_1}}{I_{S_2}} I_{D_2} + I_{D_2}$$

$I_{D_2} = 0.897\,m$

$I_{D_1} = 0.0897\,m$

$$I_{D_1} = I_{S_1}(e^{V_D/V_t} - 1) \qquad V_D = 0.3397$$

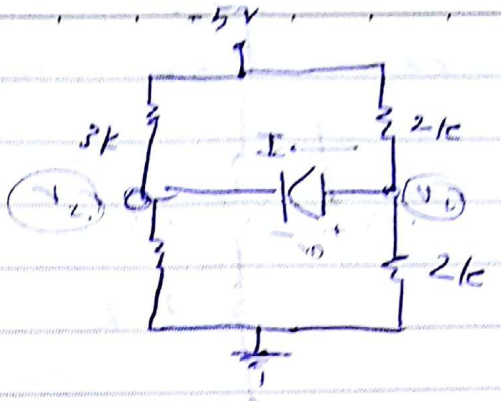
$I_{D_2} = I_{S_2}$

No.

Ex: Find I_D and V_D if

a) $V_\gamma = 0.6$

b) $V_\gamma = 0.7$



at V_1

(1) $\frac{V_1 - 5}{2k} + I_D + \frac{V_1}{2} = 0$

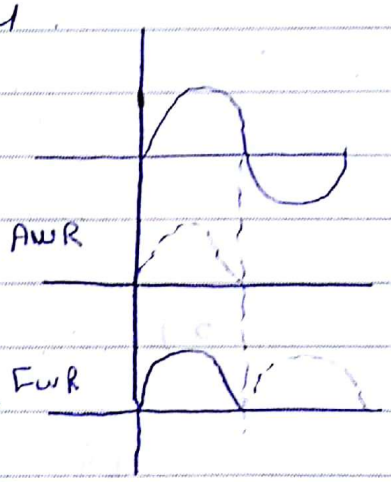
(2) $\frac{V_2 - 5}{3k} - I_D + \frac{V_2}{2k} = 0$

(3) $V_1 - V_2 = V_\gamma$

Ch 2 :- Rectifier ckt :-

Rectifier ckt is the first step in converting an ac signal to a Dc signal.

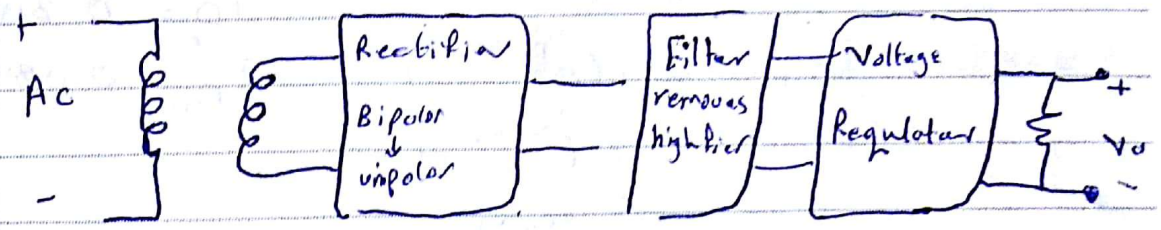
* Rectifier converts a bipolar signal into a unipolar one



Application :- Power Supply, Transformer, wave shaping ckt ...

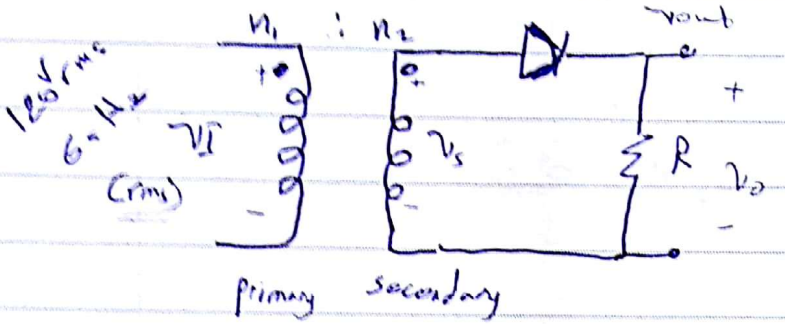
~~[redacted] used~~

Dc power Supply :-



No.

Half-wave Rectifier (HWR)



N_1, N_2 : number of windings for primary & secondary respectively

$\frac{N_1}{N_2} = \frac{V_I}{V_s}$ $\frac{N_1}{N_2}$: turn ratio

for $V_s < V_I$ N_1 must be less than N_2

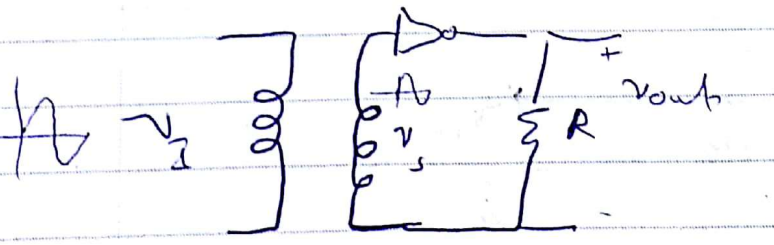
(RMS) Root mean square $\sqrt{\frac{ac^2 + dc^2}{2}}$ / $\sqrt{\frac{Vp^2}{2}}$

$V_{rms} = \frac{Vp}{\sqrt{2}}$ for sine wave

N_s is in peak value where V_1 is added to an subtracted from it

Voltage Transfer characteristics (VTS)

VTC = V_{in} V_s V_{out}



No.

Test Diode state by removing diode and Calculate V (open ckt)

o (open)

$$-V_s + V + I_f R = 0$$

$$V_s = V$$

① $V > V_\gamma$ Diode on (Forward)

$V_s > V_\gamma$, $V_{out} = V_s - V_\gamma$

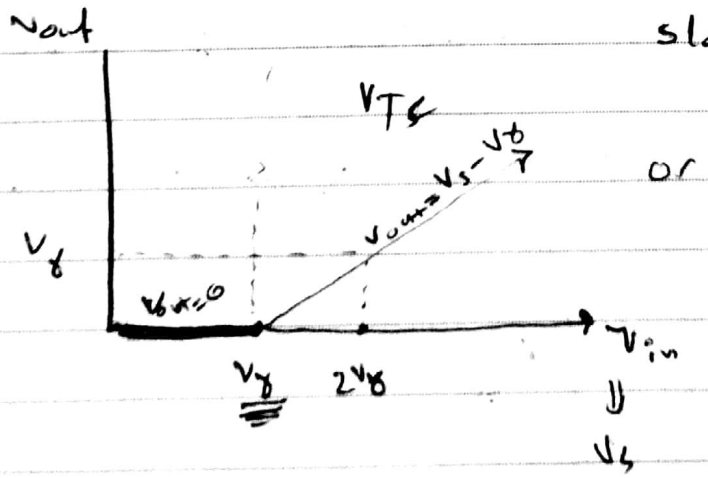
$$V_{out} = i_D R = i_D R$$

$$i_D = \frac{V_{out}}{R} = \frac{V_s - V_\gamma}{R}$$

if $i_D = 0$, $V_D = V_\gamma$

② if $V_s \le V_\gamma$ Diode off (reverse)

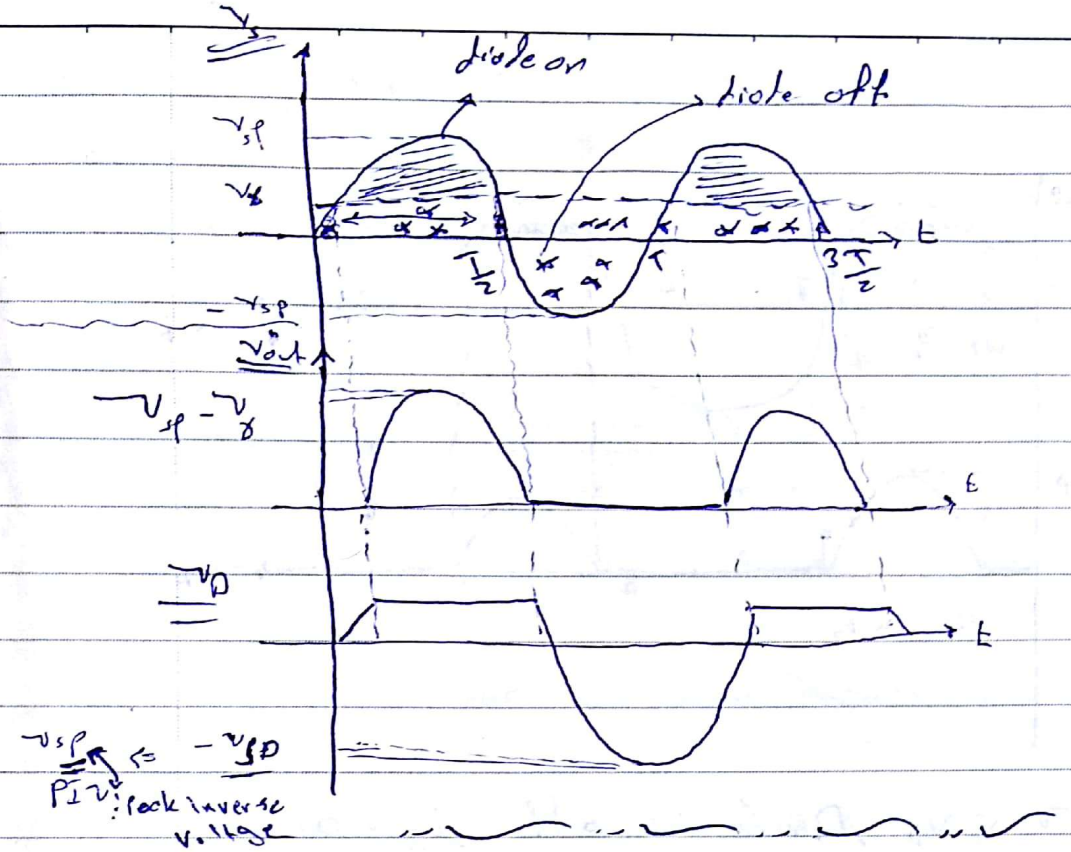
$$i_D = 0, \quad V_{out} = 0 \quad V_D = V_s$$



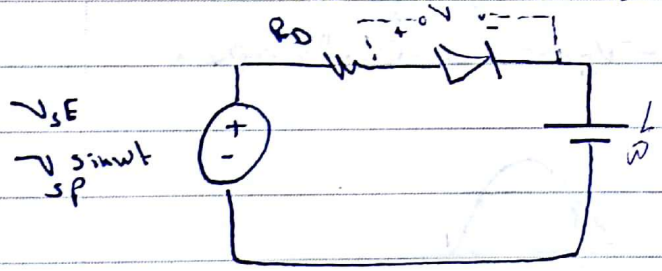
$$\text{slope} = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{V_\gamma - 0}{2V_\gamma - V_\gamma} = 1$$

$$\text{or slope} = \frac{\partial V_{out}}{\partial V_{in}} = 1$$

No.



Diode Rectifier as a battery charger



$\Rightarrow V > V_\gamma$, Diode ON.

$V = V_s - V_B$ $\quad V_s - V_B > V_\gamma \Rightarrow V_s > V_B + V_\gamma$

range between ωt_1 & ωt_2 is when battery charging

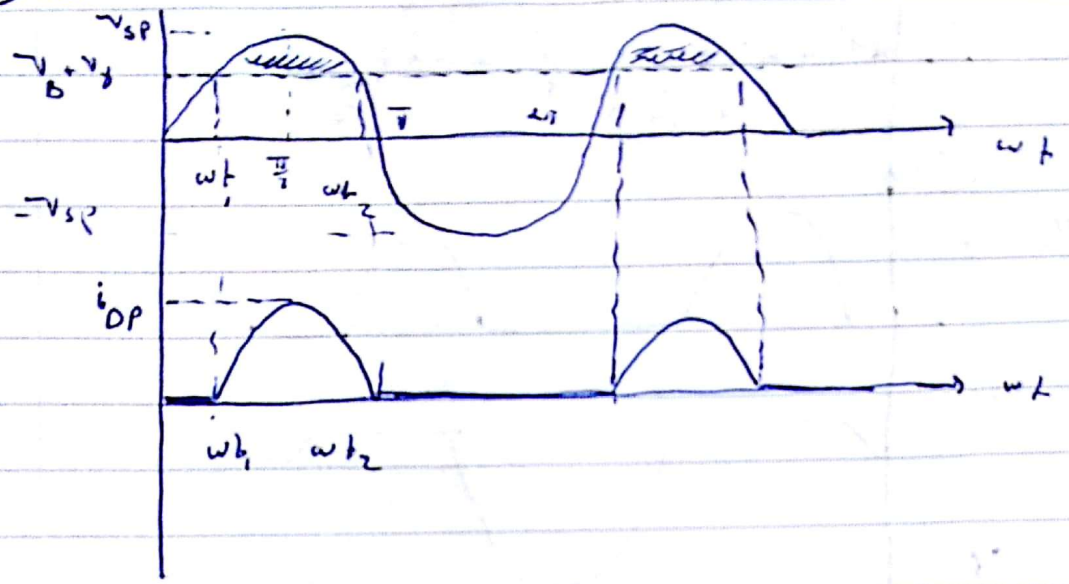
$I_D > 0$.

$$i_D = \frac{V_s - V_\gamma - V_B}{R}$$

$$i_{DP} = \frac{V_{sp} - V_\gamma - V_B}{R}$$

No.

I_D : DC
i_D : Ac signal



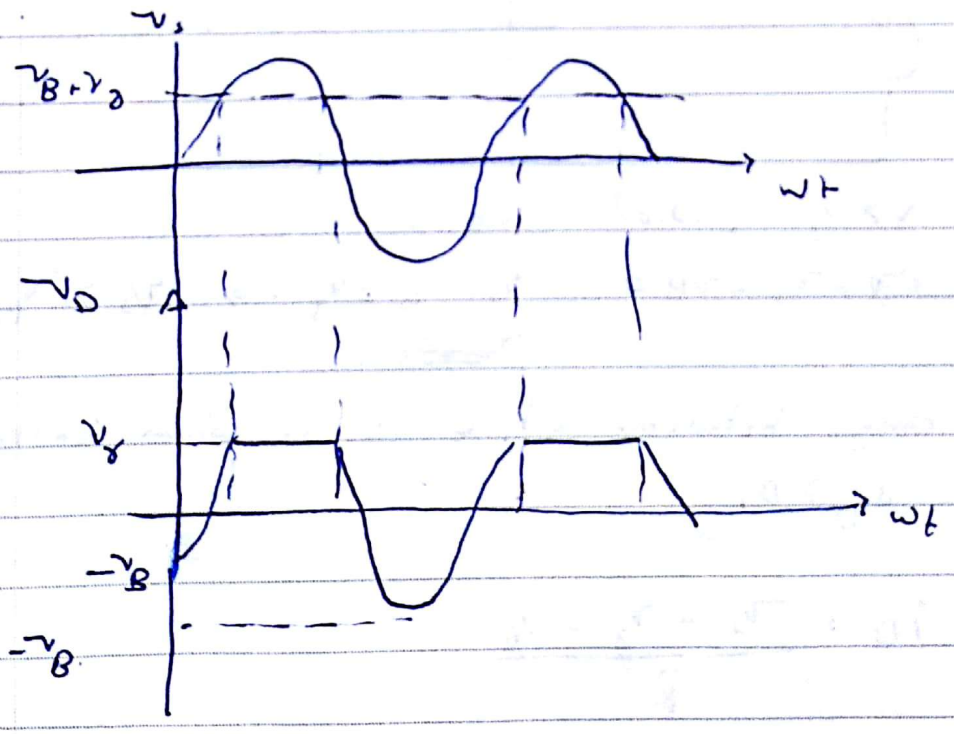
** $v < v_\gamma$, Diode is off , $i_D = 0$

⇒ Battary Doesn't charge

PIV $v = v_s - v_B$ ⇒ Diod open

Peak value at $-v_{sp}$

$v_o = -v_{sp} - v_B$



$PIV = v_{sp} + v_B$

No.

Ex 2.1 $V_B = 12\,V$, $R = 100\,\Omega$, $V_\gamma = 0.6\,V$ $V_s(t) = 24.8 \sin \omega t$

a) find peak diod current

b) Max reverse ~~bais~~ bias diode voltage. (PIV)

c) fraction of the cycle over which diode is conducting

a) $i_{D_f} = \dfrac{V_{sp} - V_\gamma - V_B}{R} = \dfrac{24 - 0.6 - 12}{100} = 112\,mA$

b) $PIV = V_{sp} + V_B = 24 + 12 = 36\,V$

c) Diode turns on when ~~$V_s(wt) = V_B + V_\gamma$~~

$V_s(t) = V_B + V_\gamma$

$24 \sin(\omega t) = 12 + 0.6 = 12.6$

$\omega t = \sin^{-1}\left(\frac{12.1}{24}\right) = 31.7^\circ$

Due to symmetry $\omega t_2 = 180 - \omega t_1$

$= 180 - 31.7 = 148.3^\circ$

the fraction when diode conducts:

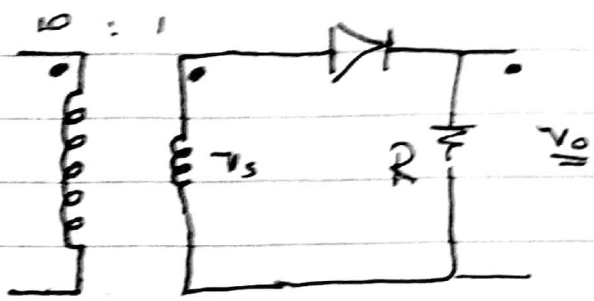
$\dfrac{\omega t_2 - \omega t_1}{360} * 100\% = 32.4\%$

ωt is only 32.4 of a full cycle when diode Conducts. $\Rightarrow$ inefficient

$I_{D(Avg)} = \frac{I_{DP}}{\pi}$

No.

P.2.3



$V_\gamma = 0.7$

a) find peak output voltage

b) " : diod current

c) " fraction of diod conductance

d) avarge diode current

a) Voltpeakpeak, $V_{sp} - V_\gamma$

$\frac{N_1}{N_2} = \frac{10}{1} = \frac{V_1}{V_s} \Rightarrow V_{s_{rms}} = 12_{rms} \Rightarrow V_{sp} = 12 \times \sqrt{2}$

$= 16.27\ V$

$V_{DP} = V_{sp} - V_\gamma$

$= 16.97 - 0.7$

$= 16.27\ V$

b) $I_{DP} = \frac{V_{DP}}{R} = \frac{16.27}{2k} = 8.13\ mA$

c) fraction when diode conducts $V_s = V_\gamma$

$16.97 \sin \omega t_1 = 0.7$

$\omega t_1 = \sin^{-1}\left(\frac{0.7}{16.97}\right) = 2.36°$

$\omega t_2 = 180 - 2.36 = 175.23$

$\text{fraction} = \frac{\omega t_2 - \omega t_1}{360} \times 100\% = 48.88\%$

d) $I_{D(Avg)} = \frac{I_{DP}}{\pi} = \frac{8.13\ m}{\pi} = 2.59\ mA$

e) $PIV = V_{sp} = 16.97\ V$

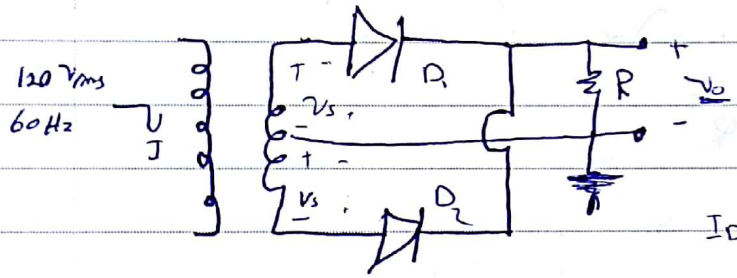
No.

2.1.2 Full wave rectifier

the full wave rectifier converts the -ve portion of the sine wave into a positive one

(FWR) (TFLR)
① center tapped full wave Rectifier
② Bridge Rectifier

* Center tapped Full wave rectifier :-



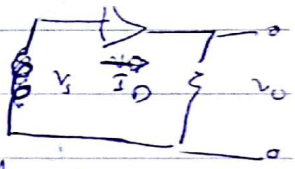
$I_{D_1} = \frac{V_{out}}{R} = \frac{V_s - V_\gamma}{R}$

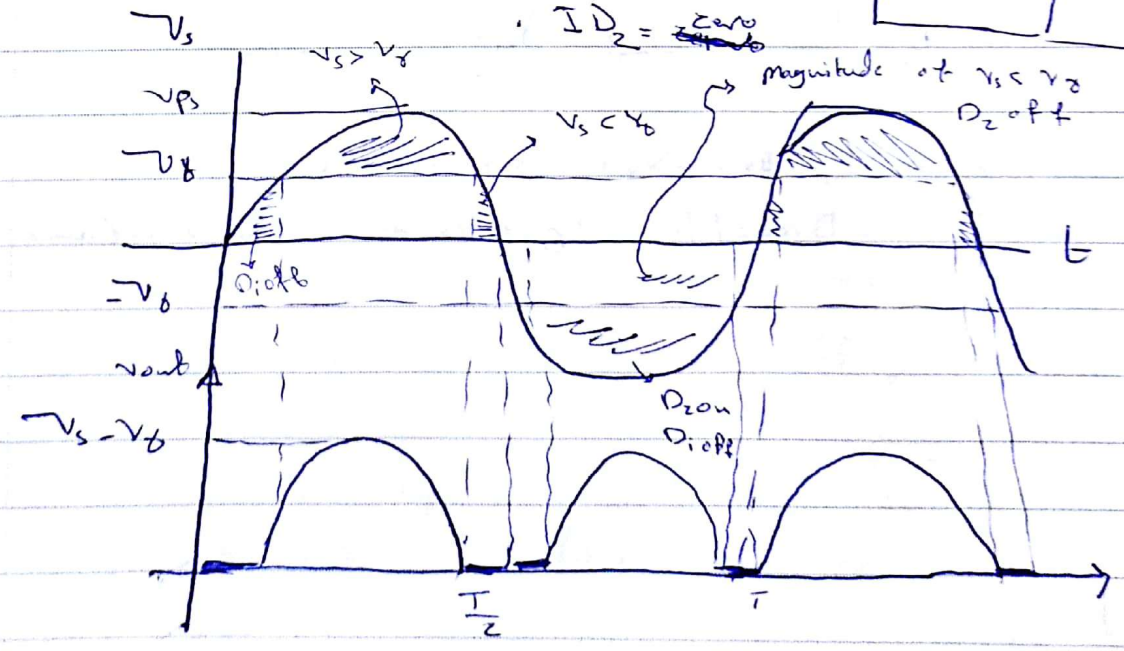
$\Rightarrow V_{out} = V_s - V_\gamma$

* ⊕ve half cycle : D_2 is off

$\Rightarrow$ if $V_s > V_\gamma \Rightarrow$ D_1 is on

$I_{D_2} =$ zero





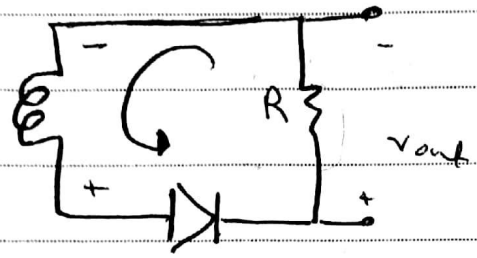
$\Rightarrow$ if $V_s < V_\gamma$, D_1 is off $I_D = 0$ $V_{out} = I_{D_1} R = 0$

No.

(-ve) half cycle (D_1 is off)

(a) ⇒ if $v_s < v_\gamma$ / $-v_s > v_\gamma$ ⇒ magnitude of $v_s > v_\gamma$

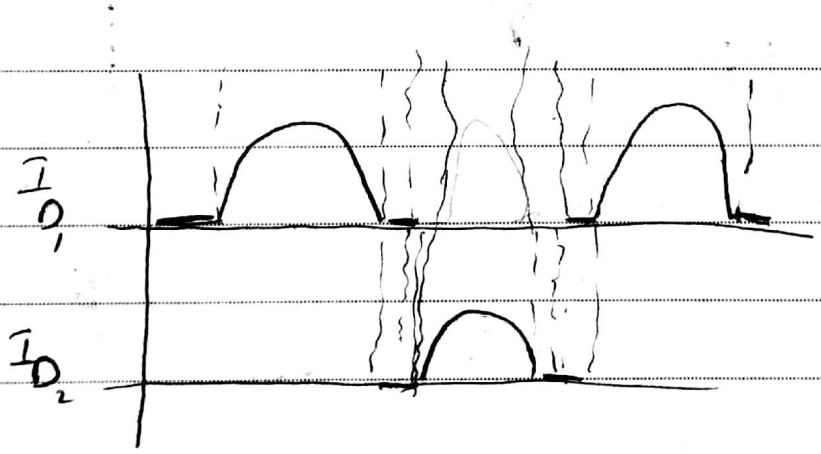
D_2 is on



$-v_s + v_\gamma + v_{out} = 0$ $\quad I_{D_1} = 0$

$v_{out} = v_s - v_\gamma$

$I_{D_2} = \frac{v_{out}}{R}$

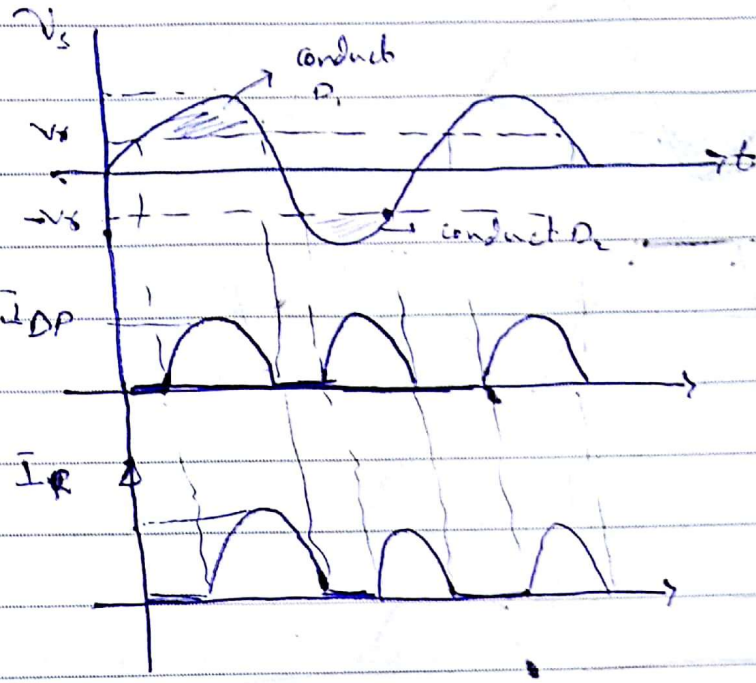


(b) ⇒ if $v_s > -v_\gamma$ ⇒ $-v_s > v_\gamma$

D_2 ⇒ off $\quad I_{D_2}$ = zero $\quad$ hence = Zero

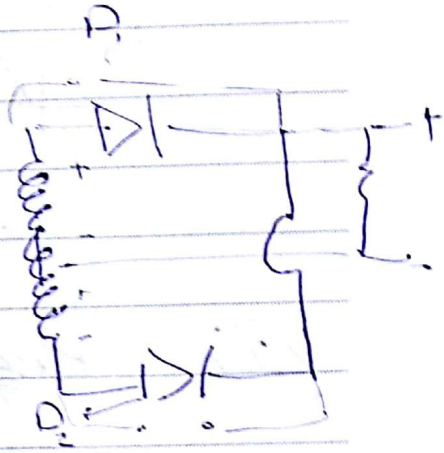
No.

Currents : I_{D_1}, I_{D_2}, I_R



$$i_{D_1(Avg)} = i_{D_2(Avg)} = \frac{i_{DP}}{\pi}$$

$$i_{R(avg)} = \frac{i_{RP(2)}}{\pi}$$



PIV ⇒ PIV for Both is the same +ve half cycle

D_1 on, D_2 off

$$-2V_s + V_\gamma - V_2 = 0$$

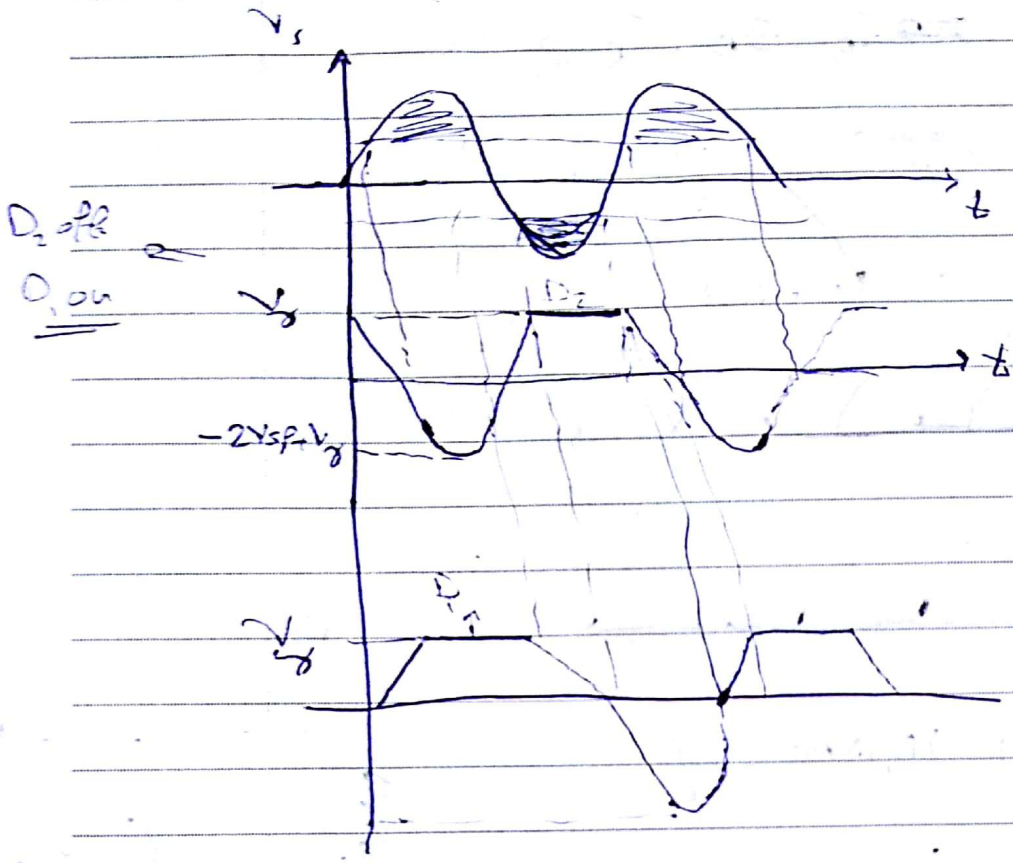
$$V_2 = -(-2V_s + V_\gamma) \Rightarrow \boxed{V_2 = 2V_s - V_\gamma}$$

PIV

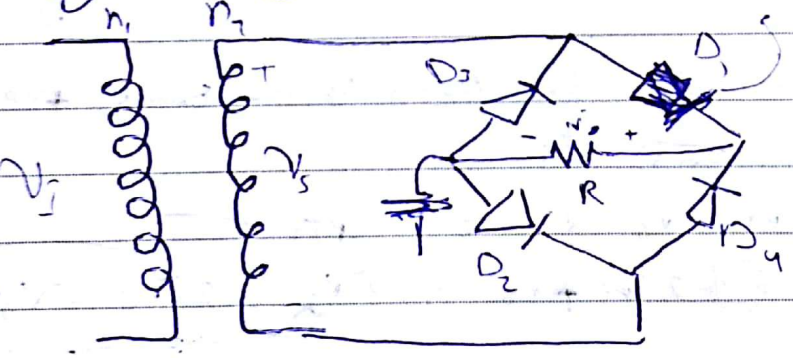
+ -ve half cycle ⇒ D_1 off, D_2 on

$$2V_s + V_1 - V_\gamma = 0$$

$$V_1 = (V_\gamma - 2V_s) \Rightarrow PIV = 2V_s - V_\gamma$$



(2) Bridge Rectifier



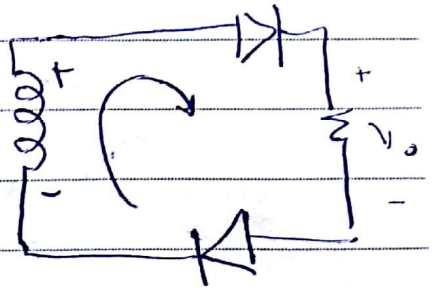
* +ve half cycle :- $V_s > V_\gamma$

$V_s > 0$

D_1, D_2 on

D_3, D_4 off

Consider ideal diodes

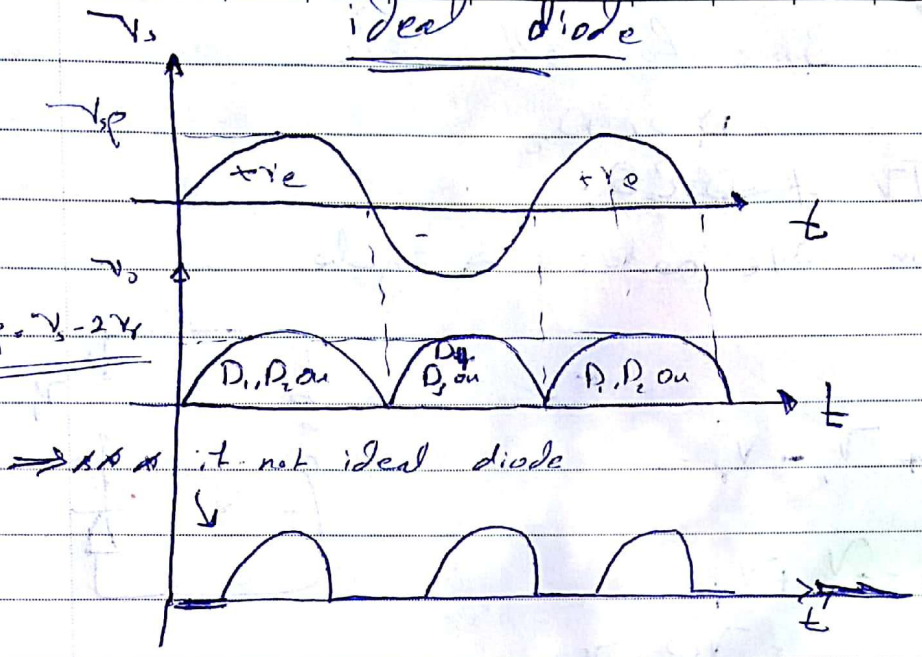


$-V_s + 2V_\gamma + V_o = 0$

$V_o = V_s - 2V_\gamma = V_s$ for ideal

No.

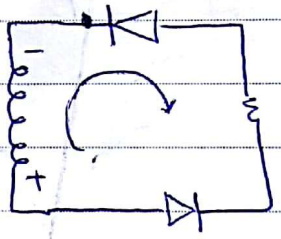
ideal diode



-ve half cycle:-

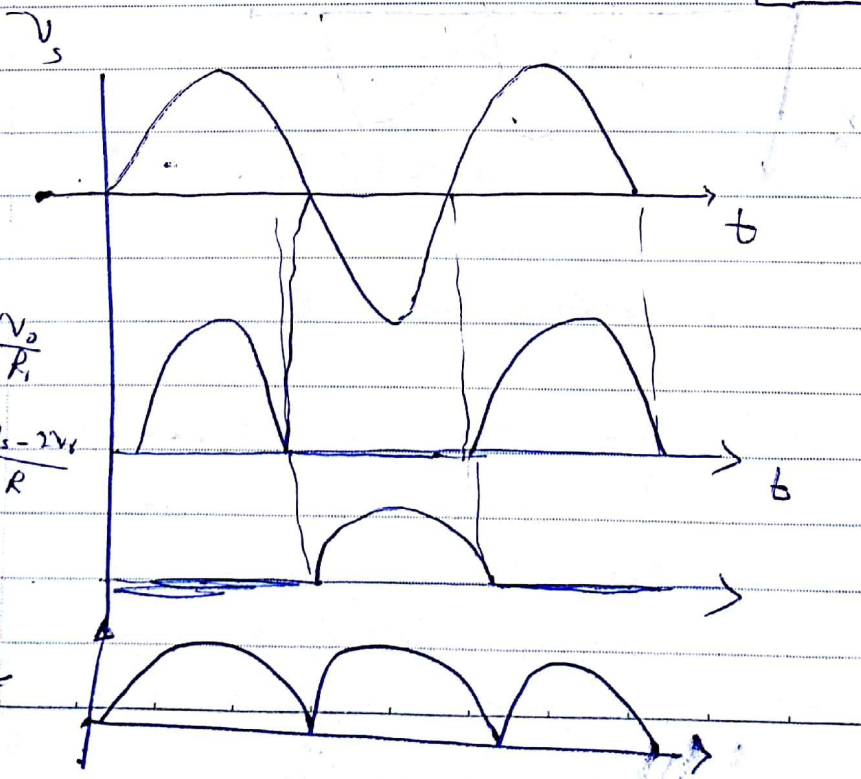
$V_s < V_\gamma$ D_1, D_2 off

$V_s < 0$ D_3, D_4 on



$+V_s - 2V_\gamma - V_o = 0$

$V_o = V_s - 2V_\gamma$



Prac 2.14 { Negative Output rectification }

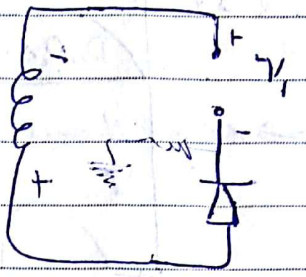
No.

PIV :- Same for all diode

D_1 or D_2

PIV at ~~D_1~~ D_2

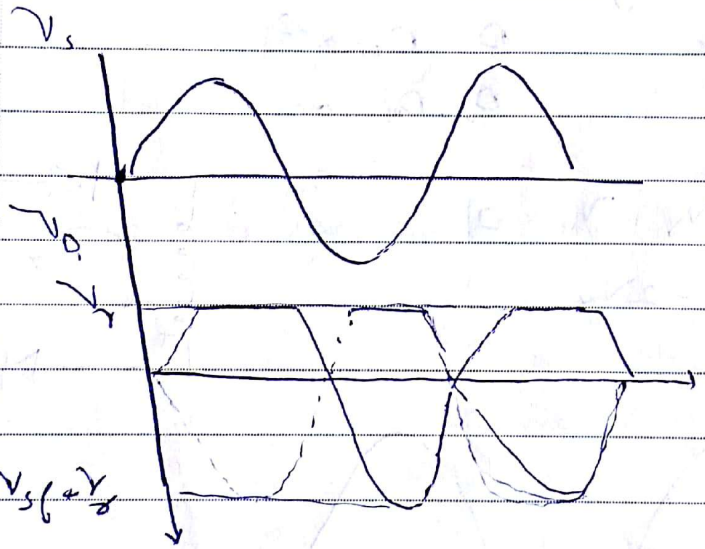
in -Ve half cycle



$V_s + V_1 + V_\gamma = 0$

$V_1 = -V_s + V_\gamma$

at PIV $= V_{sp} - V_\gamma$



No.

Example 2.2 Compare Voltage (V_s, PIV) and transformer turn ratio $\left(\frac{N_1}{N_2}\right)$ between CT, FWR & Bridge.

$V_I = 120\ V_{rms}$, 60Hz $V_o = 9\ V_p$ $V_\gamma = 0.7\ V$

⇒ CT $V_o = V_s - V_\gamma$

$V_s = V_o + V_\gamma$

$V_{sp} = V_{op} + V_\gamma = 9 + 0.7 = 9.7V$

$V_{rms} = \frac{V_{sp}}{\sqrt{2}} = \frac{9.7}{\sqrt{2}} = 6.86\ V_{rms}$

$\Rightarrow \frac{N_1}{N_2} = \frac{V_I}{V_s} = \frac{120}{6.86} = 17.5$

$PIV = 2V_{sp} - V_\gamma = 2 \times (9.7) - 0.7 = 18.7\ V$

* Brige

$V_o = V_s - 2V_\gamma$

$V_s = V_o + 2V_\gamma$

$V_{sp} = V_{op} + 2V_\gamma = 9 + 2 \times 0.7 = 10.4$

$V_{sp_{rms}} = \frac{10.4}{\sqrt{2}} = 7.35\ V$

$\frac{N_1}{N_2} = \frac{V_I}{V_{sp}} = \frac{120}{7.35} = 16.3$

$PIV = V_{sp} - V_\gamma = 10.4 - 0.7 = 9.7$

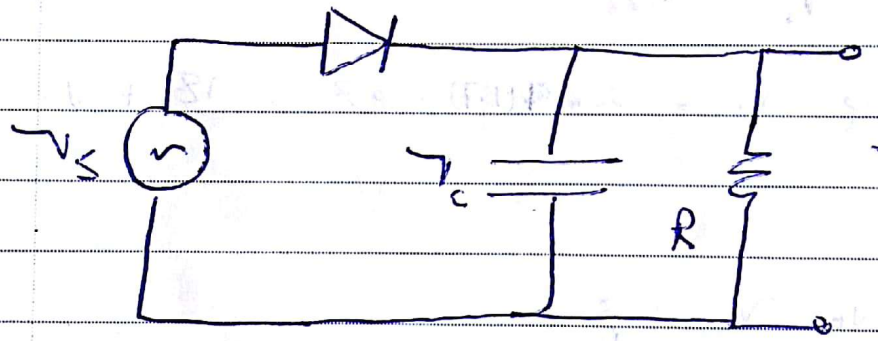
No.

* CT utilizes only half of the Secondary windings at each half cycle, but the ~~bride~~ bridge utilizes all windings. This is a waste for CT, since turn ~~ratios~~ ratios are almost the same

* PIV for CT is almost twice the ~~PIV~~ PIV of Bridge ⇒ diode in CT need to sustain more voltage on diode when it is open

2.1.3 Filter

Consider a half wave rectifier (Same principle for Full)



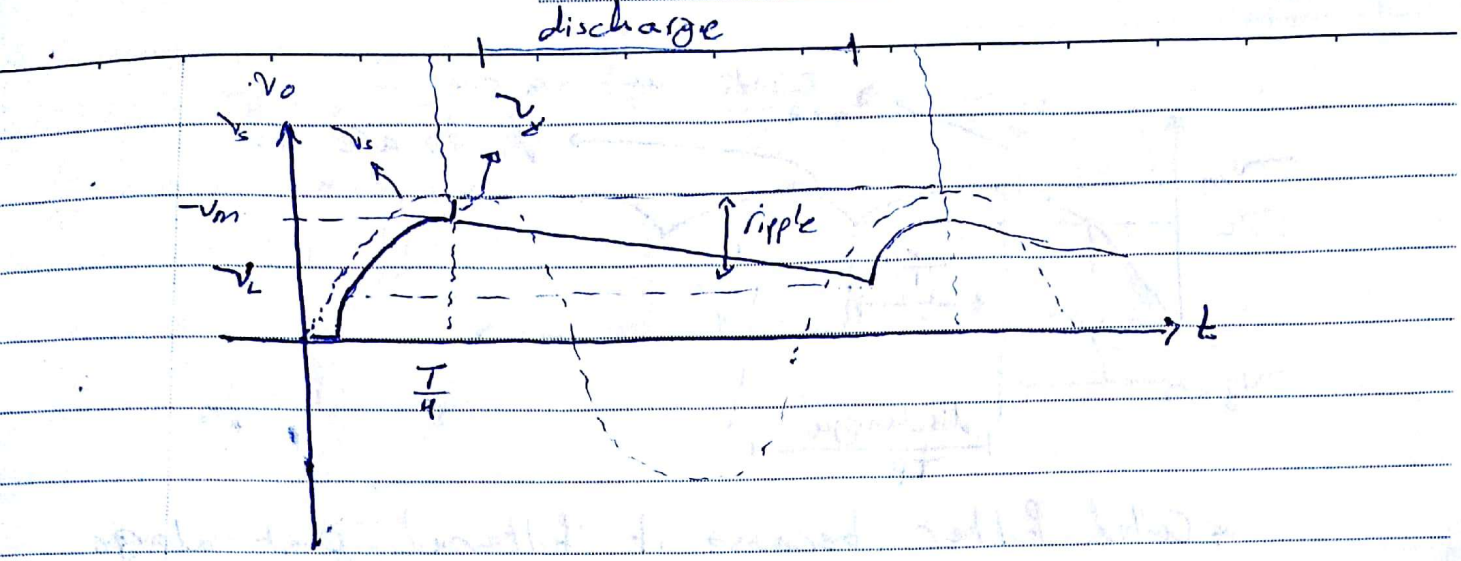
① ~~Fast~~ at $T < \frac{T}{4}$, diode will be on, & capacitor will charge through rf $Z = rf * C \Rightarrow$ very small

⇒ Output signal will keep with input signal

in other words there will be on delay

$V_o = V_c = V_s - V_\gamma$

No.



$t > \frac{T}{4}$

(2) V_s starts to decrease & V_o will decrease & capacitor will discharge through R

$\tau_{disch} = RC \Rightarrow$ high, $R >> r_f$, $\therefore \tau_{disch} >> \tau_{ch}$

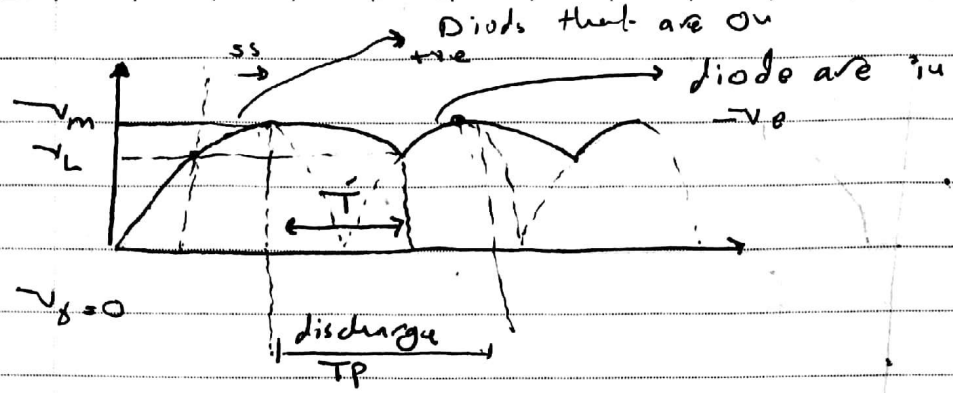
which causes delay between input and output signal

At some point V_o will be less than V_s and diode will turn off.

Capacitor will continue discharging slowly, until the next +ve half cycle V_s & V_s becomes higher than $-V_o$ again $\Rightarrow$ Diode will be on again an Capacitor will charge, and so on.

$V_{ripple} = V_m - V_L$

No.



* Called filter because it filtered out alarge portion of the sinewave
* or because it filtered out the high freq

⇒ During Discharging $v_o(t) = V_m e^{-t/2}$

$= V_m e^{-t/RC}$

$V_r = V_m - V_L$

$= V_m - V_m e^{-T'/RC}$

$= V_m (1 - e^{-T/RC})$

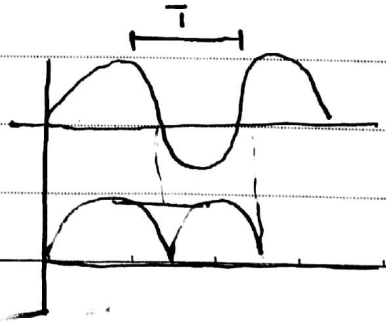
$e^{-T/RC} = 1 - \frac{T'}{RC}$, $RC >> T'$

$V_r = V_m (1 - 1 + \frac{T'}{RC}) = V_m (\frac{T'}{RC})$

* for small ripple (ideal) $T' = T_p$

$V_r = V_m (\frac{T_p}{RC})$

* For ~~FW~~ FWR :-

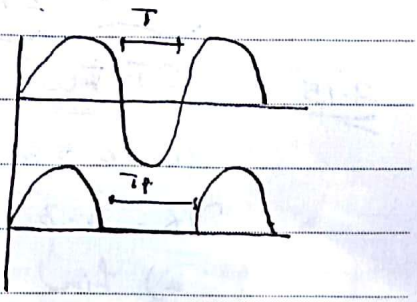


$T_p = \frac{T}{2}$

No.

$$V_r = V_m \frac{T}{2RC} = \frac{V_m}{2RCf}$$

* for HWR

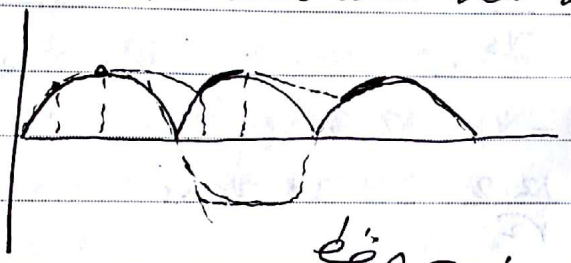


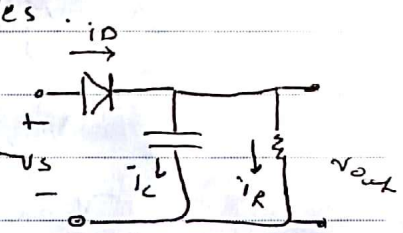
$$T = T_f = \frac{1}{f}$$

$$V_r = \frac{V_m}{RCf}$$

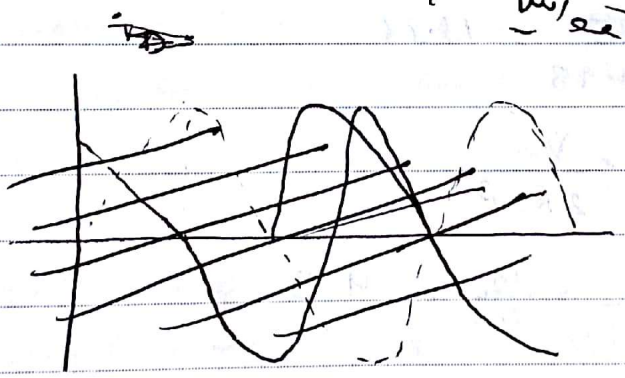
Diode Behavior and i_D :-

consider full wave with ideal diodes.





dep wise



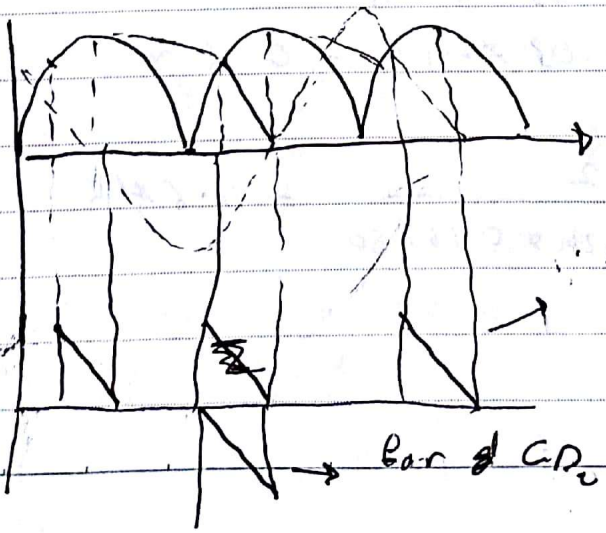
$$i_D = i_c + I_R$$

$$= C\frac{d v_{out}}{dt} + \frac{V_o}{R}$$

$$i_{D,Peak} = \frac{V_m}{R}\left(1 + \pi\sqrt{\frac{2V_m}{V_r}}\right)$$

Δt : Conduction time

$$i_{D Avg} = \frac{V_m}{R}\left(1 + \frac{\pi}{2}\sqrt{\frac{2V_m}{V_r}}\right)\frac{\Delta t}{T}$$



current of diode on +ve HC

for C_D Diode qu in −ve HC

No.

قانون التفاضل

$$\Delta t = \frac{1}{2\pi f}\sqrt{\frac{2V_r}{V_m}}$$

2.15 CT FWR, $V_o = 12 V_p = V_m$

$i_L = 0.5\,A$ $\quad V_r = 3\%$ of V_m $\quad \omega = 2\pi f$

$V_\gamma = 0.8$, $V_I = 120\sqrt{2}\left[2\pi(60)t\right] V$

a) find transforms ratio

b) min value of C

c) in peak, in avg, PIV

قانون

a) $\frac{N_1}{N_2} = \frac{V_I}{V_s}$

$V_s = V_p + V_\gamma = 12.8\, V_p$

$V_{s\,rms} = \frac{12.8}{\sqrt{2}} = 8.98\, V_{rms}$

$\frac{N_1}{N_2} = \frac{120}{8.98} = 13.36$

b) $V_r = \frac{V_m}{2RCf}$

$R = \frac{V_o}{i_L} = \frac{12}{0.5} = 24\,\Omega$

$V_r = 0.03 \times V_m$

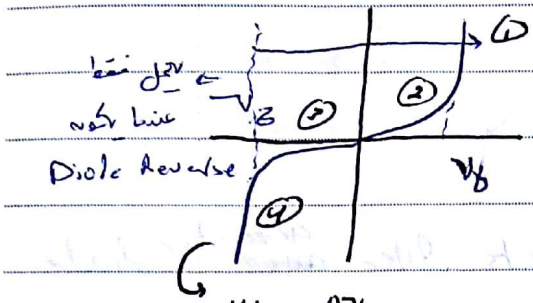
$= 0.03 \times 12 = 0.36\, V$

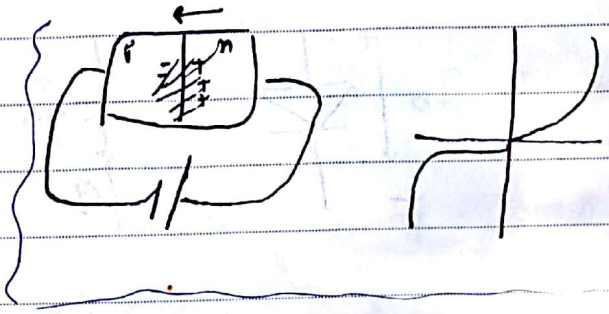
$C = \frac{12}{2 \times 24 \times 0.36 \times 60} = 11.6\,\mu F$

c)

No.

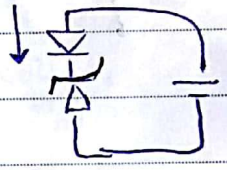
1.11 :- Zener Diode :-





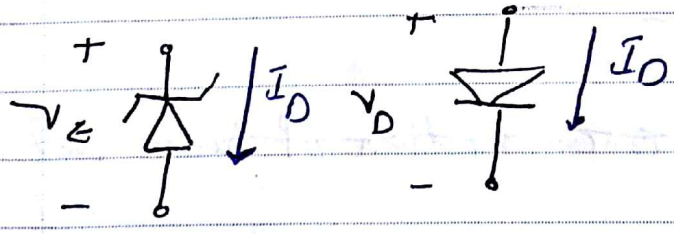
$$r_z = \frac{\Delta V_z}{\Delta I_z} \Rightarrow \frac{1}{r_z} = \frac{\Delta I_z}{\Delta V_z} \qquad r_z \approx 0$$

* Current drops down in the -ve region $\Rightarrow$ I for Zener diode is opposite to I of regular diode in forward active mode.



* On voltage of Zener diode is smaller than Breakdown voltage in regular diode due to high concentration of holes and electrons

* slight slope in curve due to small r_z for ideal zener $r_z = 0$ slope = ∞ (vertical)

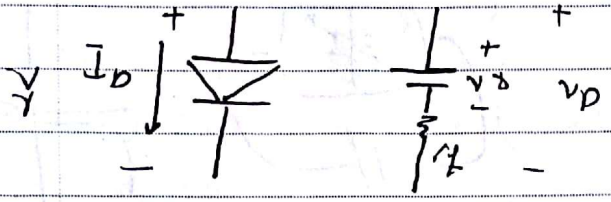


Zener voltage can be controlled by changing the Dopping level

No.

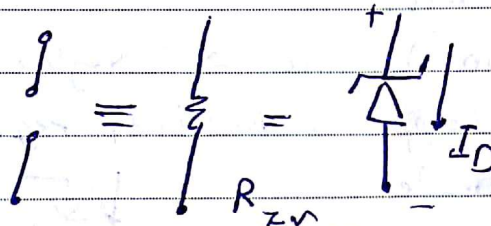
region 1 & 3 :- Zener operates like a regular diode

→ If $v_D \approx 0$ (or small) $v_D \simeq v_\gamma$



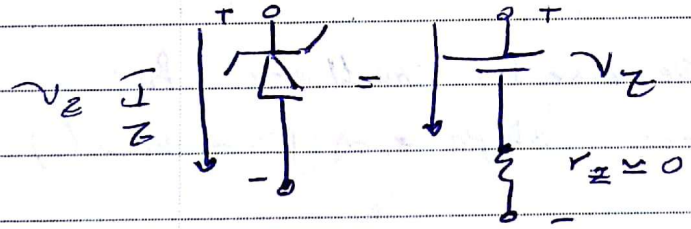
region 2 & 3 :- Diode off also acts like a regular diode

Voltage in magnitude Less than V_z



Voltage in zener is the open ckt voltage

region 4 :- Diode is on, $r_z \approx 0$ Voltage on Zener is V_z



~~due to high concentration of holes and~~

$$P_z = I_z V_z$$

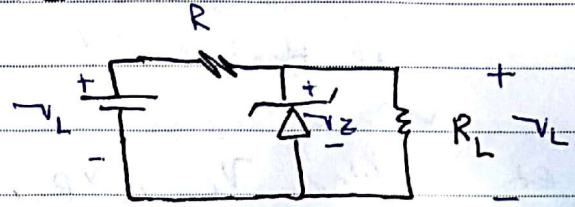
$$P_{z\,max} = I_{z\,max} \times V_z$$

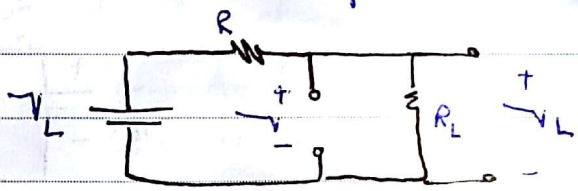
No.

Zener diode as a Voltage Regulator:

① V_I Fixed & R Fixed

* to check for the operation mode of the Zener remove it from the ckt & find open ckt & voltage:

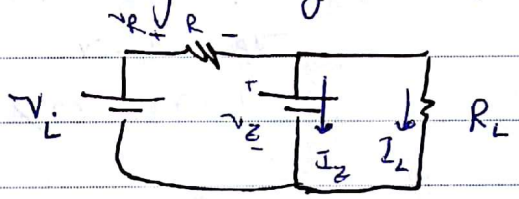




$$V = \frac{V_L R_L}{R_L + R}$$

* if $V > V_Z \Rightarrow$ diode On $\Rightarrow$ and $V_L = V_Z$
* if $V < V_Z \Rightarrow$ diode off $\Rightarrow V_L = V = \frac{V_i R_L}{R_L + R}$, $I_Z = 0$

* for on state the following analyses are performed



$$I_L = \frac{V_Z}{R_L}$$

$$V_R = V_i - V_Z$$

$$I_R = \frac{V_R}{R} = \frac{V_i - V_Z}{R}$$

$$I_Z = I_R - I_L$$

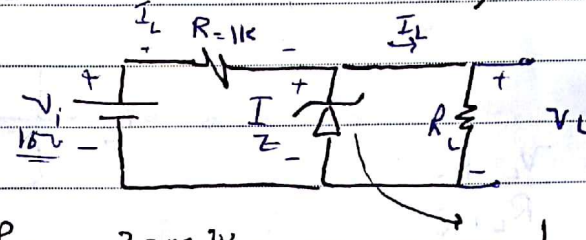
$$P_Z = I_Z V_Z \leq P_{Z,max}$$

No.

Note: when Zener is on, voltage on Zener diode can never be V_i. Its voltage is held at V_z, and the diode is said to (Lock-in) at that level

ex find V_L, V_R, I_z, P_z a.) $R_L = 1.2k$

b) $R_L = 7k$



$V_z = 10V$, $P_{z,max} = 30mW$

a) $V = 16 * \frac{R_2}{R + R_L} = 16 * \frac{1.2k}{1.2k + 1k} = 8.73V$

$V < V_z \Rightarrow$ Zener off

$I_z = 0$ $P_z = 0$

$V_R = V_i - V = 16 - 8.73 = 7.27V$

$V_L = V = 8.73V$

b) $R_L = 3K\Omega$

$V = 16 * \frac{3k}{(1+3)} = 12V$

$V > V_z \Rightarrow$ Zener on

$V_L = V_z = 10V$

$V_R = V_i - V_z = 16 - 10 = 6V$

$I_R = \frac{V_R}{R} = \frac{6}{1k} = 6mA$

$I_z = I_R - I_L$

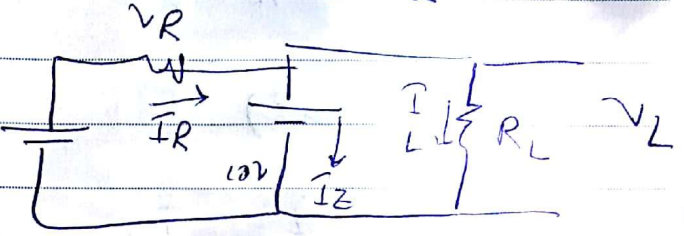
No.

$$I_L = \frac{V_z}{R_L} = \frac{V_L}{R_L} = \frac{10}{3k} = 3.33\,mA$$

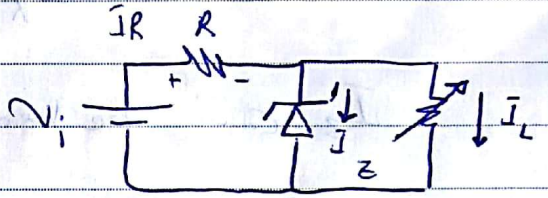
$$I_z = 6 - 3.33 = 2.67\,mA$$

$$P_z = I_z V_z = 2.67m * 10 = 26.7\,mW \quad (< 30mW)$$

acceptable



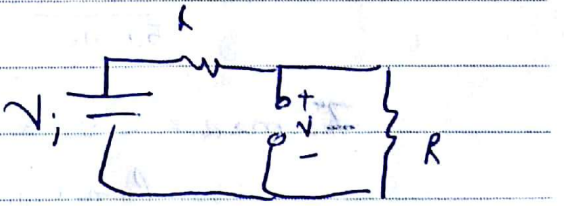
fixed V_i, variable R_L



* If R_L goes below acertain value (R_{min}) then Zener goes off ⇒ avoid $R_L < R_{min}$

* If R_L is too high, I_L is too low ⇒ I_z is high and can exceed $I_{z\,max}$ ⇒ P_z will be higher than $P_{z\,max}$ which should be avoide ⇒ $R_{L\,max}$ must be determined

$R_{L(min)}$



$$V = V_i \frac{R_L}{R_L + R}$$

$V > V_z$ ⇒ Zener is On

$$\Rightarrow V_z = V_i \frac{R_L}{R_L + R}$$

No.

$$R_{L,min} = \frac{R V_z}{V_i - V_z}$$

$$I_{L_{max}} = \frac{V_z}{R_{min}}$$

$$I_{z_{min}} = I_R - I_{L,max}$$

$\Rightarrow R_L$ (max)

$$I_L = I_R - I_z$$

fixed $\quad I_R = \frac{V_R}{R} = \frac{V_i - V_z}{R}$

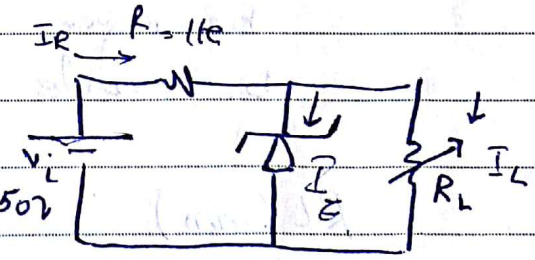
I_z can't be heigher than $I_{z\,max} \Rightarrow$

$$I_{L\,min} = I_R - I_{z\,max}$$

$$R_{L\,max} = \frac{V_z}{I_{L\,min}}$$

example find R_L & I_L that will result in $V_{R_L} = 10$

b) find $P_{z\,max}$



$$R_{L\,min} = \frac{1K(10)}{50-10} = 250\,\Omega$$

$V_z = 10V \quad I_{z\,max} = 37mA$

$$I_{L\,max} = \frac{V_z}{R_{L\,min}} = \frac{10}{250} = 40mA$$

for RL max

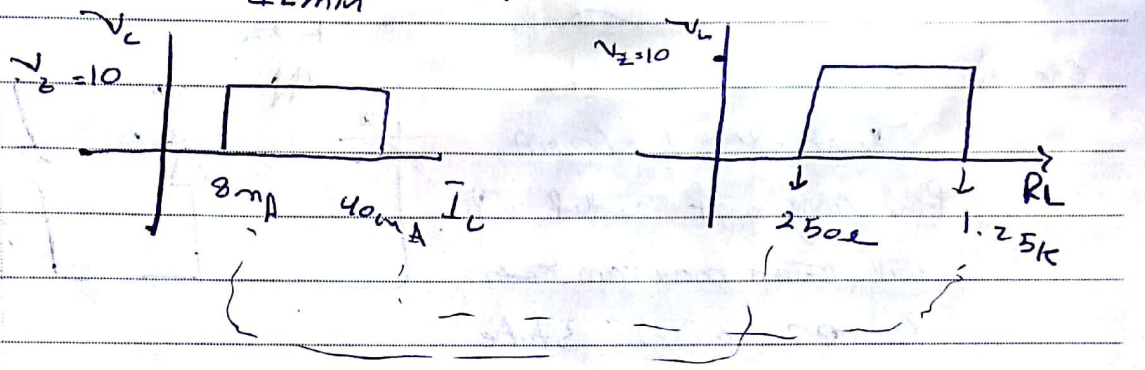
$$I_{L\,min} = I_R - I_{z\,max}$$

No.

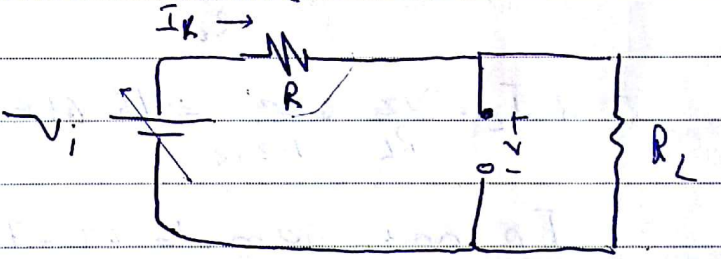
$I_R = \frac{V_R}{R} = \frac{40}{1k} = 40mA$

$I_{L\,min} = 40m - 32m = 8mA$

$R_{L\,max} = \frac{V_z}{I_{L\,min}} = \frac{10}{8m} = 1.25k\Omega$



* Fixed R_L and variable V_i :-



$V = V_i \frac{R_L}{R_L + R}$ for Zener to be on $V \geq V_z$

$V_{i\,min} = V_z \frac{(R_L + R)}{R_L}$

* less than $V_{i\,min}$ diode will be off

$I_L = \frac{V_z}{R_L}$ fixed

$I_{R_{min}} = \frac{V_{i\,min} - V_z}{R}$ variable

I_z also changes. $I_{z\,min} = I_{R_{min}} - I_L$

2.21

No.

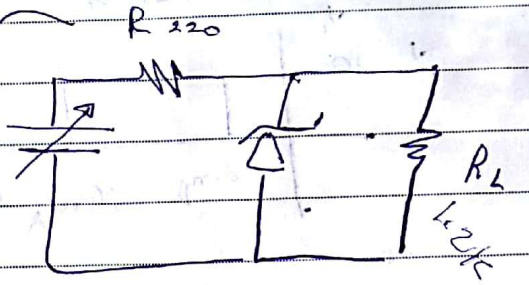
⇒ $V_{i\,max}$:-

I_z can't be higher than $I_{z\,max}$

$I_{R\,max} = I_{z\,max} + I_L$

$V_{i\,max} = I_{R\,max} R + V_z$

example :-



$V_z = 20V$, $I_{zm} = 60mA$

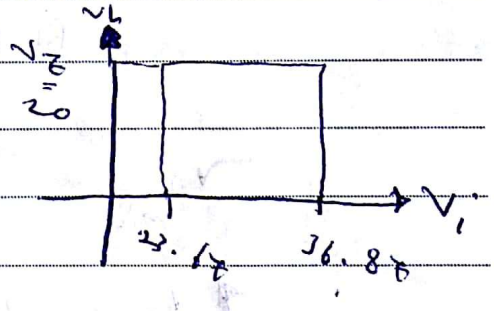
Find range of V_i that V_i will maintain Zener in "On" state

$V_{i,min} = V_z \frac{R_L + R}{R_L} = 20 \frac{(1.2k + 220)}{1.2k} = 23.67$

$I_L = \frac{V_z}{R_L} = \frac{20}{1.2k} = 16.67mA$

$I_{R\,max} = 60m + 16.67 = 76.67\,mA$

$V_{i\,max} = 76.17^{m}(220) + 20 = 36.87V$.



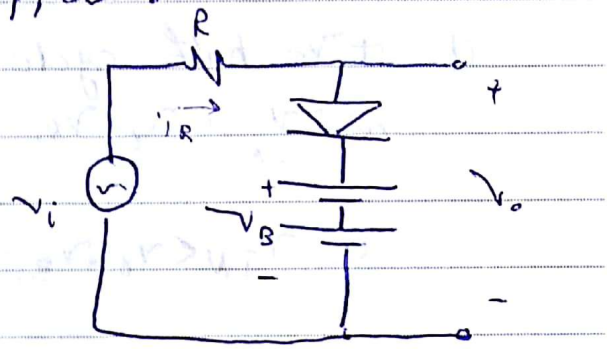
No.

2.3 Clipper & Clampers

2.1 Clipper (limiter) :-

Remove part of the applied signal that is either smaller or bigger than a certain value

Signal single diode clipper :



① $V_{IN} > V_\gamma + V_B$

$\Rightarrow$ Diode on

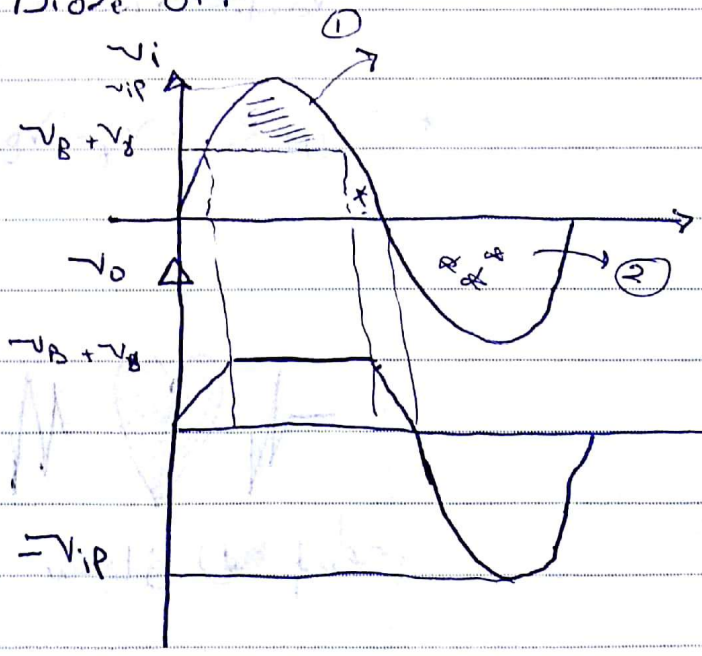
$V_o = V_B + V_\gamma$

$i_R = \dfrac{V_i - V_B - V_\gamma}{R}$

② $V_{IN} < V_B + V_\gamma \Rightarrow$ Diode off

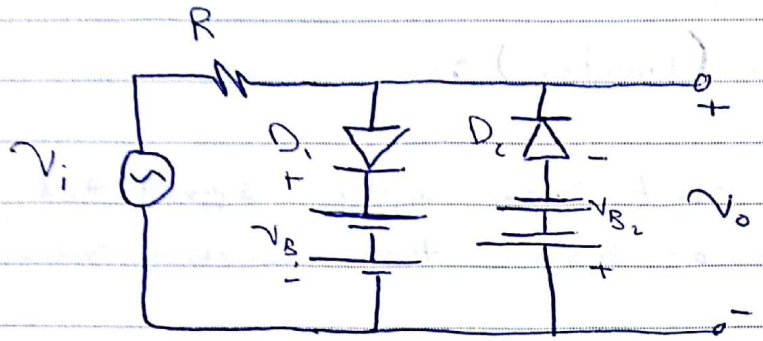
$i_R = 0$

$V_o = V_i$



No.

* Parallel based clipper :-



① +ve half cycle, D_2 off

ⓐ $V_{IN} > V_\gamma + V_{B_1}$ D_1 on $\Rightarrow V_o = V_\gamma + V_{B_1}$

ⓑ $V_{IN} < V_\gamma + V_{B_1}$ D_1 off $\Rightarrow V_o = V_{IN}$

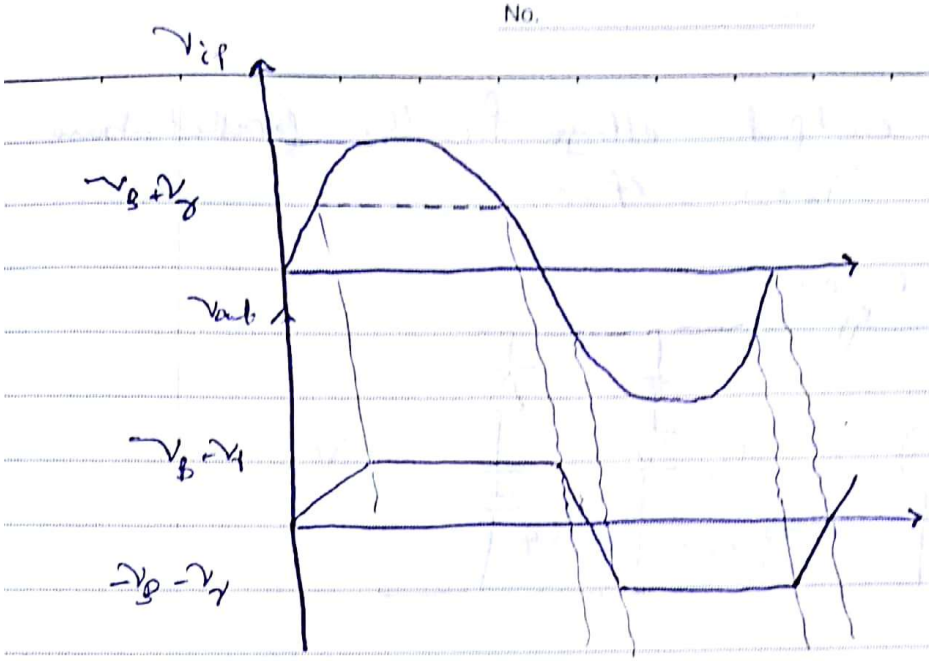
② -ve half cycle D_1 off :-

* $V_{IN} > -V_\gamma - V_{B_2}$ D_2 off

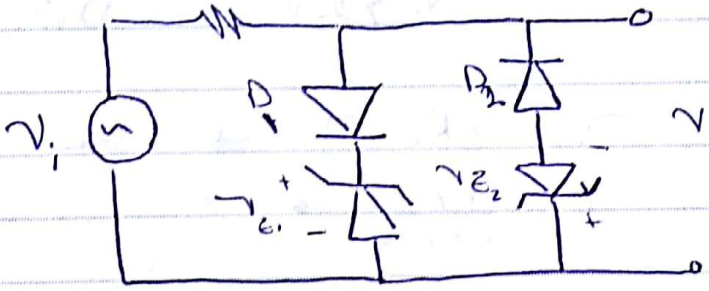
$V_{out} = V_i$

* $V_{IN} < -V_\gamma - V_{B_2}$ D_2 on $V_{out} = -V_\gamma - V_{B_2}$

سبحان الله وبحمده سبحان الله العظيم

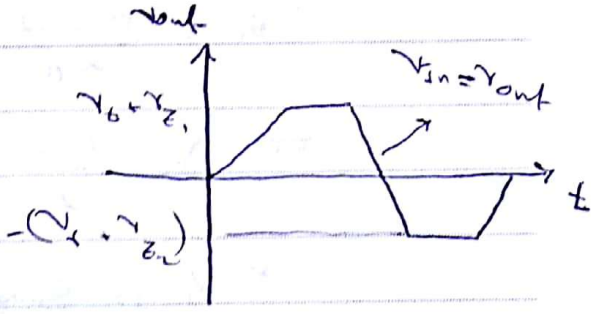


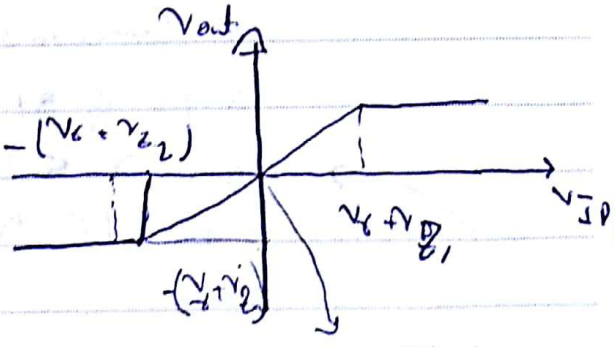
Zener for a clipper ckt



$** \Rightarrow -V_\gamma - V_{z_2} < V_{in} < V_\gamma + V_{z_1}$

$V_{out} = V_{IN}$

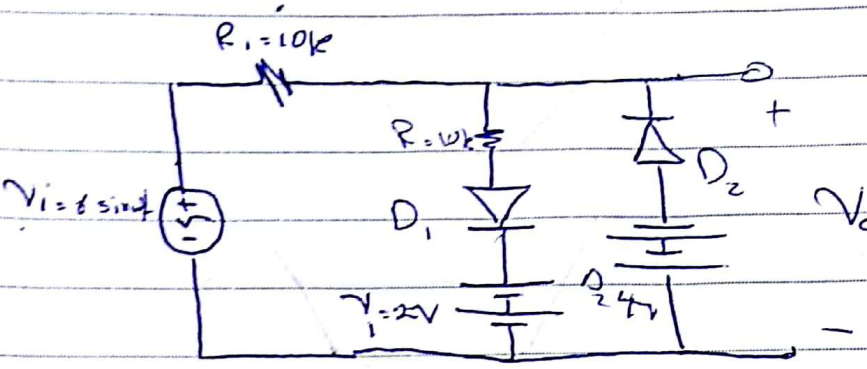




$V_{out} = V_{IN}$

No.

Ex8- Find the output voltage for the parallel-base clipper $V_\gamma = 0$, $r_f = 0$



① +ve half cycle D2 off

* $V_i > V_\gamma + V_1$

$V_i > 2V \Rightarrow$ Diode On

$V_o = iR_2 + V \Rightarrow$

$I = \frac{V_i - 2}{10k + 10k}$

$V_o = \frac{V_i - 2}{20k} * 10k + 2$

$\Rightarrow V_o = \frac{V_i}{2} - 1 + 2 = \frac{V_i}{2} + 1$

* V_i is Sinewave & V_o is a function of V_i

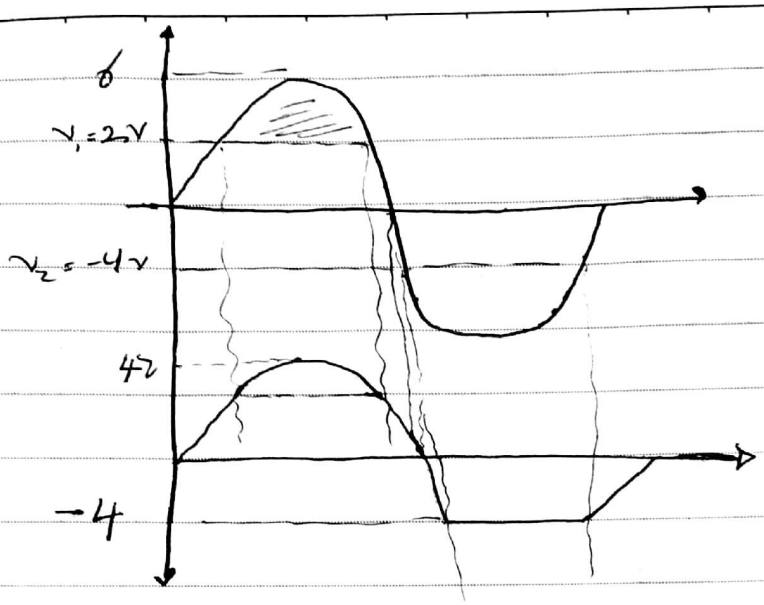
$\Rightarrow$ Sinewave

$V_{of} = \frac{6}{2} + 1 = 4$

** $V_i < V_i = 2V$

D_i off, $V_o = V_i$

No.



$\Rightarrow$ -ve half cycle D_1 off

* $V_{IN} < V_z = -4V$

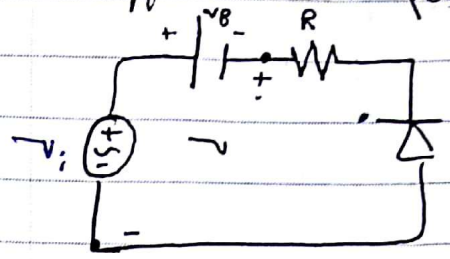
D_z is on, $V_{out} = -4V$

* $V_{IN} > V_z = -4V$

D_z is off $V_{out} = V_{IN}$

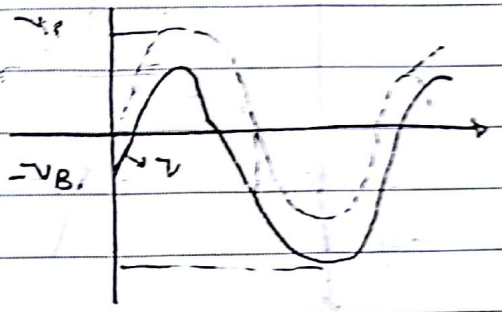
No.

* clipper with power supply C,h Series with input



$V_\gamma = 0$ $r_f = 0$

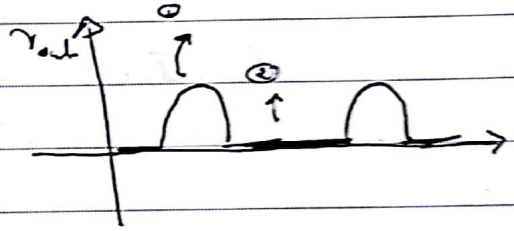
$v = v_i - v_B$



① if $v > v_\gamma = 0$

diode off $v_{out} = v = v_z - v_B$

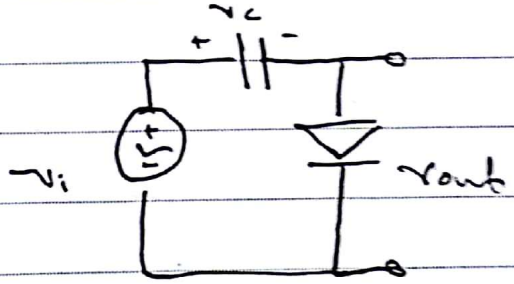
② if $v < v_\gamma = 0$ diode on $v_{out} = v_\gamma = 0$



2.3.2 Clampers :-

Does not change the form of the input signal It only shifts it aparalown has acapacitor in the ckt.

* Clamper with no DC Source



$V_\gamma = 0$, $r_f = 0$

No.

* $t < \frac{T}{4}$ (initially assume $V_c = 0$)

+Ve half cycle, Diode on Capacitor will charge, I.e. $C = 0$, Capacitor will charge until

$V_i = V_m \quad V_o = V_\gamma = 0$

* $t > \frac{T}{4}$ &

input starts decreasing

$V_m > V_i \Leftarrow V_{out} = V_i - V_c$

$= V_i - V_m$

$= -Ve$

$\Rightarrow$ Diode open (off)

Capacitor can't discharge V_{out} and V_c is fixed at V_m

$V_c = V_m$

$V_{out} = V_i - V_c$

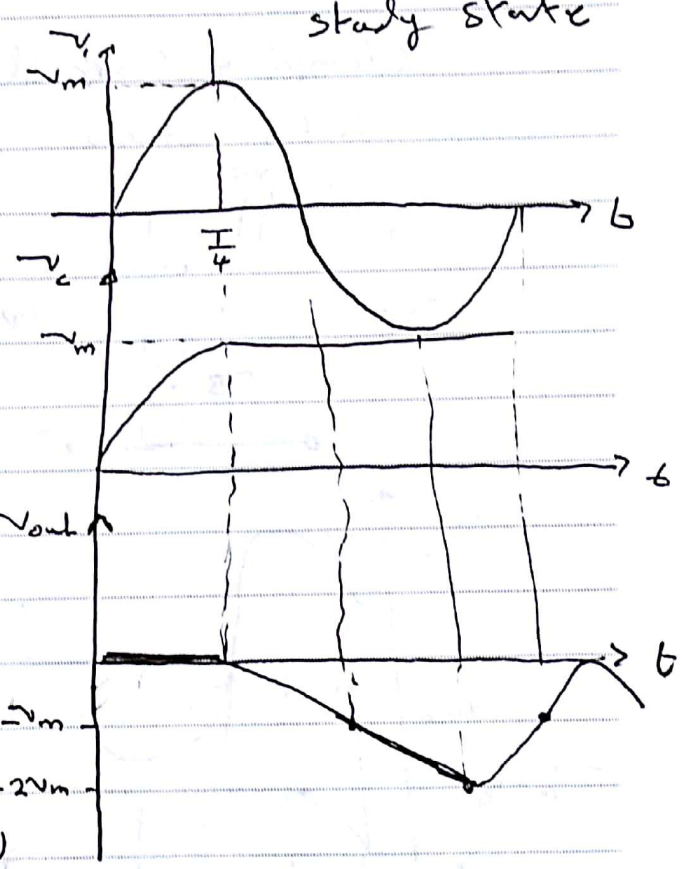
$V_m \sin\omega t$

$V_{out} = V_i - V_m = V_m(\sin\omega t - 1)$

at $V_i = V_m$, $V_{out} = 0$

at $V_i = 0$, $V_{out} = -V_m$

$\therefore V_i = -V_m$, $V_{out} = -2V_m$



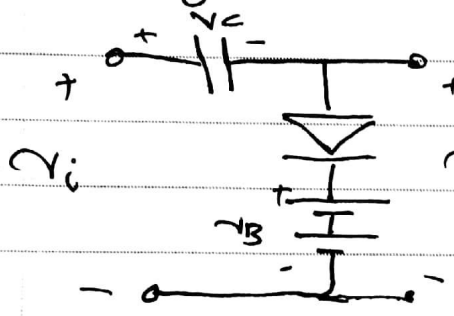
* Tip: if Diode points down down, signal will shift down, and upper peak will clamp at Voltage Connected to Diode in series

No.

* if diode points up, signal will shift up with -ve peak clamping at a value that is equal to the voltage connected to diode in ~~s~~ series

In our example $V_{avg} = -V_m$

Clamping Circuit that includes an independent voltage source



(initially $V_c = 0$)

* $t \leq \frac{T}{4}$, $V_i > V_B$

Diode On, $V_{out} = V_B$

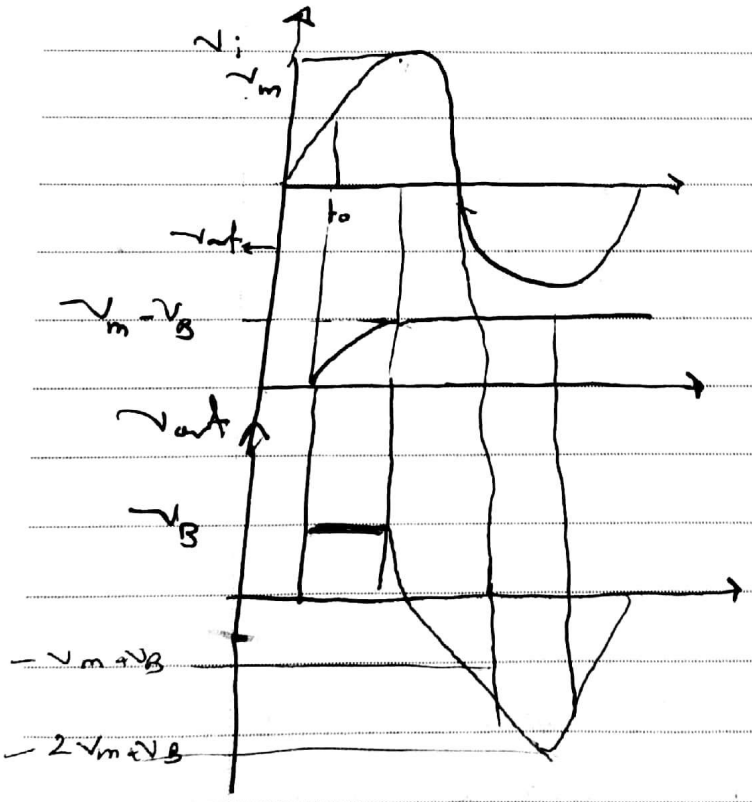
Capacitor charges

$V_c = V_i - V_B$

$V_{cm} = V_m - V_B$ $\quad V_m > V_i$

* $t > \frac{T}{4}$ $\quad -V_c$

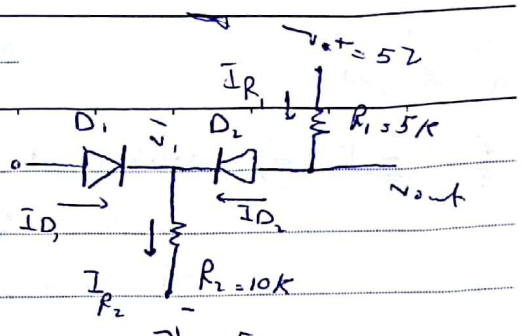
$V_{out} = V_i - V_c = V_i - V_m + V_B$



No.

Example :- 2.9

$V_\gamma = 0.7$



Find V_{out}, I_{D_1}, I_{D_2}, I_{R_2}

a) $V_I = 0V$ b) $V_I = 4V$

Sol a) $I_{D_1} = \text{zero}$, $I_{D_2} = I_{R_1} = I_{R_2} = \frac{5 - -5 - 0.7}{15k} = 0.62\ mA$

$V_{out} = V^+ - I_{R_1} R_1 = 5 - 0.62(5) = 1.9V$

$V_{D_1} = V_I - V^- = 0 - 1.2 = \ominus 1.2V \Rightarrow D_1$ off

& $I_{D_1} = 0$

b) $V_I = 4V$ Assume both diode on

$-V_{in} + V_\gamma - V_\gamma + V_{out} = 0$

$V_{out} = 4V$

$I_{R_1} = \frac{5 - 4}{5k} = 0.2\ mA$

$\bar{V} = V_I - V_\gamma = 4 - 0.7 = 3.3V$

$I_{R_2} = \frac{\bar{V} - -5}{10k} = \frac{3.3 + 5}{10k} = 0.83\ mA = I_{D_2}$

$I_{D_1} = 0.83 - 0.2 = 0.63\ mA$

No.

Ex 2.10 a) assume D_1, D_2 on.

$V_{out} = V_2 = 0V$

$V = V_I - V_\gamma = -0.7V$

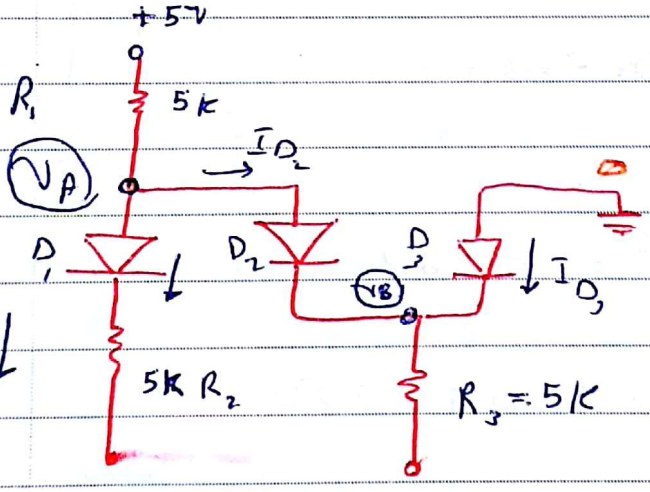
$I_{R_1} = \frac{5-0}{5K} = 1m \rightarrow = I_{D_2}$

$I_{R_2} = \frac{-0.7+5}{10K} = 0.43m$

$I_{D_1} = I_{R_2} - I_{D_2} = 0.43m - 1 = -ve$

D_1 is off $\Rightarrow I_{D_1} = 0$

Ex 2.11 find V_A, V_B & Diod Currents $V_\gamma = 0.7V$



Node Voltage at V_a

$\frac{V_A - 5}{5K} + \frac{V_A + 10 - 0.7}{5K} + I_{D_2} = 0$

$I_{D_2} = -0.86mA$

D_2 off & $I_{D_2} = 0$

Assume all diode on

$V_B = -V_\gamma = -0.7$

$V_A = V_\gamma + V_B = 0$

No.

Assume D_1 & D_3 on & D_2 off

$V_B = -0.7V$

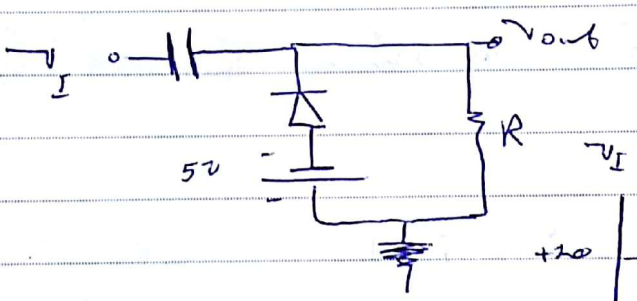
$I_{D_3} = \frac{V_B + 5}{5k} = 0.86mA + Ve$ ✓

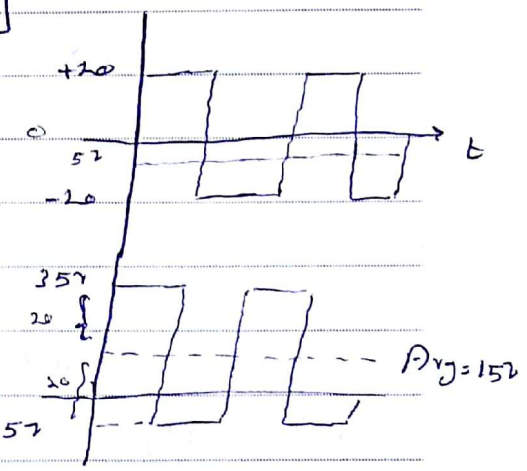
$I_{D_1} = \frac{5 - 0.7 + 10}{10k} = 1.43mA = I_{R_1}$

$V_A = 5 - I_{R_1} R_1 = -2.15V$

$V_{D_2} = V_A - V_B = -2.15 - 0.7 = -1.45V \Rightarrow D_2$ off

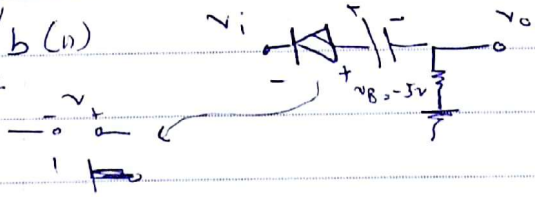
Problem 2.34 b)





2.35 / b (ii)

$V_\gamma = 0.7$



$-V_i + V + V_B = 0$

$V = V_i - V_B$

$V > V_\gamma$ & D on

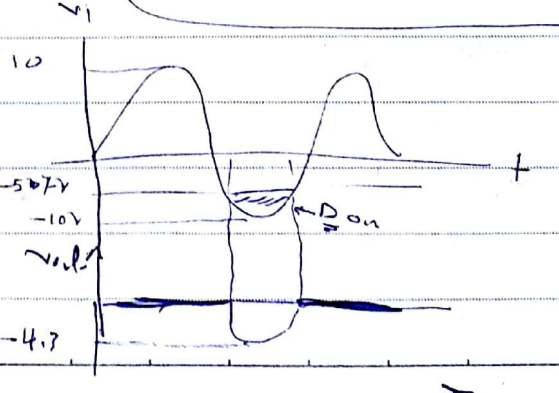
$V_i + V_B > V_\gamma$

$V_i > V_\gamma - V_B$

$V_i > -5.7V$

$-V_i + V_\gamma + V_B + V_{out} = 0$

$V_{out} = V_i + V_\gamma - V_B \Rightarrow = V_i + 0.7 + 5 = V_i + 5.7V$



Intrinsic semiconductor

No.

* $n_i^\circ = BT^{3/2}\left(e^{-E_g/2KT}\right)$
* $n_i^2 = n_o p_o$
* current density $= \frac{I}{Area} = \frac{A}{cm^2}$

Drift
* $v_{dn} = -\mu_n E \Rightarrow J_n = +e\mu_i E n = -e n v_{dn}$
* $v_{dp} = \mu_p E \Rightarrow J_p = e p \mu_p E$
* Total current density $= J_n + J_p = \sigma E = \frac{E}{\rho}$

Diffusion
* $J_n = e D_n \frac{dn}{dx}$
* $J_p = -e D_p \frac{dp}{dx}$

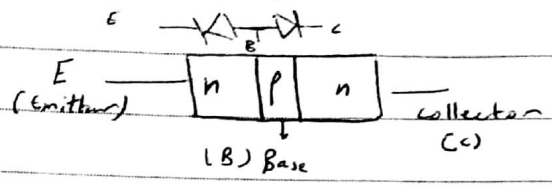
at $T = V_T = 0.0259 \approx 0.26\ m$

* $V_{bi} = \frac{kT}{e} \ln\left(\frac{N_a N_D}{n_i^2}\right)$
* $C_j = C_{jo}\left(1 + \frac{V_R}{V_{bi}}\right)^{-\frac{1}{2}}$
* $I_D = I_s\left(e^{V_D/nV_T} - 1\right)$
* $V_{ps} = I_s R\left(e^{V_D/nV_T} - 1\right) + V_D \Rightarrow$ iteration

No.

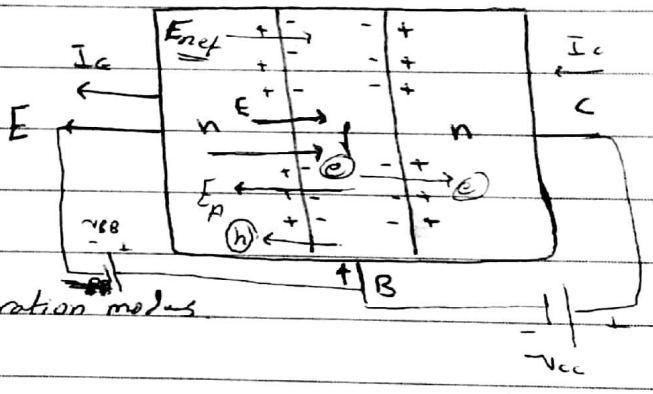
Ch:5 Bipolar Junction Transistor (BJT)

5.1.1 structure :-



Bipolar because both electrons and hole movement create a current

for (BJT) to operate properly, Base must be very thin 10^{-6} m.



4 Two junctions ⇒ 4 operation modes

5.1.2 npn transistor : forwards advice mode (FA)

(B-E) J is forward Biased

(B-C) J is Reverse Biased

forward biased of (B-E) J created an electric field E_A.

$E_A < E$

⇒ net E < E and in the same direction as E

No.

I_E * Force due to electric field will be less than force induced by gradient concentration ⇒ electrons will across from n to p & holes from p to n. Keep in mind that concentration of electrons in Emitter is much higher than concentration of holes in base

⇒ number crossing electrons is higher than number of crossing holes

* electron movement creates a current called emitter Current I.E

$$i_E = I_{E_0}\left[e^{V_{BE}/nV_T} - 1\right] \approx I_{E_0} e^{V_{BE}/nV_T}$$

$n = 1$ / I_{E_0} is directly proportional to cross sectional area of pn junction

I_C * most of electrons that cross to base Continue to Collector since base is very thin & e in emitter >> h in Base

These electrons will create the Collector current (I_C)

$$I_C = I_S\left(e^{V_{BE}/V_t} - 1\right) \qquad \alpha = \frac{I_C}{I_E} = \frac{I_S}{I_{E_0}}$$

** α: Common base Current gain.

α slightly less than 1.

No.

I_B ~~**~~ Base Current has two components :-

① a small portion of electrons crossing to Base due to (B-E) +ve biasing will recombine with holes in base => these hole must meby ~~be~~ replaced by Base terminal

② due to biasing the (B-E) J ⇒ holes will ~~no~~ move from p to n

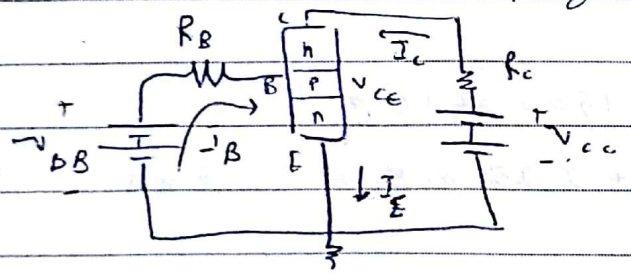
$$I_B = I_{B_0} [e^{V_{BE}/V_t} - 1]$$

Common Emitter Current Gain :-

$$\beta = \frac{I_c}{I_B} = \frac{I_s e^{V_{BE}/V_T}}{I_{B_0} e^{V_{BE}/V_T}} = \frac{I_s}{I_{B_0}}$$

50 < β < 300 Bjdully is constant but in practial varies

Common Emitter current gain (Cont)



$V_{CE} = V_{cc} - I_c R_c$

V_{cc} Controls Value of Value of V_{CE}

$V_{BB} = I_B R_B + V_{BE}$

iff $V_{BB} = 0$ $I_B = 0$ transistor is off

$I_B = I_c + I_E = 0$

~~$I_c = \beta I_B$~~ $I_c = \beta I_B$

No.

* Voltage between B and E, controls current at collection. I_C is dependent of V_{BC}

Current relations :-

$I_C = \beta I_B$

$I_E = I_C + I_B \Rightarrow = \beta I_B + I_B = (1+\beta) I_B$

$=$

$I_E = I_C + \frac{I_C}{\beta} \Rightarrow I_E = \frac{\beta+1}{\beta} I_C$

$I_C = \frac{\beta}{\beta+1} I_E \qquad I_C = \alpha I_E$

α : Common Base current gain $\alpha = \frac{\beta}{\beta+1} \rightarrow \alpha \simeq 1$ Less than

$\beta = \frac{\alpha}{1-\alpha}$

eg find I_E, I_C & α if $\beta = 150$, $I_B = 15mA$

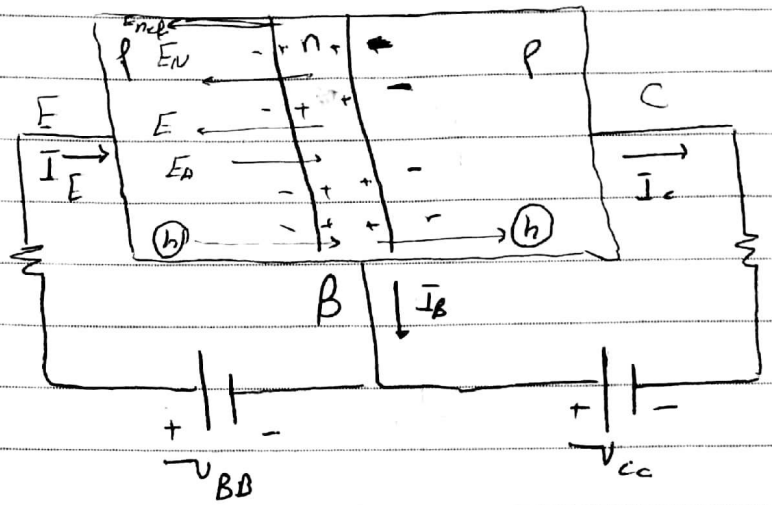
$I_C = 15M * 150 = 2.25\ mA$

$I_E = 15M + 2.25\ mA = 2.27\ mA$

$\alpha = \frac{150}{151} = 0.9934$

No.

5.1.3 P.N.P transistor: FA mode.



(B-E) Junction forward

(B-C) J Reverse

PNP

$V_{CB} = V_E - V_B$ (+ve)

$V_{CB} = V_C - V_B$ (-ve)

NPN

$V_{BE} = V_B - V_E$ +ve

$\Rightarrow V_{BC} = V_B - V_C$ -ve

$$I_E = I_{E_0} e^{V_{EB}/V_T}$$

$$I_C = \alpha I_E = I_S e^{V_{EB}/V_T}$$

$$I_B = I_{B_0} e^{V_{EB}/V_T} = \frac{I_C}{\beta}$$

$$I_E = I_C + I_B$$

$$I_E = (1+\beta) I_B$$

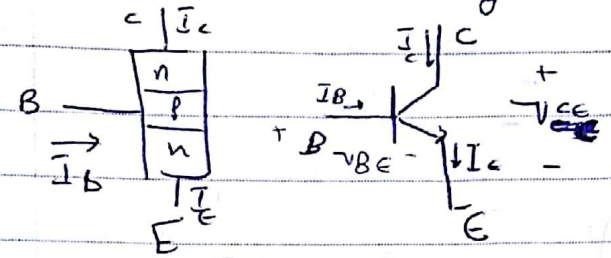
$$\alpha = \frac{\beta}{\beta+1}$$

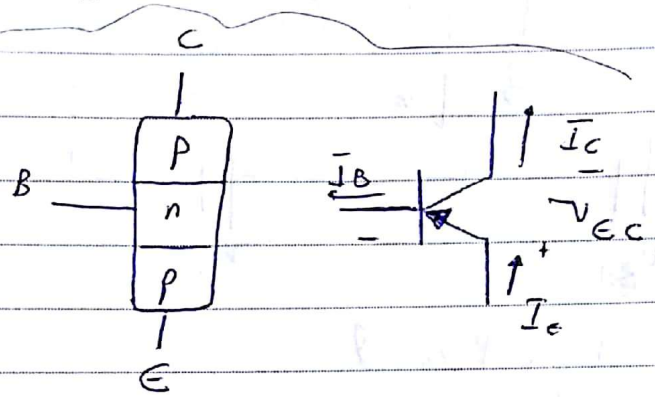
$$\beta = \frac{\alpha}{1-\alpha}$$

$$\Rightarrow I_C = \frac{\beta}{\beta+1} I_E$$

No.

5.1.4 :- Circuit symbol & conventions

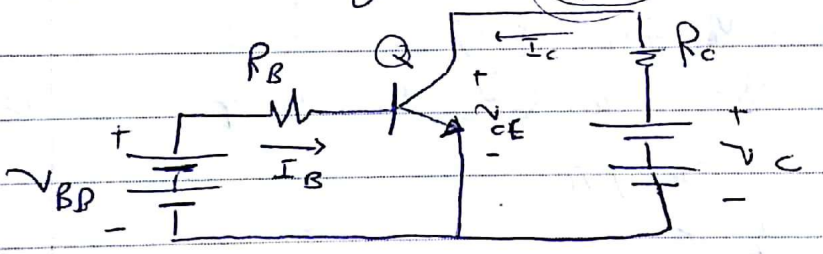




$V_{EC} = V_E - V_C$

$V_{EB} = V_E - V_B$

FA : Biasing for (npn) :-



Forward for FA mode

V_{BE} +ve

V_{BC} -ve

V_{CE} +ve

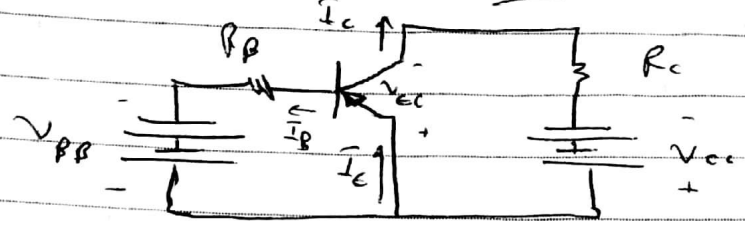
$V_{CE} = V_{CC} - I_C R_C$

$I_B = \dfrac{V_{BB} - V_{BE}}{R_B}$

FA Biasing for (pnp) :-

No.

FA Biasing for fwd,



V_{EB} +ve $V_C > V_B$

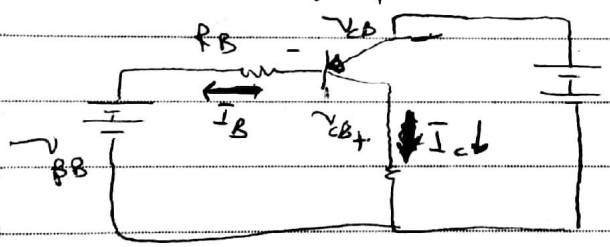
V_{CB} -ve $|V_{BB}| < |V_{cc}|$

$+V_{cc} - I_c R_c - V_{EC} = 0 \Rightarrow V_{EC} = V_{cc} - I_c R_c$

$V_{BB} - I_B R_B - V_{EB} = 0 \Rightarrow I_B = \frac{V_{BB} - V_{CB}}{R_B}$

P.T.O

FA : Biasing using +ve power supplies



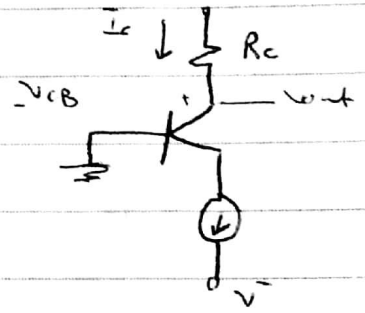
$V_{cc} > V_{BB}$, V_{EB} +ve

V_{CB} -ve

No.

5.1.5 Common Base (CB) :-

output voltage vs output current for different values of input (I or V)



$V_{out} = V_{CB}$

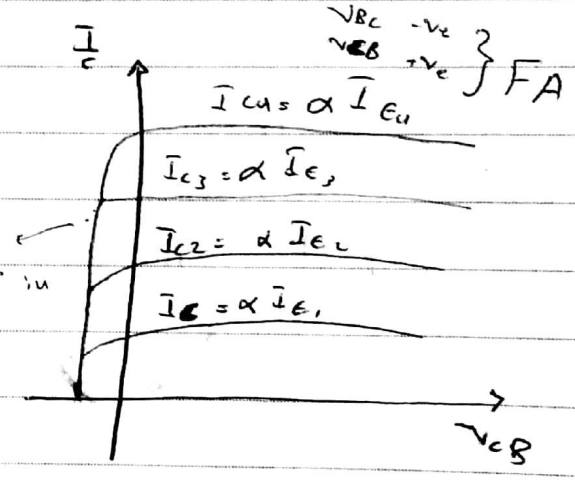
$I_{out} = I_c$

for FA mode

V_{BC} -ve , V_{BE} +ve

V_{CB} +ve

input current I_E

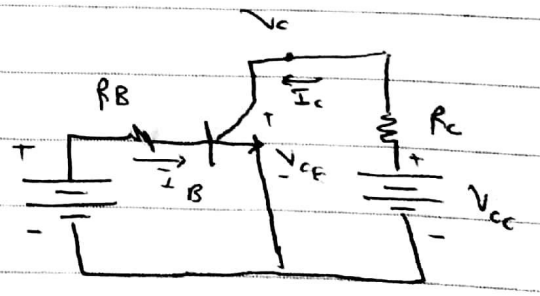


$I_c = \alpha I_E$, I_c is independent of V_{CB}

no longer in FA mode

$I_c \neq \alpha I_E$

Common Emitter CE :-



$V_{CE} = V_C - V_E$, $V_{BE} = V_B - V_E$

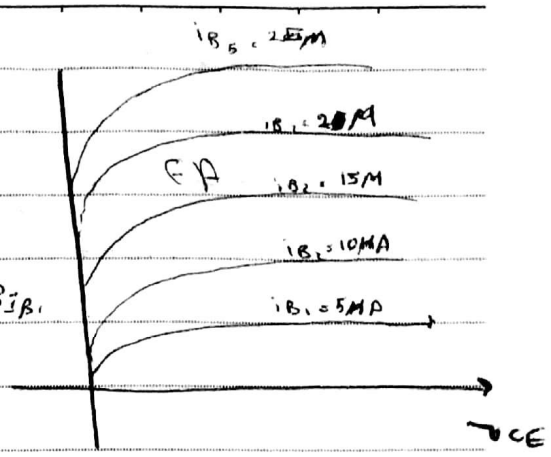
$V_{BE} = V_B - V_E$

I_c Vs V_{CE} for different value of I_B or V_{BE}

No.

Ideal I_C is independent of V_{CE}

$\text{slope} = \frac{\Delta I_C}{\Delta V_{CE}} = 0$



FA :-

V_{BE} +Ve $\quad V_B > V_E$

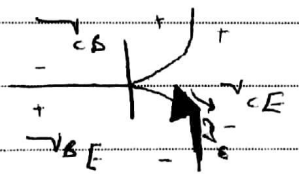
V_{BC} -Ve $\quad V_C > V_B$

$V_{CE} = V_C - V_E = +Ve$

& $V_{CE} > V_{BE}$

Early Voltage (VA) :-

Ideally I_C is independent of V_{CE}, But inpractice I_C depends on V_{CE}



$V_{BE} = V_{BC} + V_{CE}$

*** $V_{CE} = V_{CB} + V_{BE}$

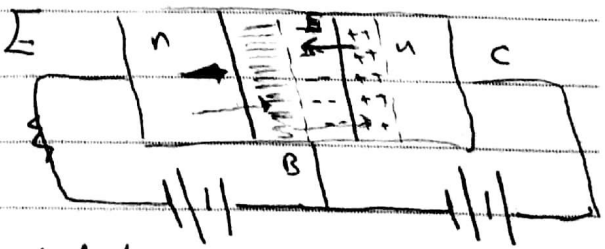
$V_{CB} = V_{CE} - V_{BE}$

} if V_{CE} increases, V_{CB} increase in FA, V_{CB} +Ve

(V_{BC} -Ve) ⇒ reverse voltage between Base & Collector & increase.

if V_{CB} increase, E ↑

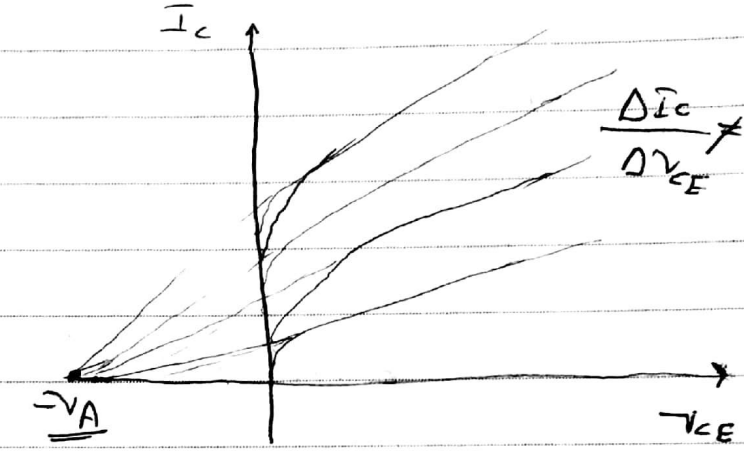
width of depletion region ↑ ⇒ less holes concentration in Base & more injected electrons



No.

~~Collector~~ Radio continue to collector ⇒ increasing I_C & decreasing I_B, and β increasses.

* this change of Base width is called Base-width modulation.



Early Voltage

* All curves will meet at $-V_A$ which is called Early Voltage V_A is positive

$50V \leq V_A < 300V$

* For the Ideal case slope = 0, $V_A = \infty$

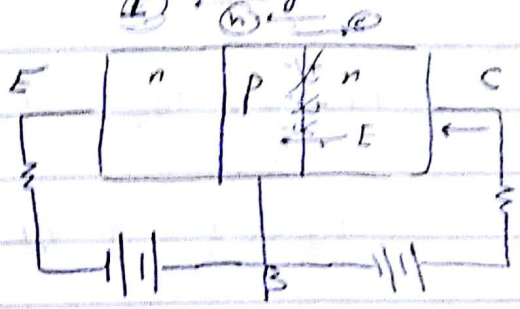
$$i_C = I_S e^{V_{BE}/V_T} \left(1 + \frac{V_{CE}}{V_A}\right)$$

$$\frac{\Delta i_C}{\Delta i_B} = I_S e^{V_{BE}/V_T} \frac{1}{V_A} = \boxed{\frac{I_C}{I_A}} = \text{slope}$$

if r_o is the resistance $r_o = \left(\frac{\Delta i_C}{\Delta V_{CE}}\right)^{-1} = \frac{V_A}{I_C}$

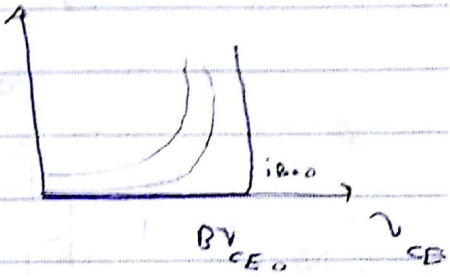
No.

Break down for CE Configuration :-



$V_{BC} = -V_e$, Avalanche high reverse voltage between Collector Base

Break down is obtained at $I_B = 0$



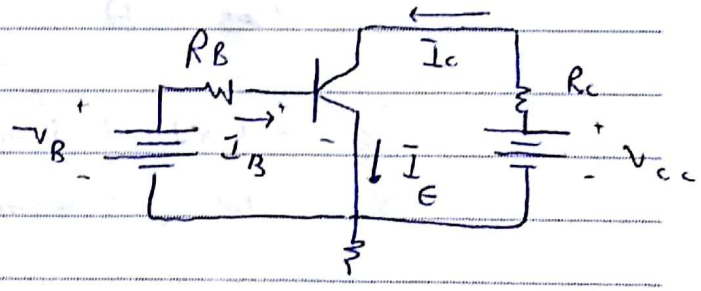
I_B

At higher currents than i_{B_0}, Break down occure at Lower voltages.

" " " "

5.2 DC Analysis of Transistor Circuits :-

5.2.1 Common Emitter Circuit CE



* Assume BJT in FA mode find

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

$V_{BE}(on) = 0.7\,V$

$I_C = \beta I_B$

$V_{CE} = V_{CC} - I_C R_C$ if $V_{CE} > V_{BE}$ then assmption is correct

$V_C > V_B$

$V_{BC} = -V_e$

No.

Power Dissipated in BJT :-

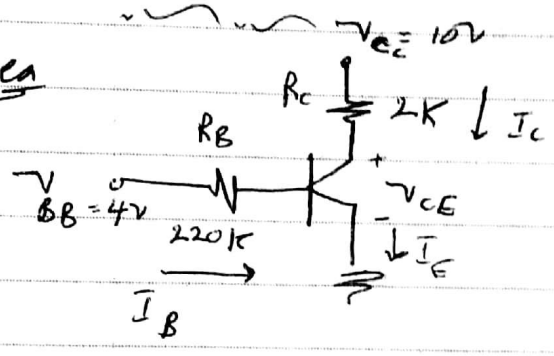
$$P_T = I_B V_{BE} + I_c V_{CE}$$

(small)

$I_B << I_c \rightarrow V_{BE} < V_{CE}$

for FA mode $I_B V_{BE}$ can be ignored

Ex



find I_B, I_c, I_c, V_{CE} and P_T

$\beta = 200$

$V_{(BE\ (on))} = 0.7V$

$$I_B = \frac{4 - 0}{220K} = 15\,MA$$

$$I_c = 200 * 15mA$$

$= 3$ mA

$I_E = 201 * 15M = 3.02$ mA

$V_{CE} = 10 - (2K * 3m) = 4V$.

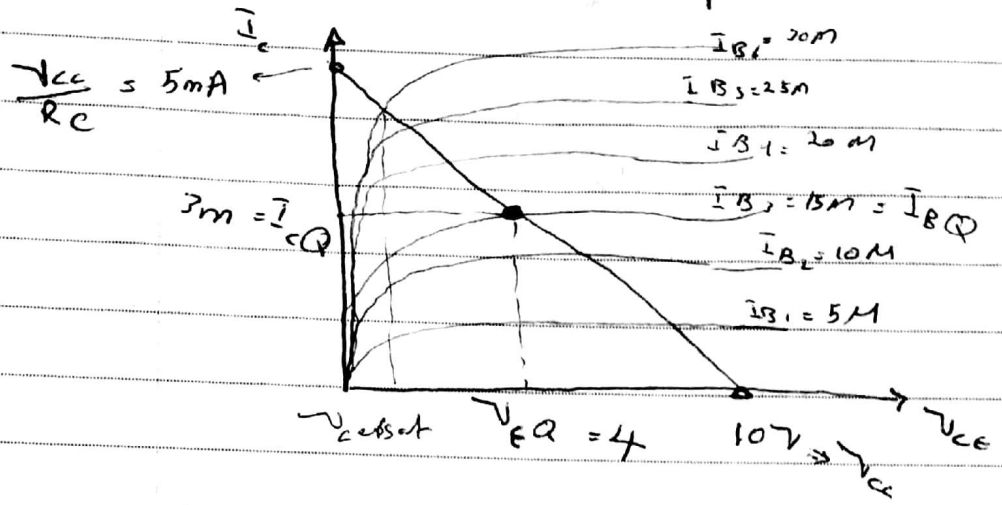
$P_T = 15M(0.7)(\quad) + 3m(4) \leq 12mW$

$V_{BB} = 4 > V_{BE} \rightarrow$ (B-E) j forward

$V_{CE} = 4 > V_{BE} \Rightarrow$ FA mode

No.

5.2.2 Common Emitter characteristics and Collector Emitter Load Line with Q-point



⇒ to find the intersection of DCLL with I_c & $V_{CE} = 0$ in Dcll eq.

DcLL eq = $V_{CE} = V_{cc} - I_c R_c$

$0 = V_{cc} - I_c R_c \Rightarrow I_c = \frac{V_{cc}}{R_c}$

for example $I_c = \frac{10}{2k} = 5mA$

⇒ to find the intersection between DCLL and V_{CE} axis, $I_c = 0$ in DCLL eq.

$V_{CE} = V_{cc} = 10V$

* for our example $I_{BQ} = 15MA$ ⇒ Q point is at intersection between I_{BQ} & DC load line

* Q point: Operation point ≡ point where I/V curve intersets with DCLL

No.

* If $V_{BB} < V_{BE} \Rightarrow$ BJT off $I_B = I_E = 0 = I_C$

in this Case $V_{CE} = V_{cc} - I_L^{\circ} R_c = V_{cc} = 10V$

If Q point moves up DCLL, I_B will increase and so will I_c. Ate some point I_c won't be able to increase more. This condition is called Saturation & $V_{CE} = V_{CE}(sat)$ will be less than V_{BE}.

$V_{CE}(sat)$ ranges between 0.1V & 0.3V

$V_{CE} < V_{BE} \Rightarrow V_B > V_C$, $V_{BE} = +Ve$

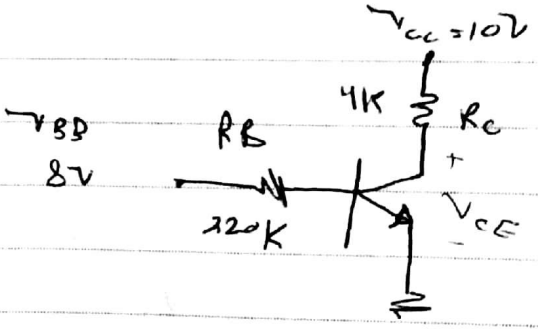
for Saturation mode, Both V_{BE} & V_{BC} are $+Ve$

Examples

find Current & Voltage

$\beta = 100$, $V_{BE}(on) = 0.7$

$V_{CE}(sat) = 0.2V$



$$I_B = \frac{8 - 0.7}{220k} = 33.2\mu A$$

$I_C = 100 \times 33.2\mu A = 3.32mA$

$V_{CE} = 10 - 3.32(4) = -3.28V < V_{BE}(on)$

Assumption incorrect & BJT Saturation

~~Assumption~~

$V_{CE} = V_{CE}(sat) = 0.2V$

$I_C = \frac{10 - 0.2}{Kc} = 2.45mA$ / I_B (Sat) $= 33.2MA$

~~$I_B(sat) = 33.2m$~~ $\beta(sat) = \frac{I_C}{I_B} = \frac{2.45mA}{33.2mA}$

$\beta = 74 < 100$

No.

$I_C \neq \beta I_B$ & $I_E \neq (1+\beta) I_B$

Forced β $I_E = I_C + I_B = 2.48\,mA$

$\beta I = 2.45_m (0.2) + 33.2m(0.7) = 0.511\,mA$

Problem Solving techiques :-

Assume BJT FA.

$V_{BE} = V_{BE(on)} = 0.7V$

$\Rightarrow I_B, I_C = \beta I_B, V_{CE}$

$V_{CE} > V_{BE}$ (FA) $\Rightarrow$ BJT FA $\Rightarrow$ (assumption)

If $V_{CE} < V_{BE}$ of $V_{CE} < 0 \Rightarrow$ then assume incorrect & Repeat for BJT in Sat.

$V_{CE} = V_{CE(sat)}$

Transistor operation modes.

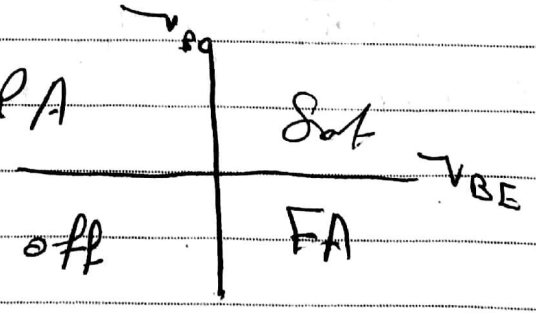
→ off : V_{BC} -ve, V_{BE} -ve

→ FA : V_{BC} -ve, V_{BE} +ve

→ RA : V_{BC} +ve

Collector acts like an emitter & emitter acts like a collector

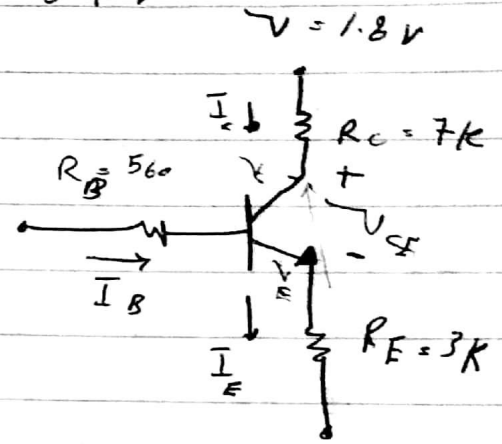
→ Sat : V_{BC} +ve, V_{BE} +ve



No.

32.4.

$\beta = 75$ $V_{BC(on)} = 0.7\,V$



find I_C, I_B, I_E
V_{CE}, DCLL, Slope

① Assume FA mode
$V_{BE(on)} = 0.7$

$I_E = (1+\beta) I_B$

$-V_{BB} + V_{BE(on)} + (1+\beta) I_B R_E + V = 0$

$I_B = \dfrac{V_{BB} - V_{BB} - V}{R_B + (1+\beta) R_E} = \dfrac{1 - 0.7 + 1.8}{560K + 76(3k)} = 2.66\,\mu A$

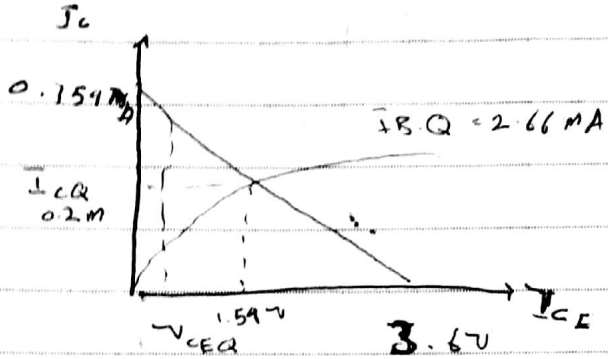
$IQ = I_C = 75 * 2.66\,\mu = 0.2\,mA$
$I_E = 76 * 2.66\,\mu = 0.203\,m$

$V_{CEQ} = V_{CE} = V^+ - I_C R_C - I_E R_C - V$
$= 1.8 - 0.2m(7k) - 0.203m(3k) + 1.8$
$= 1.59V > V_{BE(on)} \Rightarrow$ Assume Correct
$\therefore$ BJT is forward Active (FA) mode

No.

Dcll eq :-

$$V_{EE} = V^+ - V^- - I_C\left[R_C + \frac{B+1}{B} R_E\right) = 3.6 - I_C\left[7k - \frac{7k}{75}(1k)\right.$$



* at $V_{CE} = 0 \Rightarrow I_C = \frac{3.6}{7k + 1k\frac{7k}{75}} = 0.359\,mA$

* at $I_C = 0$

$V_{CE} = 3.6V$

$\Rightarrow$ slope $= \frac{\partial I_C}{\partial V_{CE}}$

$$I_C = \frac{V^+ - V^- - V_{CE}}{R_C + \frac{B+1}{B} R_E} = \frac{-1}{R_C + \frac{B+1}{B} R_E} = \frac{-1}{10.04\,k}$$

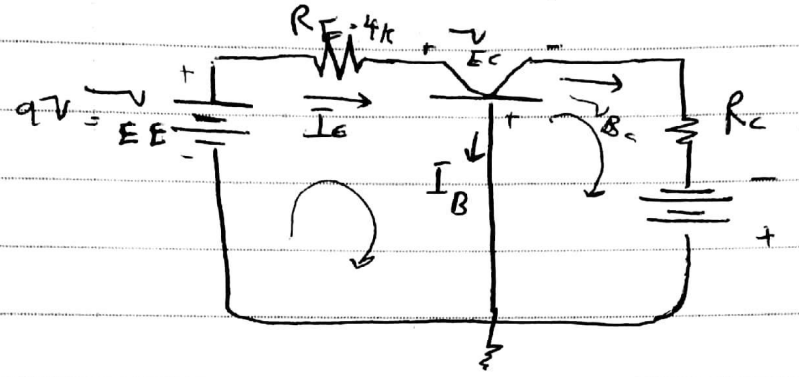
$\therefore$ if $B \gg 1$ slope $= \frac{-1}{R_C + R_E} = \frac{-1}{10\,k}$

No.

5.37 pnp common Base:

find I_E, I_C, V_{BC}, V_{EC} $\quad V_{EB(on)} = 0.7V$

$\alpha = 0.9920$



$$\Rightarrow \quad -V_{EE} + I_E R_E + V_{EB} = 0$$

$$I_E = \frac{V_{EE} - V_{EB}}{R_E} = \frac{9 - 0.7}{4k} = 2.075\ mA$$

$$\Rightarrow \quad I_C = \alpha I_E = 0.992 \times 2.075m = 2.058\ mA$$

$$\Rightarrow \quad V_{BC} + I_C R_C - V_{CE} = 0$$

$$V_{BC} = V_{CC} - I_C R_C = 9 - 2.058(2.2) = 4.472V$$

$$V_{CB} = -4.472V$$

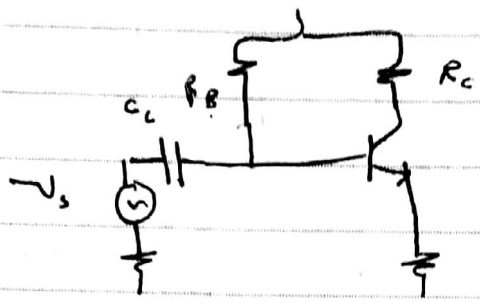
$$\Rightarrow \quad -V_{EE} + I_E R_E + V_{EC} + I_C R_C - V_{CC} = 0$$

$$V_{EC} = V_{EE} + V_{CC} - I_C R_C - I_E R_C = 5.177 \approx V_{EB(on)}$$

$$\alpha = \frac{B}{B+1} \quad \Rightarrow \quad B = \frac{\alpha}{1-\alpha}$$

No.

5.4 Bipolar Transestor Biasing

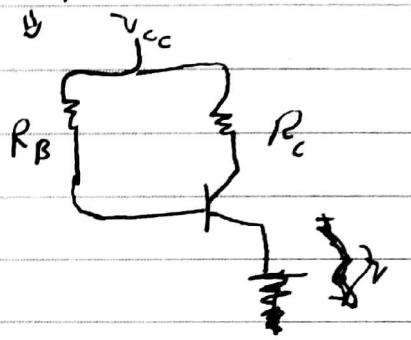


C_c : Coupling Capacitor

for DC analysis $f = 0$

$$X_c = \frac{1}{\omega C} = \frac{1}{2\pi f C} = \infty$$

⇒ open for DC analysis

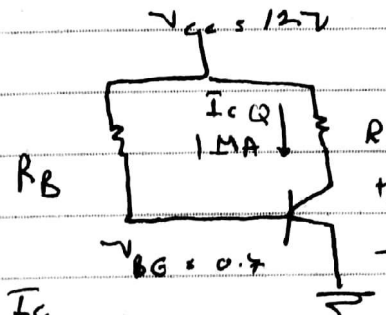


Ex 5.14 :- Design a single-Base resister npn ckt

$V_{cc} = 12V$, $I_{CQ} = 1mA$, $V_{CEQ} = 6V$, $\beta_o = 100$ ←

, $V_{BE(ON)} = 0.7V$ $\beta_1 = 50$ ←

$R_B = ??$, $R_c = ??$ $\beta_2 = 150$ ←



$$I_{BQ} = \frac{I_c}{\beta} = \frac{1m}{100} = 10\,MA$$

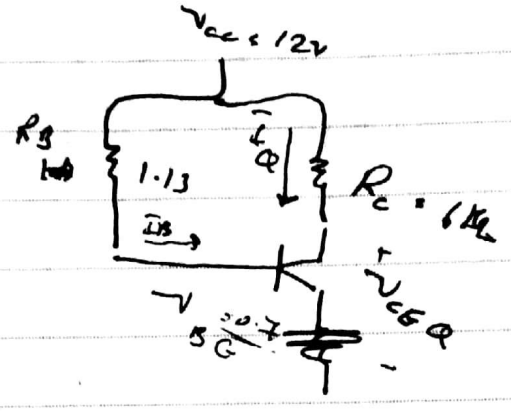
$$I_c = \frac{V_{cc} - V_{CEQ}}{R} = \frac{12 - 6}{1MA} = R \Rightarrow R = 6K\Omega$$

$$R_B = \frac{V_{cc} - V_{BE(on)}}{I_{BQ}} = \frac{12 - 0.7}{10M} = 1.13M\Omega$$

No.

For R_C & R_B find V_{CEQ}, I_{CQ}, I_B, for $\beta = 50, 100, 150$

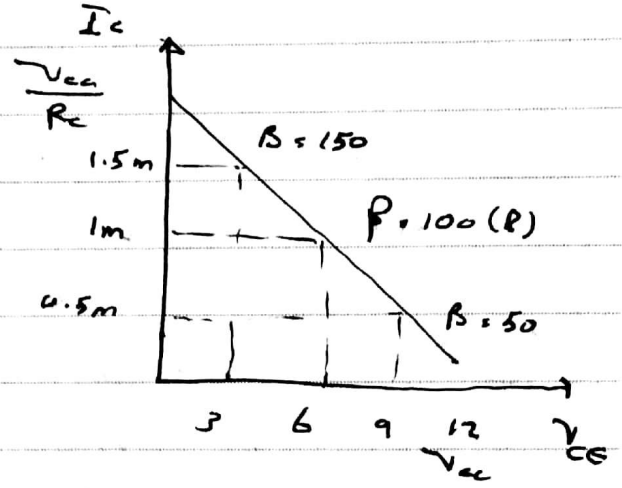
$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = 10\text{mA}$$



$$I_{CQ} = \beta I_{BQ}$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C$$

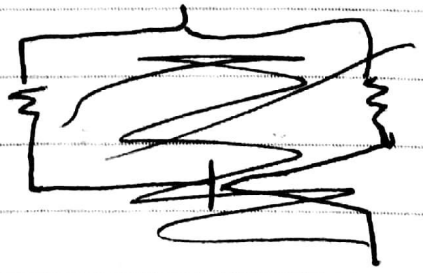
$$V_{CE} = V_{CC} - I_C R_C$$



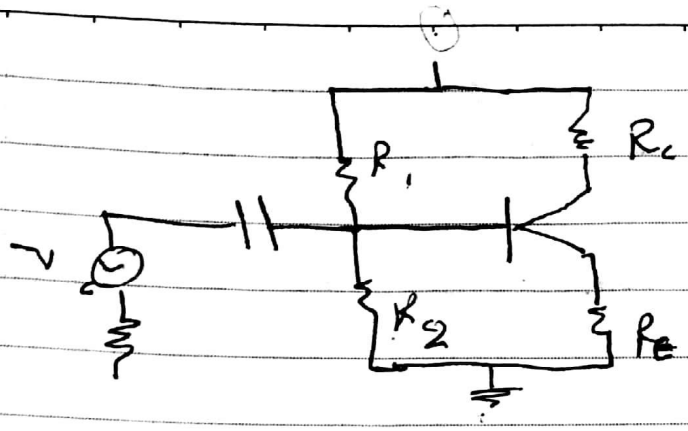
B	50	100	150
I_B	10M	10M	10M
I_C	0.5m	1m	1.5m
V_{CE}	9	6	3

5.4.2 Voltage Divider Biasing & Bias stability :-

⇒ Instead of a single R_B, R_B is replaced with the Resistors (R_1, R_2) & Resistor R_F is connected to the emitter

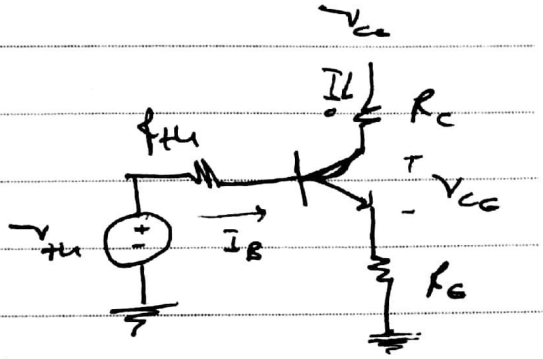


No.



$$R_{th} = R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{th} = V_{cc} \frac{R_2}{R_1 + R_2}$$



$$-V_{th} + I_B R_{th} + V_{BE(on)} + I_E R_E = 0$$

$$I_E = (1+\beta) I_B$$

$$I_B = \frac{V_{th} - V_{BE(on)}}{R_{th} + R_E (1+\beta)}$$

$$\rightarrow I_C = \beta I_B = \beta \left(\frac{V_{th} - V_{BE(on)}}{R_{th} + R_E (1+\beta)} \right)$$

$$-V_{cc} + I_C R_C + V_{CE} + I_E R_E = 0$$

$$I_E = \frac{\beta + 1}{\beta} I_C$$

$$V_{CE} = V_{cc} - I_C \left(R_C + R_E \frac{\beta + 1}{\beta} \right)$$

No.

Ex find I_B, I_C, V_{CE} given that $V_{cc} = 10V$
$R_C = 2k$, $R_E = 0.4K$, $R_1 = 56k$ $R_2 = 12.2k$
$V_{BE}(on) = 0.7\ V$, $\beta = 100$
when Done repeat for $\beta = 50$, $\beta = 150$

$$R_{th} = \frac{56k * 12.2k}{56k + 12.2k} = 10k\ \Omega$$

$$V_{th} = 10 * \frac{12.2k}{56k + 12.2k} = 1.79\ V$$

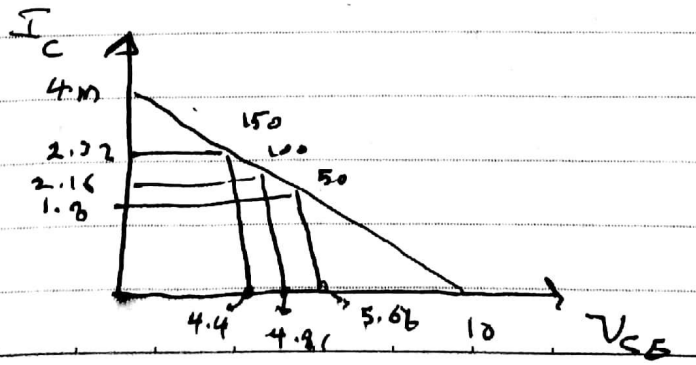
$$I_B = \frac{1.79 - 0.7}{10k + 101(0.4k)} = 21.6\ \mu A$$

$$I_C = \beta\ 100 * 21.6\mu = 2.16\ mA$$

$$I_E = 101 * 21.6\mu = 2.18\ mA$$

$$V_{CEQ} = 12 - 2K(2.16m) - 0.4K(2.18m)$$
$$= 4.81\ V$$

β	50	100	150
I_B	35.9m	21.6m	15.5m
I_C	1.8m	2.16m	2.32m
V_{CE}	5.67V	4.81V	4.4V



No.

Design requirement of stability

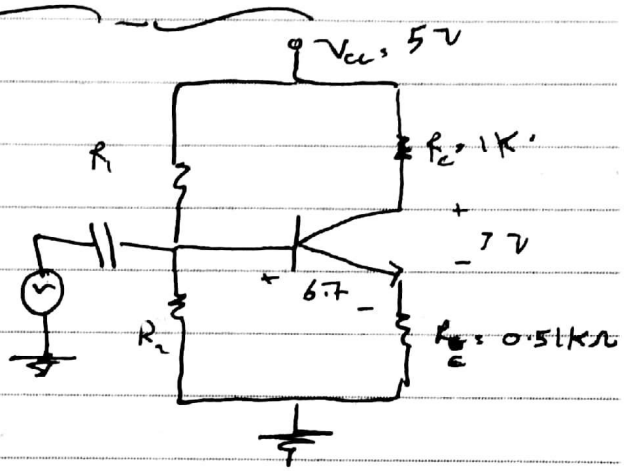
$R_{th} \ll (1+\beta) R_E \Rightarrow \beta \gg 1$

$I_{CQ} = \frac{V_{th} - V_{BE}}{R_E}$ independant of β

but R_{th} can't be too small, because R_1 & R_2 will be too small too $\Rightarrow$ power dissipation in R_1 & R_2 will be too high

$\Rightarrow$ agneral rule for bzai bias stability was developed : $R_{th} = 0.1 (\beta+1) R_E$

eg



$V_{CEQ} = 3V$

$V_{BE(on)} = 0.7 V$

$\beta = 120$

$60 \leq \beta \leq 180$

$R_1, R_2 = ??$

for stability

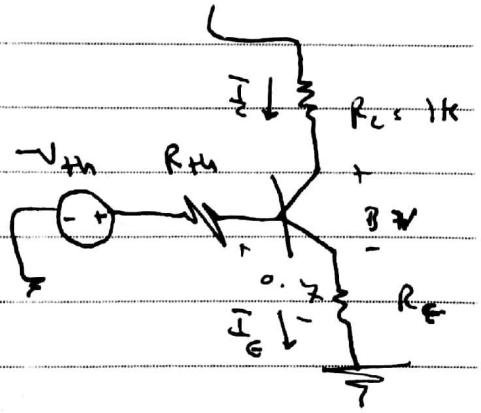
$V_{th} = V_{cc} \frac{R_2}{R_1 + R_2}$

$R_{th} = R_1 // R_2$

$R_{th} = 0.1(\beta+1) R_E$

$= 0.1 (121) 0.51K$

$= 6.17K$



$V_{th} = I_B R_{th} + V_{BE(on)} + (\beta+1) I_B R_E$

I_E

No.

$I_B \approx I_C$

$$I_C = \frac{V_{cc} - V_{CE}}{R_C + R_E} = \frac{5 - 3}{1.51k} = 1.32mA$$

$$I_{BQ} = \frac{I_C}{\beta} = \frac{1.32m}{120} = 11\mu A$$

$$V_{th} = 11M(6.17k) + 0.7 + 121\ (0.51k)(11M)$$
$$= 1.447V$$

$$1.447 = 5\frac{R_2}{R_1 + R_2} \quad ① \quad \text{Solve for}$$

$$R_1 = 21.3k$$

$$6.17k = \frac{R_1 R_2}{R_1 + R_2} \quad ② \quad R_2 = 8.69k$$

Create

for $\beta = 60$
120
180

I_B stock

$R_1 = 20k$

$R_2 = 8.2k$

$$R_{th} = \frac{20k * 8.2k}{20k + 8.2k} = 5.82k\Omega$$

$$V_{th} = \frac{8.2k * 5}{8.2k + 20k} = 1.454V$$

$$I_B = \frac{1.454 - 0.7}{5.82k + (1+\beta)(0.51k)}$$

$$I_{CQ} = I_{BQ} \times \beta$$

$$V_{CEQ} = V_{cc} - I_c(1k) - \frac{(1+\beta)}{\beta} I_c (0.51k)$$

No.

β	60	120	180
I_{BQ}	20.4 μA	11.2 mA	7.68 μA
I_{CQ}	1.23 m	1.34 mA	1.38 m
V_{CE}	3.13	2.97	2.91 V

Q-point are close for different value of β

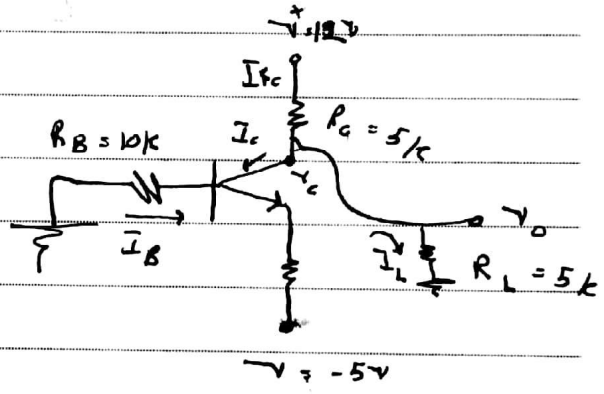
Also $R_1 \& R_2$ are not very small

⇒ power dissipation not too high

Note 2: R_G also reduces temperature effects

5.2.4 مثال سابق تم حله

Ex: 5.10



Find currents V_{CE} and DCLL eq

$V_{BE(ON)} = 0.7$ V

$\beta = 100$

$$I_B = \frac{-V_{BE(on)} \overset{(=5}{-V}}{R_B + (1+\beta) R_E} = 8.35\ \mu A$$

$I_C = 100 * 8.35 = 0.835$ mA

$I_E = 101 * 8.35 \mu = 0.843$ mA

⇒ at V_C node Voltage:

$$I_1 = I_C + I_L \quad / \quad \frac{V^+ - V_C}{R_C} = 0.835m + \frac{V_C}{R_L}$$

No.

Solve for V_c

$$V_c = V_o = 7.91\ V$$

$$I_1 = \frac{12 - 7.91}{5k} = 1.62\ mA$$

$$I_L = \frac{7.91}{5k} = 0.782\ mA$$

$$V_{CE} = V_C - I_E R_E - V$$

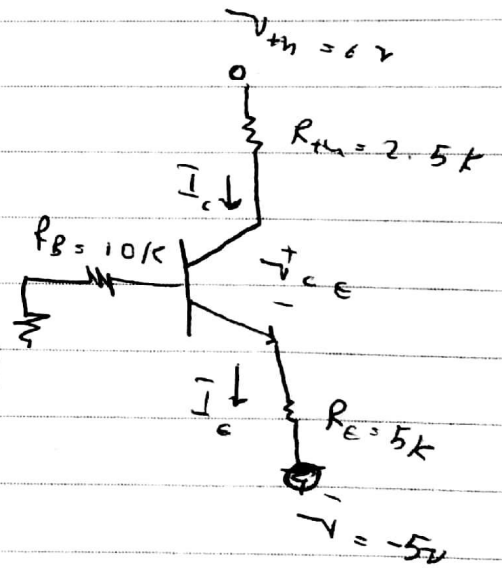
$$= 3.91 - 0.843\ m(5K) + 5$$

$$= 4.7\ V$$

Thevenin

$$V_{th} = V_{cc}\frac{R_L}{R_L + R_C} = \frac{12\ (5K)}{10\ k} = 6\ V$$

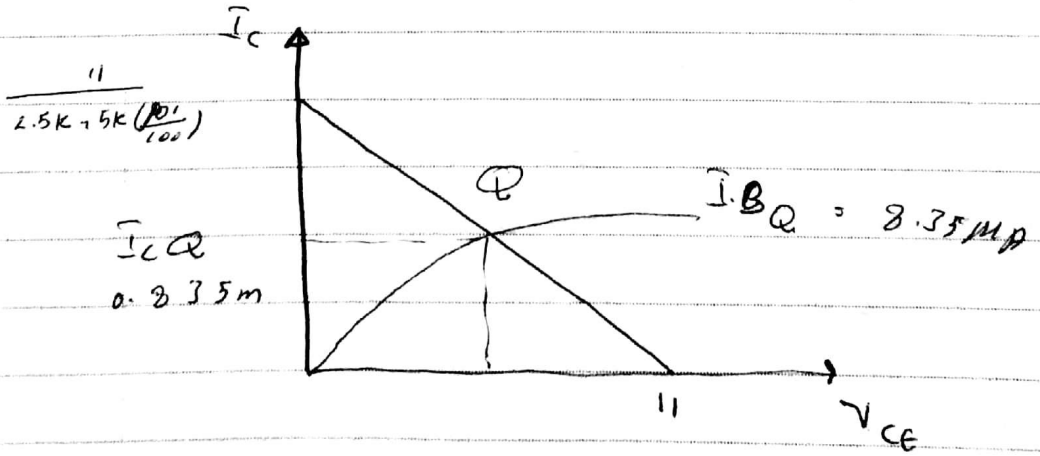
$$R_{th} = R_L // R_C = 2.5K\ \Omega$$



$$V_{CE} = V_{th} - R_{th}\frac{I_c}{} - I_E R_E - V$$

$$\Rightarrow V_{CE} = 11 - I_c\left(2.5k + 5k\left(\frac{\beta+1}{\beta}\right)\right)$$

R_{th} R_E

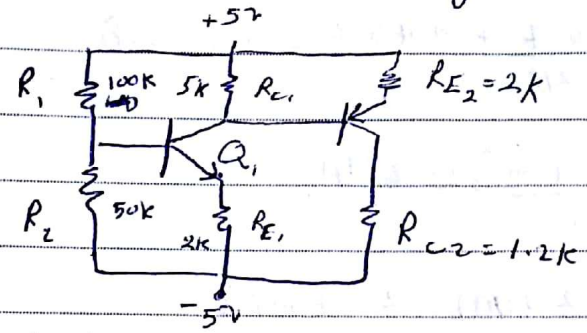


No.

Slope = $\frac{-1}{R_{th} + \frac{\beta+1}{\beta} R_E} \approx \frac{-1}{R_{th} + R_E}$

5.5 Multistage Circuits :-

Cascal :- o/p of stage 1 is input to stage two

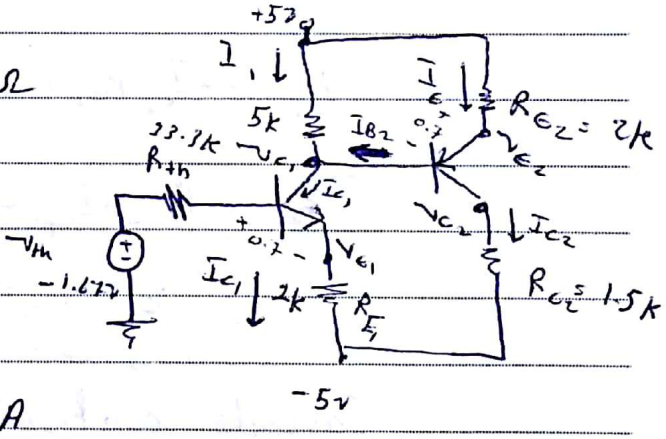


Ex Find currents & voltage at each node and V_{EC} & V_{CE}

$V_{BE(on)} = 0.7V$ / $\beta = 100$ / $V_{EB(on)} = 0.7V$

$V_{th} = 5\frac{R_2}{R_1+R_2} - 5\frac{R_1}{R_1+R_2} = 1.67V$

$R_{th} = R_1 // R_2 = 37.3K\Omega$



$I_{B1} = \frac{V_{th} - V_{BE_1(on)} + 5}{R_{th} + R_{E_1}(\beta+1)}$

$= \frac{-1.67 - 0.7 + 5}{33.3K + 2K(101)} = 11.2\mu A$

$I_{E_1} = 1.13A$, $I_{C_1} = 1.12mA$

$I_1 = I_{C_1} = I_{B_2} \rightarrow (1)$

$I_1 = \frac{5 - V_{C1}}{R_{C1}} = \frac{5 - V_{C1}}{5K}$ → (2)

$I_{B_2} = I_{E_1}/(\beta+1)$

$I_{E_2} = \frac{5 - V_{EB\,on} - V_{C1}}{R_{E_2}}$

$I_{B_2} = \frac{5 - 0.7 - V_{C1}}{(\beta+1)(2K)} \rightarrow (3)$

No.

$\Rightarrow \frac{5 - V_{C1}}{5K} = 1.12m = \frac{5 - 0.7 - V_{C1}}{(101)(2K)}$ Solve for V_{C1}

$V_{C1} = 0.482\,V$

$I_1 = \frac{5 + 0.482}{5K} = 1.096\,mA$

$I_{E2} = \frac{5 - 0.7 + 0.482}{2K} = 2.39\,mA$

$I_{B2} = \frac{2.39\,m}{101} = 23.2\,\mu A$

$I_{C2} = \frac{100}{101}(2.34M) = 2.37\,mA$

$V_{E1} = I_{E1} R_{E1} - 5 = -2.74\,V$

$V_{CE1} = V_{C1} - V_{E1} = -0.482 + 2.74 = 2.26\,V$

$V_{E2} = 5 - I_{E2} R_{E2} = 0.218\,V$

$V_{E2} = R_{C2} * I_{C2} - 5 = -1.45\,V$

$V_{EC2} = V_{E2} - V_{C2} = 1.67\,V$

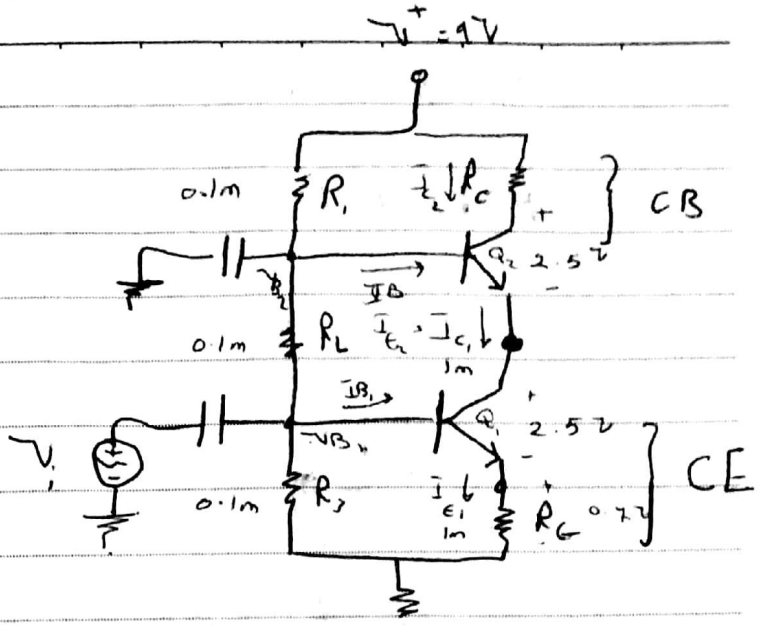
Cascode configuration:-

Compare to a single stage ckt high input impedance high O/P impedance high BW.

O/P of CE applied at input of ~~ckt~~ CB ckt

No.

ex 5.20 Design



$V_{CE_1} = V_{CE_2} = 2.5V$

$I_{C_1} \approx I_{C_2} = 1mA$

$I_{R_1} = I_{R_2} \approx I_{R_3} = 0.1mA$

$R_T = R_1 + R_2 + R_3$

$R_T = \frac{V^+}{I_{R_1}} = \frac{9}{0.1m} = 90K\Omega$

$\Rightarrow V_{B_1} = V_{RE} + V_{BE_1}(on) = 0.7 + 0.7 = 1.4V$

$\Rightarrow V_{B_2} = V_{RE} + V_{CE_1} + V_{BE_2} = 0.7 + 0.7 + 2.5 = 3.9V$

$\Rightarrow R_2 = \frac{V_{B_2} - V_{B_1}}{0.1m} = \frac{3.9 - 1.4}{0.1m} = 25K\Omega$

$\Rightarrow R_1 = R_T - R_2 - R_3 = 51K\Omega$

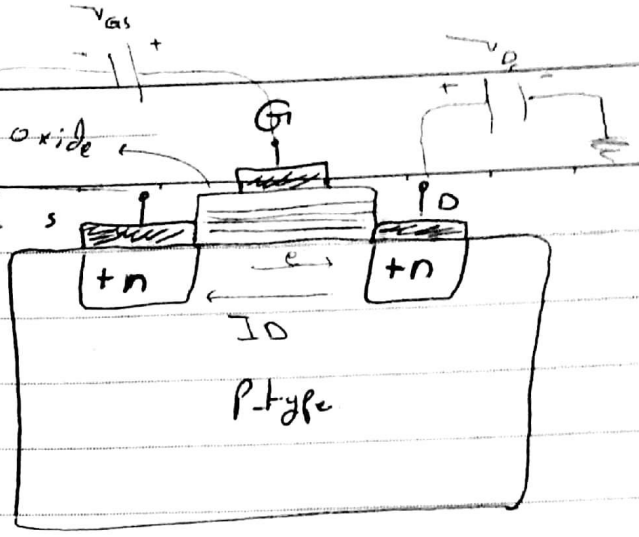
$R_E = \frac{V_{RE}}{1m} = \frac{0.7}{1m} = 0.7K\Omega$

$V_{C_2} = 2V_{CE} + V_{RE} = 5.7V$

$R_C = \frac{9 - V_{C_2}}{1m} = \frac{9 - 5.7}{1m} = 3.3K$

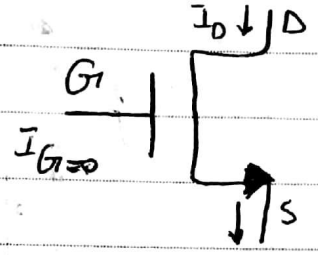
No.

MOSFET :-



N-channel MOSFET

≡ NMOS



- ~~mosfet~~ mosfet

⇒ ~~Mosfet~~ has three terminals

Source , Gate , Drain

S G D

~~Drain~~ size ←

* ~~Drain~~ Gate is isolated from source and Drain by oxide Layer ⇒ $I_G = 0$

* The space between Drain and source is called channel.

* ~~There~~ There are two types of MOSFETs :-

1 → Depletion :- has aphysical channel between source and drain. A small Voltage on Drain will cause current to flow in channel. Even if Voltage between Gate and Source is Zero ($V_{GS} = 0$)

⇒ the transistor is considered normally

No.

(2) ⇒ Enhancement : A channel is induced between Drain and Source once V_{GS} is higher than a voltage called Threshold Voltage V_{TH}

→ Both Enhancement & Depletion MOSFETs come in two types.

(a) N-channel MOSFET (NMOS), where electrons are carriers

(b) P-channel MOSFET (PMOS) where holes are the carriers

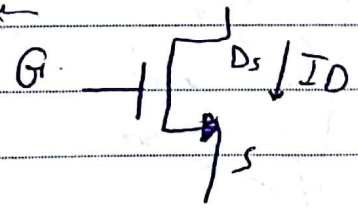
For Enhancement MOSFETs :-

V_{tN} is +ve for N mos

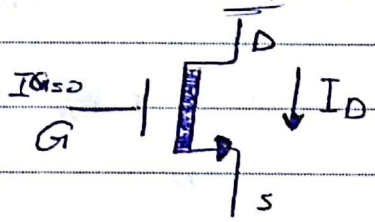
V_{tp} : -ve for P mos

Symbols for E mos & D-mos

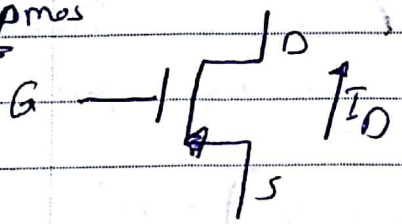
E-NMOS ←



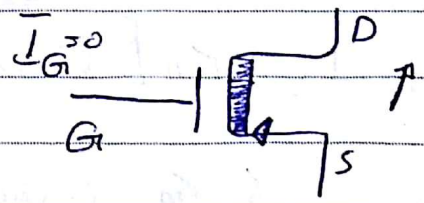
D-NMOS



E-pmos



D-pmos



Linear clipper clamper multivibrate

No.

BJT (no multi stage)

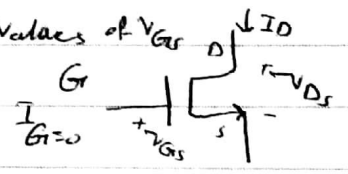
The Direction of the arrow indicates the direction of I_D.

* Since $I_G = 0$, $I_D = I_S$

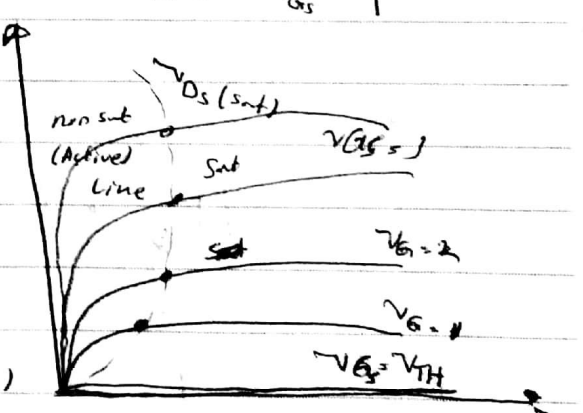
⇒ operation of Enhancement mosfet :-

if $V_{GS} > V_{th}$, achannel is created between source & Drain once V_{DS} is applied electrons will move from source to Drain ⇒ I_D will be from D to S.

⇒ Ideal current voltage characteristics : is a graph of I_D vs V_{DS} for different values of V_{GS}



$V_{DS(sat)} = V_{GS} - V_{TH}$



① $V_{GS} < V_{TH}$, NMOS is off

$I_D = 0$

② $V_{GS} > V_{TH}$, $V_{DS} < V_{DS(sat)}$

NMOS is linear (active, non-saturating region)

** ⇒ when linear, NMOS is used as a resistance

$$\Rightarrow I_D = K_n \left[2(V_{GS} - V_{TN}) V_{DS} - V_{DS}^2 \right] \longrightarrow (1)$$

* K_n : Conduction parameter

$K_n = \mu C_{ox} \frac{W}{L}$ → width of gate

→ Length of gate

A/V^2 وحدة

μ → Mobility

C_{ox} → Capacitance of oxide layer per unit area

No.

③ $V_{GS} > V_{TH}$, $V_{DS} > V_{DS(sat)}$ ⇒ NMOS is in saturation region And can be used as Amplifier.

$$\Rightarrow I_D = K_n (V_{GS} - V_{TH})^2 \rightarrow (2)$$

⇒ Ideally I_D is not a function of V_{DS} in Sat mode.

Analysis Techiques :-

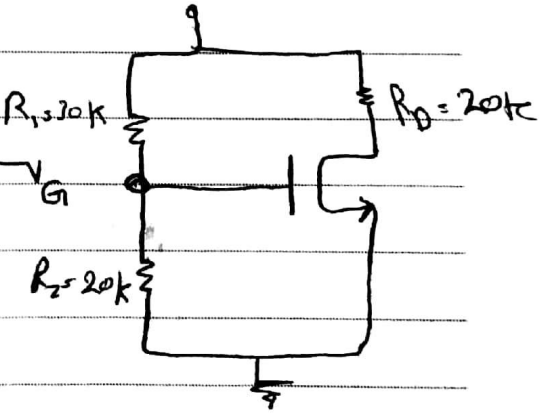
* Assume MOSFET in saturation region ⇒ use eq (2)
* perform Analysis :- I_D , V_{GS} , V_{DS} , $V_{DS(sat)}$
  → if $V_{DS} > V_{DS(sat)}$, then NMOS in Sat region and cait analysis.
  → if $V_{DS} < V_{DS(sat)}$, then NMOS in active region repeat for I_D(this) using eq ① & recalaute I_D, V_{GS}, V_{DS}

examples :-

$V_{IN} = 1V$, $K_n = 0.1\ mA/V^2$

① find V_{GS}, I_D, V_{DS} & P_D

② Draw the DCLL



$V_S = 0$

$$V_G = \frac{5 * 20}{20+30} = 2V$$

$V_{GS} = V_G - V_S = 2V$

No.

Assume S.t.

$$I_D = K_n (V_{GS} - V_{TH})^2$$

$$= 0.1m (2-1)$$

$$= 0.1 mA$$

$$\Rightarrow V_{DS} = 5 - I_D R_D = 5 - 0.1m\,20k$$

$$= 3V$$

$$V_{DS}(s.t) = V_{GS} - V_{TH} = 2 - 1 = 1V$$

$$V_{DS} > V_{DS}(s.t)$$

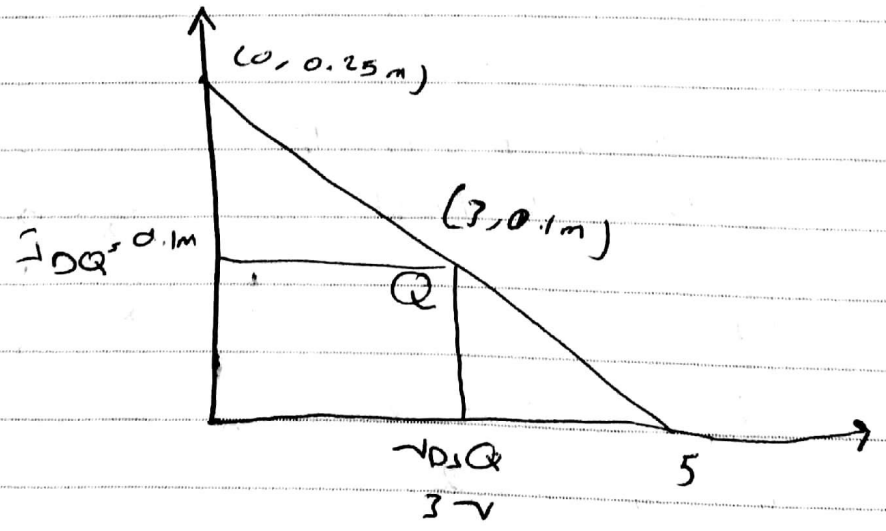
$3 > 1 \Rightarrow$ Assume correct

$$P_D = I_D V_{DS} = 0.1m * 3 = 0.3 mW \text{ watt}$$

$$\Rightarrow V_{DS} = 5 - I_D R_D$$

at $V_{DS} = 0$, $I_D = \frac{5}{R_D} = \frac{5}{20k} = 0.25mA$

at $I_D = 0 \Rightarrow V_{DS} = 5V$

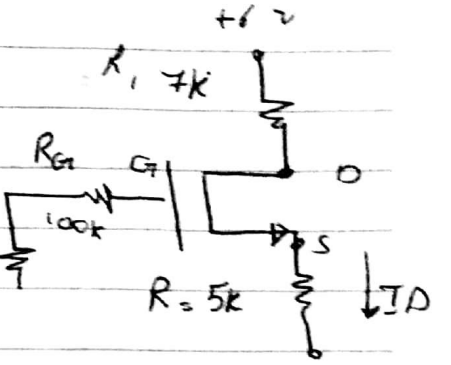


No.

Ex $V_{TN} = 1V$, $K_n = 0.25\,mA/V^2$

① find V_{GS}, I_D, V_{DS}, V_S, V_D, PD ?

② Draw DCLL & show Q-point



Assume Sat:-

① $V_G = 0$, Since $I_G = 0$

$V_S = I_D R_S - 6 = 5K(I_D) - 6$

$V_{GS} = 0 - [5K(I_D) - 6]$

$I_D = \dfrac{6 - V_{GS}}{5k} \rightarrow ①$

$I_D = K_N (V_{GS} - V_{TN})^2$

$= 0.25 (V_{GS} - 1)^2 \rightarrow ②$

eq① = eq② $\Rightarrow$ $\dfrac{6 - V_{GS}}{5k} = 0.25 (V_{GS} - 1)^2$

$\Rightarrow 1.25 V_{GS}^2 - 1.5 V_{GS} - 4.75 = 0$

$V_{GS} = -1.44 V$ ✗

$V_{GS} = 2.64 V$ Since +ve & bigger than V_{TN}

find I_D from eq① or ②

$I_D = \dfrac{6 - 2.64}{5} = 0.672\,mA$

$V_S = 5k(0.672m) - 6 = -2.64 V = -V_{GS}$

$V_D = 6 - I_D R_1 = 6 - 0.672m(7k) = 1.296 V$

$V_{DS} = V_D - V_S = 1.246 + 2.64 = 3.936 V$

or $V_{DS} = 6 + 6 - I_D(R_1 + R_S)$

$V_{DS(sat)} = V_{GS} - V_{TN} = 2.64 - 1 = 1.64 V$

$V_{DS} > V_{DS(sat)} \Rightarrow$ in saturation mode

No.

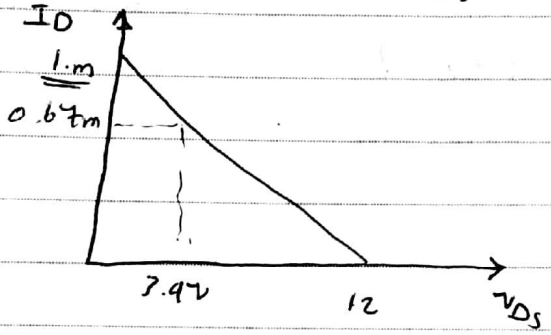
⇒ DCLL:

$$-6 + I_D R_D + V_{DS} + I_D R_S - 6 = 0$$

$$V_{DS} = 12 - I_D(R_D + R_S)$$

$$V_{DS} = 12 - 12k\, I_D$$

$$\text{Slope} = \frac{-1}{12k} = -\frac{1}{R_D + R_S}$$

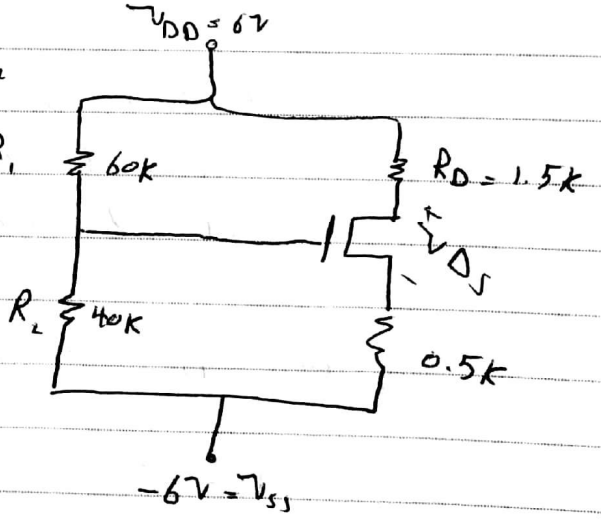


تذكر ⇒ power dissipated in MOSFET ⇒ $P_D = I_D V_{DS}$

Example:

$V_{TN} = 2V$, $K_n = 0.5mA/V^2$

Find V_{GS} , I_D , V_{DS} , V_D , V_S , P_D



Assume Saturated

$$V_G = \frac{6*40k}{100k} - \frac{6*60k}{100k} = -1.2V$$

$$V_{GS} = V_G - V_S$$

~~$V_S = 12 - (0.5k) I_D$~~

$$V_{GS} = -1.2 - V_S$$

No.

$V_S = (0.5k) I_D - 6$

$V_{GS} = -1.2 + 6 - (0.5k) I_D$

$V_{GS} = 4.8 - (0.5k) I_D$

$I_D = \frac{4.8 - V_{GS}}{0.5k} \rightarrow ①$

$I_D = k_n (V_{GS} - V_{TN})^2$

$= 0.5m (V_{GS} - 2)^2 \rightarrow ②$

eq ① = eq ②

$\frac{4.8 - V_{GS}}{0.5k} = 0.5m (V_{GS} - 2)^2$

$0.5 V_{GS}^2 - 7.6 = 0 \Rightarrow V_{GS} = 7.9V, -7.9V$

$I_D = \frac{4.8 - 7.9}{0.5k} = 1.8mA$

$V_{DS} = 6 + 6 - I_D (1.5k + 0.5k)$

$= 8.4V$

$V_{DS}(sat) = V_{GS} - V_T$

$= 7.9 - 2 = 1.9V$

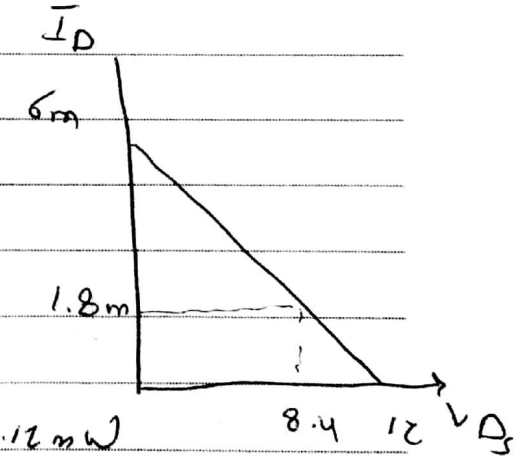
$V_{DS} > V_{DS}(sat) \Rightarrow$ Sat

$V_D = 6 - I_D (1.5k) = 3.3V$

$V_S = V_D - V_{DS} = 3.3 - 8.4 = -5.1V$

$\Rightarrow$ or $V_S = I_D R_D - 6$

$P_D = I_D V_{DS} = 1.8m (8.4) = 15.12mW$



KVL Ckt 2 - $-6 + I_D(R_D) + V_{DS} + I_D R_S - 6 = 0$

output

$V_{DS} = 12 - I_D (R_D + R_S)$

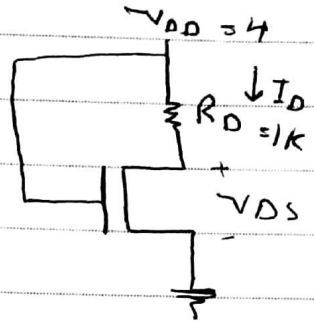
at $I_D = 0$, $V_{DS} = 12$

at $V_{DS} = 0$, $I_D = 6m$

No.

Problem 7.27 :-

$V_{TN} = 0.2V$, $K_n = 0.25\ mA/V^2$



Find Q point and DC

Assume Saturation

$V_{GS} = V_{DD} = 4V$, $V_S = 0$

$V_{GS} = 4 - 0 = 4V$

$$I_D = k(V_{GS} - V_{TN})^2 = 0.25m\,(4 - 0.8)^2$$

$$= 2.56mA$$

$\Rightarrow$

$$V_{DS} = V_{DD} - I_D R_D = 4 - 2.56m\,(1K) = 1.44V$$

$$V_{DS(sat)} = V_{GS} - V_{TN} = 4 - 0.8 = 3.2V$$

$V_{DS(sat)} > V_{DS}$ $\Rightarrow$ non-saturating (Lin)

repeat

$$I_{D(lin)} = K_n\left[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2\right]$$

$$= 0.25m\,(2(4 - 0.8)V_{DS} - V_{DS}^2 \longrightarrow (1)$$

Also $\Rightarrow$ $I_D = \dfrac{V_{DD} - V_{DS}}{R_L} = \dfrac{4 - V_{DS}}{1k} \longrightarrow (2)$

eq(1) = eq(2) Solve for V_{DS}

$V_{DS} = 1.88V$ ✓

$$I_D = \frac{4 - 1.88}{1K} = 2.12mA$$

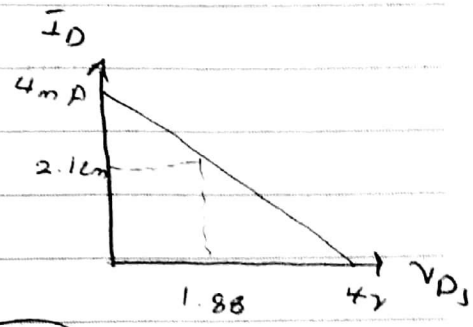
3.38 problem

No.

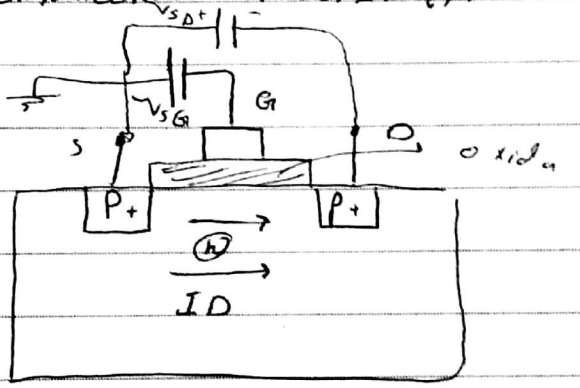
$V_{DS} = V_{DD} - I_D R_D = 4 - 1K(I_D)$

at $I_D = 0$, $V_{DS} = 4$

at $V_{DS} = 0$, $I_D = 4m$



3.104 P-channel Enhancement MOSFET (PMOS)



I_D move from S to D.

For PMOS to Conduct $V_{SG} > -V_{TP}$

V_{TP} -Ve Value

⇒ operation modes :-

① $V_{SG} < -V_{TP}$ PMOS off $I_{DP} = 0$

② $V_{SG} > -V_{TP}$, $V_{SD} < V_{SD(sat)}$

PMOS Lin.

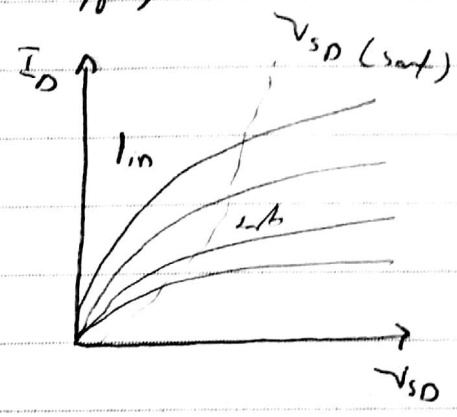
$I_{DP(Lin)} = K_P [2(V_{SG} + V_{TP}) V_{SD} - V_{SD}^2]$

No.

② $V_{SG} > -V_{TP}$, $V_{SD} > V_{SD(sat)}$

PMOS Sat

$I_{DD(sat)} = k_p (V_{SG} + V_{TP})^2$



"هذا عمل بشري وقد تحتمل الصواب والخطأ"

دعواتكم.

Bawi & Alaa Alham