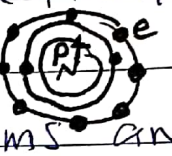
Electronics I .... 1104092 40 .... Dr. Hadi

CH.1: Semiconductor Materials and Diodes

Introduction: Most electronic devices are fabricated using Semic. materials along with conductors and Insulators. Silicon is the most Common Semic. material used for electronic devices and Integrated ccts. fabrication, due to its noval characteristics Compared to other Semic. materials.



*However, all materials Consist of Atoms and any Atom Contains nucleus which have positive charge Protons and nuetral neutrons. The Atom also has electrons distributed in orbits at different distance From the nucleus. Electrons at the outermost orbit are Called Valence electrons Materials in the periodic table are classified according to the No of electrons in the external orbit. For exA. Silicon From group 4, has 4e in ext. orbit

*In general, in any Atom, electrons Can be in one of the two-band: Valence band" and "Conduction band" as Shown in the energy band diagram Shown in Fig.1: where:

Ev: The Max. energy of the Valance band

Ec: The minimum energy of Conduction band.

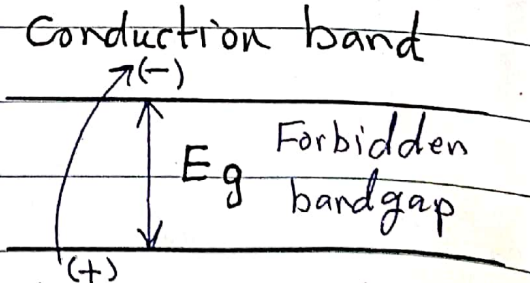


Fig.1 "Energy band diagram"

Eg: "bandgap energy": The minimum energy required by electron in Valance band to break the bond and move to Conduction band. The relation between these levels are: $E_c = E_v + E_g$ (eV).

* In "Forbidden bandgap" there is No electrons.

*"classification of Materials"

Materials are classified into:

1) Conductors: they are charaterised by:

a) Very large of free electrons in conduction band.

b) Very low resistivity ρ (Ω.Cm) and Very high conductivity ($\sigma = \frac{1}{\rho}$) (Ω.Cm)$^{-1}$. For Copper $\rho_{Cu} = 10^{-6}$ Ω.Cm

c) No bandpap energy ($E_g = 0$). In Conductors V.B & C.B are overlapped.

2) Insulators: The main c/cs. are: "c/cs: Characteristics"

a) No electrons in conduction band (at Room Temp).

b) Very high resistivity & Very low conductivity.

" For mica $\rho_{mica} = 10^{12}$ Ω.cm (at Room Temp).

c) Eg is in the range (3 ⟶ 6) eV.

3) Semiconductors: The main c/cs. are:

a) group 4 materials: (have 4 electrons in external orbit.

b) Resistivity and conductivity levels are between conductors & Insulator levels. At Room Temp.
$\rho_{Si} = 5 \times 10^{4}$ Ω.Cm, $\rho_{Ge} = 50$ Ω.Cm.

c) The bandgap energy Eg, are Around 1 eV
$E_{gSi} = 1.12$ eV, $E_{gGe} = 0.66$ eV, $E_g(GaAs) = 1.42$ eV

d) The electrical characteristics of Semic. materials can be greatly changed by "doping" adding atoms from other groups to Semiconductors. mainly adjecent group "3 or 5". resulting in "producing" new Semic. material called "Dopped Semic" or "Extrinsic Semic".

"Semiconductors"

Intrinsic Semic. "نقي"	Extrinsic Semic. "مطعم / مشوب"
"Pure Semic"	"Impure Semic."
"Intrinsic Semic"	"Extrinsic Semic" "غير نقي"

Intrinsic Semiconductors

Pure Semic. material "without any impurities", They can be elemental Semic - such as Silicon Si or Ge or Compound Semic.. such as GaAs (group 3 & 5).

For example Silicon: The two-dimentional represent. of Si-crystal is shown in Fig. 2

a) At T = 0 K (Kelven) all Valance electrons are in Valance energy band.

b) For T > 0 K, Valence electrons may gain enough thermal energy, break covalent bond and move away from original position. Any electron gain minimum energy "Eg" move to conduction band and called free electron. flow of these electrons in C.B generates Current a Current.

pure Si Crystal

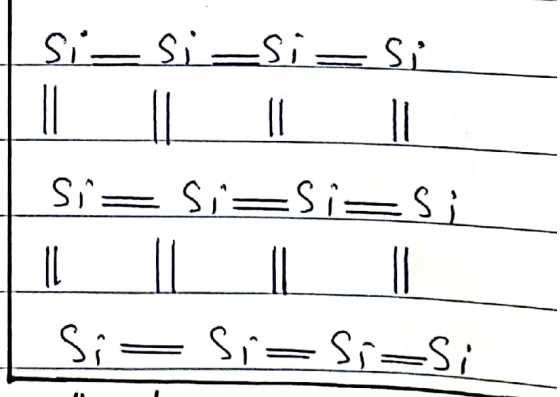


Fig. 2 "Silicon Crystal"

Any electron moves. leaves an empty space with +ve charge called "hole". the electron with a certain level and adjucent to empty space may move into that position as shown in Fig.3. This appear as if a +ve charge is moving. The movement of electrons and holes in the Semiconductor is the Current.

- The Concentration of electrons and holes ($\#/Cm^3$) is a very important parameters of a Semic. material because it is directly influnces the magnitude of Current.

"Movment of e & hole

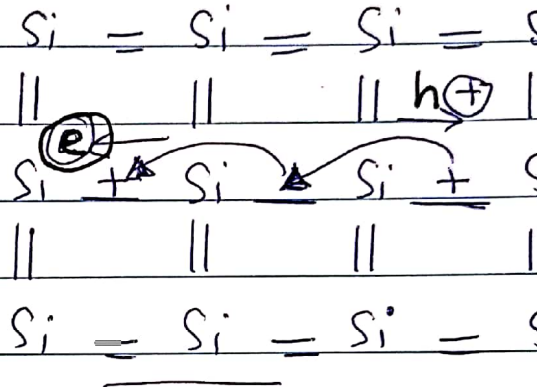


Fig. 3

movement of Holes

- At a certain temp. the Concent. of electran & hole in an intrinsic Semic. is called "Intrinsic Carrier Concentration" and is given by:

$$n_i = B \cdot T^{3/2} e^{\frac{-Eg}{2kT}} \quad (\#/Cm^3)$$ where:

B: a coefficient related to Semic. material ($Cm^{-3} K^{-3/2}$)

T: Temp. in K (Kelven).

Eg: bandgap energy (eV)

k: Boltzmann's Constant (86×10^{-6} eV/K).

EXAMPLES: Calculate intrinsic Carrier Concent. for Si at T = 300 K. Given: $Eg_{Si} = 1.1$ eV, $k = 86 \times 10^{-6}$, $B_{Si} = 5.23 \times 10^{15}$

$$n_i = 5.23 \times 10^{15} \cdot (300)^{3/2} \cdot e^{\frac{-1.1}{2 \times 86 \times 10^{-6} \times 300}} = 1.5 \times 10^{10} / Cm^3$$

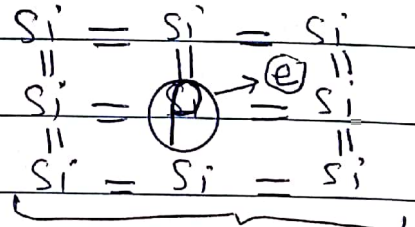
This N_o: represent concent. of electrons & holes It seems Large but it is Low Compared to No of Silicon atoms in Cm^3 of pure Silicon which is $[5 \times 10^{22}\ Atom/Cm^3]$. To increase electrons and hole Concentration and enable Large Current to flow in Semic, we have to add controlled amounts of Certain impurities. (Atoms from adjucent group of Semic) mainly group three or group Five) and produce dopped Semic or Extrinsic Semiconductor.

Extrinsic Semiconductor

"Pure Semic + impurities"

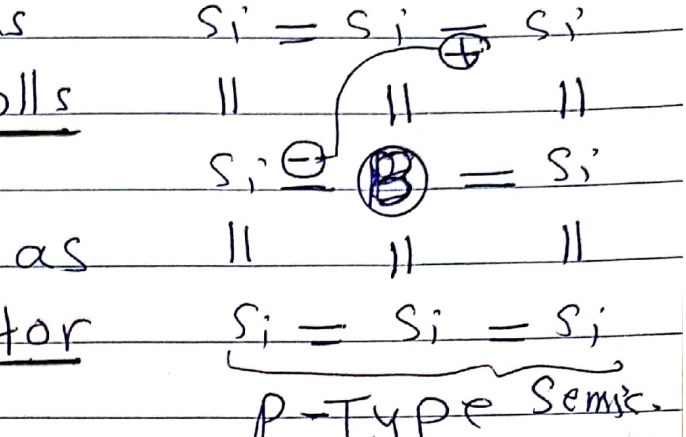
1) n-type Semiconductor: "pure Semic + group V (Five) Atom

a) pure Semic + group Five Atoms such as phosphorus.
b) Contain an excess No. of electrons.
c) It is electrically neutral.
d) The phosphour atom is called Donar Atom.
e) The process is called Doping.
f) The Concentration of phosphour Atom (N_d) is the dopping level.
g) the letter (n) refers to negative charge of electron. which are the majority Carriers n-type in n-type material.
h) The majority Carriers are Electrons and minority Carriers are Holes



2) P-type Semiconductor

a) Pure Semic + group 3 Atoms
b) Contain an excess No of holls
c) It is electrically neutral
d) The group 3 Atom (Such as "BORON") is called Acceptor Atom.



e) The concentration of BORON Atom is the doping level (N_a).
f) The letter p- refers to positive charge of holes which are the majority Carriers
g) The majority Carriers are "Holes" and the minority Carriers are "Electrons"

"The doping process, which allows to control electrons and holes Concentration in extrinsic Semiconductor, determine the conductivity and Current in the Semiconductor."

"Electrons and Hole Concentration in extrin. Semic"

The fundemental relationship between electron and hole Concent. at thermal equilibrium is given by: $n_o \cdot P_o = n_i^2$

n_o : T.E concent. of electron.
P_o : T.E " = Hole
n_i : Intrinsic Carrier Concent.

i) For n-type: $N_d \gg n_i$ ($N_d > 10^{14}$), $n_i = 1.5 \times 10^{10}$

$n_o \cong N_d$, $P_o = \frac{n_i^2}{N_d}$

2) For P-Type: $N_a > n_i$ So:
$P_o \cong N_a$ and $n_o = \frac{n_i^2}{N_a}$.

EXA: Calculate thermal electron and hole Concentration for a Silicon (at T = 300K) doped with a phosphoure at a Concentration of $N_d = 10^{16}\ Cm^{-3}$. Given $n_i = 1.5 \times 10^{10}\ Cm^{-3}$.

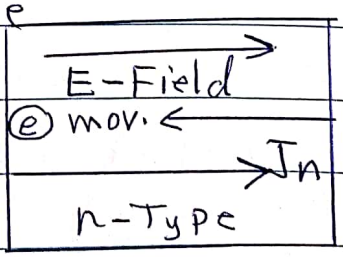
* The resulting material is n-type Semic.
electron Concent. $n_o \cong N_d = 10^{16}\ Cm^{-3}$
Hole $\Rightarrow$ $P_o = (n_i^2/N_d) = \frac{(1.5\times10^{10})^2}{10^{16}}$
$P_o = 2.25 \times 10^{4}\ Cm^{-3}$.

* Recalculate minority & majority Carrier Concent. If the Silicon is doped with Boron at a Concentration of $10^{17}/Cm^3$. What is the resulted material?
→ The resulted material is P-Type material.
majority Carriers are Holes, hole Concent $\cong N_a = 10^{17}\ Cm^{-3}$
minority are Electrons, electron Concen $= \frac{n_i^2}{N_a}$
∴ e-Concent $= (1.5\times10^{10})^2/10^{17} = 2.25\times10^{3}\ Cm^{-3}$.

Currents in Semiconductors

Current in Semic. is the flow of Carriers (electrons & hole) in the Semic. There are two types of Current.

1) Drift Current density: movement of Carriers Caused by an electric field. where this field will produce an force, which will cause a movement of Carriers. For n-Type shown: electrons move opposite to E-Field, J_n: opposite to electron movement.



* because e-charge is -ve it move opposite to E-Field

The Convential direction of drift Current density is opposite to electron movement!!! *

The drift Current density carried by electron is:

$J_n = e \cdot n \cdot \mu_n \cdot E \ (A/Cm^2)$

e: electron charge. (Colomb → A/s)

n: electron Concentration $(\#/Cm^3)$

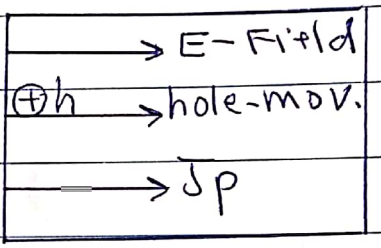
μ_n: electron mobility $\left(\frac{Cm^2}{V \cdot S}\right)$, E → Electric field (V/Cm)

"mobility is a parameter indicating how well Carriers can move in a Semic. For Silicon $\mu_n = 1350\ Cm^2/V \cdot s$"

* For P-type with a Large number for Holes

Since hole has +ve charge, holes move in the Same direction of E-Field

$J_p = e \cdot p \cdot \mu_p \cdot E \ (A/Cm^2)$



P-Type

J_p: Hole Current density (A/Cm^2)

e: electron charge (Colomb).

p: Hole Concentration $(\#/Cm^3)$

μ_p: " mobility $(Cm^2/V \cdot S)$ [For Si $\mu_p \approx 450\ (Cm^2/V \cdot S)$]

E: Electric field (V/Cm).

*NOTE: The drift Current in N-Type & P-type is in the direction of E-Field"

* The mobility of electron is three times that of Holes

The total drift Current density: $J = J_n + J_p \ (A/Cm^2)$

$J = e \cdot n \cdot \mu_n E + e \cdot p \cdot \mu_p \cdot E = \sigma \cdot E = \frac{1}{\rho} E$

where: $\sigma = e \cdot n \cdot \mu_n + e \cdot p \cdot \mu_p$, σ = Conductivity $(\Omega \cdot Cm)^{-1}$

ρ: resistivity of Semic. $(\Omega \cdot Cm)$.

6. Can be controlled by controlling electron & hole Concentration i.e by controlling doping level, and that enables us to fabricate the varienty of electronic devices. $I = J.A$ (Amp) where A: Cross-sectional Area (Cm^2)

Example 2: ① Calculate drift Current density For a Si doped with arsenic atoms at Concent. oF $8\times10^{16}\ Cm^{-3}$. and Subjected to E-Field oF 100 V/Cm. Given: $\mu_n = 1350\ Cm^2/V.S$ & $\mu_p = 480\ Cm^2/V.S$, $n_i = 1.5\times10^{10}\ Cm^{-3}$.

② IF the area oF the semic is $0.01\ Cm^2$ → Calculate I?

$J = J_n + J_p \Rightarrow e.n\mu_n E + e.p.\mu_p.E$

electron Concent. $n = N_d = 8\times10^{16}\ Cm^{-3}$

Hole $p = \frac{n_i^2}{N_d} = (1.5\times10^{10})^2/8\times10^{16} = 2.5\times10^{3}\ Cm^{-3}$

Since $n \gg p$ → So Conductivity $\sigma = e.n.\mu_n$

$\sigma = 1.6\times10^{-19}\times8\times10^{16}\times1350 = 19.44\ (\Omega.Cm)^{-1}$

$J = \sigma.E = 19.44\times100 = 1944\ A/Cm^2$

$I = J.A = 1944\times0.01 = 19.44\ Amp.$

2) Hole drift Current density (A/Cm^2)

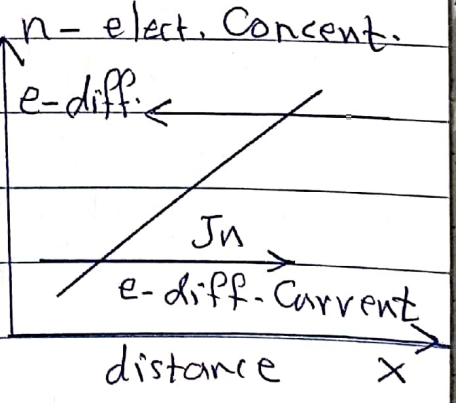
" flow oF Carriers due to Variation of Concentration where Carriers move from high Concentration region to low Concentration region.

a) Electron diff. Current Jn:

Consider e- Concent. Shown:

electrons move in -ve x-direction

So Conventional direction oF Jn is in +ve x-direction.



The electron diffusion Current density Jn is given by the following equation

$J_n = e \cdot D_n \cdot \frac{dn}{dx}$ (A/cm^2)

J_n: electron diff Current. (A/cm^2)

e: electron charge (C)

$\frac{dn}{dx}$: gradiant of electron concentration

D_n: electron diffusion coefficient (cm^2/s)

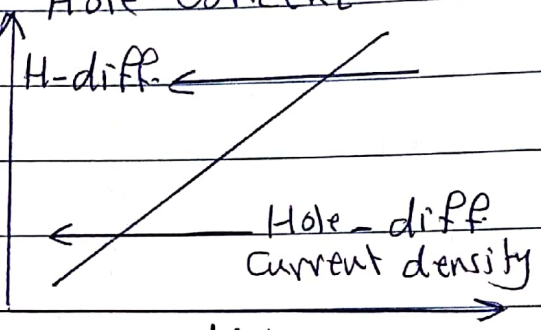
b) Hole diffusion Current density : J_p.

Consider the Hole Concent. versus distance shown.

Holes move in -ve x-direction p

So the conventional direction of J_p also in -ve x-direction

$J_p = -e \cdot D_p \cdot \frac{dP}{dx}$ (A/cm^2)



D_p: Hole diffusion coefficient (cm^2/s)

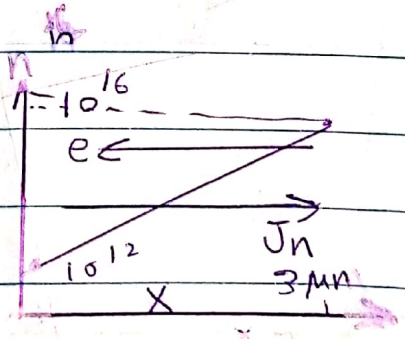
(dP/dx): gradiant of Hole concentration.

*NOTE: The direction of this Current (Diff. Current).

is +ve when J in +ve x-direction.

-ve ≤ J ≤ -ve ≤ ≤.

Example 3: For a Si at T = 300k, the electron Concent. varies from $n = 10^{12}\ cm^{-3}$ to $n = 10^{16}\ cm^{-3}$ over a distance from x = 0 μm to x = 3. Calculate J_n and indicate direction.



Given: $D_n = 30\ cm^2/s$

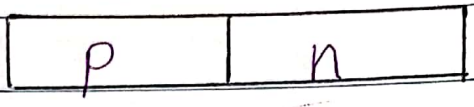
$J_n = e \cdot D_n \cdot \frac{dn}{dx}$

$= 1.6 \times 10^{-19} \times 30 \frac{(10^{12} - 10^{16})}{(0-3) \times 10^{-4}} = 16\ A/cm^2$

The pn Junction

"It is a single Cryst. Semic. material with one region doped to be p-type and the adjacent regn. doped to be n-type".

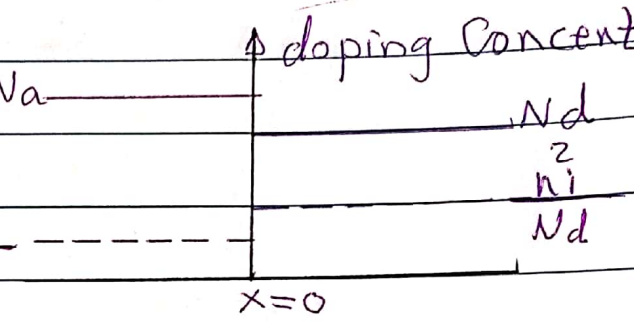
Fig. 1



1) Equilibrum pn-Jn.

(PN Jn under No biase)

- Due to difference in Concent. electrons move from (n → P) and Holes move from (P → n)
- Each electron moves, leaves +ve ion and each hole accept electron leaves -ve ion. (shown in Fig. 2). This will establish depletion region which has No Carriers.
- An electric field will be established directed from (+ to −) → E which will be resulted in an induced voltage called "built-in" voltage (V_{bi}) with polarity and is given by:



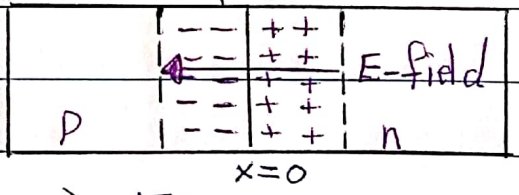
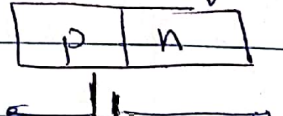


Fig. 2



$$V_{bi} = \frac{kT}{e} \ln\left(\frac{N_a \cdot N_d}{n_i^2}\right)$$

$$= V_T \ln\left(\frac{N_a \cdot N_d}{n_i^2}\right) \quad \text{where } V_T = \frac{kT}{e} \text{ (Thermal Voltage)}$$

Where: k: Boltzmann's const., T: absolute temp., e: electron charge, N_a, N_d: Acceptor and Donar Concent. respectively.

At T = 300k, $V_T \simeq 0.026\,V$

*Note: The movement of electrons and holes will be stopped when the force produces by E-Field balances the force produced by the density gradiant.

* The voltage V_{bi} can not be measured by voltmeter and does not drive a current in the Jn.

EXAMPLES:

a Pn Jn (Si) at T = 300K, doped with $N_a = 10^{16}\ Cm^{-3}$ and $N_d = 10^{17}\ Cm^{-3}$. Given $n_i = 1.5 \times 10^{10}\ Cm^{-3}$, $V_T = 0.026\ V$. Calculate V_{bi} (built-in potential barriee).

$$V_{bi} = 0.026 \ln \frac{10^{16} \cdot 10^{17}}{(1.5 \times 10^{10})^2} = 0.757 \text{ Volt}.$$

2) Reverse-biased pn Junction.

"Reverse bias: Connecting +ve terminal of D.c to n-type and -ve terminal to p-type." as shown in Fig. 3

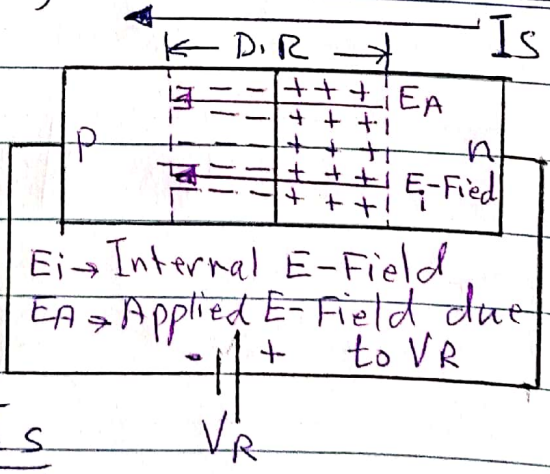
* In this case, the biasing will force the carriers to move away from the Jn. (Due to its repeltion force) and widening D.R. No maj. Carrent will cross the Jn.

"only very Small Current due to minority Carriers will flow from (n → P) called "Reverse Saturation Current Is"

* For Silicon pn Jn. the value of Is is in the range of $(10^{-18} \rightarrow 10^{-12})$ A.

*(Is is temp. dependant). *(Is does not depend on V_R)

biasing: a process of applying D.C voltage to the device to force to work at a certain mode of operation.



The reverse-biased pn Jn. can be used as Voltage-controlled capacitance called "Junction Capacitance" or "depletion layer Capacitance" and is given by:

$$C_j = C_{j0}\left(1+\frac{V_R}{V_{bi}}\right)^{-\frac{1}{2}} \quad \text{or} \quad C_j = \frac{C_{j0}}{\sqrt{1+\frac{V_R}{V_{bi}}}} \text{ (farad)}$$

where C_{j0} is zero-bias cap. (C_j when $V_R = 0$).

V_R: reverse voltage, V_{bi}: built-in voltage

$\left(C_j \propto \frac{1}{V_R}\right)$.

* The Junctions fabricated specifically for this purpose are called "Varactor Diodes" which has many applications.

EXAMPLE

Consider a Si pn Jn. at $T = 300k$.

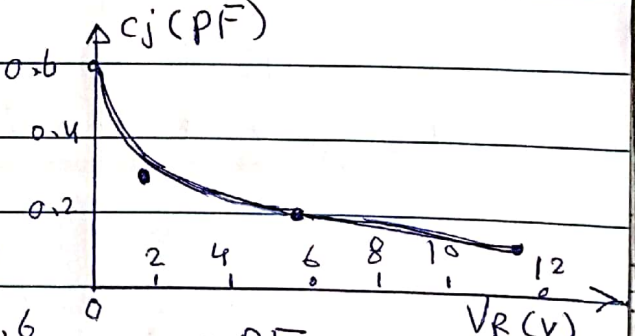
With $N_a = 10^{16}\ cm^{-3}$, $N_d = 10^{17}$ and given

$n_i = 1.5\times10^{10}\ cm^{-3}$, $C_{j0} = 0.6pF$, $V_T = 0.026V$

1) Calculate C_j at:

$V_R = 2.3V$, $V_R = 6V$, $V_R = 11.5V$

2) Sketch C_j versus V_R graph.



$$V_{bi} = V_T \ln\frac{N_a N_d}{n_i^2} = 0.75V$$

$$V_R = 2.3V,\ C_j = \frac{0.6}{\sqrt{1+2.3/0.75}} = \frac{0.6}{\sqrt{4}} = 0.3pF.$$

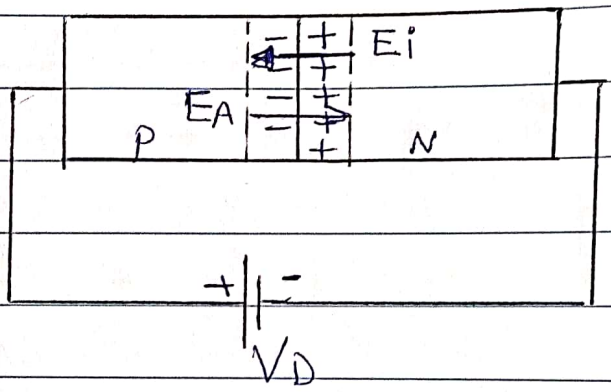
$$V_R = 6V,\ C_j = \frac{0.6}{\sqrt{(6/0.75)+1}} = \frac{0.6}{\sqrt{9}} = 0.2pF.$$

$$V_R = 11.5V,\ C_j = \frac{0.6}{\sqrt{1+\frac{11.5}{0.75}}} = \frac{0.6}{\sqrt{16}} = 0.15pF$$

3) Forward-biased pn Junction:

"Forward biase means Connecting +ve terminal of D.C to p-side and -ve terminal to n-side".

- In this case, the Carriers (majority) are forced to Cross the Jn. (Due to repelling force by E-Field)
- A Current will flow in the pn Jn. directed Conventionaly from (p → to → n) and Carried by the majority Carrier. It is I_D and is given by:



I_D

$$I_D = I_s e^{\frac{V_D}{nV_T}} \quad (mA).$$

I_s: Reverse Sat. Current

V_D: applied F.W Voltage

V_T: thermal Voltage

n: ideality factor

$n=1$ → High Current level

$n=2$ → Low " "

Ideal Voltage-Current Relationship

The relation related current to voltage in the pn Jn. is in general given by:

$$I_D = I_s\left[e^{\frac{V_D}{nV_T}} - 1\right]$$ parameters are defined above

When V_D is +ve → PN Jn → F.W

V_D is -ve → pn Jn → Rev.

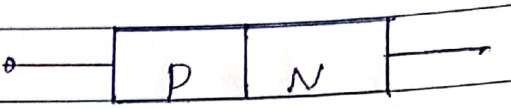
EXAMPLE Find I_D for a pn Jn. with $I_s = 10^{-14}$ A, $n=1$, $V_T = 0.026$ V For $V_D = 0.7$ V, $V_D = -0.7$ V

For $V_D = 0.7$ V, $I_D = 10^{-12}\left(e^{\frac{0.7}{0.026}} - 1\right) \approx 4.93$ mA

For $V_D = -0.7$ V, Jn. is Rev. $I_D \approx -I_s = -10^{-12}$ A.

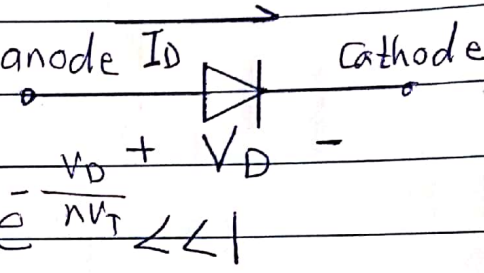
pn Junction Diode

The simplest electronic device. It is a pn Jn. fitted in a suitable case with two conducting leads for connection with other cct. elements. Diode is a nonlinear element. idealy it is short cct. when it is Forward-biased an it is an open-cct. when it is reversed-biased. The symbol is shown.



The general diode equation is:

$$I_D = I_S\left[e^{\frac{V_D}{nV_T}} - 1\right]$$



when V_D is +ve, $e^{\frac{V_D}{nV_T}} \gg 1$

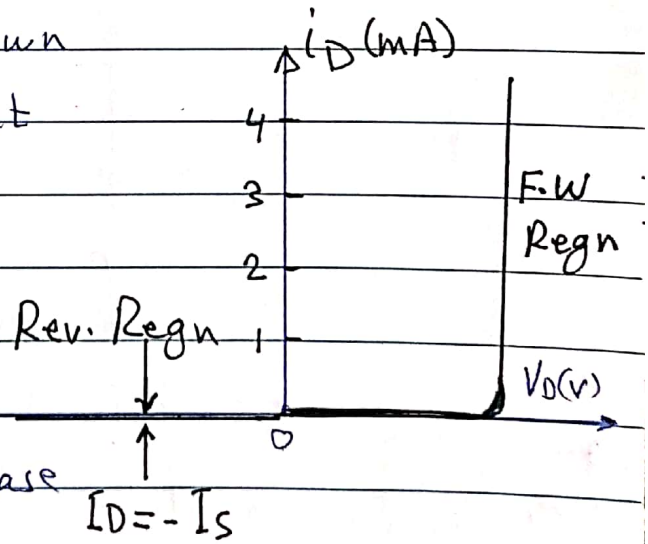
$I_D = I_S e^{\frac{V_D}{nV_T}}$ (diode is F.W)

when V_D is (-ve), diode is Rev., $e^{-\frac{V_D}{nV_T}} \ll 1$

So $I_D \approx -I_S$ (very very small).

i.e when Diode is F.W, I_D is exponentionaly related to V_D, and when it is Rev, $I_D \approx -I_S \approx$ zero.

The I-V characteristics is shown



I_S: is Reverse Saturation Current

I_S: is temp. dependant.

also depends on doping level and cross-sectional area.

I_S: depend on n_i.

I_S doubles for each 5°C increase in Temp.

For Germanium I_S is higher than that For Si because n_i For Ge is greater than n_i For Si

** If I_S is 20nA at 38°C Find I_S at 68°C

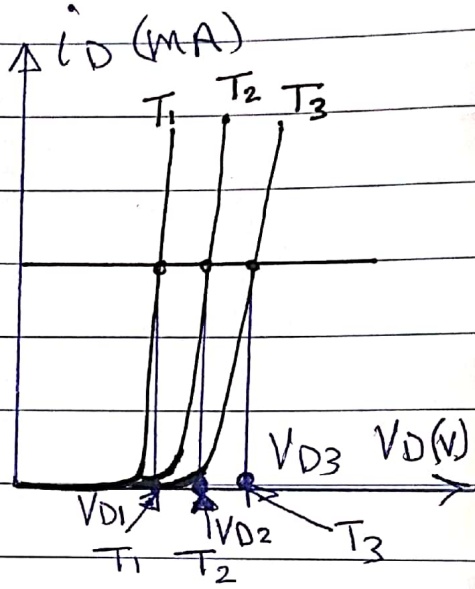
$$I_{S(68)} = I_{S(38)} \cdot 2^{\frac{\Delta T}{5}} = 20 \cdot e^{\frac{30}{5}} = 20 \times 2^6 = 1280\,nA$$

Effect of Temp. on diode I-V characteristics:

When diode is F.W, then $I_D = I_s e^{\frac{V_D}{nV_T}}$ and so $V_D = nV_T \ln \frac{I_D}{I_s}$. i.e $V_D \propto \frac{1}{I_s}$ but $I_s \propto T$ so $V_D \propto \frac{1}{Temp}$. i.e as Temp ↑, V_D ↓.

For Silicon as T ↑ by 1C°, V_D reduces by 2mV

"In general: For the Same Current level, as T increase V_D decreases"



* a Si diode has $I_D = 5mA$, $V_D = 0.65V$ at $T = 60°C$. Find V_D at $T = 70°C$ and $I_D = 5mA$.

$\Delta T = 70 - 60 = 10°C$

$\therefore V_{D2} = V_{D1} - (\Delta T \times 2)$

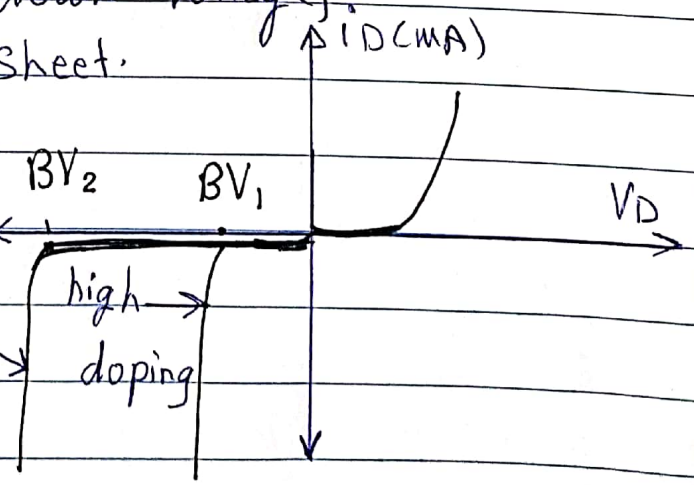
$= 0.65V - (10 \times 2)mV$

$= 0.63V$

Breakdown Voltage:

We Can't increase the reverse voltage For the diode in reverse biasing. At a certain Value of reverse voltage the diode may be damaged and burnout. The reverse voltage at which the diode is damaged is called "Breakdown Voltage V_{BR}" and it is given in data sheet.

"V_{BR}" $\propto \frac{1}{\text{doping concentration}}$.



* It must be avoided in biasing diode *

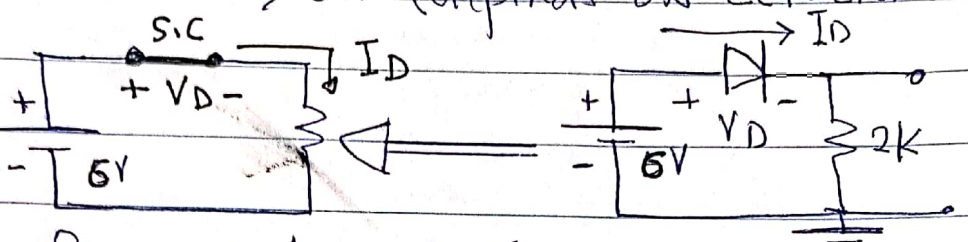
Diode D.C model "equivalent cct"

1) Ideal Diode:

a) when it is F.W ⇒ It is represented by short-cct. with $V_D \leq 0$ and $I_D > 0$. (depends on cct. elements)

$V_D = 0\ V$

$I_D = \frac{5V}{2k} = 3\ mA$



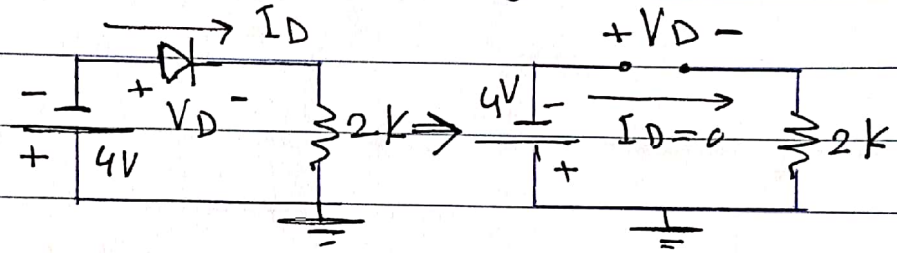
b) when It is Reversed biased: It is represented by open-cct. with $V_D < 0$ and $I_D = 0$.

$I_D = 0$

$4V + V_D + I_D \cdot 2k = 0$

but $I_D = 0$,

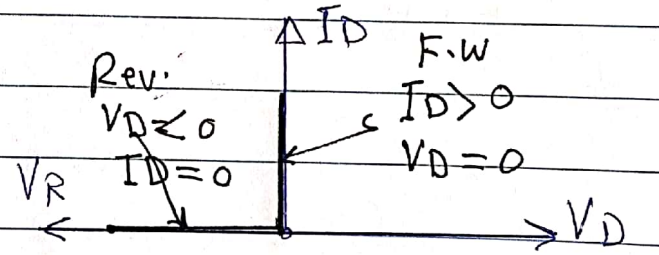
so $V_D = -4V$



2) Nonideal diode "Real diode"

For nonideal diode the (I-V) relation is:

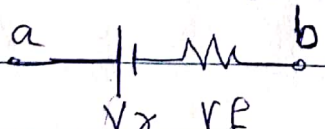
$$I_D = I_s\left[e^{\frac{V_D}{nV_T}} - 1\right]$$



ideal diode c/c.

a) when it is F.W

(i) For $V_D > V_\gamma$, it can be represented by a Voltage Source V_γ and resistance r_f:

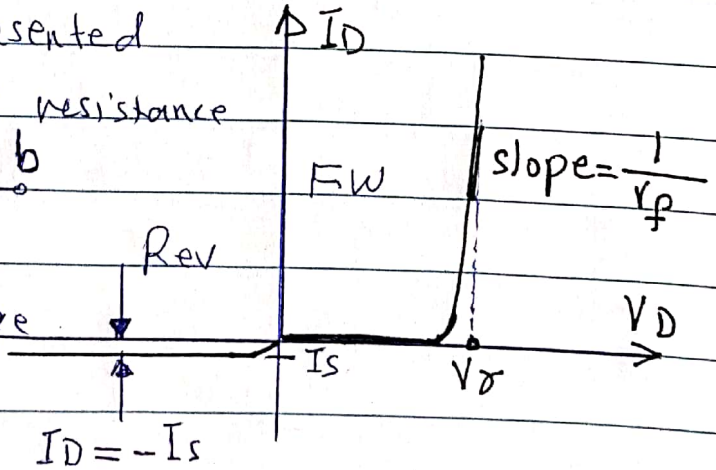


where:

V_γ: turn-ON or (Cut-in) Voltage

r_f: Forward diode resistance.

"both of them are given"



ii) For $V_D < V_\gamma$, it is represented by open-ckt.

b) when it is Reverse ~~voltage~~ biased. then $I_D = -I_S$ but I_S is very Small, So it can be represented by open ckt. ($I_D = 0$).

* This model is called "piecewise linear model"

Notice:

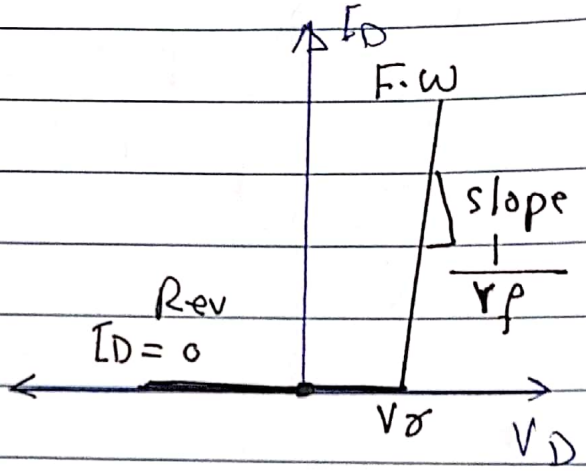
*When real diode is "ON". $I_D > 0$

$V_D = V_\gamma$ (when $r_f = 0$)

$V_D = V_\gamma + I_D r_f$ (when $r_f \neq 0$).

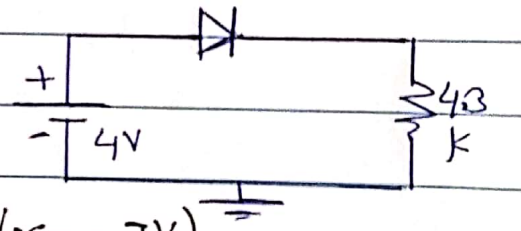
For Si diode $V_\gamma \approx (0.6 \rightarrow 0.7)V$

For Ge $V_\gamma \approx (0.2 \rightarrow 0.3)V$



EXAMPLE

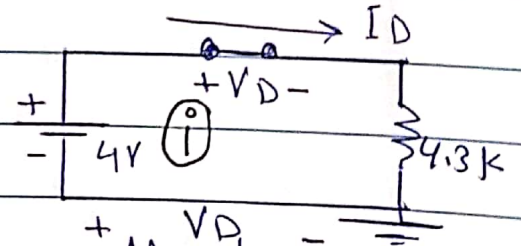
For the ckt. shown calculate I_D, V_D and power dissipated in diode D when the diode is: i) ideal, ii) has $r_f = 30\Omega, V_\gamma = 0.7V$) iii) has $V_\gamma = 0.7V$, $r_f = 0$.



Since the diode is Forward"

i) $V_D = 0$, $I_D = \frac{4V}{4.3k} = 0.93mA$

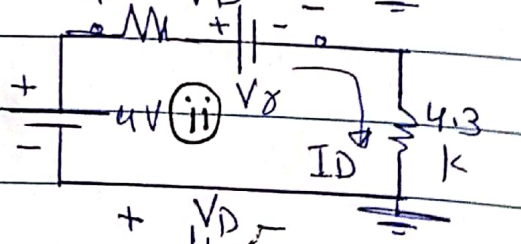
$P_D = I_D \cdot V_D = 0$



ii) $I_D = \frac{(4-0.7)V}{r_f + 4.3k} = \frac{3.3V}{4.33k} = 0.7621$ mA

$V_D = V_\gamma + I_D r_f = 0.7228V$

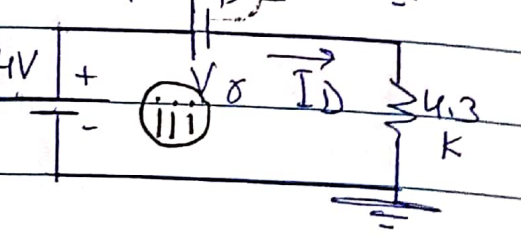
$P_D = I_D \times V_D = 0.551$ mW



iii) $I_D = \frac{(4-0.7)V}{4.3k} = 0.7674$ mA

$V_D = V_\gamma = 0.7V$

$P_D = I_D \cdot V_\gamma = 0.5372$ mW.



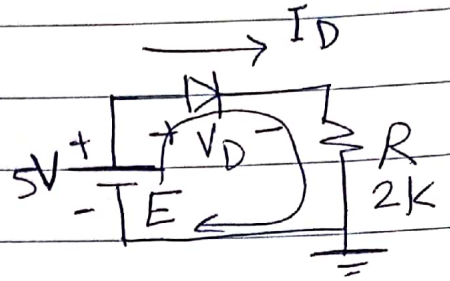
D.C Analysis of Diode Ccts: (19)

There are three methodes of diode cct. Analysis:

1) Iteration methode:

This methode uses trail and Error to Find solution and requires the value of Is.

EXAMPLES: For the cct. shown the diode has: $I_S = 10^{-12}$ A. Find the values of I_D, V_D and P_D.



Write KVL For the cct.

$-E + V_D + I_D R = 0$ and $I_D = I_S\left[e^{\frac{V_D}{nV_T}} - 1\right]$

$5 = I_S R\left[e^{\frac{V_D}{nV_T}} - 1\right] + V_D$

For $n=1$, $V_T = 0.026$ V

$5 = 10^{-12} \times 2 \times 10^{3}\left[e^{\frac{V_D}{1 \times 0.026}} - 1\right]$ ——— eqn. (X)

Assume (Gusse a value for V_D, near V_γ.

the value of V_D which makes L.H.S = R.H.S of eqn. (X) is the right value, then:

Find I_D from its equation or $I_D = \frac{5 - V_D}{R}$

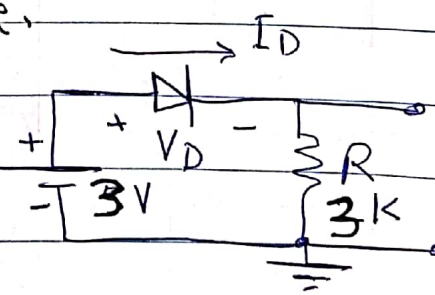
then $P_D = I_D \cdot V_D$.

* For Si diode, $V_\gamma \Rightarrow (0.6 \rightarrow 0.7)$ V, $V_{\gamma Ge} = (0.2 - 0.3)$ V.

2) graphical Methode:

This methode requires the diode characteristic drawn to scale.

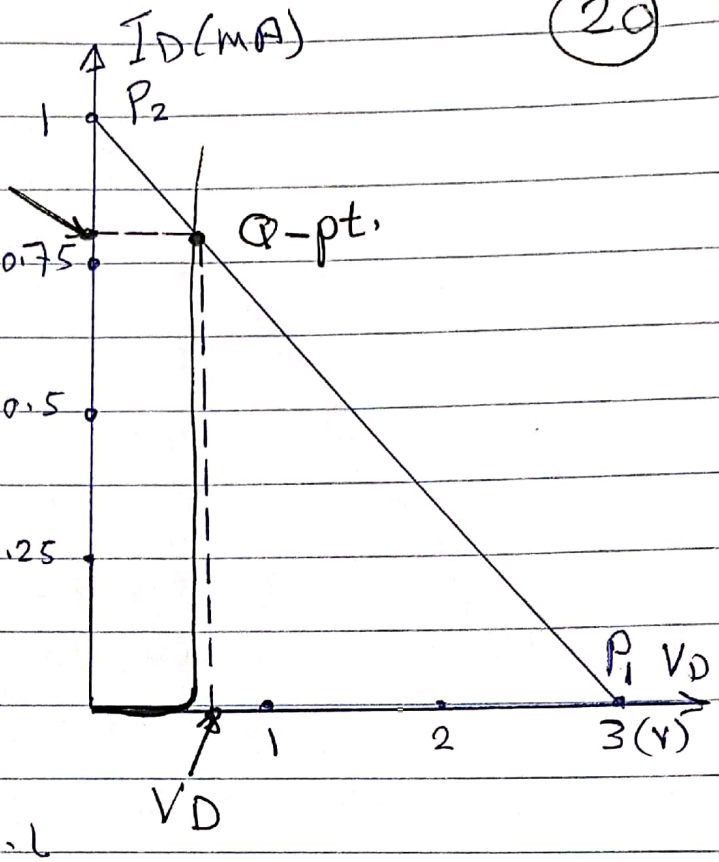
EXA: For the cct. shown, the diode characteristic is shown in Fig., Determine the values of I_D, V_D and P_D.



* To use graphical methode:

i) Write KVL For diode cct: $-3 + V_D + I_D R = 0$

$$I_D = \frac{3}{R} - \frac{V_D}{R} \quad (\otimes)$$



eqn. ⊗ is called D.C. Load-line eqn.

ii) Draw D.C.L.L on diode ~~eqn~~ charateristic

* For $V_D = 0$, $I_D = \frac{3}{R} = \frac{3}{3} = 1$ mA
$P_1(0, 1\text{mA})$.

* For $I_D = 0$, $V_D = 3V$
$P_2(3V, 0\text{mA})$

iii) The intersection of D.C.L.L with Diode c/c give Q-pt. which is the Solution. graphically $V_D \simeq 0.72V$, $I_D = 0.77$ mA
then: $P_D = V_D \cdot I_D = 0.77 \times 0.72 = 0.5544$ mW

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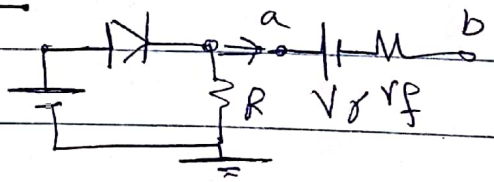
3) Using Piecewise Linear Model:

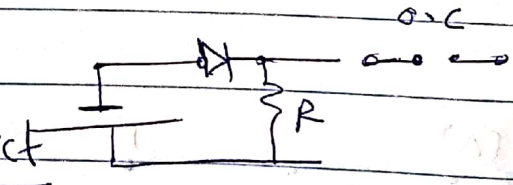
This methode uses diode model.

F.W and $V_D > V_\gamma$

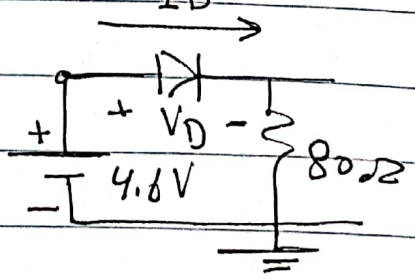
"Constant-Voltage Source + Resistance"
V_γ + r_f



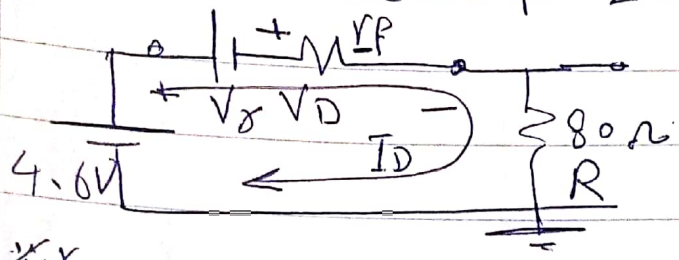
For $V_D < V_\gamma$ or Reverse ⇒ open-cct



Exa: For the cct. Shown. Calculate I_D, V_D & P_D when the diode has: i) $V_\gamma = 0.6V$, $r_f = 20\Omega$
ii) $V_\gamma = 0.8$, $r_f = 0$



i) For $V_\gamma = 0.6V$, $r_f = 20\Omega$



$-4.6 + 0.6 + I_D r_f + I_D R = 0$

$\therefore I_D = \frac{(4.6-0.6)V}{(20+80)\Omega} = \frac{4V}{100\Omega}$

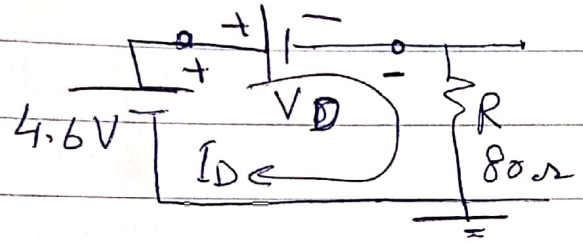
$= 40mA$ mV mV

$V_D = I_D r_f + V_\gamma = 40 \times 20 + 600$

$= 1.4V$

$P_D = I_D V_D = 40 \times 1.4 = 56mW$

ii) For $V_\gamma = 0.6V$, $r_f = 0$



$-4.6 + V_\gamma + I_D R = 0$

$I_D = (4.6-0.6)V/80 = 50mA$

$V_D = V_\gamma = 0.6V$

$P_D = I_D . V_D = 50 \times 0.6 = 30mW$

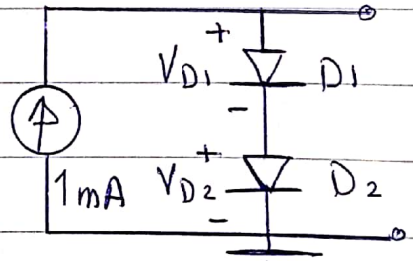
"Examples"

EXA 1: For the cct. shown in Fig. $I_{S1} = 10^{-12}A$, $I_{S2} = 10^{-9}A$.

Given: $n = 1$, $V_T = 0.026V$

i) Calculate V_{D1}, V_{D2}

ii) If D_1 has $V_\gamma = 0.5V$ Find r_{f1}?



$I_{D1} = I_{D2} = 1mA$

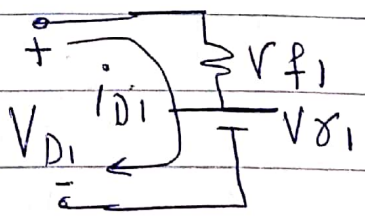
(i) $I_D = I_S e^{\frac{V_D}{nV_T}} \Rightarrow V_D = nV_T \ln \frac{I_D}{I_S}$

$V_{D1} = 1 \times 0.026 \ln \frac{10^{-3}}{10^{-12}} = 0.539V$

$V_{D2} = 1 \times 0.026 \ln \frac{10^{-3}}{10^{-9}} = 0.355V$

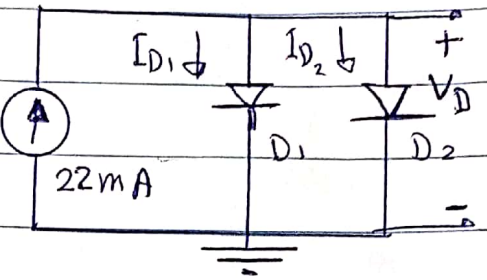
(ii) : $V_{D1} = V_{\gamma 1} + I_{D1} r_{f1}$

$r_{f1} = \frac{V_{D1} - V_{\gamma 1}}{I_{D1}} = \frac{(0.539-0.5)V}{1mA}$



$r_{f1} = 39\Omega$

EXA 2: For the cct. shown in Fig., $n=1$, $V_T = 0.026V$, $I_{S1} = 10^{-12}A$, $I_{S2} = 10^{-13}A$ Calculate I_{D1}, I_{D2}, V_{D1}, P_{D2}



$I_{D1} = I_{S1} e^{\frac{V_{D1}}{nV_T}}$ ①, $I_{D2} = I_{S2} e^{\frac{V_{D2}}{nV_T}}$ ②

but $V_{D1} = V_{D2} = V_D$

Divide eqn. ① by eqn. ②

$$\frac{I_{D1}}{I_{D2}} = \frac{I_{S1} e^{\frac{V_D}{nV_T}}}{I_{S2} e^{\frac{V_D}{nV_T}}} = \frac{I_{S1}}{I_{S2}} = \frac{10^{-12}}{10^{-13}} = 10$$

$\therefore I_{D1} = 10 I_{D2}$

but $I_{D1} + I_{D2} = 22\,mA$

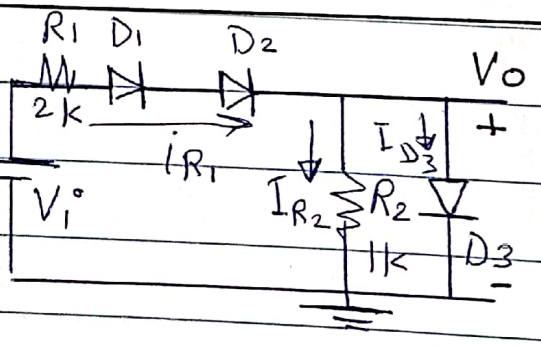
$10 I_{D2} + I_{D2} = 22\,mA$

$\therefore I_{D2} = 2mA$, $I_{D1} = 20mA$

$V_{D1} = V_{D2} = 1 \times 0.026 \ln \frac{20 \times 10^{-3}}{10^{-12}} = 0.6167V$

$P_{D2} = I_{D2} \cdot V_{D2} = 2 \times 0.6167 = 1.235\,mW$

EXA 3: For the cct. shown all diodes has $I_S = 10^{-14}A$, Given: $n=1$, $V_T = 26mV$ Calculate: I_{D1}, I_{D3}, V_{D2} Such that $V_o = 0.6V$? Also Find V_i?



$I_{D3} = I_S e^{\frac{V_D}{nV_T}} = 10^{-14} e^{\frac{0.6}{0.026}} = 0.105\,mA$

$I_{R_2} = \frac{V_o}{R_2} = 0.6\,mA$

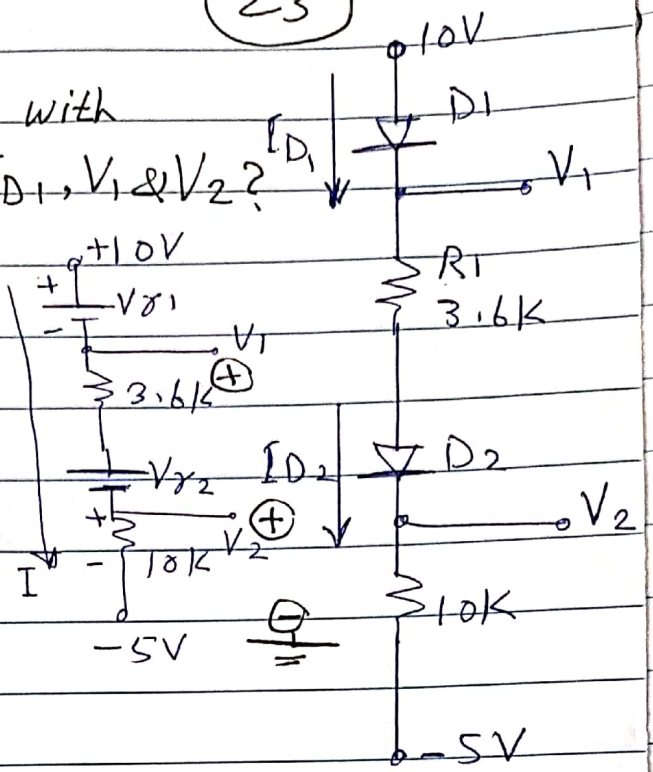
$I_{D1} = I_{D2} = I_{R_1} = I_{D3} + I_{R_2} = 0.705\,mA.$

$V_{D1} = V_{D2} = nV_T \ln \frac{I_{D1}}{I_S} = 1 \times 0.026 \ln \frac{0.705 \times 10^{-3}}{10^{-14}} = 0.645V$

$V_i = I_{R_1} \cdot R_1 + V_{D1} + V_{D2} + V_o$

$V_i = 0.705 \times 2 + 0.645 + 0.645 + 0.6 = 3.3V$

EXA 4: D_1 & D_2 are identical with $V_\gamma = 0.7V$. Calculate I_{D_1}, V_1 & V_2?



* Assume D_1 & $D_2 \Rightarrow$ ON

$$-10 + V_{\gamma 1} + 3.6I + V_{\gamma 2} + 10I - 5 = 0$$

$$I = \frac{(15 - 1.4)V}{(3.6 + 10)k} = \frac{13.6V}{13.6k} = 1mA$$

$$I_{D_1} = I_{D_2} = I = 1mA.$$

$$-10 + V_{\gamma 1} + V_1 = 0$$

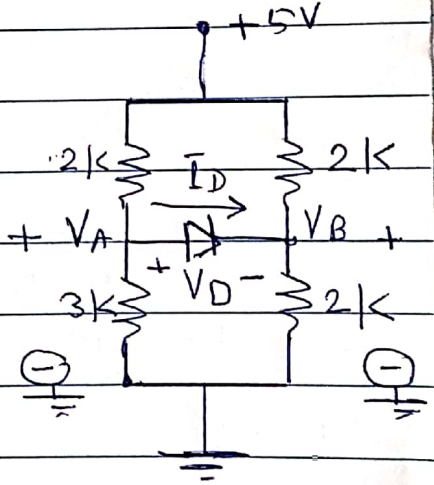
$$V_1 = 10 - V_{\gamma 1} = 9.3V$$

$$-V_2 + 10I - 5 = 0$$

$$V_2 = 10 \times 1 - 5 = 5V$$

EXA 5: For the cct shown, Find I_D, V_D V_A, V_B when the diode has:

i) $V_\gamma = 0.6V$ ii) $V_\gamma = 0.3V$.



Assume Diode is OFF

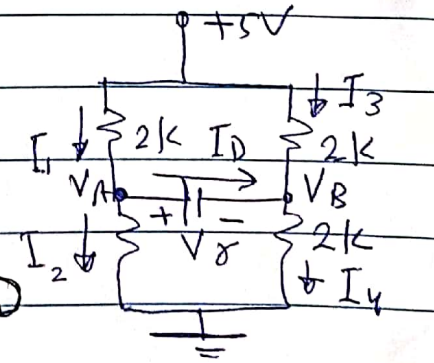
$$V_A = \frac{5 \times 3}{5} = 3V, \quad V_B = \frac{5 \times 2}{4} = 2.5V$$

$$V_{AB} = V_A - V_B = 3 - 2.5 = 0.5V$$

i) For $V_\gamma = 0.6V$, D $\rightarrow$ OFF, $I_D = 0$

$V_D = V_A - V_B = 0.5V$, $V_A = 3V$, $V_B = 2.5V$

ii) When $V_\gamma = 0.3V$, D $\rightarrow$ ON



KCL at Node (A) $I_1 = I_D + I_2$

$$\frac{5 - V_A}{2} = I_D + \frac{V_A}{3}$$

$$15 - 3V_A = 6I_D + 2V_A \Rightarrow \boxed{15 - 5V_A = 6I_D} \quad (1)$$

KVL For node (B)

$$I_3 + I_D = I_4 \Rightarrow \frac{5 - V_B}{2} + I_D = \frac{V_B}{2} \Rightarrow 5 - V_B + 2I_D = V_B$$

$$\boxed{2V_B - 5 = 2I_D} \quad (2)$$

$-V_A + V_\gamma + V_B = 0 \Rightarrow V_A = V_\gamma + V_B \Rightarrow \boxed{V_A = 0.3 + V_B}$ — (3)

Sub. (3) in (1)

~~$V_B = 5(0.3 + V_B) = 6 I_D$~~

$15 - 5(0.3 + V_B) = 6 I_D$

$13.5 - 5V_B = 6 I_D$ — (4)

$-5 + 2V_B = 2 I_D$ — (2) from this $\boxed{I_D = V_B - 2.5}$ — (5)

Sub. (5) in (4) $\Rightarrow 13.5 - 5V_B = 6V_B - 15$

$28.5 = 11 V_B \Longrightarrow V_B = 2.59\,V$

$V_A = 0.3 + 2.59 = 2.89\,V$

$I_D = 2.59 - 2.5 = 0.09\,mA.$

$I_1 = \frac{5 - 2.89}{2} = 1.055\,mA$

$I_2 = \frac{V_A}{3} = \frac{2.89}{3} = 0.9633\,mA$

$I_3 = \frac{5 - V_B}{2} = 1.205\,mA$

$I_4 = \frac{V_B}{2} = 1.295\,mA$

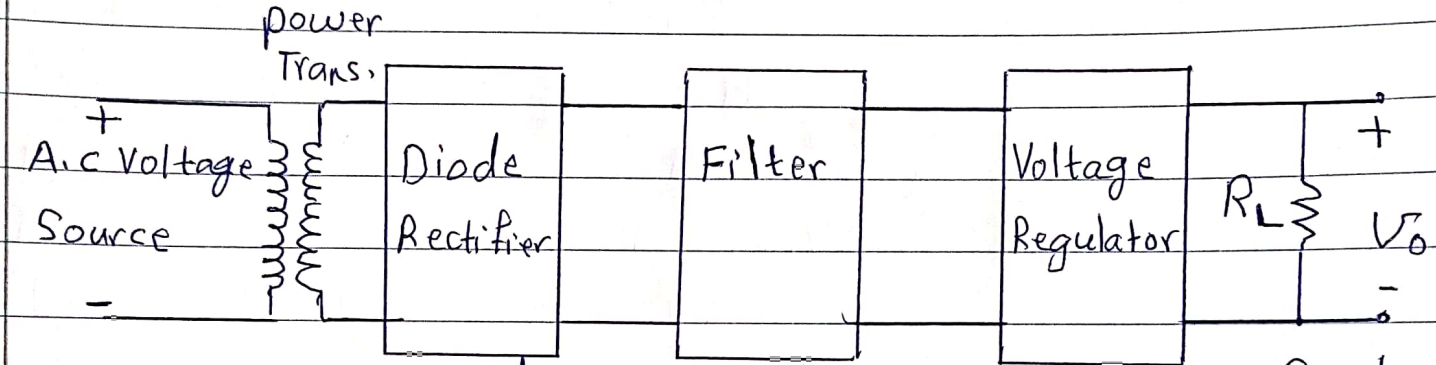
$P_D = I_D \cdot V_D = 0.09 \times 0.3 = 27\,\mu W$

CH. 2: Diode ccts. "Diode Applications"

*) Rectifiers: "Circuits which convert A.C into D.C Using diode as a nonlinear element.

Rectefication: A.C to D.C conversion.

Rectifier: It is the main cct. in electronic D.C power supply. Shown in Fig.

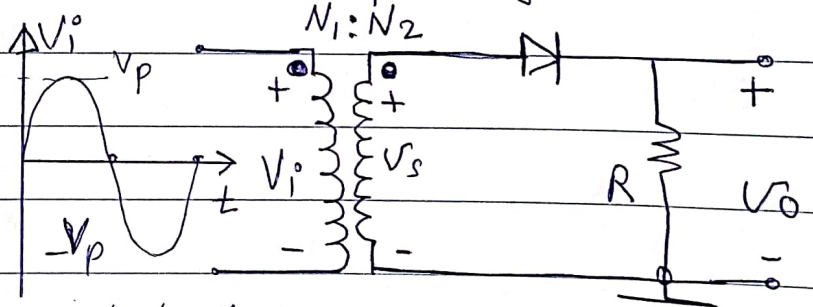


Block diagram of Electronic D.C power Supply

1) Half-Wave Rectification:

In HWR only half-cycle of the A.C input signal is converted into D.C.

*Assume the diode has V_γ and $r_f = 0$



The secondary voltage is related to primary

$$\frac{V_s}{V_p} = \frac{N_2}{N_1} \Rightarrow \frac{V_s}{V_i} = \frac{N_2}{N_1} \Rightarrow V_s = \frac{N_2}{N_1} V_i$$

*The transformer is power transformer used to step-up or step-down depending on its turn-ratio $\left(\frac{N_1}{N_2}\right)$

*It isolates the D.C side from A.C side and prevent sparking.

i) During +ve Half-Cycle of V_i $\Rightarrow$ +ve H.C of V_s

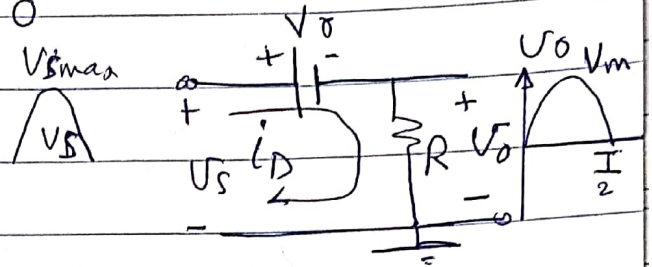
the diode is F.W and represented by $\Rightarrow$ V_γ

$V_o = i_D \cdot R$, $-V_s + V_\gamma + i_D R = 0$

$i_D = \frac{V_s - V_\gamma}{R} \Rightarrow V_o = V_s - V_\gamma$

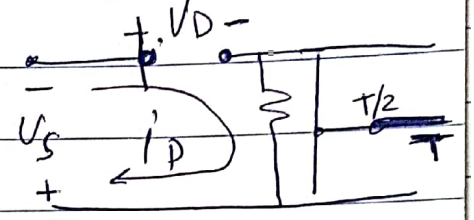
$V_{o\,max} = V_{s\,max} - V_\gamma = V_m$.

Where $V_{s\,max} = \frac{N_2}{N_1} V_{i\,max}$.



ii) During -ve H.C of V_i $\Rightarrow$ -ve H.C of V_s

Diode is OFF, $i_D = 0$, $V_o = i_D R = 0$

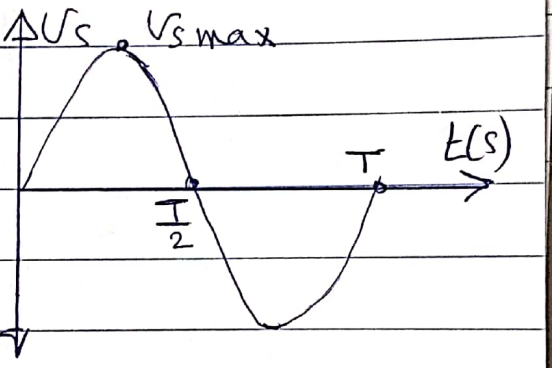


iii) For a Complete cycle of V_i the o/p is only a half-cycle

EXA: For $V_i = 120 \sin \omega t$ V

$(N_1/N_2) = (1/10)$, $V_\gamma = 0.6$V, $R = 2$KΩ

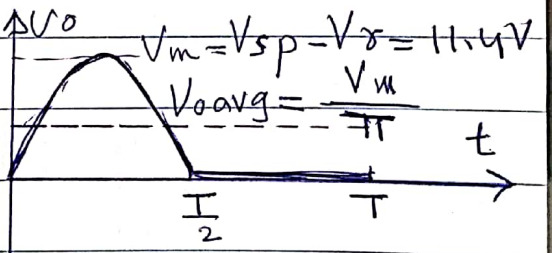
$V_s = \frac{1}{10}(120 \sin \omega t) = 12 \sin \omega t$ V



* peak output Voltage $= V_m$

$V_m = 12 - 0.6 = 11.4$ V

$V_{o\,avg} = \frac{V_m}{\pi} = 3.628$ V

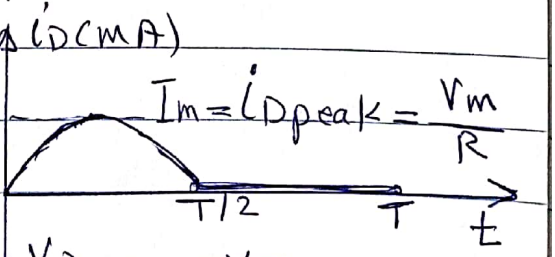


* peak diode current: $i_{D\,peak} = I_m$

$i_{D\,peak} = I_m = \frac{V_m}{R} = \frac{11.4}{2} = 5.7$mA

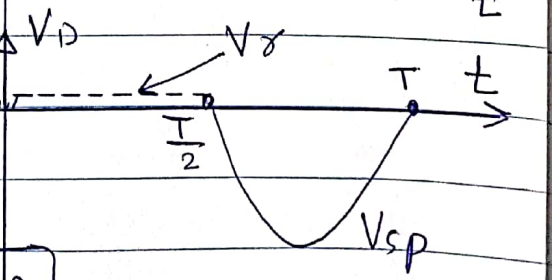
$i_{D\,avg} = \frac{I_m}{\pi} = 1.814$ mA

$P_D = I_{D\,avg} \cdot V_\gamma = 1.088$ mW



peak Inverse Voltage: The max. peak reverse Voltage which the diode withstand befor breakdown

$PIV = V_{sp} = 12$V

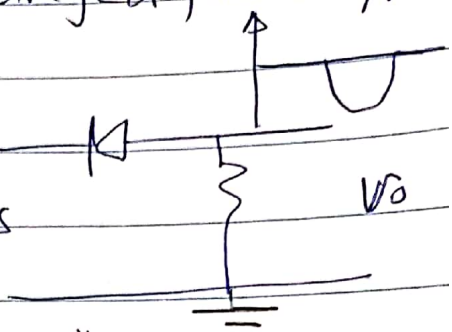


"The Value of V_D when diode is OFF"

* For OFF diode: $+V_s + V_D + i_D R = 0$

$\therefore V_D = -V_s \rightarrow V_{D\,max} = -V_{sp}$ $\therefore$ PIV = Vsp

* If the direction of diode is changed, the o/p will be the -ve H.C, the Rect. is called -ve HWR. $V_{oavg} = \frac{-V_m}{\pi}$

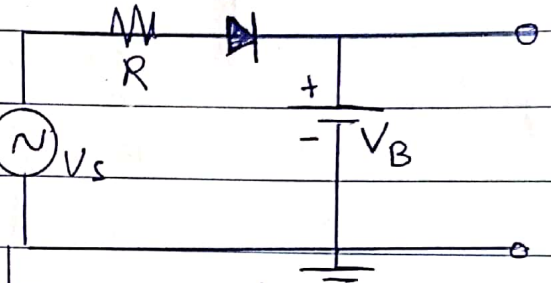


EXA 2: "Using HWR as a Battary charger" For the cct. shown, the diode has $V_\gamma = 0.6V$. Determine:

i) peak diode Current i_{Dp}.

ii) peak Inverse Voltage For diode PIV.

iii) The fraction of cycle over which the diode is conducting. "ON"



$R = 100\Omega$, $V_B = 12V$

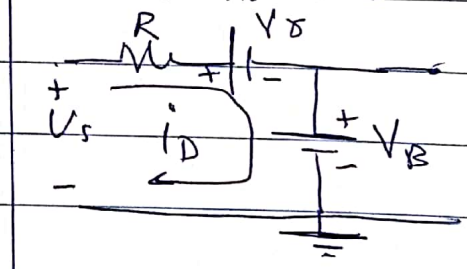
$V_s = 24 \sin\omega t$ V

During +ve H.C of V_s, D → ON

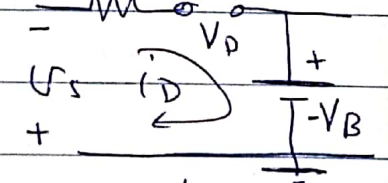
$-V_s + i_D R + V_\gamma + V_B = 0$

$i_D = \frac{V_s - V_\gamma - V_B}{R} \Rightarrow i_{Dp} = \frac{(V_{sp} - 12.6)}{100}$

$\therefore i_{D\,peak} = \frac{24 - 12.6}{100} = 114\ mA$



* To find PIV, find V_D when Diode is OFF

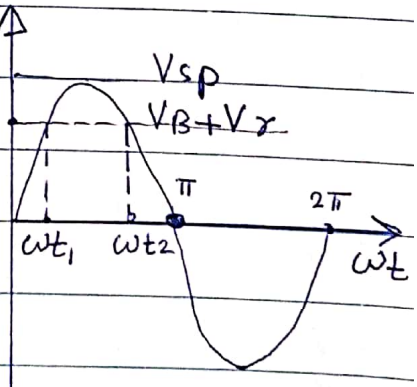


$V_s + i_D R + V_D + V_B = 0$

But $i_D = 0$

$\therefore V_D = -V_s - V_B \Rightarrow V_{D\,max} = -V_{sp} - V_B$

$\therefore PIV = (V_{sp} + V_B) = 36V$



(iii) To Find Conduction angle

$V_s = 24 \sin\omega t \Rightarrow$ at ωt_1, $V_s = V_B + V_\gamma = 12.6V$

then $\omega t_1 = \tan^{-1}\frac{12.6}{24} = 31.7^\circ$

By Symmetry, $\omega t_2 = 180^\circ - 31.7 = 148.3^\circ$

Conduction angle $= \omega t_2 - \omega t_1 = 116.6^\circ = \phi_c$

% Conduction angle $= \frac{\phi_c}{360^\circ} \times 100\% = 32.4\%$

② Full-wave Rectifiers

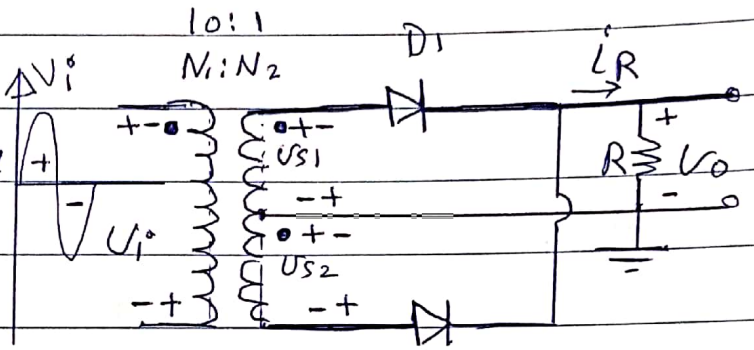
In FWR both halves of the A.C input signal are converted to D.C. The d.c output of FWR is twice that of the HWR, but at least two diodes are used in FWR.

There are basically two types of FWR:

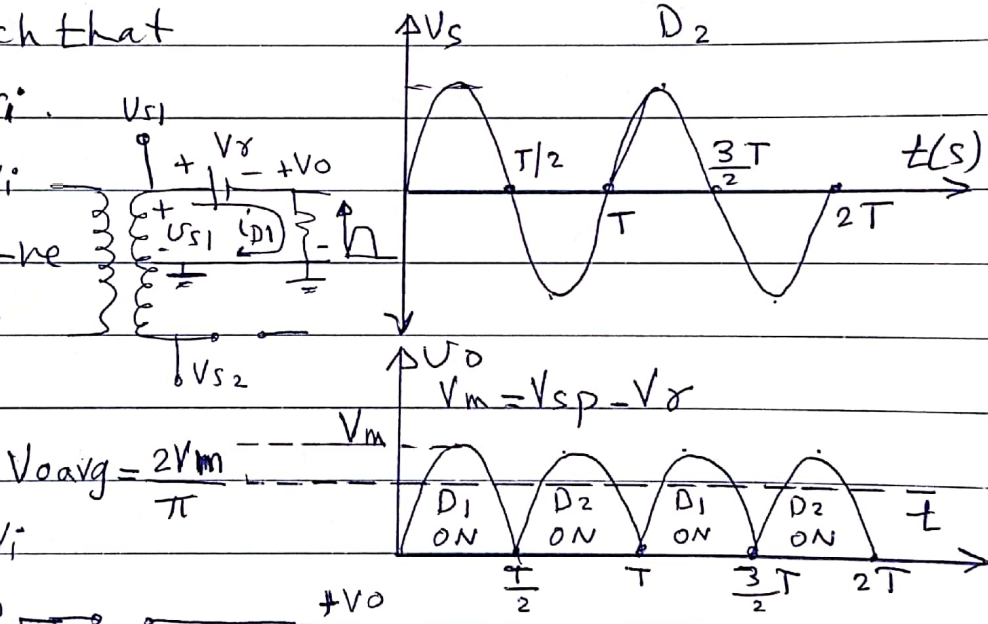
i) Full-Wave Rectifier using Center-tapped Transfor.

The type of transformer is Center-tapped transforme which produces two output V_{s1} and V_{s2} which have equal amplitude but 180° out of phase such that

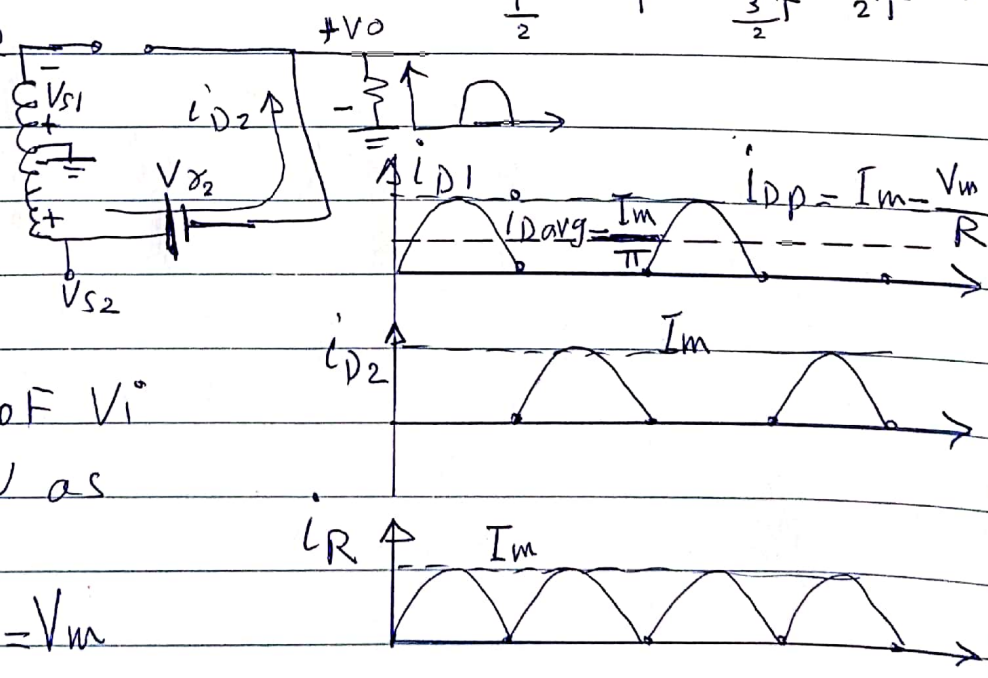
$V_{s2} = -V_{s1} = \frac{N_2}{N_1} V_i$.



* For +ve H.C of V_i
→ V_{s1} → +ve, V_{s2} → -ve
D_1 → ON, D_2 → OFF
$V_{o1} = V_{s1} - V_\gamma$
$V_{o,max} = V_{sp} - V_o$ $\quad V_{oavg} = \frac{2V_m}{\pi}$



* For -ve H.C of V_i
V_{s1} → -ve, V_{s2} → +ve
i_{D2} flows in R
$i_{D1} = 0$ (D_1 → OFF)
$V_{o2} = V_{s2} - V_\gamma$
$V_{omax} = V_{sp} - V_\gamma$



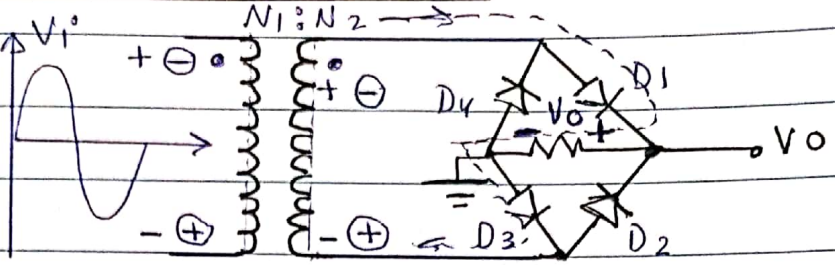
* For a Full-cycle of V_i the o/p is a FW as shown above.

$V_{omax} = V_{sp} - V_\gamma = V_m$

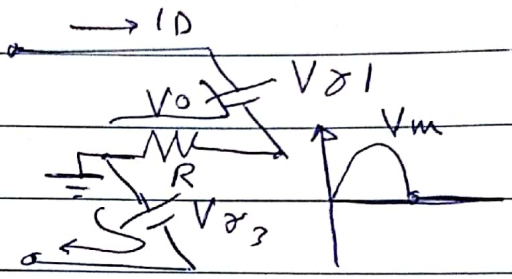
For this rectifier PIV For diodes " $PIV = 2V_{sp} - V_\gamma$ "

The average output voltage $V_{oavg} = V_{d.c} = \frac{2V_m}{\pi}$.

ii) Full-wave Bridge Rectifier " FWBR "



This cct. uses Four diode of the same type and normal transformer (If necessary).



* During +ve H.C of $V_i \rightarrow$ +ve H.C of V_s, D_1 & D_3 are "ON" but D_2 & $D_4 \rightarrow$ OFF

$i_{D1} = i_{D3} = i_D$ will flow in R causing $V_o = i_D \cdot R$ with polarity [V_o+]

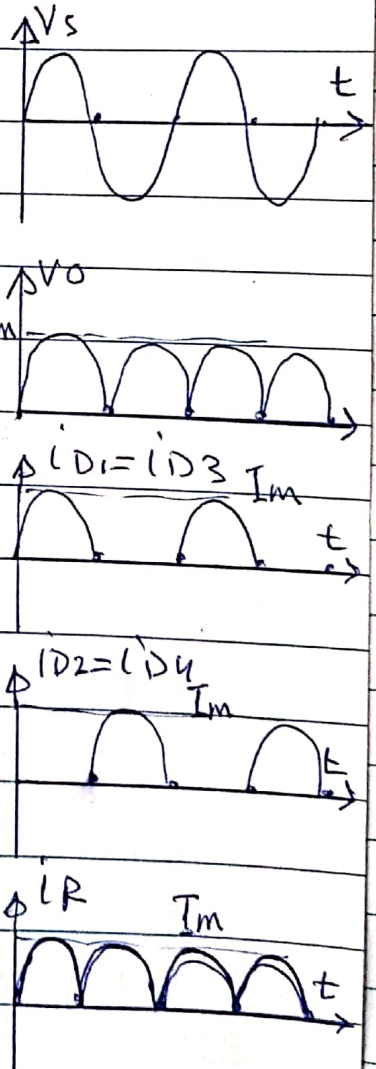
$V_o = V_s - 2V_\gamma \rightarrow V_{omax} = \boxed{V_m = V_{sp} - 2V_\gamma}$

* During -ve H.C of $V_i \rightarrow$ -ve H.C of V_s , D_1 & $D_3 \rightarrow$ OFF, but D_2 & $D_4 \rightarrow$ "ON"

$i_{D2} = i_{D4} = i_D$ will flow in R causing

$V_o = i_D R = V_s - 2V_\gamma \rightarrow V_{omax} = V_m = V_{sp} - 2V_\gamma$ with polarity [V_o +] Same as in +ve H.C

* For a Full-cycle of V_i, the o/p will be a Full-wave as shown.



* The peak output voltage $V_m = V_{sp} - 2V_\gamma$

$V_{oavg} = V_{d.c} = \frac{2V_m}{\pi}$, peak diode Current

$i_{Dp} = I_m = \frac{V_m}{R}$

$i_{Davg} = \frac{I_m}{\pi}$

PIV For diode : $\boxed{PIV = V_{sp} - V_\gamma}$

Example: Design a FWR to deliver a peak o/p voltage of 15 Volt. to 100Ω load. Use diodes with $V_\gamma = 0.7$ V. [Hence: determine turn-ratio $(\frac{N_1}{N_2})$, PIV rating, peak diode current i_{Dp} and power dissipation P_D] perform the design using (i) FWR with C-T trans. (ii) FWBR. *which approach will you prefer and why? Given: $V_i = 120$ V (rms).

(i) Using C-T transformer:

$V_{sp} = V_m + V_\gamma = 15 + 0.7 = 15.7$ V

$(N_1/N_2) = \frac{V_i}{V_s} = \frac{V_{i(rms)}}{V_{s(rms)}} = \frac{V_{ip}}{V_{sp}}$.

$V_{ip} = V_{i(rms)} \cdot \sqrt{2} = 120 \cdot \sqrt{2} = 169.7$ V

$\therefore (N_1/N_2) = \frac{169.7}{15.7} = 10.8$

$\boxed{PIV} = 2V_{sp} - V_\gamma = 2 \times 15.7 - 0.7 = \boxed{30.7\ V}$

$i_{Dp} = I_m = \frac{V_m}{R} = \frac{15}{100} = 150$ mA.

$P_{D\,avg} = I_{D\,avg} \cdot V_\gamma = \frac{150}{\pi} \times 0.7 = 33.42$ mW

(ii) Using FWBR:

$V_{sp} = V_m + 2V_\gamma = 15 + 2 \times 0.7 = 16.4$ V

$\left(\frac{N_1}{N_2}\right) = \frac{169.7}{16.4} = \boxed{10.3}$

$\boxed{PIV} = V_{sp} - V_\gamma = \boxed{15.7\ V}$

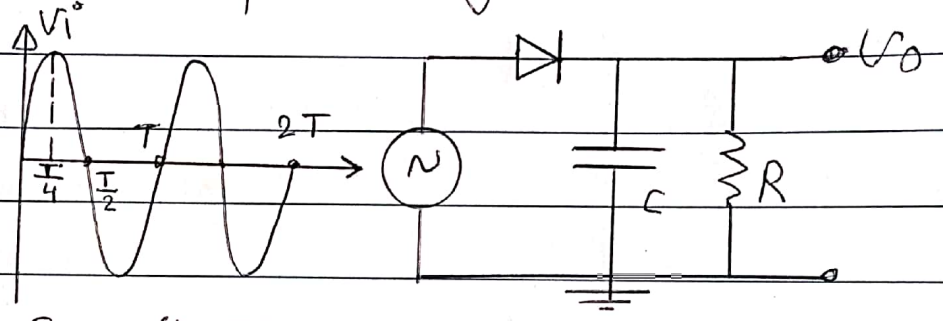
$i_{Dp} = I_m = 150$ mA

$P_{D\,avg} = 33.42$ mW.

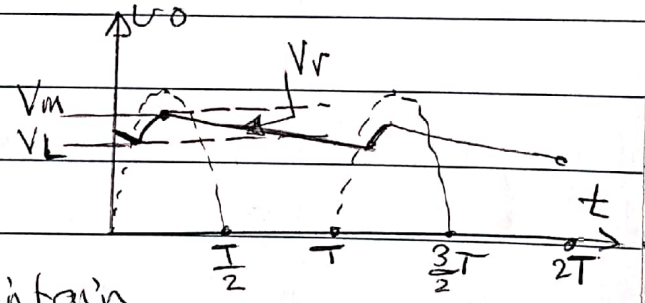
* FWBR is preferable because
- PIV rating is low.
- The transformer is Normal trans. and has one Secondary compared to C-T trans. which has two Secon

Filters, Ripple Voltage, and Diode Current

Filter: Simply, It is a capacitor connected in parallel with the load resistor in a rectifier and used to transform the pulsating d.c (HW or FW Sinusoidal) into a d.c Voltage. The output of rectifier with filter is D.C with small ripple voltage due to charging and discharging of the capacitor. Consider the HWR with filter shown with its output Voltage.



* Assume diode with V_γ and $r_f = 0$
* When Diode is "ON" Capacitor charges with time constant $r_f \cdot C = 0 \left(t < \frac{T}{4}\right)$
* When diode "OFF", Capacitor discharges with time Constant. $\tau_{dis} = RC$. So by choosing RC too Large the Cap. will maintain its Voltage and Since $V_o = V_c$, so the o/p will be (D.C + ripple voltage). the Value of ripple voltage (V_r) is related to [V_m, R, C, f] by the following relation:



$$V_r = \frac{V_m}{fCR} \quad \text{(HWR)} \quad (1)$$

$$V_r = \frac{V_m}{2fCR} \quad \text{(FWR)} \quad (2)$$

* Derivation of these eqns. are in the text book.*

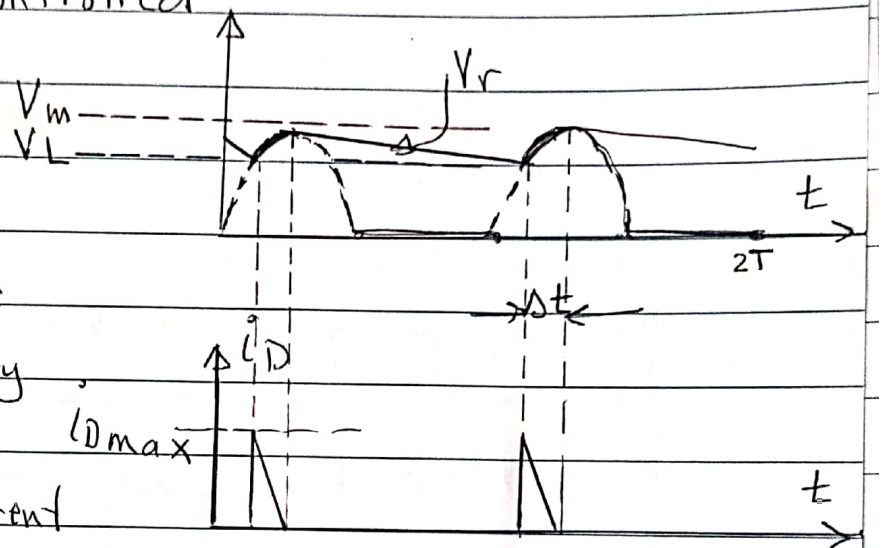
Where:
V_m: peak o/p Voltage
R: load Resistance
C: Filtering Cap.
f: frequency of the input Signal.
V_r: ripple Voltage

From eqn ① and ②, it is clear that:

i) For the Same f, V_m, C, R &
$V_r(FWR) = \frac{1}{2} V_r(HWR)$.

ii) For the Same V_r, R, f, V_m then $\boxed{C_{FWR} = \frac{1}{2} C_{HWR}}$.

* The Value of V_r is controlled via choosing C.
* To achieve Small V_r we have to use Large C but we Can't choose the filtering cap. C arbitrary, the limitting factor is the max. diode Current $i_{D\max}$ which is Given in data sheet. because $i_D = C\frac{dV_c}{dt}$.



EXAMPLES: Design a FWBR to deliver 12V (peak o/p Voltage) to 100Ω load. with ripple Not more than 5%. the available input is 120V(rms), f = 50 Hz. Use Si diode with $V_\gamma = 0.6V$
* Calculate (N_1/N_2) of trans. Filtering Cap. C, diode PIV
* Draw output Voltage, indicating all voltage levels.

For FWBR: $V_{sp} = V_m + 2V_\gamma = 16.2V$

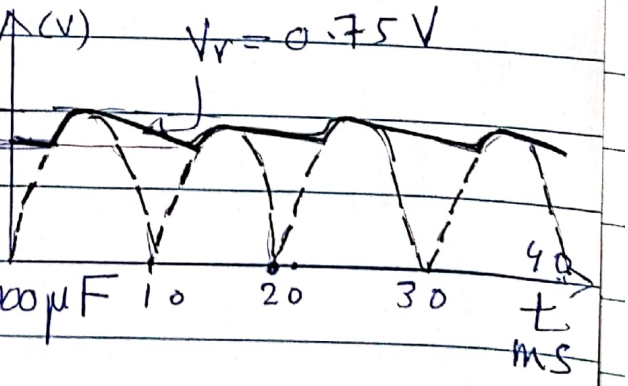
$V_{ip} = V_i(rms)\sqrt{2} = 169.7V$

$\therefore (N_1/N_2) = \frac{169.7}{16.2} = 10.5$

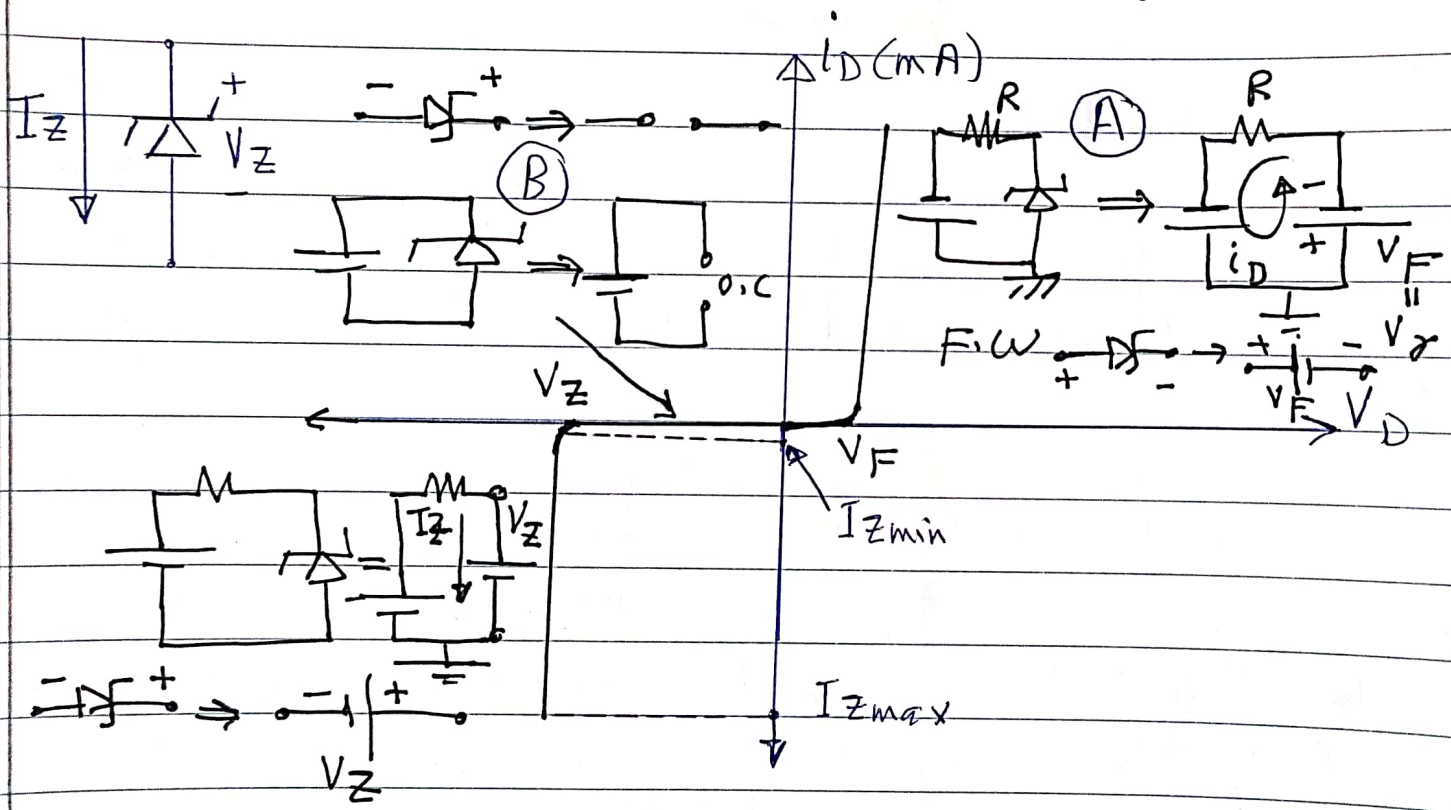
$V_m = 15V$
$V_L = 14.25V$

$$C = \frac{V_m}{2fCRV_r} = \frac{15}{2\times 50\times 0.75\times 100} = 2000\mu F$$

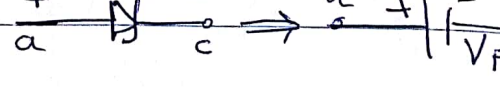
$PIV = V_{sp} - V_\gamma = 15.6V$

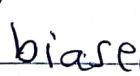


Special type of diodes, designed and fabricated to operate at breakdown regn. with a certain breakdown voltage V_Z, over a wide range of current and temp.
- The current is limited to a value within the capabilites of the device. Such a diode can be used as a Constant-Voltage reference in a circuit. The Symbole, notations and device characteristics is shown in Fig.

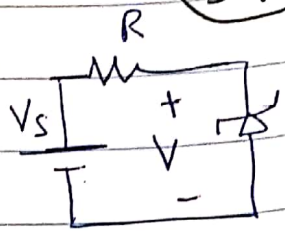


This diode behaves as follow:

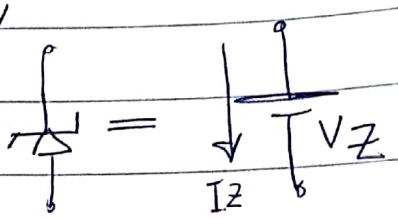
1) When it is biased in F.W, it is similar to normal Diode i.e it is represented by a Constant-Voltage reference of Value ($V_F = V_\gamma$)  (Regn. A in I-V c/c)

2) When it is reverse biased:  it behaves as follow:

i) If the Voltage across Z-D is ($V < V_Z$) then Z-D is OFF $\Rightarrow$ open-cct, $I_Z = 0$ (Regn. B in I-V c/c).



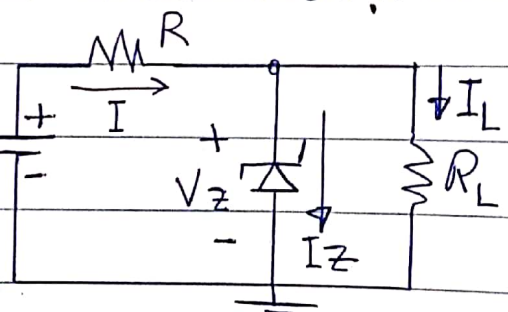
ii) If the Voltage across Z-D, ($V \geq V_Z$), then the Z-D is "ON" and $I_Z > 0$, it behaves as a Constant-Voltage reference with polarity as Show and Current $I_Z > 0$. (Regn. C in I-V c/c).



* Because of this characteristic of Z-D (behaves as Constant-Voltage Reference) it is Used as a Voltage-Regulator to maintain a certain Voltage a cross a certain load *

* The Basic Voltage-Reg. cct. using Z-D is Shown in Fig. and it will be analyzed under three conditions.

i) Fixed V_i and Fixed R_L:



Zener diode Regulator.

the analysis of this case is:

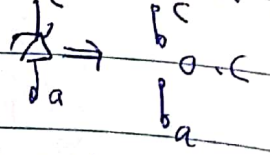
a) Determine the State of the Z-D "(ON)" or "OFF"

* "by assuming Z-D "OFF" and Calculate (V) then: If $V < V_Z$ the Z-D is "OFF", $I_Z = 0$ But If ($V \geq V_Z$) Z-D is "ON" and $I_Z > 0$"

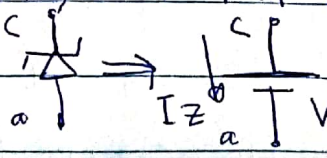
* "OR assuming Z-D is ON and Find I_Z: If I_Z is > 0 It is "ON" but If $I_Z < 0$, it is OFF and $I_Z = 0$

b) Replace Z-D by its proper eqnt. cct. and Find required information.

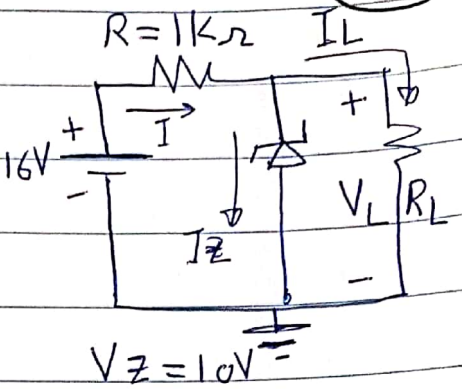
"OFF" $\Rightarrow$ O.C



"ON" $\Rightarrow$ Const-Ref-Voltage



EXA: For the cct. shown: determine
I, I_L, I_Z, P_Z & V_L when:
i) $R_L = 1K\Omega$ ii) $R_L = 3K\Omega$.

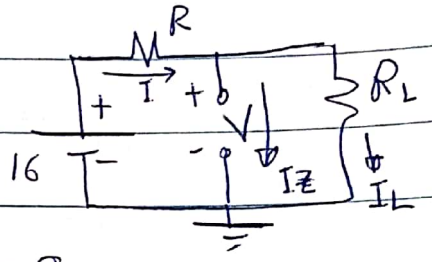


Assume Z-D is OFF and Calculate

$V = \frac{16 \times R_L}{R + R_L}$. If $V < V_Z \rightarrow$ OFF
If $V \geq V_Z \rightarrow$ ON

i) For $R_L = 1K$

$V = \frac{16 \times 1}{1+1} = 8V$



Since $V < V_Z$, Z-D is OFF $I_Z = 0$

$I = I_L = \frac{V_i}{R + R_L} = \frac{16}{2K} = 8mA$

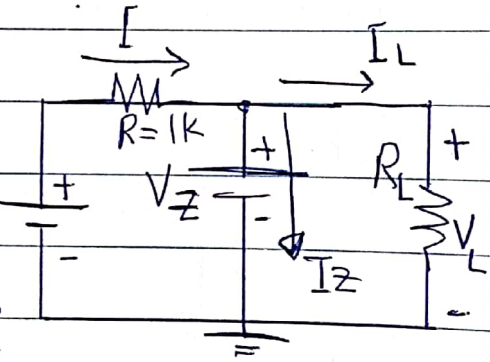
$V_L = V = 8V$

$P_Z = I_Z \times V_Z = 0$

ii) For $R_L = 3K\Omega$

$V = \frac{16 \times 3}{4} = 12V$

Since $V > V_Z \Rightarrow$ Z-D is "ON"



$V_L = V_Z = 10V$, $I_L = \frac{V_Z}{R_L} = \frac{10}{3} = 3.33$ mA

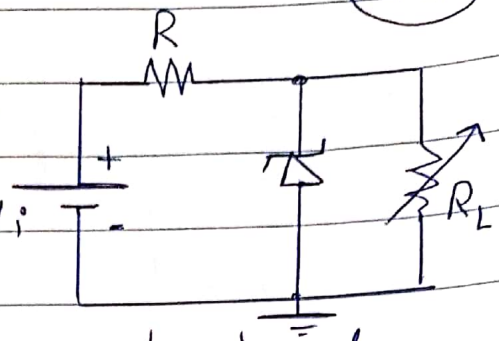
$I = \frac{V_i - V_Z}{R} = \frac{(16-10)V}{1K} = 6mA$.

$I_Z = I - I_L = 6 - 3.33 = 2.67$ mA.

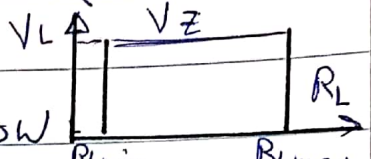
$P_Z = I_Z . V_Z = 2.67$ mW.

NOTE: ① Z-D is used to protect the load (R_L). when V_i is Varied or R_L is Varied or both.
② R is used to protect Z-D and "NOT" allow more than $I_{Z max}$ to follow in Z-D.

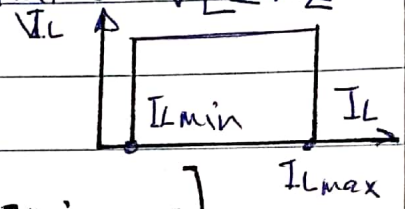
ii) Fixed V_i and Variable R_L:



In this case, the Z-D will be "ON" For a certain range of R_L extending from (R_{Lmin} to R_{Lmax}) and maintain a certain voltage (V_Z) across the Load, Hence protect the load. The range of R_L over which the Z-D is "ON" depends on Z-D parameters (V_Z, I_{Zmax} I_{Zmin}), V_i and R.



* The value of R_{Lmin} is determined as follow R_{Lmin} is the minimum value of R_L which makes $V_L = V_Z$



i.e: $V_L = V_Z = \dfrac{V_i \cdot R_{Lmin}}{R_{Lmin} + R}$ which gives

$$R_{Lmin} = \frac{R \cdot V_Z}{V_i - V_Z}$$ *[this eqn. is based on $I_{Zmin} = 0$]

Any value more than R_{Lmin} will make Z-D "ON" and replaced by V_Z. This value will specify $I_{Lmax} = \dfrac{V_Z}{R_{Lmin}}$

To determine R_{Lmax}, we can use:

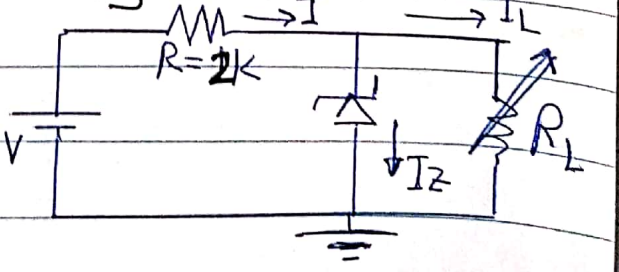
$$R_{Lmax} = \frac{V_Z}{I_{Lmin}}$$ * where $I_{Lmin} = I_R - I_{Zmax}$

and: $I_R = \dfrac{V_i - V_Z}{R}$ and I_{Zmax} either given in data sheet or from $I_{Zmax} = \dfrac{P_{Zmax}}{V_Z}$.

EXA: For the cct. shown, the Z-D has: $V_Z = 10V$, $P_{Zmax} = 15$ mW

i) Determine the range of R_L and I_L over which the Z-D maintain 10V across the load.

ii) Determine the max. wattage rating of the Z-D (i.e Determine P_{Zmax}).



$$R_{Lmin} = \frac{R.V_Z}{V_i - V_Z} = \frac{2 \times 10}{50-10} = 0.5 K\Omega$$

$$I_R = \frac{50-10}{2} = 20mA.$$

$$I_{Lmin} = I_R - I_{Zmax} = 20 - 15 = 5mA$$

$$R_{Lmax} = \frac{V_Z}{I_{Lmin}} = \frac{10V}{5mA} = 2K\Omega$$

$$P_{Zmax} = V_Z . I_{Zmax} = 10 \times 15 = 150 mW$$

$$I_{Lmax} = V_Z / R_{Lmin} = \frac{10V}{0.5k} = 20mA.$$

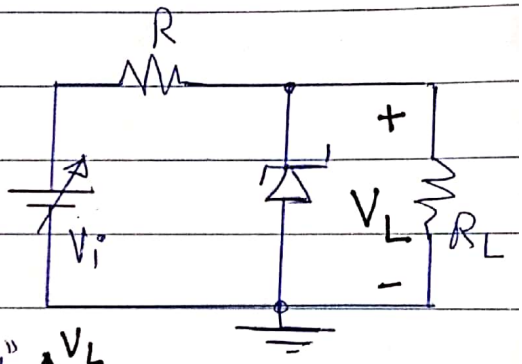
** If $I_{Zmin} \neq 0$ then:

$$R_{Lmin} = \frac{V_Z}{I_{Lmax}}$$

where:

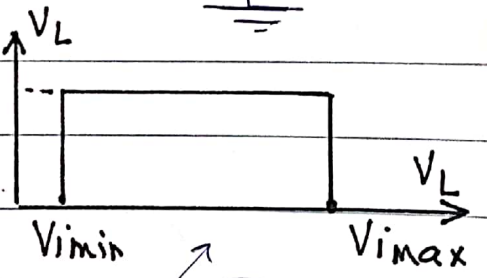
$$I_{Lmax} = I_R - I_{Zmin}$$

iii) Fixed R_L and Variable V_i:



For Fixed R_L, Z-D can maintain a Fixed voltage across R_L (V_Z) when V_i varies from $V_{imin} \rightarrow V_{imax}$.

- The range of V_i over which Z-D is "ON" depends on Z-D parameters. For certain values of R & R_L.



V_{imin}: when Z-D is OFF ($I_{Zmin} = 0$)

the Value of Voltage across Z-D is $V = \frac{V_i . R_L}{R_L + R}$

the Value of V_i which makes $V = V_Z$ is V_{imin}

i.e $V = V_Z = \frac{V_{imin} \cdot R_L}{R_L + R} \Rightarrow \boxed{V_{imin} = \frac{(R_L + R) V_Z}{R_L}}$ ——— ①

V_{imax}: The Value of V_{imax} is determined by I_{Zmax}.

$V_i = I_R . R + V_Z \Rightarrow V_{imax} = I_{Rmax} + V_Z$, $I_R = I_Z + I_L$

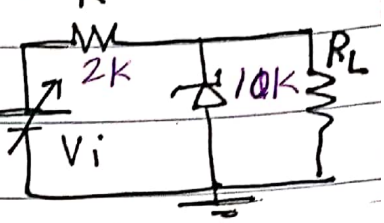
and $I_L = \frac{V_Z}{R_L}$ (Fixed) So $I_{Rmax} = I_R + I_{Zmax}$

$$\boxed{V_{imax} = [I_{Zmax} + I_L] R + V_Z} \quad \text{——— ②}$$

eqn. ① is used when $I_{Zmin}=0$

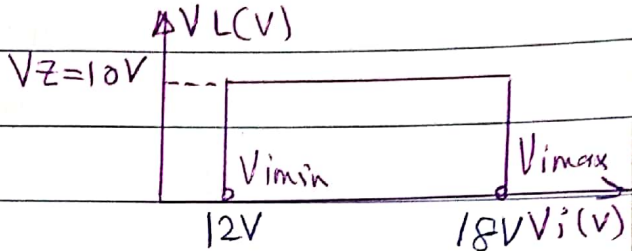
* If $I_{Zmin} \neq 0$, then $V_{imin}=[I_{Zmin}+I_L]R+V_Z$.

EXA: For the cct. shown the Z-D has $V_Z=10V$, $P_{Zmax}=30mW$ * Determine the range of V_i over which the Z-D is "ON"



* Sketch V_L versus V_i? * Recalculate V_{imin} when $I_{Zmin}=1mA$

$$V_{imin}=\frac{(R_L+R)V_Z}{R_L}=\frac{(2+10)\times 10}{10}=\boxed{12V}$$



$$V_{imax}=(I_{Zmax}+I_L)R+V_Z$$

$$I_{Zmax}=\frac{P_{Zmax}}{V_Z}=\frac{30}{10}=3mA$$

$$I_L=\frac{V_Z}{R_L}=\frac{10V}{10K}=1mA$$

$$\therefore V_{imax}=[3+1]\times 2+10=\boxed{18V}$$

* when $I_{Zmin}=1mA$, then: $V_{imin}=(I_{Zmin}+I_L)R+V_Z$

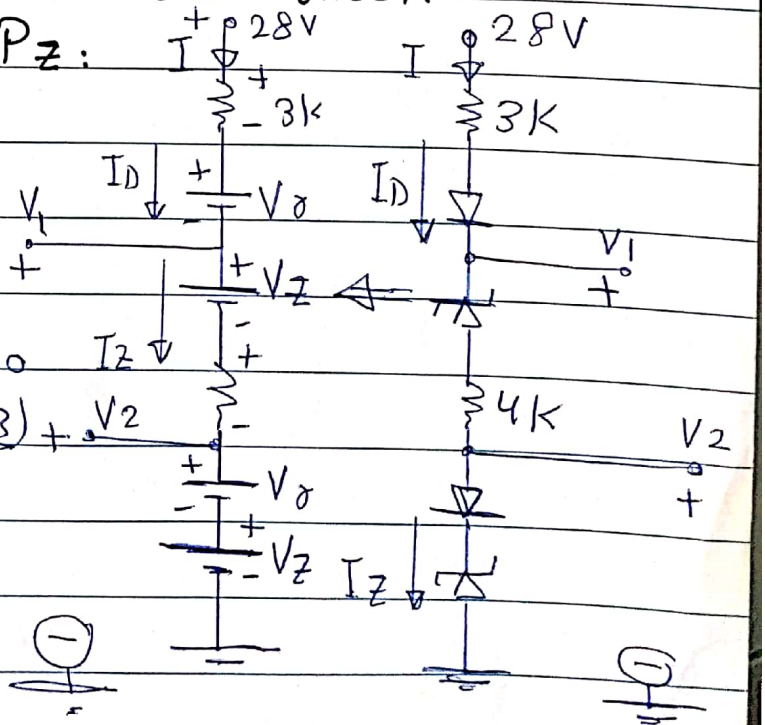
$$\therefore V_{imin}=(1+1)\times 2+10=14V$$

EXA: Combination of Z-D with normal diode

Determine I_Z, I_D, V_1, V_2, P_Z:

Given: $V_\gamma=0.7V$, $V_Z=6.3V$.

Assume all diodes "ON"



* KVL For the cct:

$$-28+3I+V_\gamma+V_Z+V_\gamma+V_Z+I\times 4=0$$

$$I=I_Z-I_D=\frac{28-(0.7+6.3+0.7+6.3)}{7K}+\frac{V_2}{}$$

$$I=I_Z=I_D=2mA.$$

$$V_1=28-2\times 3-0.7=21.3V$$

$$V_2=0.7+6.3=7V$$

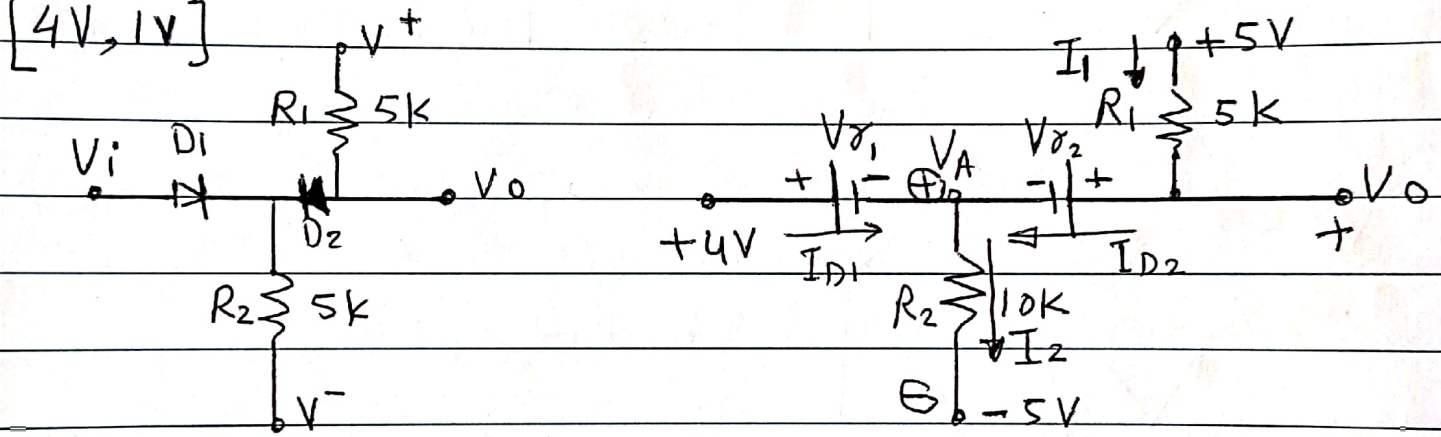
$$P_Z=I_Z\times V_Z=12.6mW$$

Multiple-Diode Circuits

Circuits contains more than one diode. Diodes can be "ON" or "OFF", so analysis can be complicated. In these ccts. you have to Gusse the state of Diode: but remember "ON" diode has: $I_D > 0$ and "OFF" diode have $V_D < 0$ or $V_D < V_\gamma$.

EXA: For the cct. shown in Fig. the diodes have $V_\gamma = 0.7V, r_f = 0$

Calculate: $I_{D1}, I_{D2}, V_{D1}, V_{D2}, V_A$ and V_o. For V_i [4V, 1V]



① Assume D_1 & D_2 ⇒ ON (For $V_i = 4V$)

$-4 + V_{\gamma 1} - V_{\gamma 2} + V_o = 0 \Rightarrow V_o = 4V$

$I_1 = \frac{V^+ - V_o}{R_1} = \frac{5-4}{5} = .8mA = I_{D2}$

$-4 + V_{\gamma 1} + V_A = 0 \Rightarrow V_A = 4 - V_{\gamma 1} = 3.3V$

$-V_A + I_2 R_2 - 5 = 0 \Rightarrow I_2 = \frac{V_A + 5}{R_2} = 0.83\,mA$

$I_{D1} + I_{D2} = I_2$

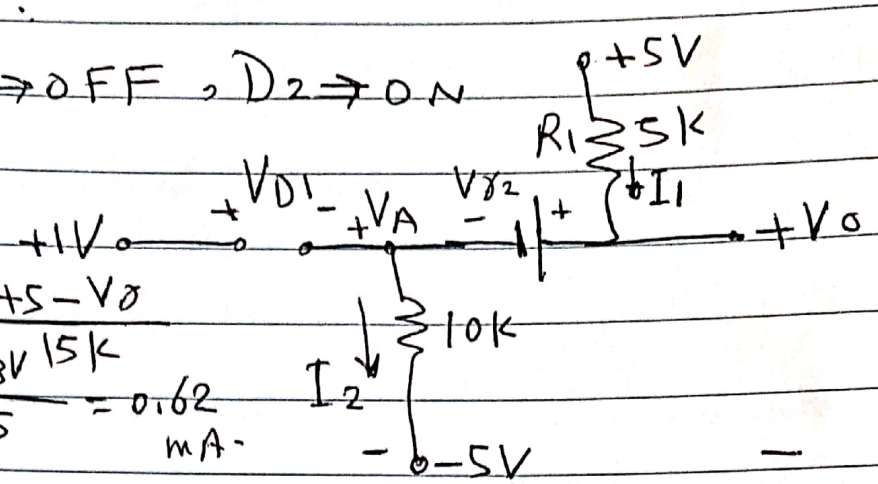
∴ $I_{D1} = I_2 - I_{D2} = 0.83 - 0.8 = 0.03\,mA$

Since I_{D1} & $I_{D2} > 0$ ∴ D_1 & D_2 ⇒ ON

$V_{D1} = V_{D2} = V_\gamma = 0.7V$.

2) For $V_i = 1V$.

Assume $D_1 \rightarrow OFF$, $D_2 \rightarrow ON$



$$I_1 = I_{D2} = I_2 = \frac{5+5-V_\gamma}{15K} = \frac{9.3V}{15} = 0.62 \text{ mA}$$

$$-V_A + I_2R_2 - 5 = 0$$

$$V_A = I_2R_2 - 5 = 0.62 \times 10 - 5 = 1.2V$$

$$-1 + V_{D1} + 1.2 = 0$$

$$V_{D1} = 1 - 1.2 = -0.2V$$

∴ D_1 is realy "OFF", $I_{D1} = 0$

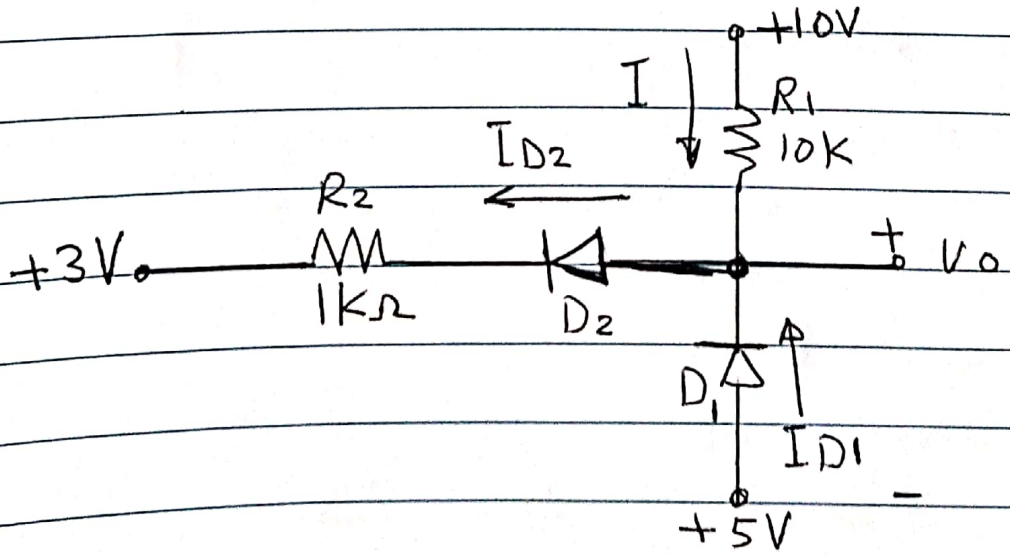
$$V_o = 5 - I_1R_1 = 5 - 0.62 \times 5 = 1.9V$$

Since $I_{D2} > 0$ ∴ D_2 is realy "ON"

$$V_{D2} = V_\gamma = 0.7V.$$

H.W: For the cct. shown D_1 & D_2 are identical with $V_\gamma = 0.6V$, $r_f = 0$.

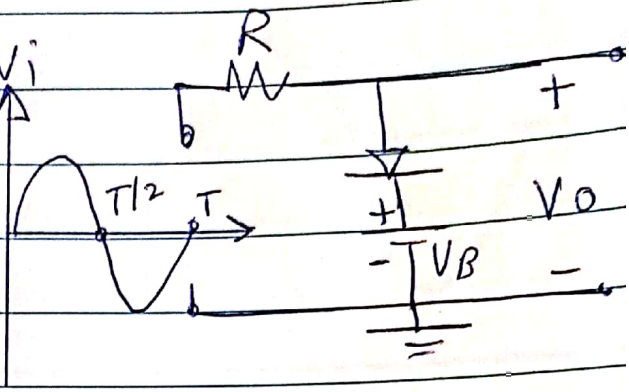
Calculate I_{D1}, I_{D2}, I and V_o?



Clipping:

Cutting a portion of the A.C input signal to a certain specified level. The clipper is shown in Fig.

- The i/p Signal Can be clipped either from +ve H.C or -ve H.C depending on the direction of the diode.

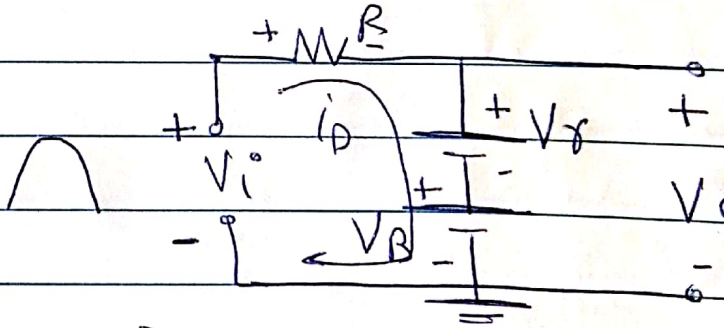


- The clipping level depends on the value and polarity of the D.C battary connected with diode

* EXAMPLE: Given $V_\gamma = 0.6V$, $V_B = 1.4V$. Draw $V_o(t)$ for the indicated input.

Solution:

* For the +ve H.C of Vi, Diode is F.W and eqnt. cct. is shown



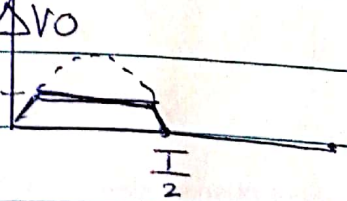
$$-V_i + i_D R + V_\gamma + V_B = 0$$

$$\therefore i_D = \frac{V_i - V_\gamma - V_B}{R}$$

$$i_D = \frac{V_i - 2}{R},$$

(i) So when $V_i > 2$, $i_D > 0$, D → ON and $V_o = V_\gamma + V_B = 2V$.

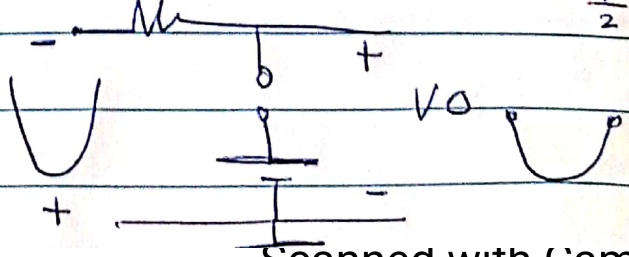
(ii) For $V_i < 2$, $i_D < 0$, D → OFF. $V_o = V_i$ i.e the o/p (V_o) will be as shown.



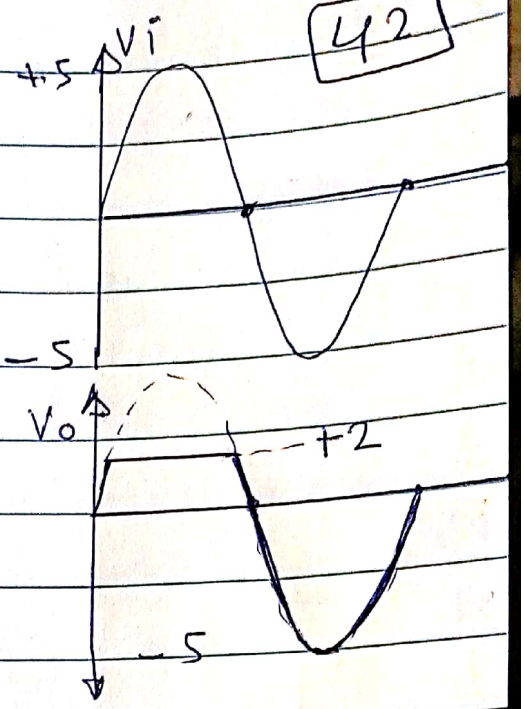
* For -ve H.C of Vi, D → Rev

So $i_D = 0$, $V_o = V_i$

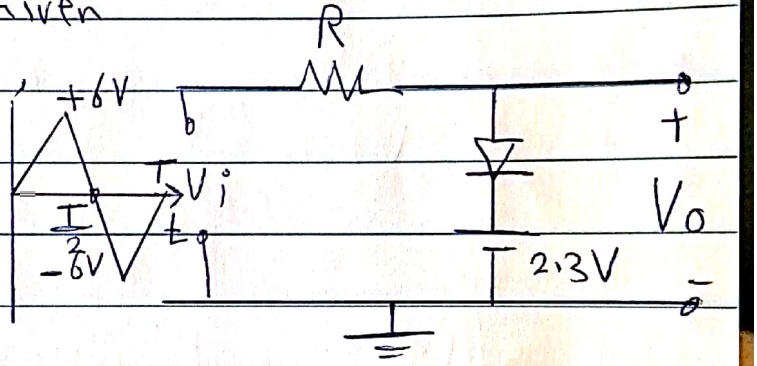
In this H.C ($V_o = V_i$)



* The type of clipping is positive clipping.
* The clipping level is +2V
* The shape of the input signal is changed.



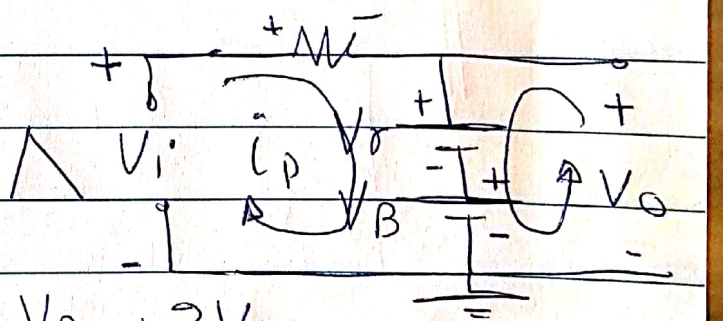
EXA2: For the ckt. shown draw Vo(t) For the indicated input. Given $V_\gamma = 0.7V$, $V_B = 0$,



① For the +ve H.C of Vi, Diode will be FW:

$$-V_i + i_D R + V_\gamma + V_B = 0$$

$$i_D = \frac{V_i - (V_\gamma + V_B)}{R} = \frac{V_i - 3}{R}$$



∴ (i) For $V_i > 0$, $i_D > 0$

Diode is ON,

$$-V_o + V_\gamma + V_B = 0 \Rightarrow V_o = V_\gamma + V_B = +3V$$

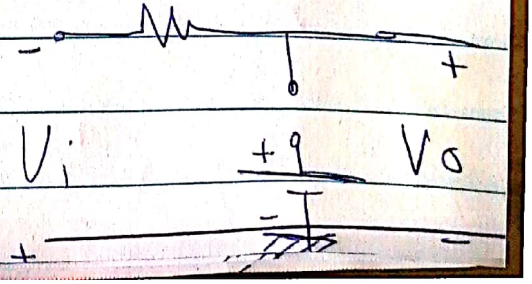
(ii) For $V_i < 3$, $i_D < 0$, Diode → OFF. (O.C)

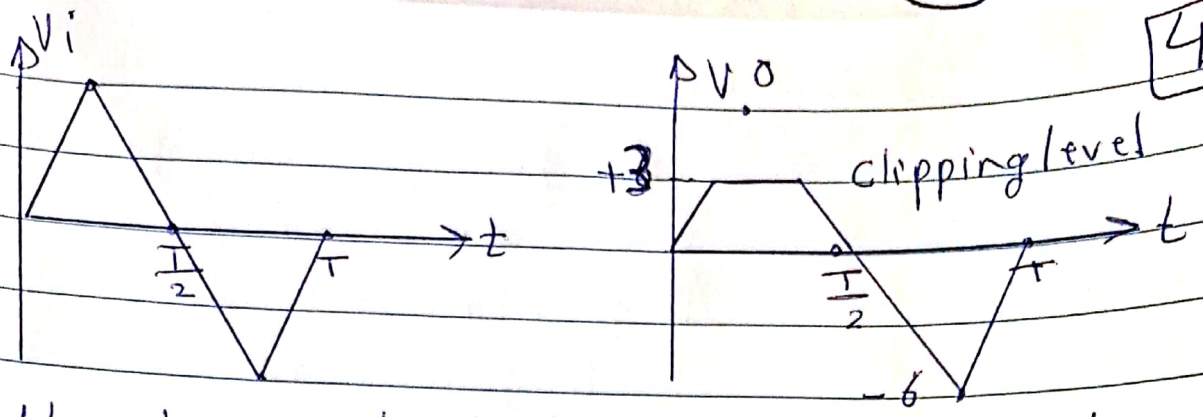
$V_o = V_i$ ($-V_i + V_o = 0 \Rightarrow V_o = V_i$)

② For -ve H.C of Vi, D → Reverse, $i_D \to 0$

$V_o = V_i$.

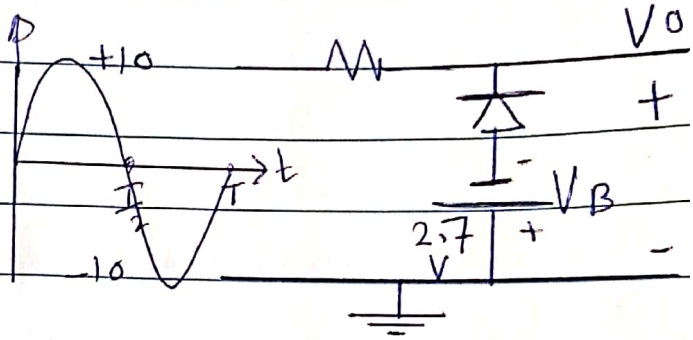
③ For Full cycle of Vi, the o/p will be





i.e the clipping level depends on value of V_B.

Exa 3: For the ckt. shown the diode has $V_\gamma = 0.3V$, $V_f = 0$. Draw $V_o(t)$ for the input shown indicating type of clipping & clipping level.

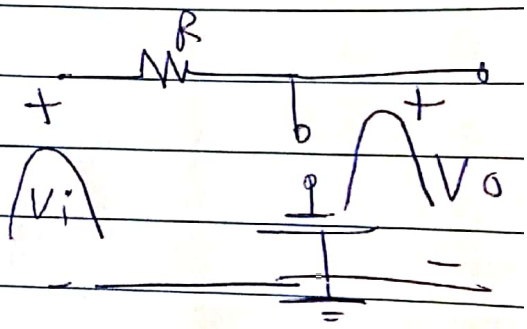


① During +ve H.C of V_i

D → Reverse → O.C → OFF

$-V_i + i_D R + V_\gamma = 0$, but $i_D = 0$

$\therefore V_o = V_i$

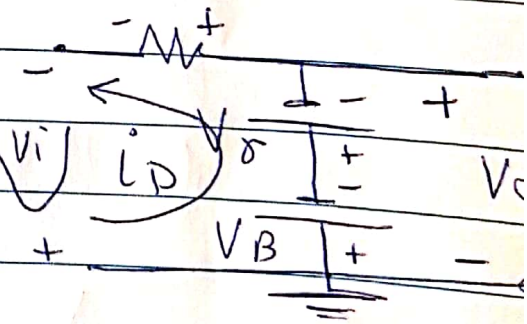


② During -ve H.C of V_i

Diode will be F.W

$-V_i + V_B + V_\gamma + i_D R = 0$

$$i_D = \frac{V_i - (V_B + V_\gamma)}{R} = \frac{V_i - 3}{R}$$



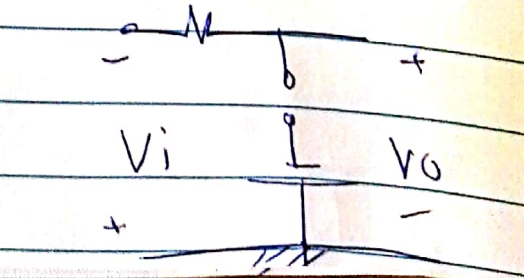
(i) For $V_i > 3$ [$V_i > -3$ i.e For $(-3 \to -10)$]

Diode is ON ($i_D > 0$), $V_o = -(V_B + V_\gamma) = -3V$

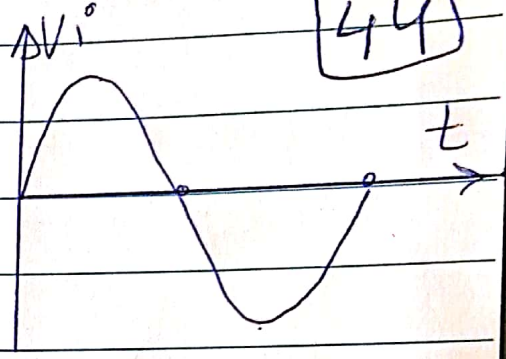
(ii) For $V_i < 3$ [$V_i < -3$ i.e $0 \to -3V$] $i_D < 0$

Diode OFF, $V_o = V_i$

③ For a Full-Cycle of V_i the o/p will be as shown (in next page)

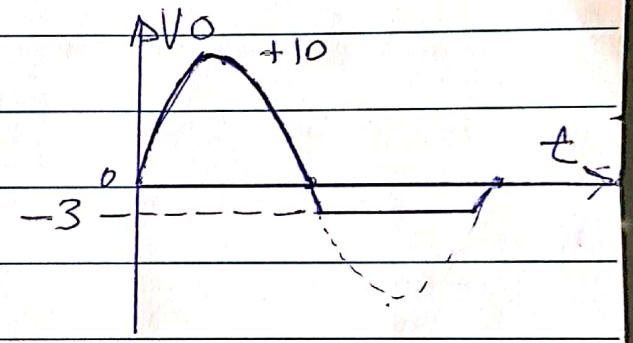


The type of clipping is negative clipping and the clipping level is $\boxed{-3V}$



"So the type of clipping depends on the direction of diode"

"The clipping level depends on the value and polarity of D.C Source connected with Diode".

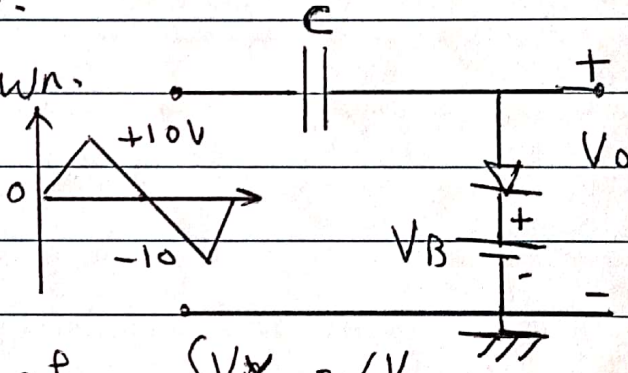


1) Rectifiers : A.C to D.C Convertors
2) clipper
3) clamper:

Clamping

Clamping: changing the D.C level of the A.C input signal to a certain specified level.

* The type of clamping: (+ve or -ve) depends on the Diode direction.
* The clamping level and d.c level depend on Value and polarity of D.C Source Connected with Diode (if any).
* The main difference between clipper and clamper is the capacitor.
* Consider the cct. shown.



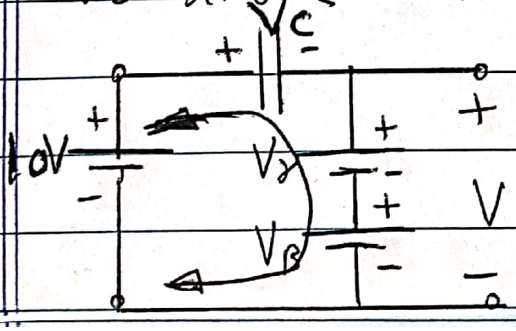
The D.C. level of Vi:

$$D.C.L = \frac{V^+ + (V^-)}{2} = \frac{10-10}{2} = 0$$

How to draw Vo(t) and calculate D.C. level of Vo(t) indicating type of clamping and clamping level.

$V_\gamma = 0.6V$
$V_B = 3.4V$

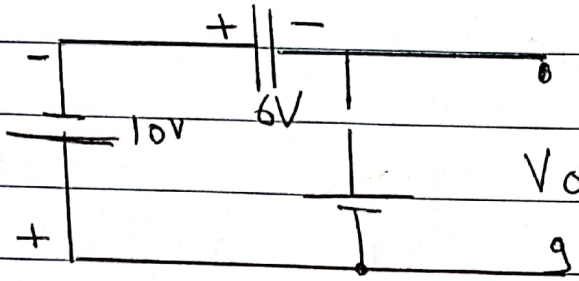
1) Start with Half-cycle of Vi which makes Diode F.W, replace Vi with Batary of Value Vip, replace diode with its model, Calculate Vo and (Vc with its polarity). as follow



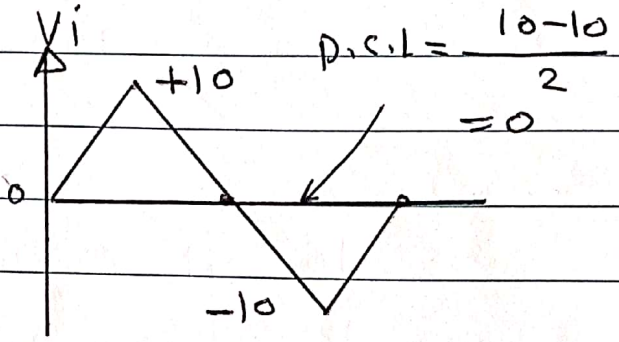
$$-10 + V_C + V_\gamma + V_B = 0 \Rightarrow V_C = 6V$$

$$V_o = 4V$$

2) Consider H.C which makes D → OFF
replace Diode with O.C
= Vi with Batary of Vip.
calculate Vo using (Vc) calculated in (1)

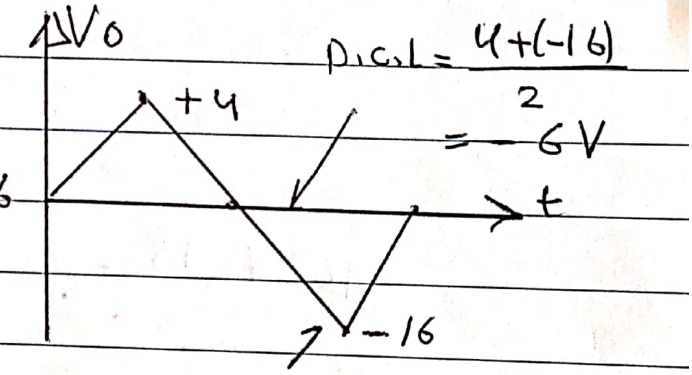


$10 + 6 + V_o = 0$
$\therefore V_o = -16\,V$

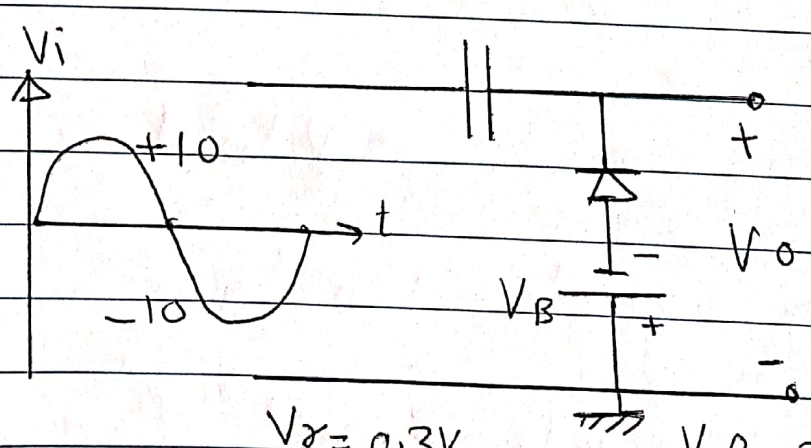


* This is −ve clamping with −ve level

Notic:
1) The shape of Vi is not changed.
2) The peak-to-peak Value of Vi is not changed.

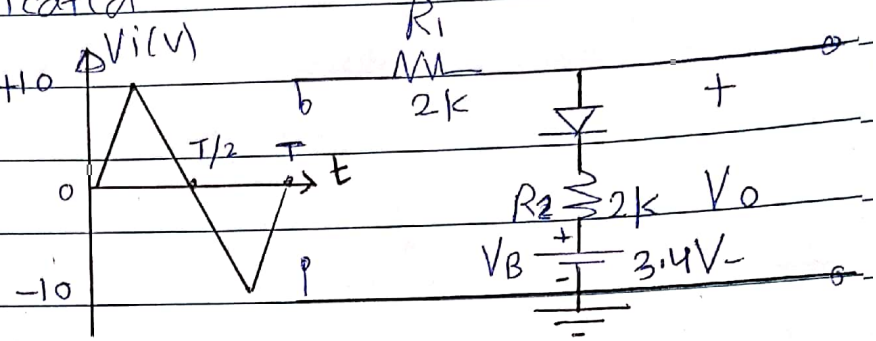


3) If the direction of Diode is changed the type of clamping will be +ve.
4) If the value of V_B is changed then D.C. level will be changed.



H.W
Draw Vo(t) indicating type and D.C level

EXA4: For the cct. shown, the diode has $V_\gamma = 0.6V$, $V_f = 0$, draw $V_o(t)$ For the indicated input.

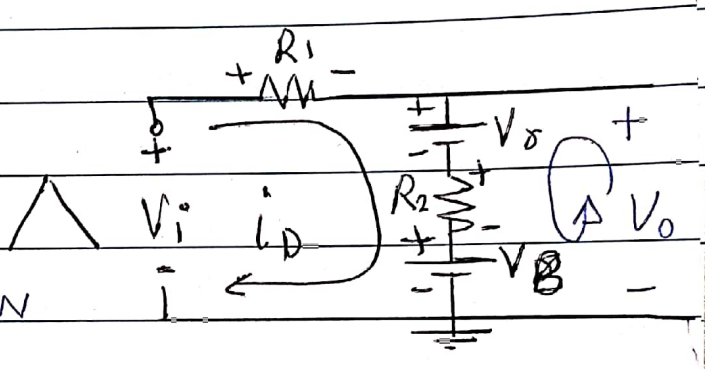


Solution:

① During +ve H.C of V_i, the diode is F.W (replace it by V_γ)

$$-V_i + i_D R_1 + V_\gamma + i_D R_2 + V_B = 0$$

$$i_D = \frac{V_i - (V_\gamma + V_B)}{R_1 + R_2} = \frac{V_i - 4}{R_1 + R_2}$$



(i) For $V_i > 4V$, $i_D > 0$, D → ON

$$-V_o + V_\gamma + i_D R_2 + V_B = 0$$

$$\therefore V_o = V_\gamma + V_B + i_D R_2 = 4 + i_D R_2 = 4 + \frac{V_i - 4}{R_1 + R_2} \cdot R_2$$

at the instant when $V_i = 10$, $V_o = 4 + (10-4)\frac{2}{2+2} = 7V$

i.e when D is "ON", $V_o = 4 + (V_i - 4) \times \frac{2}{4} = 2 + 0.5V_i$

(ii) For $V_i < 4$, $i_D < 0$, Diode is OFF

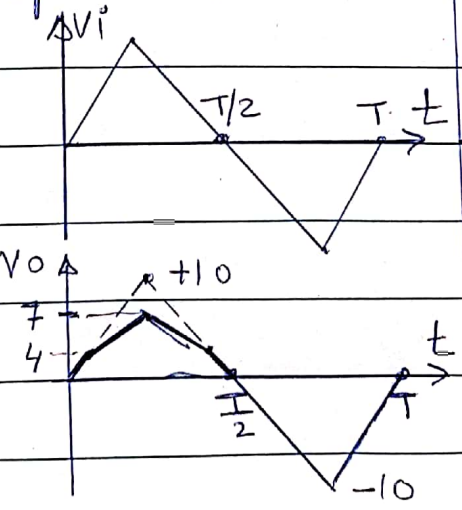
$i_D = 0$, $\boxed{V_o = V_i - i_D R_1 = V_i}$

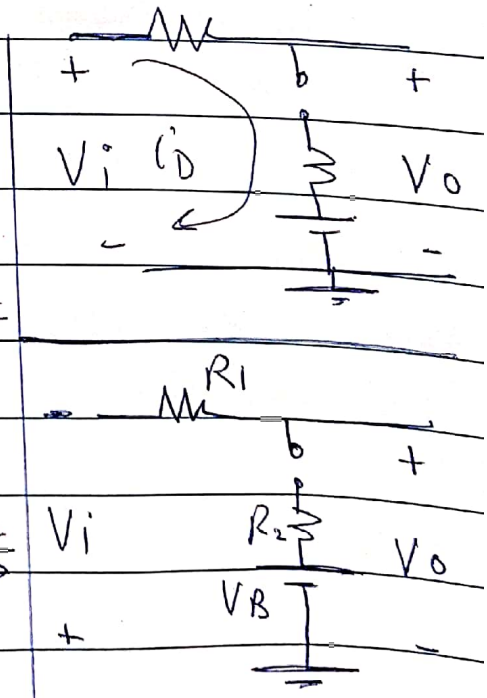
② For -ve H.C of V_i, D → Rev

Diode is OFF → open-ckt.

$\boxed{V_o = V_i}$

*when there is a resistance in Series with Diode in output loop "No clipping".

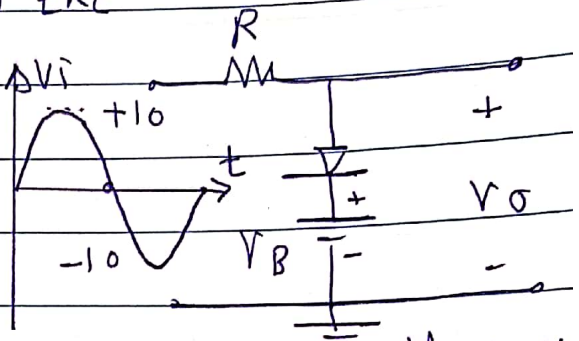




Transfer characteristics

T.C: It is a plot of V_o versus V_i for the cct.

EXAMPLE: For the cct. shown draw the Transfer characteristics: V_o versus V_i



$V_\gamma = 0.6V$, $V_B = 1.4V$

① For +ve H.C of V_i

D → F.W

$-V_i + i_D R + V_\gamma + V_B = 0$

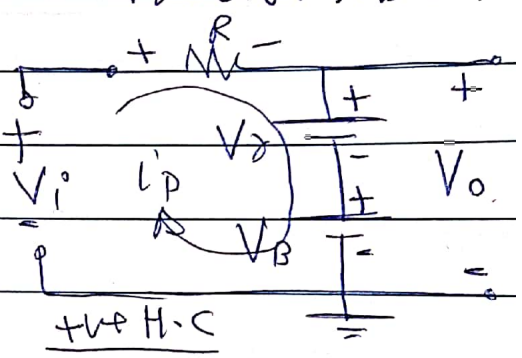
$i_D = \frac{V_i - (V_\gamma + V_B)}{R} = \frac{V_i - 2}{R}$

(i) For $V_i > 2$, $i_D > 0$, D → ON

$V_o = V_\gamma + V_B = 2V$ ——— (1)

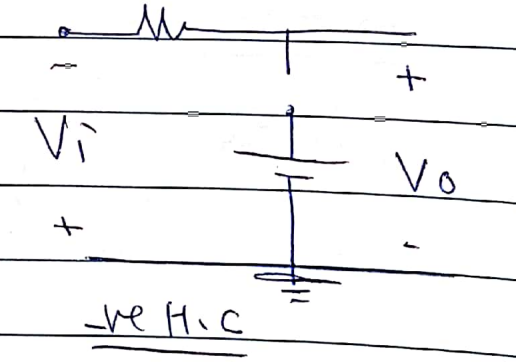
(ii) For $V_i < 2$, $i_D < 0$, D → OFF

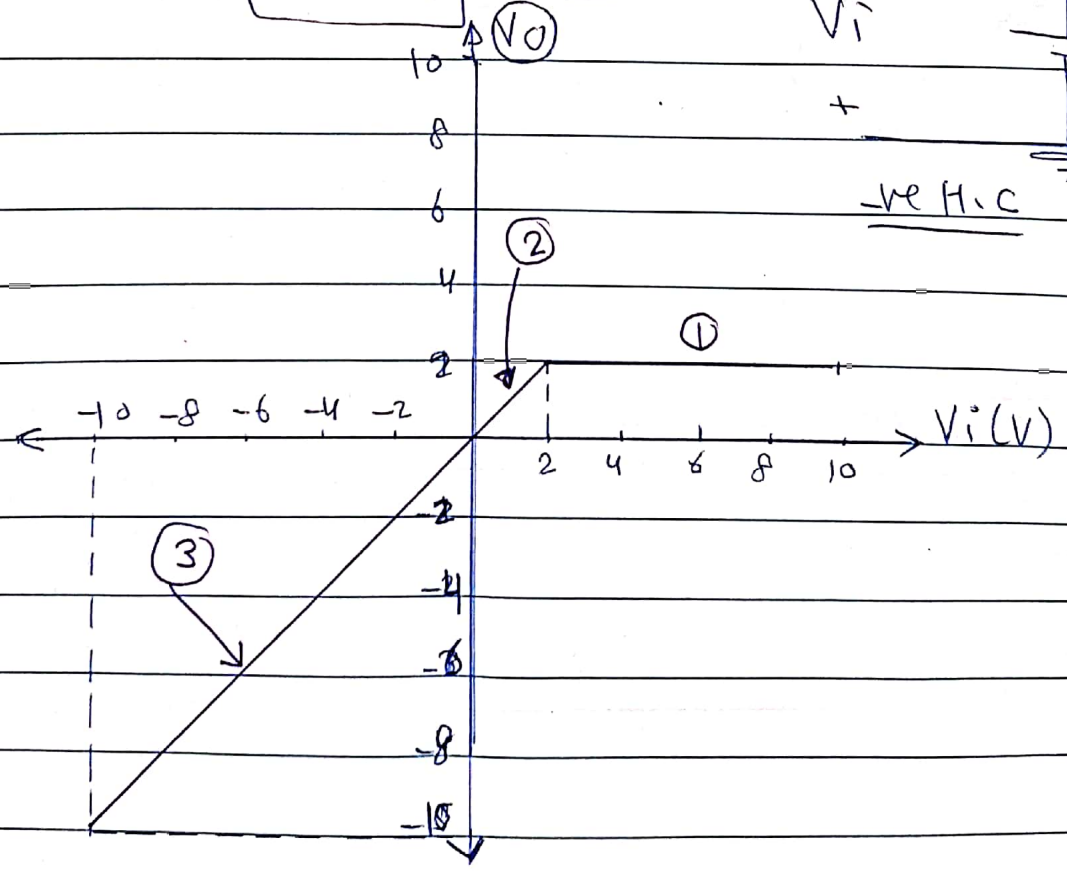
$\boxed{V_o = V_i}$ ——— (2)



② For -ve H.C, D → Rev

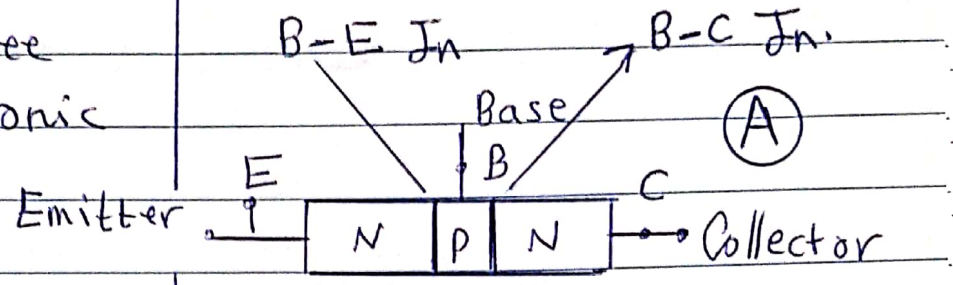
open-ckt. → $\boxed{V_o = V_i}$ ——— (3)





Bipolar Junction Transistor BJT

* BJT is a three terminal electronic device
* E → Emitter
  B → Base
  C → Collector
* It Can be NPN or PNP
* It Contains two P-N Junctions.
  B-E Jn: Base-Emitter Junction.
  B-C Jn: Base-Collector Junction.
* The arrow direction in the Emitter represents the Conventional direction of Emitter Current, which is the direction of hde movement
* In NPN: it is out of Emitter
* In PNP, it is "IN" Emitter.
* E, B, C are different in area and Carrier Concentration.



NPN Transistor

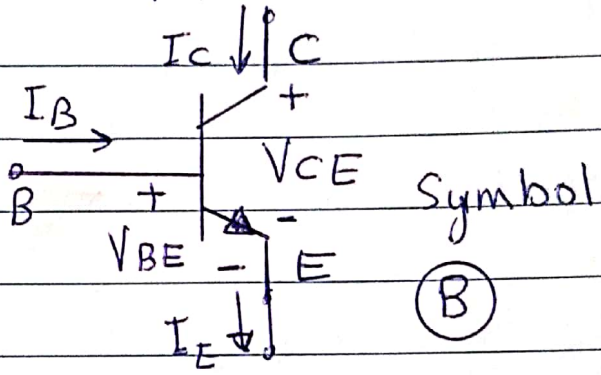
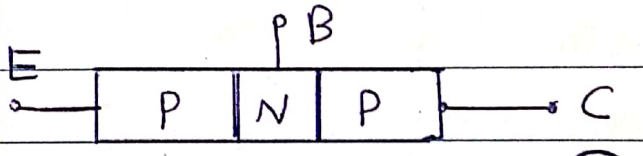


Fig. 1 NPN Tran.



PNP Transistor

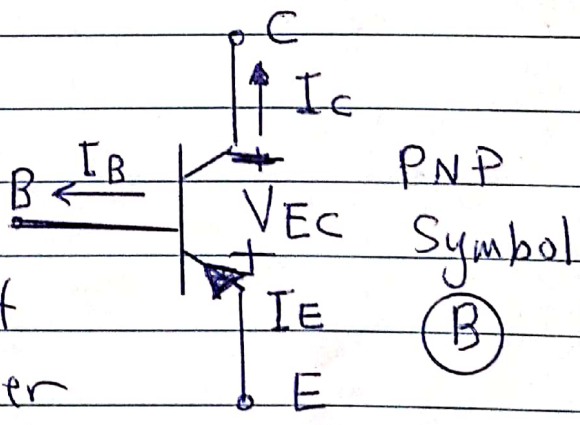
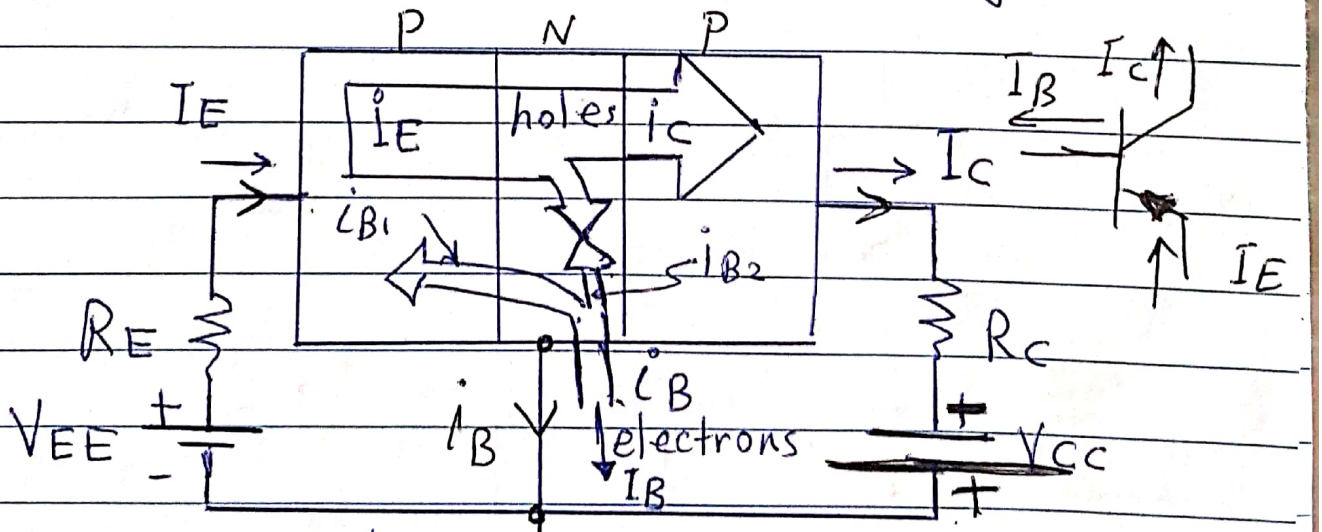


Fig. 2 PNP Tran.

* Normally the doping concentrations in E, B, C are 10^{19}, 10^{17}, 10^{15} / Cm^3 respectively, So even though both ends either P or N, the BJT is "NOT" reversable device.
* The Base is thin and has low doping level Compared to Emitter, to minimize number of Carriers lost by recombination in Base Regn.
* The structure, Symbols, Currents and Voltage notations with their directions and polarities are shown in Fig. 1 and Fig. 2 for NPN & PNP transistors respectivily.
* Since the BJT has two PN Jns. So it can be biased in ONE of the following modes:

① Forward Active Mode "F.A.M".

In this mode, the B-E Jn must F.W biased and B-C Jn. must be Rev. biased. Consider NPN Transistor in FAM shown in Fig. 3



Electrons and holes Currents in PNP Trans. biased in FAM.

Currents in FAM:

Since B-E Jn. is F.W biased, i_E is given by:

$$i_E = I_{EO}\, e^{\frac{V_{EB}}{V_T}}$$

where V_{EB} is the voltage between E and B.
with E is +ve with respect to base.

The collector Current i_C is the major Component of i_E and is given by:

$$i_C = \alpha i_E = I_S\, e^{\frac{V_{EB}}{V_T}} \quad (0.95 < \alpha < 1)$$

where α is Current gain in Common-Base cct.

$$i_B = i_{B_1} + i_{B_2}$$

where i_{B_1}: diffusion Components, electrons flow from base to Emitter.

i_{B_2}: Compensation Components, Compensate electrons lost in recombination in base.

i_{B_1} & i_{B_2} relate exponentionaly with V_{EB}

$$i_B = I_{BO}\, e^{\frac{V_{EB}}{V_T}} = \frac{I_S}{\beta}\, e^{\frac{V_{EB}}{V_T}}$$

where β is the Common-Emitter Current gain of the PNP device.

Currents relation in FAM:

The following relations are satisfied:

$$i_E = i_C + i_B \cdots (1), \quad i_C = \beta i_B \cdots (2)$$

$$i_E = (1+\beta) i_B \ (3), \quad i_C = \left(\frac{\beta}{1+\beta}\right) i_E = \alpha i_E \ (4)$$

where $\alpha = (\beta / \beta+1)$.

where α: Current-gain in C.B ccts. and it is close to (1).

$\alpha = \frac{\beta}{\beta+1}$, for $\beta = 100$, $\alpha = \frac{100}{101} = 0.99$.

and For $\alpha = 0.98$, $\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$

Summary of BJT operation, (In FAM)

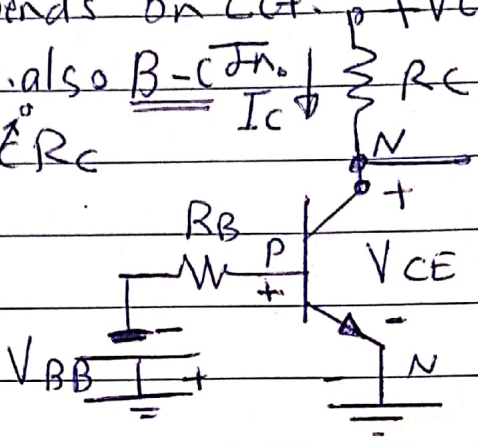
In F.W biased B-E Jn, the maj. Carriers are forced to cross the Jn and be in Base Regn., the Rev. bias B-C Jn. will Collect the maj. Carrier from base due to an E-field on Collector. Very Small Component will be lost in base by recombination.
As. Long as B-E → F.W & B-C → Rev., the Emitter will continue emitting maj. Carriers and Collector Collect them. Creating a Current flowing Conventionaly out of E in NPN and IN E - For PNP. (

(2) Saturation Mode:

In this mode B-E Jn is F.W, B-C Jn is F.W the BJT behaves as a closed-Swith with $I_C > 0$ and $V_{CE} < V_{CE(sat)}$ or < 0 (For Ideal BJT)

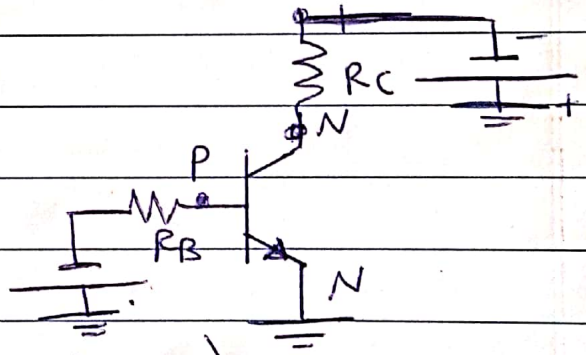
③ Cut-OFF mode:

The BJT will be in this mode when:
B-E Jn: Reverse Biase, B-C Jn → Rev. Bias.
The BJT will behave as an open-switch with $I_C = 0$, $V_{CE} > 0$ depends on Ckt.
Here: B-E Jn is Rev. also B-C Jn. $I_C = 0$
So $I_C = 0$, $V_{CE} = V_{CC} - I_C R_C$
So $V_{CE} = V_{CC}$.



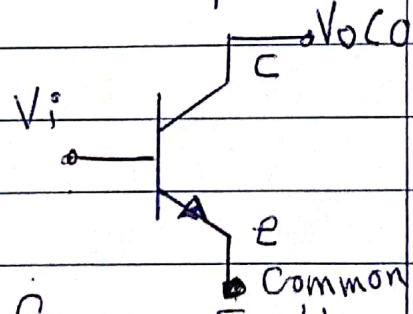
④ Inverse F.A.M

In this mode B-E → Rev. & B-C ⇒ F.W
the BJT has certain Applications.

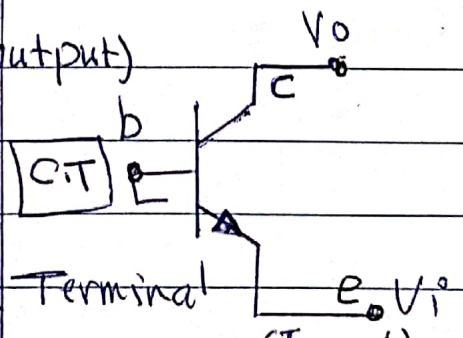


BJT Configurations (Connections)

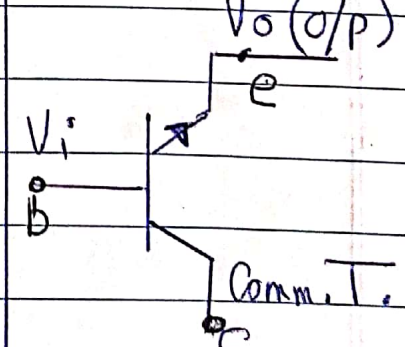
Since BJT is a three-terminals device, so it Can be Connected in ONE of the followings config. as an Amplifier.



Common-Emitter cct. (C.E)



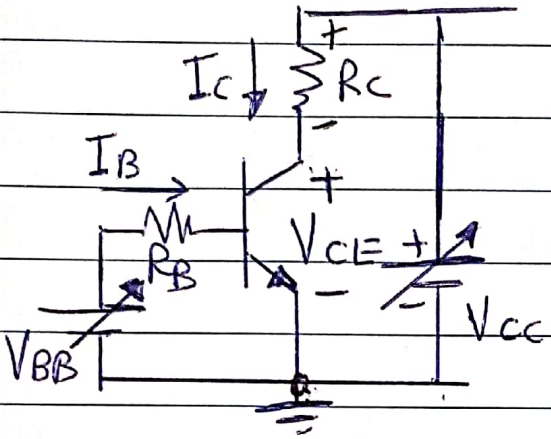
Common-Base (C.B) cct.

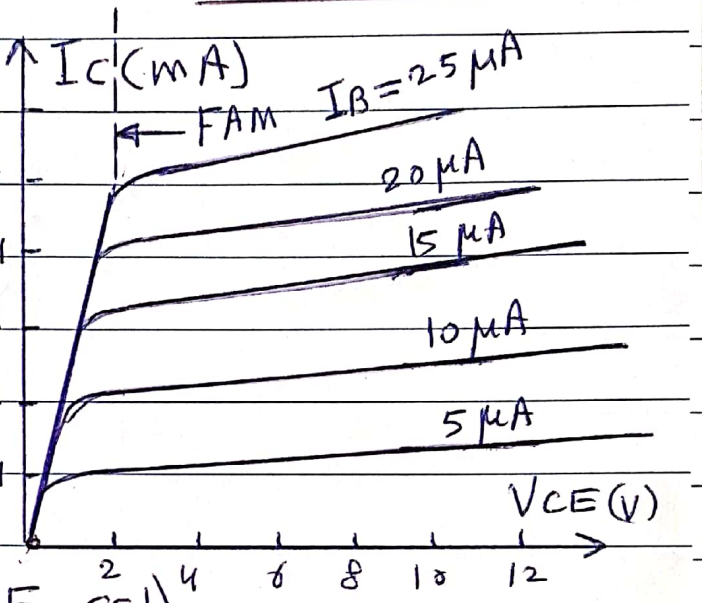


Common-Collect. (C.C) cct.

Current-Voltage Characteristics

It is a plote of transistor Current Versus transistor Voltage For the output loop." It is related to the Device its self. For the Common-Emitter cct. Configuration shown in Fig. with NPN BJT.

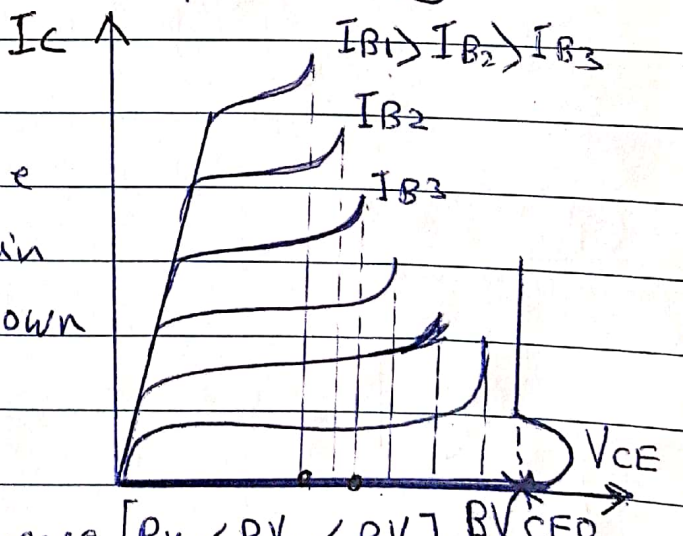




For this configuration (C.E cct)
It is a plote of Collector Current Ic(mA) Versus Collector-Emitter Voltage VCE(V) For Constant Values of Base Current IB(μA).
Normally it is given in data sheet of Each BJT. or can be obtained experimently in the Lab.

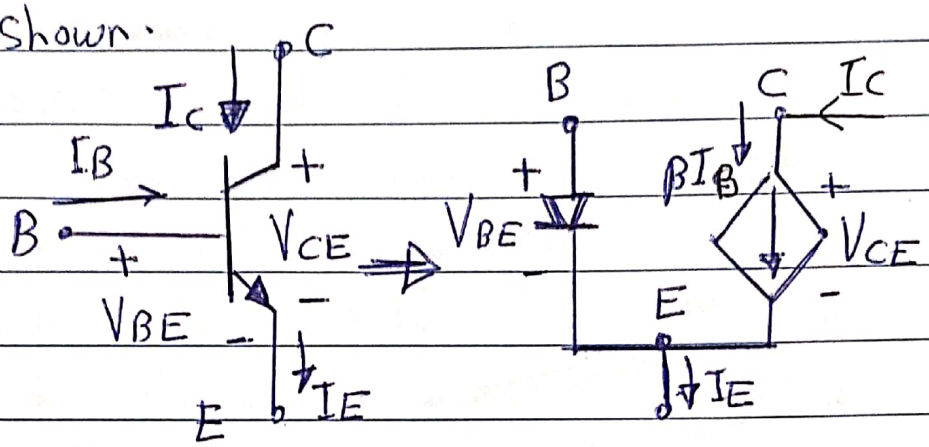
Breakdown Voltage:

We Can't increase the Value of VCE indefinitly, at a Certain Value the BJT will be breakdown this is given in data sheet as BVCEO measured at IB = 0, as ~~IB~~ level increase [BV1 < BV2 < BV3] breakdown happen earilier



D.C Analysis of BJT circuits

When the BJT in FAM, it can be represented by the D.C model shown.



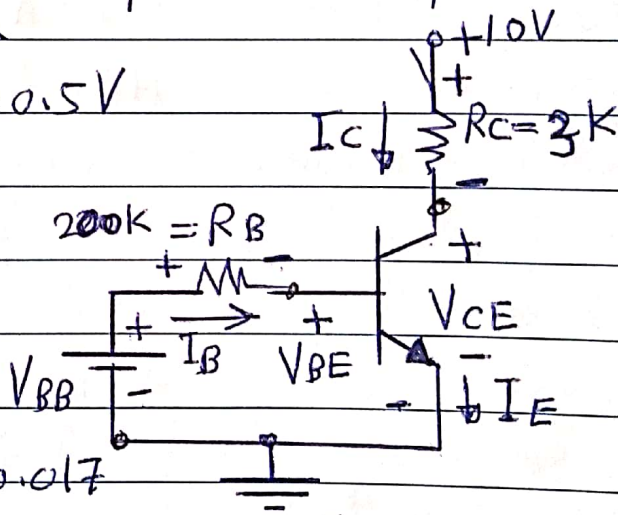
NPN in FAM D.C equivalent cct.

Exa 1:

For the cct. shown, the BJT has: $\{V_{CE(sat)} = 0.3V \;,\; \beta = 100 \;,\; V_{BE(ON)} = 0.6V\}$

Calculate I_B, I_C, I_E, V_{CE} and power dissipation P_D on the transistor when

$V_{BB} = 4V \;,\; V_{BB} = 8V \;,\; V_{BB} = 0.5V$



(i) For $V_{BB} = 4V$

Write KVL For B-E loop:

$-V_{BB} + I_B R_B + V_{BE} = 0$

$\therefore I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{(4 - 0.6)V}{200k}$

$I_B = 0.017\,mA \;,\; I_C = \beta I_B = 100 \times 0.017$

$\therefore I_C = 1.7\,mA \;,\; I_E = I_B + I_C = 1.717\,mA$ or $I_E = (\beta + 1) I_B$

$-10 + I_C R_C + V_{CE} = 0$

$\therefore V_{CE} = 10 - I_C R_C = 10 - 1.7 \times 3 = 4.9V$

Since $I_B > 0$ $\therefore$ B-E Jn F.W & Since $V_{CE} > V_{BE}$

$\therefore$ B-C Jn is Rev. So the BJT in F.A.M

$P_D = I_C V_{CE} + I_B V_{BE}$ but $I_C \gg I_B$ & $V_{CE} > V_{BE}$

$\therefore P_D \simeq I_C . V_{CE} = 1.7(mA) \times (4.9)V = 8.33\,mW.$

ii) For $V_{BB} = 8V$.

Assume the BJT in FAM:

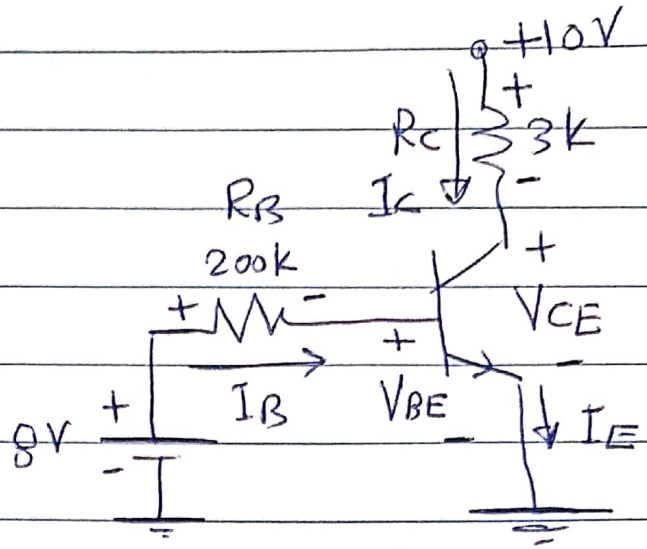
Write KVL For B-E loop:

$-8 + I_B R_B + V_{BE} = 0$

$I_B = \frac{(8-0.6)V}{200k} = 0.037\,mA$

$I_C = \beta I_B = 100 \times 0.037$

$= 3.7\,mA$



$V_{CE} = 10 - I_C R_C = 10 - 3.7 \times 3 = -1.11V$?

Since $I_B > 0 \Rightarrow$ B-E Jn is F.W

and $V_{CE} < V_{BE} \Rightarrow$ B-C Jn is F.W

So the BJT in Saturation mode-

So $V_{CE} = V_{CE(sat)} = 0.3V$ (Given in data sheet)

$I_C = I_{C(sat)} = \frac{10 - V_{CE(sat)}}{R_C} = \frac{(10-0.3)V}{3k} = 3.233\,mA.$

$I_E = I_{Csat} + I_B = 3.233 + 0.017 = 3.25\,mA.$

$P_D = I_C V_{CE} + I_B V_{BE}$ (because $V_{CE} < V_{BE}$, $I_C \not\gg I_B$)

$P_D = 3.233 \times 0.3 + 0.017 \times 0.7 = 0.9699 + 0.0119 = 0.9818$ mW

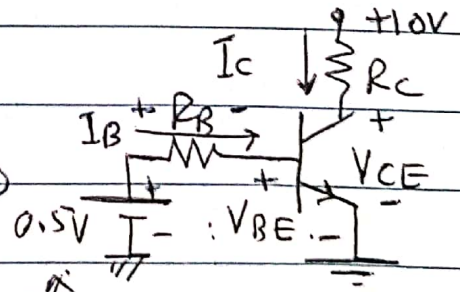
* When BJT in Sat. mode

i) $I_C V_{CE} \not\gg I_B V_{BE}$

ii) $\frac{I_C}{I_B} < \beta$, $\frac{I_{C(sat)}}{I_B} = \boxed{\beta_{Forced}} = \frac{3.233}{0.037} = \boxed{87.4}$.

iii) For $V_{BB} = 0.5V$

$-0.5 + I_B R_B + V_{BE} = 0$, $I_B = \frac{(0.5-0.6)}{R_B} < 0$



$\therefore$ B-E Jn is Rev $\therefore$ BJT is OFF

$I_C = 0$, $I_B = 0$, $I_E = 0$, $V_{CE} = 10 - I_C R_C = 10V$.

$P_D = 0$.

D.C Load line and Q-point

D.C.L.L is a straight line drawn on transistor characteristic characteristic (I_C Vs V_{CE}) represents the relation between(I_C and V_{CE}) For the BJT in the cct.

EXA: For the cct. shown, the BJT has $V_{BE}=0.7$ V and $\beta=100$.

1) Calculate I_B, I_C, V_{CE} & P_D
2) Draw D.C.L.L, indicate its slope and Q-point position.

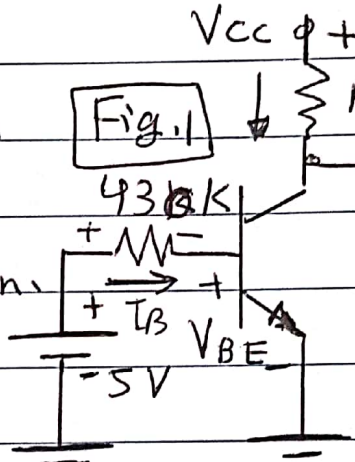


Fig.1

① $-5+43I_B+V_{BE}=0$

$I_B=\frac{(5-0.7)V}{430K}=0.01\ mA$

$I_C=\beta I_B=100\times0.01=1\ mA$

$-10+5I_C+V_{CE}=0$

$\therefore V_{CE}=10-5\times1=5V$

$\therefore I_C=I_{CQ}=1\ mA$

$V_{CE}=V_{CEQ}=5\ V$

$\therefore$ Q-pt(V_{CEQ}, I_{CQ})

Q-pt(5V, 1 mA)

② D.C.L.L: Write KVL For C-E loop: $-V_{CC}+I_CR_C+V_{CE}=0$

$\therefore I_C=\frac{V_{CC}}{R_C}-\frac{V_{CE}}{R_C}$ ——①

$y=b+mx$

$\therefore$ slope $=m=-\frac{1}{R_C}$

OR $V_{CE}=V_{CC}-I_CR_C$ ②

when $m=\frac{-1}{R_C}$

Draw D.C.L.L

① From eqn. ① or ②

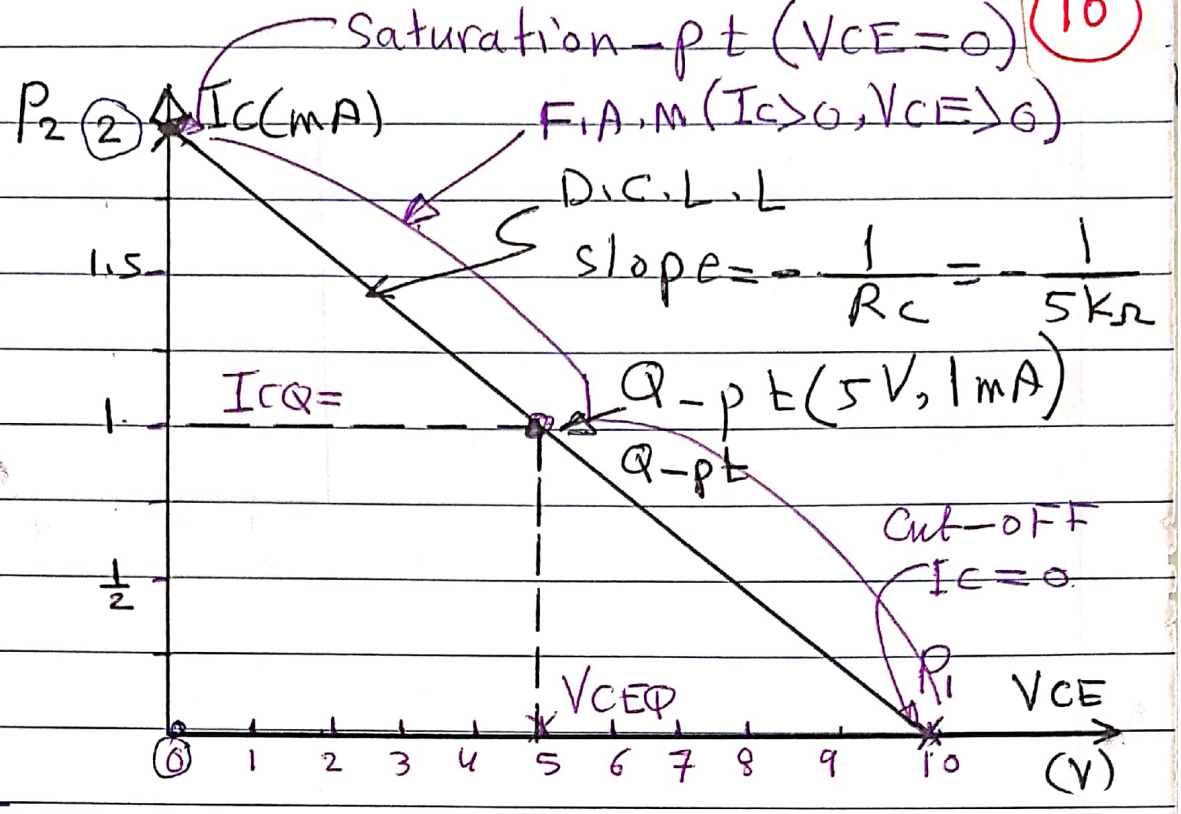
(i) For $I_C=0$, $V_{CE}=V_{CC}=10V$

P_1(10V, 0 mA)

(ii) For $V_{CE}=0$

$I_C=\frac{V_{CC}}{R_C}=\frac{10V}{5K}=2mA$

$\therefore P_2$(0 V, 2mA).



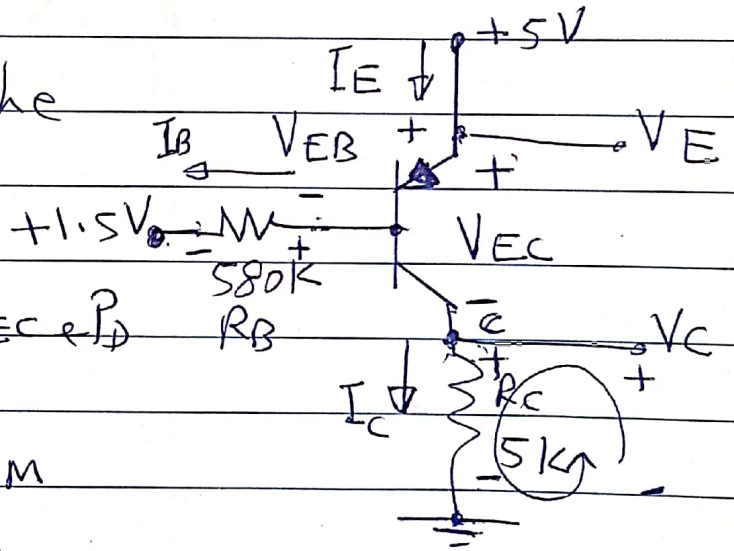
D.C.L.L

Analysis of D.C cct. using PND Transistor:

For the cct. shown, the BJT has: $\beta = 100$

$V_{EB} = 0.6V$.

Calculate I_B, I_C, I_E, V_{EC} & P_D



Solution:

Assume the BJT in FAM

KVL For E-B loop.

$-5 + V_{EB} + I_B R_B + 1.5 = 0$

$\therefore I_B = \frac{5 - 0.6 - 1.5}{580k} = 0.005mA = 5\mu A$

$I_C = \beta I_B = 100 \times 0.005 = 0.5mA$

$V_C = I_C R_C = 0.5 \times 5 = 2.5V$

$-5 + V_{EC} + I_C R_C = 0 \quad \therefore V_{EC} = 2.5V$

Since $I_B > 0$ $\therefore$ B-E Jn $\Rightarrow$ F.W and $V_{EC} > V_{EB}$

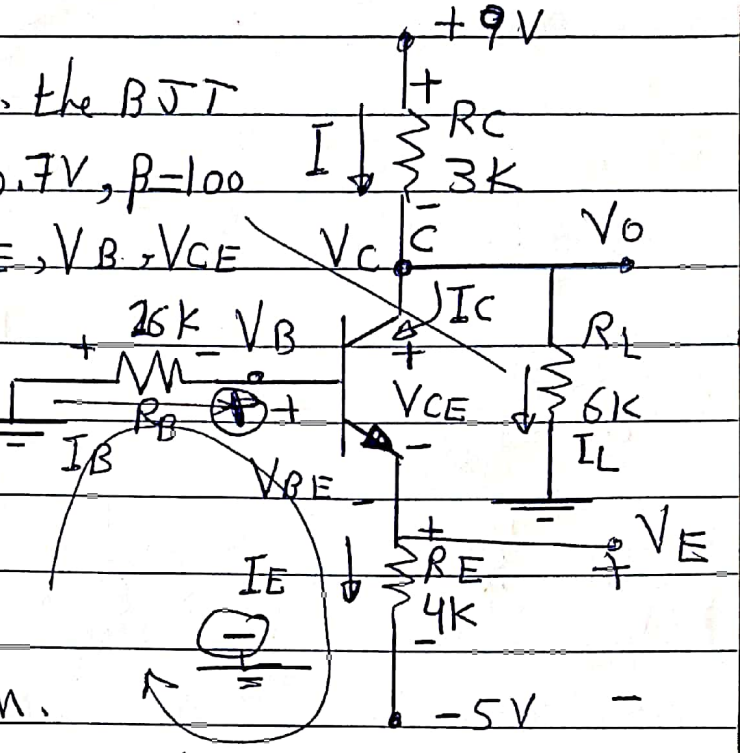
$\therefore$ B-C Jn is Rev. $\therefore$ BJT in F.A.M.

Commonly used D.C cct.

For the cct. shown in Fig. the BJT parameters are: $V_{BE(ON)} = 0.7V$, $\beta = 100$

1) Calculate $I_B, I_C, I_E, V_C, V_E, V_B, V_{CE}$

2) Write D.C.L.L eqn, find its slope and draw D.C.L.L indicating Q-pt. position.



Solution:

Assume the BJT in FAM.

$I_B R_B + V_{BE} + (\beta+1) I_B R_E - 5 = 0$ (KVL For B-E loop)

$$I_B = \frac{(5-0.7)V}{R_B + (\beta+1)R_E} = \frac{4.3V}{26 + 101 \times 4} = \frac{4.7V}{430K} = 0.01\,mA$$

$I_C = \beta I_B = 100 \times 0.01 = 1\,mA$, $I_E = (\beta+1) I_B = 1.01\,mA$

$-9 + I \cdot R_C + V_{CE} + I_E R_E - 5 = 0$

$\therefore V_{CE} = 14 - I R_C - I_E R_E = 14 - 1.01 \times 4 - 3I = 9.96 - 3I$

To Find I we must ~~find~~ write KCL at Node (C)

$$I = I_C + I_L \Rightarrow \frac{9 - V_C}{3K} = 1 + \frac{V_C}{6K}$$

$18 - 2V_C = 6 + V_C$

$12 = 3V_C \Rightarrow V_C = 4V \Rightarrow I = \frac{9-4}{3} = 1.67\,mA$, $I_L = 0.67\,mA$

$\therefore V_{CE} = 9.96 - 1.67 \times 3 = 4.96V$

$P_D = I_C V_{CE} = 4.96\,mW$,

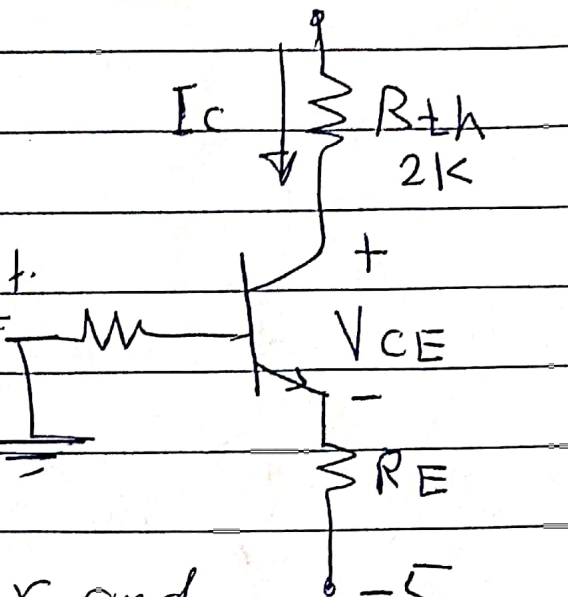
$-V_E + I_E R_E - 5 = 0 \Rightarrow V_E = I_E R_E - 5 = -0.96V$

$I_B R_B + V_B = 0 \Rightarrow V_B = -I_B R_B = -0.26V$

OR: From $V_{BE} = V_B - V_E \Rightarrow V_B = V_{BE} - V_E = -0.26V$

(12)

To Write D.C.L.L eqn.
we must make the cct. as Shown in Fig. (i.e Convert Rc, RL and Vcc into Thevien cct. where:



$R_{th} = R_C // R_{th} = 3 // 6 = 2K\Omega$

$V_{th} = \frac{V_{cc} R_L}{R_C + R_L} = \frac{9 \times 6}{9} = 6V$

(i.e make open-cct. at Collector and look From Collector applying ~~Thevimin Theorm~~.)

Now: Write KVL For C-E loop:

$-V_{th} + I_C R_{th} + V_{CE} + I_E R_E - 5 = 0$

but $I_E = \frac{\beta+1}{\beta} I_C$ (make I_E interms of I_C) !!!

$\therefore V_{CE} = 11 - I_C\left(R_{th} + \frac{\beta+1}{\beta} R_E\right)$ D.C.L.L eqn.

$\therefore$ The slope is: $-1 / \left(R_{th} + \frac{\beta+1}{\beta} R_E\right) \approx -\frac{1}{R_{th} + R_E}$

Q-pt: $V_{CEQ} = V_{CE} = 4.96V$, $I_{CQ} = I_C = 1mA$

* Plote D.C.L.L:

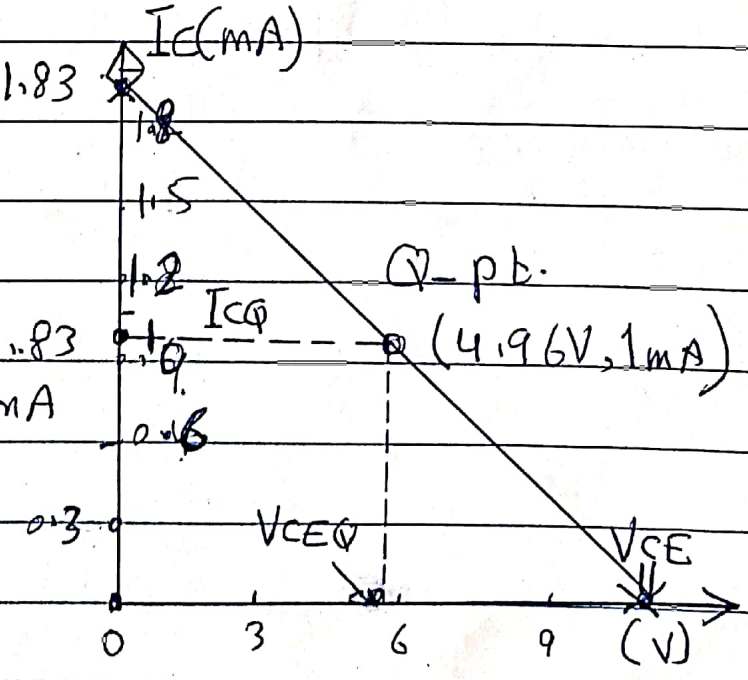
From D.C.L.L eqn.

(i) For $I_C = 0$, $V_{CE} = 11V$

$P_1(11V, 0mA)$.

(ii) For $V_{CE} = 0$, $I_C \approx \frac{11}{6} = 1.83$ mA

$P_2(0V, 1.83mA)$



BJT Biasing

When the BJT is required to be used as an Amplifier, it must be biased in FAM and apply the signal to be amplified. Normally it is required to seperate A.C from D.C. two biasing ccts. are used :

① Single Base Resistor Biasing

C_B is used to isolate D.C from A.C

R_B : Control the base Current I_B

R_C : Control C-E Voltage V_{CE}

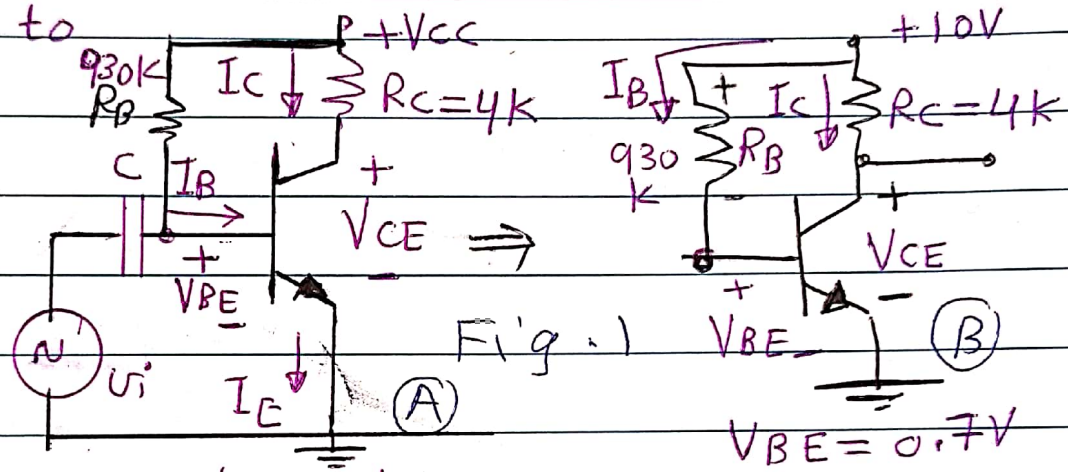


Fig. 1

Ex: For the cct. above calculate

① I_B, I_C, V_{CE} When β is varied From 100 → 200

② Calculate $\Delta I_C/_o$ & $\Delta V_{CE}/_o$ Corespounding to change in β.

---

* For D.C Analysis, C → open-cct ($X_C = \infty$)

$$-10 + I_B R_B + V_{BE} = 0$$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B} = \frac{(10 - 0.7)V}{930K} = 0.01\,mA.$$

① For $\beta = 100$, $I_C = \beta I_B = 1\,mA$

$$-V_{cc} + I_C R_C + V_{CE} = 0$$

$$\therefore V_{CE} = 10 - I_C R_C = 10 - 1 \times 4 = 6V$$

(ii) For $\beta = 200$, $I_C = \beta I_B = 200 \times 0.01 = 2mA$

$V_{CE} = 10 - I_C R_C = 10 - 2 \times 4 = 2V$

$\Delta I_C\% = \frac{I_{C2} - I_{C1}}{I_{C1}} \times 100\% = \frac{2-1}{1} \times 100\% = 100\%$

$\Delta V_{CE}\% = \frac{V_{CE2} - V_{CE1}}{V_{CE1}} \times 100\% = \frac{(2-6)}{6} \times 100\% = -66.6\%$

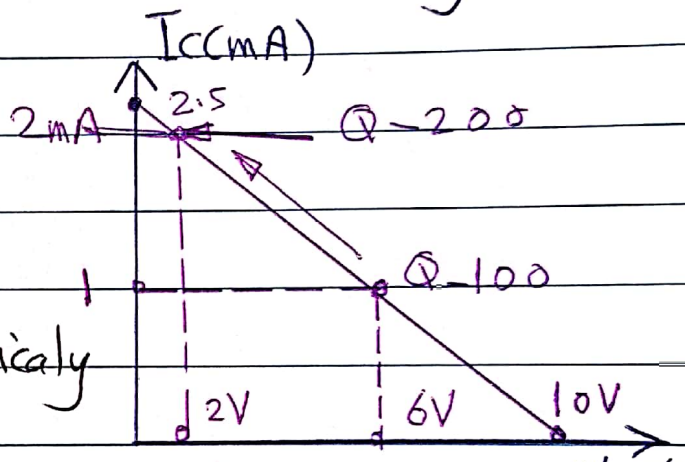
This means: For this cct. when β is increased by 100% (100 → 200), I_C is increased by 100% and V_{CE} decreases by 66%, which indicates:

"The Q-pt. is very sensitive to β Variation OR this cct. has poor biase Stability.

Consider the D.C.L.L and Q-pt. position.

where Q-pt move up twored Sat. point.

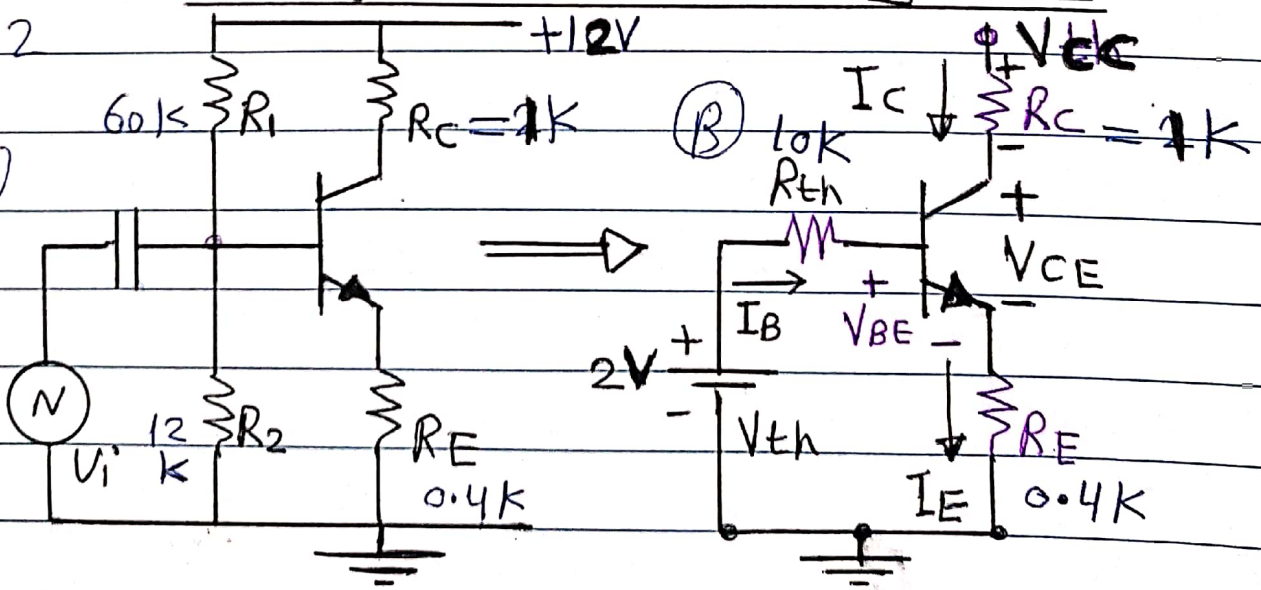
Q-pt is changed dramaticaly with β-Variation.



* This is NOT desired in Amplifier design which may cause diction in A.c output Signal.

(2) Voltage-divider biasing cct.

Fig. 2



Compared to Single-Base Resistor cct. this cct. replaced R_B by two resistors R_1 & R_2 also R_E is used in Emitter. We will see the advantages of this cct. From the following Exampl

EXA: For the cct. shown, the BJT has $V_{BE(ON)} = 0.7V$. ① Calculate I_B, I_C, I_E, V_{CE}. when β is changed from $(100 \rightarrow 200)$

② Calculate $\Delta I_C\%$ and $\Delta V_{CE}\%$ when β Varies from $100 \rightarrow 200$.

Solution: To analyze this cct. it is required to Convert the base-cct. into Thevinin equivalent cct. (Seen beside the original cct).

where: $R_{th} = R_1 // R_2$, $V_{th} = \frac{V_{cc} R_2}{R_1 + R_2}$

"R_{th}: wheen $V_{cc}=0$" "V_{th}: when V_{cc} is present"

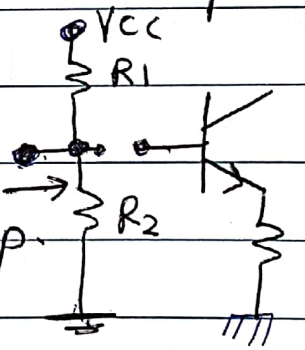


Fig.3

For this example: $V_{th} = \frac{12 \times 12}{(12+60)} = 2V$

$R_{th} = 60 // 12 = 10K\Omega$

To Find I_B: Write KVL For B-E loop.

$-V_{th} + I_B R_{th} + V_{BE} + I_E R_E = 0$

but $I_E = (\beta+1) I_B$ "For $\beta = 100$"

$\therefore -V_{th} + I_B (R_{th} + (\beta+1) R_E) + V_{BE} = 0$

$I_B = (V_{th} - V_{BE}) / [R_{th} + (\beta+1) R_E] = \frac{(2-0.7)V}{(10+101 \times 0.4)K} = 25.8 \mu A$

$I_C = \beta I_B = 100 \times 0.0258 = 2.58 mA$

$-V_{cc} + I_C R_C + V_{CE} + I_E R_E = 0$

$V_{CE} = V_{cc} - I_C R_C - I_E R_E$

$= 12 - 2.58 \times 1 - 2.6 \times 0.4 = 8.38 V$

$I_E = (\beta+1) I_B = 2.6 mA$

(ii) For $\beta = 200$

$$I_B = \frac{(2-0.7)V}{10+201\times0.4} = \frac{1.3V}{90.4k} = 0.0144\,mA$$

$$I_C = \beta I_B = 200 \times 0.0144 = 2.88\,mA$$

$$I_E = (\beta+1) I_B = 2.89\,mA$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 12 - 2.88\times1 - 2.89\times0.4$$

$$= 7.96\,V$$

$$\Delta I_C\% = \frac{I_{C2} - I_{C1}}{I_{C1}} \times 100\% = \frac{2.88-2.58}{2.58} \times 100\% = 11\%$$

$$\Delta V_{CE}\% = \frac{V_{CE2} - V_{CE1}}{V_{CE1}} \times 100\%$$

$$= \frac{7.96-8.38}{8.38} \times 100\% = -5\%$$

This indicates that when β is increased by 100% I_C increased by only 11% and V_{CE} decreased by 5% only. i.e this cct has Q-pt which is less dependant on β. (See Fig. shown)

This means: This cct. has a very good biase Stability

- Hence R_E is used to Stabilise Q-pt against β-Variation.

only very Small change in Q-pt position which very desired and preferable in Amplifier design.

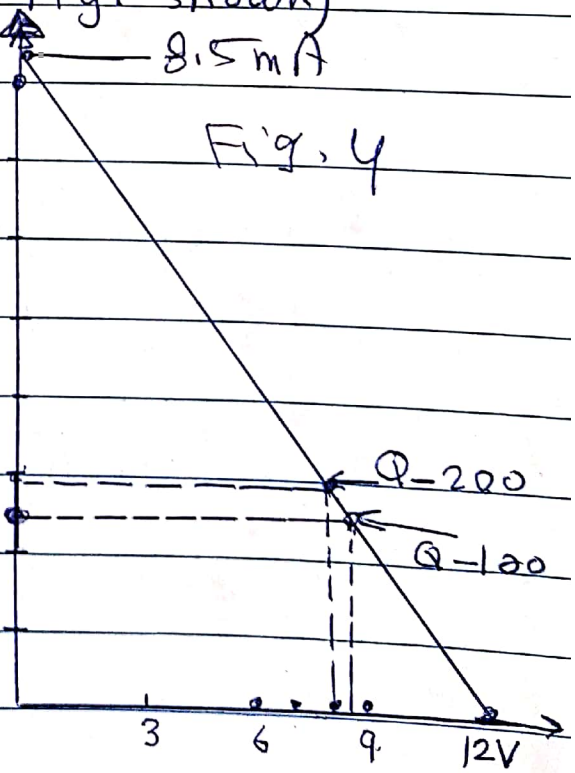


Fig. 4

Bias Stable Condition

Consider the voltage divider cct. discussed later and expression of $I_B = \frac{V_{th} - V_{BE}}{R_{th} + (\beta+1) R_E}$

Since $I_C = \beta I_B$, $\therefore I_C = \frac{\beta (V_{th} - V_{BE})}{R_{th} + (\beta+1) R_E}$

IF $R_{th} << (\beta+1) R_E$ and $\beta >> 1$ then: $\boxed{I_C \simeq \frac{V_{th} - V_{BE}}{R_E}}$

This mean that I_C will be independant on β. i.e If this condition is satisfied ($R_{th} << (\beta+1) R_E$ & $\beta >> 1$) then Q-pt will be independant on β and the cct. will be bias-Stable. So:

(1) For a voltage-divider cct. when $\boxed{R_{th} \leq 0.1 (\beta+1) R_E}$ the cct. is $\boxed{\text{bias-stable}}$

(2) For design a bias-stable cct. choose $R_{th} = 0.1 (\beta+1) R_E$

EXAMPLE: Design a bias-Stable cct. to have $I_{CQ} = 1\,mA$, $V_{CEQ} = 5$. Use a BJT with with $\beta = 100$, $V_{BE} = 0.7V$, $R_E = 0.2 K\Omega$, $V_{CC} = 10V$ (Hence Find R_1, R_2, R_C).

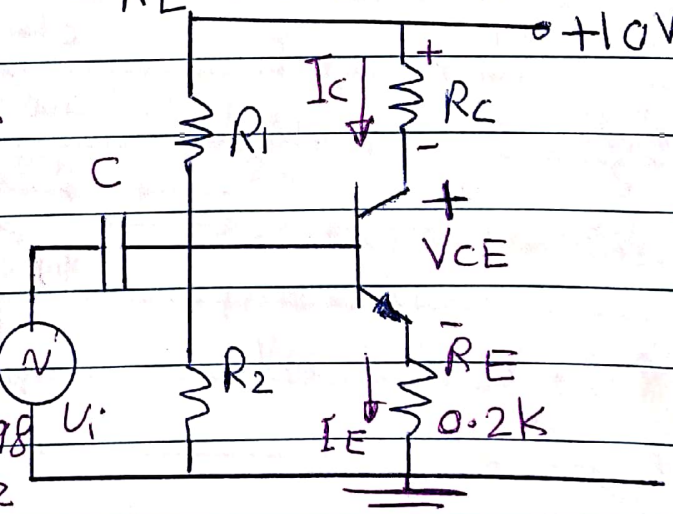
R_E? KVL For C-E loop:

$-10 + I_C R_C + V_{CE} + I_E R_E = 0$

$I_C R_C = 10 - V_{CE} - I_E R_E$

$I_E = \frac{(\beta+1)}{\beta} I_C = 1.01\,mA$

$R_C = \frac{10 - 5 - 1.01 \times 0.2}{I_C} = 4.798\ K\Omega$



To Find R_1 & R_2??

Remember Thevenin eqnt. cct.

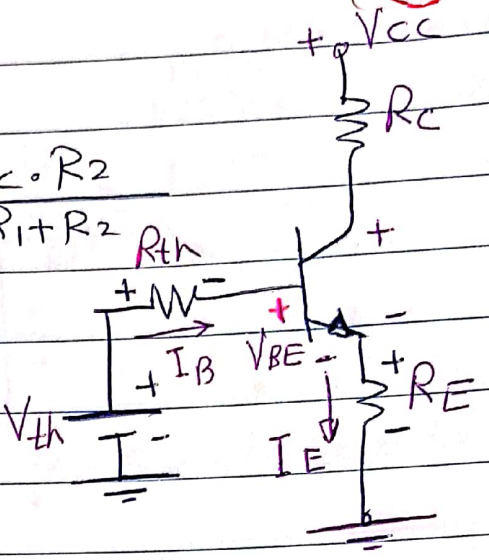
where: $R_{th} = R_1 // R_2$, $V_{th} = \frac{V_{cc} \cdot R_2}{R_1 + R_2}$

For a bias-stable:

choose $R_{th} = 0.1(\beta+1)R_E$

∴ choose $R_{th} = 0.1(101)0.2$

$= 2.02\,K\Omega$



$R_1 V_{th} = \frac{V_{cc} R_2}{R_1 + R_2} \times R_1 \rightarrow R_{th}$

∴ $R_1 = \frac{V_{cc}}{V_{th}} R_{th}$

and $V_{th} = I_B R_{th} + V_{BE} + I_E R_E$ & $I_B = \frac{I_C}{\beta} = 0.01$ mA

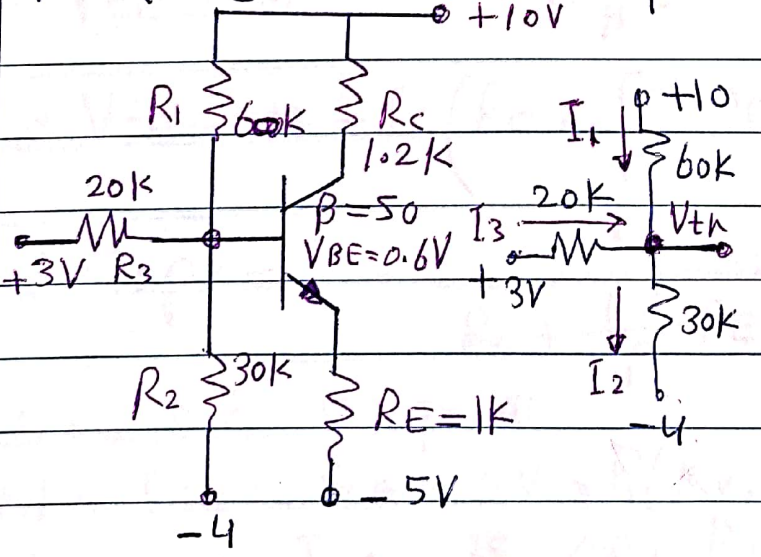
∴ $V_{th} = 0.01 \times 2.02 + 0.7 + 1.01 \times 0.2 = 0.9222\,V$

∴ $R_1 = \frac{10\,V}{0.9222\,V} \times 2.02 = 21.9\,K\Omega$

but $R_{th} = R_1 // R_2 = \frac{R_1 \cdot R_2}{R_1 + R_2}$

∴ $R_2 = \frac{R_1 \cdot R_{th}}{R_1 - R_{th}} = \frac{21.9 \times 2.02}{21.9 - 2.02} = 2.225\,K\Omega$

EXAMPLE: For the cct. shown, ① Find R_{th}, V_{th}, I_{CQ} & V_{CEQ}. ② Write D.C.L.L eqn and Find slope? Draw D.C.L.L



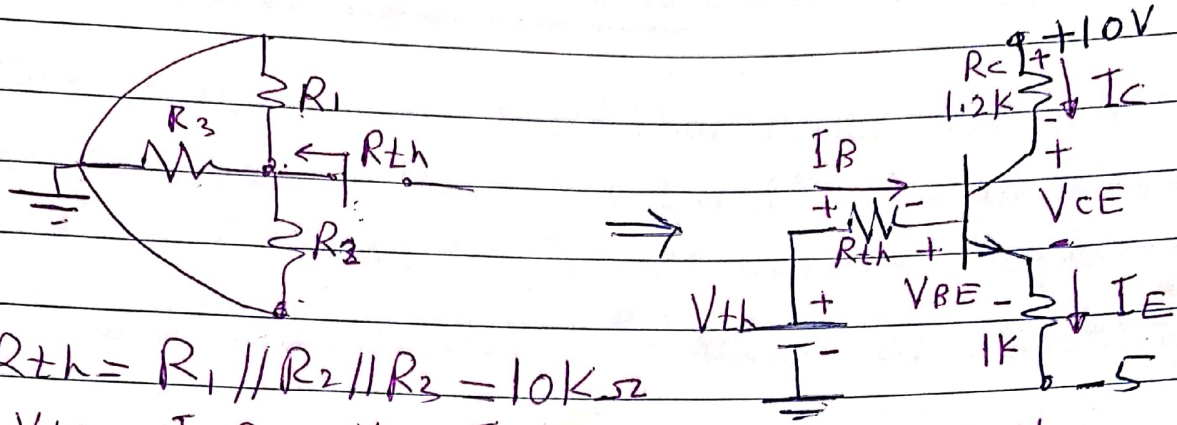
$I_1 + I_3 = I_2$

$\frac{3 - V_{th}}{20} + \frac{10 - V_{th}}{60} = \frac{V_{th} + 4}{30}$

$9 - 3V_{th} + 1.0 - V_{th} = 2V_{th} + 8$

$11 = 6\,V_{th}$

∴ $V_{th} = \frac{11}{6} = 1.83\,V$



$R_{th} = R_1 // R_2 // R_3 = 10K\Omega$

$-V_{th} + I_B R_{th} + V_{BE} + I_E R_E - 5 = 0$ $\quad \beta = 50, V_{BE} = 0.6V$

but $I_E = (\beta+1) I_B$

$\therefore I_B = \frac{V_{th} + 5 - V_{BE}}{R_{th} + (\beta+1) R_E} = \frac{(1.83 + 5 - 0.6)V}{(10 + 51 \times 1)K} = 0.102\ mA$

$I_C = \beta I_B = 50 \times 0.102 = 5.1\ mA.$

$I_E = (\beta+1) I_B = 51 \times 0.102 = 5.202\ mA.$

To Find V_{CE}, Write KVL For C-E loop.

$-V_{CC} + I_C R_C + V_{CE} + I_E R_E - 5 = 0$

$\therefore V_{CE} = 10 + 5 - 5.1 \times 1.2 - 5.202 \times 1 = 3.678\ V$

* Since $I_B > 0$, $V_{CE} > V_{BE}$ $\therefore$ BJT in FAM.

D.C.L.L eqn:

$-V_{CC} + I_C R_C + V_{CE} + I_E R_E - 5 = 0$

but $I_E = \left(\frac{\beta+1}{\beta}\right) I_C$

$\therefore V_{CE} = 15 - I_C R_C - \left(\frac{\beta+1}{\beta}\right) R_E I_C$

$\therefore V_{CE} = 15 - I_C \left(R_C + \frac{\beta+1}{\beta} R_E\right)$ ①

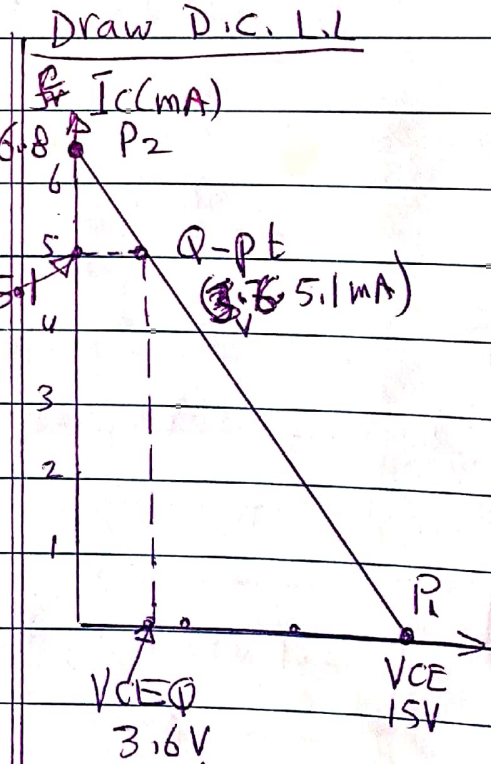
$\therefore Slope = -\frac{1}{R_C + \frac{\beta+1}{\beta} R_E}$

From D.C.L.L eqn. ①

when $I_C = 0$, $V_{CE} = 15V \Rightarrow P_1(15V, 0mA)$

when $V_{CE} = 0$, $I_C = \frac{15}{1.2+1} = 6.8mA$, $P_2(0, 6.8mA)$

Draw D.C.L.L



Multistage Circuits

These ccts. contain more than ONE transistor which can be of the same type (PNP) or (NPN) or two types (NPN & PNP). These can be Connected as "Cascade Connection" or "Cascode Connection"

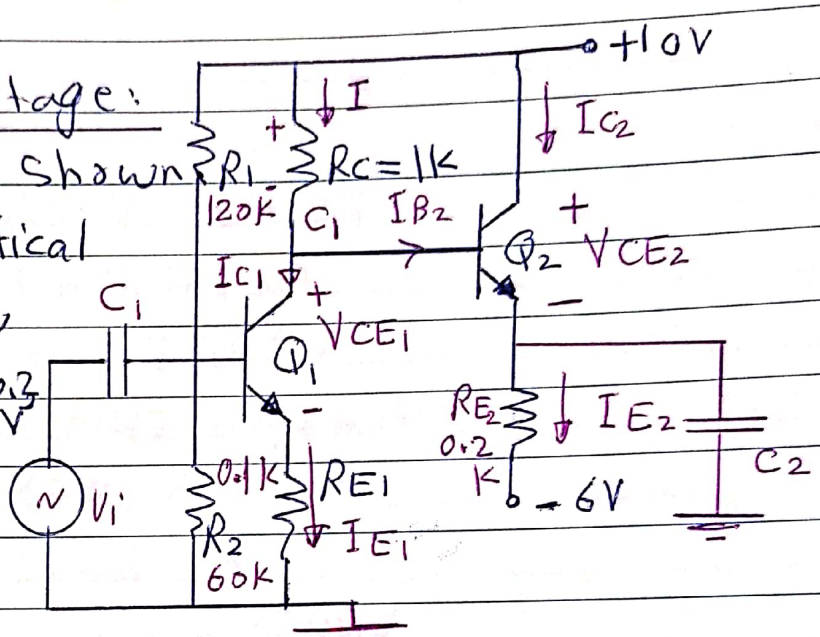
① Cascade Multistage:

Consider the cct. shown "Q_1 & Q_2 are identical BJTs with $\beta = 100$, $V_{BE} = 0.6V$, $V_{CE(sat)} = 0.3V$

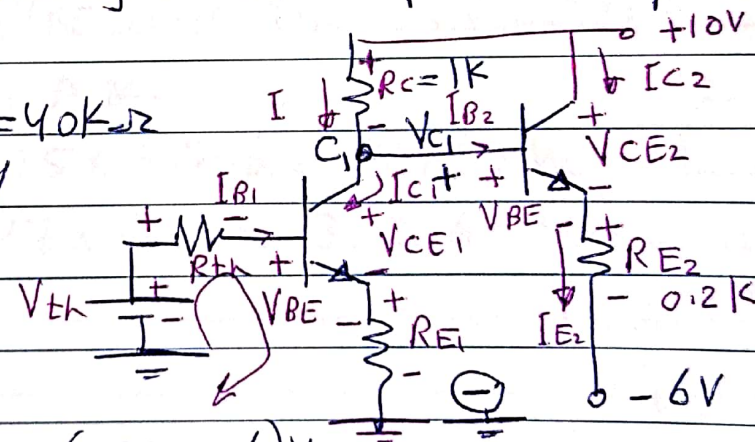
Calculate:

$I_{B1}, I_{C1}, V_{CE1}, P_{D1}$

$I_{B2}, I_{C2}, V_{CE2}, P_{D2}$



Solution: For D.C Analysis all caps. are open.



$R_{th} = R_1 // R_2 = 120 // 60 = 40K\Omega$

$V_{th} = \frac{10 \times 60}{180} = 3.33V$

$-V_{th} + I_{B1} R_{th} + V_{BE} + (\beta+1) I_{B1} R_{E1} = 0$

$\therefore I_{B1} = \frac{V_{th} - V_{BE}}{R_{th} + (\beta+1) R_{E1}} = \frac{(3.33 - 0.6)V}{(40 + 101 \times 0.1)K} = 0.0525\ mA$

$I_{C1} = \beta I_{B1} = 100 \times 0.0525 = 5.25\ mA$

$I_{E1} = (\beta+1) I_{B1} = 5.3\ mA$

$-10 + I \cdot R_C + V_{CE1} + I_{E1} R_{E1} = 0$

$V_{CE1} = 10 - I R_C - 5.3 \times 0.1$

$V_{CE1} = 9.47 - I R_C$

To Find I we must Write KCL at Node C_1

$I = I_{C_1} + I_{B_2}$

$-V_{C_1} + V_{BE} + (\beta+1) I_{B_2} R_{E_2} - 6 = 0$

$\therefore I_{B_2} = \frac{(V_{C_1}+6) - V_{BE}}{(\beta+1) R_{E_2}} = \frac{V_{C_1} + 5.3}{20.2K}$

$\frac{10 - V_{C_1}}{R_C} = 5.25 + \frac{V_{C_1} + 5.3}{20.2K}$ ——— (X)

For $R_C = 1K\Omega$

Solving eqn. (1) Gives: $V_{C_1} = 4.27V$

$I_{B_2} = 0.47\,mA$, $I = 5.724\,mA$.

$V_{CE_1} = 9.47 - 5.724 \times 1 = 3.746\,V$

$I_{C_2} = \beta I_{B_2} = 100 \times 0.47 = 47\,mA$.

$I_{E_2} = (\beta+1) I_{B_2} = 47.47\,mA$

$-10 + V_{CE_2} + I_{E_2} R_{E_2} - 6 = 0$

$\therefore V_{CE_2} = 16 - 47.47 \times 0.2K = 6.494V$

Since $I_{B_1} > 0$, $V_{CE_1} > V_{BE}$ and $I_{B_2} > 0$, $V_{CE_2} > V_{BE}$

$\therefore$ Both BJTs are F.A.M.

$P_{D_1} = I_{C_1} \cdot V_{CE_1} = 5.25 \times 3.746 = 19.66\,mW$

$P_{D_2} = I_{C_2} \cdot V_{CE_2} = 47 \times 6.494 = 302.68\,mW$

Cascode Multistage

The cct. shown is called Cascode in which two transistors are used ONE ON the top OF other. To perform the D.C analysis or design follow the following example.

EXA: Design the cct. shown in Fig. to have the following specifications: $V_{CE_1} = V_{CE_2} = 3V$ $I_{C_1} = I_{C_2} = 1mA$. the Current $I = 0.1mA$. Given BJTs with $V_{BE} = 0.7V$.

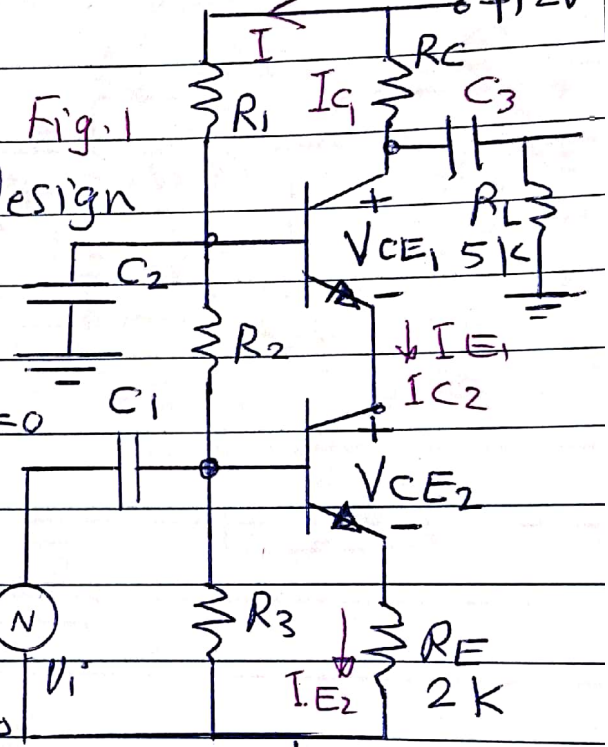


Fig. 1

Solution:

To performe D.C analysis or design "For this cct. Assume $\boxed{I_C = I_E}$

R_C? KVL For C-E loop:

$$-12 + I_C R_C + V_{CE_1} + V_{CE_2} + I_{C_2} R_E = 0$$

$$\therefore I_{C_1} R_C = 12 - 3 - 3 - 1 \times 2 = 4V$$

$$\therefore R_C = \frac{4V}{1mA} = \boxed{4K\Omega}$$

$$R_3 = \frac{V_{B_1}}{I}, \quad -V_{B_1} + V_{BE_1} + I_E R_E = 0$$

$$V_{B_1} = V_{BE_1} + I_C R_E = 0.7 + 1 \times 2 = 2.7V$$

$$\therefore R_3 = \frac{2.7V}{0.1mA} = \boxed{27K\Omega}$$

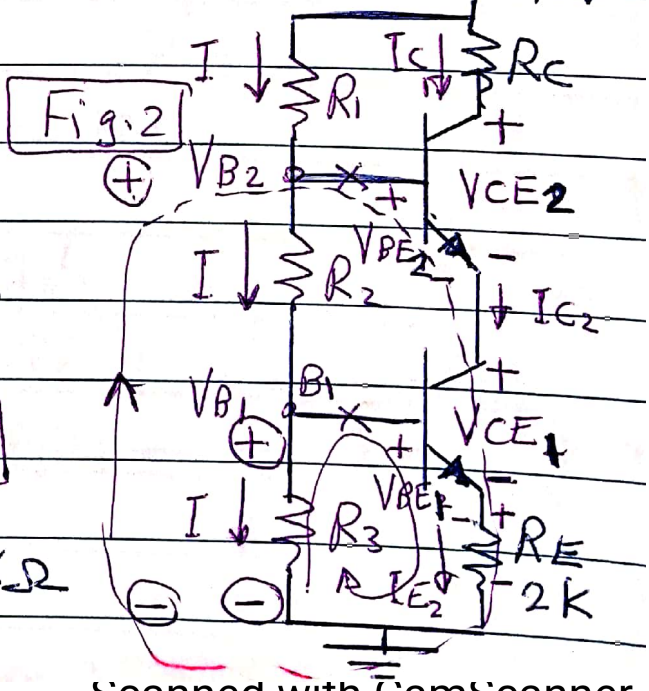


Fig. 2

$$R_2 = \frac{V_{B_2} - V_{B_1}}{I}$$

$$-V_{B_2} + V_{BE_2} + V_{CE_1} + I_E R_E = 0$$

$$\therefore V_{B_2} = 0.7 + 3 + 1 \times 2 = 5.7V$$

$$\therefore R_2 = \frac{(5.7 - 2.7)V}{0.1mA} = \boxed{30K\Omega}$$

$$R_1 = \frac{V_{CC} - V_{B_2}}{I} = \frac{12 - 5.7}{0.1mA} = 63K\Omega$$

To cheak the answer, you must cheak that:

$\frac{V_{cc}}{I} = R_T = R_1 + R_2 + R_3$

$\frac{12V}{0.1} = 63 + 30 + 27$

$120K = 120K$ ∴ Answer is Correct.

Other D.C ccts Analysis

EXA: Given $\alpha = 0.99$ Determine: V_E, $I_E, I_B, I_C, V_{EC}, V_E, V_C$

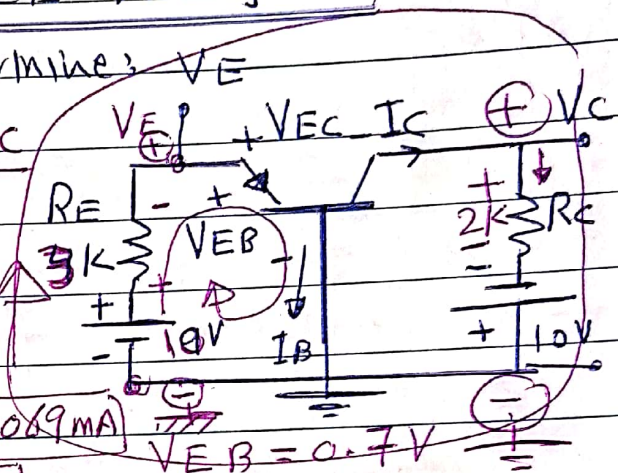


Fig 3

KVL For B-E loop:

$-10 + I_E R_E + V_{EB} = 0$

∴ $I_E = \frac{(10 - 0.7)V}{3K} = 3.1mA$

$I_C = \alpha I_E = 0.99 \times 3.1 = 3.069mA$

$\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = 99$

$I_B = \frac{I_E}{\beta+1} = \frac{3.1mA}{99+1} = 0.031mA$

KVL For C-E loop:

$-10 + I_E R_E + V_{EC} + I_C R_C - 10 = 0$

∴ $V_{EC} = 20 - 3.1 \times 3 - 3.069 \times 2 = 4.562V$

Since $V_{EC} > V_{EB}$ ∴ B-C Jn is Rev.

& $I_B > 0$ ∴ B-E Jn is F.W

∴ BJT in FAM.

$-V_E + V_{EB} = 0 \Rightarrow V_E = V_{EB} = 0.7V$

$-V_C + I_C R_C - 10 = 0 \Rightarrow V_C = I_C R_C - 10 = -3.862V$

∴ $V_{EC} = V_E - V_C = 0.7 - (-3.862) = 4.562V$

EXA:

For the cct. shown, the BJT has: $\beta = 100$, $V_{EB} = 0.6V$

① Calculate: I_E, I_B, I_C, V_C, V_E, V_{EC}, P_D ?

② Is the cct. bias-stable?

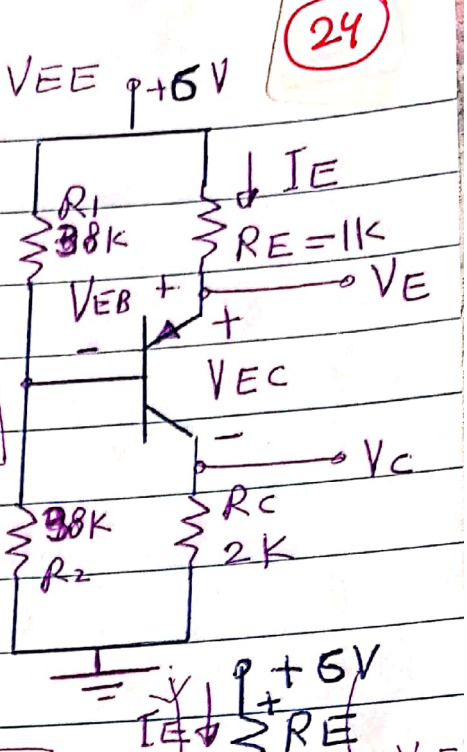


Fig.4

Solution:

$R_{th} = R_1 // R_2 = 38 // 38 = 19K\Omega$

$V_{th} = \frac{V_{EE} \cdot R_2}{R_1 + R_2} = \frac{6 \times 38}{(76)} = 3V$

KVL For E-B loop:

$-6 + I_E R_E + V_{EB} + I_B R_{th} + V_{th} = 0$

But $I_E = (\beta+1) I_B$

$\therefore I_B = \frac{6 - 3 - 0.6}{(\beta+1)R_E + R_{th}} = \frac{2.4V}{120K}$

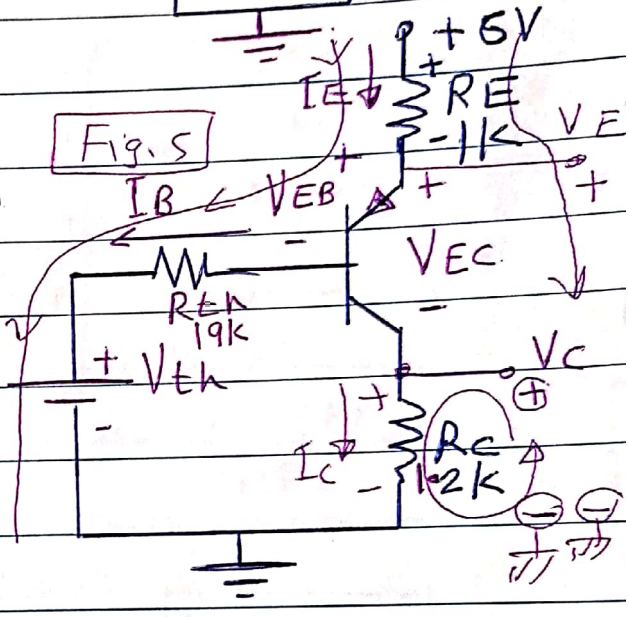


Fig.5

$\therefore I_B = 0.02mA$, $I_C = \beta I_B = 2mA$

$I_E = (\beta+1) I_B = 2.02mA$.

$V_E = 6 - I_E R_E = 6 - 2.02 \times 1 = 3.98V$

$V_C = I_C R_C = 2 \times 1.2 = 2.4V$

$V_{EC} = V_E - V_C = 3.98 - 2.4 = 1.58V$

Since $I_B > 0$, $V_{EC} > V_{EB}$ ∴ BJT in F.A.M.

② For a bias-stable condition. Cheak For " $R_{th} \leq 0.1(\beta+1)R_E$?

$38 // 38 \leq 0.1(101) \times 1$

$19K\Omega \overset{?}{\leq} 10.1K\Omega$

(L.H.S) (R.H.S)

Since $19K \not\leq 10.1K\Omega$ ∴ The cct. is NOT bias-stable.

$P_D = I_C \cdot V_{EC}$

$= 2 \times 1.58$

$= 3.16mW$

EXA: 5.17

$$V_{th} = \frac{(V^+ - V^-)}{R_1}\underbrace{R_2 R_1}_{R_{th}} + (V^-)$$

$$= \frac{(V^+ - V^-)\,R_{th}}{R_1} + (V^-)$$

$$\boxed{V_{th} = \frac{18\,R_{th}}{R_1} - 9} \quad \text{---(1)}$$

but $V_{th} = 9 - V_{EB} - I_E R_E - I_B R_{th}$

$$= 9 - 0.7 - 1 - \frac{0.5}{80} \times 16.2 = \boxed{7.2\,V}$$

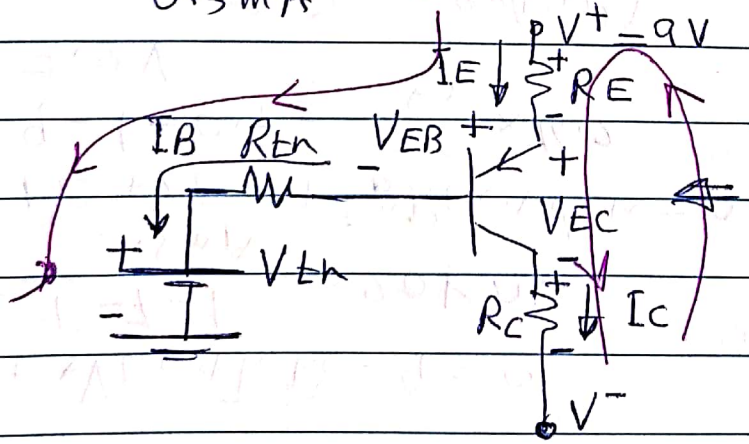
$$V_{th} + 9 = \frac{18\,R_{th}}{R_1}$$

$$\text{or } R_1 = \frac{18 \times 16.2}{16.2 + 9} = \boxed{18\,k\Omega}$$

$$\text{or } R_2 = \frac{R_1 \cdot R_{th}}{R_1 - R_{th}} = \frac{18 \times 16.2}{18 - 16.2} = \boxed{162\,k\Omega}$$

$$-9 + I_E R_E + V_{EC} + I_C R_C - 9 = 0$$

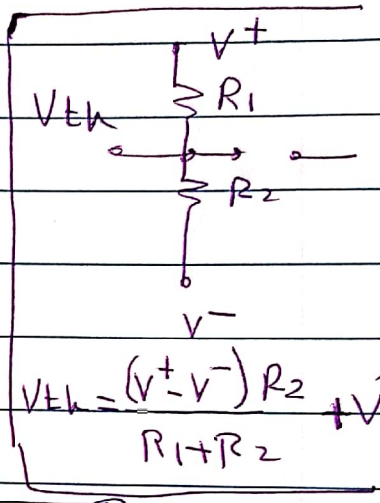
$$\therefore R_C = \frac{18 - 7 - 1}{0.5\,mA} = 20\,k\Omega$$

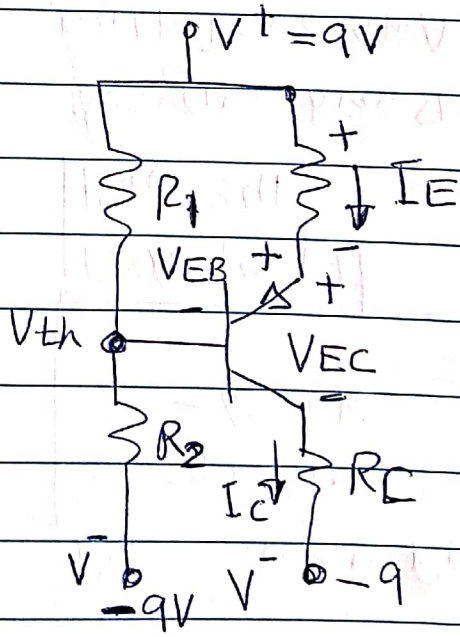


EXAMPLE (1)

$$R_E = \frac{V_{RE}}{I_E} \approx \frac{1V}{0.5^-} = \boxed{2k}$$

$$R_{th} = 0.1(81) \times 2 = \boxed{16.2\,k}$$





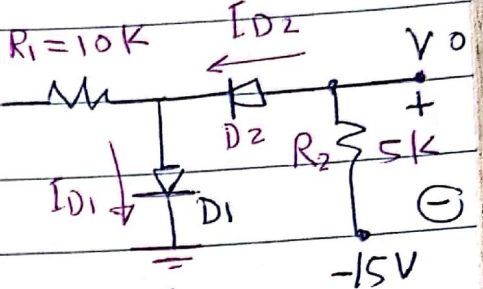
Design the cct: such that $I_{CQ} = 0.5\,mA$, $V_{RE} = 1V$, $V_{EC} = 7V$, Given $\beta = 80$, $V_{EB} = 0.7V$, (R_1, R_2, R_E, R_C)?

"Such that It is bias-Stable"

EXAMPLE

2.55 page 121

Given $V_\gamma = 0.7V$ For each diode +10V.
Determine $I_{D1}, I_{D2}, V_O, V_{D1}, V_{D2}$



Solution: Since D_1 has +10V on its anode and D_2 has −15V on anode side

So Assume $D_1 \rightarrow$ ON, $D_2 \rightarrow$ OFF

$$-10 + R_1 I + V_\gamma = 0$$

$$\text{or } I = I_{D1} = \frac{10 - V_\gamma}{10K} = 0.93\ mA$$

$I_{D2} = 0$ (Assumed OFF)

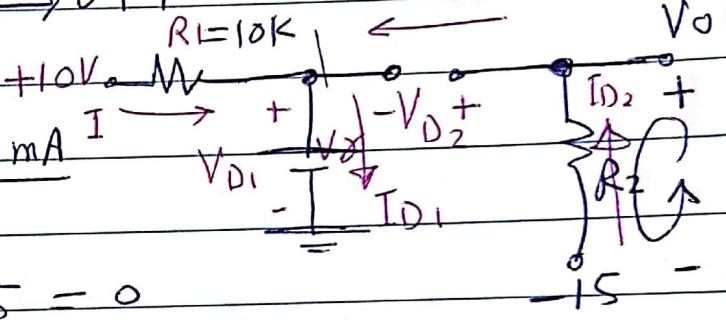
$$-10 + I R_1 - V_{D2} - I_{D2} R_2 - 15 = 0$$

$$V_{D2} = -25 + 0.93 \times 10 = -15.7V$$

Since $V_{D2} < 0$ so D_2 is indeed OFF, $I_{D2} = 0$

$$-V_O - I_{D2} R_2 - 15 = 0$$

$$\text{or } V_O = -15V$$



$I_{D2} = 0, V_{D2} = -15.7V$
$I_{D1} = 0.93\ mA$
$V_{D1} = 0.7V, V_O = -15V$

Field-Effect-Transistor "FET"

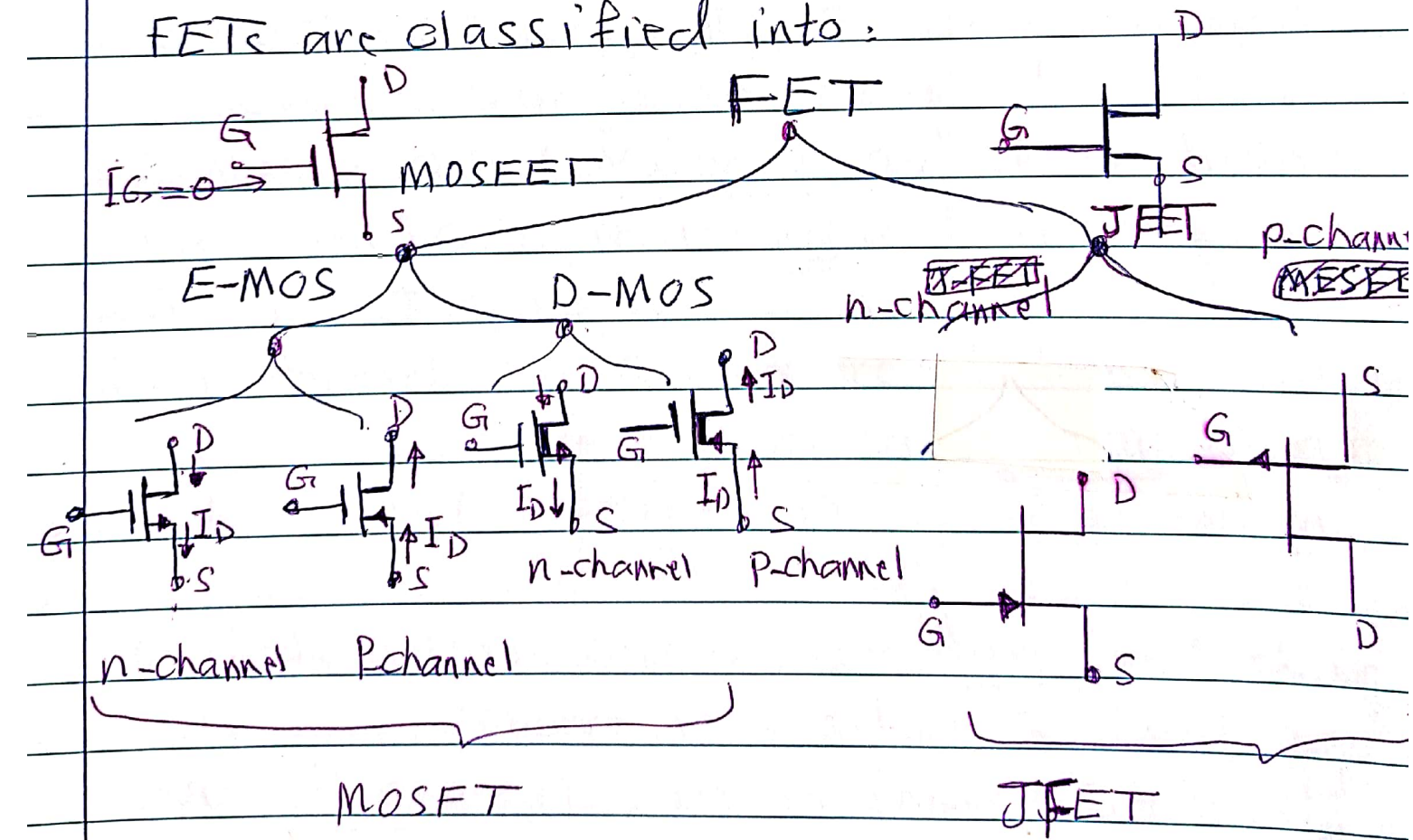
It is a three-terminal device, Gate, Drain and Source. the Current between Drain and Source is Controlled via an electric field applied perpendicular on drain-Source region created by applying a D.C voltage on the gate.

Compared to BJT:

FET is ① Unipolar device, only one type of carrier consisting Current. either
- electron (in n-channel devices)
- Holes (in p-channel devices)

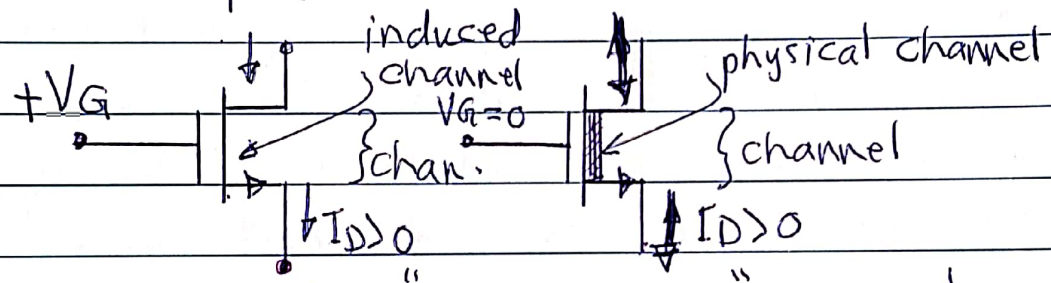
② $I_D = I_S$ and $I_G = 0$ in all types of FET ③ MOS is Small Size.

FETs are classified into:



MOSFET JFET

* The main difference between MOSFET and JFET is " In MOSFE the Gate is isolated from drain and Source by alayer of oxide. While in JFET all terminal are meeting in a Junction.
* The difference between D-MOS(deplesion MOS) and E-MOS(Enhancement MOS) is " In E-MOS the channel is enhancement channel (electronic) due to applying D.C voltage on gate) . i.e it has No physical existance. While in D-MOS, the channel is physical channel



* E-MOS: is called "normally OFF" device, because when VG=0, there is No channal, ID = 0
* D-MOS: is called "Normally ON" device because even when VG=0 it is ON and ID>0
* In all FET type:

① In n-channel: the carriers are electrons, and Since electron has Negative charge so it is called ~~N-MOS~~ N-channel, ID is, out of Source

② In P-channel: the carriers are Holes and their charge is positive, So they are called P-channel, ID is inward Source

MOSFET

Metal oxide Semiconductor Field-Effect Transistor

In this transistor the gate is isolated from drain and Source by a layer of oxide, their are two types: ① E-MOS ② D-MOS

⊛ N-channel Enhancement MOSFET

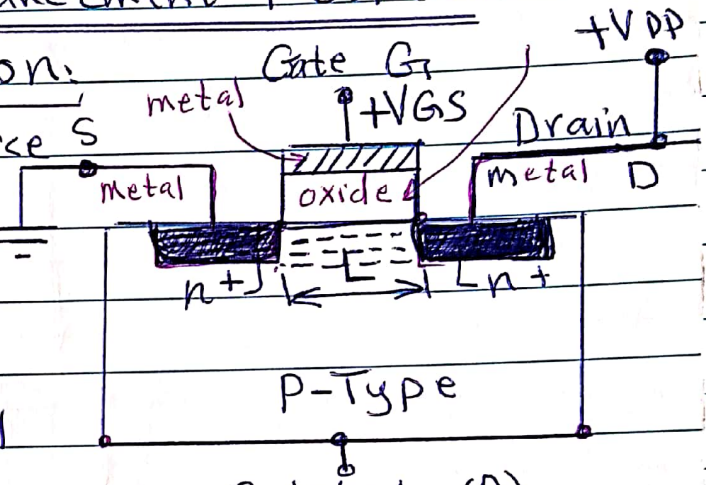
Structure and operation:

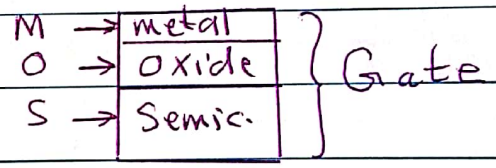
*The drain and Source are heavily dopped n+ (n-type).

*When a positive VGS is applied, it will Collect all electrons from far side and create electronic channel betwee S and D.

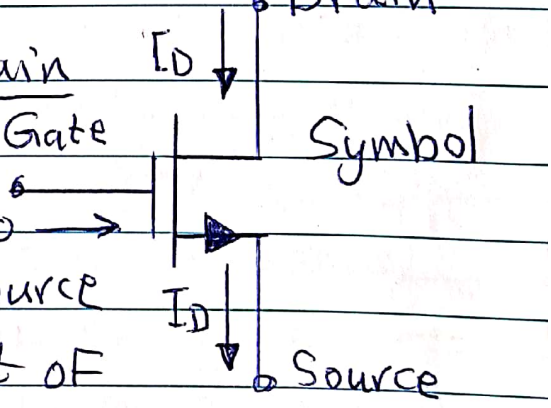
*When +VDD is applied on drain, this will attract electrons and force electrons to move from Source to drain

*The Conventional direction is from D → S, i.e ID with direction out of Source So the arrow direction is out of Source which is the Conventional direction of ID, IG is always Zero.





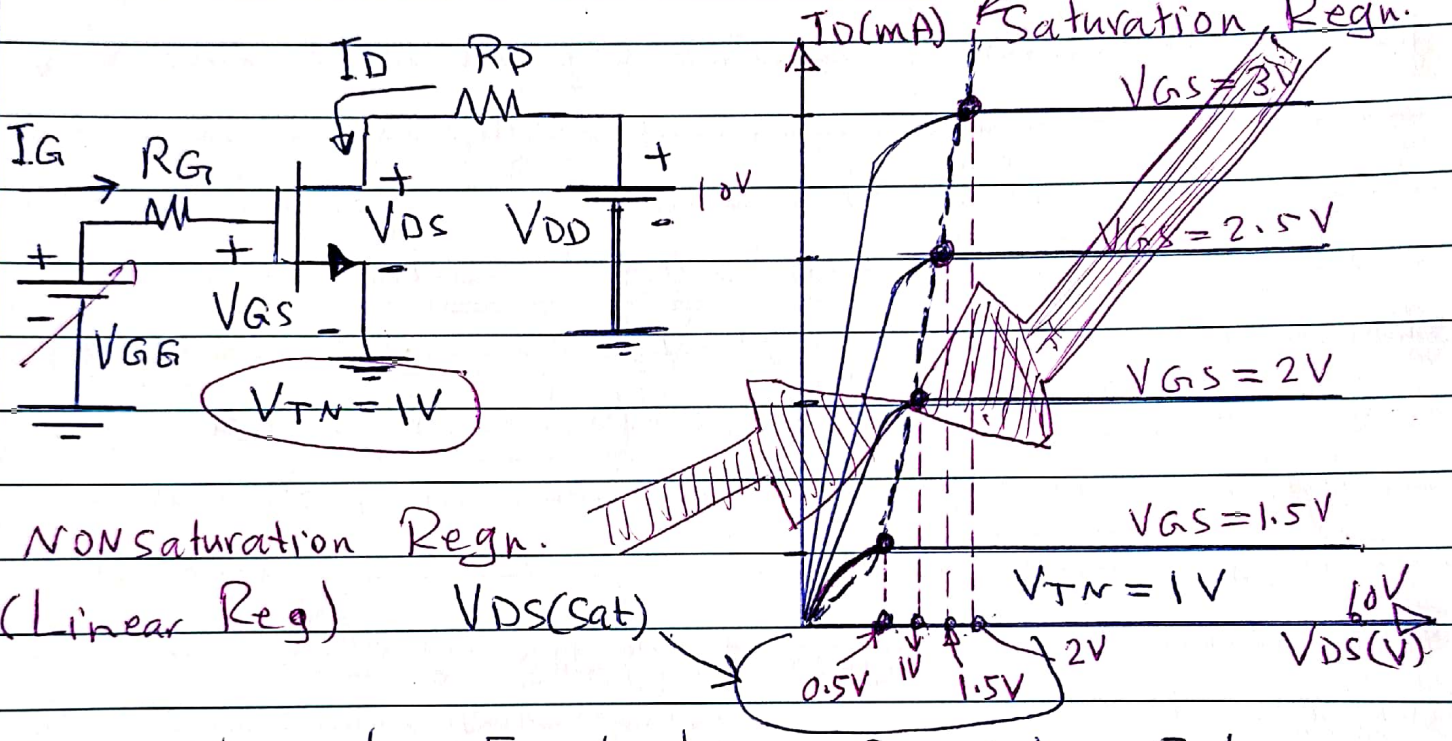
Gate Structure.



Symbol

Not any value of V_{GS} will create a channel, To create a channel, V_{GS} must **+ve** and Greator than a Certain Value V_{TN} which is called Threshold Voltage and is +ve also. and given in data sheet. So $V_{GS} > V_{TN}$.

MOSFET I-V characteristic [I_D Versus V_{DS}]



From the c/c, Each line, Consists of two regions:

$V_{DS(sat)} = V_{GS} - V_{TN}$

① Saturation Regn: In this region I_D is independan on V_{DS} & In this Regn. $V_{DS} > V_{DS(sat)}$ and I_D is given by: $I_D = K_n (V_{GS} - V_{TN})^2$ → (1)

where V_{TN}: Threshold Voltage (For n-channel) and given. (in data sheet)

K_n: conduction parameter (given) For n-channel in (mA/V^2), I_D: Drain Current (mA).

K_n is given by the following eqn.

$$K_n = \frac{W \mu_n C_{ox}}{2L} = \bar{K}_n \frac{W}{2L}$$ → process const.

Where W and L are Width & Length of channel

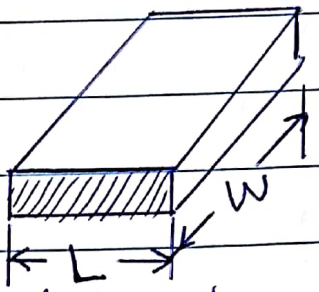
μ_n : electron mobility

C_{ox} : Gate-oxide-Capacitance

$\bar{K}_n$: process parameter.

$V_{DS(sat)} = V_{GS} - V_{TN}$.

* In this Regn. the MOSFET is used as an **Amplifier**



* From I_D eqn: It is cleare that $I_D \propto V_{DS}$.

(2) NONsaturation Regn (Linear Regn)

In this Regn, $V_{DS} < V_{DS(sat)}$ and I_D is given by

$$I_D = K_n [2(V_{GS} - V_{TN}) V_{DS} - V_{DS}^2] \quad \text{---(2)}$$

The MOSFET is used as a Voltage-Controlled resistance

$$R_{MOS} = \frac{1}{2K_n (V_{GS} - V_{TN})}$$

Since V_{TN} is constant

K_n = Constant

So $R_{MOS} \propto \frac{1}{V_{GS}}$.

this means:

MOSFET Can be used as a Voltage-Controlled Resistance.

* R_{MOS} is Controlled Via changing V_{GS}

this application is widely used in Communication electronics.

For Small V_{DS}

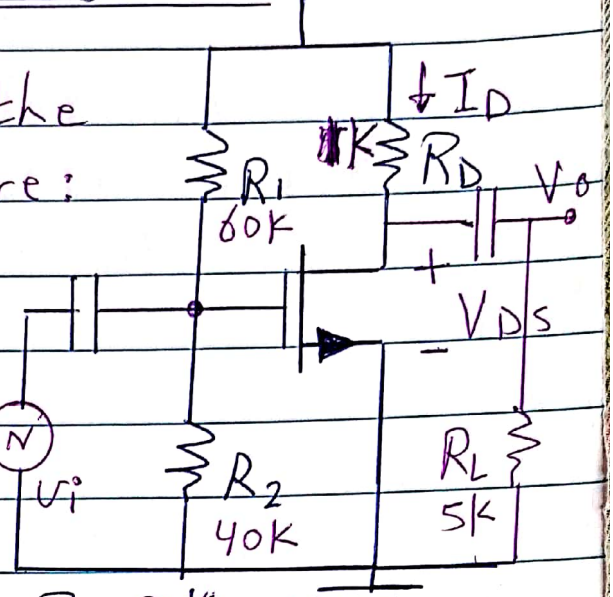
V_{DS}^2 term is negligible

So $I_D \approx 2K(V_{GS} - V_{TN}) V_D$

$\frac{I_D}{V_{DS}} = \frac{1}{R} = 2K_n (V_{GS} - V_{TN})$

So $R_{MOS} = \frac{1}{2K_n (V_{GS} - V_{TN})}$

MOSFET D.C ccts Analysis



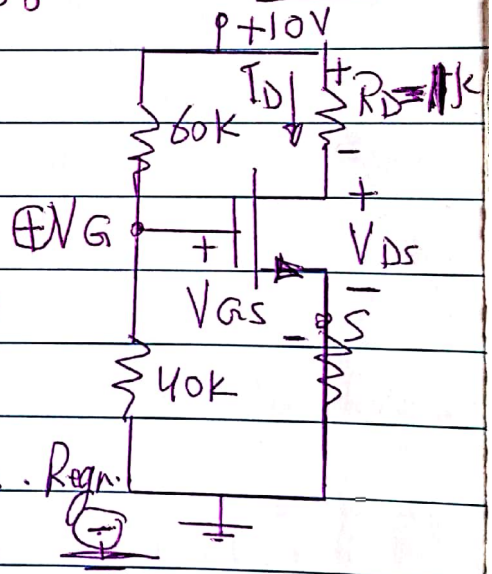
EXA1: For the cct. shown, the MOSFET parameters are:
$K_n = 1\ mA/V^2$, $V_{TN} = 2V$.

1) Calculate V_{GSQ}, I_{DQ}, V_{DSQ} and P_D.
2) Draw D.C.L.L eqn & lable Q-pt.
3) Recalculate V_{GSQ}, I_{DQ}, V_{DS} when $R_D = 2.2K$

For D.C analysi, all caps. are open-cct.
Assume the MOSFET in Saturation Regn. So:

$I_D = K_n(V_{GS} - V_{TN})^2$, K_n & V_{TN} → given

$$V_{GS} = V_G - V_S = \frac{10 \times R_2}{R_1 + R_2} - 0 = \frac{10 \times 40}{100} - 0 = 4V$$



then: $I_D = 1(4-2)^2 = 4\ mA$.

$-10 + I_D R_D + V_{DS} = 0$

$\therefore V_{DS} = 10 - 4 \times 1 = 6V$

$V_{DS(sat)} = V_{GS} - V_{TN} = 4 - 2 = 2V$

Since $V_{DS} > V_{DS(sat)}$

∴ MOSFET is in Saturation Regn.

$P_D = I_D \cdot V_{DS} = 4 \times 6 = 24\ mW$.

(2) D.C.L.L: KVL For D-S Loop:

$-10 + I_D R_D + V_{DS} = 0$ ① (D.C.L.L eqn).

$$\therefore I_D = \frac{10}{R_D} - \frac{V_{DS}}{R_D} \rightarrow y = b + mX \Rightarrow m = -\frac{1}{R_D}$$ Slope

or $V_{DS} = 10 - I_D R_D$ ② (D.C.L.L eqn) $\Rightarrow$ Slope $= -\frac{1}{R_D}$

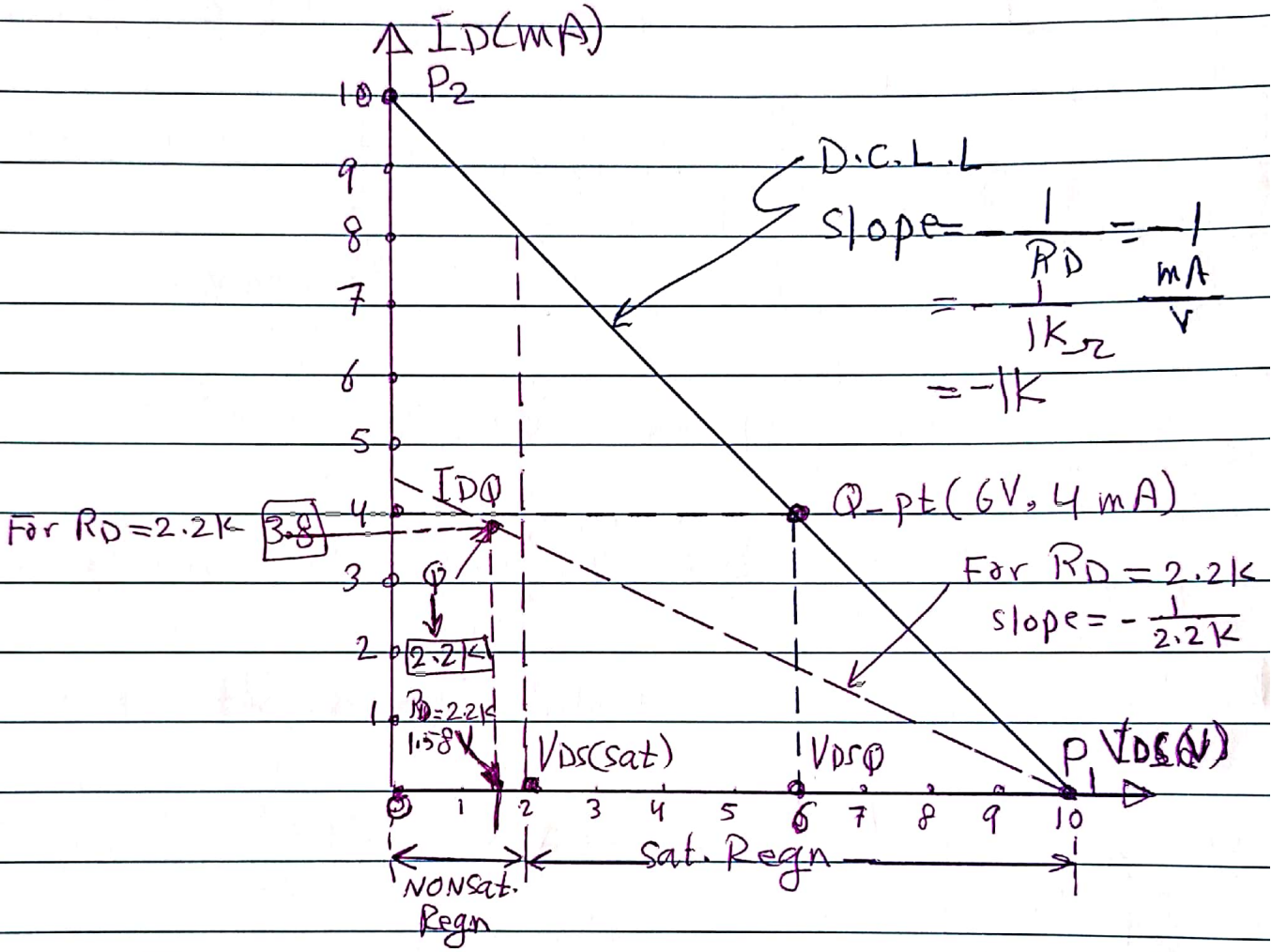
To draw D.C.L.L, use eqn ① or ②

from eqn. ② ($V_{DS} = 10 - I_D R_D$)

(i) For $I_D = 0$, $V_{DS} = 10V \Rightarrow P_1(10V, 0mA)$

(ii) For $V_{DS} = 0$, $I_D = \frac{10V}{1K} = 10mA$, $P_2(0V, 10mA)$.

~~&~~ Q-pt(V_{DSQ}, I_{DQ}) $\Rightarrow$ (6V, 4mA).



3) For $R_D = 2.2K\Omega$, Assume MOSFET in Sat. Regn.

$V_{GS} = V_G - V_S = 4V$

$I_D = 1(4-2)^2 = 4mA$, $\boxed{V_{DS}} = 10 - I_D \times R_D = 10 - 4 \times 2.2K = \boxed{12V}$

$\boxed{V_{DS(sat)}} = V_{GS} - V_{TN} = 4 - 2 = \boxed{2V}$

Since $V_{DS} < V_{DS(sat)}$ ∴ MOSFET is NONsat. Regn

So we must use: $I_D = K_n[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$

V_{GS} is $\boxed{NOT}$ changed. $V_{GS} = 4V$

So we shall write $I_D = \frac{10 - V_{DS}}{R_D} = K_n\left[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2\right]$

$\therefore \frac{10 - V_{DS}}{2.2} = 1\left[2(4-2)V_{DS} - V_{DS}^2\right]$

$10 - V_{DS} = 2.2\left[4V_{DS} - V_{DS}^2\right] = 8.8V_{DS} - 2.2V_{DS}^2$

$2.2V_{DS}^2 - 9.8V_{DS} + 10 = 0$

$\therefore V_{DS} = \frac{-(-9.8) \mp \sqrt{(-9.8)^2 - 4 \times 2.2 \times 10}}{2 \times 2.2}$

$= \frac{9.8 \mp \sqrt{96.04 - 8.8 \times 10}}{4.4}$

$= \frac{9.8 \mp 2.835}{4.4}$ $\therefore V_{DS} = 2.87V$ or $V_{DS} = 1.583V$ ✓

$y = Ax^2 + Bx + C$

$x = \frac{-B \mp \sqrt{B^2 - 4AC}}{2A}$

Since $V_{DS} = 1.583V < V_{DS(sat)}$

$\therefore$ It is the Correct Value. ✓

then:

$I_D = \frac{10 - 1.583}{2.2K} = 3.826\,mA$

or From $I_D = 1\left[2(4-2)1.583 - (1.583)^2\right] = 3.826\,mA$

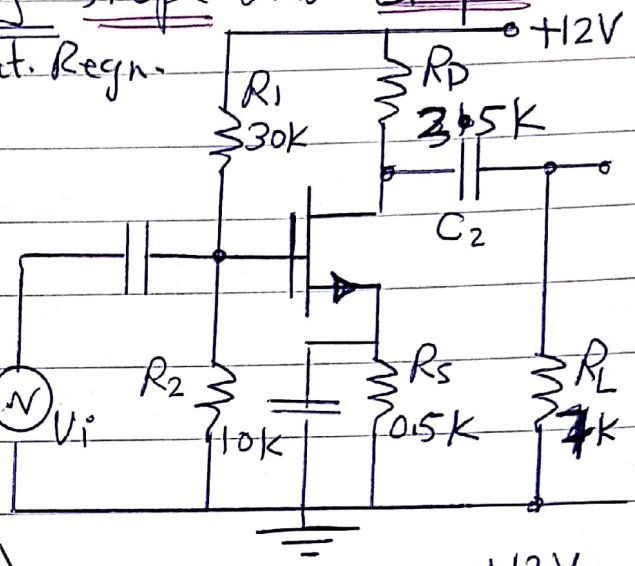
$\therefore$ the Q-pt $(1.583V, 3.826\,mA)$

$V_{DS} = 10 - 2.2I_D$

EXA 2: For the ckt. shown, the transistor paras. are: $K_n = 1\,mA/V^2$, $V_{TN} = 2V$, $\lambda = 0$.

1) Calculate V_{GSQ}, I_D, V_{DS}, V_D, and P_D.

2) Draw D.C.L.L indicating slope and Q-pt.



Assume the transistor in Sat. Regn.

$I_D = K_n(V_{GS} - V_{TN})^2$

$V_{GS} = V_G - V_S$, $V_S = I_D R_S$

$= \frac{12 \times 10}{10+30} - I_D R_S$

$V_{GS} = 3 - 0.5 I_D$

$\therefore I_D = \frac{3 - V_{GS}}{0.5} = 1(V_{GS} - 2)^2$

$3 - V_{GS} = 0.5(V_{GS}^2 - 4V_{GS} + 4)$

$0.5V_{GS}^2 - 2V_{GS} + 2 = 3 - V_{GS}$

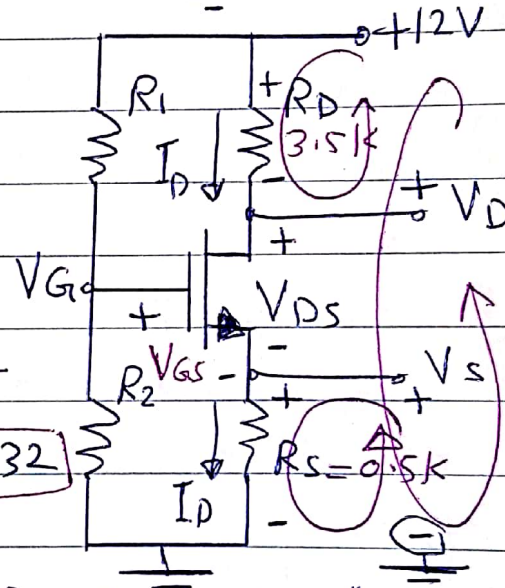
$0.5V_{GS}^2 - V_{GS} - 1 = 0$ — (X)

$\therefore V_{GS} = \frac{-(-1) \pm \sqrt{(-1)^2 - 4 \times 0.5(-1)}}{2 \times 0.5}$

$= \frac{1 \pm \sqrt{3}}{1} = \frac{1 \pm 1.732}{1}$

$\therefore$ either $V_{GS} = 2.732V$ or -0.732 (X)

(V_{GS} must be +ve and $> V_{TN}$).



$\therefore I_D = 0.536$ mA.

For D.C Analysis all Caps. are open-ckt.

$-12 + I_D R_D + V_{DS} + I_D R_S = 0$

$\therefore V_{DS} = 12 - 0.536(3.5 + 0.5) = 9.856V$

$V_{DS(sat)} = V_{GS} - V_{TN} = 0.732V$

Since $V_{DS} > V_{DS(sat)}$ $\therefore$ MOSFET in Sat. Regn.

$V_S = I_D R_S = 0.536 \times 0.5 = 0.268V$

$V_D = 12 - I_D R_D = 10.124V$, $P_D = I_D V_{DS} = 5.283$ mW

D.C.L.L: Write KVL For D-S Loop:

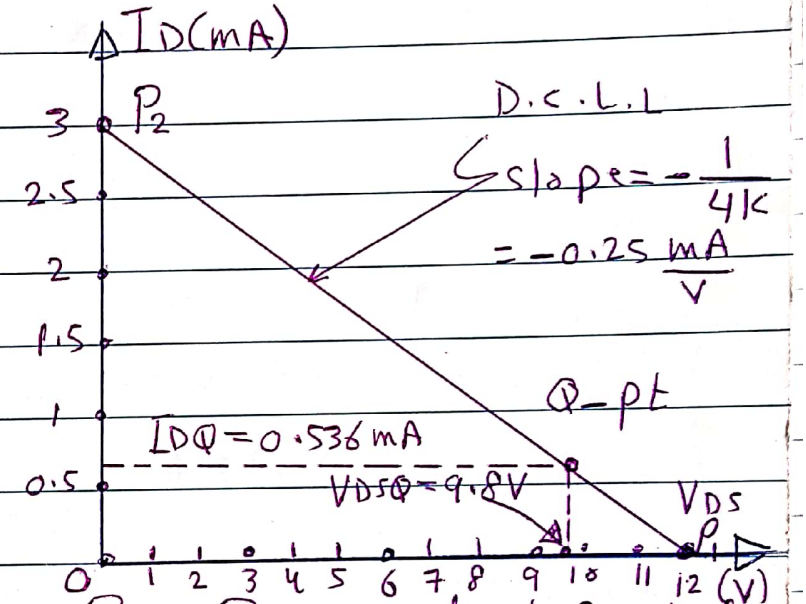
$-12 + I_D R_D + V_{DS} + I_D R_S = 0$

$\therefore \boxed{V_{DS} = 12 - I_D(R_D + R_S)}$ D.C.L.L eqn.

the slope is: $\boxed{-\frac{1}{R_D + R_S}}$

i) For $I_D = 0$, $V_{DS} = 12V \rightarrow P_1(12V, 0\,mA)$

ii) For $V_{DS} = 0$, $I_D = \frac{12V}{(3.5+0.5)} = 3\,mA$, $P_2(0, 3mA)$



3) Recalculate V_{DS} when R_L & R_D are direct Coupled.

V_{GS} & I_D will not affected:

$V_{GS} = 2.732V$, $I_D = 0.536\,mA$

$V_{DS} = 12 - IR_D - I_D R_S = V_D - V_S$

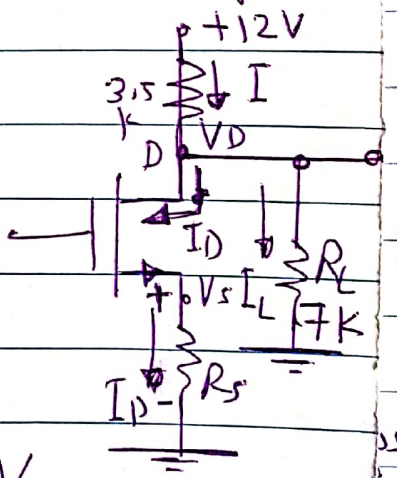
KCL at Node D: $\boxed{I = I_D + I_L}$

$\frac{12 - V_D}{3.5K} = 0.536 + \frac{V_D}{7K}$ (multiply by 7)

$24 - 2V_D = 3.752 + V_D \rightarrow V_D = 6.75V$

$\therefore V_{DS} = 6.75 - 0.536 \times 0.5 = 6.482V$

$V_{DS} = V_D - V_S = 6.75V - I_D \cdot R_S$



(Two D.C Sources)

$V_{TN} = 1 V$

EXA: Given a MOSFET with $K_n = 100 \mu A/V^2$, $\frac{W}{L} = 20$

Design the cct. to have $I_{DQ} = 1 mA$, $V_{DS} = 6V$

① Calculate (R_D, R_S, R_g). ??

$I_D = K_n (V_{GS} - V_{TN})^2$

$K_n = K_n' \frac{W}{2L} = 100 \frac{20}{2} = 1 mA/V^2$

$V_{GS} = V_{TN} \mp \sqrt{\frac{I_D}{K_n}} = 1 \mp \sqrt{1}$

$\therefore V_{GS}$ is either: $2V$ or $0V$ ✗

$V_{GS} = V_G - V_S \Rightarrow V_S = V_G - V_{GS}$

$\therefore V_S = I_G R_g - V_{GS} = 0 - V_{GS} = -2V$

$-V_S + I_D R_S - 5 = 0$

$I_D R_S = 5 + V_S = 5 - 2 = 3V$

$\therefore R_S = \frac{3V}{1mA} = 3 K\Omega$ ✓

$V_{DS} = V_D - V_S \Rightarrow V_D = V_{DS} + V_S = 6 - 2 = 4V$

$R_D = \frac{8 - V_D}{I_D} = \frac{8-4}{1mA} = 4 K\Omega$ ✓

R_g can be any value, because $I_G R_G = 0$

② Write D.C.L.L eqn and determine slope.

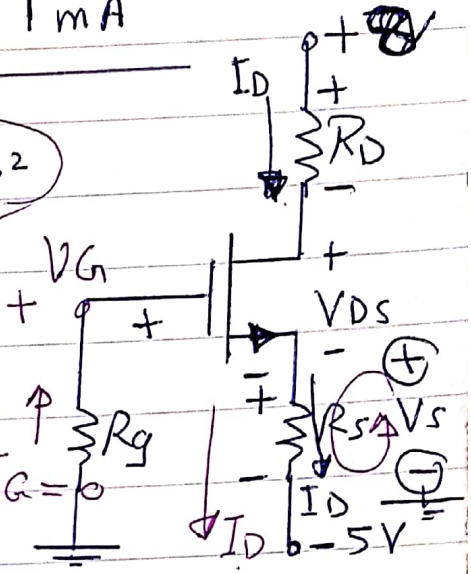
$-8 + I_D R_D + V_{DS} + I_D R_S - 5 = 0$

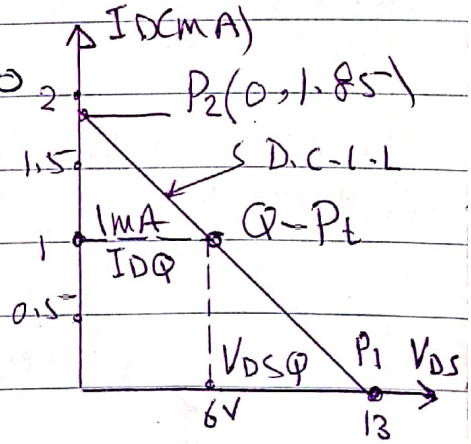
$V_{DS} = 13 - I_D (R_D + R_S)$ ⊗

$\therefore$ Slope $= -\frac{1}{R_D + R_S}$

for $I_D = 0$, $V_{DS} = 13V \Rightarrow P_1(13, 0)$

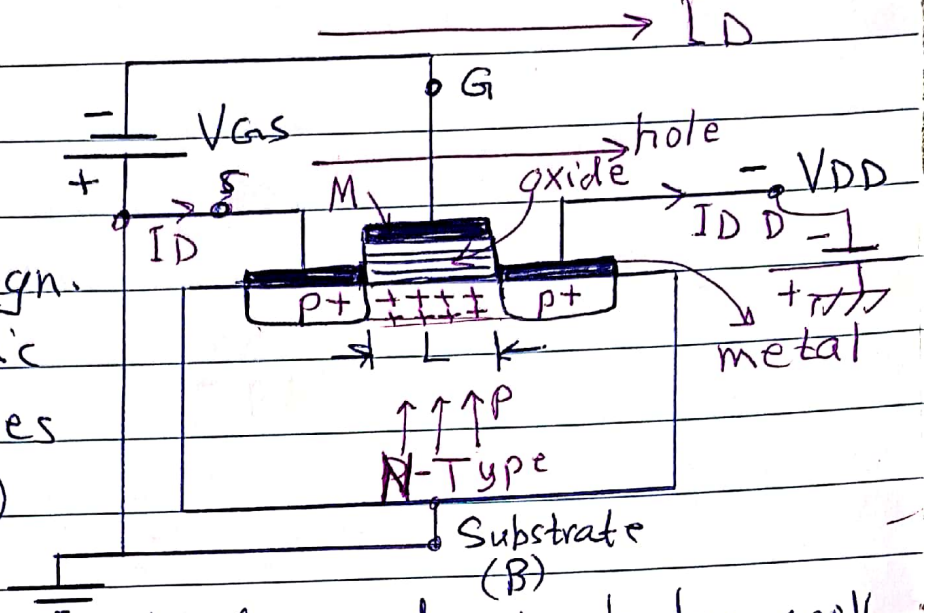
for $V_{DS} = 0$, $I_D = \frac{13}{7} = 1.85 mA$, $P_2(0, 1.85)$





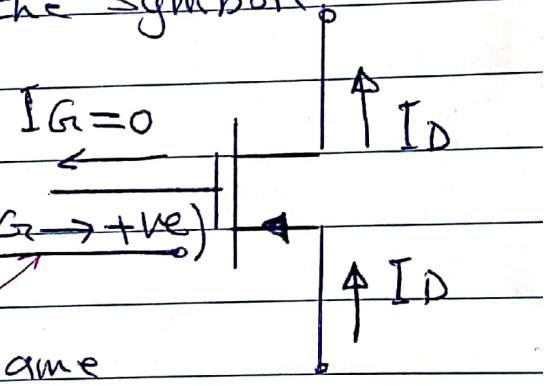
P-Channel MOSFET

Due to biasing (-ve V_{GS}), holes will be pulled under gate Regn. creating electronic channel with holes and since (D & S) are (p^+), so when -ve V_{DD} is applied on drain, holes will move from (Source to drain) causing a Current I_D directed conventionaly from Soure to drain i.e in ward Source, as in the Symbole.



* The Value of V_{GS} which Causes a channel must be negative ($V_{GS} \rightarrow$ -ve or $V_{SG} \rightarrow$ +ve)

$V_{GS} < V_{Tp}$ or $V_{SG} > V_{Tp}$



* The operation Regns. are the Same as for n-channel

P_MOS

1) Saturation Regn.: $(V_{SD} > V_{SD(sat)}) \rightarrow I_D = k_p (V_{SG} + V_{Tp})^2$

where $V_{SD(sat)} = V_{SG} + V_{Tp}$

2) Nonsaturation Regn.: $I_D = k_p [2(V_{SG} + V_{Tp}) V_{SD} - V_{SD}^2]$

where V_{Tp} is given and it is negative

$$k_p = \frac{\mu_p C_{ox} W}{2L} = k_p' \frac{W}{2L} \quad (mA/V^2)$$

k_p: conduction parameter.

Notice: Instead of $-V_{GS}$ we use V_{SG}

" " $-V_{DS}$ " " $+V_{SD}$

(i.e $V_{GS} = -2V$ means $V_{SG} = 2V$!!!) and

($V_{DS} = +5V$ means $V_{SD} = +5V$)

So we use positive values and reverse Subscript

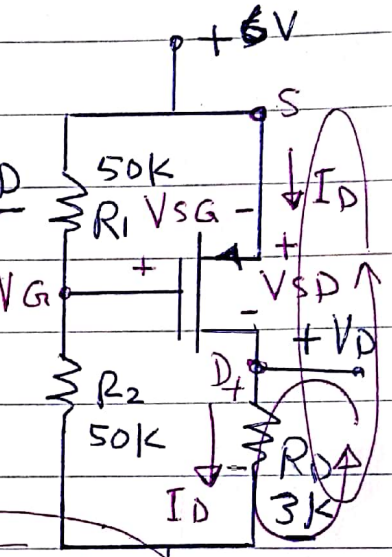
$-V_{DS} \rightarrow +V_{SD}$, $-V_{GS} \rightarrow +V_{SG}$

1 D.C Analysis

Ex: Given $k_p = 0.2 mA/V^2$

$V_{TP} = -1V$, Calculate V_{SG}, I_D, V_D, V_{SD}

Assume the MOSFET in Sat. Regn.



$I_D = k_p (V_{SG} + V_{TP})^2$ — (X)

$V_{SG} = V_S - V_G = 6 - \frac{6 \times 50}{100} = 3V$

$\therefore I_D = 0.2 (3 + (-1))^2 = 0.8 mA$

$-6 + V_{SD} + I_D R_D = 0$

$\therefore V_{SD} = 6 - 0.8 \times 3 = 3.6 V$

$V_D = I_D R_D = 0.8 \times 3 = 2.4 V$

$P_D = I_D \cdot V_{SD} = 0.8 \times 3.6 = 2.88 mW$

$V_{SD(sat)} = V_{SG} + V_{TP}$

$= 3 - 1 = 2V$

Since $V_{SD} > V_{SD(sat)}$ & MOSFET in Sat. Regn.

D.C.L.L & slope

$-6 + V_{SD} + I_D R_D = 0$

$\therefore V_{SD} = 6 - I_D R_D$ — (Y) D.C.L.L eqn.

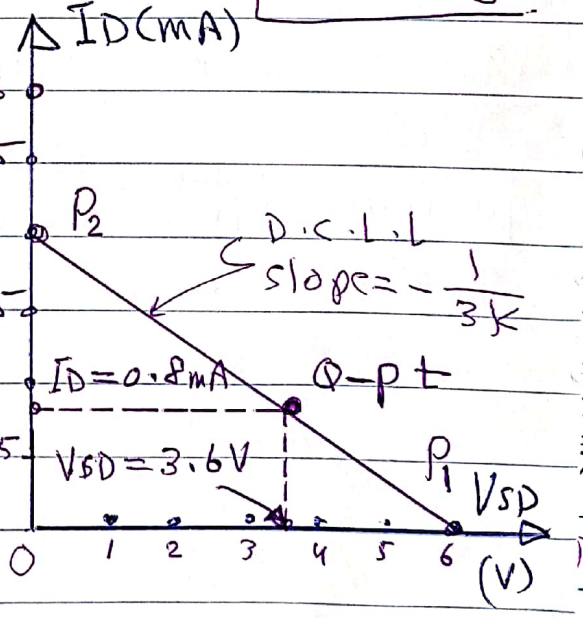
$\therefore$ Slope $= -\frac{1}{R_D}$

i) For $I_D = 0$, $V_{SD} = 6V$

$P_1 (6V, 0mA)$

ii) For $V_{SD} = 0$, $I_D = \frac{6}{3} = 2mA$

$P_2 (0, 2mA)$



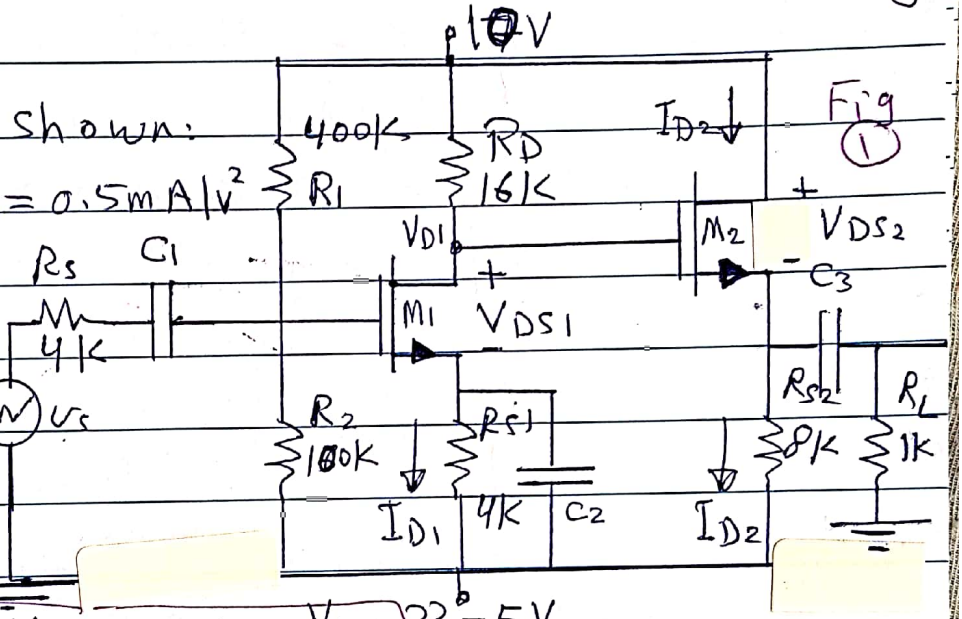
"Multitransistors Circuit"

Circuits Contain more than ONE transistor, at least two transistors, can be of the same type or complemantary (different types). They can be connected in two forms:

(1) Cascade Configuration

This is Series connection. as for the following circuit.

EXA: For the cct. shown:
M_1 parameters: $K_{n1} = 0.5 mA/V^2$
$V_{TN1} = 1V$ and
M_2 parameters:
$K_{n2} = 0.25 mA/V^2$
$V_{TN2} = 1V$.
Calculate:
$V_{GS1}, I_{D1}, V_{DS1}, V_{GS2}, I_{D2}, V_{DS2}$?? $-5V$



* For D.C Analysis, all Caps. → O.C
* Assume both MOSFETs in Sat. Regn.

$$I_{D1} = K_{n1}(V_{GS1} - V_{TN1})^2 \quad (1)$$

$$V_{GS1} = V_{G1} - V_{S1}$$

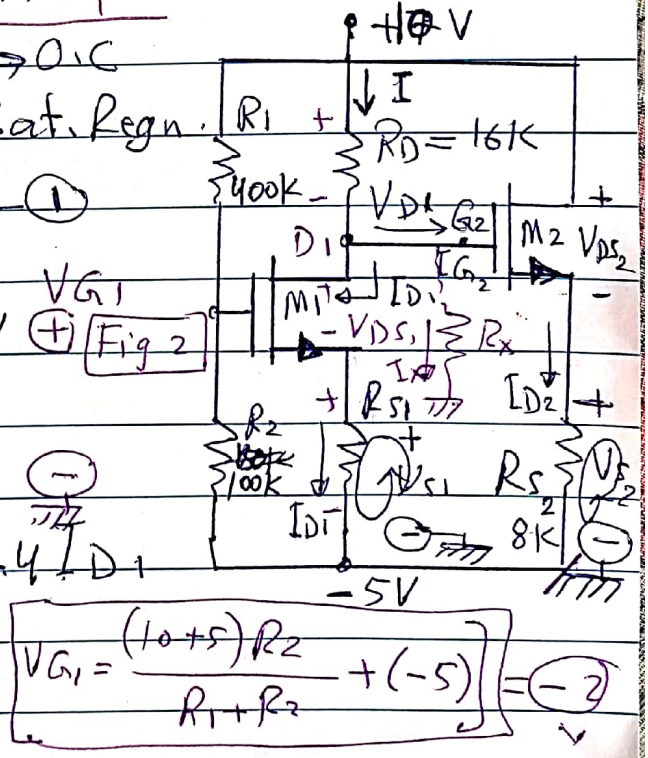
$$V_{G1} = \frac{10 \times 100}{400+100} + \frac{-5 \times 400}{500} = -2V$$

$$-V_{S1} + I_{D1}R_{S1} - 5 = 0$$

$$V_{S1} = 4I_{D1} - 5$$

$$\therefore V_{GS1} = -2 + 5 - 4I_{D1} = 3 - 4I_{D1}$$

$$\therefore \boxed{I_{D1} = \frac{3 - V_{GS1}}{4}} \quad (2)$$



V_{G1} ⊕ Fig 2

$$\boxed{V_{G1} = \frac{(10+5)R_2}{R_1+R_2} + (-5)} = -2V$$

$$\therefore \frac{3-V_{GS1}}{4} = 0.5\left(V_{GS1}^2 - 2V_{GS1} + 1\right)$$

$$3 - V_{GS1} = 2V_{GS1}^2 - 4V_{GS1} + 2$$

$$2V_{GS1}^2 - 3V_{GS1} - 1 = 1$$

$$\therefore V_{GS1} = \frac{-(-3) \mp \sqrt{(-3)^2 + 4\times2\times1}}{4} = \frac{3 \mp \sqrt{17}}{4} = +1.78V \checkmark$$

or $-0.28V$ ✗

$$\therefore I_{D1} = \frac{3-1.78}{4} = 0.305mA.$$

$$-10 + IR_D + V_{DS1} + I_{D1}R_{S1} - 5 = 0$$

$I = I_{D1} + I_{G2}^{\,0} \Rightarrow I = I_{D1} = 0.305mA$

$$V_{DS1} = 10 + 5 - I_{D1}(R_D + R_{S1}) = 15 - 0.305\times20 = 9.9V$$

$$V_{DS1(sat)} = V_{GS1} - V_{TN1} = 0.78V$$

Since $V_{DS1} > V_{DS1(sat)}$ $\therefore M_1$ is in Sat. Reg.

For M_2: Assume M_2 in Sat Reg.

$$I_{D2} = K_{n2}(V_{GS2} - V_{TN2})^2 \quad (3)$$

$V_{GS2} = V_{G2} - V_{S2}$ ~~$V_{GS2} = (5.12)V + 5 - 8I_D$~~

$V_{S2} - I_{D2}R_{S2} - 5 = 8I_{D2} - 5$

$\therefore$ ~~$V_{G2} = V_{D1}$~~ $= 10 - I_{D1}R_D = 10 - 0.305\times16 = 5.12V$

$\therefore V_{GS2} = 5.12 + 5 - 8I_{D2} = 10.12 - 8I_{D2}$

$$I_{D2} = \frac{10.12 - V_{GS2}}{8} \quad (4)$$

$$\frac{10.12 - V_{GS2}}{8} = 0.25\left(V_{GS2}^2 - 2V_{GS2} + 1\right)$$

$$10.12 - V_{GS2} = 2V_{GS2}^2 - 4V_{GS2} + 2$$

$$2V_{GS2}^2 - 3V_{GS2} - 8.12 = 0 \quad (5)$$

$$\therefore V_{GS2} = \frac{-(-3) \mp \sqrt{(-3)^2 + 4\times2\times8.12}}{2\times2} = \frac{9 \mp \sqrt{73.96}}{4}$$

$V_{GS2} = 4.4V$ ✓ or $-0.1V$ ✗

$$\therefore I_{D2} = \frac{10.12 - 4.4}{8} = 0.715mA$$

$$V_{DS2} = 15 - I_{D2}R_{S2} = 9.28V$$

$V_{DS2(sat)} = V_{GS2} - V_{TN}$

$= 3.4V$

$\therefore M_2$ in Sat. Reg.

(2) Cascode Configuration.

This cct. contains Common Source Amp and Common gate Amp. It is used For high frequency response.

EXA: Given M_1 & M_2 are identical with $K_{n_1} = K_{n_2} = 1\ mA/V^2$

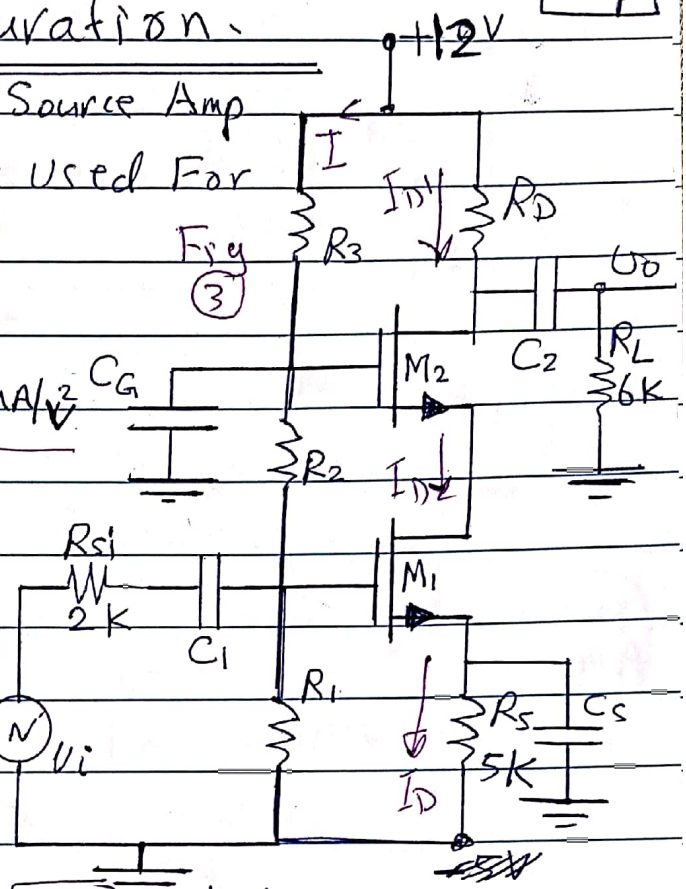
$V_{TN_1} = V_{TN_2} = 1V$.

Design the cct. to have:

$I_{DQ} = 1\ mA, V_{DS_1} = 3V$

$V_{DS_2} = 2V$. Let $R_1 + R_2 + R_3 = 120K$

* For D.c Analysis, all Caps. are open cct.



* For $R_T = 120K\Omega$, $I = \frac{12V}{120K} = 0.1\ mA$

$R_1 = \frac{V_{G1}}{I}$, $R_2 = \frac{V_{G2} - V_{G1}}{I}$, $R_3 = \frac{12 - V_{G2}}{I}$

$-V_{G1} + V_{GS_1} + I_D R_S = 0$

$V_{GS_1} = V_{G1} - V_{S1} \Rightarrow V_{G1} = V_{GS_1} + V_{S1}$

$V_{G1} = V_{S1} + V_{GS1}$

$V_{S1} = I_D \times R_S = 1 \times 5 = 5V$

$V_{GS_1} = V_{TN} \mp \sqrt{\frac{I_D}{K_n}} = 1 \mp \sqrt{\frac{1}{1}} = 2V$

$\therefore V_{G1} = 2 + 5 = 7V$

$\therefore R_1 = \frac{7V}{0.1mA} = 70K\Omega$

$-V_{G2} + V_{GS2} + V_{DS1} + I_D R_S = 0$

$V_{G2} = 2 + 3 + 1 \times 5 = 10V$

$\therefore R_2 = \frac{(10-7)V}{0.1mA} = 30K\Omega$

$R_3 = \frac{(12-10)V}{0.1mA} = 20K\Omega$

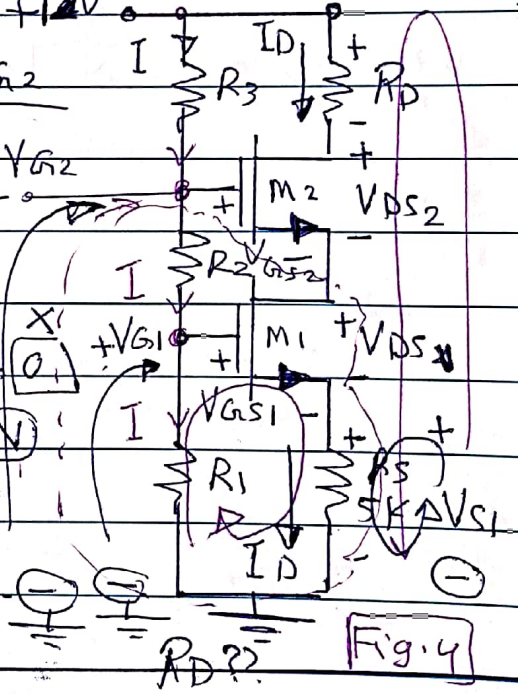


Fig. 4

$-12 + I_D R_D + V_{DS2} + V_{DS1} + I_D R_S = 0$

$\therefore R_D = \frac{12 - 2 - 3 - 5 \times 1}{1mA}$

$R_D = \frac{2}{1} = 2K\Omega$

① $K_n = \bar{K_n} \frac{W}{2L}$

EXA: For the cct. shown, the MOSFET has $\bar{K_n} = 100\mu A/V^2$, $V_{TN} = 1V$, $V_{DS} = 3V$

1) Calculate $(\frac{W}{L})$ of the transistor
2) Calculate I_D, V_S, P_D

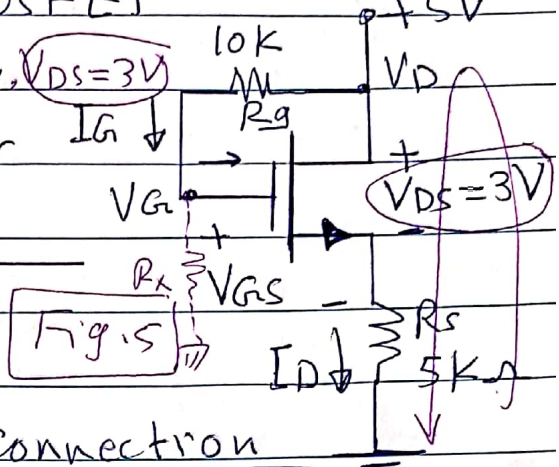


Fig. 5

Assume the MOSFET in Sat.

$I_D = K_n(V_{GS} - V_{TN})^2$

For this Connection (D-G) Connection

$V_D = V_G$ because $I_G = 0$ $\therefore$ $\boxed{V_{DS} = V_{GS} = 3V}$

$-5 + V_{DS} + I_D R_S = 0 \Rightarrow (I_D) = \frac{5 - V_{DS}}{R_S} = \frac{5-3}{5} = (0.4\ mA)$

$0.4 = K_n^{?}(3-1)^2 = 4K_n$

$\therefore K_n = \frac{0.4}{4} = 0.1\ mA/V^2$ $\quad \bar{K_n} = 100\mu A/V^2 = 0.1\ mA/V^2$

$K_n = \bar{K_n} \frac{W}{2L} \Rightarrow \frac{W}{L} = \frac{2K_n}{\bar{K_n}} = \frac{2 \times 0.1}{0.1} = 2$

$\boxed{V_S} = I_D R_S = 0.4 \times 5 = \boxed{2V}$

$P_D = I_D V_{DS} = 0.4 \times 3 = 1.2\ mW$

② **EXA:** $K_n = 0.2 mA/V^2$, Given: $V_{TN} = 1V$

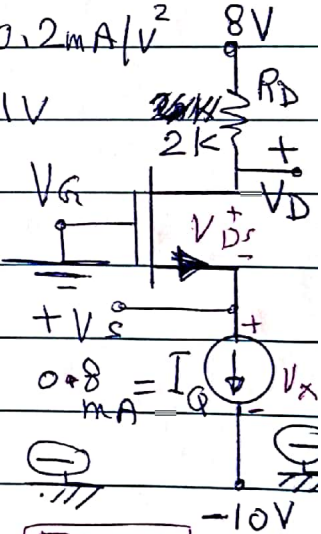


Fig. 6

Calculate V_S, V_D, V_{DS}, P_D.

$I_D = K_n(V_{GS} - V_{TN})^2$ $\quad (I_D = I_Q)$

$\therefore \boxed{V_{GS}} = V_{TN} \mp \sqrt{\frac{I_D}{K_n}} = 1 \mp \sqrt{\frac{0.8}{0.2}} = \boxed{3V}$ or $\boxed{-1V}$ (×)

$V_{GS} = V_G - V_S$ $\rightarrow$ but $V_G = 0$

$\therefore (V_S) = -V_{GS} = \boxed{-3V}$ $\quad [-8 + I_D R_D + V_D = 0]$

$(V_D) = 8 - I_D R_D = 8 - 0.8 \times 2 = (6.4V)$

$(V_{DS}) = V_D - V_S = 6.4 - (-3) = (9.4V)$

$V_{DS(sat)} = V_{GS} - V_{TN} = 3 - 1 = (2V)$

$\therefore$ MOSFET in Sat. Regn.

$P_D = I_D V_{DS} = 0.8 \times 9.4 = 7.52\ mW$