ElCoM
ELECTRICAL COMPUTER MECHATRONICS

تقدم لجنة ElCoM الاكاديمية

دفتر لمادة:

الكترونيات (١)

من شرح:

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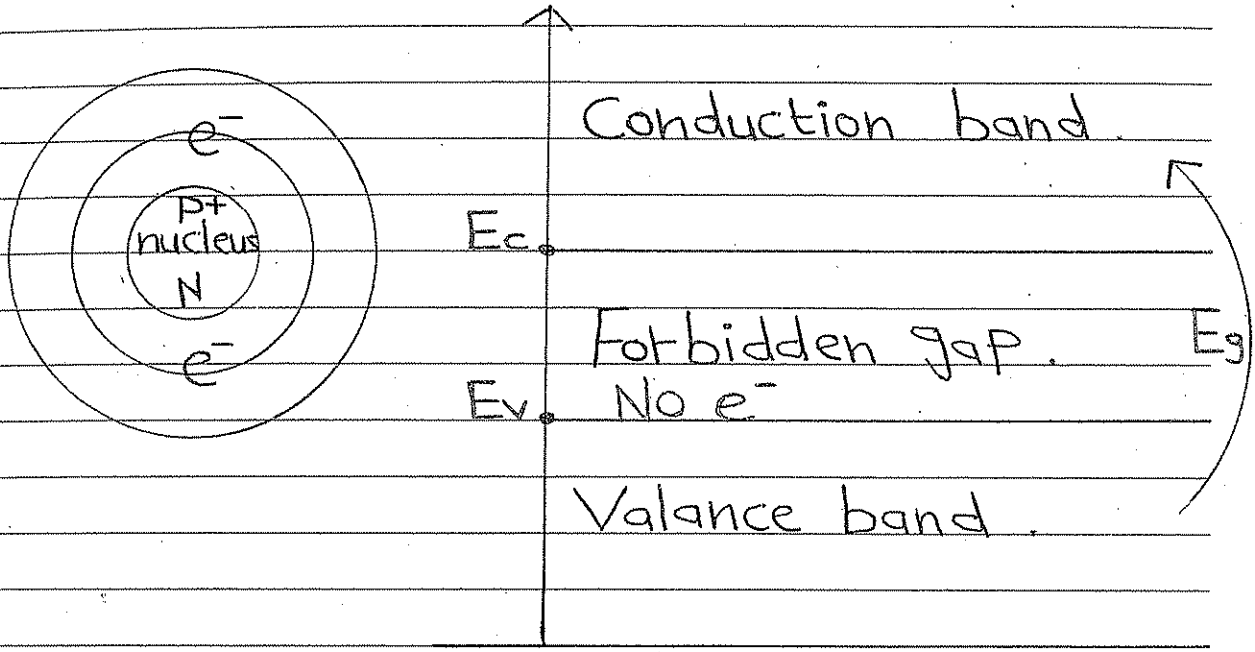
جزيل الشكر للطالب:

عدنان حوراني

Chapter (1):

Semiconductor Materials and Diodes:



Energy level Diagram.

Ev : Max. energy of V.B.

Ec : Minimum energy of C.B.

Eg (Band gap Energy) : Minimum energy required by e^- to move from V.B to C.B.

* Eg depends on material.

$$\boxed{E_c = E_v + E_g}$$

Material Types :

*1) Conductors : الموصلات

- Contain very large number of e^- in C.B.
- Have very large Conductivity $\sigma (\Omega.cm)^{-1}$ and very small resistivity ρ ($\rho_{Cu} = 10^{-6} \Omega.cm$) متدانية ، Copper.
- C.B and V.B are overlapped ($E_g = 0$).

*2) Insulators : العوازل

- No Free e^- in C.B (All in V.B).
- Very high resistivity ρ ($\rho_{mica} = 10^{12} \Omega.cm$). and Very Low Conductivity.
- (E_g) is between [3-6] e.V.

*3) Semiconductors : أشباه الموصلات

1) Materials from group (4) in periodical table. (have ($4e^-$) in external Orbit).

2) Eg is around 1 ev.

1.1 ev for Si } elemental Semiconductor.
0.66 ev for Ge }

1.4 ev for GaAs → compound Semiconductor.

(3) ثلاثي (5) خماسي

↳ used for optical devices fabrication.

3) (σ) and (ρ) level are in between Conductor and Insulator.

$\rho_{Si} = 5 \times 10^4 \ \Omega \cdot cm$.

$\rho_{Ge} = 50 \ \Omega \cdot cm$.

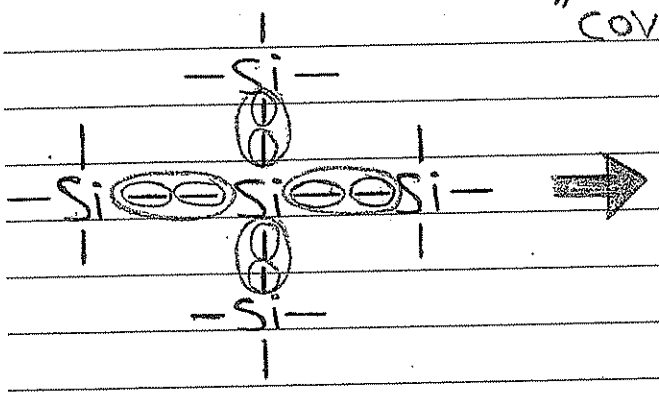
4) The electrical Characteristics for Semiconductor can be greatly Charged by Doping.

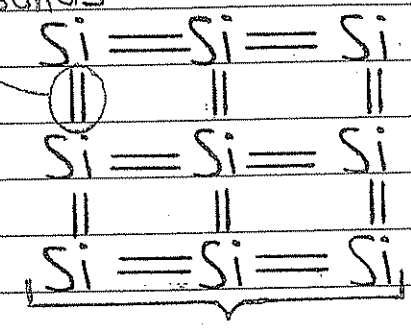
* Doping: Adding Atoms from group (3) or (5) to the pure Semiconductor.

* Intrinsic Semiconductors : (pure Semic):

Example : Silicon.

روابط تساهمية
"covalent bonds"





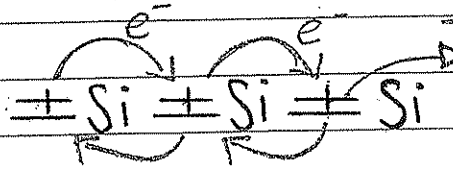
(Si) Crystal

1) At ($T = 0\,k$) : all e^- in V.B and So Silicon is considerd as an Insulator.

2) At ($T > 0\,k$) : Some e^- gain enough energy and break the bond leaving a (+ve) Charge called Hole.

* e^- and Hole are called Carriers.

مسؤولة عن حمل التيار



3) At a Certain temp. :-

* $\boxed{\text{No. of } e^- = \text{No. of Hole} = n_i}$

Where: n_i : Intrinsic Carrier Concentration ($\#/cm^3$).

* n_i can be calculated using :

$$\boxed{n_i = B \cdot T^{3/2} \cdot e^{\frac{-E_g}{2kT}}} \quad (\#/cm^3)$$

B : Constant related to material.

For Si : $B = 5.23 \times 10^{15}$ $(k^{-3/2} \cdot cm)$.

T : Temp. (k).

E_g : Band gab Energy. (eV).

k : Boltzmann's Constant.

$(k = 86 \times 10^{-6}$ ev/k)

EXA :- Calculate (e^-) and (h^+) consentration on Silicon at T = 300 k (room temp.), Given :

$B_{si} = 5.23 \times 10^{15}$; $E_{g_{si}} = 1.1\,ev$; $k = 86 \times 10^{-6}\,ev/k$.

Sol :- $e^- = h^+ = n_i$

$$= (5.23 \times 10^{15}) \cdot (300)^{\frac{3}{2}} \cdot e^{\frac{-1.1\,ev}{2 \times 86 \times 10^{-6} \times 300}}$$

$$= 1.5 \times 10^{10}/cm^3.$$

→ This no. is Small compared to no. of (Si) atom is Cm^3, Which is $5 * 10^{22}$ Atom/cm^3.

* To increase No. of cartier, we have to use Doping.

At (T = 300 k) ; :-

$n_{i_{Si}} = 1.5 * 10^{10}\ Cm^{-3}$.

$n_{i_{Ge}} = 2.4 * 10^{13}\ Cm^{-3}$.

$n_{i_{GaAs}} = 1.8 * 10^{6}\ Cm^{-3}$.

*Extrinsic Semiconductors :

***Extrinsic Semic. = Intrinsic Semic. + impurities.**

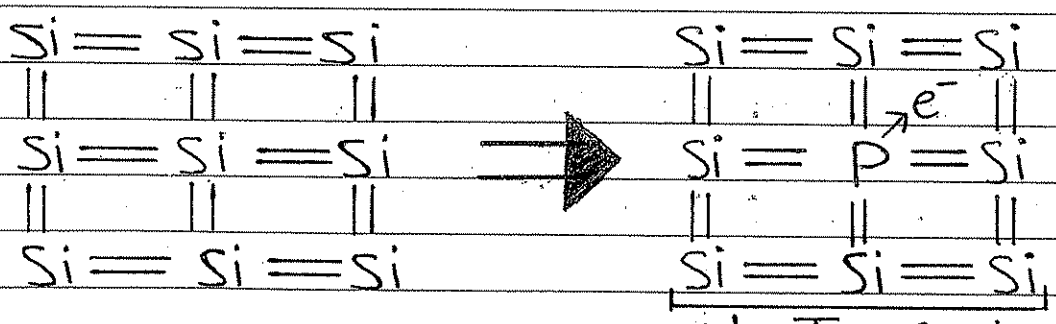
Impurities : Atoms from group (3) and group (5) Added to pure semic. by Doping process to increase No. of carriers.

*Extrinsic Semic. :-

- N-Type semic.
- P-Type semic.

I] N-Type semic. :-

1) :: Intrinsic Semic. + Atoms from group (5) Such as : Phosphour (P)



N - Type Semic.

From negative charge of (e^-)

*من الشحنات الأغلبية

2) It contain an excess of (e^-).

3) It is electrically nuetral.

4) The "pentavalent Atom" (Phosphour) is called Donar Atom.

5) The Concentration of Donar Atom is N_D ⇒ Doping Level.

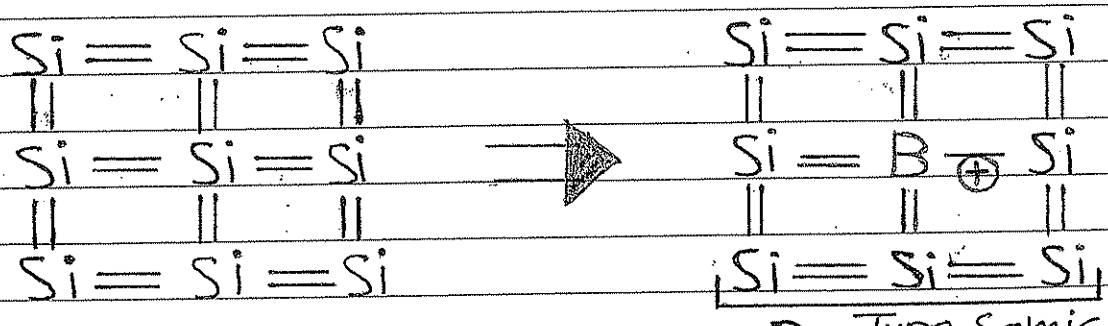
6) The Majority carriers → e^-.

The Minority carriers → h^+.

2] P-Type Semic :

1) :: Intrinsic Semic. + Atoms from group (3)

Such as: Botown (B).



P-Type Semic.

From positive charge of (h^+)

× من الناقلات الغالبية ؛

2) It contains an excess of (holes).

3) It is electrically huetral.

4) The "Trivalent Atoms" (Borown) are called Aceptor Atom.

5) The Concentration of Trivalent Atom is N_A.

6) The Majority Carriers $\rightarrow h^+$.

The Minority Carriers $\rightarrow e^-$.

* Calculation of (e^-) and (h^+) Concentration in (N-Type) and (P-Type) :-

- At the room temp. :

(No. of e^- = No. of h^+ = n_i = n_o = P_o)

Where:

n_o : e^- concentration at Thermal Equilibrum

P_o : h^+ concentration at Thermal Equilibrum

n_i : The intrinsic carrier concentration.

$$n_o \cdot P_o = n_i^2$$

* For N-Type : When ($N_D \gg n_i$) ; So e^- No. or e^- concentration $\backsim N_D$ ($e^- \rightarrow$ Majority)

→ The hole Concentration is : ($h^+ \rightarrow$ Minority)

$$\left(P_o = \frac{n_i^2}{N_D} \right)$$

* For P-Type : When ($N_A \gg n_i$) ; So h^+ No. or h^+ Concentration $\simeq N_A$ ($h^+ \rightarrow$ Majority)

→ The e^- Concentration is :- ($e^- \rightarrow$ Minority)

$$\left(n_o = \frac{n_i^2}{N_A} \right)$$

EXA. :- A (Si) is doped with phosphoure at a rate of ($10^{16}\ cm^{-3}$) at room temp. :

- Identify the type of resulted material.
- Calculate maj. and min. concentration?

Sol.

- N-Type semic.
- Majority → e^- conc. $= N_D = 10^{16}\ cm^{-3}$.
- Minority → h^+ conc. $= \frac{n_i^2}{N_D} = \frac{(1.5 \times 10^{10})^2}{10^{16}}$

$= 2.25 \times 10^{4}\ cm^{-3}$.

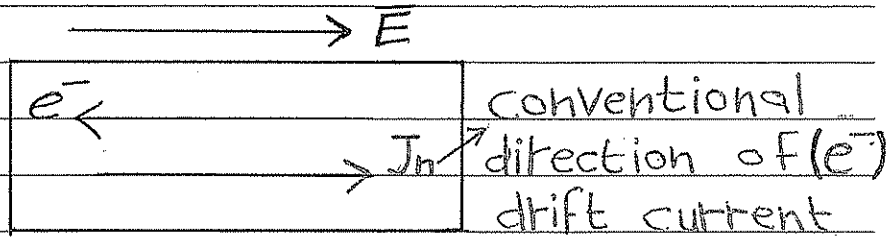
* Currents in Semiconductor :-

→ (Movement of Carriers).

1) Drift Current density : ($J \rightarrow A/cm^2$)

Movement of Carriers due to Applying electric field.

ⓘ For e^- (N-Type) :



(N-Type)

$$J_n = e \cdot n \cdot \mu_n \cdot \bar{E} \quad (A/cm^2)$$

J_n : e^- drift current.

e : e^- charge. (C)

n : e^- Concentration ($\#/cm^3$)

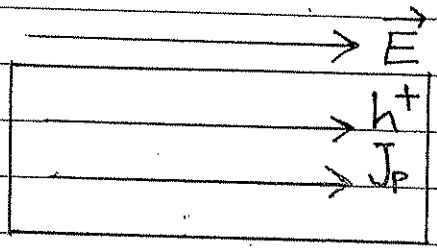
μ_n : e^- mobility = 1350 $cm^2/V.s$

E : Electric field density. (V/cm)

* $\boxed{I = J_h \cdot Area}$ (A)

Area : Semic. Cross Sectional Area (Cm^2)

(ii) For hole (P-Type) :-



(P-Type)

$\boxed{J_p = e \cdot p \cdot \mu_p \cdot E}$ (A/Cm^2)

J_p : h^+ drift current density.

p : h^+ concentration ($\#/Cm^3$)

μ_p : h^+ mobility = 450 ($Cm^2/V.s$)

* The total drift current density (J):

$$\boxed{J = J_n + J_p}$$

$$= ((e \cdot n \cdot \mu_n) + (e \cdot p \cdot \mu_p)) E \quad (A/cm^2)$$

$$J = \sigma \cdot E$$

σ : conductivity. $(1/\Omega \cdot cm)$

$$\sigma = \sigma_n + \sigma_p$$

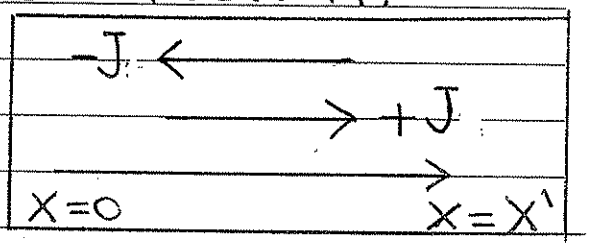
$$\rho = \frac{1}{\sigma} \quad (\Omega \cdot cm)$$

* Since σ is directly proportional to No. of e^- and No. of h^+;
So we can control the conductivity Via controlling Doping Level.

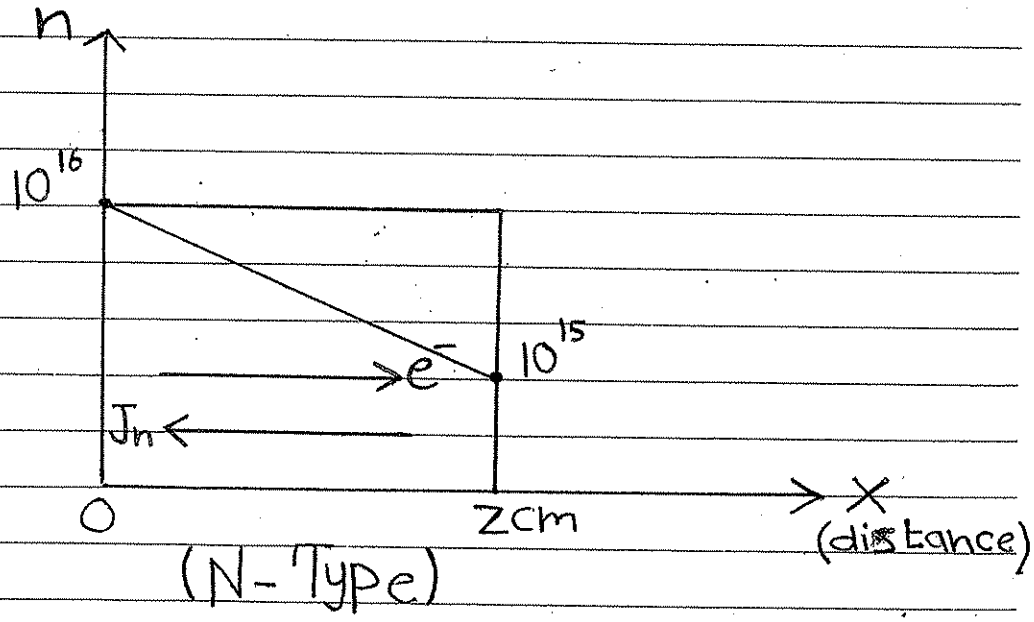
$\Rightarrow$ Doping $\uparrow$ $\Rightarrow$ Concentration $\uparrow$

2) Diffusion Current Density : (A/cm^2)

Movement of carriers Due to difference in Concentration where carriers move from high concentration Region to low concentration Region. The direction of this current is (+Ve) X direction.



(i) Electron diffusion current density (J_n):



(N-Type)

$$J_n = -e \cdot D_n \cdot \frac{dn}{dX} \quad (A/cm^2)$$

(-) direction.

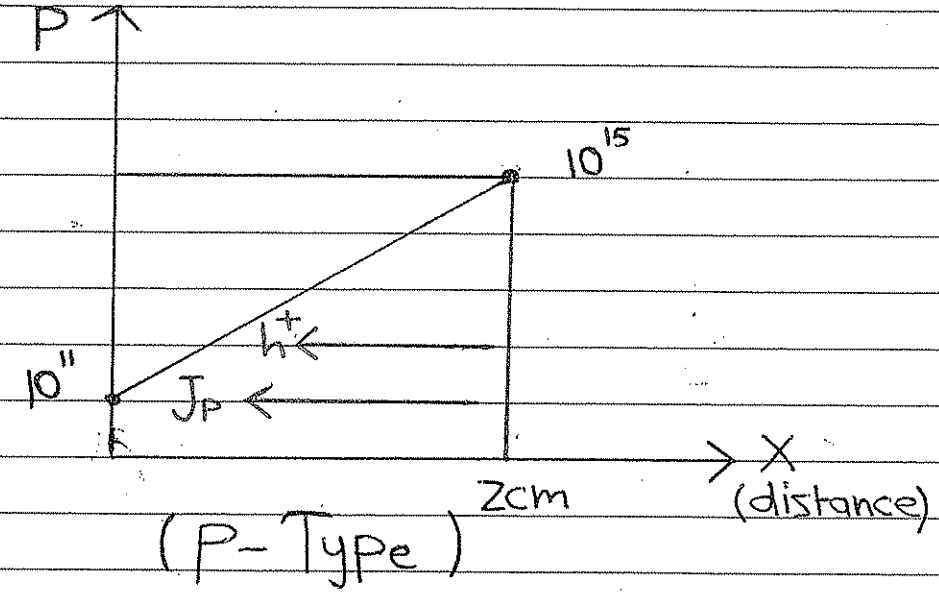
J_n : Electron diff. current density, (A/cm^2).

e : e^- Charge (C)

D_n : e^- diffusion Coefficient, (cm^2/s) given

$\frac{dn}{dX}$: e^- gradiant $(\#/cm)$.

(ii) Hole diffusion current density (J_p):



(P-Type)

$$J_p = -e \cdot D_p \cdot \frac{dp}{dx} \quad (A/cm^2)$$

↓

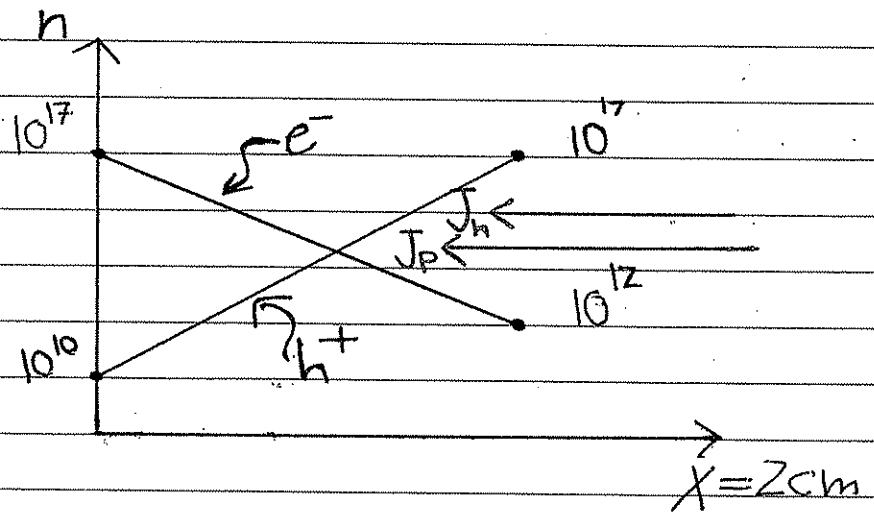
((X) direction).

J_p : Hole diff. Current density. (A/cm^2)

D_p : h^+ diffusion Coefficient (cm^2/s).

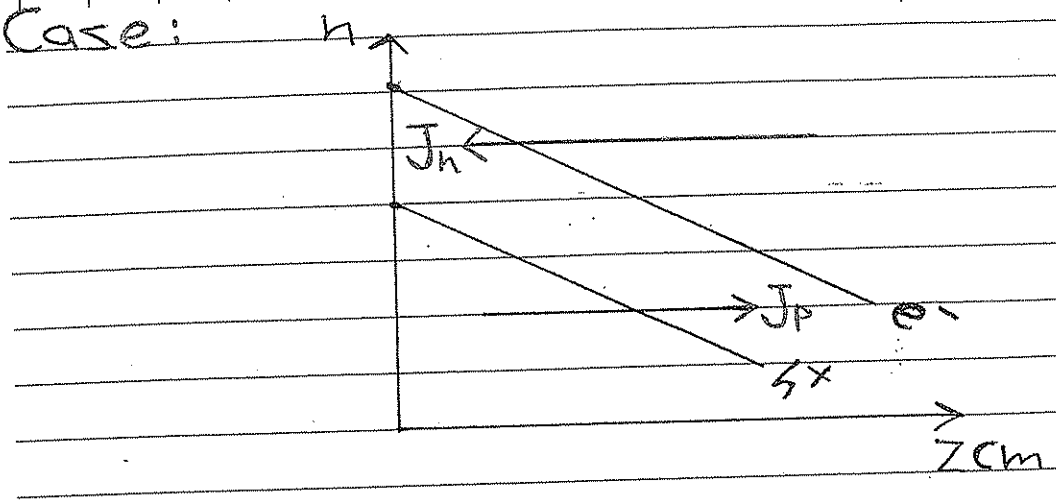
$\frac{dp}{dx}$: h^+ gradiant ($\#/cm$).

Case:



$$J = -(J_n + J_p)$$

Case:



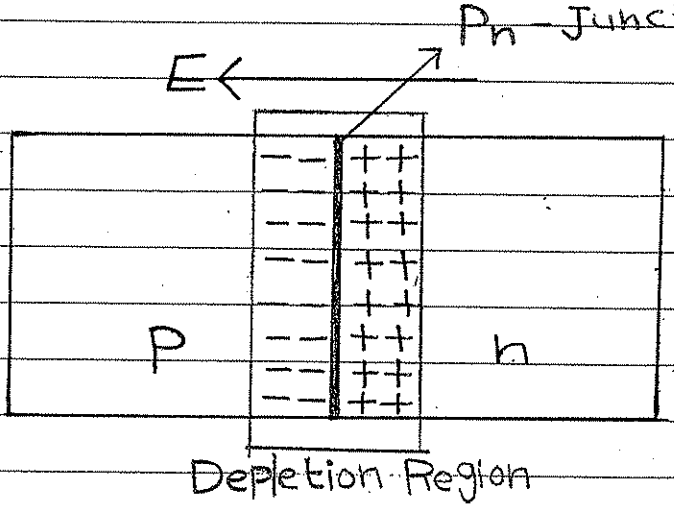
$$J = J_P - (J_h)$$

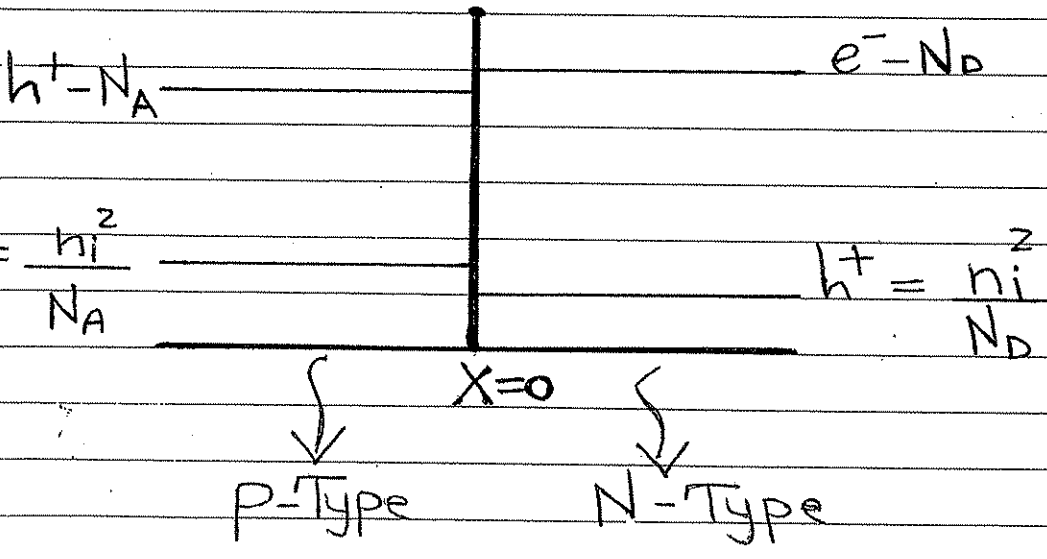
* Biasing :-
(DC Voltages لعمل الدوائر الإلكترونية . Ele. devices)

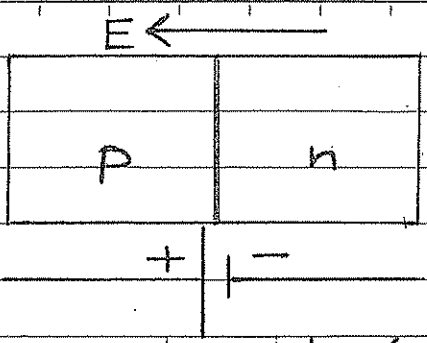
The (pn) Junction :-

1) (ph)-Jn. in Thermal Equilibrium :

*(No biasing) ⇝ (No DC Voltage)







$$V_{bi} = \frac{kT}{e} \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right)$$

$$= V_T \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right)$$

$$\rightarrow V_T = \frac{k\left(\frac{eV}{k}\right) \cdot T(k)}{e}$$

$$= (V) \rightsquigarrow \text{Volt.}$$

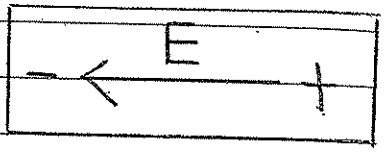
*At Room Temp. : *T = 300k

$$*e = 1.6 \times 10^{-19} C$$

$$*k = 86 \times 10^{-6} ev/k$$

$$\Rightarrow V_T = 0.026 V = 26 mV.$$

1) Due to difference in Concentration (e^-) move from (N) to (p) and (h^+) move From (p) to (N) Leaving +ve and -ve Ions, and establishing an internal E-field

directed from N to P. 

2) The movement of Carriers will be Stopped When the diffusion force balance E-Field Force.

$$\text{diff. force} = \text{E-field force}$$

3) This Field will induce an internal Voltage called built-in Voltage (barrier Potential) give by:

$$V_{bi} = \frac{KT}{e} \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right)$$

$$= V_T \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right)$$

Where :-

V_{bi} : built-in Potential barrier.

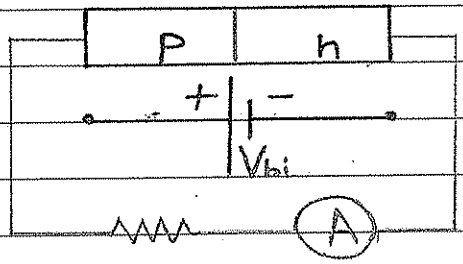
$V_T = \frac{KT}{e}$: Thermal Voltage and it is 26 mV at Room Temp..

N_A , N_D : Acceptor and Donor Concentration respectivity.

n_i : Intrinsic Carrier Concentration.

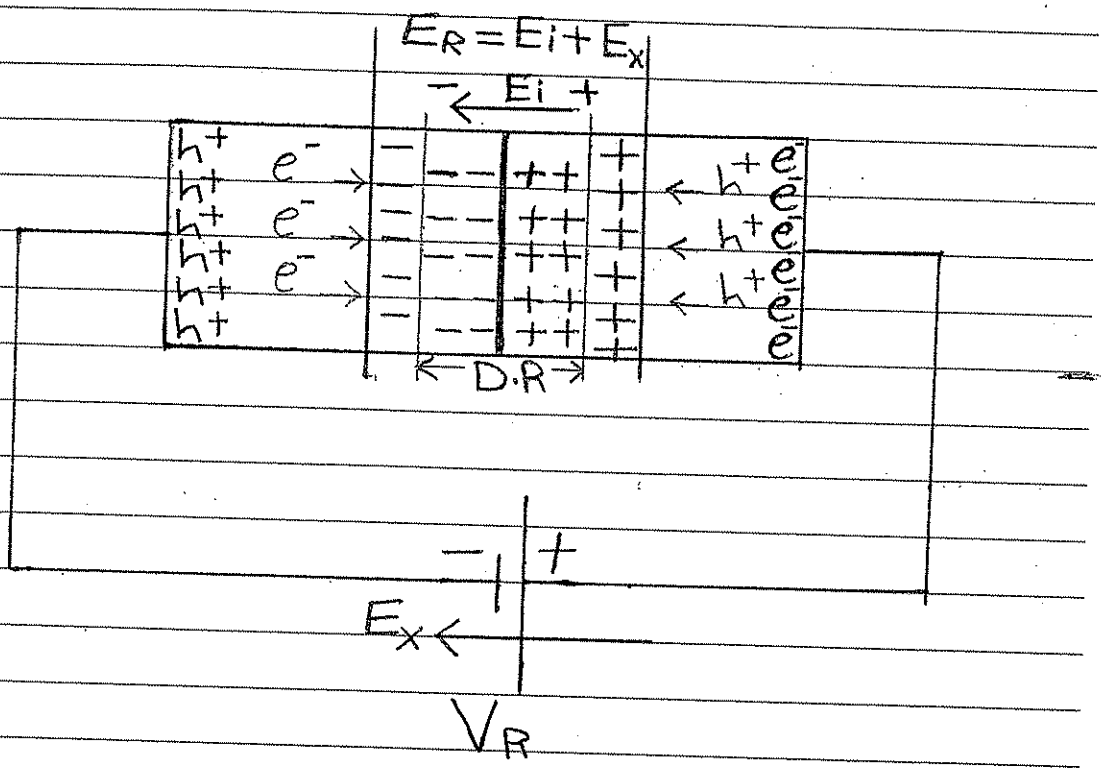
$$n_i = B T^{3/2} e^{\frac{-E_g}{2KT}}$$

Note:



: without any bias
لا تدفع تيار و لا يمكن قياسها.

2) Reverse - bias (Pn) - Jn :



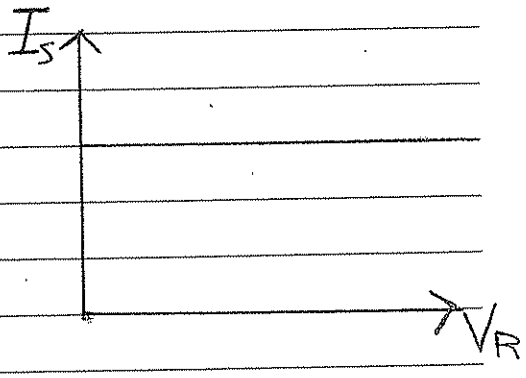
Due to this basing, the majority carriers will move away from the junction. (No maj. carriers will cross the Jn.)

The width of Depletion Region will increase with increasing V_R.

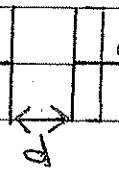
Only very small current carried by majority carrier will flow conventionally from N to P called (Reverse-Bias Saturation Current (I_S)). [تيار الاشباع العكسي]
(بمعنى أنه لا يعتمد على V_R)

It is in range of ($10^{-18} \rightarrow 10^{-12}$) A.

(I_S) depends on Temp. (it Doubles every 5°C increase in Temp.).

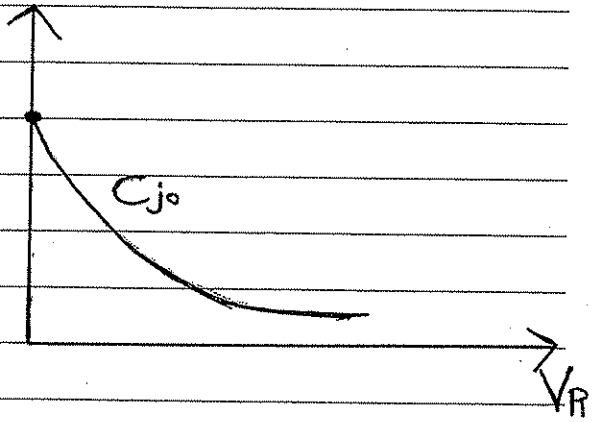


$$C = \frac{\epsilon \cdot A}{d}$$



A capacitance is associated (مرتبط) with the pn junction When a reverse-bias voltage is applied. This junction capacitance, or depletion layer capacitance, can be written in the form:

$$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{V_{bi}}}}$$



Where:

C_j : Junction Capacitance.

C_{j0} : Zero-bias capacitance. (given)

V_R : Reverse Voltage.

V_{bi} : built-in Voltage.

$$\left(V_{bi} = V_T \, Ln\left(\frac{N_A - N_D}{n_i^2}\right) \right).$$

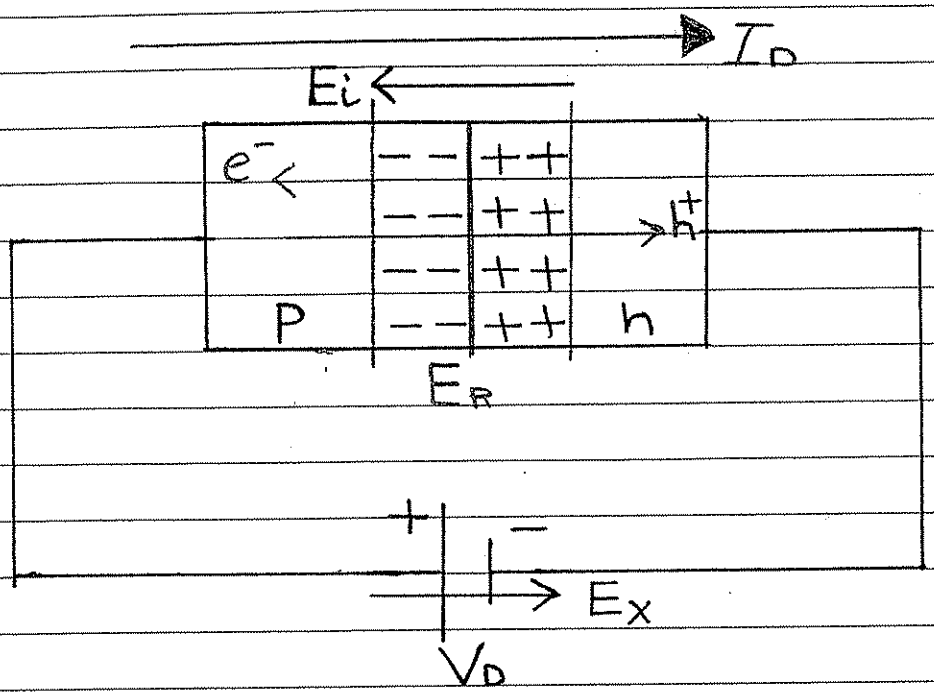
EXA. : Calculate (C_j) for a Rev. bias pn jn. with $V_R = 3V_{bi}$, $C_{j_o} = 8$ P.F ?

Sol.

$$C_j = \frac{C_{j_o}}{\sqrt{1 + \frac{V_R}{V_{bi}}}}$$

$$= \frac{8}{\sqrt{1 + \frac{3V_{bi}}{V_{bi}}}} = 4 \text{ P.F} \quad \#.$$

3) Forward - bias (Ph) - Jn. :-



The Forward bias Forces the majority Carrier to cross the junction, a Current (I_D) will flow from P → h (conventionally) (I_D) is related to (V_D) by the following relation :

$$I_D = I_S e^{\frac{V_D}{nV_T}}$$

Where :

I_D : Forward Current . (mA)

I_S : Reverse - bias Saturation Current.

V_D : Forward Voltage across the junction.

V_T : Thermal Voltage (26mV).

n : Ideality Factor.

* n=1 (For high Current level).

* n=2 (For Low Current level).

(n) related to recombination of maj. Carriers.

✳ Ideal Current – Voltage Relationship:

$$I_D = I_s\left(e^{\frac{V_D}{nV_T}} - 1\right)$$

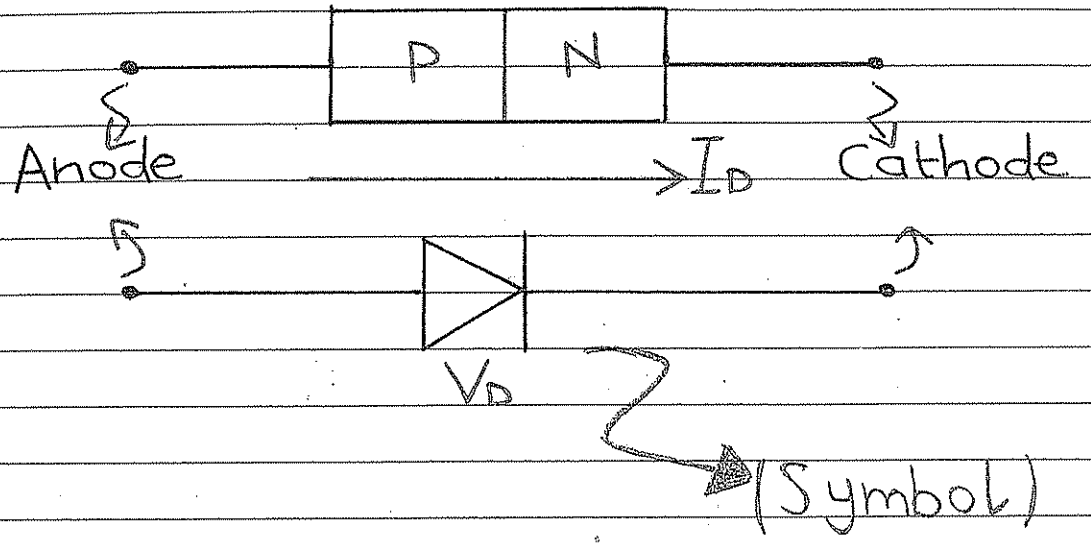
→ When V_D is (+Ve) (Forward):

$e^{\frac{V_D}{nV_T}} \gg 1$, $I_D = I_s e^{\frac{V_D}{nV_T}}$.

→ When V_D is (−Ve) (Reverse):

$e^{\frac{-V_D}{nV_T}} \ll 1$, $I_D \simeq -I_s$.

* PN Junction Diode :-



PN Junction Diode : A PN Jn. Fitted in a Propriate case with two Conducting Leads to connect it in a Circuit With other Circuit elements.

* Diode Model :

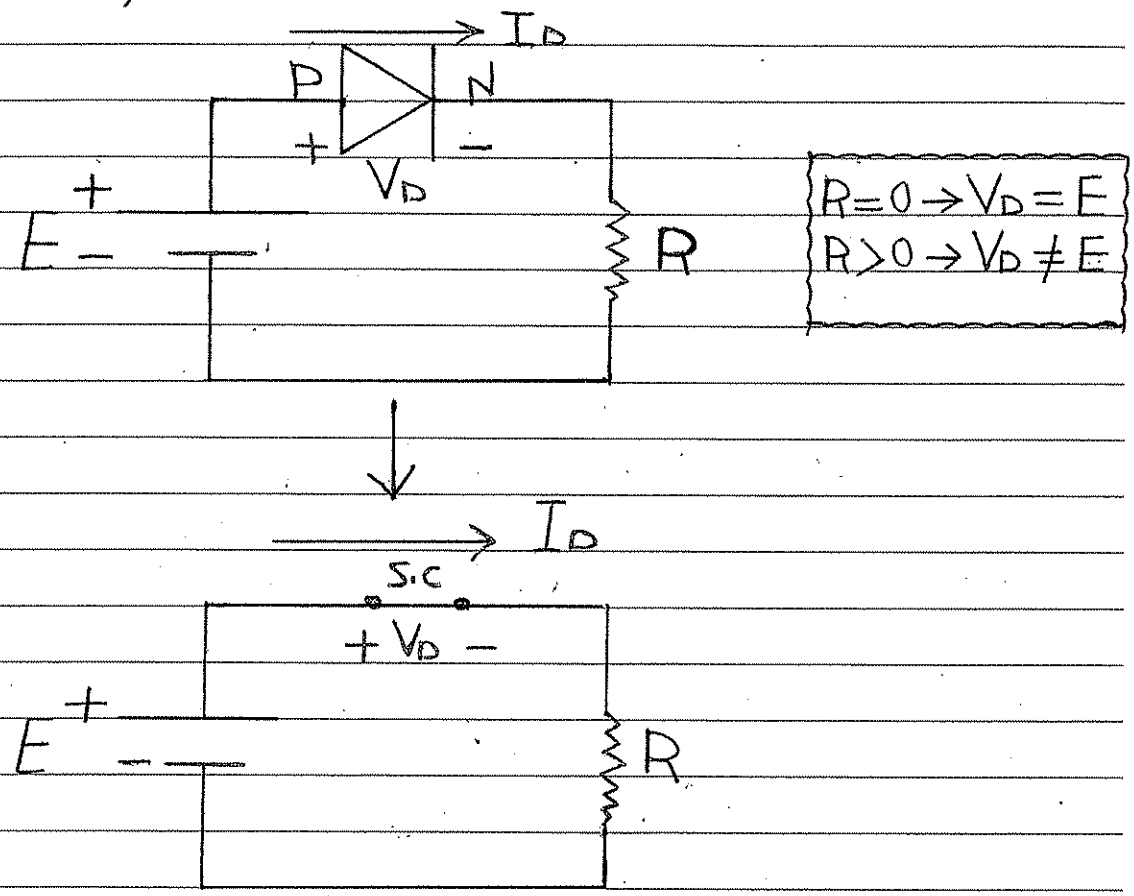
1) Ideal Diode.

2) Real Diode.

1) Ideal Diode :

(i) In Forward, it is Short Circuit,

$V_D = 0$, $I_D > 0$.

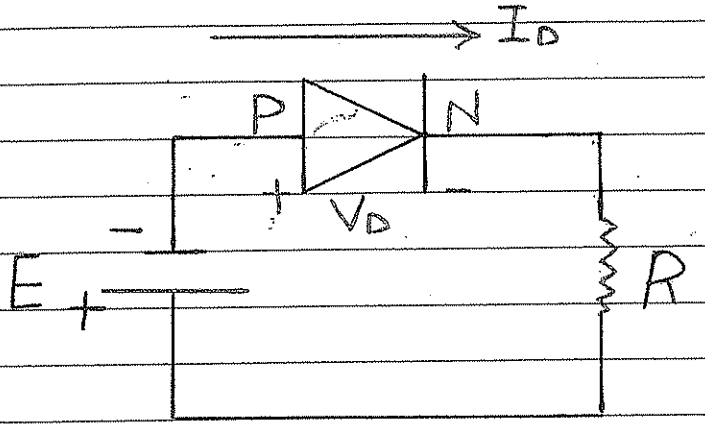


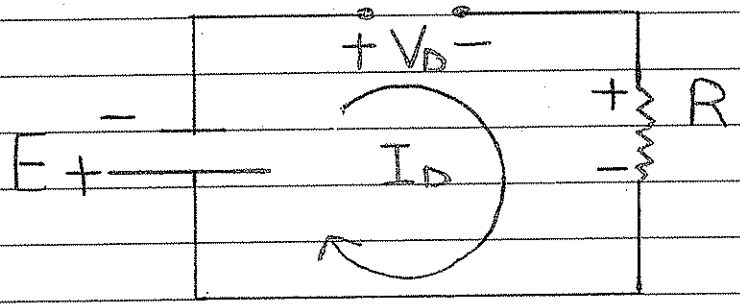
$$V_D = 0$$

$$I_D = \frac{E}{R}$$

(ii) In Reverse, it is Open Circuit;

$I_D = 0$, V_D 0.



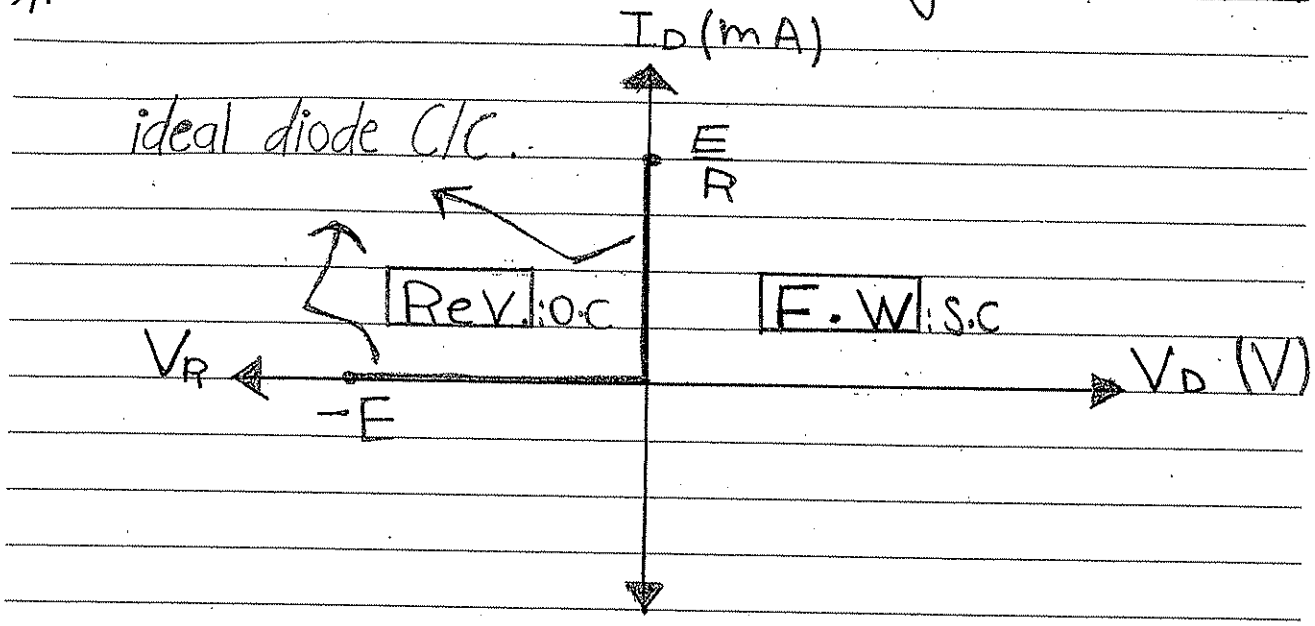


$\boxed{I_D = 0}$

$\Rightarrow$ KVL : $E + V_D + I_D R = 0$ ($I_D R \to 0$)

$\boxed{V_D = -E}$

* Diode Current – Voltage Characteristics



Ideal diode :-

* F.W : S.C ; $V_D = 0$

$$I_D = \frac{E}{R} > 0$$

* Rev. : O.C ; $I_D = 0$

$$V_D = -E < 0$$

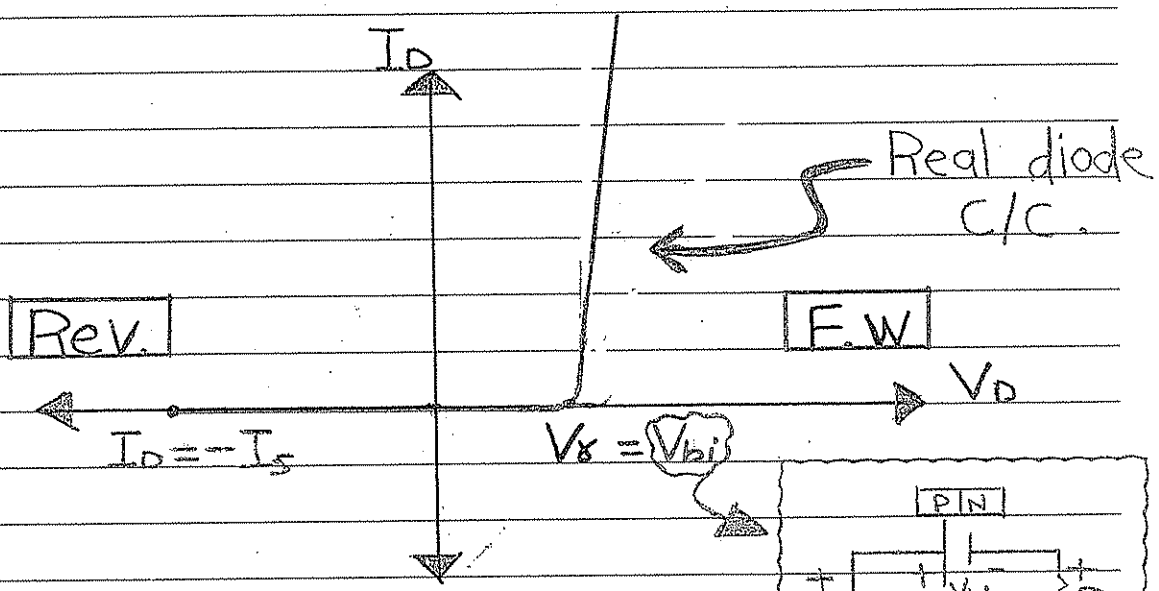
2) Real Diode :

(i) In Forward ;

$(V_D > 0)$, $e^{\frac{V_D}{nV_T}} \gg 1$, $I_D \simeq I_S e^{\frac{V_D}{nV_T}}$.

(ii) In Reverse ;

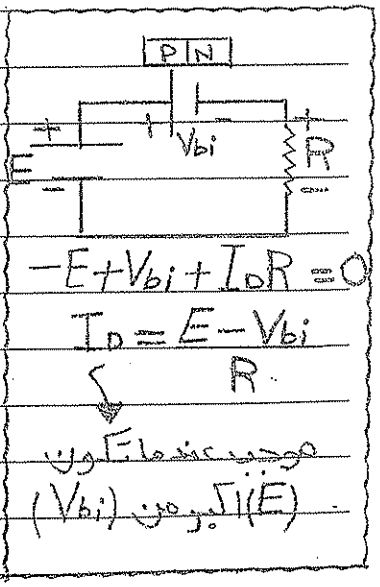
$(V_D < 0)$, $e^{\frac{-V_D}{nV_T}} \ll 1$, $I_D \simeq -I_S$.



V_γ = Cut-in Voltage

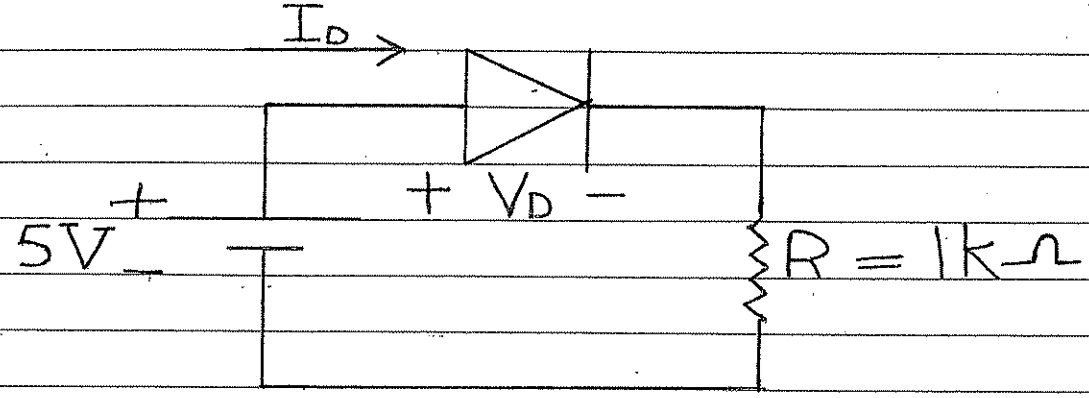
= 0.3 V → Ge diode.

= 0.7 V → Si diode.



✳ Diode Circuits : 'DC' Analysis & Models :

(How to find (I_D, V_D) ?) :-



To Solve :

1) Iteration Method :- مبنية على التجربة والخطأ

$$-5 + V_D + I_D \cdot R = 0$$

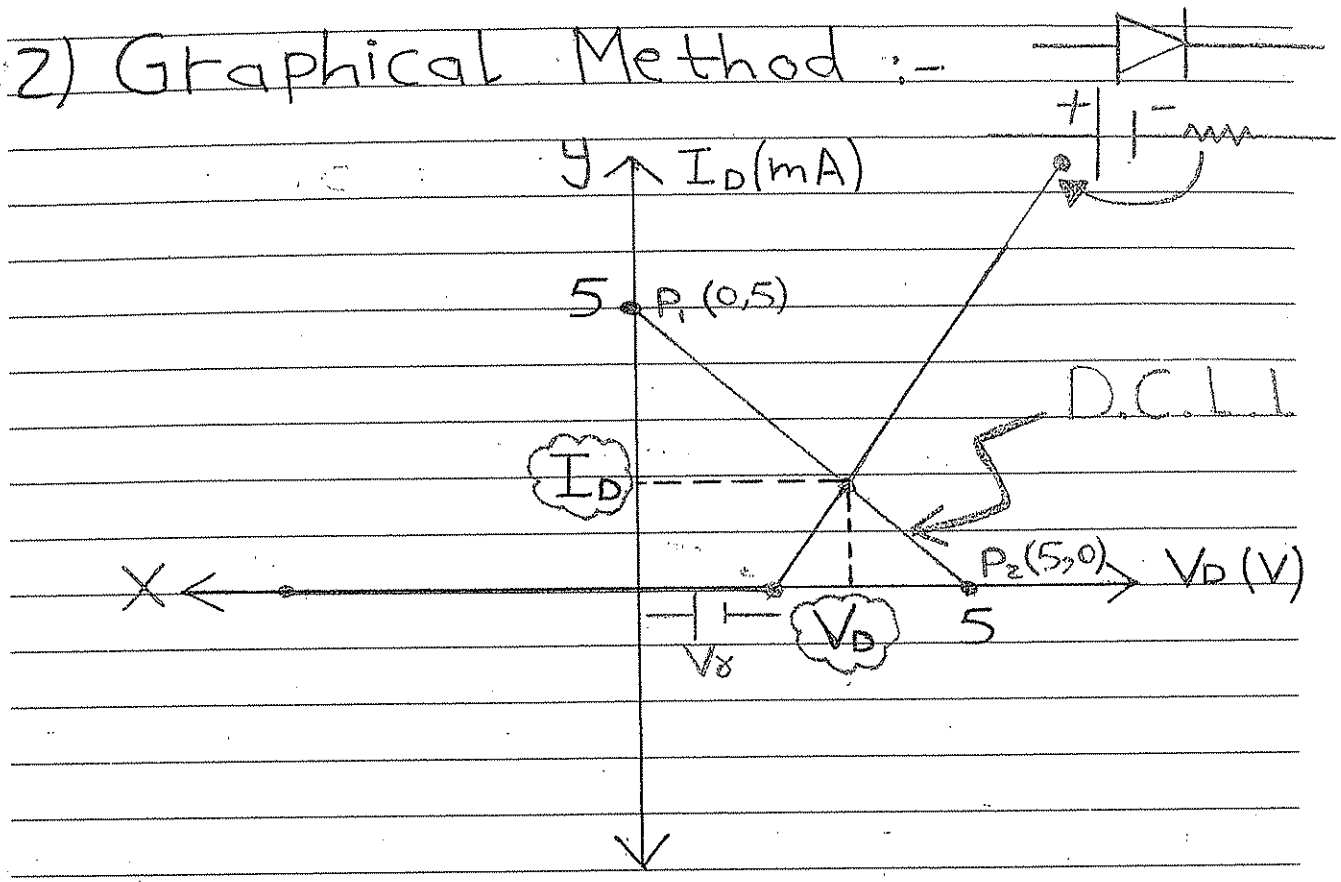
$$V_D = 5 - I_D \cdot R$$

$$V_D = 5 - I_S e^{\frac{V_D}{nV_T}} \cdot R$$

(I_S : given, n : given, R : given)

* نحل بفرض قيمة لـ (V_D) وعندما يتساوى الحد الأيمن مع الحد الأيسر يكون الفرض هو القيمة الصحيحة.

2) Graphical Method :-



This method Requires diode C/C in Scale.

1) Write KVL for the cct. :-

$$-5 + V_D + I_D R = 0$$

2) find D.C lead-line equ. :
(I_D, V_D, relation)

$$\underbrace{I_D}_{y} = \frac{5}{R} - \frac{V_D}{R}$$

$$y = b + mx \quad ; \quad m = \text{slope} = -\frac{1}{R}$$

3) Draw D.C load line on diode C/C:

(i) For $V_D = 0$, $I_D = \frac{5}{R} = 5\,mA$.

→ $P_1(0, 5\,mA)$

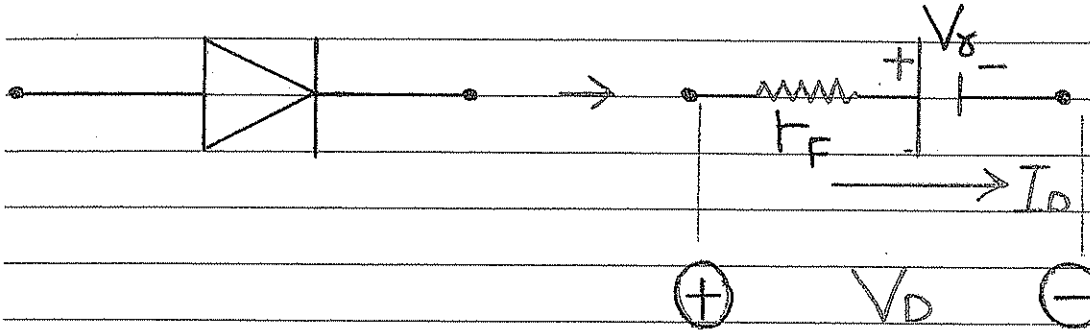
(ii) For $I_D = 0$, $V_D = 5\,V$

→ $P_2(5V, 0)$

4) The Intersection of D.C.L.L with diode C/C gives the solution I_D, V_D.

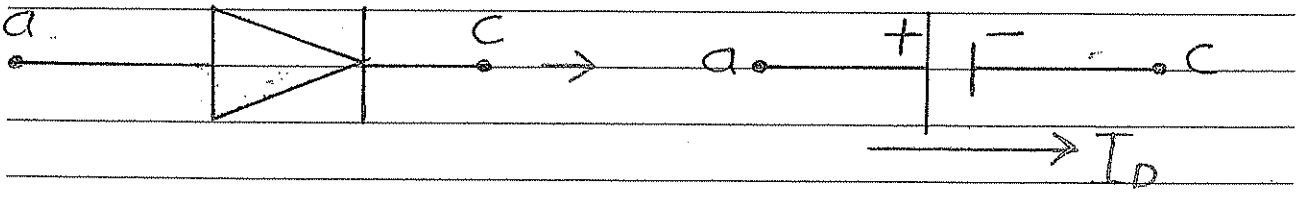
3) Using Diode Linear Model (piecewise Linear Model) :-

F.W



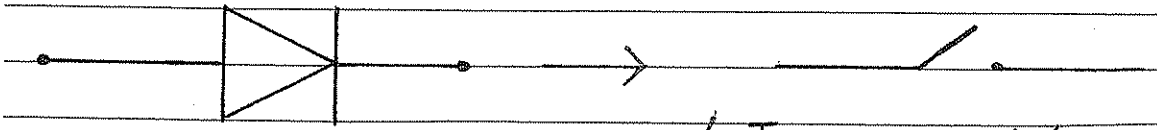
$$(V_D = I_D \cdot r_F + V_\gamma)$$

For negligible r_f ($r_f = 0$) :-



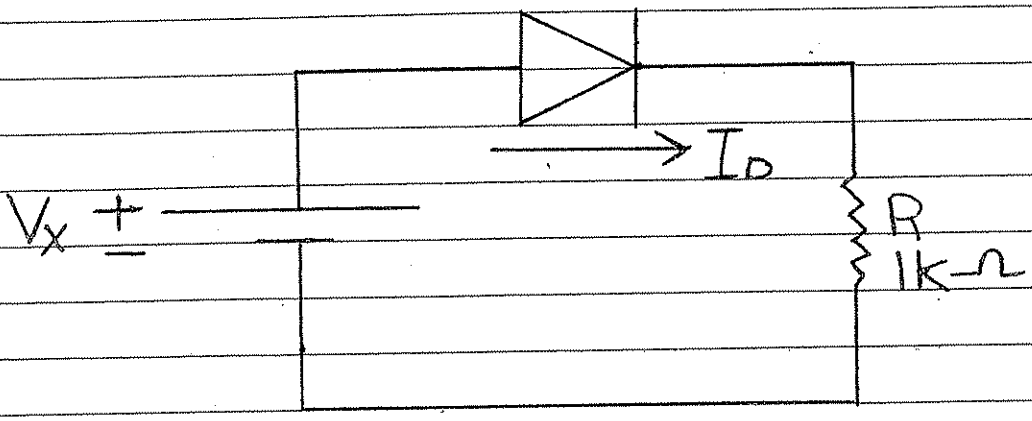
$$(V_D = V_\gamma)$$

Rev.



$$(I_D = 0 \ , \ V_D < 0)$$

EXA. Find I_D, V_D, P_D, Where :-

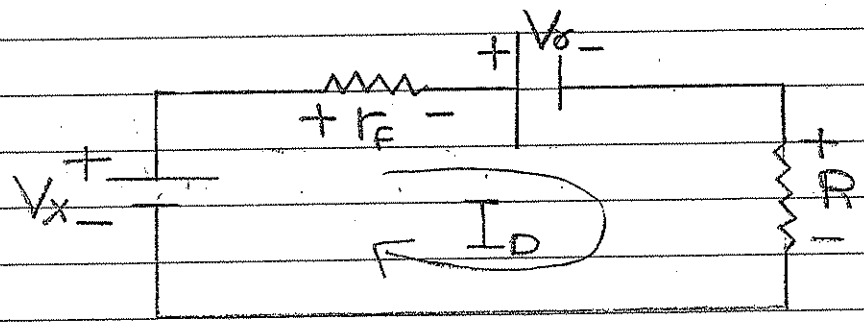


1) $V_x = 0.5\ V$.

$V_\gamma = 0.6\ V$.

$r_f = 20\ \Omega$.

Sol.



KVL :

$$V_x + I_D \cdot r_f + V_\gamma + I_D \cdot R = 0$$

$$I_D = \frac{V_x - V_\gamma}{(r_f + R)} = \frac{0.5 - 0.6}{1020\ \Omega} < 0$$

Since $I_D < 0 \therefore D \rightarrow OFF$.

→ $I_D = 0$; $P_D = V_D \cdot I_D = 0$

$-V_x + V_D + I_D \cdot R = 0$

$V_D = V_x = 0.5\ V.$

2) $V_x = 5\ V.$

$V_\gamma = 0.6\ V.$

$r_f = 20\ \Omega.$

Sol. $I_D = \frac{5 - 0.6}{1020} = \frac{4.4}{1020} = 4.35\ mA.$

$V_D = I_D \cdot r_f + V_\gamma$

$= 4.35m \cdot 20\ \Omega + 0.6 = 0.687\ V.$

$P_D = I_D * V_D$

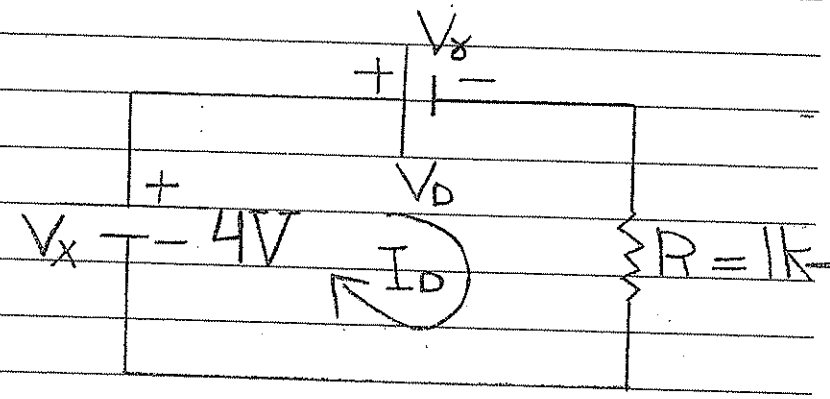
$= 4.35m * 0.687$

$= 2.8\ mW.$

3) $V_x = 4\,V$.

$V_\gamma = 0.6\,V$.

$r_f = 0$.



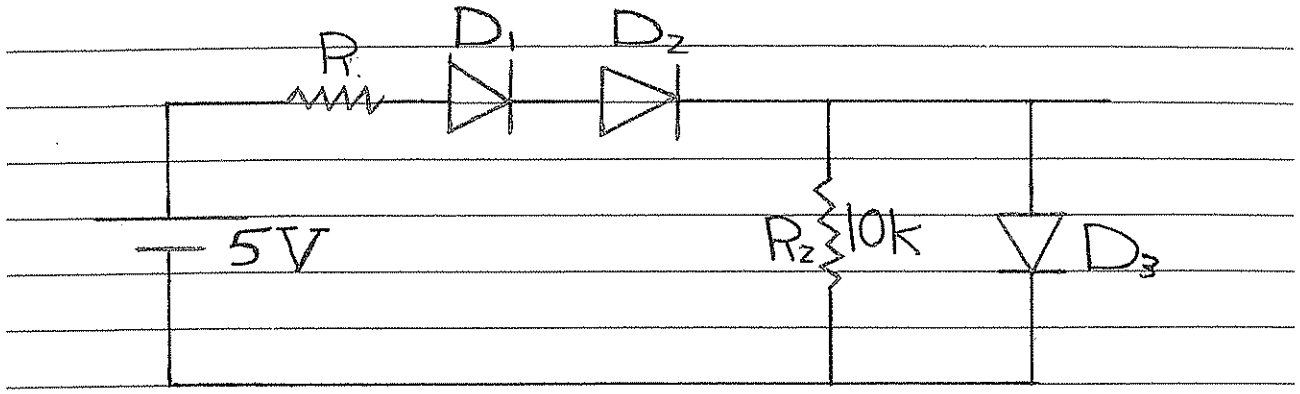
$$I_D = \frac{(4 - 0.6)}{1k} = 3.4\ mA.$$

$$V_D = V_\gamma = 0.6\ V.$$

$$P_D = I_D \cdot V_D = 3.4 * 0.6$$

$$= 2.04\ mW.$$

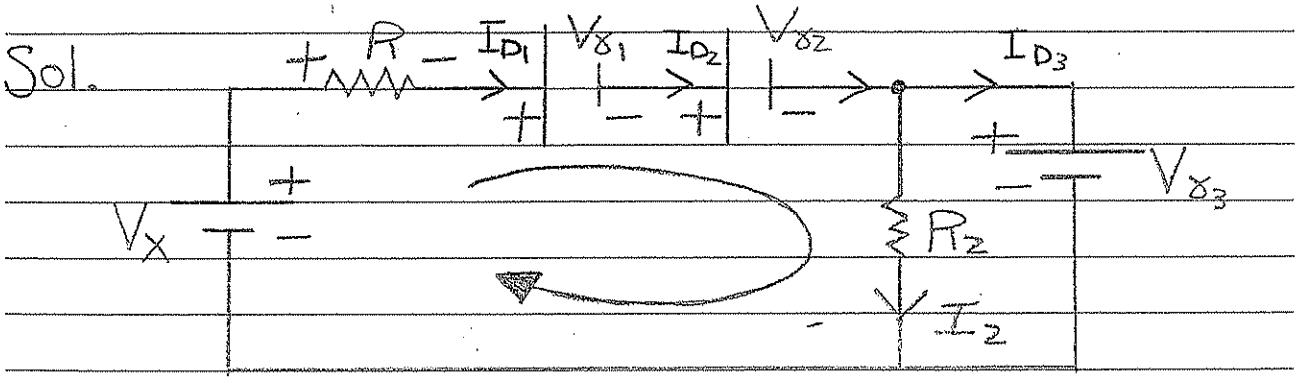
problem 1.50 :- -(page 63) - :



Calculate (R) such that : $I_{D_1} = 2 I_{D_3}$

(Assume D_1, D_2, D_3 identical with $V_\gamma = 0.65\ V$) .

Sol.



$$-V_X + I_{D_1} \cdot R + V_{\gamma_1} + V_{\gamma_2} + V_{\gamma_3} = 0$$

$$R = \frac{V_X - (V_{\gamma_1} + V_{\gamma_2} + V_{\gamma_3})}{I_{D_1}}$$

$$I_{D_1} = I_{D_2} = 2 I_{D_3}$$

$$I_2 = \frac{V_{63}}{R_2} = \frac{0.65}{10} = 0.065\,mA.$$

* From the given condition :-

$$I_{D_3} = I_2 = 0.065\,mA.$$

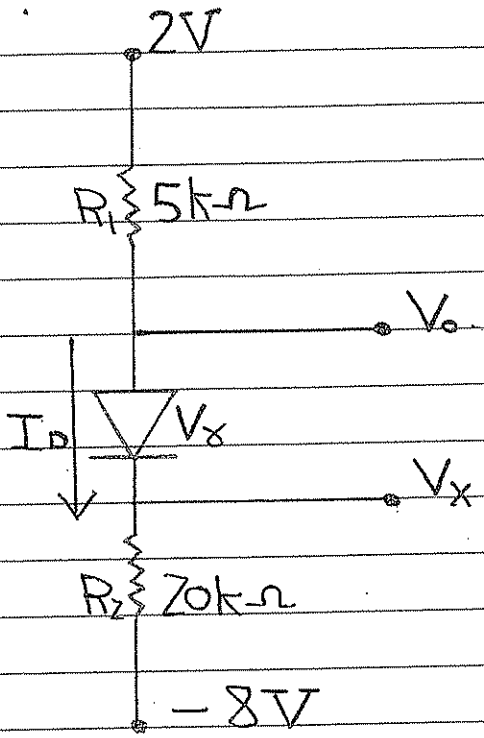
$$I_{D_1} = 2 * 0.065m = 0.13\,mA.$$

$$\rightarrow R = \frac{5 - 1.95}{0.13} = \frac{3.05\,V}{0.13\,mA}$$

$$= 23.46\,k\Omega.$$

EXA. Given : $V_\gamma = 0.6\ V$

Find : I_D, V_o, V_x ?



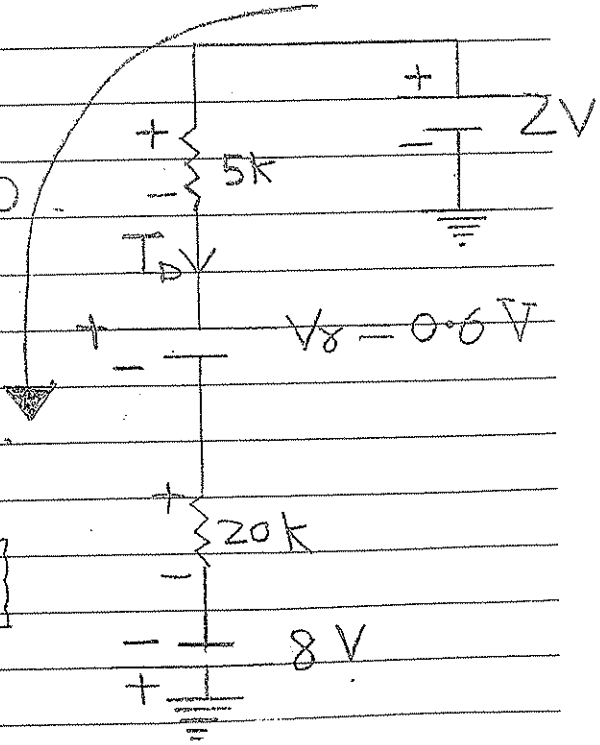
Sol. ASSume the diode is (on).

KVL :

$-2 + 5k \cdot I_D + V_\gamma + 20k \cdot I_D - 8 = 0$

$I_D = \frac{2 + 8 - 0.6}{5 + 20} = \frac{9.4}{25} = 0.376\ mA$

$\therefore$ Diode on $\rightarrow I_D > 0$

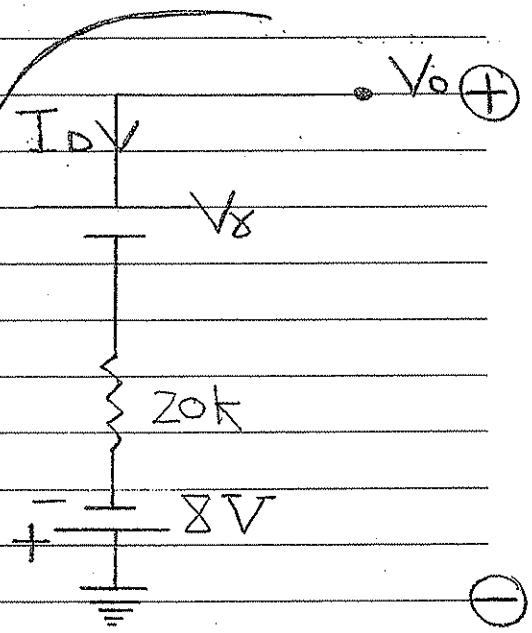


KVL:

$-V_o + V_x + I_D \cdot R_2 - 8 = 0$

$V_o = 0.6 + 7.52 - 8$

$= 0.12\ V.$

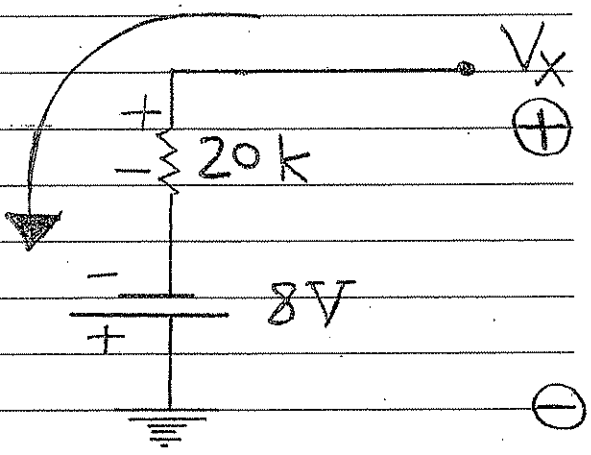


KVL:

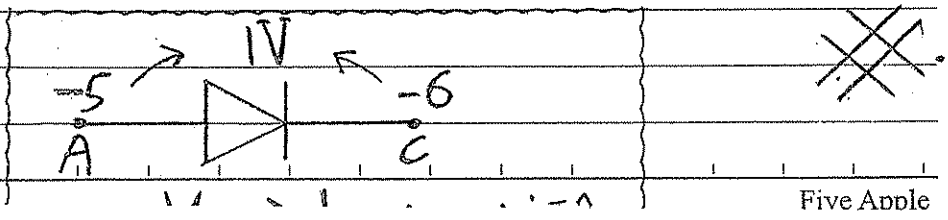
$-V_x + I_D \cdot R_2 - 8 = 0$

$V_x = 7.52 - 8$

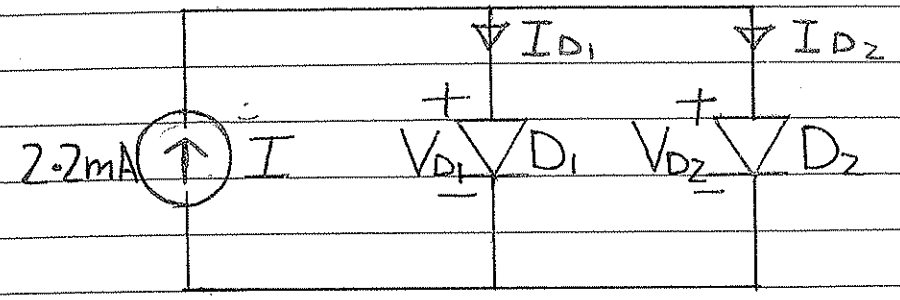
$= -0.48\ V.$



* $V_o - V_x = 0.12 - (-0.48) = 0.6 = V_x$



EXA. :



$I_{S_1} = 5 \times 10^{-14}\,A$; $I_{S_2} = 5 \times 10^{-13}\,A$

Find I_{D_1}, I_{D_2}, V_{D_1} ? $(n=1, V_T = 26mV)$

Sol.

$I = I_{D_1} + I_{D_2} = 2.2mA.$

$* \; I_{D_1} = I_{S_1} \cdot e^{\frac{V_{D_1}}{nV_T}}$

$* \; I_{D_2} = I_{S_2} \cdot e^{\frac{V_{D_2}}{nV_T}}$

$$\frac{I_{D_1}}{I_{D_2}} = \frac{I_{S_1}}{I_{S_2}} = \frac{5 \times 10^{-14}}{5 \times 10^{-13}} = 0.1$$

$\rightarrow I_{D_1} = 0.1\, I_{D_2}$

$* \; I_{D_1} + I_{D_2} = 2.2m$

$0.1\, I_{D_2} + I_{D_2} = 2.2m$

$1.1\, I_{D_2} = 2.2m \rightarrow \boxed{I_{D_2} = 2mA}$

$I_{D_1} = 0.1 * 2$

$\boxed{I_{D_1} = 0.2\,mA}$

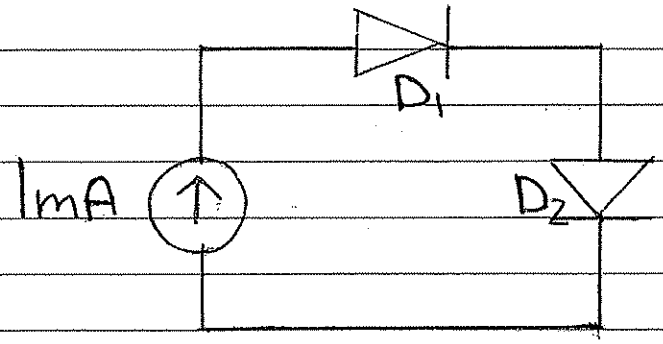
$\rightarrow V_{D_1} = n V_T \ln \frac{I_{D_1}}{I_{S_1}}$

$= 0.026 * \ln \frac{0.2\,m}{5 \times 10^{-14}}$

$= 0.57\ V$

$= V_{D_2}$ ∴ ✗✗

EXA. :



$I_{S_1} = 5 \times 10^{-14}\ A$; $I_{S_2} = 5 \times 10^{-13}\ A$

Find V_{D_1}, V_{D_2}, P_D ?

Sol.

* $I_{D1} = I_{D2} = 1mA$.

* $V_{D1} = n V_T \ln \frac{I_{D1}}{I_{S1}}$

$= 1 * 0.026 * \ln \frac{1mA}{5 \times 10^{-14}}$

$= 0.61\ V$.

* $V_{D2} = n V_T \ln \frac{I_{D2}}{I_{S2}}$

$= 1 * 0.026 * \ln \frac{1mA}{5 \times 10^{-13}}$

$= 0.55\ V$.

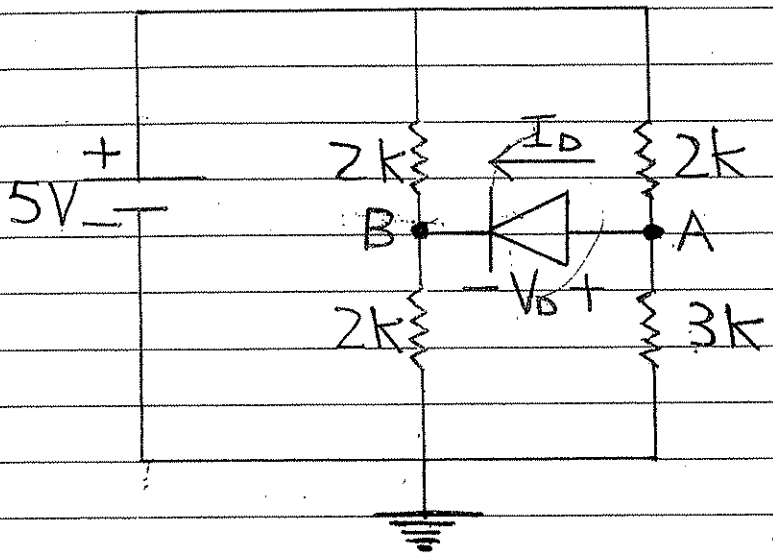
$P_{D1} = I_{D1} * V_{D1}$

$= 1m * 0.61 = 6.1 \times 10^{-4}\ W$.

$P_{D2} = I_{D2} * V_{D2}$

$= 1m * 0.55 = 5.5 \times 10^{-4}\ W$.

EXA. :



Find I_D, V_D When the diode is:

1) Si diode with $V_\gamma = 0.7$ V.

2) Ge diode with $V_\gamma = 0.3$ V.

Sol.

Assume D → OFF.

$$V_A = \frac{5 * 3}{2+3} = 3\text{V}.$$

$$V_B = \frac{5 * 2}{2+2} = 2.5\text{V}.$$

$$V_{AB} = V_A - V_B = 3 - 2.5 = 0.5\text{V}.$$

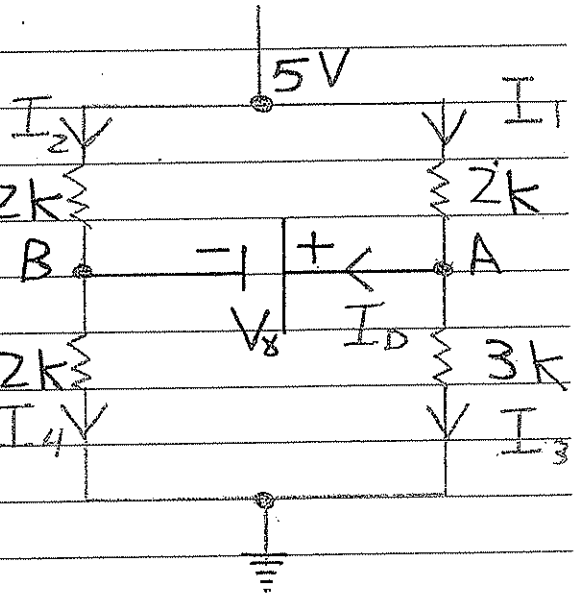
For Si diode : $V_\gamma = 0.7\ V$

$V_{AB} < 0.7\ V \rightarrow$ D : OFF.

$\rightarrow I_D = 0$, $V_D = V_{AB} = 0.5\ V$.

For Ge diode : $V_\gamma = 0.3\ V$.

$V_{AB} > 0.3\ V \rightarrow$ D : On.



KCL at node (A) :

$I_1 = I_3 + I_D$

$\frac{5 - V_A}{2} = \frac{V_A}{3} + I_D$ — (1)

KCL at node (B) :

$I_4 = I_2 + I_D$

$\frac{V_B}{2} = \frac{5 - V_B}{2} + I_D$ — (2)

from (1) : $5 - \frac{(0.3 + V_B)}{2} + \frac{0.3 + V_B}{3} + I_D = 0$

from (2) : $5 - 2V_B + 2I_D = 0$

$\boxed{V_B = 0.06\ V}$ $\boxed{I_D = -2.44\ mA}$

$$-V_A + V_\gamma + V_B = 0$$

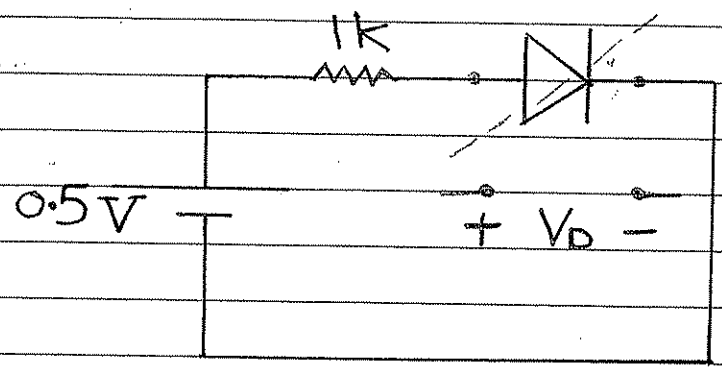
$$V_A = V_\gamma + V_B$$

$$= 0.3 + 0.06$$

$$\boxed{V_A = 0.36\ V}$$

$$\boxed{V_D = V_\gamma = 0.3\ V}$$

EXA.

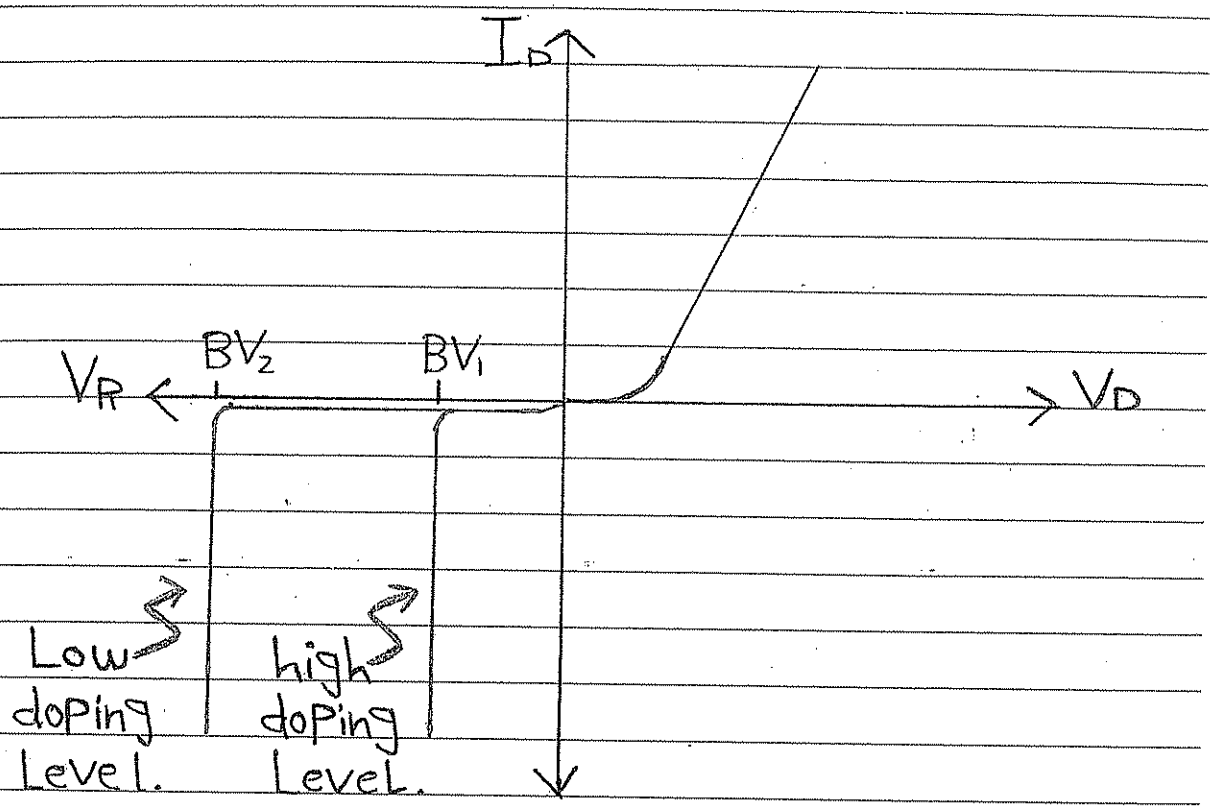


* D : off.

→ $-0.5 + I_D \cdot R + V_D = 0$

$(V_D = 0.5)$ ※

1) Breakdown Voltage : (BV) :



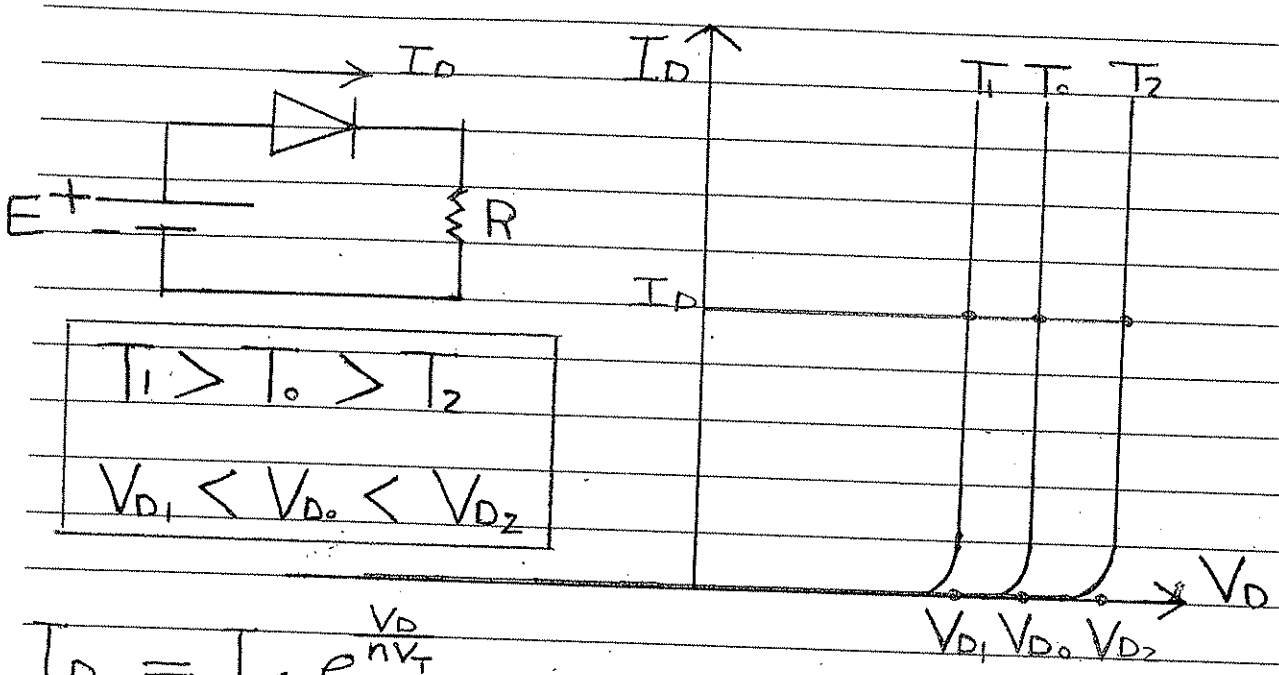
* Break down Voltage (BV) : The max. Reverse voltage which the diode can with stand.

BV : is inversaly propartional to doping Level.

$$BV \propto \frac{1}{\text{Doping Level}}$$

BV : given in data Sheet and must be avoided.

2) Effect of Temp. on diode C/C :



$$T_1 > T_0 > T_2$$

$$V_{D1} < V_{D0} < V_{D2}$$

$$I_D = I_S e^{\frac{V_D}{nV_T}}$$

$$V_D = n V_T \ln \frac{I_D}{I_S}$$

I_D ← ثابت

I_S ← يعتمد على درجة الحرارة بشكل أكبر من V_T.

$(I_S \propto T)$

as $T \uparrow$, $I_S \uparrow$

Then for the Same I_D : $V_D \downarrow$

For Si diode , V_D decrease at a rate of $2mV/1C^\circ$.

Chapter (2) :

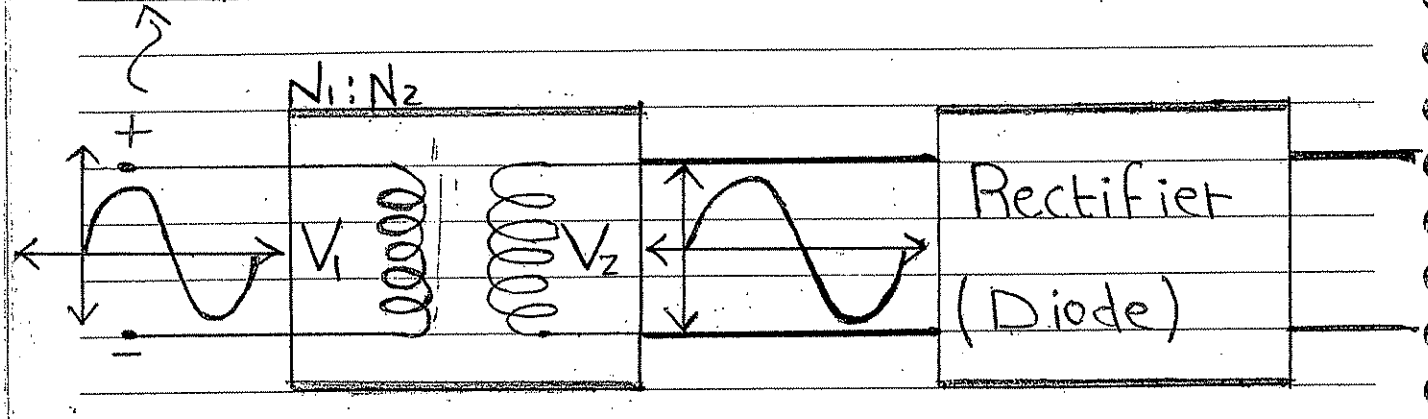
Diode Circuits :- [Diode Application] :-

1) Rectification :-

[(A.C) To (D.C) Conversion]

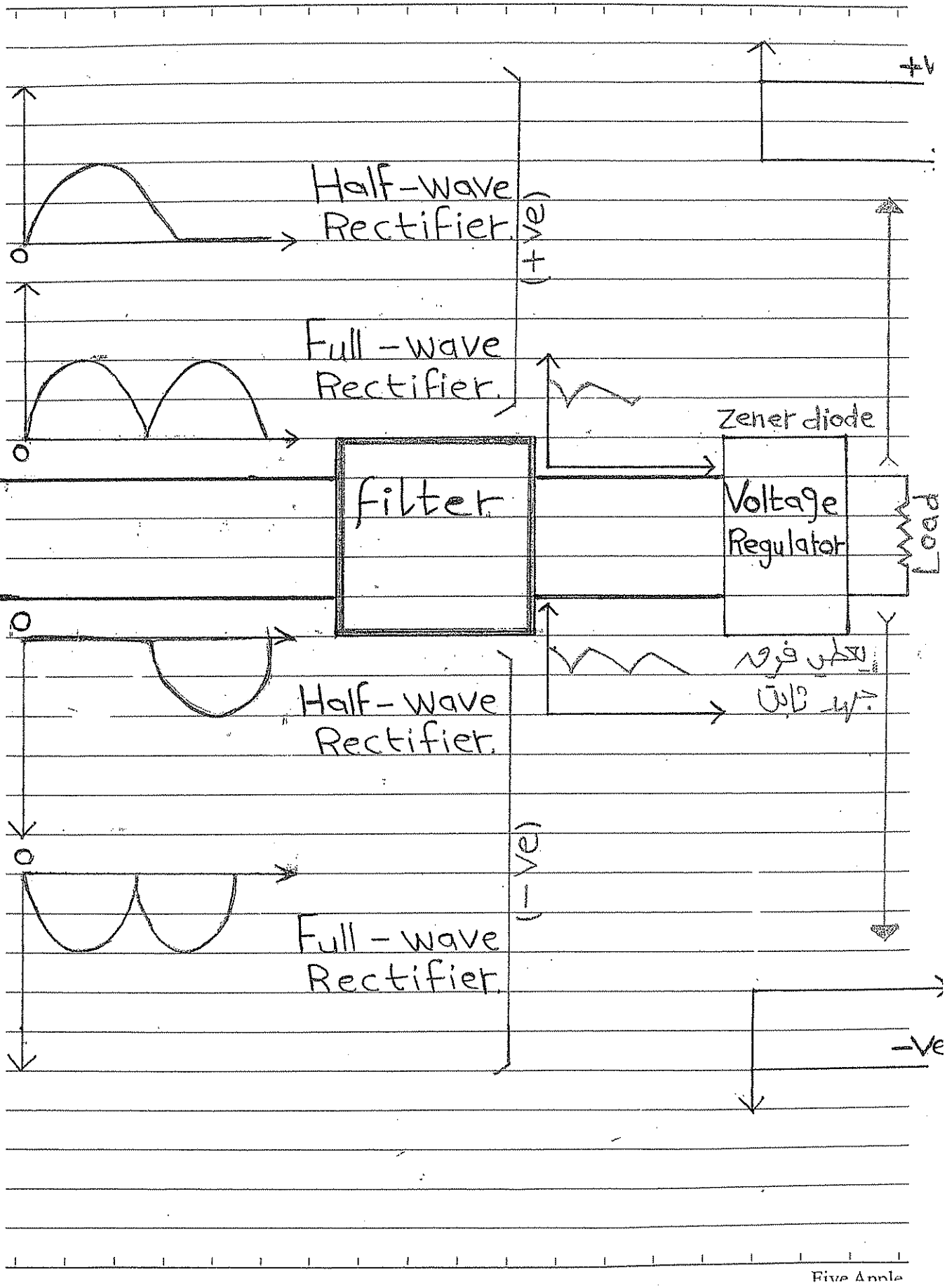
* Rectifier Circuit :- The most important Circuit in DC Power Supply, Which is a Circuit Contain Diodes.

* Block Diagram For Electronic D.C Power Supplay :-



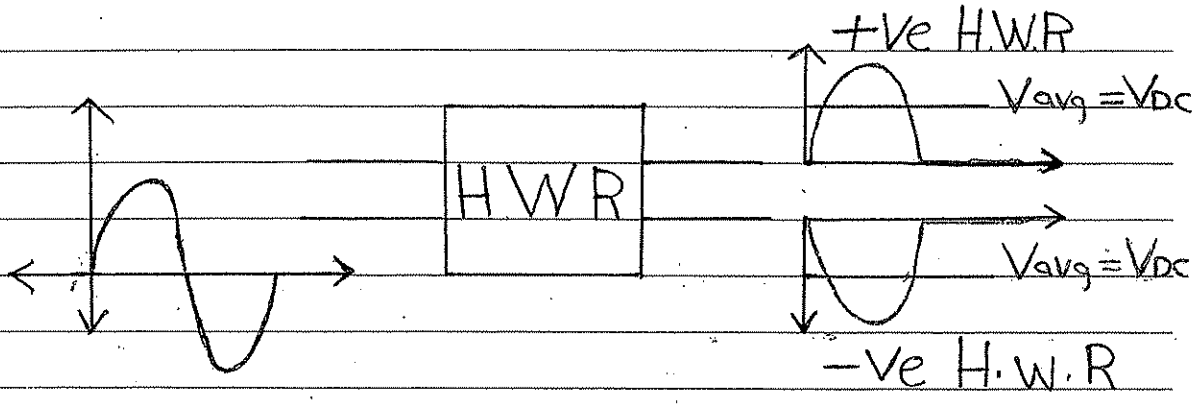
$$V_2 = \frac{N_2}{N_1} V_1$$

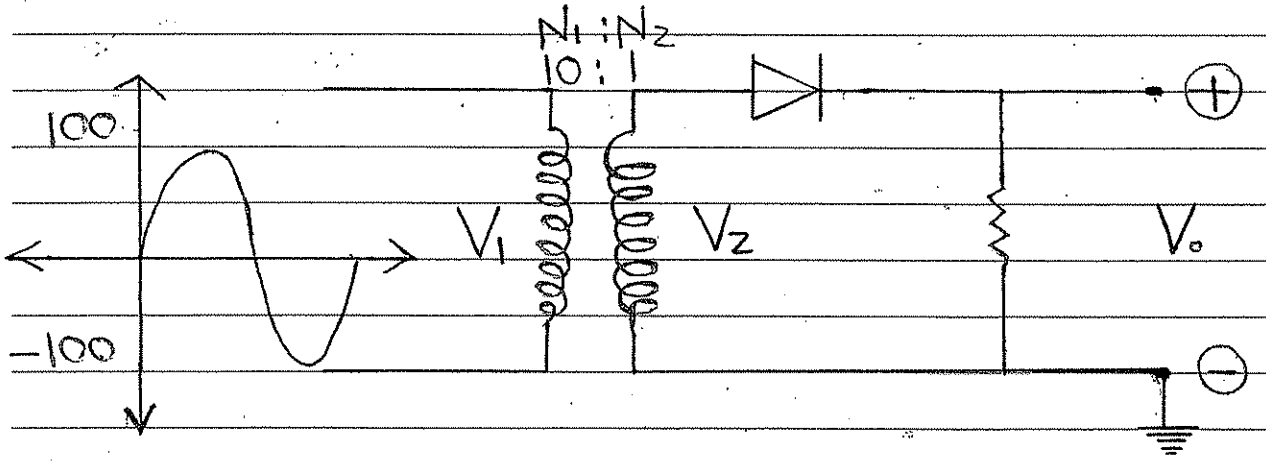
* Power transformer.


+ve
Half-wave Rectifier
Full-wave Rectifier
Zener diode
filter
Voltage Regulator
Load
Half-wave Rectifier
Full-wave Rectifier
-ve

1) Half - wave Rectifier (HWR) :

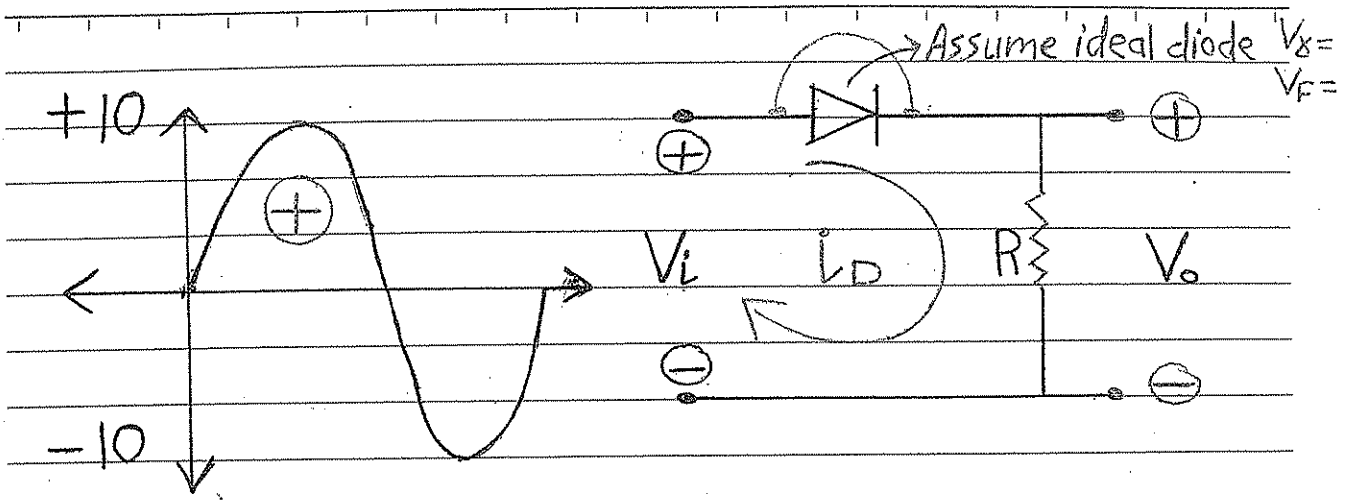
[Convert Half - Cycle of V_i into D.C]





$$V_2 = \frac{N_2}{N_1} V_1 = \frac{1}{10} (100 \sin \omega t)$$

$$= 10 \sin \omega t$$



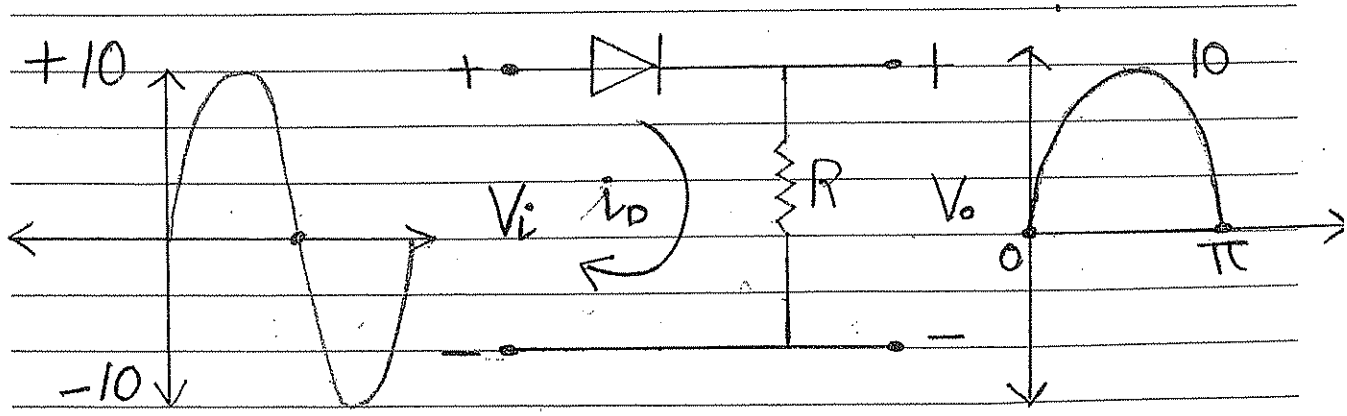
$$V_o = i_D \cdot R$$

$$-V_i + \cancel{V_D} + i_D \cdot R = 0 \quad ; V_D = 0 \text{ (F.w and ideal)}$$

$$i_D = \frac{V_i}{R} \rightarrow V_o = \frac{V_i}{R} \cdot R \rightarrow V_o = V_i$$

① During (+ve) H.C of V_i :

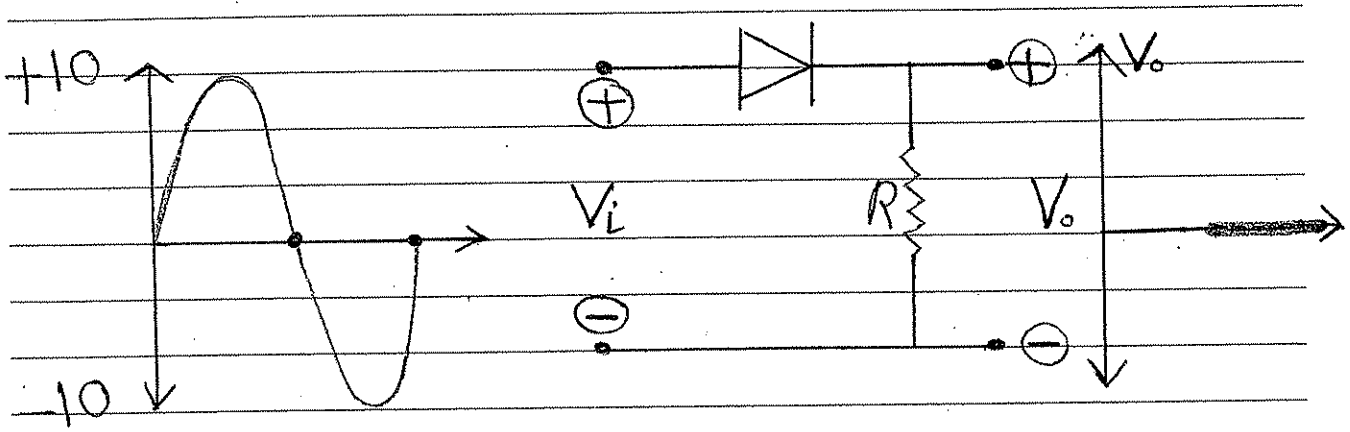
D → F.w ⇝ S.C , $V_D = 0$, $V_o = V_i$



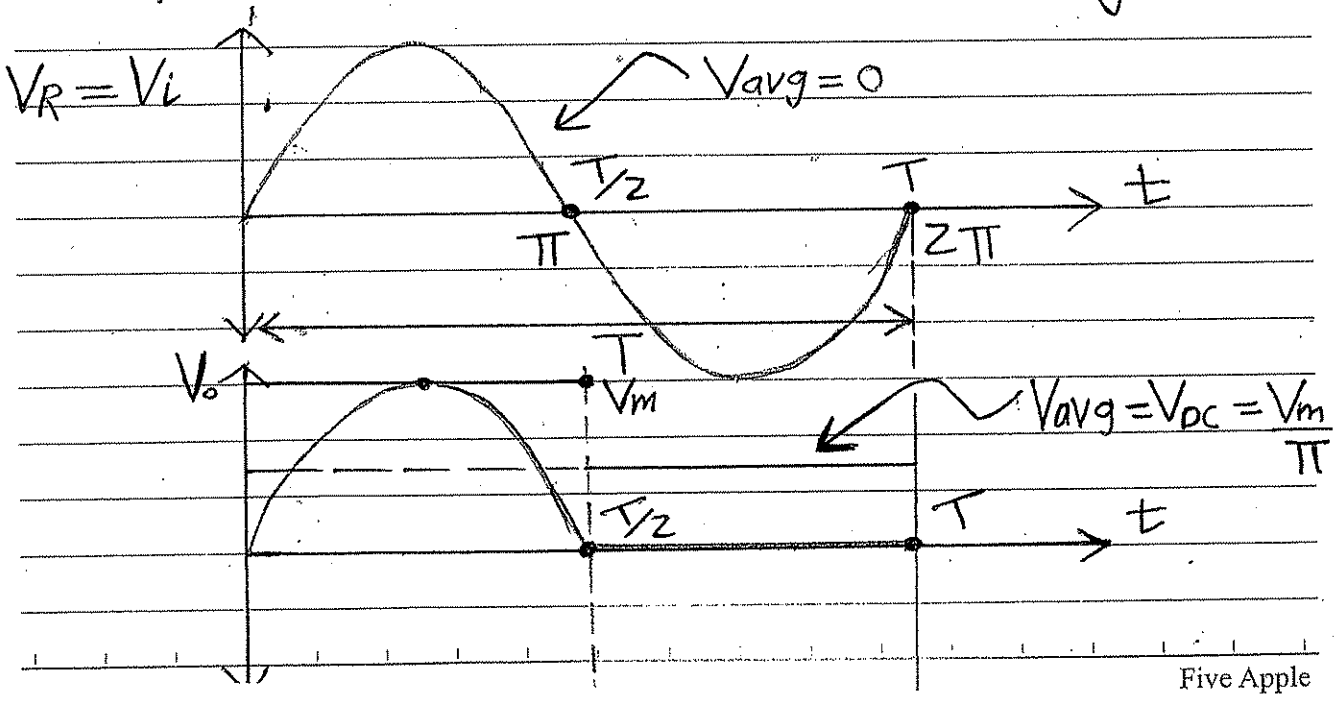
2) During (-ve) H.C of V_i :

D → Rev. ⇝ off ; $i_D = 0$, $V_o = 0$

$$\boxed{V_o = i_D R = 0}$$



3) For a complete cycle of V_i , the out put will be (+Ve) H.C only.



$$V_m = V_p - V_\gamma$$

Where :-

V_m = Peak output.

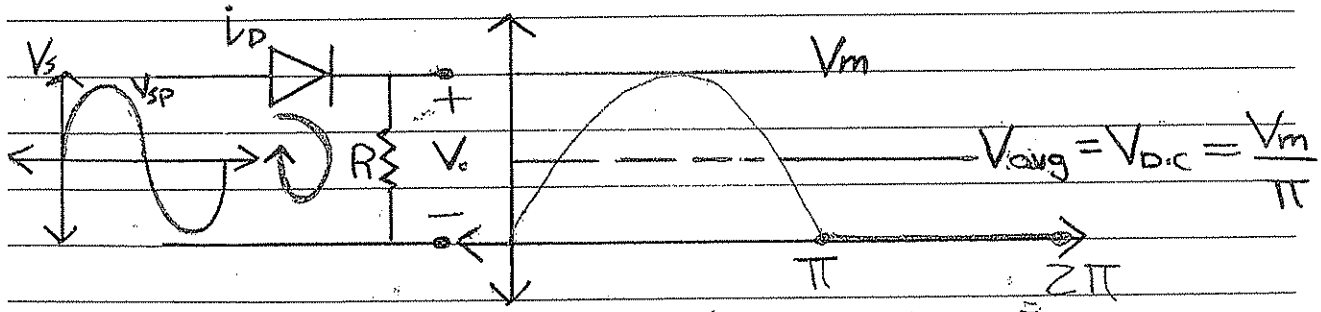
V_p = Peak Value of V_i.

For ideal diode $\rightarrow V_\gamma = 0$, $\boxed{V_m = V_p}$

$$* V_{avg} = \frac{1}{2\pi} \int_0^{2\pi} V(t) \, . \, dt$$

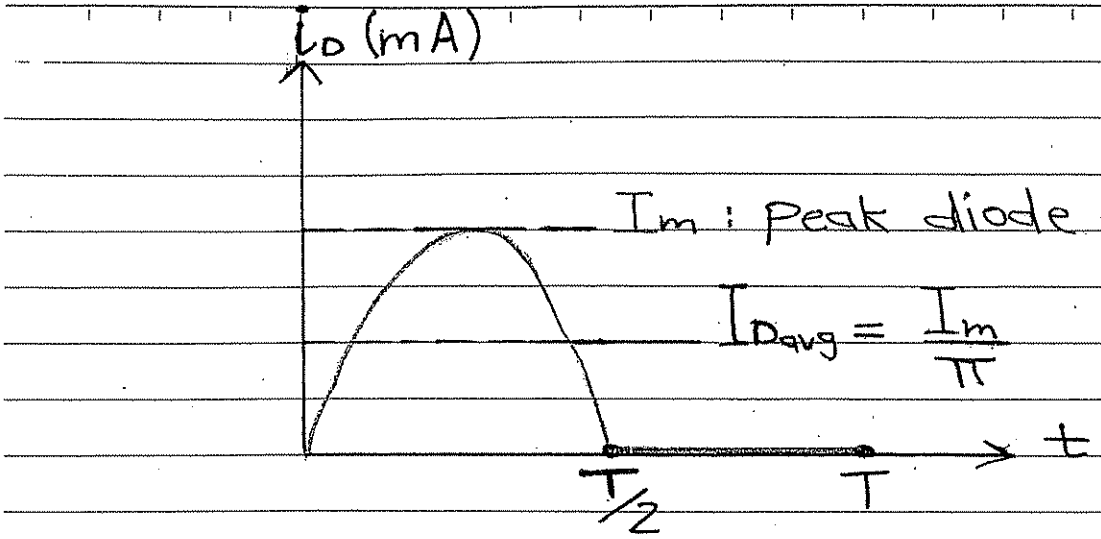
$$= \frac{1}{2\pi} \left[\int_0^{\pi} V_m \sin \omega t + \int_{\pi}^{2\pi} 0 \right]$$

$$= \frac{V_m}{\pi}$$

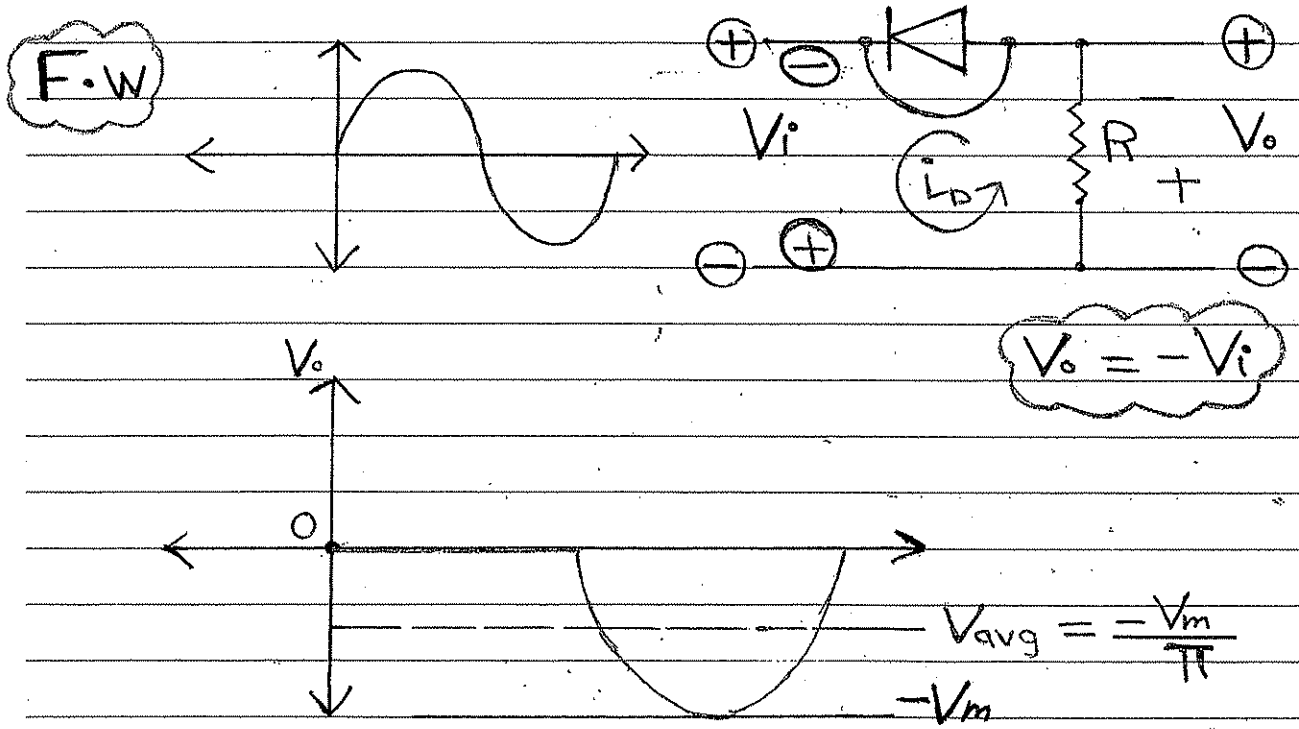


V_{sp} : Peak secondry Voltage.

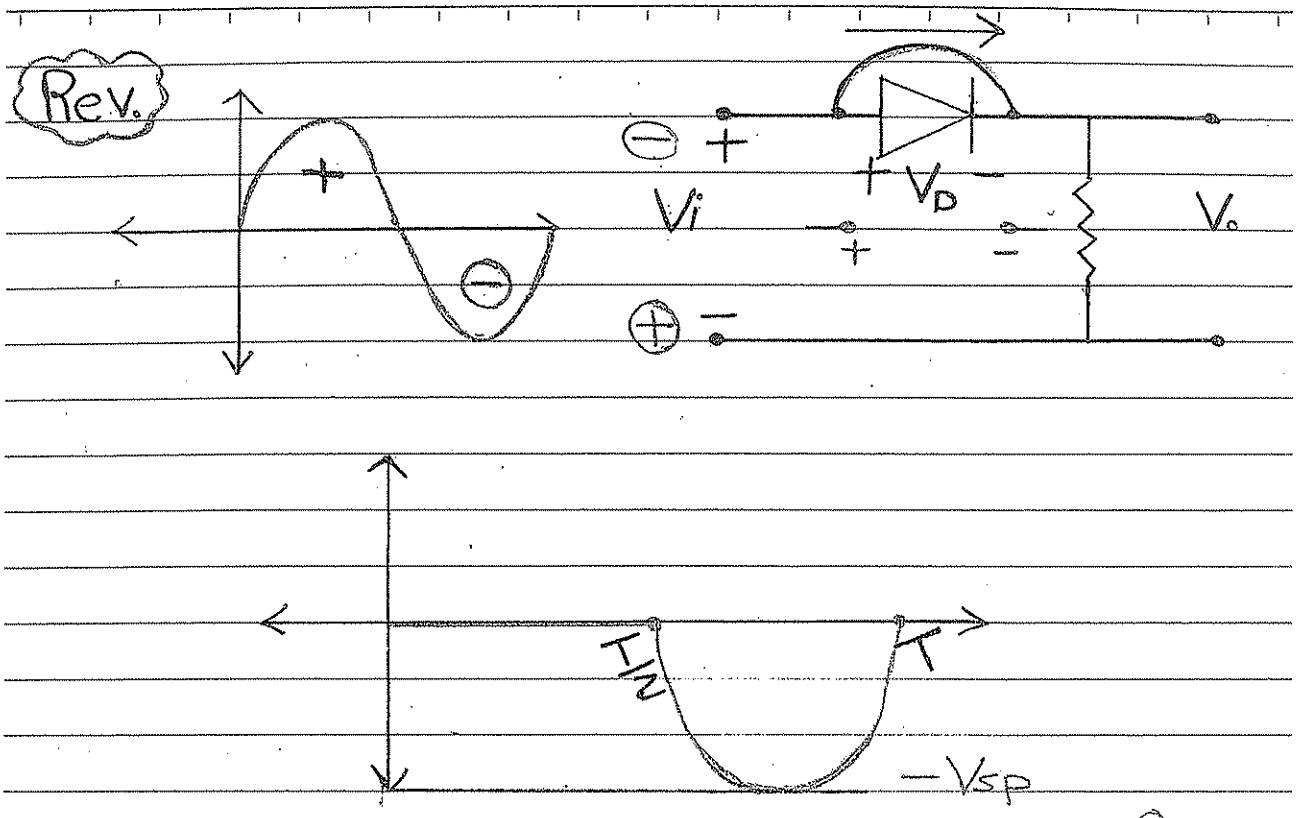
V_m : Peak output Voltage.



$$I_m = \frac{V_m}{R}$$



Five Angle



$$+V_{sp} + V_D + i_D R^{\nearrow 0} = 0$$

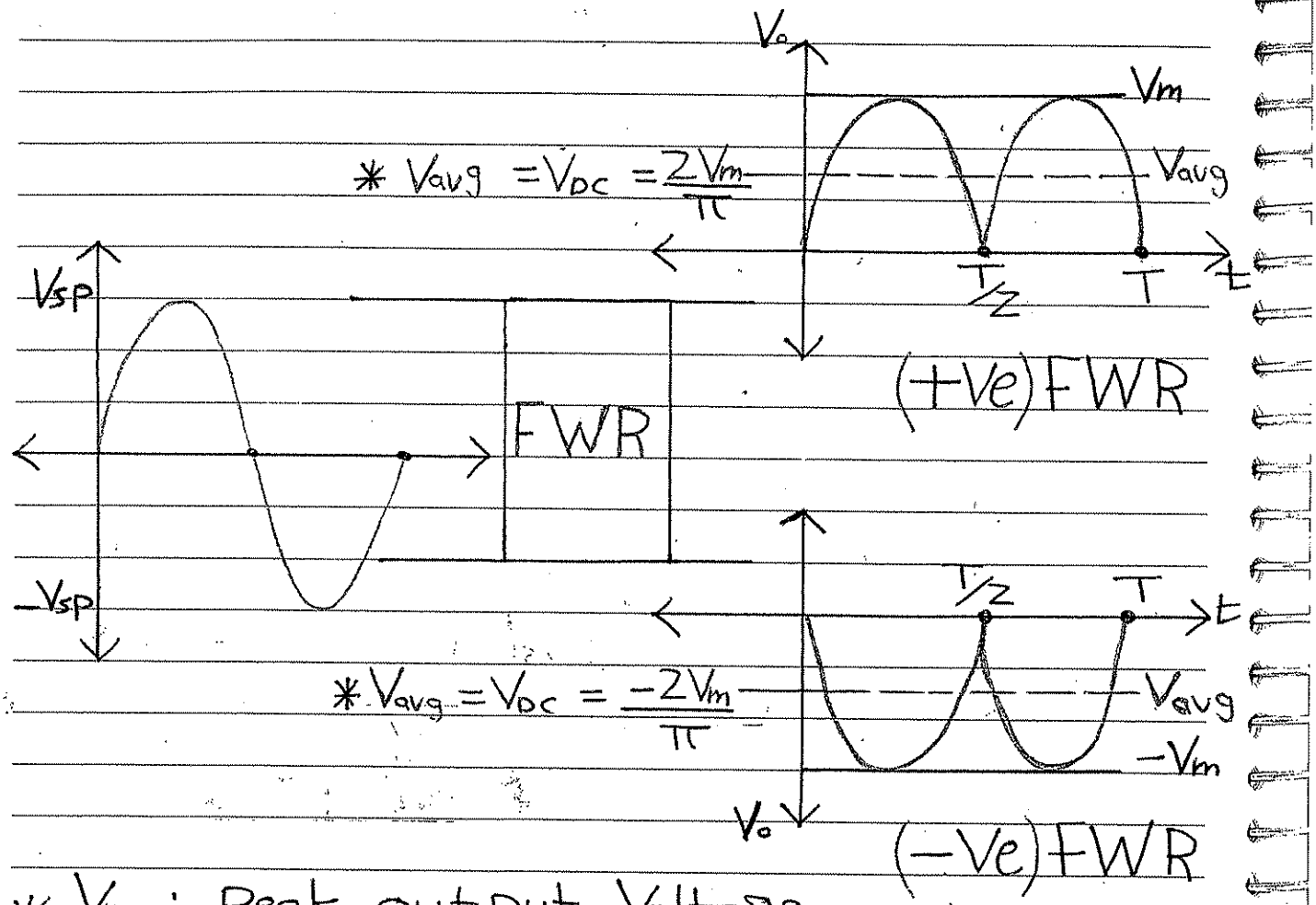
$$\boxed{V_D = -V_{sp}}$$

* PIV : (Peak Inverse Voltage)

: Max. Peak Voltage which the diode can hundle without break down.

In HWR : PIV for diode = V_{sp}

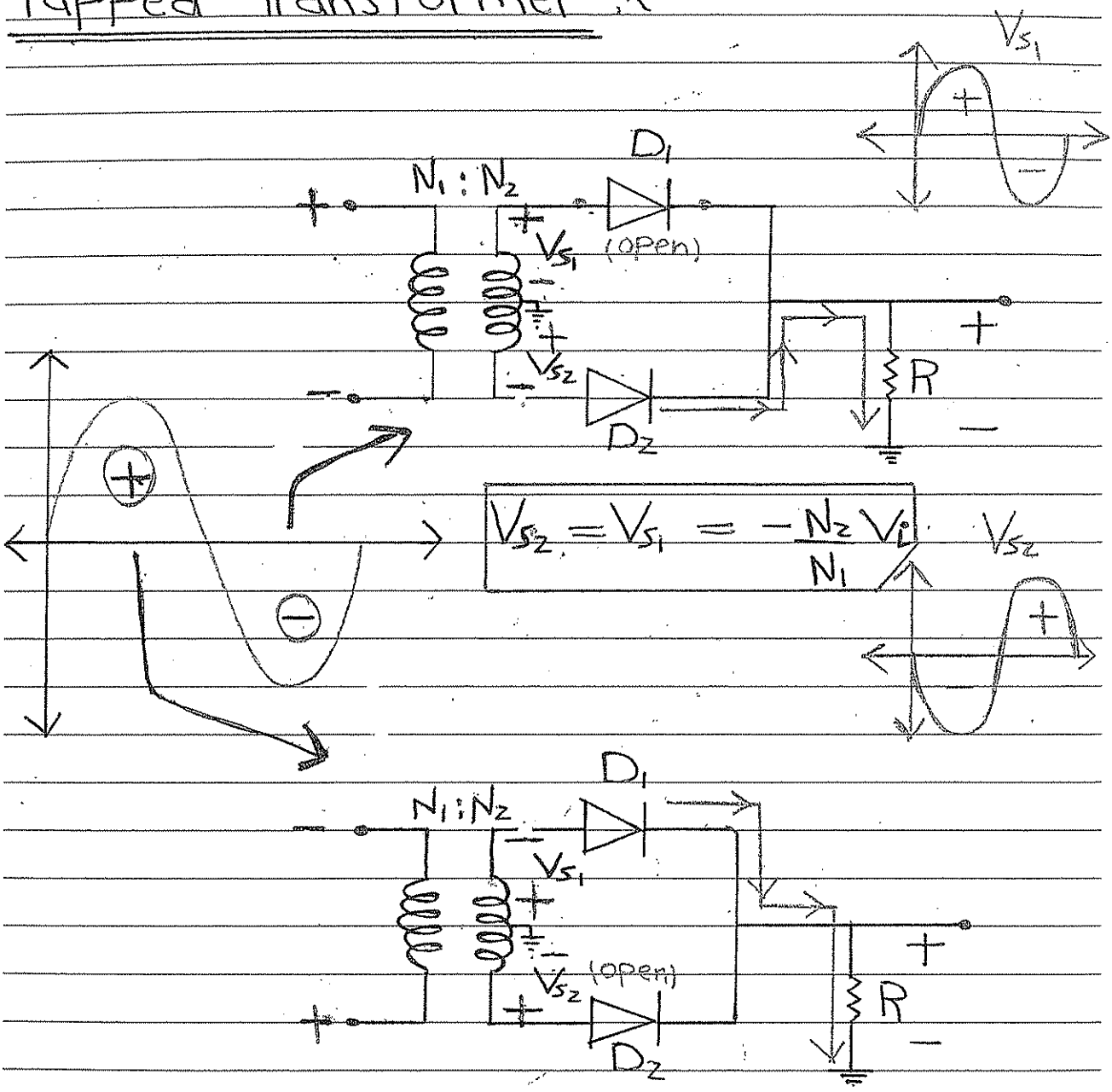
2) Full-Wave Rectifier (FWR):



* Vm : Peak output Voltage.

- 1) Full Wave Reactifier using Center tapped Transformer.
- 2) Full wave Bridge Rectifier.

1) Full Wave Rectifier Using Center Tapped Transformer :-

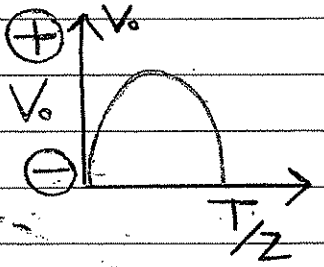


$V_m = V_{sp}$ (ideal)

$V_m = V_{sp} - V_\gamma$ (real)

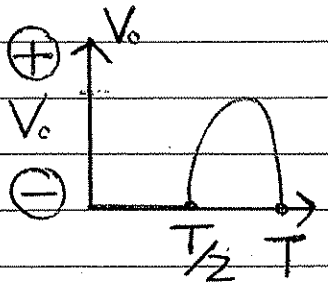
1) During (+Ve) H.C of V_i ;

* $V_{S_1} \rightarrow$ (+Ve) , $V_{S_2} \rightarrow$ (−Ve)
* D_1 : On / D_2 : off.
* i_{D_1} flows in (D_1) & (R) Causing V_o in the polarity Shown :



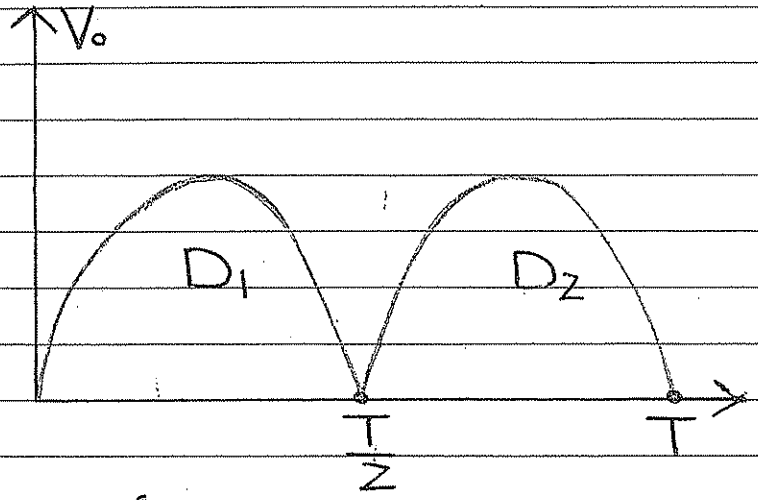
2) During (−Ve) H.C of V_i ;

* $V_{S_1} \rightarrow$ (−Ve) , $V_{S_2} \rightarrow$ (+Ve)
* D_1 : off / D_2 : On.
* i_{D_2} flows in D_2 & R causing V_o with Same ploarity as in (1).



3) For a Complete Cycle of V_i :-

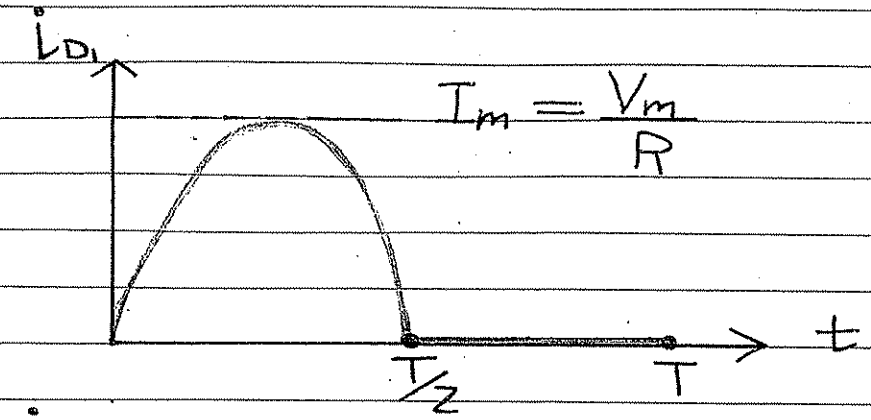
the Output will be full-Wave.

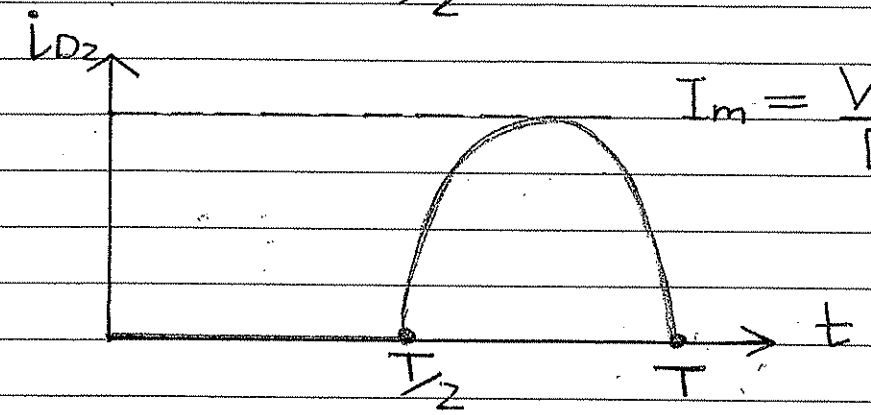


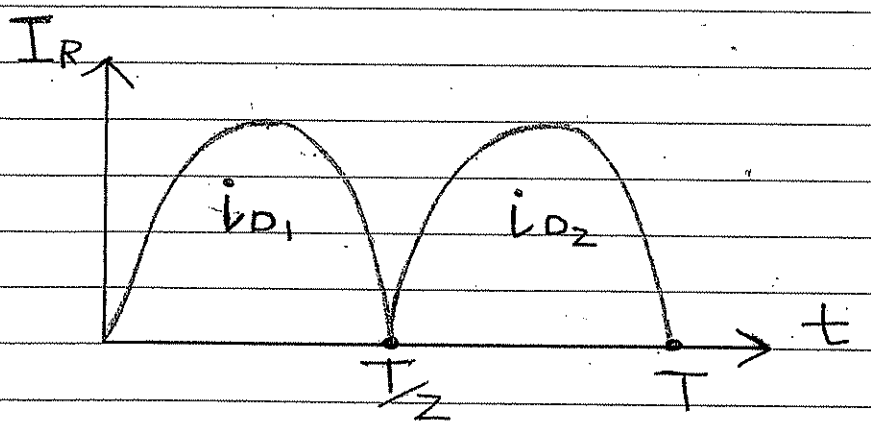
$$V_{avg} = \frac{1}{2\pi} \int V(t) \cdot dt$$

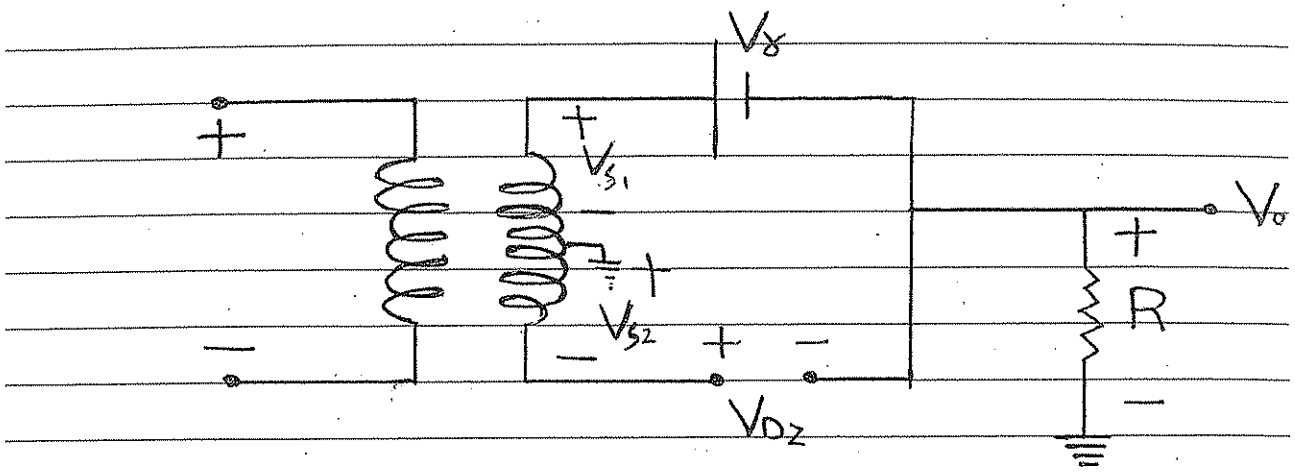
$$= \frac{1}{2\pi} \left[\int_0^{\pi} V_m \sin \omega t + \int_{\pi}^{2\pi} V_m \sin \omega t \right] . dt$$

$$= \frac{2 V_m}{\pi} \quad \#$$


i_{D_1}
$I_m = \frac{V_m}{R}$
$\frac{T}{2}$
T
t


i_{D_2}
$I_m = \frac{V_m}{R}$
$\frac{T}{2}$
T
t


I_R
i_{D_1}
i_{D_2}
$\frac{T}{2}$
T
t



During +Ve H.C :

$D_1 \rightarrow$ off & V_{DZ} ?

$\rightarrow V_{S2} + V_{DZ} + V_o = 0$

$D_1 \rightarrow$ on

$\rightarrow -V_{S1} + V_\gamma + V_o = 0$

$V_o = V_{S1} - V_\gamma$

and D_Z is off.

$V_{S2} + V_{DZ} + V_o = 0$

$V_{DZ} = -V_{S2} - V_o$

$= -V_{S2} - (V_{S1} - V_\gamma)$

$= -V_{S2} - V_{S1} + V_\gamma$

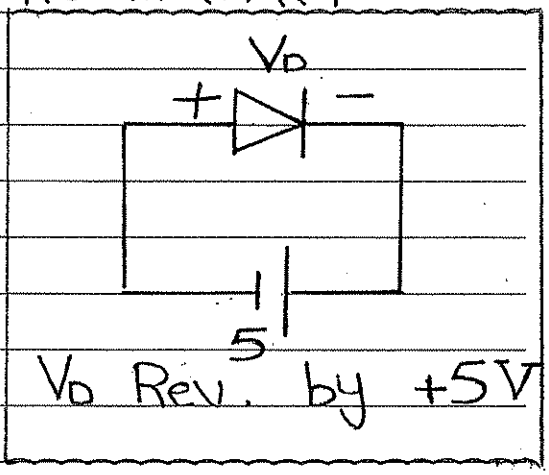
But: $|V_{s_1}| = |V_{s_2}|$:-

$V_{D_2} = -2V_s + V_\gamma$

$\therefore D_2$ is Rev. by $(2V_s - V_\gamma)$

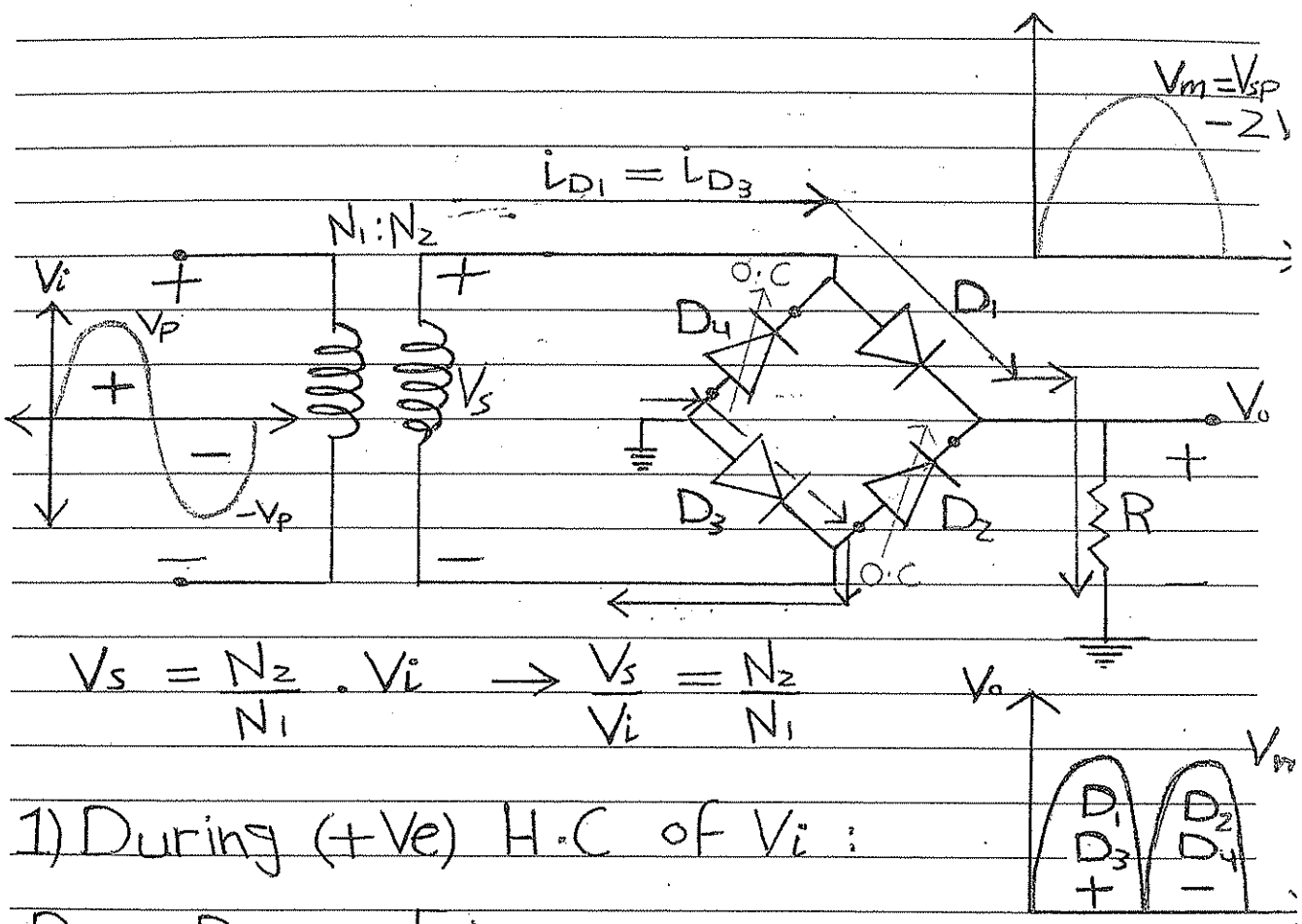
$\therefore \boxed{PIV = 2V_{sp} - V_\gamma}$

Recall that :-



V_D Rev. by +5V

2) Full Wave Bridge Rectifier :



$$V_s = \frac{N_2}{N_1} \cdot V_i \rightarrow \frac{V_s}{V_i} = \frac{N_2}{N_1}$$

1) During (+Ve) H.C of V_i :

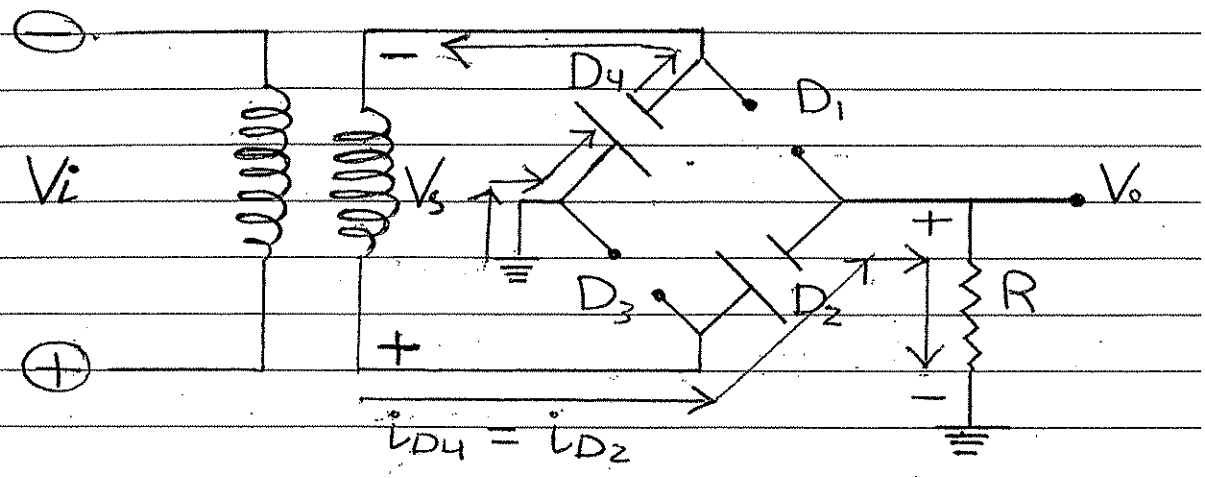
D_1 , D_3 → F.W → on .

D_2 , D_4 → Rev. → off

($i_{D1} = i_{D3} = i_D$) will flow in (R) causing V_o across (R) with Polarity $\left(\overset{+}{V_o}\overset{-}{}\right)$:

$$-V_s + V_{\gamma 1} + V_o + V_{\gamma 3} = 0 \rightarrow V_o = V_s - 2V_\gamma$$

$$\boxed{V_m = V_{sp} - 2V_\gamma}$$



2) During (-Ve) H.C of Vi :

D_1 , D_3 → Rev. → off.

D_2 , D_4 → F.W → on.

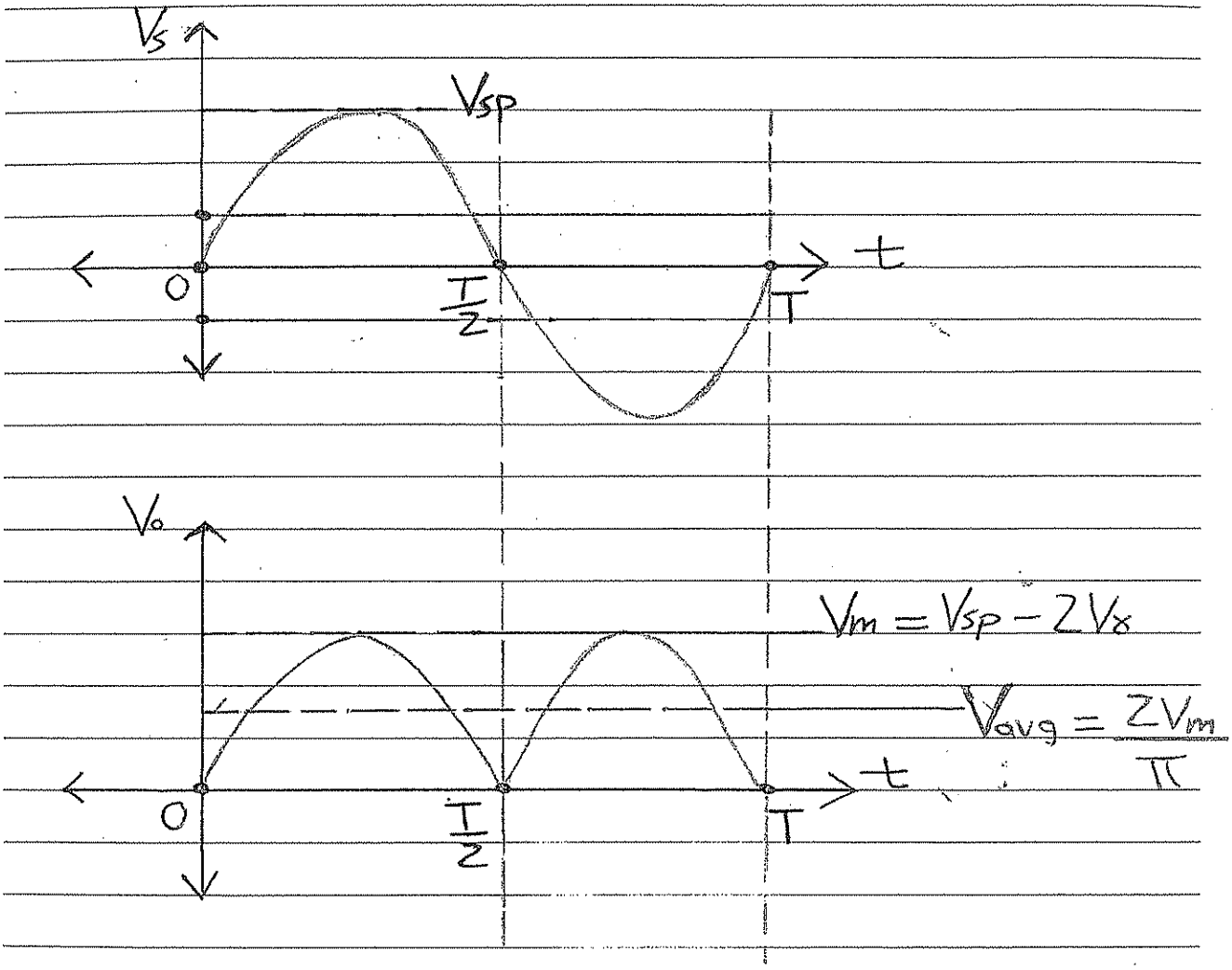
($i_{D_2} = i_{D_4} = i_D$) Will flow in (R)

Causing (V_o) with same polarity as in

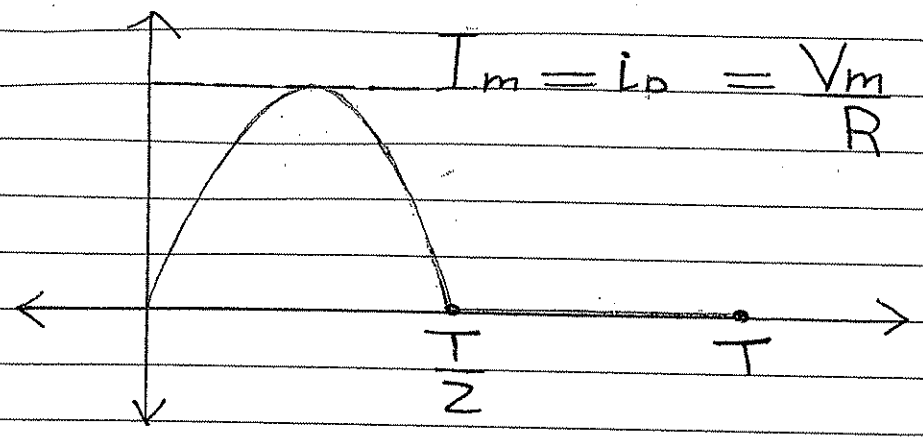
(1) : $\left(\begin{smallmatrix}+\\ V_o\\ -\end{smallmatrix}\right)$

3) For a Complete cycle of V_i :-

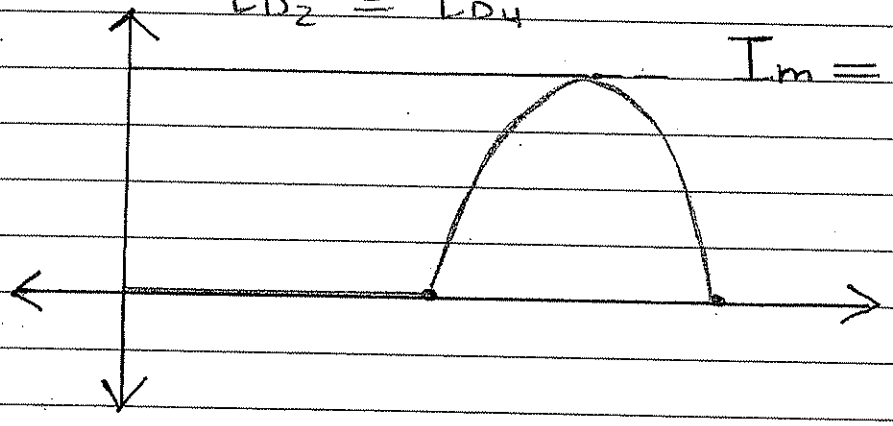
The (V_o) will be full-wave.

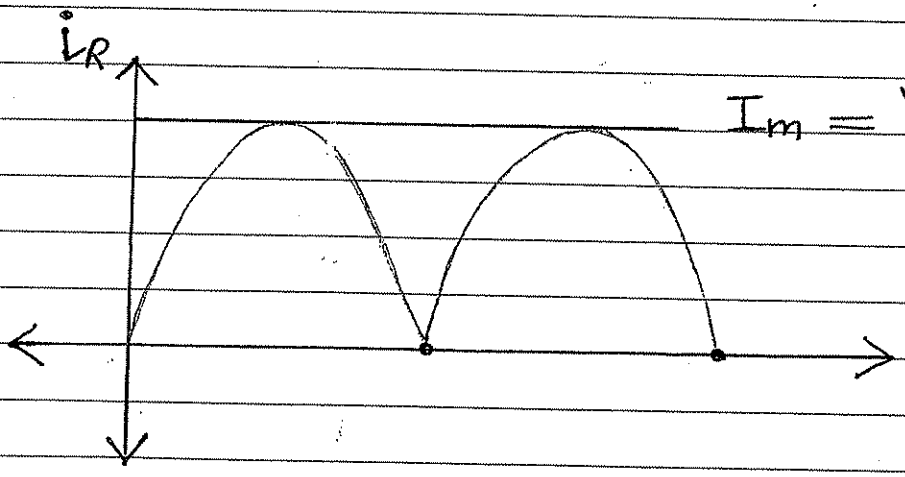


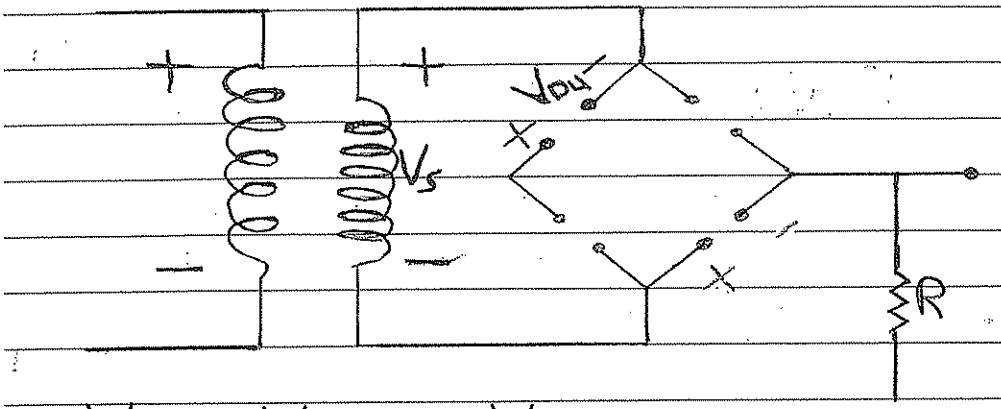
$i_{D_1} = i_{D_3}$



$i_{D_2} = i_{D_4}$



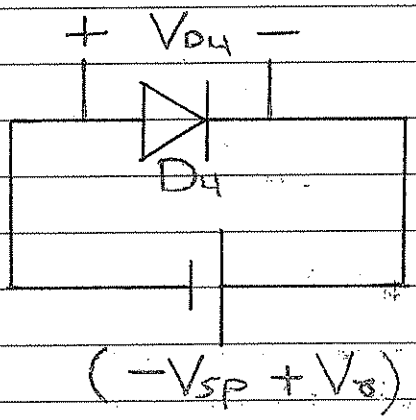




$$-V_s - V_{D4} + V_\gamma = 0$$

$$V_{D4} = -V_s + V_\gamma$$

$$\boxed{V_{D4(max.)} = -V_{sp} + V_\gamma}$$



D_4 is Reversed by $(V_{sp} - V_\gamma)$ &

PIV For diode in (FWBR) is

$\boxed{V_{sp} - V_\gamma}$.

EXA.:-

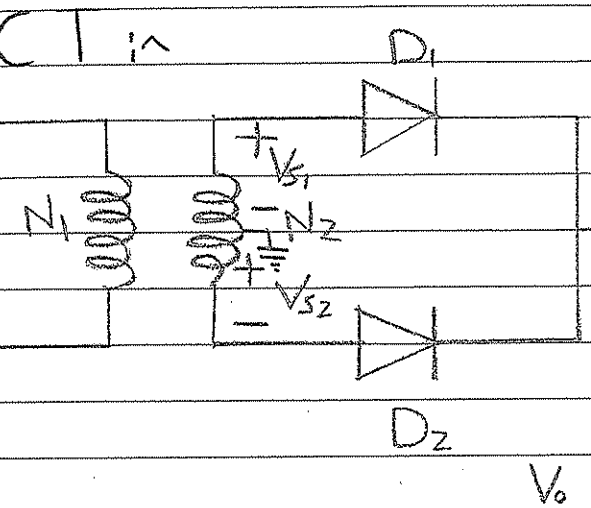
Design a **FWR** to produce a peak output Voltage ($V_m = 10\,V$) to 100-Ω load. The available input is $V_i = 120\,V_{rms}$; $F = 50\,Hz$. use Diode with $V_\gamma = 0.7\,V$.

1) Calculate turn-ratio $\frac{N_1}{N_2}$, Specify the riquired PIV rating of Diode, and max. diode current.

2) Draw the circuit diagram & output Voltage wave form. (Compare between [FWRCT] ; [FWBR] & comment.).

Sol. :-

Using CT :-

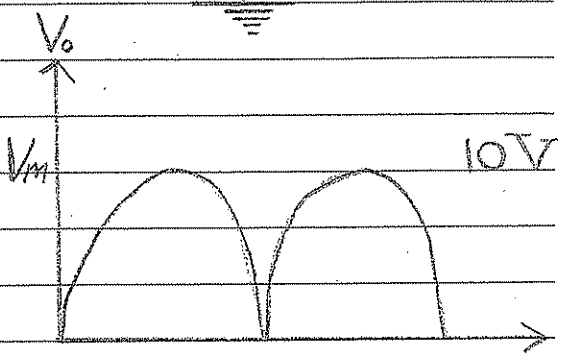


$$\frac{N_1}{N_2} = \frac{V_i}{V_s}$$

$$-V_{s_1} + V_\gamma + V_o = 0 \qquad (V_o = V_m)$$

$$V_{s_1} = V_m + V_\gamma$$

$$V_{s_1} = V_m + V_\gamma \rightarrow V_{s_1} = 10.7\ V.$$



$$V(t) = 5 \sin 2\pi * 50t$$

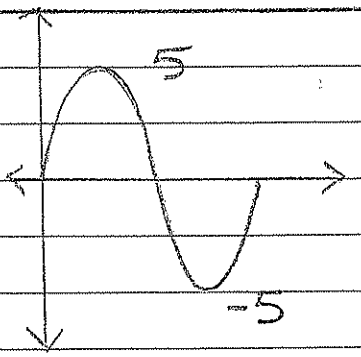
$$= V_p \sin \omega t$$

$$V_{rms} = \frac{V_p}{\sqrt{2}} = 5 * 0.702$$

$$= 3.5V.$$

$$f = 50\ Hz.$$

$$V_p = V_{rms} \cdot \sqrt{2}$$



$V_{s,p} = 10.7\ V.$

$V_{ip} = 120 * \sqrt{2}$

$\frac{N_1}{N_2} = \frac{V_{ip}}{V_{s,p}} \Rightarrow \frac{120\sqrt{2}}{10.7} = \frac{170}{10.7}$

$= 16$

$PIV = 2V_{sp} - V_\gamma$

$= 2 * 10.7 - 0.7$

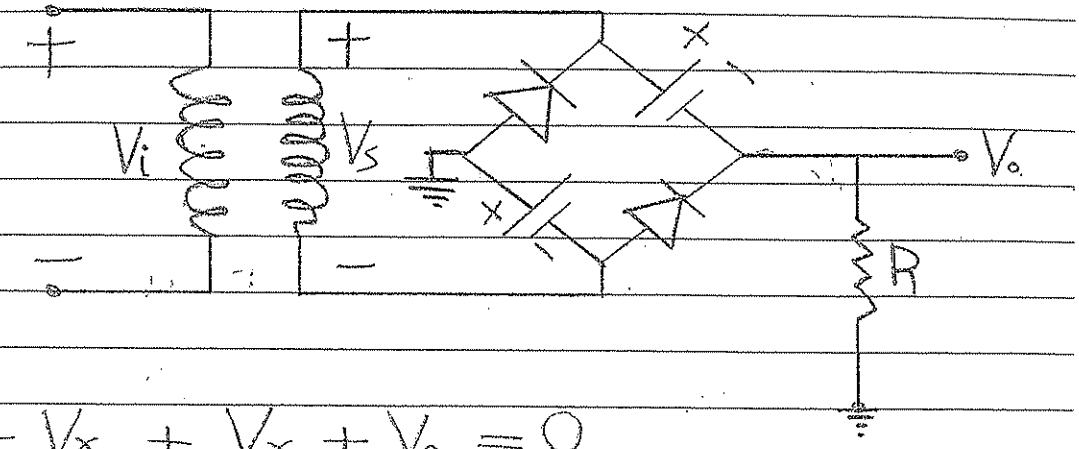
$= 20.7\ V$

$i_{op} = I_m = \frac{V_m}{R} = \frac{10V}{100\Omega} = 100\ mA.$

* $P_{D(diode)} = I_{Davg} \cdot V_\gamma$

* $I_{Davg} = \frac{I_m}{\pi}$ ✓ (half-wave)

Using FWBR :-



$$-V_s + V_\gamma + V_\gamma + V_o = 0$$

$$V_s = V_o + 2V_\gamma$$

$$V_{sp} = V_m + 2V_\gamma$$

$$= 10 + 2 * 0.7$$

$$= 11.4\ V$$

$$\frac{N_1}{N_2} = \frac{V_i}{V_s} = \frac{V_{i(rms)}}{V_{s(rms)}}$$

$$V_{s(rms)} = \frac{V_{sp}}{\sqrt{2}} = 11.4 * 0.707 = 8.2\ V.$$

$$\frac{N_1}{N_2} = \frac{120}{8.2} = 15$$

$PIV = V_{sp} - V_{\gamma}$

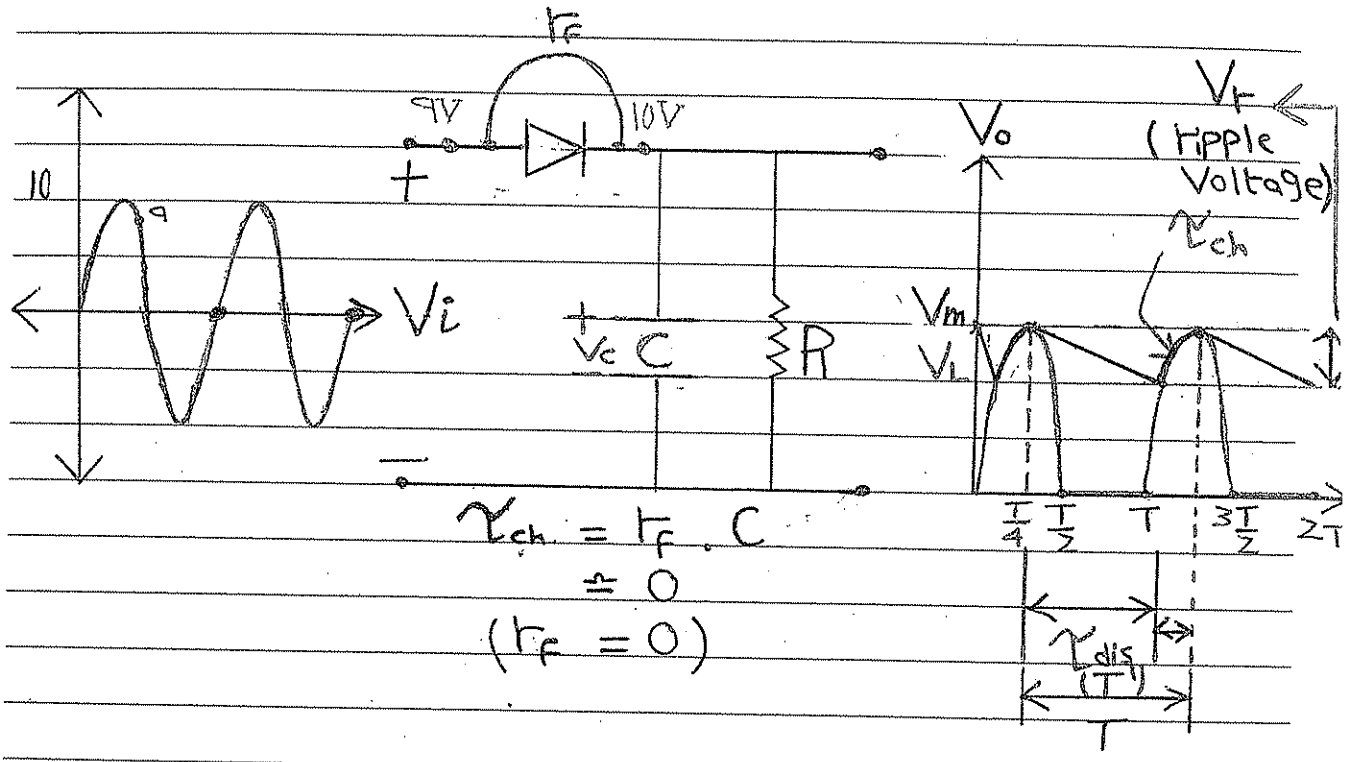
$= 11.4 - 0.7 = 10.7\ V$

Comment:-

	(C.T type)	(Bridge type)
PIV :	(20.7)	(10.7)
	(Two Second)	(one Second)
	(C.T is required)	(C.T not nessecary)
No. of diodes	(2)	(4)

* (C.T) أفضل من (Bridge) في الـ (PIV).
* (Bridge) أفضل من (C.T) في (N).

3) Filter and ripple Voltage :-



$\tau_{ch} = r_f \cdot C$

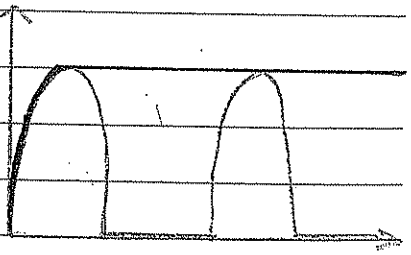
$\doteq 0$

$(r_f = 0)$

$\tau_{dis} = R \cdot C$

$T = \frac{1}{f}$

* Without (R) →



$V_r = V_m - V_L$

* During discharge time :-

$V_c(t) = V_m e^{-t/RC}$

→ at $t = T'$;

$V_c(t) = V_L$

$V_L = V_m e^{-\frac{T}{RC}}$

$\therefore V_r = V_m - V_m e^{-\frac{T}{RC}}$

$= V_m (1 - e^{-\frac{T}{RC}})$

$e^{-x} = 1 - x$ (For Small X)

Practically T' is required tobe Very Small.

$\therefore e^{-\frac{T'}{RC}} \approx 1 - \frac{T'}{RC}$

$\rightarrow V_r = V_m (1 - 1 + \frac{T'}{RC})$

$V_r = \frac{V_m T'}{RC}$

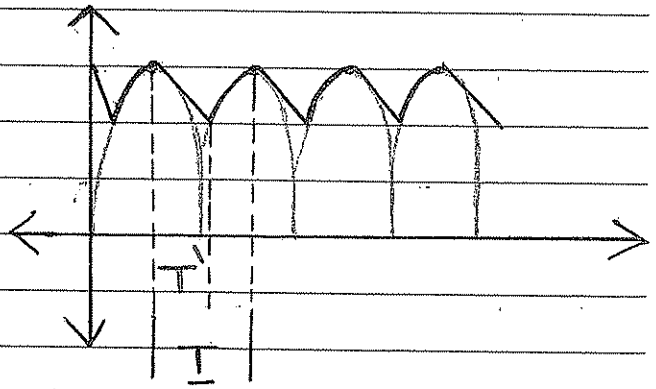
But - ($T' \approx T$) {for half Wave Rec.}

* $T' = \frac{1}{f}$

∴ $\boxed{V_r = \frac{V_m}{fRC}}$ For HWR.

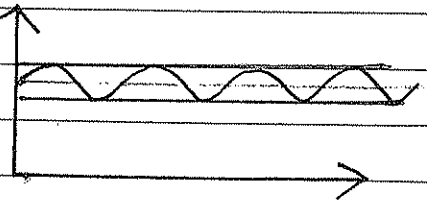
ALSO; For Full Wave Rec. :-

$T' \approx \frac{T}{2} = \frac{1}{2f}$

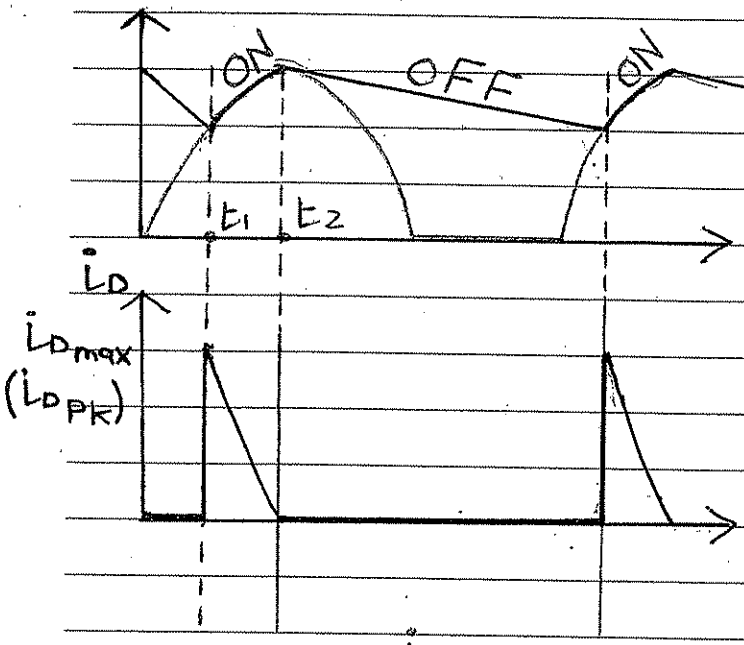


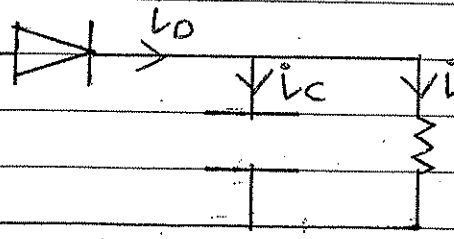
∴ $\boxed{V_r = \frac{V_m}{2fRC}}$ For FWR.

* $\left[V_{r(F)} = \frac{1}{2} V_{r(H)}\right]$ and $\left[C_{(F)} = \frac{1}{2} C_H\right]$

*  ↕ V_r : peak-to-peak ripple voltage.

Filter : Simply a capacitor Connected in parallel with (R) used to transform pulsating D.C (⎍) in to Semi pure D.C (⎍⎍⎍).





$$i_D = i_R + i_c = \frac{V_c}{R} + C\frac{dV_c}{dt}$$

* We cant increase the value of (C) indefintly the limiting factor is Choosing © is the max. Diode current.

$$i_{D_{max}} = i_{D_{Peak}} = \frac{V_m}{R}\left[1 + \pi\sqrt{\frac{2V_m}{V_r}}\right]$$

EXA. Design a FWBR with filter with the following Specification:-

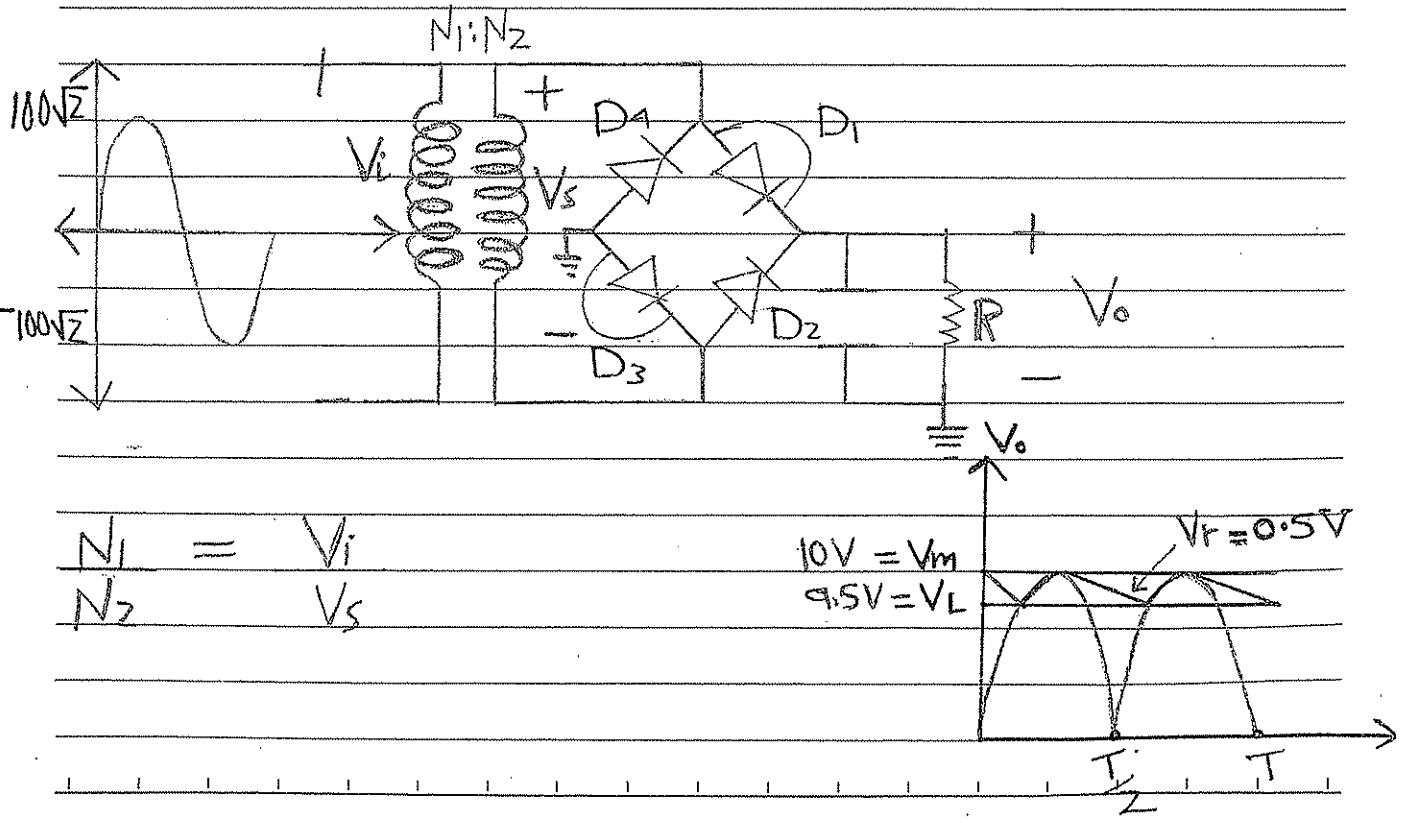
$V_m = 10V$; $I_m = 100\ mA$.

$V_r = 0.05\ V_m$ (must NOT exceed 5%).

The available $V_i = 100\ V_{rms}$, $f = 50\ Hz$ and use (Si) diode with $V_\gamma = 0.7\ V$.

($\frac{N_1}{N_2}$?, R, C, PIV, $i_{D_{max}}$) ?

[given : $i_{D_{max}} = \frac{V_m}{R}\left[1 + \pi\sqrt{\frac{2V_m}{V_r}}\right]$.]



$\frac{N_1}{N_2} = \frac{V_i}{V_s}$

$V_o = V_s - 2V_\gamma$

$V_m = V_{sp} - 2V_\gamma$

$V_{sp} = V_m + (2 * 0.7) = 11.4\ V.$

$\rightarrow \frac{N_1}{N_2} = \frac{100\sqrt{2}}{11.4} = \frac{141.4}{11.4} = 13$

$R = \frac{V_m}{I_m} = \frac{10}{100\ m} = 0.1\ K\Omega = 100\ \Omega.$

$V_r = 0.05\ V_m = 0.5\ V.$

$V_r = \frac{V_m}{2fRC}$

$C = \frac{V_m}{2fRV_r} = \frac{10}{2 * 50 * 100 * 0.5}$

$= \frac{10}{500} = 0.002\ F$

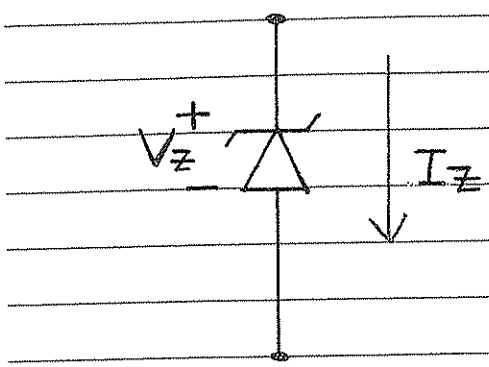
$= 2000\ \mu F.$

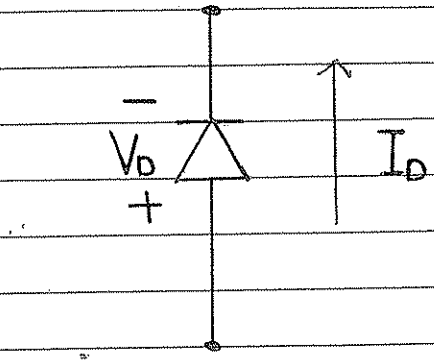
$PIV = V_{sp} - V_\gamma = 11.4 - 0.7 = 10.7\ V.$

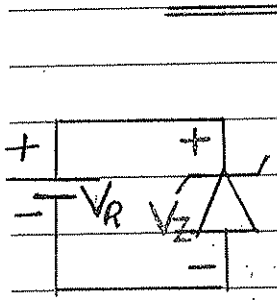
$I_{D_{max}} = \frac{10\ V}{100\ \Omega}\left(1 + \pi\sqrt{\frac{20}{0.5}}\right) = 0.1\left[1 + \pi\sqrt{40}\right]$

$= 2.1\ A.$

* Zener Diode and Voltage Regulator :

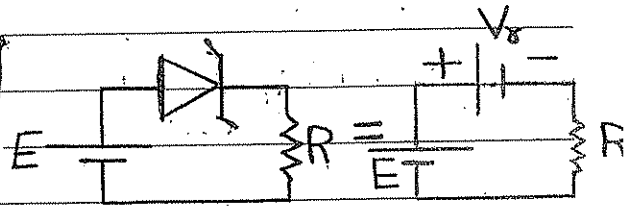






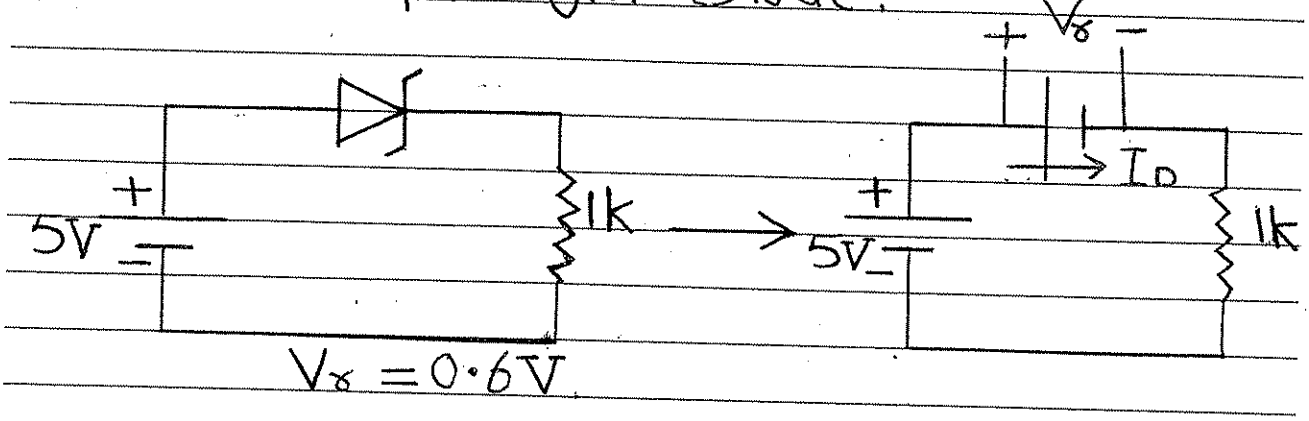
$I_Z = 0$

$(V_Z = V_R)$:

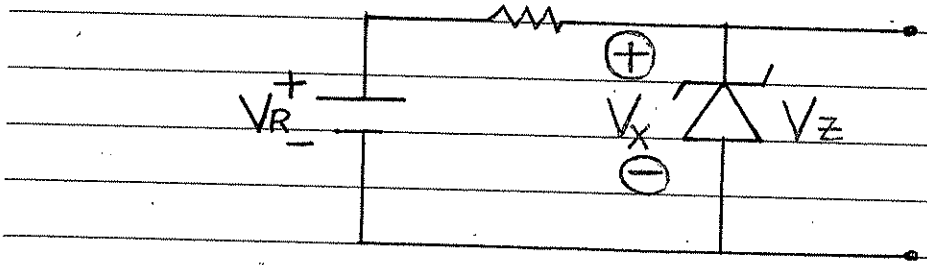


$(V_Z = 6V)$

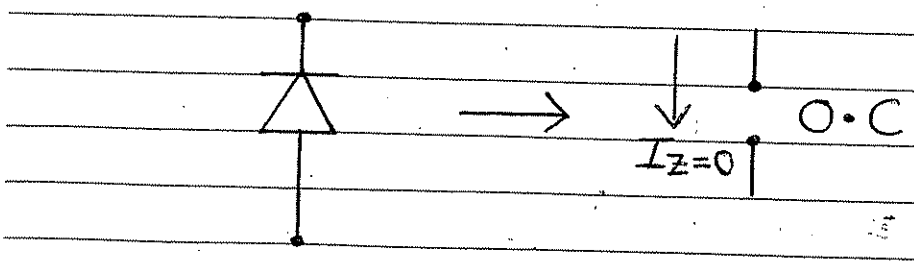
1] In (F.W) biasing :- Z-D is similar to normal PN Jn. Diode.



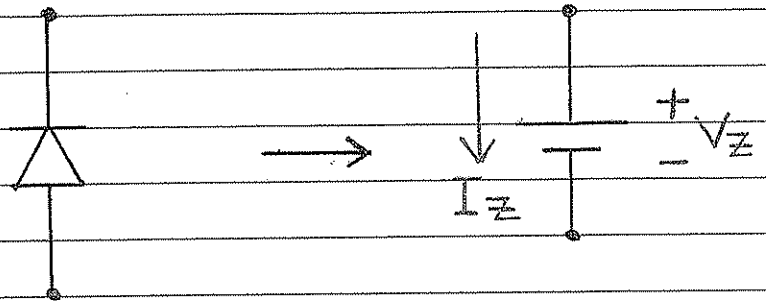
2] In (Rev.) biasing :-



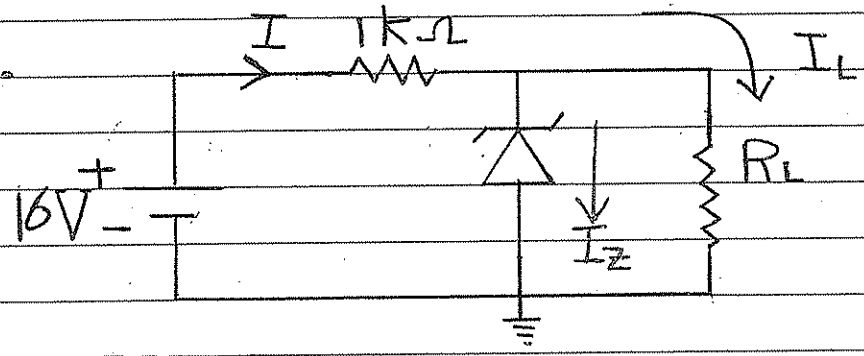
(i) When ($V_x < V_z$) ; Z-D is OFF.



(ii) If ($V_x \geq V_z$) ; Z-D will behave as a fixed Voltage Source of Value (V_z) and Variable Current (I_z).



EXA.



$V_z = 10\,V$

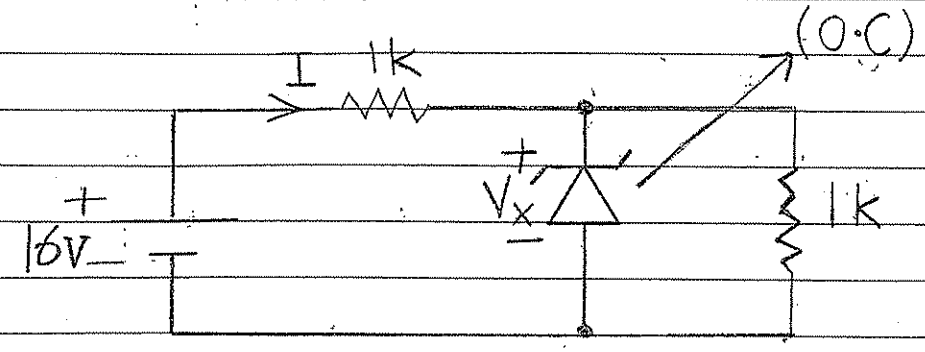
$P_{z_{max}} = 40\,mW$

find : I, I_L, I_z, P_z, V_L

When :- (i) $R_L = 1k\Omega$.

(ii) $R_L = 3k\Omega$.

(i) $R_L = 1k\Omega$.



disconnect Z-D : Assume Z-D is (0·C)

$$V_x = \frac{16 * R_L}{R_L + R_S} = \frac{16 * 1}{1+1} = 8V.$$

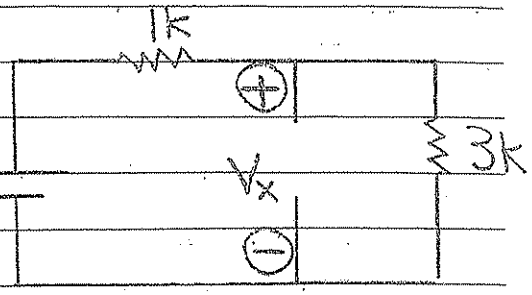
Since $V_x < V_z$ ∴ Z-D is off.

→ $I_z = 0$; $V_L = V_x = 8V$.

$$I = \frac{16}{1+1} = 8mA.$$

$$P_z = I_z V_z = 0$$.

(ii).

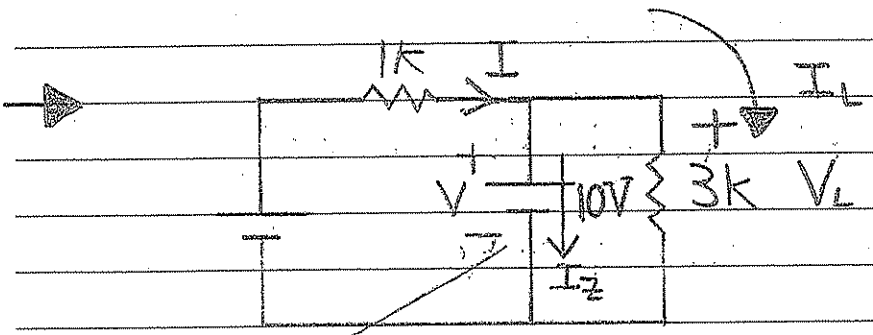


$V_x = \frac{16 * 3}{1+3} = 12V$

Since $V_x > V_z$;-

∴ Z-D is ON.

١) يشتغل بحالة الـ Rev.
٢) والفولتية الماسلطة عليه أكبر من V_z



* يتصرف كبطارية قيمتها (V_z).

$I_L = \frac{V_L}{R_L} = \frac{V_z}{3} = \frac{10}{3} = 3.33\ mA.$

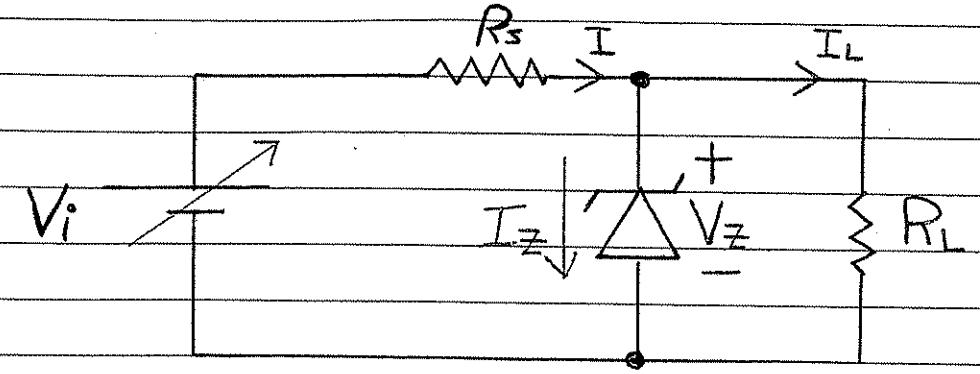
$I \Rightarrow -16 + I * R_s + V_z = 0$

$I = 16 - 10 = 6mA.$

$I_z = I - I_L = 6 - 3.33 = 2.67\ mA.$

$P_z = I_z * V_z = 2.67 * 10 = 26.7\ mW.$

* (Z - D) as a Voltage Regulator :-

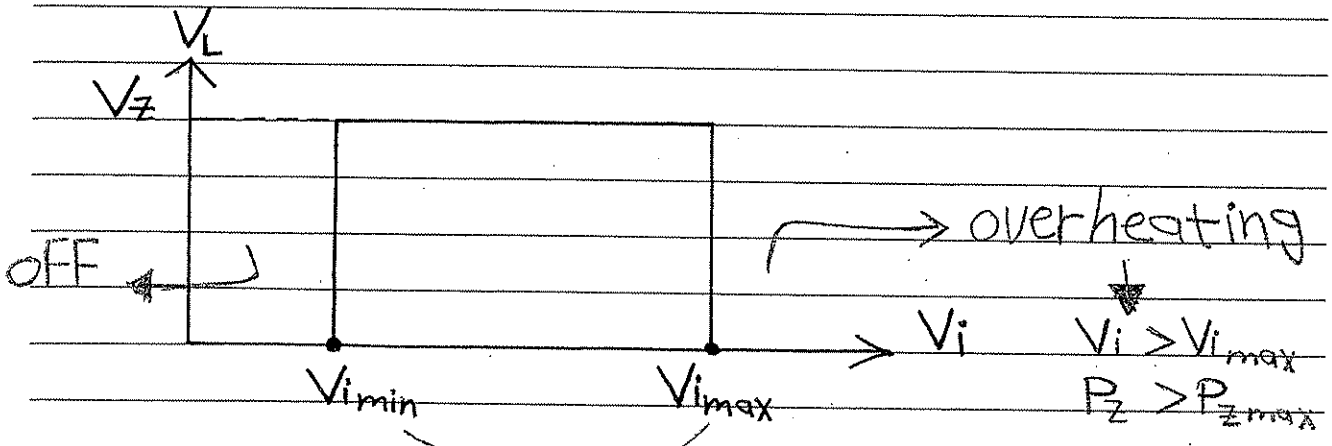


1) Rev. 2) $V_A \geq V_Z$

When (Z-D) is (ON) ;

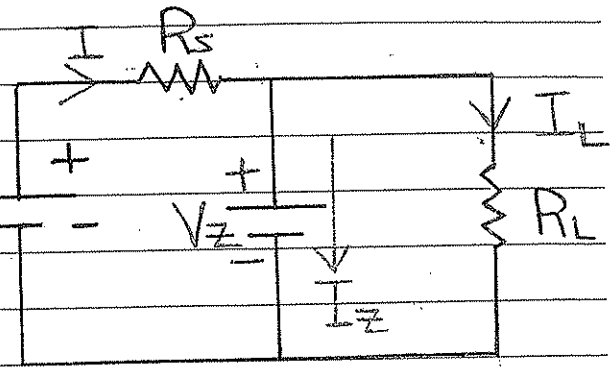
it will maintain a certain Voltage (V_Z) across the Load and protect the Load in the following Cases :-

1) Fixed (R_L) and Variable (V_i) :



• تعتمد على مواصفات الـ (Z).

* When (Z-D) is (ON) ; the following relation is correct :-



1) $I = I_Z + I_L$. ✓

2) $I_L = \frac{V_Z}{R_L}$. ✓

3) $I = \frac{V_i - V_Z}{R_S}$. ✓

4) $V_i = I \cdot R_S + V_Z$. ✓

* if $V_i \uparrow$ then $I \uparrow$; but I_L is fixed ; So I_Z must increase ($I_Z \uparrow$) .

* if $V_i \downarrow$ then $I \downarrow$; but I_L is fixed ; So I_Z must decrease ($I_Z \downarrow$) .

→ Calculate (V_{imin}) and (V_{imax}) :-

(Range of V_i over which Z-D is ON and Regulate) :-

Given : V_Z ; I_{Zmin} ; I_{Zmax} or P_{Zmax}.

Note : In General : $\boxed{P_{Zmax} = I_{Zmax} \cdot V_Z}$

* V_{imin} :-

$$V_i = I \cdot R_S + V_Z$$

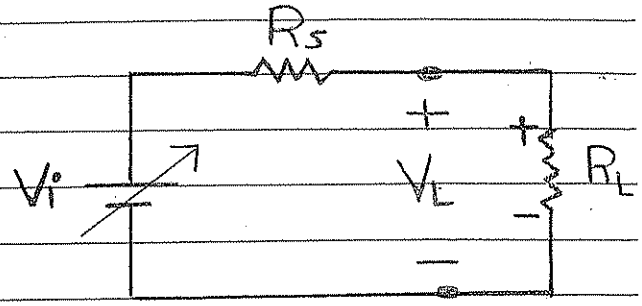
$$V_{imin} = I_{min} \cdot R_S + V_Z$$

$$= (I_Z + I_L) R_S + V_Z$$

$$\therefore V_{Imin} = (I_{Zmin} + I_L) R_S + V_Z$$

Where : $I_L = \frac{V_Z}{R_L}$.

For $I_{Zmin} = 0 \rightarrow V_{imin} = I_L R_S + V_Z$



When Z-D is oFF :

$I_Z = 0 = I_{Z\,min}$

$$V_L = \frac{V_i \cdot R_L}{R_L + R_S}$$

When $V_L = V_Z$; Z-D will be ON .

The value of V_i which makes $V_L = V_Z$ is V_{imin} ;

Then ; $V_L = V_Z = \frac{V_{imin} \cdot R_L}{R_L + R_S}$

$$\therefore \quad V_{imin} = \frac{R_L + R_S}{R_L} \cdot V_Z$$

* V_{imax} :-

$$V_i = I \cdot R_s + V_z$$

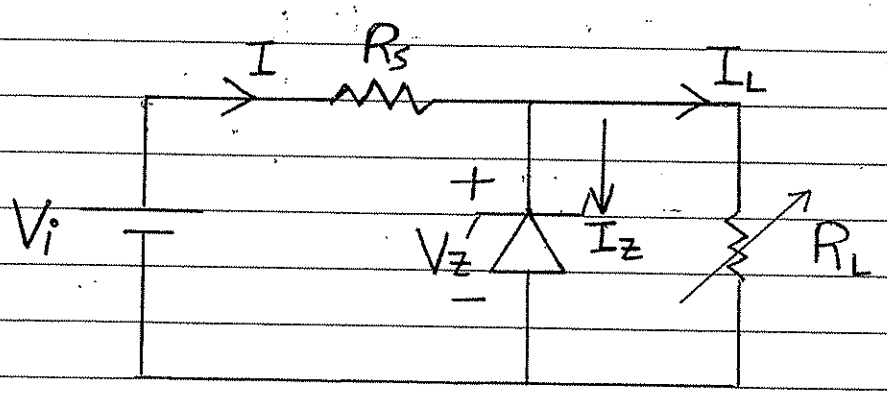
$$V_{imax} = I_{max} \cdot R_s + V_z$$

$$= (I_z + I_L) R_s + V_z$$

$$\therefore V_{imax} = (I_{zmax} + I_L) R_s + V_z$$

Where : $I_L = \frac{V_z}{R_L}$

2) Fixed (V_i) and Variable (R_L) :-



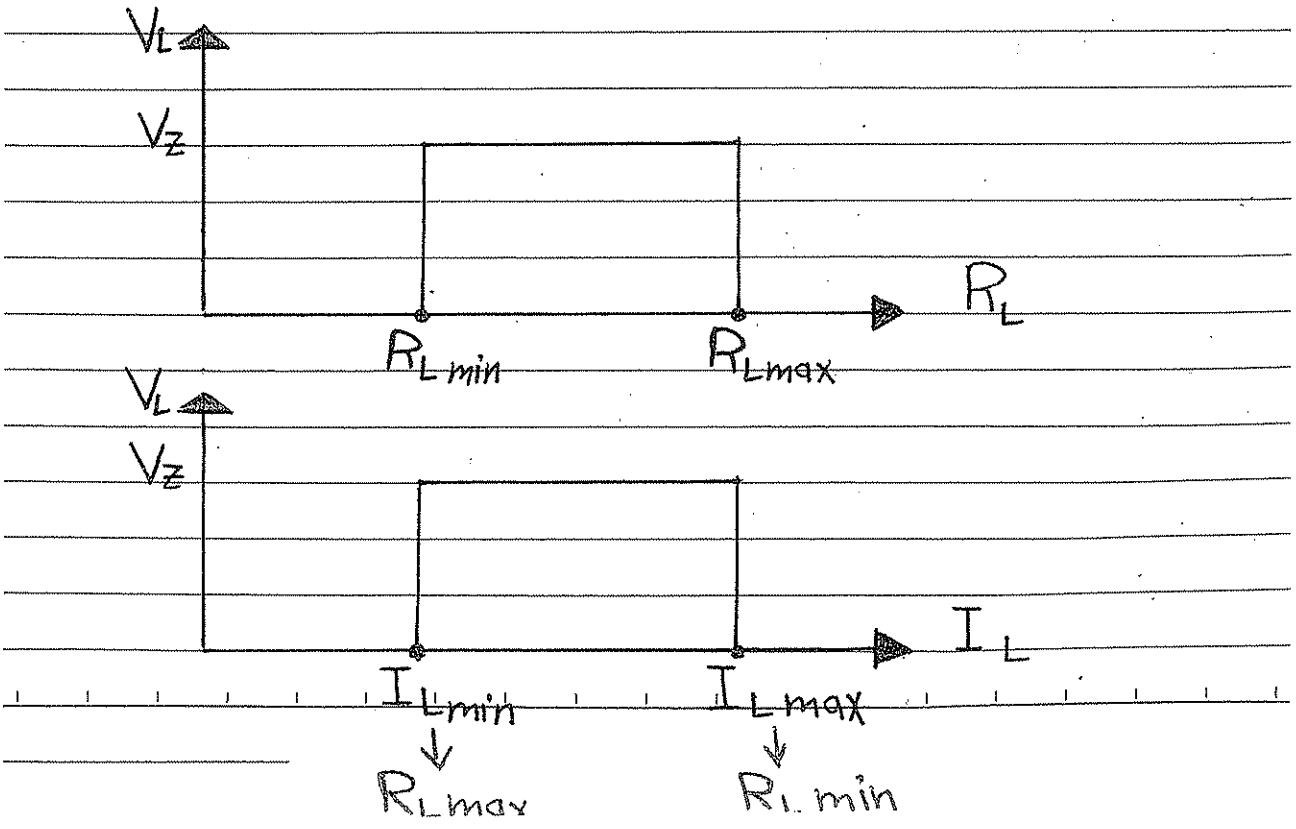
When Z-D is ON :

$I = I_z + I_L$; Where : $I_L = \frac{V_z}{R_L}$

$\rightarrow I = \frac{V_i - V_z}{R_s}$

1) When $R_L \downarrow$, then $I_L \uparrow$; but I is fixed, So I_z must decrease ($I_z \downarrow$) to compensate.

2) When $R_L \uparrow$, then $I_L \downarrow$; but I is fixed, So I_z must increase ($I_z \uparrow$) to compensate.



→ Calculate ($R_{L\,min}$) and ($R_{L\,max}$) ; (Range of R_L) :-

Given : V_Z , $I_{Z\,min}$, $I_{Z\,max}$, R_S , V_i

When Z-D is ON :- $R_L = \frac{V_Z}{I_L}$

* $\boxed{R_{L\,min} = \frac{V_Z}{I_{L\,max}}}$

* $I = I_{Z\,min} + I_{L\,max}$

→ $I = \frac{V_i - V_Z}{R_S}$; can be calculated.

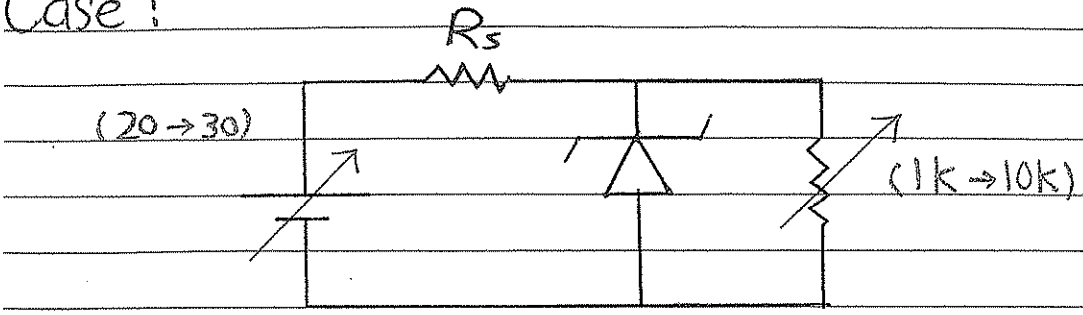
→ $\boxed{I_{L\,max} = I - I_{Z\,min}}$ (I : can be calculated, $I_{Z\,min}$: given)

Then :

$\boxed{R_{L\,max} = \frac{V_Z}{I_{L\,min}}}$

→ $\boxed{I_{L\,min} = I - I_{Z\,max}}$

Case :



2 methods to Solve :-

1) Variable R_L , Fixed V_i :-

at $V_i = 20$:-

* $R_L = 1k \rightarrow I_{L\,max} = ?$
* $R_L = 10k \rightarrow I_{L\,min} = ?$

at $V_i = 30$:-

* $R_L = 1k \rightarrow I_{L\,max} = ?$
* $R_L = 10k \rightarrow I_{L\,min} = ?$

$I_{L\,max} = ?$

$I_{L\,min} = ?$

2) Variable V_i , Fixed R_L :

at $R_L = 1k$:

* $V_i = 20 \rightarrow I_{L\,min} = ?$
* $V_i = 30 \rightarrow I_{L\,max} = ?$

at $R_L = 10k$:

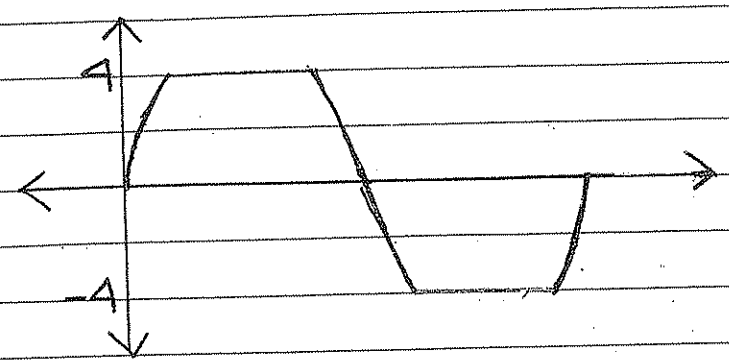
* $V_i = 20 \rightarrow I_{L\,min} = ?$
* $V_i = 30 \rightarrow I_{L\,max} = ?$

$I_{L\,min} = ?$

$I_{L\,max} = ?$

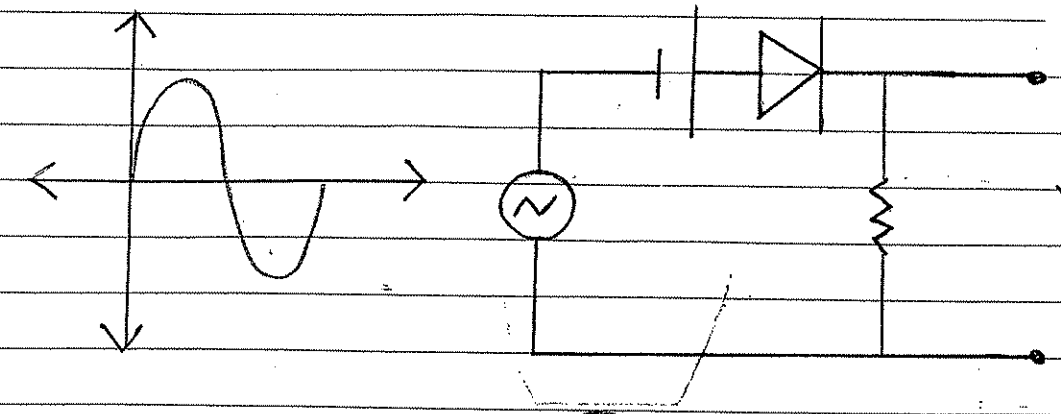
2.3 : Clipper and Clamper Circuits :-

✳ Clipping :- (Limiting) :-

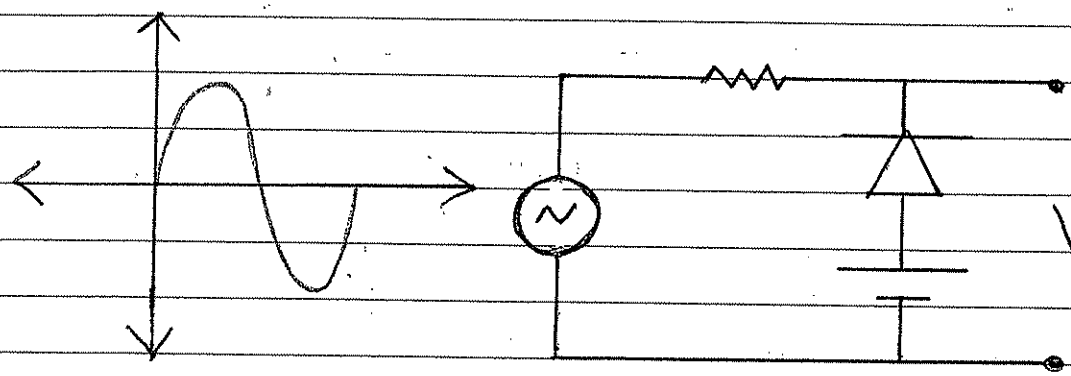


Clipping is a process of Cutting a portion of the A.C i/p Signal to a certain level (+ve, -ve, 0).

* The circuit which performs this function is called Clipper or Limiter ; which contains Diode(s), Resistor, DC Source(s) and AC Source.



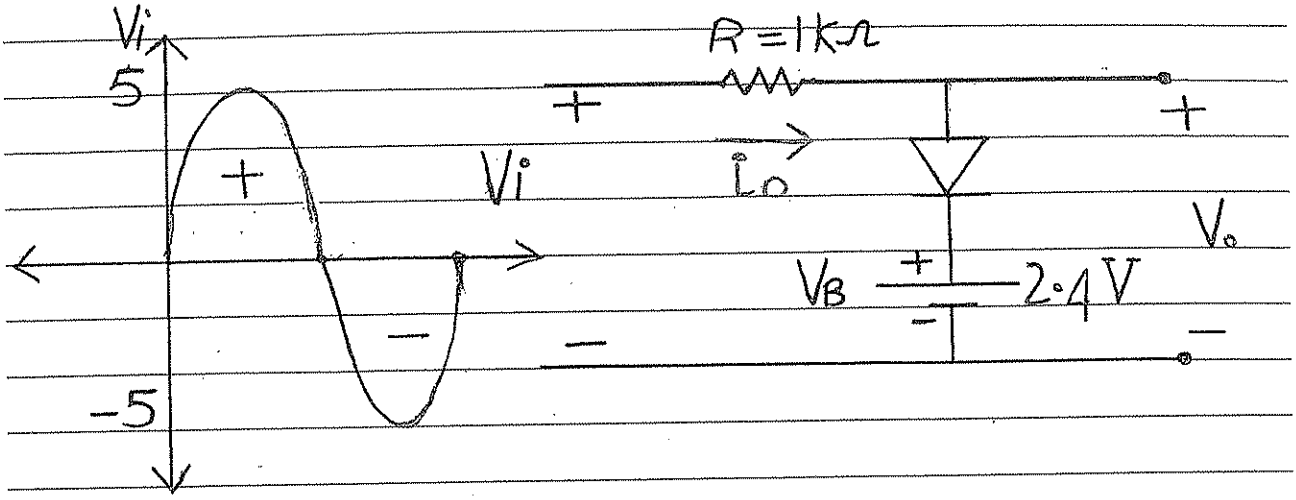
Series - Clipper.



Parallel - Clipper.

EXA. Given : $V_\gamma = 0.6\ V$;

Draw $V_o(t)$ for the indicated input.



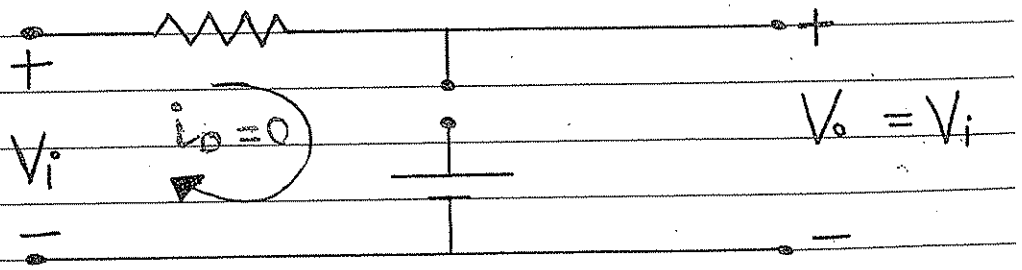
Sol.

In General :-

I] When D is off ; $i_D = 0$

$$-V_i + i_D R + V_o = 0$$

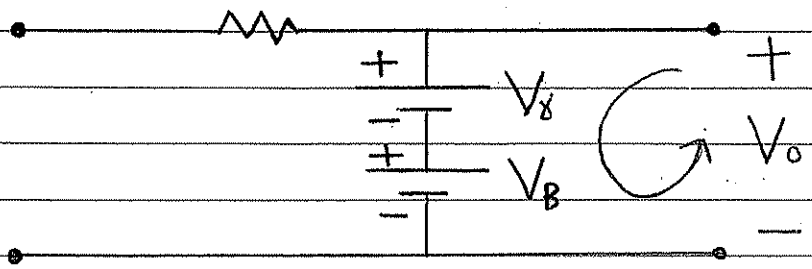
$$\rightarrow \boxed{V_o = V_i}$$



2] When D is ON ;

$$-V_o + V_\gamma + V_B = 0$$

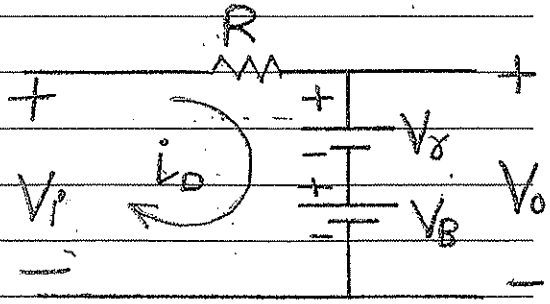
$$V_o = V_B + V_\gamma = 3\,V.$$



Then the Sol. of EXA. :-

1) For (+Ve) H.C of V_i :-

D → F.W

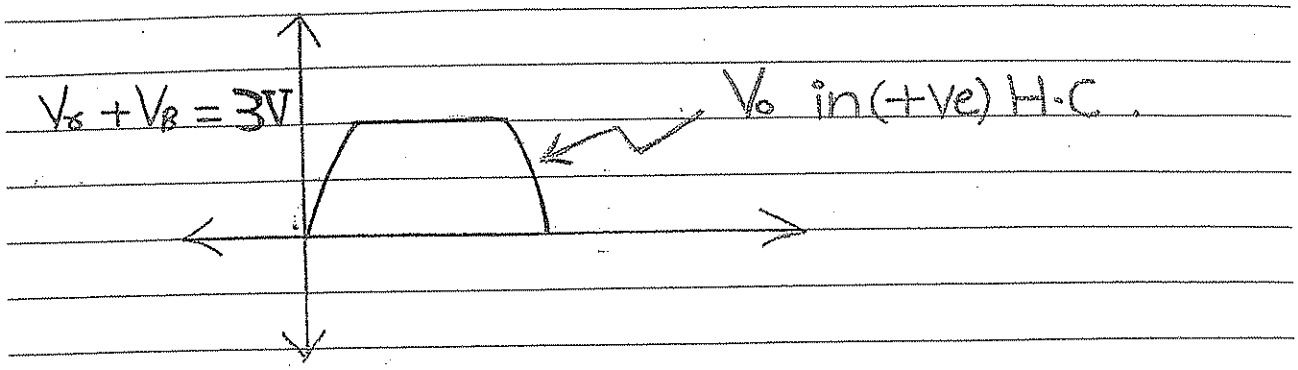


$$-V_i + i_D R + V_\gamma + V_B = 0$$

$$i_D = \frac{V_i - (V_\gamma + V_B)}{R}$$

→ D → ON : $V_i > V_\gamma + V_B$ and $i_D > 0 \rightarrow V_o = V_\gamma + V_B = 3V$

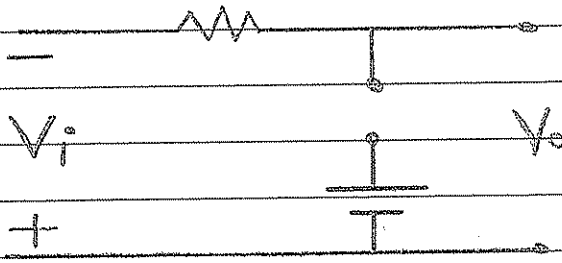
→ D → OFF : $V_i < V_\gamma + V_B$ and $i_D < 0 \rightarrow V_o = V_i$ $(V_i < 3V)$

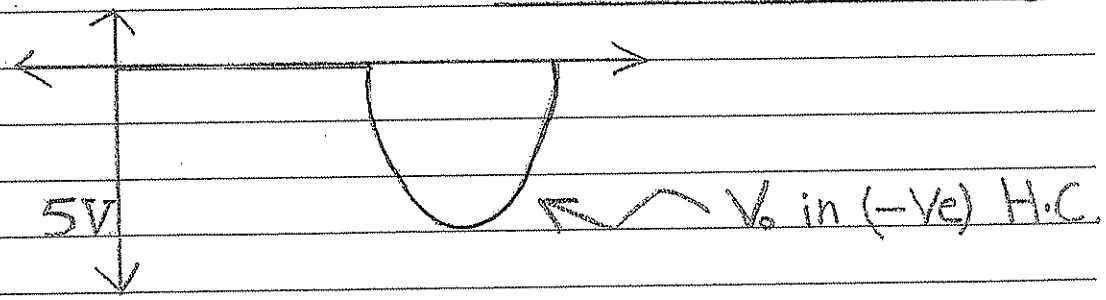


2) For (−ve) H.C of V_i :

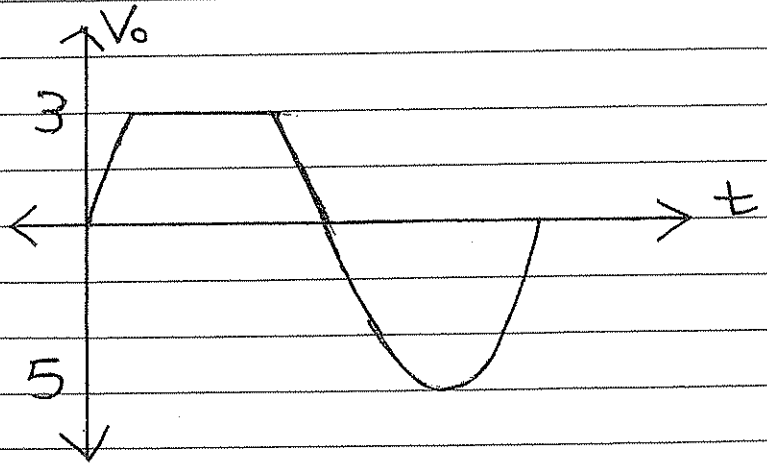
D → Rev. : O.C (off).

$V_o = V_i$

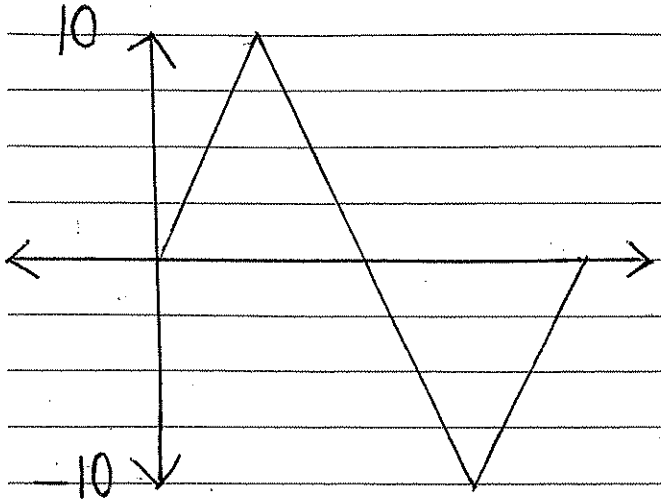


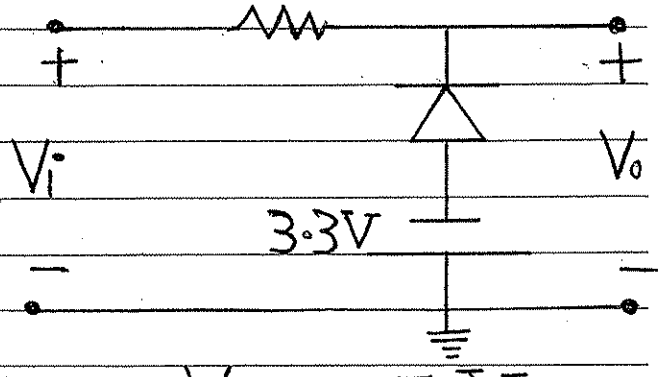


∴ $V_o(t)$:-



EXA: Draw $V_o(t)$ For indicated input:





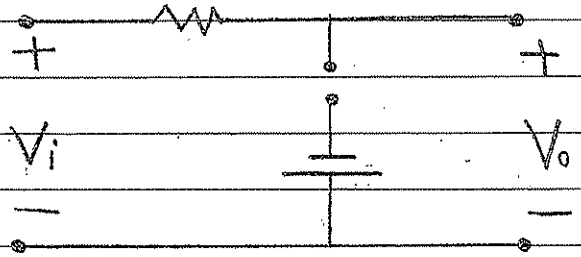
$V_\gamma = 0.7\ V$

Sol.

1) For (+Ve) H.C of V_i :

D → Rev. :- O.C. "off"

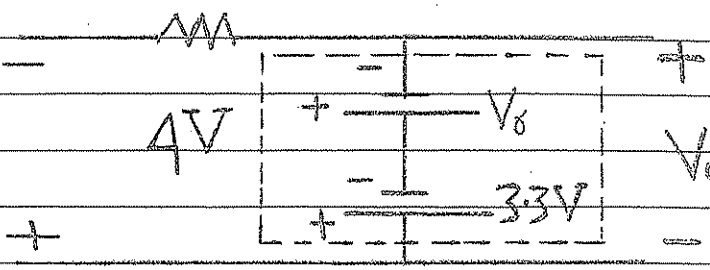
$V_o = V_i$



2) For (-Ve) H.C of V_i :-

$D \rightarrow F.W.$

But :



(1) for $V_i < (V_\gamma + V_B)$

$V_i < -4$

$(\ldots, -2, -3)$

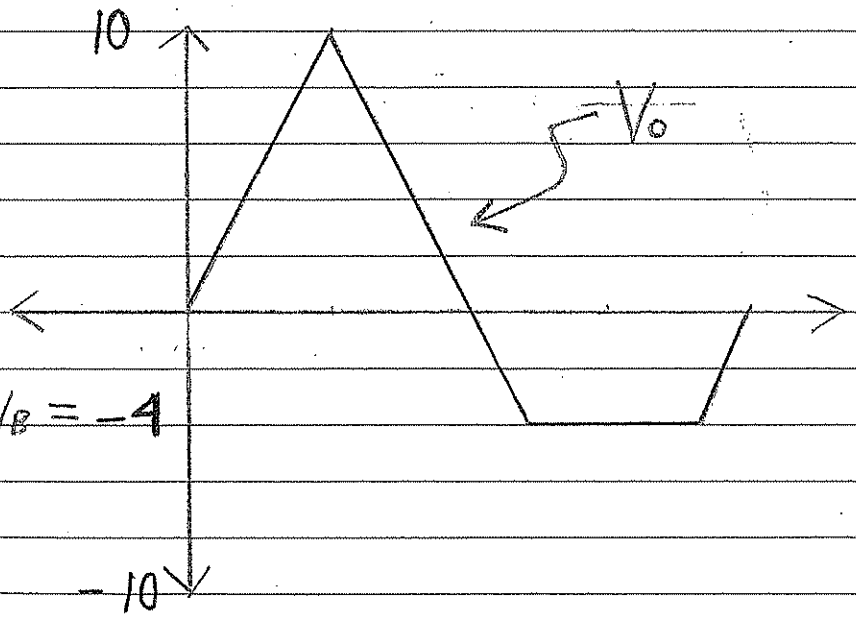
$D \rightarrow$ Off $\rightarrow V_o = V_i$

(2) for $V_i > -4$ V

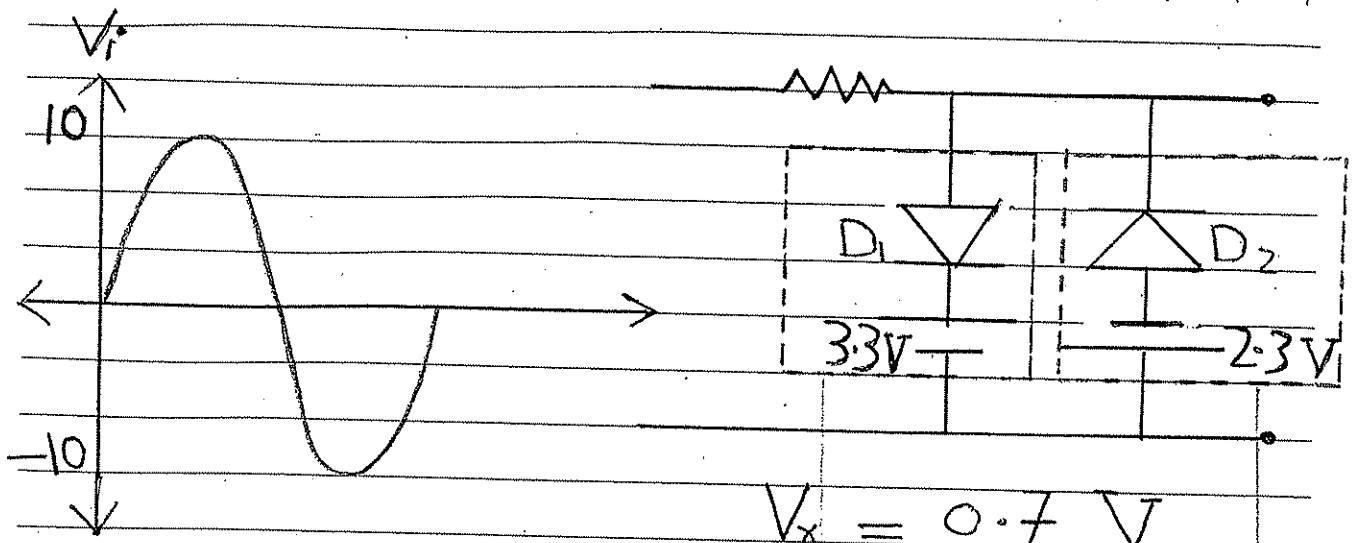
$(-5, -6, \ldots)$

$D \rightarrow$ ON

$V_o = -(V_\gamma + V_B) = -4$

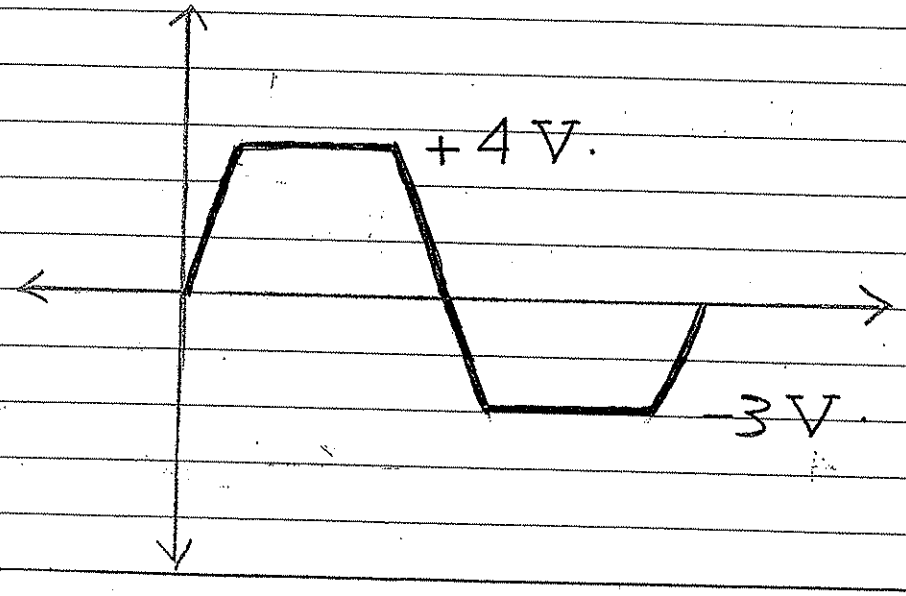


Case :

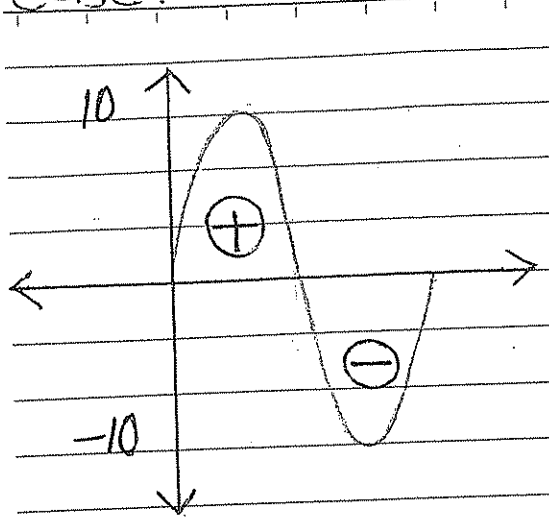


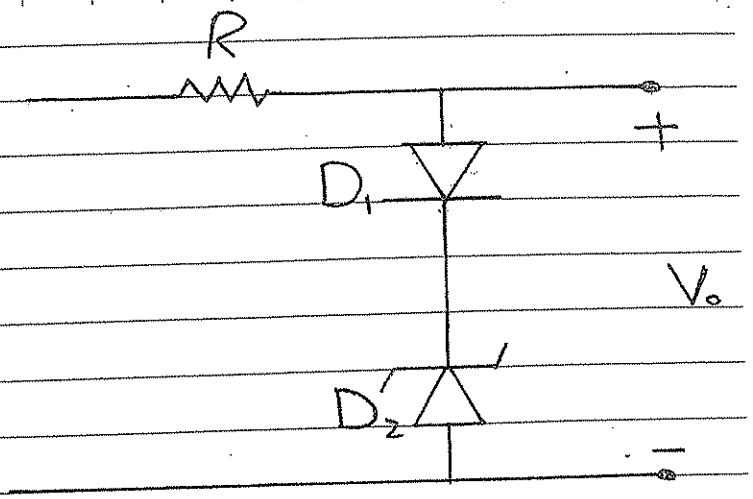
-Ve H.C
نكتبوهنا الجزء
غير موجود.

+Ve H.C
نكتبوهنا الجزء
غير موجود.



Case:





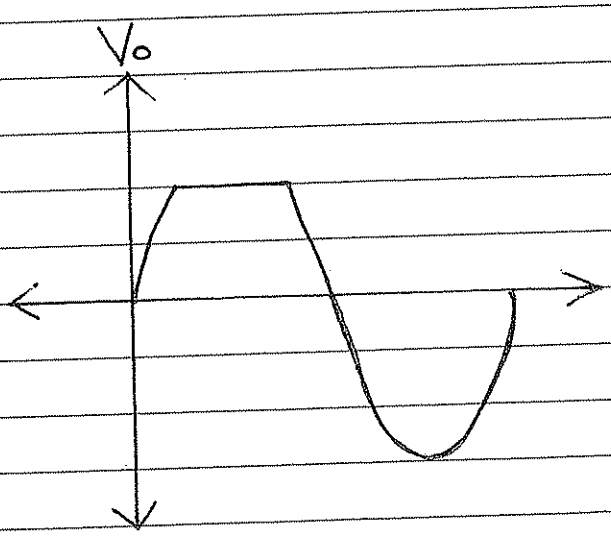
$V_\delta = 0.7\ V$, $V_Z = 6.3\ V$.

Draw $V_o(t)$?

1) When D_1 or D_2 is open : $V_o = V_i$

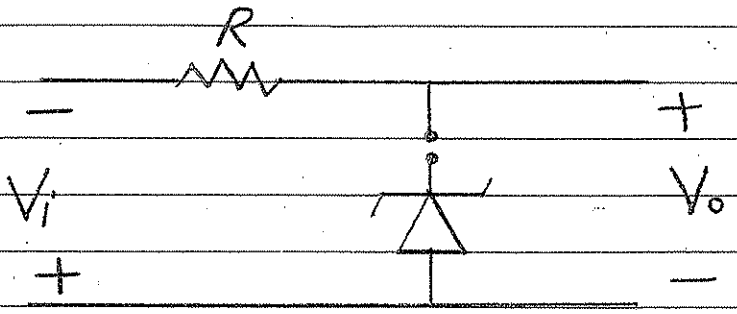
2) When Both D_1 & D_2 are (ON) :

$V_o = V_\delta + V_Z$



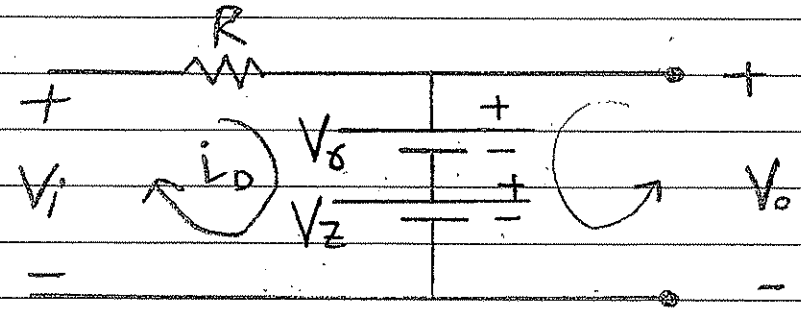
1) During (-ve) H.C of V_i :-

$D_1 \rightarrow$ OFF ; $V_o = V_i$



2) During (+Ve) H.C of V_i :-

$D_1 \rightarrow$ F.w ; $D_2 \rightarrow$ Rev.



$-V_i + i_D R + V_\gamma + V_Z = 0$

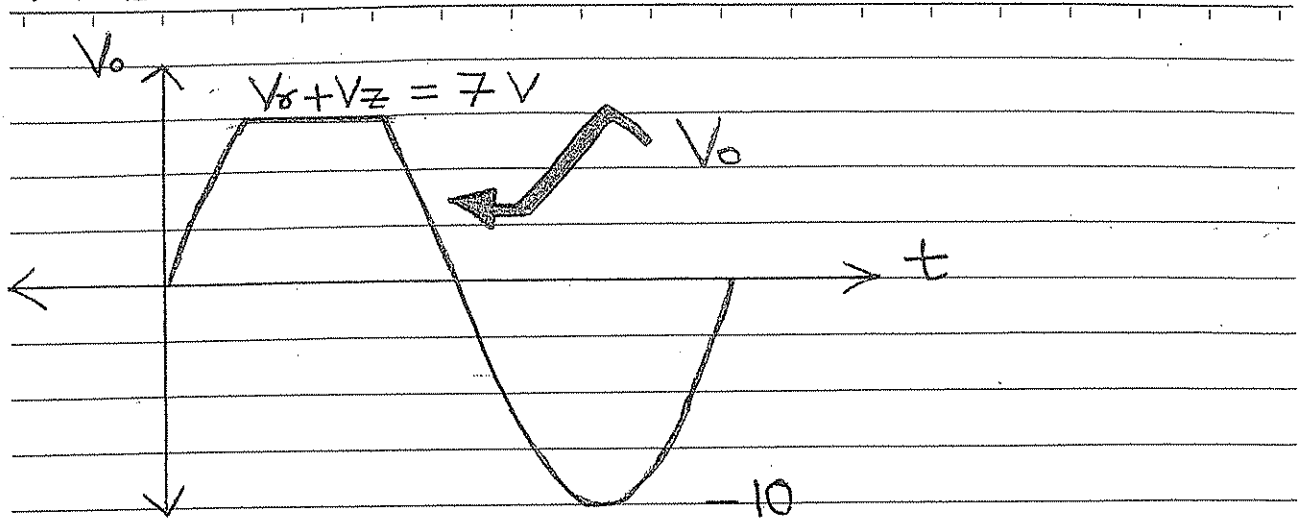
$i_D = \frac{V_i - (V_\gamma + V_Z)}{R}$

→ For $V_i > V_\gamma + V_Z$: $D_1 \rightarrow$ ON , $i_D > 0$

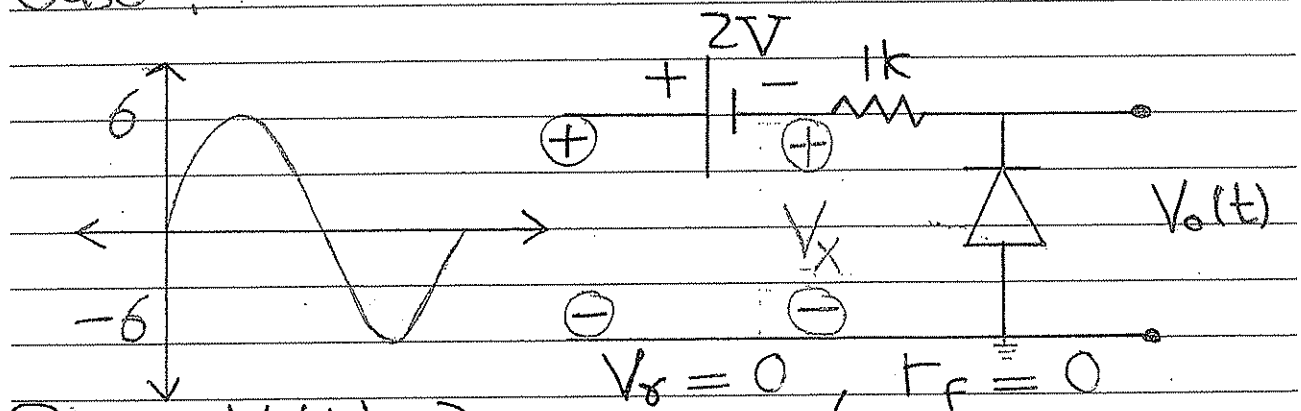
$V_o = V_\gamma + V_Z = \underline{\underline{7\ V}}$.

→ For $V_i < V_\gamma + V_Z$: $D_1 \rightarrow$ Off , $i_D < 0$

$V_o = V_i$



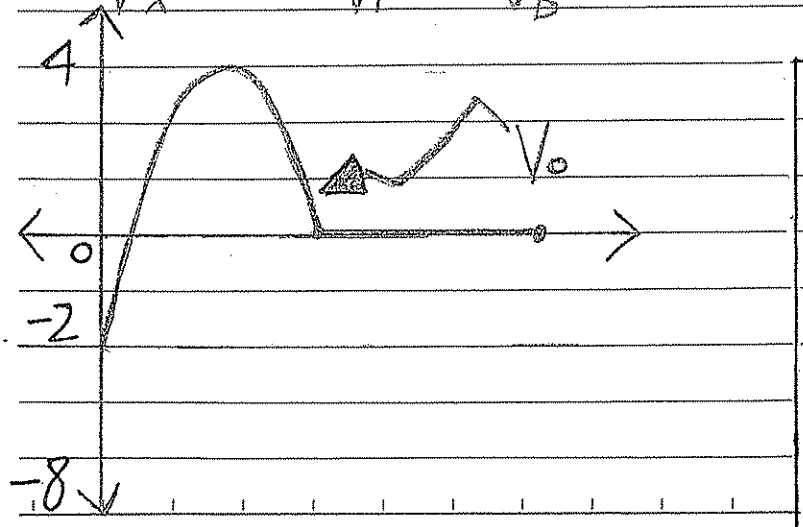
Case :



Draw $V_o(t)$?

Sol. $-V_i + V_B + V_x = 0$

$V_x = V_i - V_B = -2 + V_i$



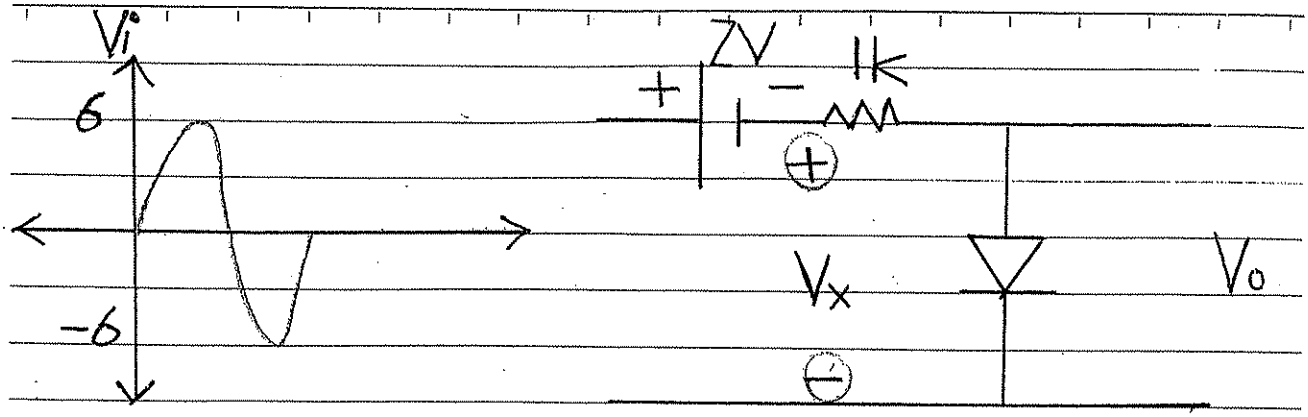
* D → ON : S.C :

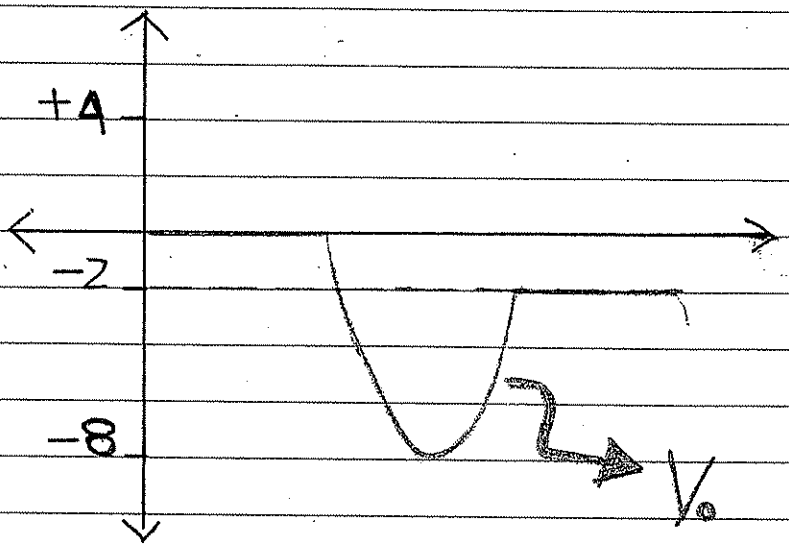
$V_o = 0$ ideal

or: $V_o = 0 - V_\gamma$ real

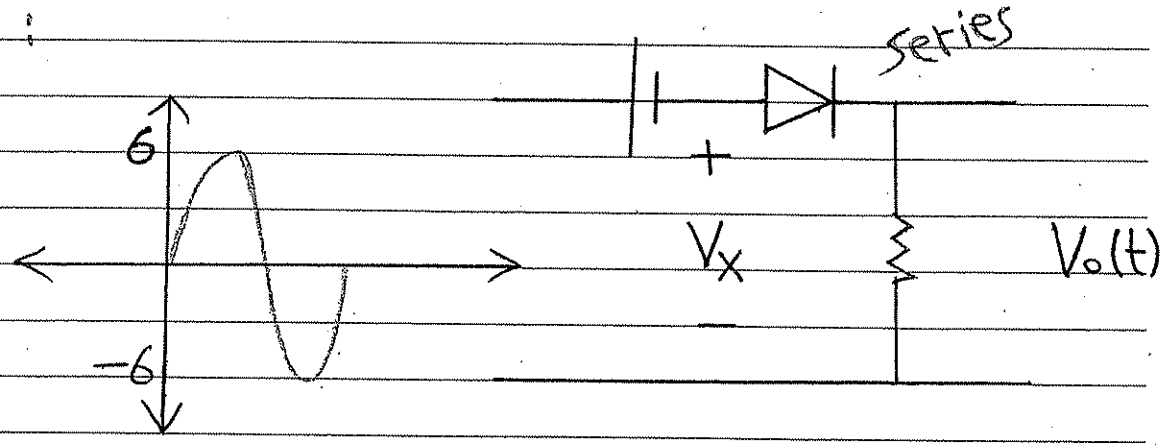
* D → OFF : O.C :

$V_o = V_x$





Case :

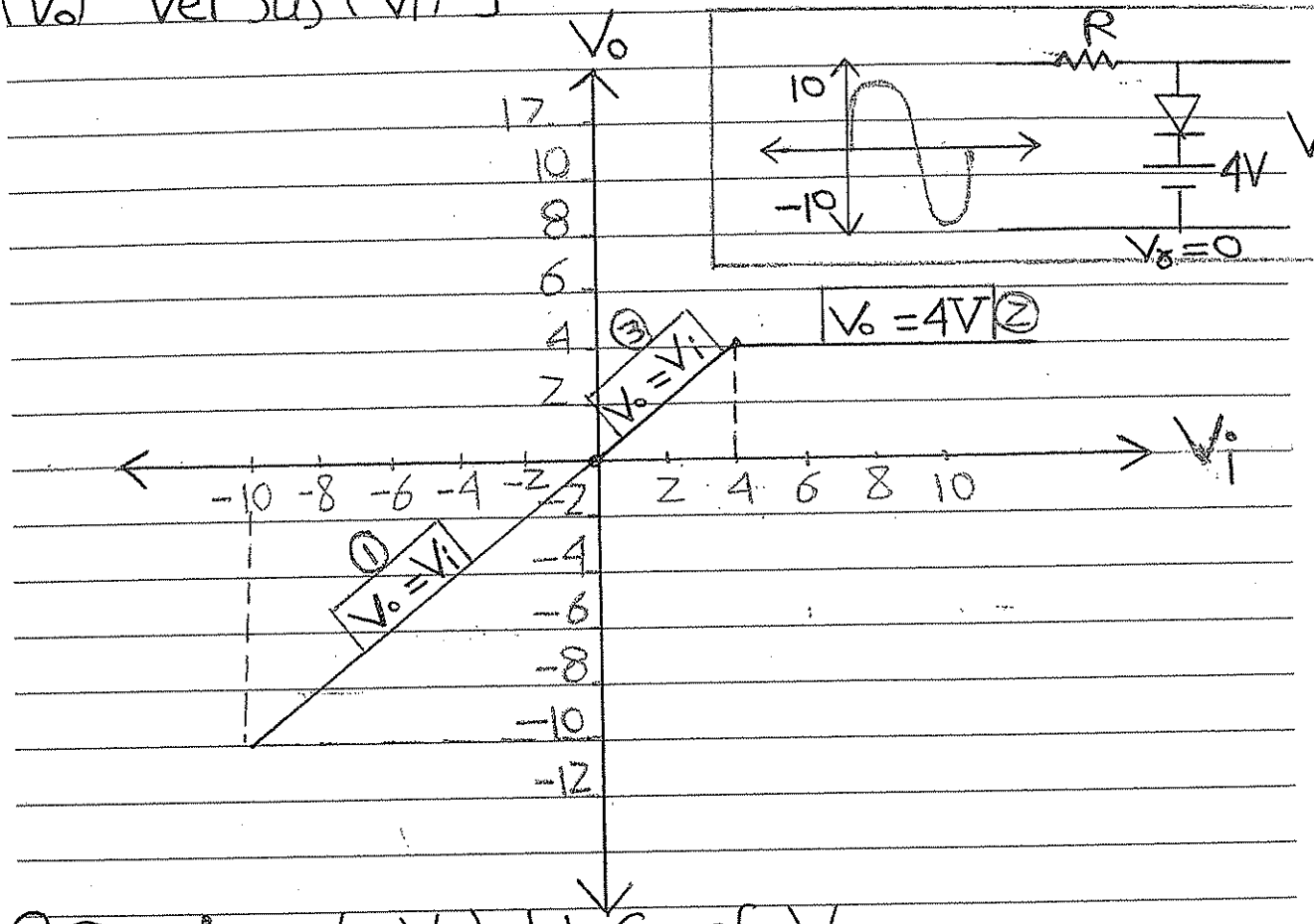


D : ON → $V_o = V_x$

D : OFF → $V_o = 0$

* Transfer Characteristics :-

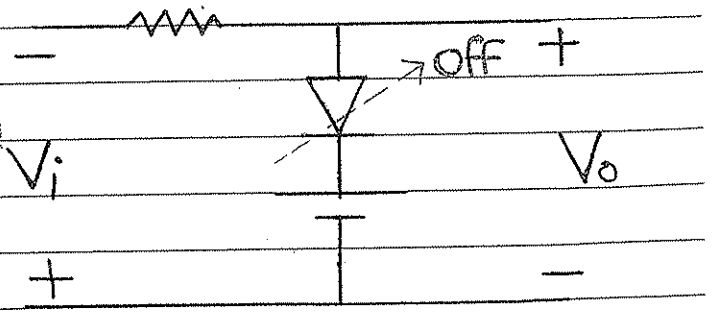
{(Vo) Versus (Vi)}



(1) During (-Ve) H.C of Vi :

D → OFF : Rev. → O.C

$V_o = V_i$ ——— (1)



(2) During (+Ve) H.C of V_i :-

$D \rightarrow F.W \quad ; \quad i_D = \frac{V_i - 4}{R}$

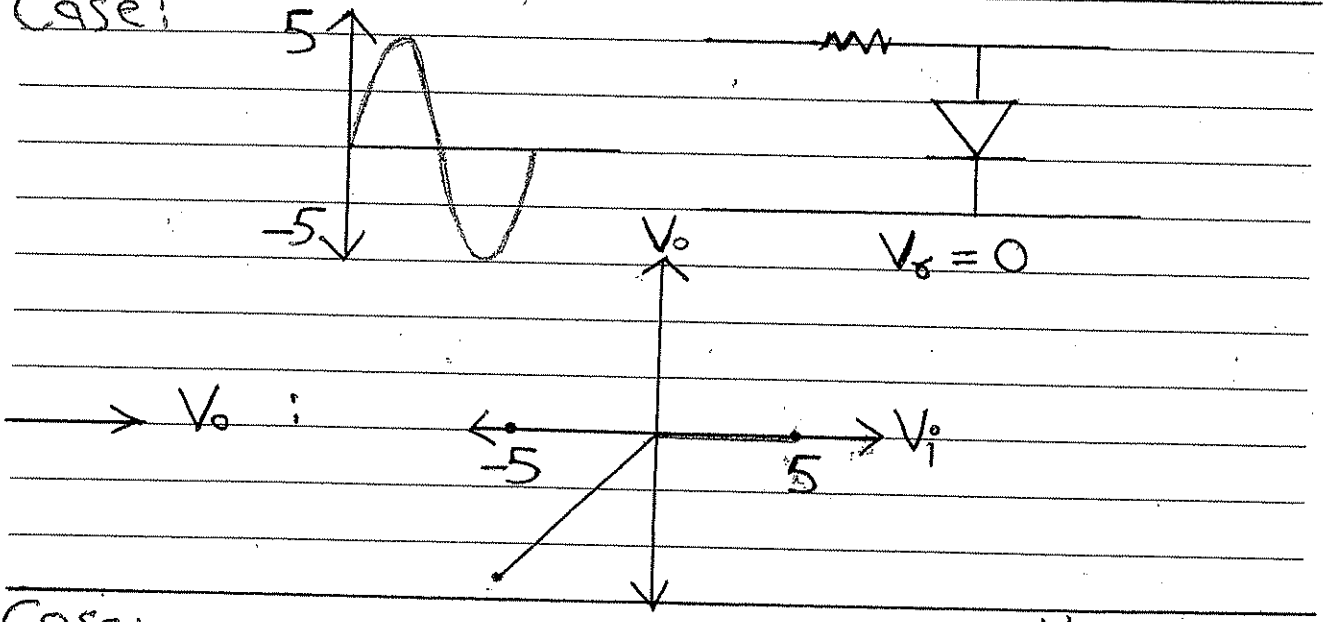
1] for $V_i > 4V$, $i_D > 0$

$\rightarrow D : ON \rightarrow \boxed{V_o = 4V}$ —— (2).

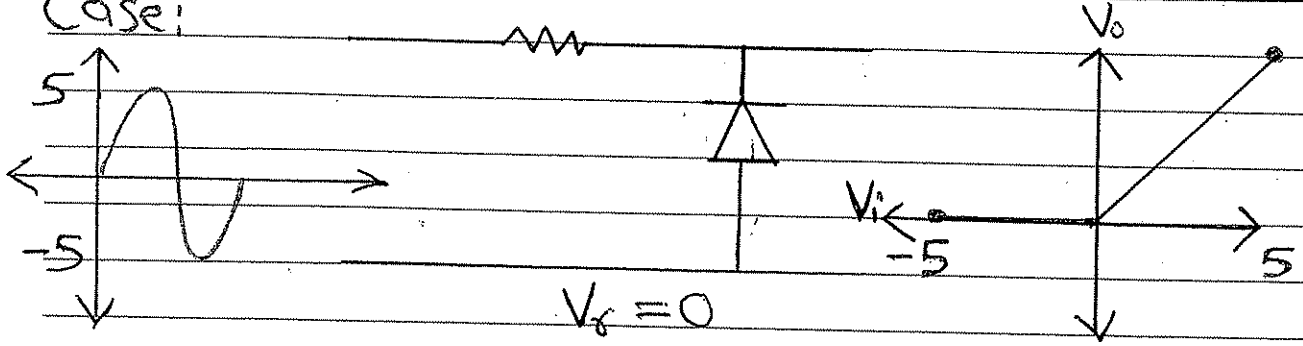
2] for $V_i < 4V$, $i_D < 0$

$\rightarrow D : OFF \rightarrow \boxed{V_o = V_i}$ —— (3).

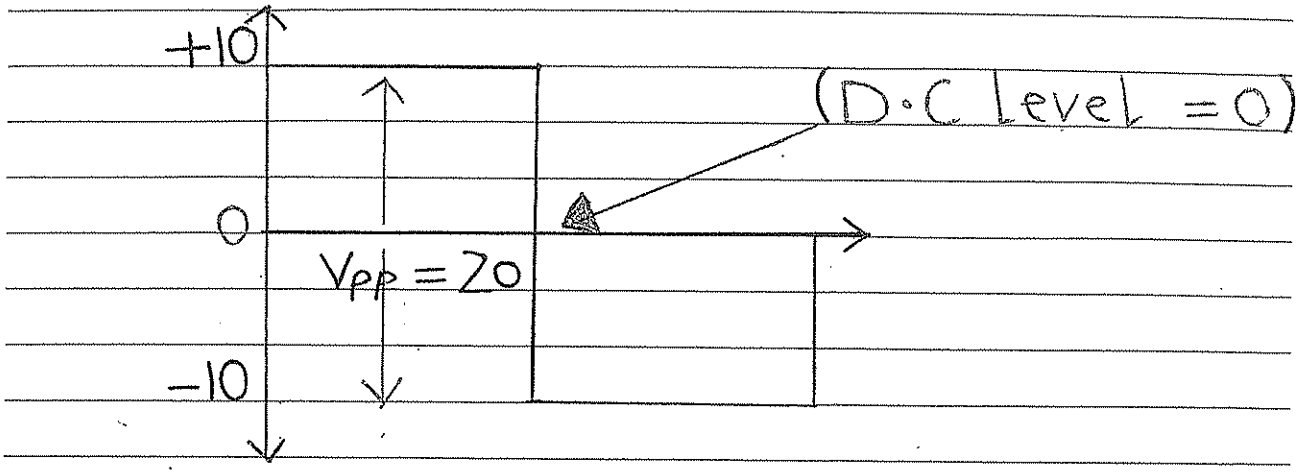
Case:



Case:

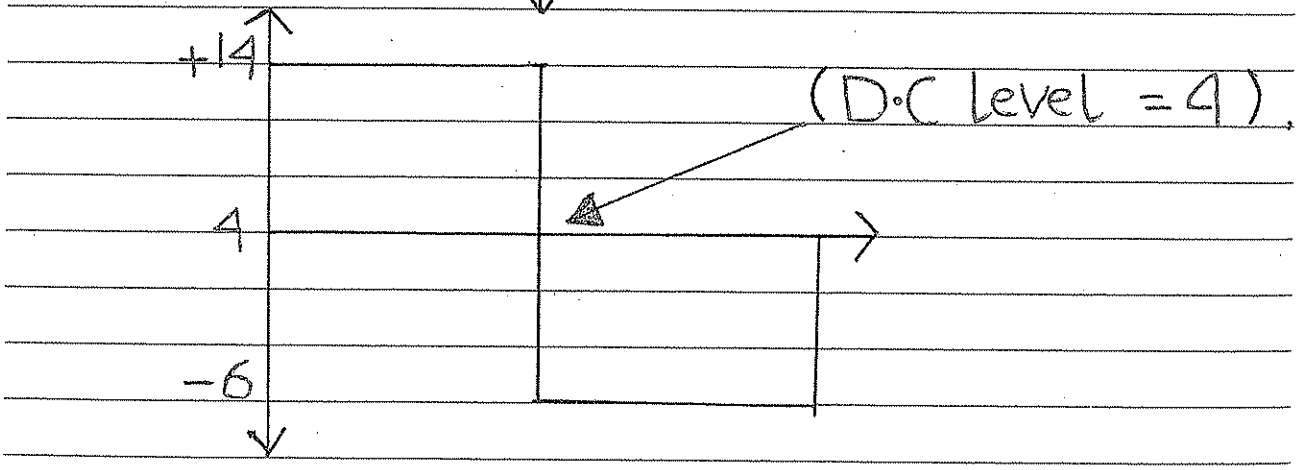


✳ Clamping :-



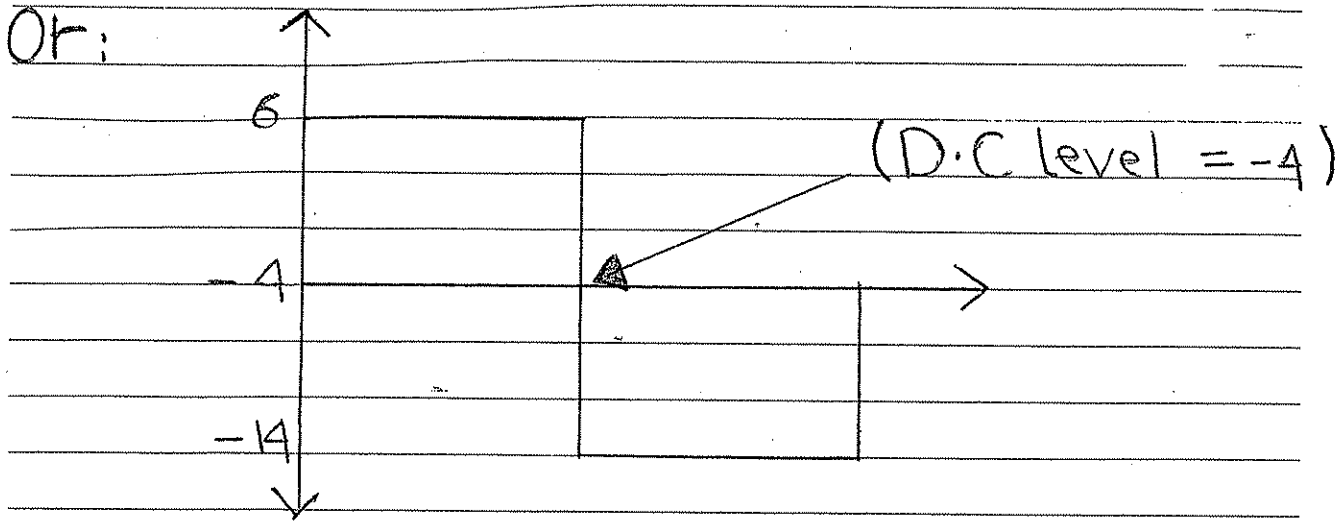
$V_{pp} = 10 - (-10) = 20\ V$

By Clamping.



$V_{pp} = 14 - (-6) = 20\ V$

Or;

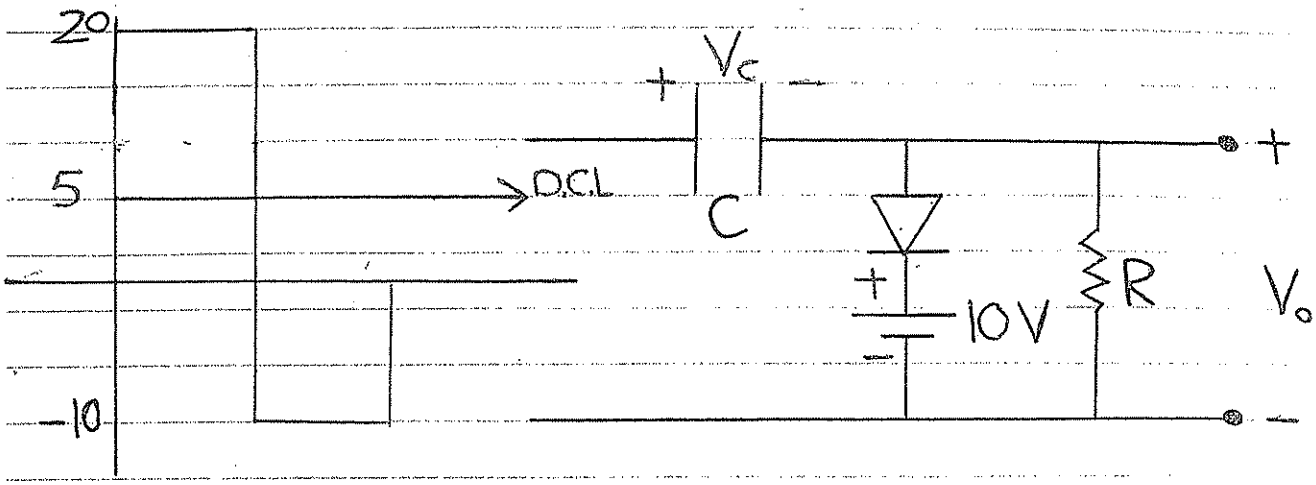


$V_{pp} = 6 - (-14) = 20\ V.$

* Clamping :-

A process of Changing D·C·Level of A·C input signal without Changing the Shape of P-P Value.

Standard :-



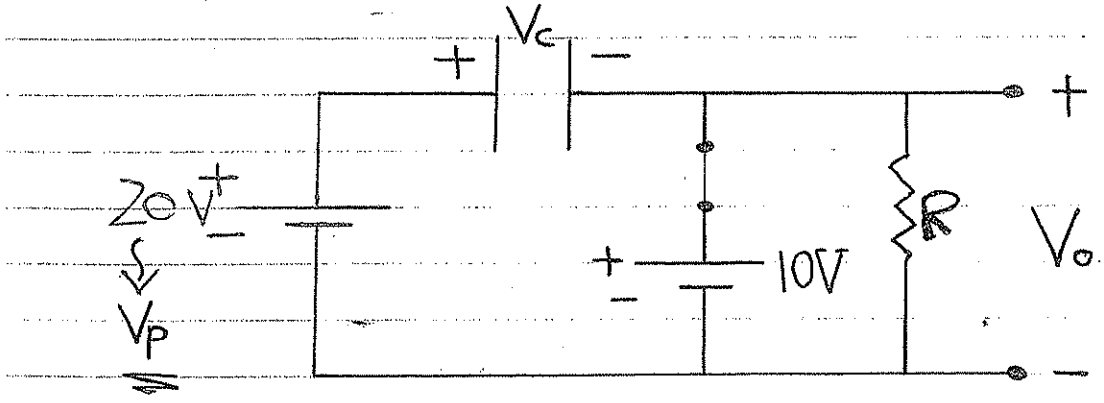
$$D.C.L = \frac{20 + (-10)}{2} = 5V.$$

$$V_{PP} = 20 - (-10) = 30\ V.$$

Draw $V_o(t)$?

Sol.

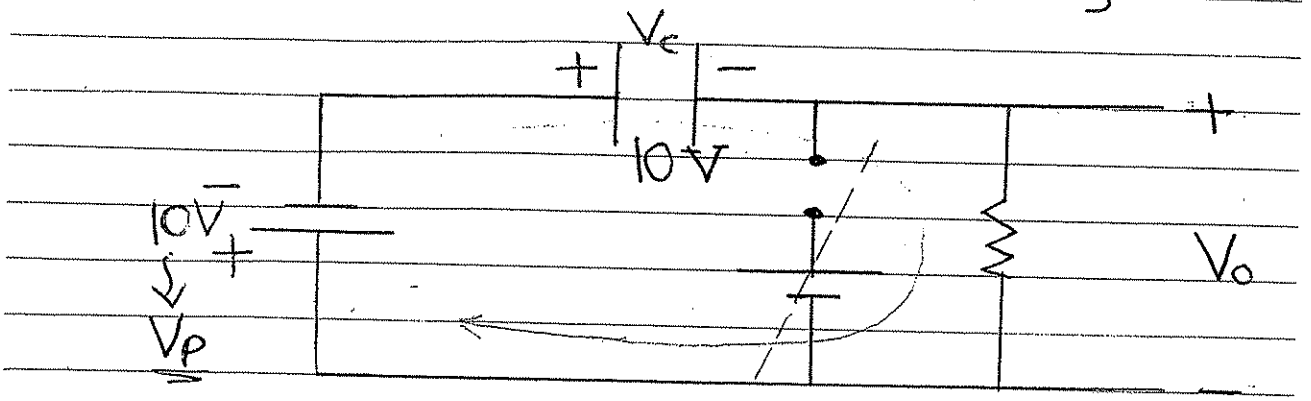
1] Start with H.C Which make D ON.



$$-20 + V_c + 10 = 0 \longrightarrow \boxed{V_c = 10\ V}.$$

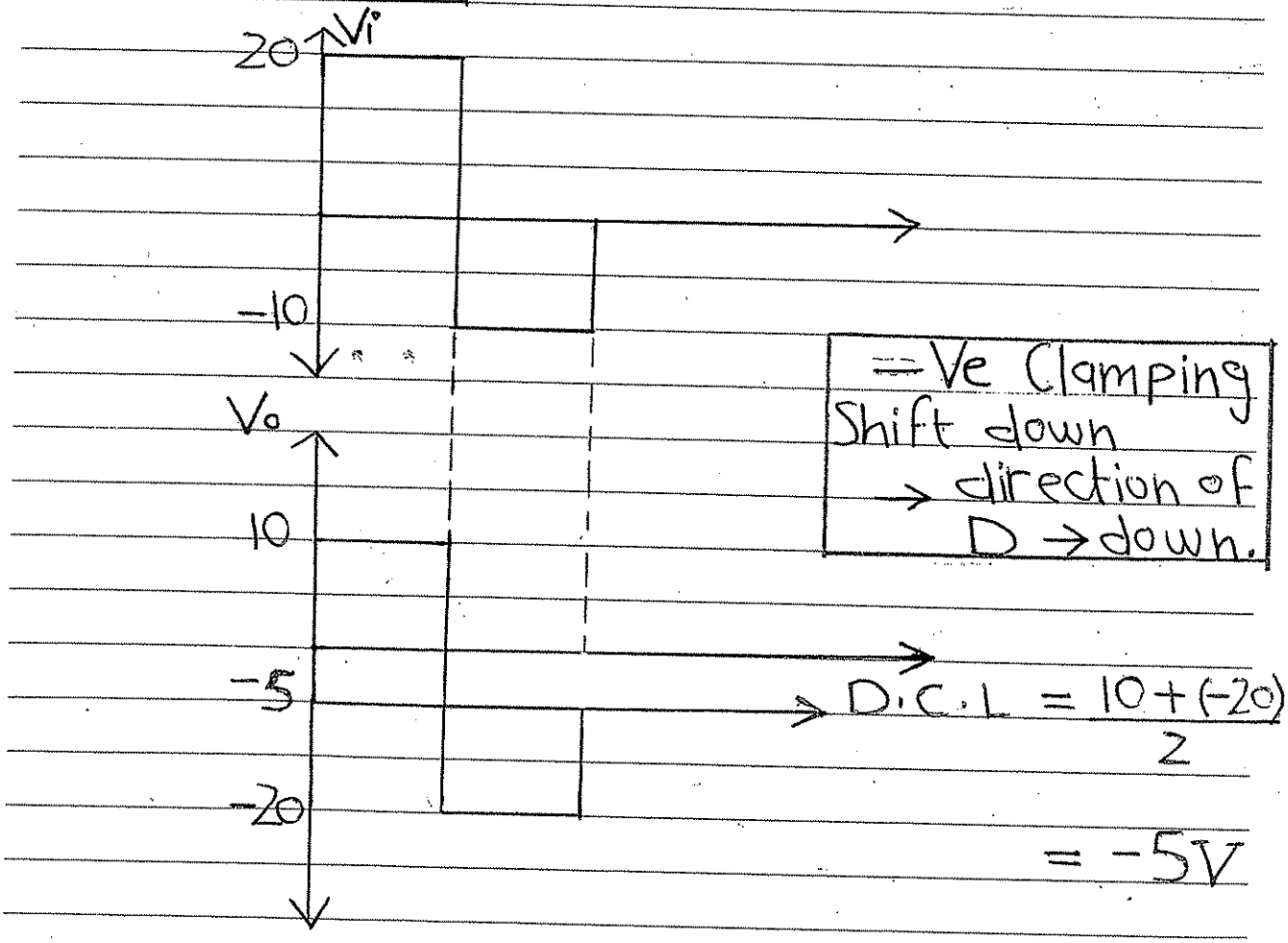
$$\boxed{V_o = 10\ V}$$

2] Consider H.C which makes D off.



$10 + 10 + V_o = 0$

$V_o = -20\ V$



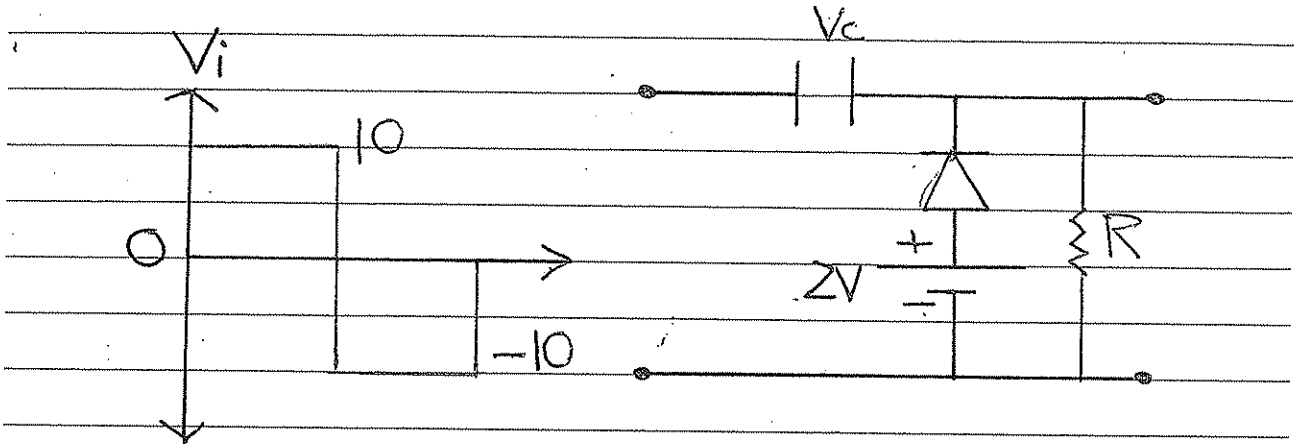
= Ve Clamping
Shift down
→ direction of
D → down.

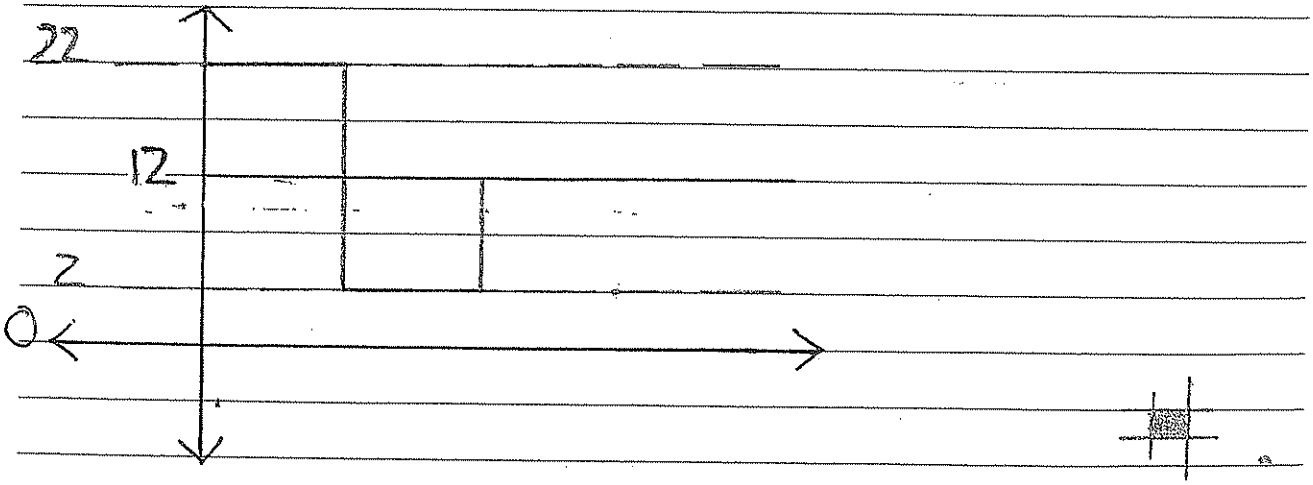
$D.C.L = \frac{10 + (-20)}{2}$

$= -5V$

* Type of Clamping ⟶ Diode Direction.

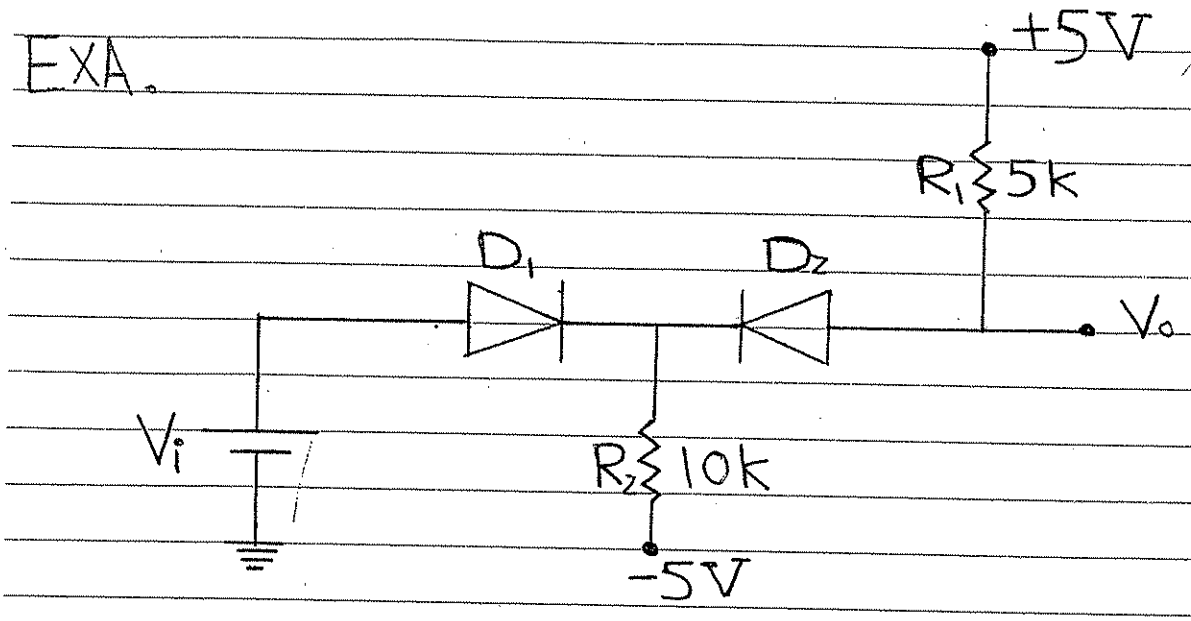
* Value of Polarity of V_B ⟶ Clamping leve & D.C. level.





2.4: Multi-Diodes Circuits :-

EXA.



$V_{\gamma_1} = V_{\gamma_2} = 0.7\ V$

$r_{f_1} = r_{f_2} = 0$

Find : I_{D_1}, I_{D_2}, V_o ; When :

i : $V_i = 1V$

ii : $V_i = 4V$

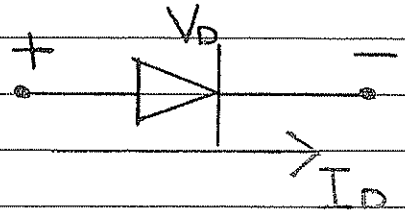
(homework)

Five Apple

Sol.

In General :-

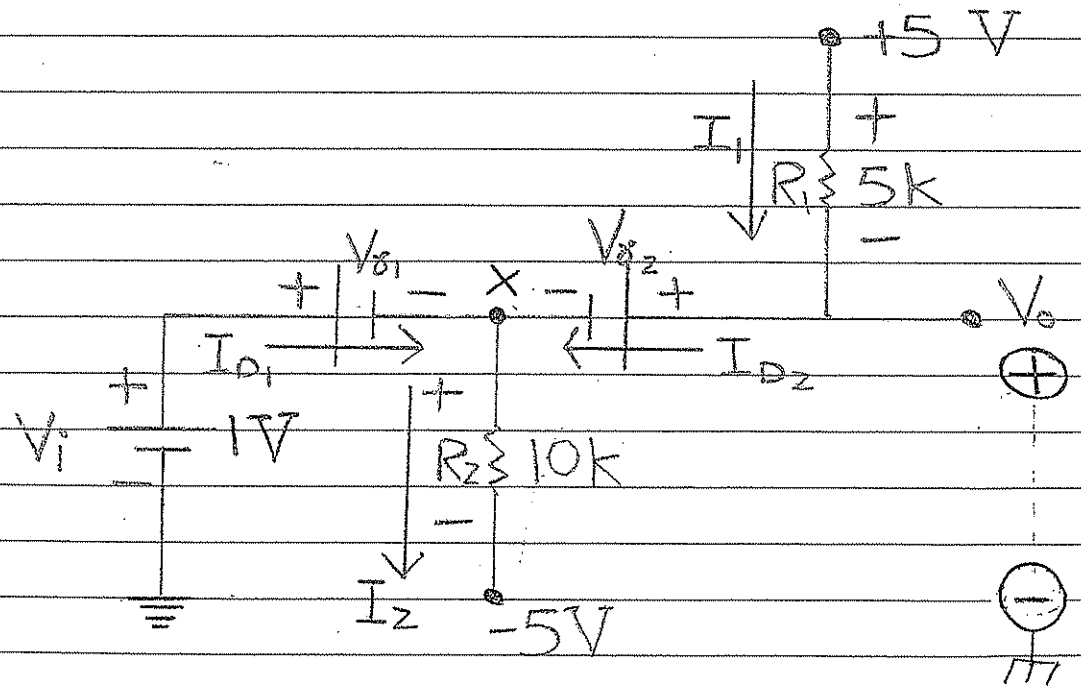
1] For (ON) Diode : $I_D > 0$.



2] For (OFF) Diode : $V_D < V_\gamma$

(i): $V_i = 1V$:-

Assume D_1 & D_2 : ON. :-



* $-1 + V_{\gamma_1} - V_{\gamma_2} + V_o = 0$

$V_o = 1 - V_{\gamma_1} + V_{\gamma_2} = 1\,V.$

* $I_1 = \frac{5 - V_o}{R_1}$

$= \frac{5-1}{5} = \frac{4}{5} = 0.8\,mA.$

$I_1 = I_{D_2} = 0.8\,mA.$

* $-1 + V_{\gamma_1} + V_x = 0$

$V_x = 1 - V_{\gamma_1}$

$= 1 - 0.7 = 0.3\,V.$

* $I_z : \quad -V_x + I_z \cdot R_z - 5 = 0$

$I_z = \frac{5 + 0.3}{R_z} = \frac{5.3}{10k} = 0.53\,mA$

* KCL at node (x) :

$I_{D_1} + I_{D_2} = I_z$

$I_{D_1} = 0.53 - 0.8$

$= -0.27\,mA.$

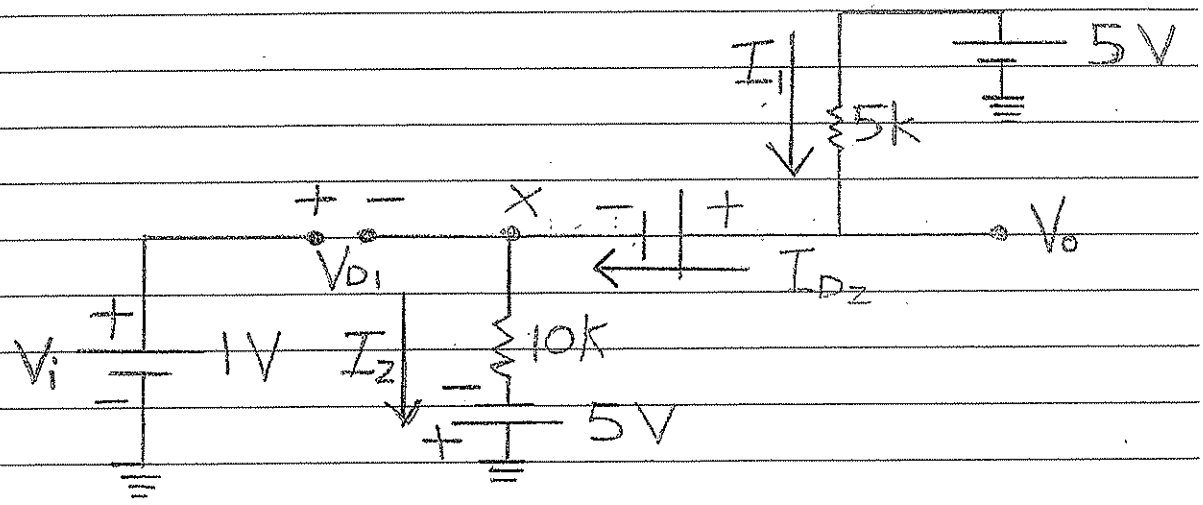
Since $I_{D_1} < 0$: $\therefore D_1 \rightarrow OFF$.

$\rightarrow I_{D_1} = 0$.

$* -1 + V_{D_1} + V_x = 0$

$V_{D_1} = 1 - 0.3 = 0.7\ V$.

$D_1 \Rightarrow$ off ; $D_2 \Rightarrow$ ON : الآن نقيد حل السؤال بناءً على



$-5 + 5I_1 + V_{\delta_2} + 10I_2 - 5 = 0$

$I_1 = I_2 = I_{D_2}$

$I_{D_2} = \frac{10 - 0.7}{15} = \frac{9.3}{15} = 0.62mA$

$V_{D_2} = V_{\delta_2} = 0.7\ V$.

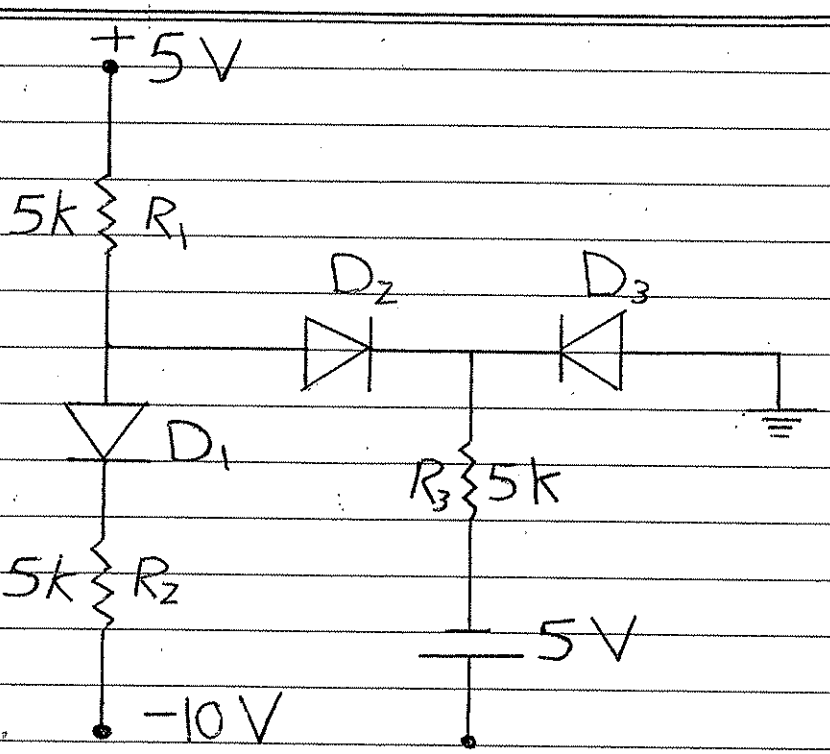
V_o :

$-5 + 5I_1 + V_o = 0$

$V_o = 5 - 5 * 0.67$

$= 1.9V.$

EXA :

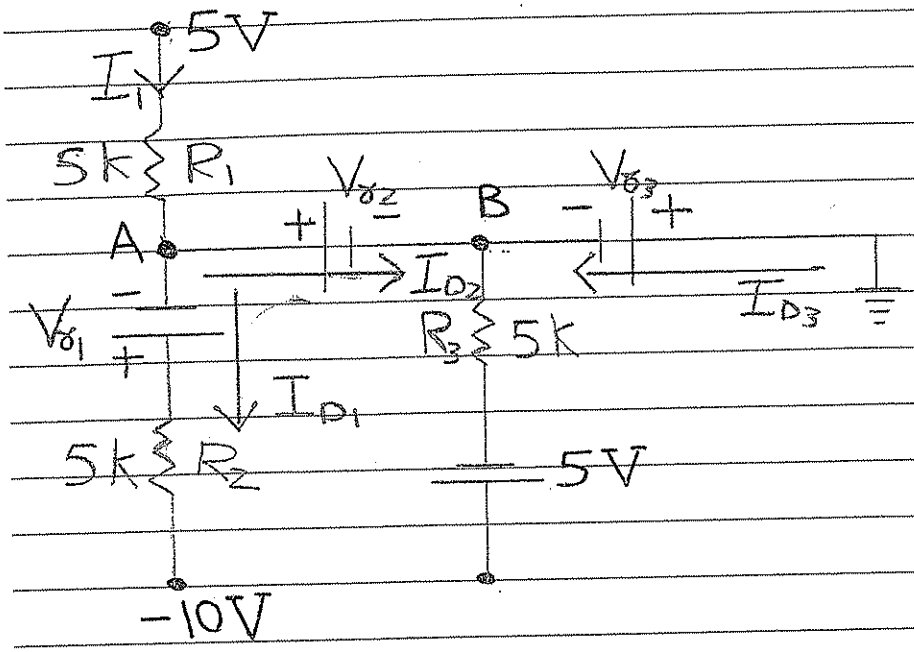


$V_{\gamma 1} = V_{\gamma 2} = V_{\gamma 3} = 0.7V$

Find I_{D1}, I_{D2}, I_{D3} ?

Sol. :-

Assume $D_1, D_2, D_3 \rightarrow ON$:-



* $-V_B - V_{\gamma_3} = 0$

$\therefore V_B = -V_{\gamma_3} = -0.7\ V.$

* $-V_A + V_{\gamma_2} - V_{\gamma_3} = 0$

$V_A = 0$

* $I_1 = I_{D_1} + I_{D_2}$; At node A.

$I_1 = \frac{5 - V_A}{R_1} = \frac{5 - 0}{5} = 1\ mA.$

* I_{D1} :

$$-V_A + V_{\gamma_1} + I_{D1} R_2 - 10 = 0$$

$$\rightarrow I_{D1} = \frac{10 + V_A - V_\gamma}{5} = \frac{9.3}{5} = 1.86\,mA$$

* I_{D2} :

$$I_{D2} = I_1 - I_{D1}$$

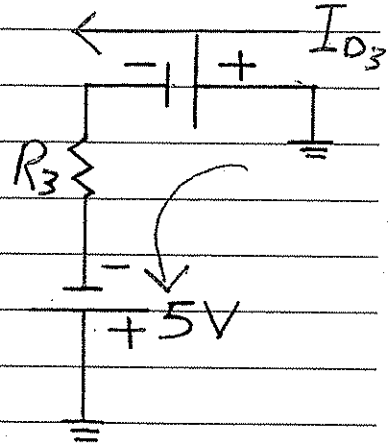
$$= 1 - 1.86 = -0.86\ mA.$$

$\therefore$ D_2 : OFF ; $I_{D2} = 0$ ✓

* $V_{\gamma_3} + 5I_{D3} - 5 = 0$

$$I_{D3} = \frac{5 - 0.7}{5}$$

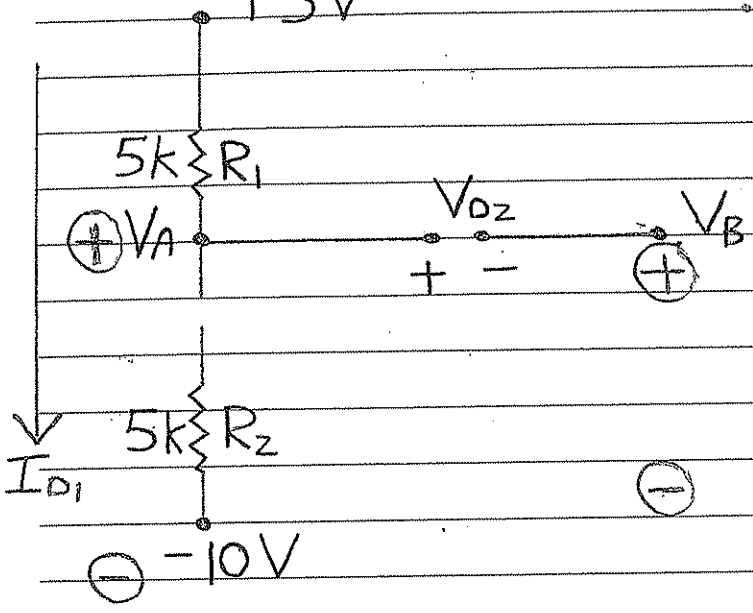
$$= \frac{4.3}{5} = 0.86\,mA$$



*New Assumption:

D_1 ON ; D_2 OFF ; D_3 ON

يجب أن نجد حساب (I_{D_1}).



$$-5 + 5I_{D_1} + V_{\gamma_1} + 5I_{D_1} - 10 = 0$$

$$\blacklozenge I_{D_1} = \frac{15 - 0.7}{10k} = \frac{14.3}{10k} = 1.43\ mA.$$

$$\blacklozenge V_{D_1} = V_{\gamma_1} = 0.7\ V.$$

$$\blacklozenge I_{D_2} = 0$$

$$\blacklozenge V_{D_2} \rightarrow -V_A + V_{D_2} + V_B = 0$$

*$V_B = -0.7V$

$-V_A + V_{\gamma_1} + I_{D_1} * 5 - 10 =$

$*V_A = 0.7 + 1.43 * 5 - 10$

$= -2.3V.$

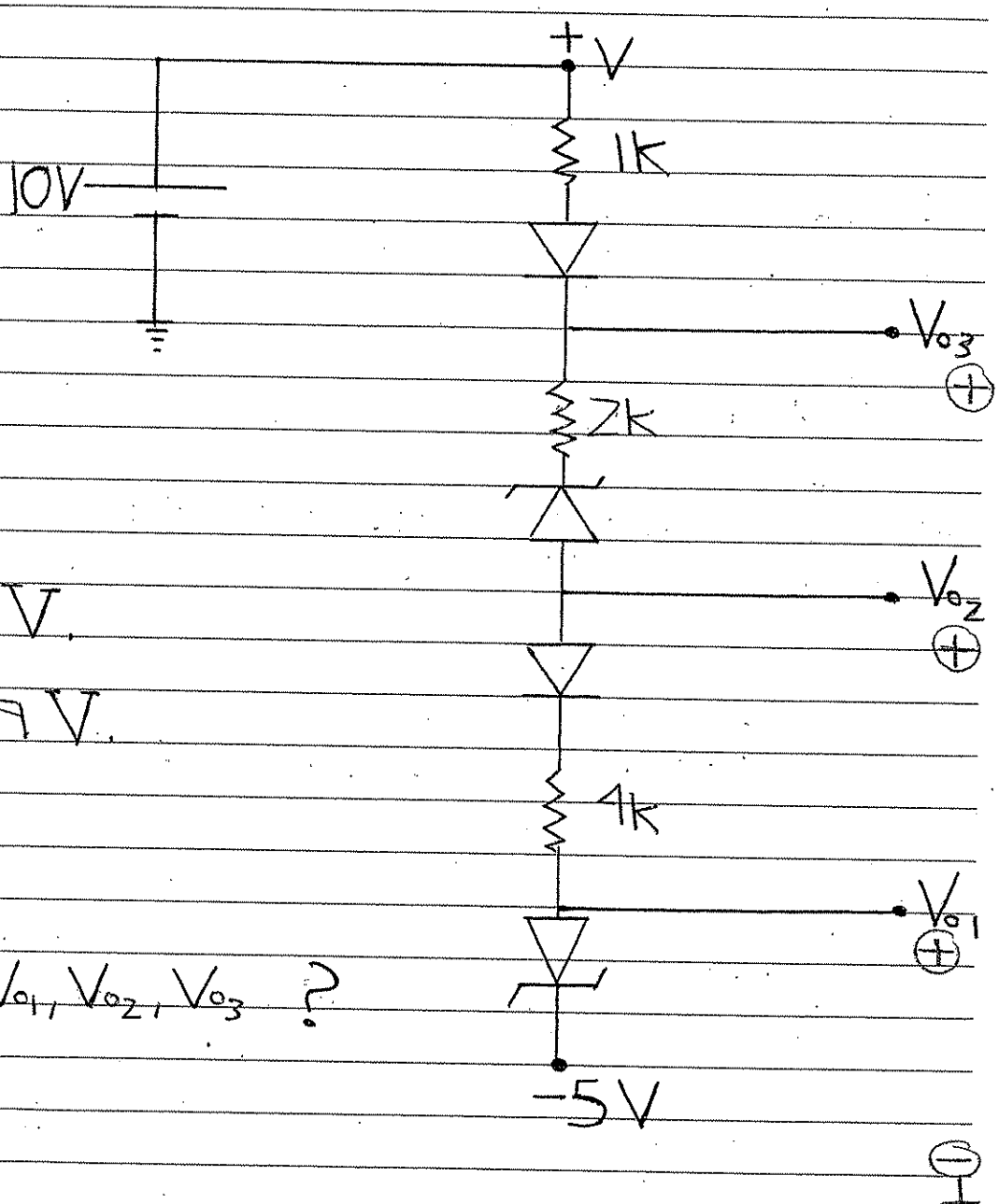
$$V_{D_2} = V_A - V_B = -2.3 + 0.7$$

$$= -1.6\ V$$

(V_{D_2} : OFF)

- $I_{D_3} = 0.86\ m \cdot A$
- $V_{D_3} = V_{\delta_3} = 0.7\ V$

EXA:



$V_6 = 0.7\ V$

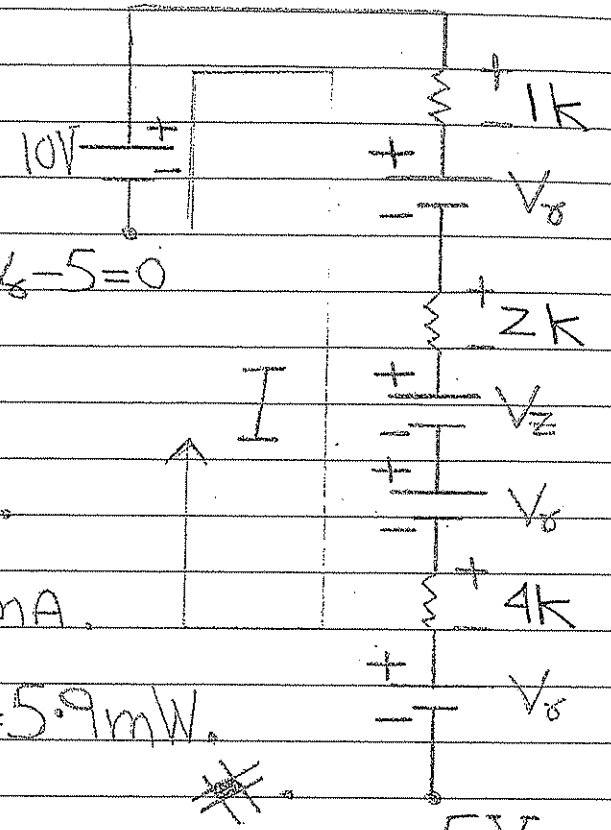
$V_Z = 5.9\ V$

Find:

$I_Z, P_Z, V_{o_1}, V_{o_2}, V_{o_3}$?

Sol. :-

Assume Diodes : ON :-



$-10 + 1I + V_\gamma + 2I + V_z + V_\gamma + 4I + V_\gamma - 5 = 0$

$I = \frac{15 - 3V_\gamma - V_z}{7k}$

$= \frac{15 - 3}{7k} = 1mA.$

$I = I_{D_1} = I_{D_2} = I_z = 1mA.$

$P_z = I_z \cdot V_z = 1 * 5.9 = 5.9mW.$

$* -V_{o_1} + V_\gamma - 5 = 0$

$V_{o_1} = 0.7 - 5 = -4.3V.$

$* -V_{o_2} + V_\gamma + 4*1 + V_\gamma - 5 = 0$

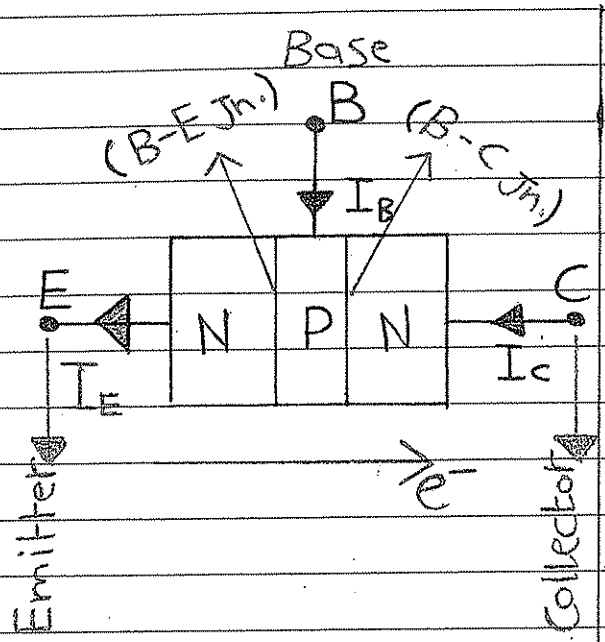
$V_{o_2} = 1.4 + 4 - 5 = 0.4V.$

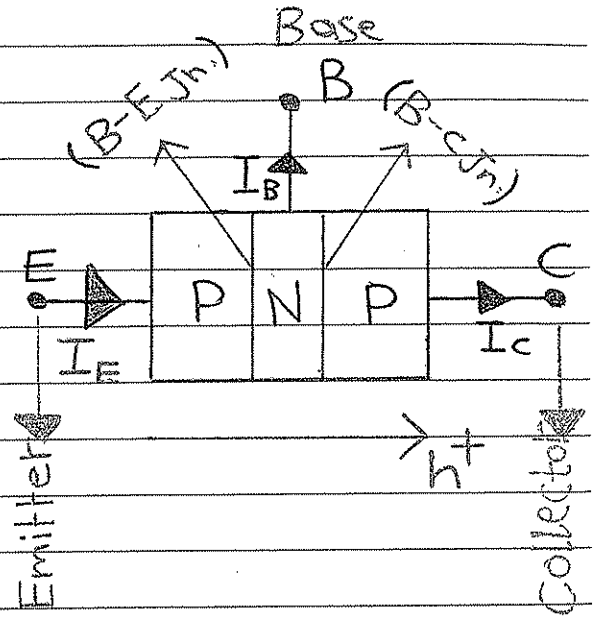
$* -10 + 1*1 + V_{\gamma_3} + V_{o_3} = 0$

$V_{o_3} = 10 - 1 - 0.7 = 8.3V.$

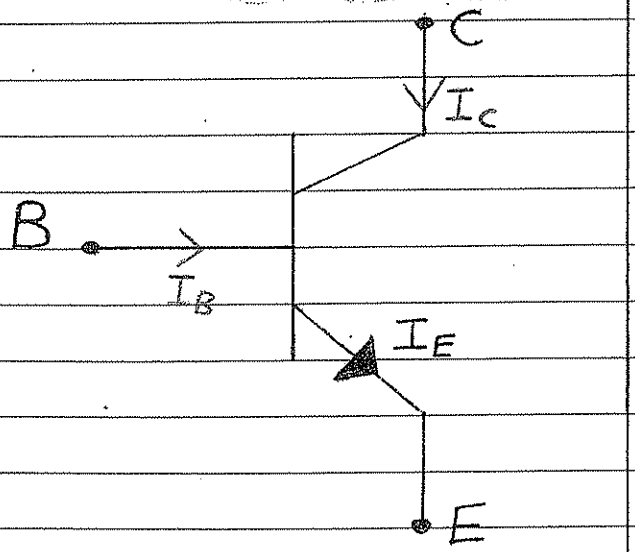
Chaptet (5) :

The Bipolat Junction Transistot :-

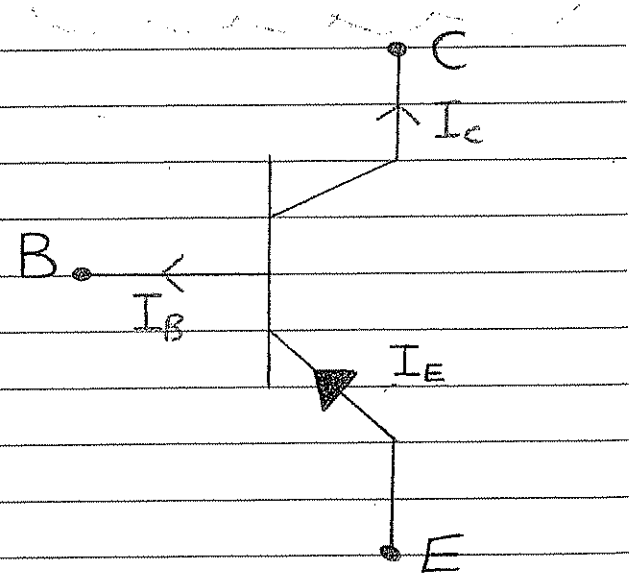




*NPN Transistot.



*PNP Transistot.



1) It is Three-terminal device ;
(Emitter , Base , Collector) .

2) It is a two - PN Jn :
(B-E Jn. and B-C Jn.) .

3) The Base is made thin and has Low doping level Compared to(E) ; to minimize No. of Carriers lost in base due to recombination.

4) It Can be (NPN) or (PNP) , but it is NOT reversable ; because (E) & (C) are different in :
(i) Geometries .
(ii) Doping Level .

5) The arrow direction in (E) refers to conventional direction of (I_E).

6) Since it has two PN. Jns. ; So it can be biased in four operating modes.

7) It can be represented by two diodes back-to-back ; but it does not work as two diodes.

8) It is called Bipolar because the current is due to movment of both carriers (e^- & h^+).

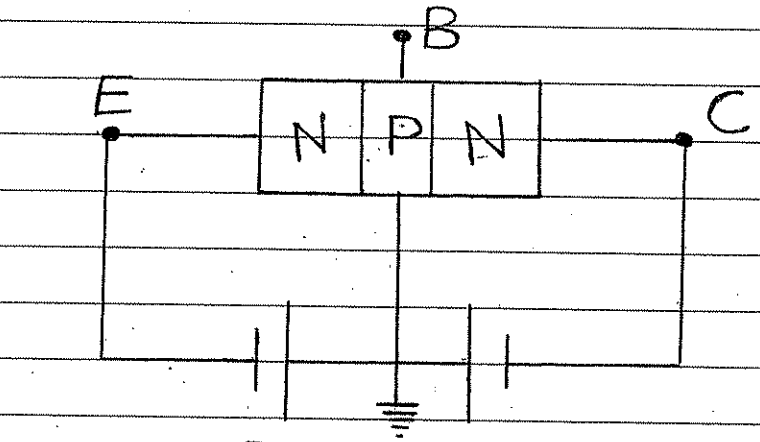
*Operating Modes (for NPN) :-

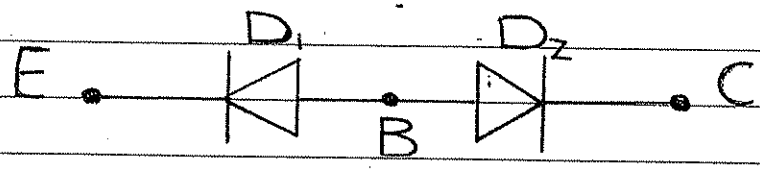
There are four Operating modes (Regions):

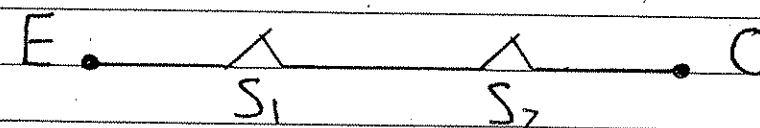
1] Saturation mode :

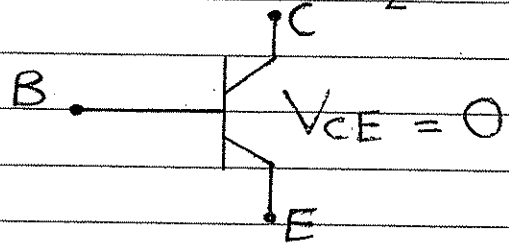
(B-E Jn.) & (B-C Jn.) must be (F.W Biased).

BJT works as a Closed - Switch.





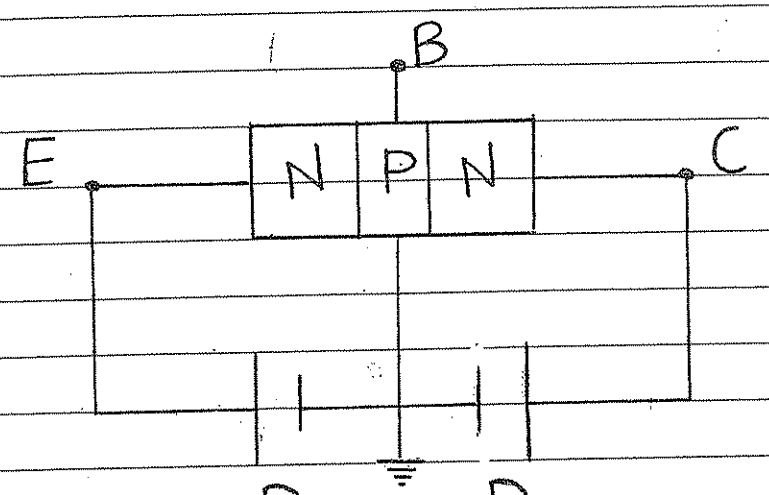


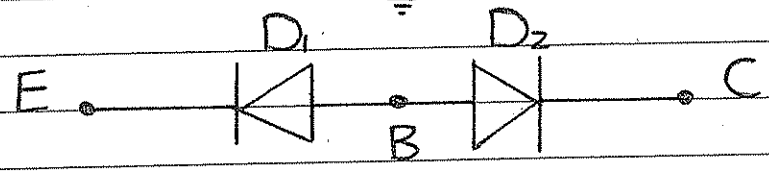


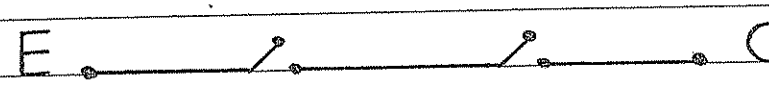
2] Cut-off mode :-

Both Jns. are (Reversed-Biased).

BJT works as open Switch.





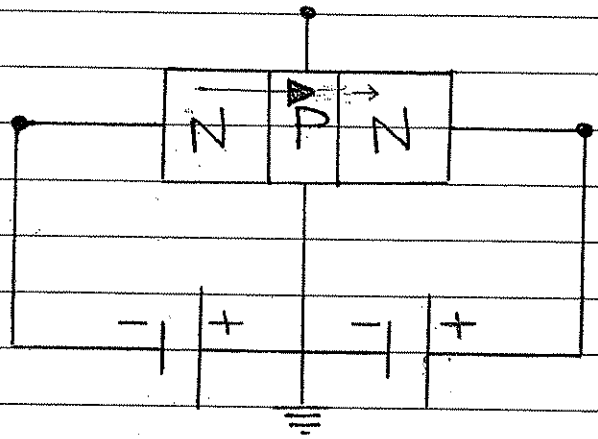


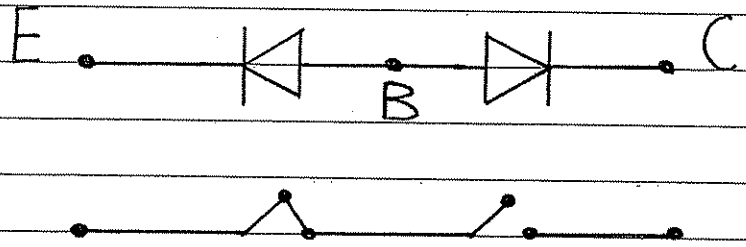
$I_C = 0$; $I_E = 0$

3] Forward - ACtive mode (FAM) :-

- B-E Jn. → F.W.
- B-C Jn. → ReV.

BJT works as an Amplifier to maghify the AC input Signal.

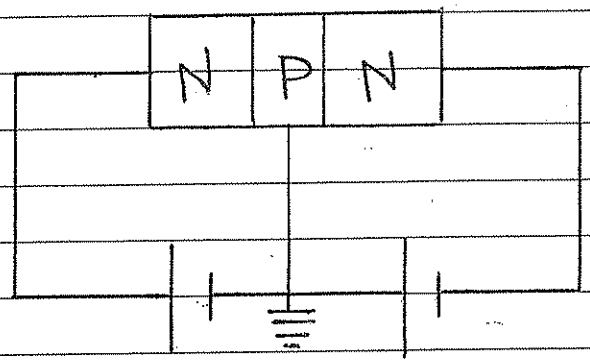




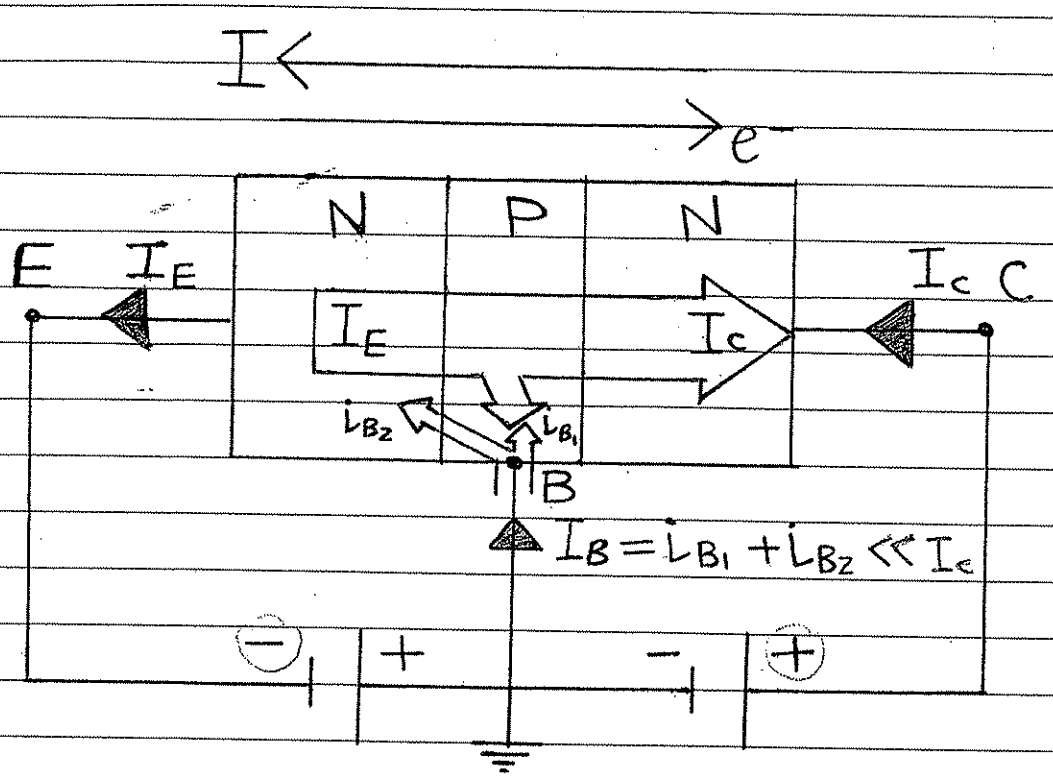
4] Inverse Forward-Active mode :

- B-E Jn. ⟶ Rev.
- B-C Jn. ⟶ F.W.

It has certain applications in digital electronics.



✳ F.A.M Operation for NPN :



II Due to F.W biasing of B-E Jn. the maj. Carriers will be forced to Cross B-E Jn., Some of them (Very Small components) will be lost in base by recombination.

The maj. component will be Collected in Collector due to electric field at Collector.

2] The Base will drive two Components.

i_{B_1} : Compensating Component.

i_{B_2} : diffusion Component.

* $I_B = i_{B_1} + i_{B_2}$ and $(I_B \ll I_C)$.

Current in BJT (F.A.M) :-

$$I_E = I_{E_0}\left(e^{\frac{V_{BE}}{VT}} - 1\right)$$

$$I_E = I_{E_0}\, e^{\frac{V_{BE}}{VT}}$$

$I_{E_0} = 10^{-16} \rightarrow 10^{-14}$ A

$$I_C = I_{C_0}\, e^{\frac{V_{BE}}{VT}}$$

$$I_B = I_{B_0}\, e^{\frac{V_{BE}}{VT}}$$

Since I_E, I_C, I_B are exponentially related to V_{BE} so I_E, I_C, I_B are linearly related to each other :-

$$I_E = I_C + I_B \quad (1)$$

$$I_C = \beta I_B \quad (2)$$

$$I_E = \beta I_B + I_B = (\beta + 1) I_B \quad (3)$$

$$I_E = I_C + \frac{I_C}{\beta} = I_C \left(1 + \frac{1}{\beta}\right)$$

$$= I_C \left(\frac{\beta + 1}{\beta}\right)$$

$$I_C = \left(\frac{\beta}{\beta+1}\right) I_E = \alpha I_E \quad (4)$$

* Valid on F.A.M only.

Where:

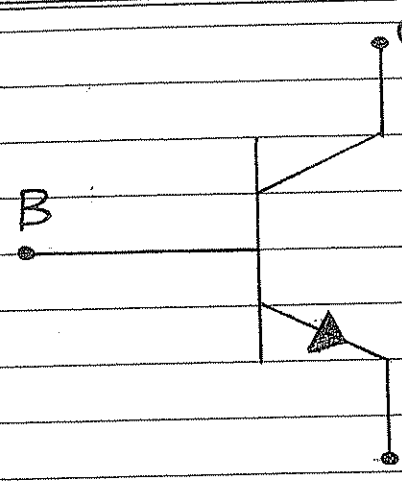
β: Current-Gain in C.E Amp. → given in data sheet.

$$50 < \beta < 300$$

α: Current-ratio in C.B Amp..

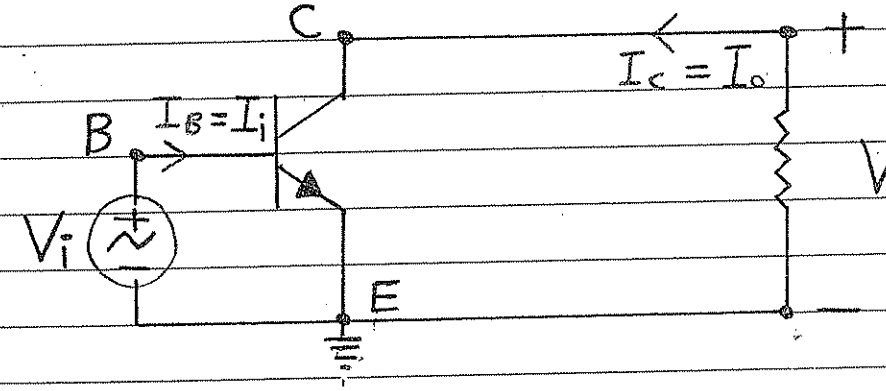
$$0.95 < \alpha < 1$$

*(BJT) Configuration (Connections) :-



Three Configuration according to Common Terminal :-

1) Common Emitter Amp. :



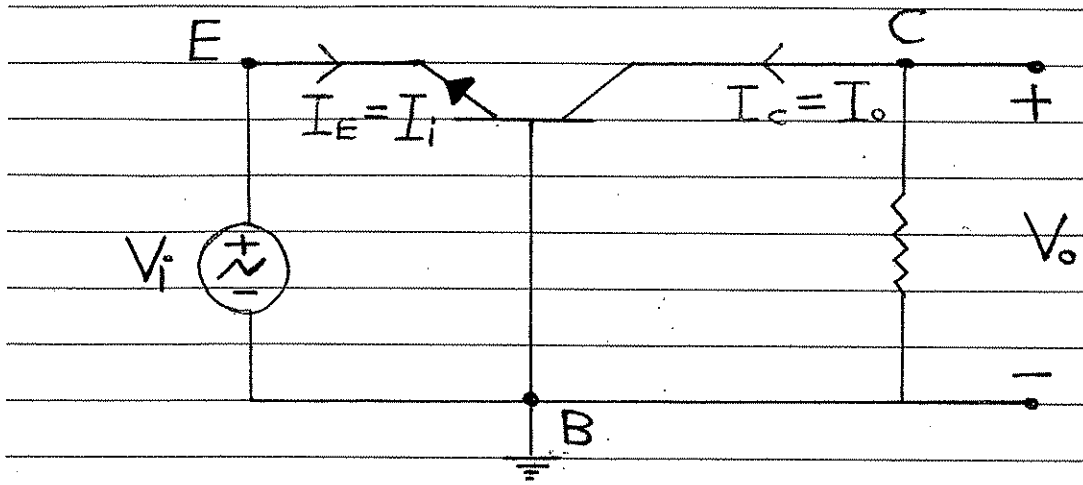
E :→ Common.

Input to base.

Out put from Collector.

Current-gain : $A_I = \frac{I_o}{I_i} = \frac{I_c}{I_B} = \beta$

3 Common Base Amp. :



Base :→ Common terminal.

Input to E.

output from C.

Current-gain $= A_I = \frac{I_o}{I_i} = \frac{I_c}{I_E} = \alpha$

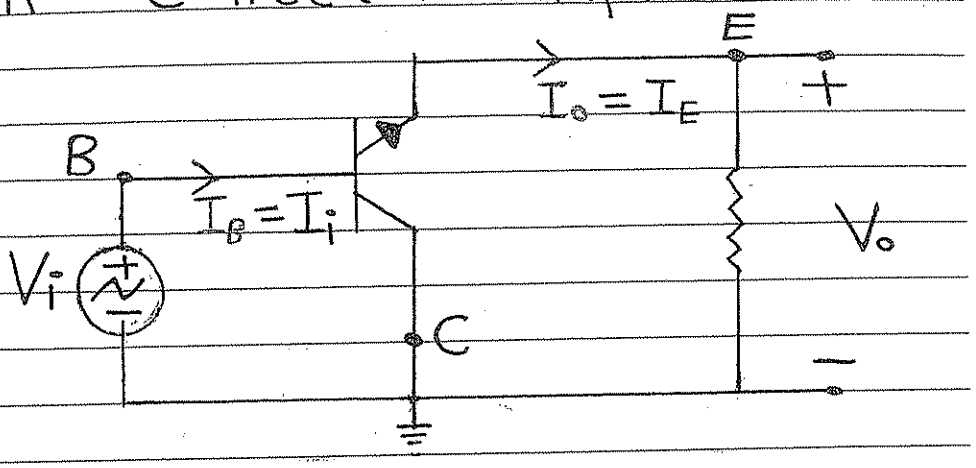
$$\alpha = \frac{\beta}{\beta + 1}$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

For $\beta = 49 \rightarrow \alpha = \frac{49}{49+1} = 0.98$

For $\alpha = 0.89 \rightarrow \beta = \frac{0.98}{1-0.98} = 49$

3) Common – Collector Amp. :-



C :→ Common.

Input to Base.

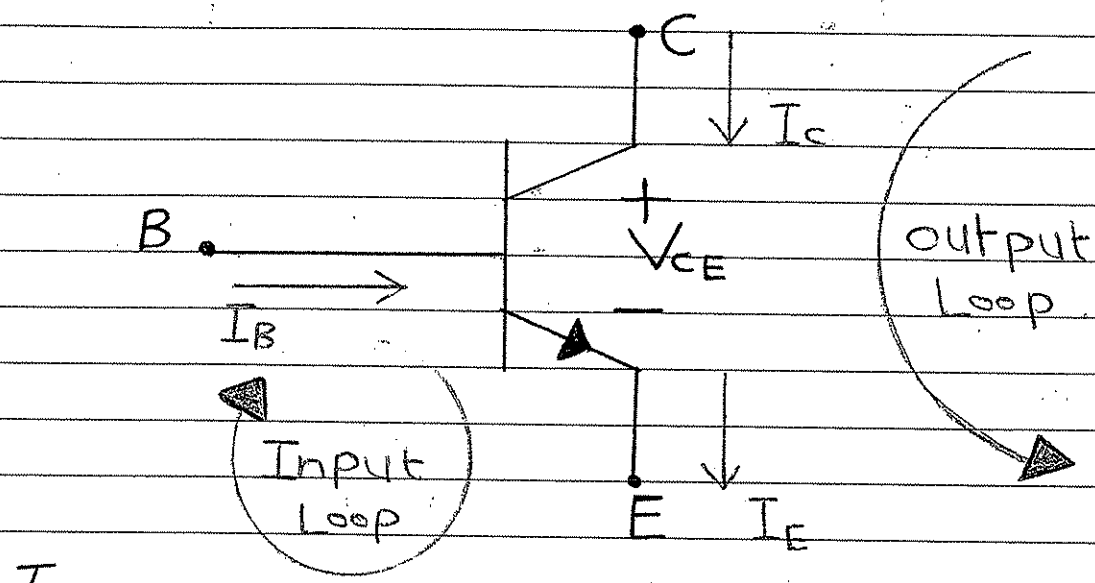
Output from E.

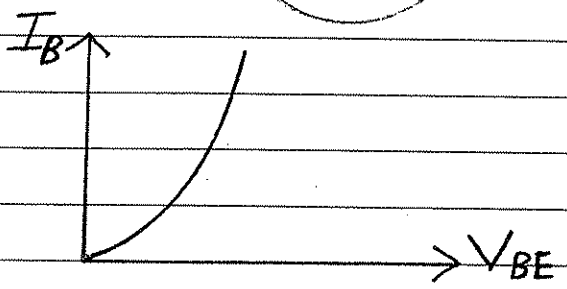
Current-gain : $A_I = \frac{I_E}{I_B} = \frac{(\beta+1) I_B}{I_B}$

$\rightarrow A_I = \beta + 1$

* Current - Voltage Characteristics :-

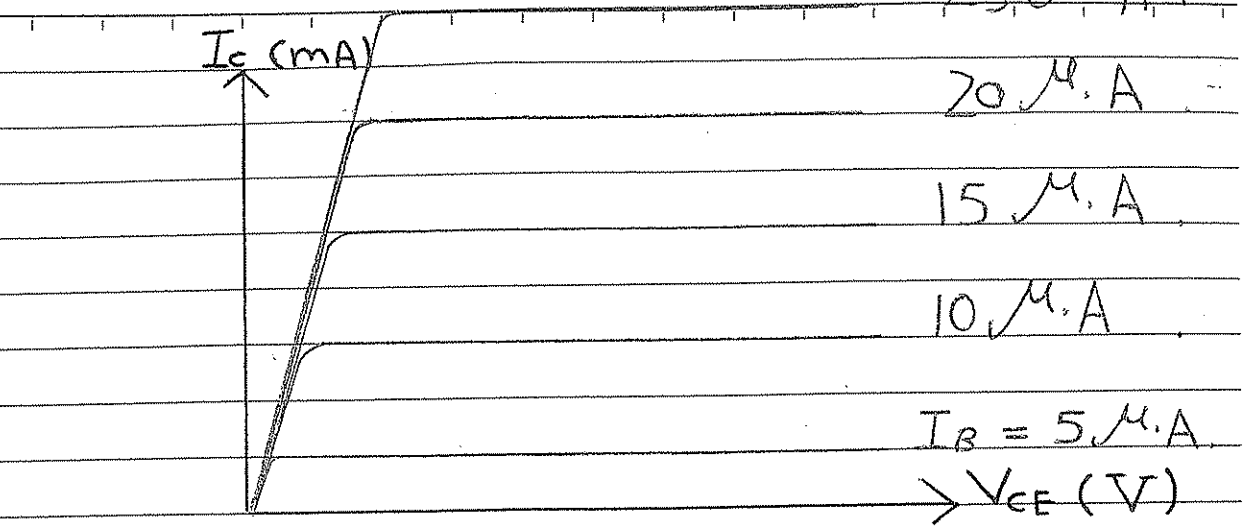
of NPN BJT as C.E Amp :-

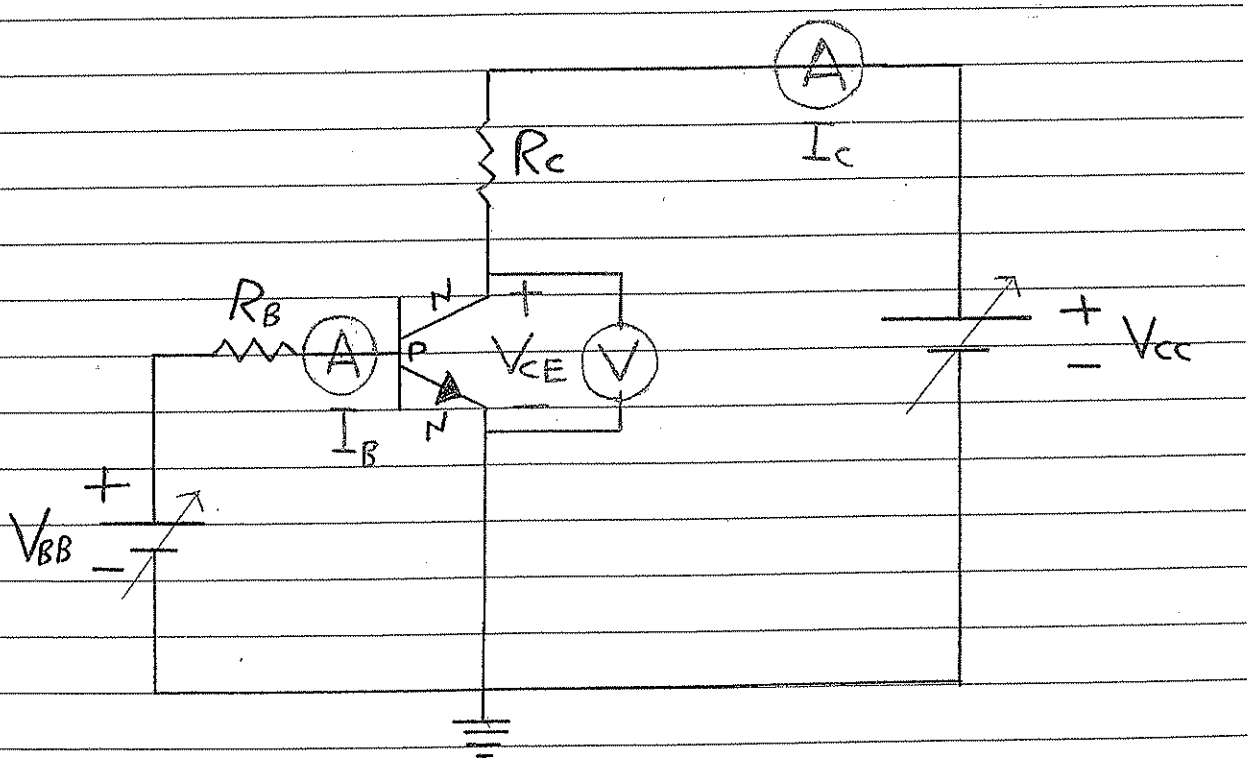




output C/C :

aplot of I_c Versus V_{cE}, for Certain Values of I_B .


25 μ.A
20 μ.A
15 μ.A
10 μ.A
I_B = 5 μ.A
I_C (mA)
V_{CE} (V)


A
I_C
R_C
R_B
A
I_B
N
P
N
V_{CE}
V
+
V_{CC}
−
+
V_{BB}
−

Break down Voltage :-

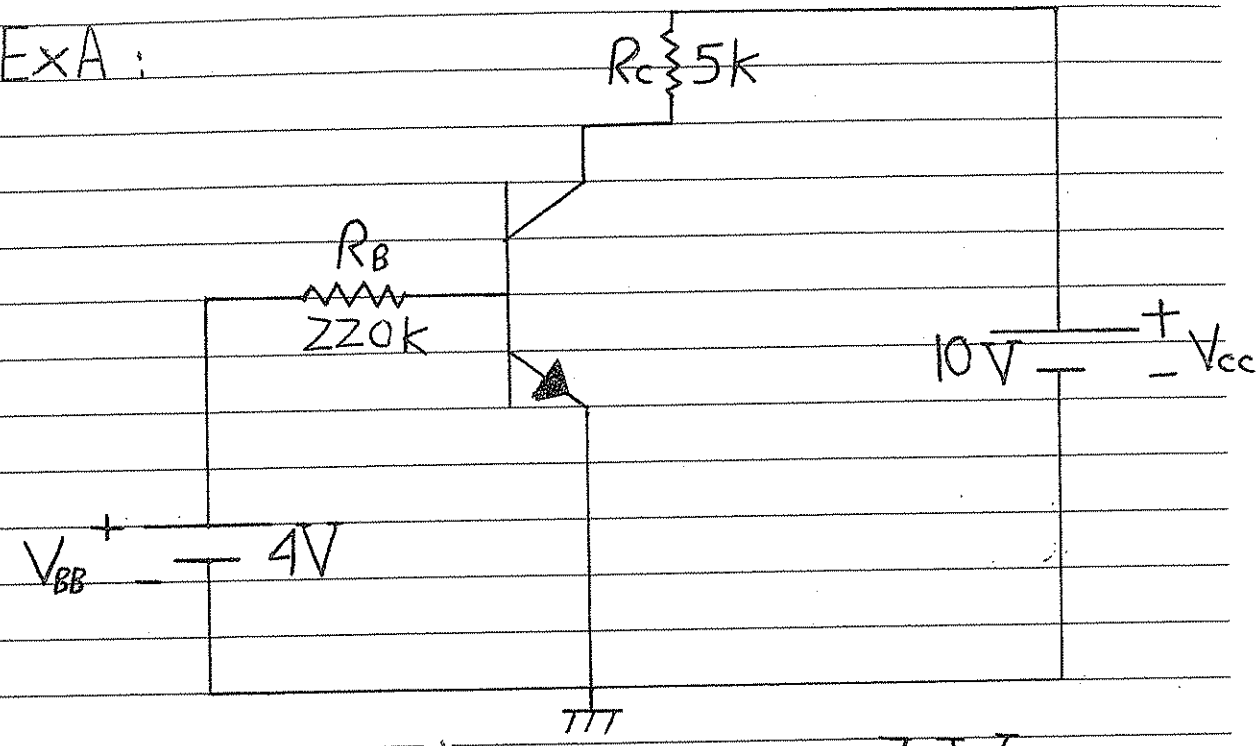
We can't increase V_{CE} indefinitly we must a void (BV_{CE_o}), Break down Value of V_{CE} When Base is open.

↳ base is open.

* BV_{CE_o} : given in data Sheet.

5.2: DC Analysis of BJT Circuits:-

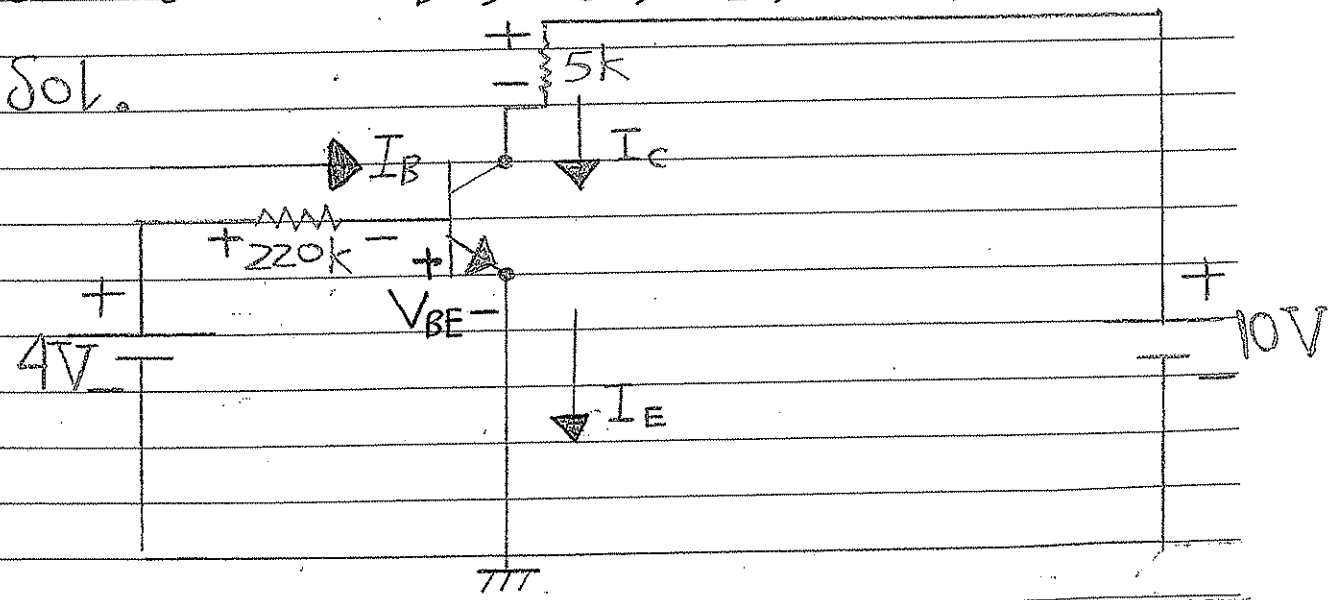
Ex A:



Given: $\beta = 100$, $V_{BE} = 0.7\,V$.

Calculate I_B, I_C, I_E, V_{CE}, P_D.

Sol.



Assume the BJT in F.A.M :-

* KVL for B-E Loop :

$$-V_{BB} + I_B R_B + V_{BE} = 0$$

$$I_B = \frac{(4 - 0.7)\ V}{220\ k} = \frac{3.3\ V}{220\ k}$$

$$= 15\ \mu A.$$

$$I_C = \beta I_B = 100 * 15 = 1.5\ mA.$$

$$I_E = (\beta + 1) I_B = 1.515\ mA.$$

* V_{CE} ?

KVL for C-E Loop :

$$-10 + I_C R_C + V_{CE} = 0$$

$$V_{CE} = 10 - (1.5 * 5) = 2.5\ V.$$

Cheak :

& Since $I_B > 0$: ∴ B-E Jn. F.W.

Since $V_{CE} > V_{BE}$: ∴ B-C Jn. Rev.

⇒ BJT is in F.A.M.

P_D = Power dissipation in BJT

$$\boxed{P_D = I_B \cdot V_{BE} + I_C \cdot V_{CE}}$$

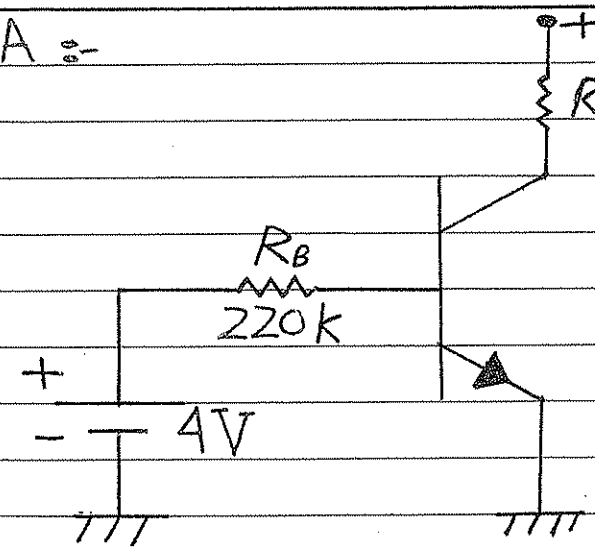
Since: $I_B \ll I_C$ and $V_{BE} < V_{CE}$:-

$\therefore I_B V_{BE} \ll I_C V_{CE}$

$\rightarrow P_D \simeq I_C \cdot V_{CE}$

$= 1.5 * 2.5 = 3.75$ mW.

Ex A :-



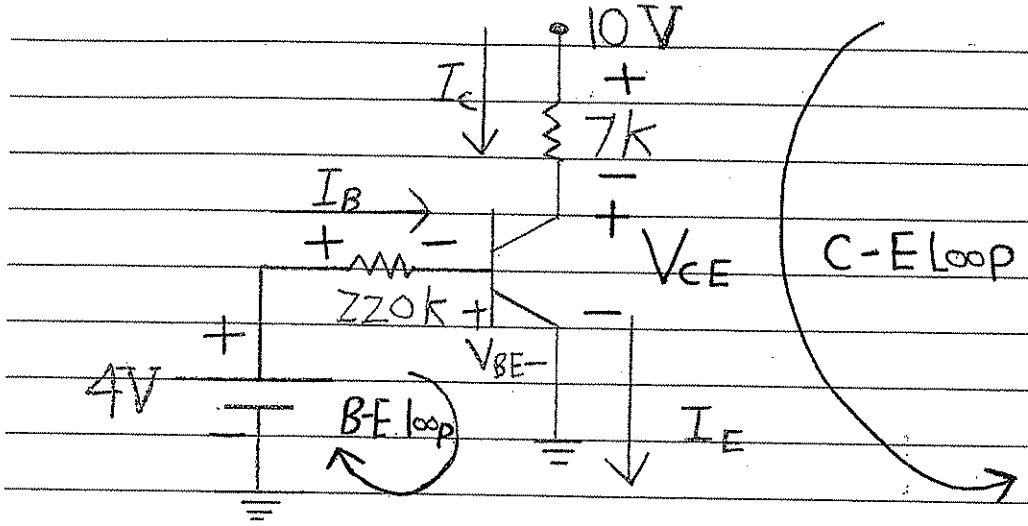
Given : $V_{BE}(ON) = 0.7$ V, $\beta = 100$,

$V_{CE}(Sat.) = 0.2$ V.

Find : I_B, I_C, I_E, V_{CE}, P_D ?

Sol.:

Assume the BJT in F.A.M :-



*KVL for B-E Loop :

$$-4 + I_B R_B + V_{BE} = 0$$

$$I_B = \frac{(4 - 0.7)}{220k} = \frac{3.3\ V}{220k} = 0.015\ mA.$$

$$I_c = \beta I_B = 100 * 0.015 = 1.5\ mA$$

→ V_{CE} ?

*KVL for C-E Loop :

$$-V_{cc} + I_c R_c + V_{CE} = 0$$

$$V_{CE} = 10 - 1.5\ mA * 7k = 10 - 10.5$$

$$= -0.5\ V.$$

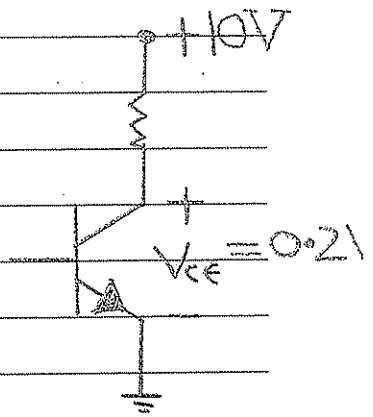
Since :

* $V_{CE} < V_{BE}$ ∴ B-C Jn. is F.W.

&

* $I_B > 0$ ∴ B-E Jn. is F.W.

⇒ BJT is in Saturation mode.



∴ $V_{CE} = V_{CE(sat.)} = 0.2\ V$

$I_B = 0.015\ mA.$

→ I_C ⇒ from C-E loop :

$-10 + I_C R_C + 0.2 = 0$

$I_C = I_{C(sat.)} = \frac{(10-0.2)\ V}{7\ k} = \frac{9.8\ V}{7\ k}$

$= 1.4\ mA.$

$I_E = I_C + I_B = 1.4 + 0.015$

$= 1.415\ mA.$

* $P_D = I_B V_{BE} + I_C V_{CE}$; In Sat. mode: $V_{CE} < V_B$
$I_B \ll I$ ليس اقل بكثير

∴ $P_D = I_B V_{BE} + I_{C(sat.)} \cdot V_{CE(sat.)}$

$= 0.015 * 0.7 + 1.4 * 0.2$

$= 0.0105 + 0.28$

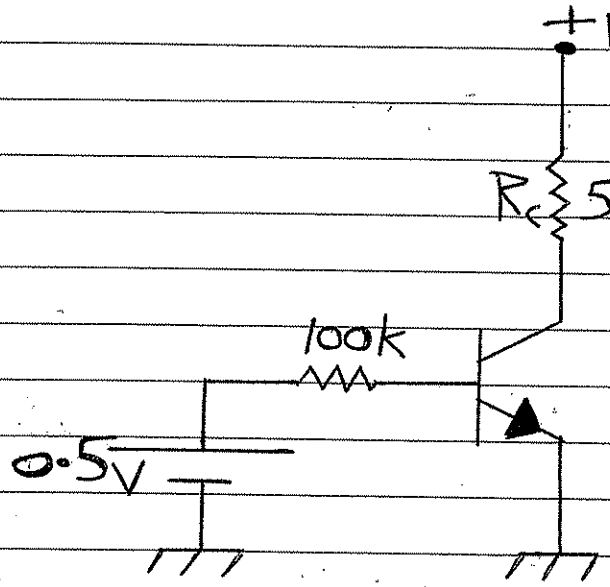
$= 0.2905\ mW.$

Ex A :-

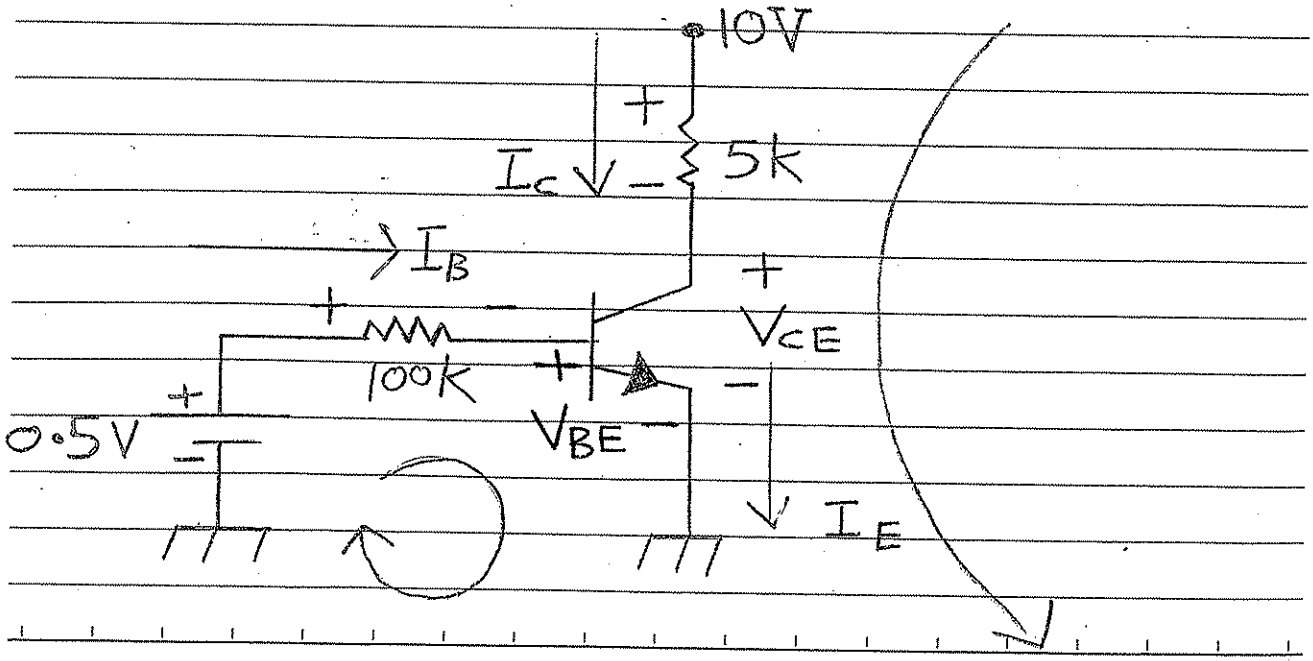
Given : $\beta = 100$, $V_{BE} = 0.7\ V$,

$V_{CE(sat.)} = 0.3\ V$.

Find I_B , I_C , I_E , V_{CE} , P_D .



Sol. Assume the BJT in F.A.M :



$$-0.5 + 100\, I_B + V_{BE} = 0$$

$$I_B = \frac{(0.5 - 0.7)\ V}{100\ k}$$

$$= -2\ \mu A .$$

Since $I_B < 0$:

$\therefore$ B-E Jn. is Rev.

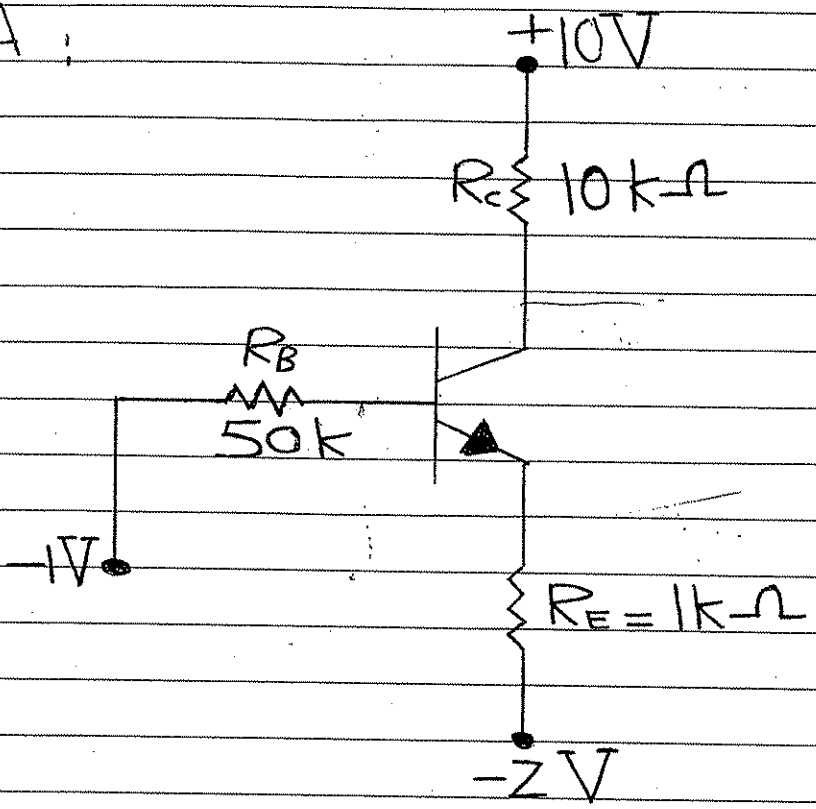
$\Rightarrow$ BJT is in Cut-OFF Mode.

So: $I_B = I_C = I_E = 0$

$$-10 + I_C R_C + V_{CE} = 0$$

$\therefore$ $V_{CE} = 10\ V$.

Ex A :



Given : $\beta = 49$, $V_{BE} = 0.7\,V$,

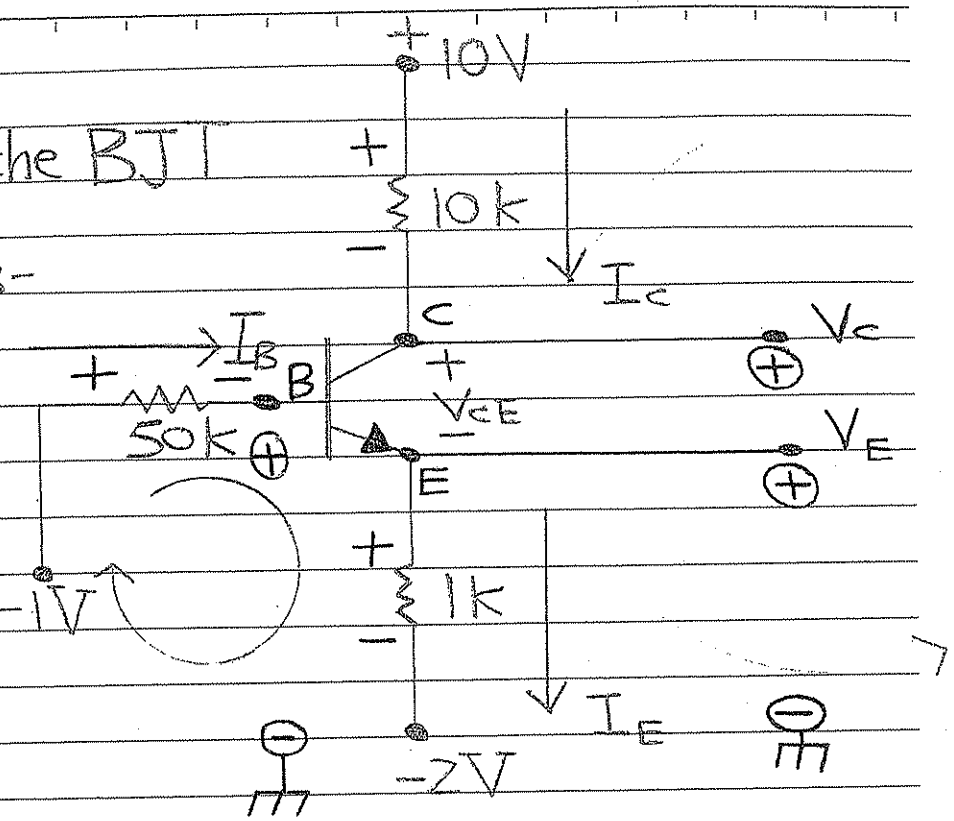
$V_{CE(sat.)} = 0.2\,V$.

Find : I_B , I_C , I_E , V_B , V_C , V_E ,

V_{CE} , P_D .

Sol.

Assume The BJT in F.A.M :-



$$1 + I_B R_B + V_{BE} + I_E R_E - 2 = 0$$

But : $I_E = (\beta + 1) I_B$

$$\rightarrow 1 + I_B R_B + V_{BE} + (\beta + 1) I_B R_E - 2 = 0$$

$$I_B = \frac{(2 - 1 - 0.7)\,V}{R_B + (\beta + 1) R_E}$$

$$= \frac{0.3V}{50k + 50 * 1} = \frac{0.3V}{100k} = 3\,\mu A.$$

$$I_C = \beta I_B = 3 * 49 = 0.147\,mA.$$

$V_{CE} = ?$

$-10 + I_C R_C + V_{CE} + I_E R_E + 7 = 0$

$V_{CE} = 10 + 7 - I_C R_C - I_E R_E$

$= 17 - I_C R_C - I_E R_E$

$* I_E = (\beta + 1) I_B = 50 * 3. = 0.15\ mA.$

$\therefore V_{CE} = 17 - (0.147 * 10k) - (0.15 * 1k)$

$= 12 - 1.47 - 0.15 = 10.38\ V.$

Since :

$V_{CE} > V_{BE} \rightarrow$ BC. Jn Rev.

& $I_B > 0$, $\rightarrow$ BE. Jn F.W.

$\therefore$ BJT is in FAM.

$V_c = ?$

$-10 + I_c R_c + V_c = 0$

$V_c = 10 - 0.147 * 10 = 8.53\,V.$ #

$V_E = ?$

$-V_E + I_E R_E - 2 = 0$

$V_E = I_E R_E - 2 = 0.15 * 1 - 2 = -1.85\,V.$ #

$V_B = ?$

$1 + 50k * 3.\mu + V_B = 0$

$V_B = -1 - 0.003 * 50 = 1 - 0.15$

$= -1.15\,V.$ #

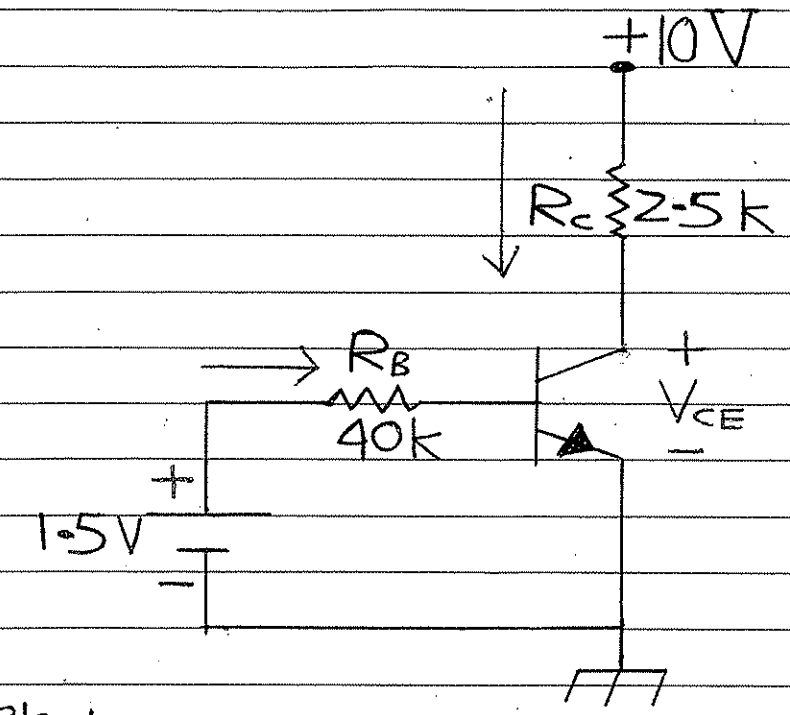
$P_D = I_B V_{BE} + I_c V_{CE}$

$= (0.003 * 0.7) + (0.147 * 10.38)$

$= 0.0021 + 1.5$

$= 1.5021\ mW.$ #

* DC Load Line , Q-Point :-



Given :

$\beta = 100$, $V_{BE} = 0.7\,V$, $V_{CE(sat)} = 0.2V$

* D.C.L.L :- a Straight line relates I_c to V_{CE} for the BJT in a Certain Circuit.

It is draw on Transistor O/P C/C.

It has a slope equal to : $\frac{-1}{R_{D.C}}$.

Where:

R_{DC} : Total resistance in output loop. (CE-loop).

* KVL for CE-Loop :-

$$-V_{CC} + I_C R_C + V_{CE} = 0$$

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} \quad \text{1} \rightarrow \text{D.C.L.L equation.}$$

$y = b + mx$; $m = \text{Slope} = \frac{-1}{R_C}$

or:

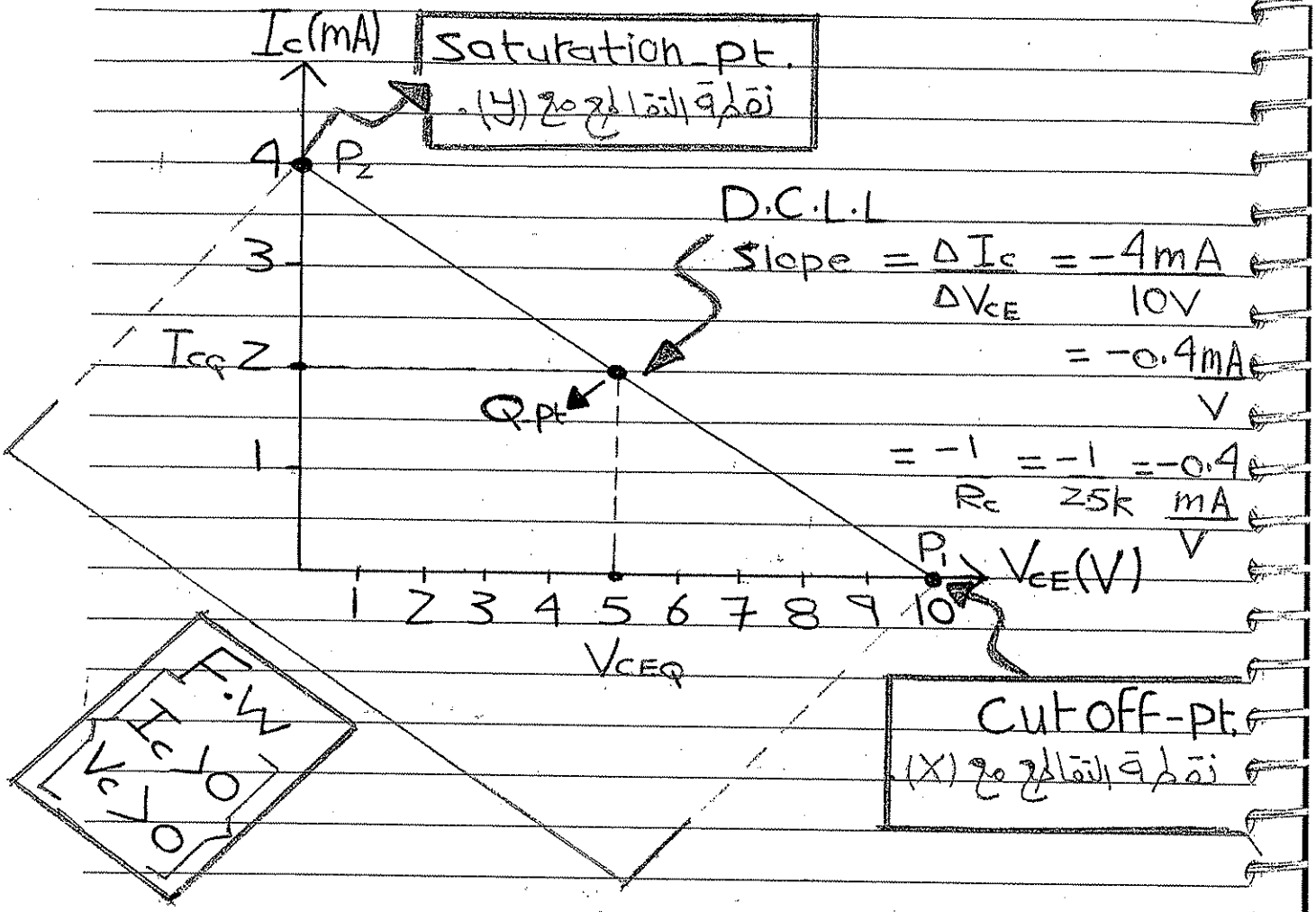
$$V_{CE} = V_{CC} - I_C R_C \quad \text{2} \rightarrow \text{D.C.L.L equation.}$$

* How to Draw (D.C.L.L) P:-

from 2:

i) For $I_C = 0$, $V_{CE} = V_{CC}$: $P_1(10V, 0)$

ii) For $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C}$: $P_2(0, 4mA)$

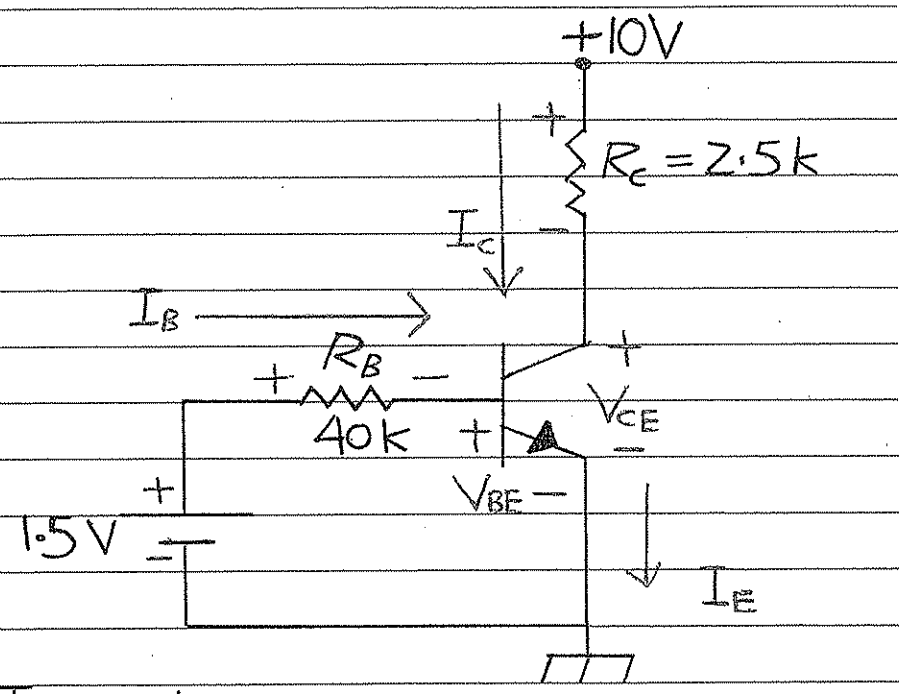


* Q-Point (Operating point):
The Value of (I_c) and (V_{CE}) for the BJT in the circuit.

How to Find Q-point Values ?:

* From D.C Analysis :-

Assume FAM Operation



$$-1.5 + 40 I_B + V_{BE} = 0$$

$$I_B = \frac{(1.5 - V_{BE})}{40k} = \frac{0.8}{40k} = 0.02\ mA = I_{BQ}$$

$$I_c = \beta I_B = 100 * 0.02 = 2\ mA = I_{cQ}$$

$$-10 + I_c R_c + V_{CE} = 0$$

$$V_{CE} = 10 - 2 * 2.5 = 5V = V_{CEQ}$$

$Q\text{-}pt = (V_{CEQ}, I_{CQ})$

$= (5V, 2mA)$.

In FAM :-

IF $R_B \uparrow$: $I_B \downarrow$, $I_C \downarrow$ and Q-Pt : Down.

IF $R_C \uparrow$:

Slope تتغير — I_C : لايتغير $I_C = \beta I_B$

Q-Pt : Left.

Q-Pt
- V_{CE}
- V_{CC}
- R_C

* تؤثر على حركتها لليمين أو لليسار .

- I_B
- R_B
- I_C

* تؤثر على حركتها لأعلى أو لأسفل

IF $V_{CE} \uparrow$: R_C ثابت and Q-Pt : right.

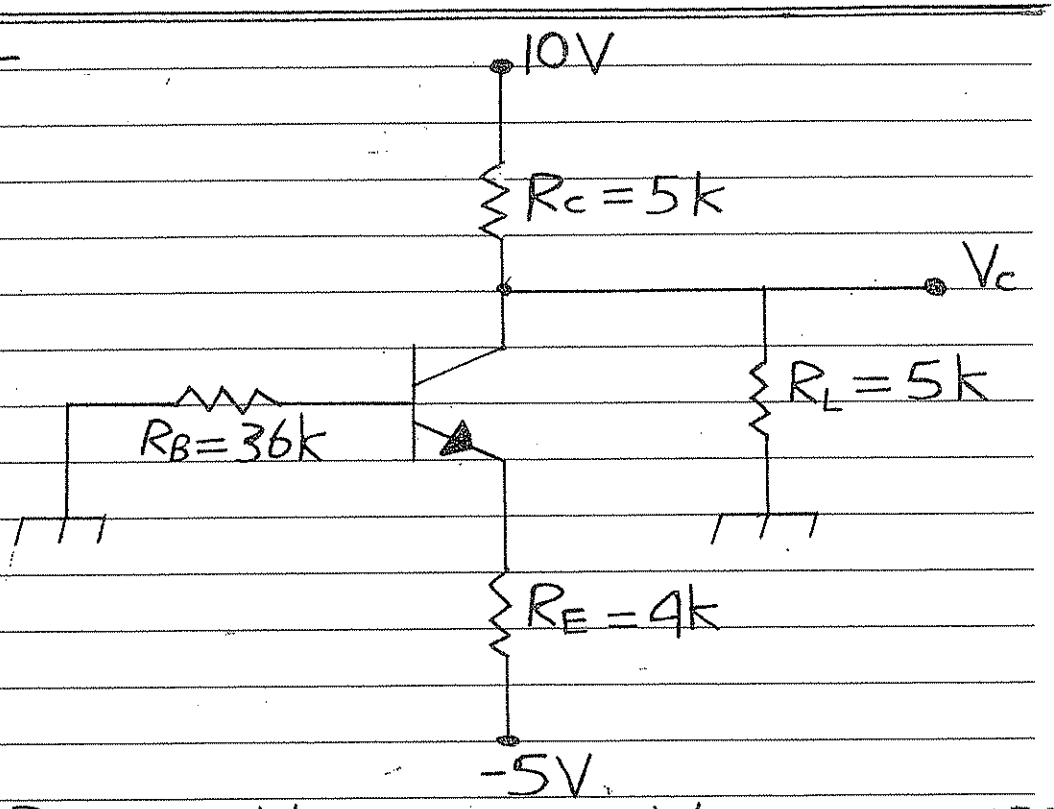
كل شيء في input Loop يؤثر على Q-Pt لأعلى أو لأسفل	كل شيء في out Put Loop يؤثر على Q.Pt لليمين أو لليسار .

In Sat. Mode :

If $R_B \downarrow$: I_C ثابت ، $V_{CE(sat)}$ ثابت

∴ Q-pt : نقطة على (y) ثابتة ولا تتغير.

EXA. :-

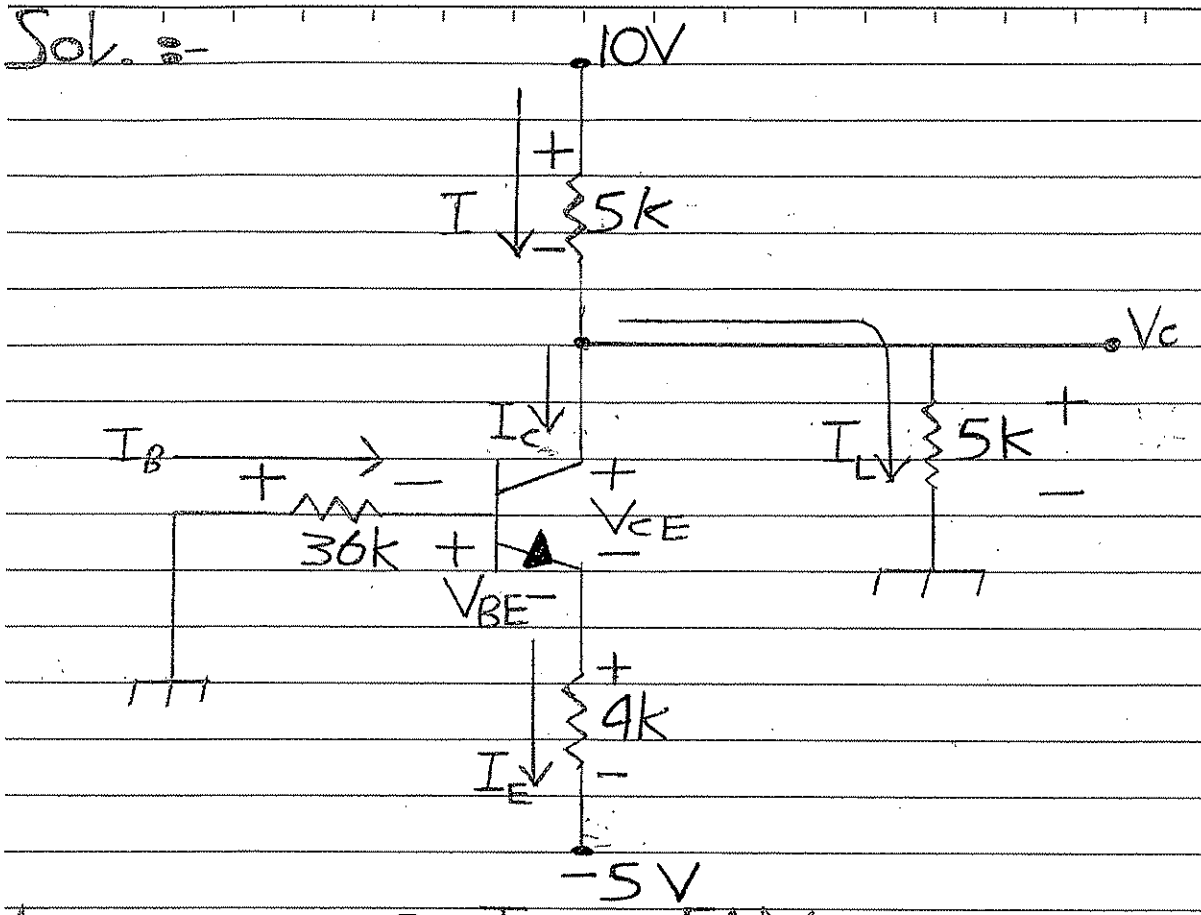


Given: $B = 100$, $V_{BE} = 0.7V$, $V_{CE(sat)} = 0.3V$

1) Calculate Q-Pt Values (I_{BQ}, I_{CQ}, V_{CEQ}).

2) Draw D.C.L.L , indicate Q-Pt and Slope.

Sol. :-



1)

Assume the BJT in FAM :-

$$R_B I_B + V_{BE} + I_E R_E - 5 = 0$$

$$I_E = (\beta+1) I_B$$

$$\Rightarrow I_B(R_B + (\beta+1) R_E) + V_{BE} - 5 = 0$$

$$I_B = \frac{5 - V_{BE}}{36 + (101 * 4)} = \frac{4.3}{440K} = 9.7 \mu A.$$

$$I_C = \beta I_B = 100 * 9.7 = 0.97 mA.$$

V_{CE} ?

$-10 + 5I + V_{CE} + 4I_E - 5 = 0$

$\rightarrow I_E = (\beta+1) I_B = 0.87\,mA.$

$\therefore V_{CE} = 15 - 0.87 * 4 - 5I$

$$\boxed{V_{CE} = 11.5 - 5I}$$

$I = I_C + I_L$

$$\frac{10 - V_c}{R_c} = 0.86 + \frac{V_c}{R_L}$$

$$\frac{10 - V_c}{5} = 0.86 + \frac{V_c}{5}$$

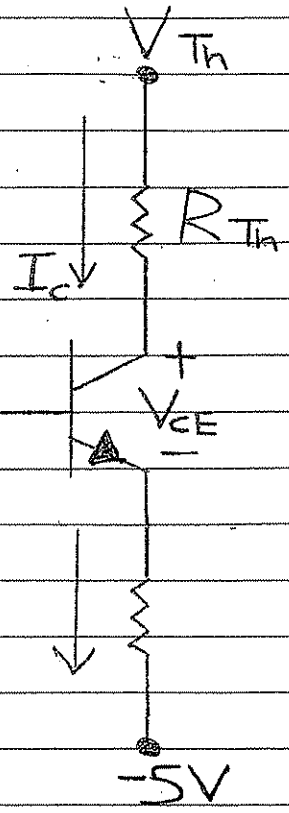
$10 - V_c = 4.3 + V_c \rightarrow V_c = \frac{5.7}{2} = 2.85V.$

$I = \frac{10 - 2.85}{5} = 1.43\,mA.$

$V_{CE} = 11.5 - 1.43 \times 5 = 4.4V$; FAM.

$I_L = \frac{V_c}{R_L} = \frac{2.85}{5k} = 0.57\,mA.$

2)



$R_{Th} = R_c // R_L = 5 // 5 = 2.5k.$

$V_{Th} = \frac{10 * R_L}{R_L + R_c} = 5V.$

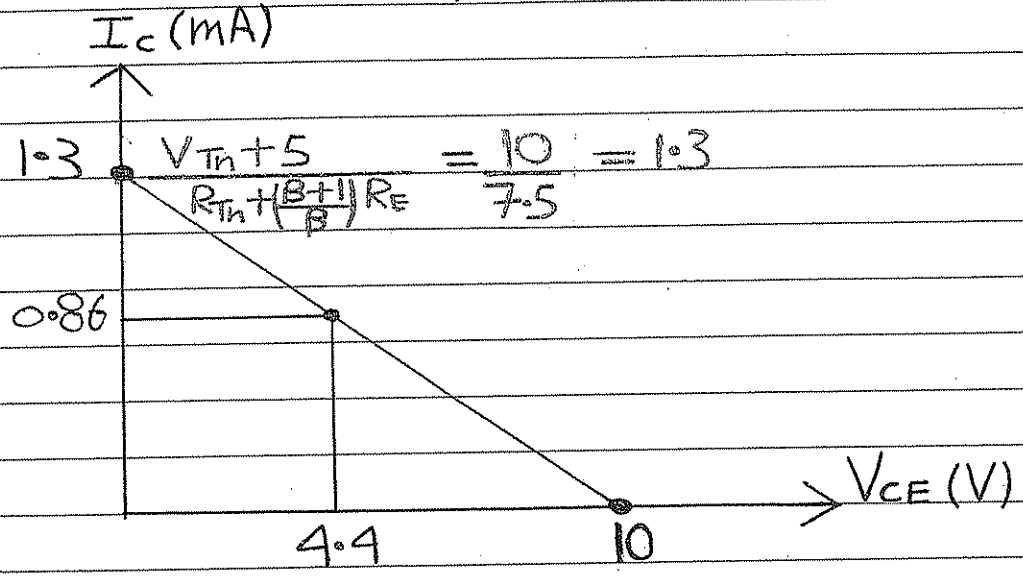
$\rightarrow -V_{Th} + I_c R_{Th} + V_{CE} + I_E R_E - 5 = 0$

$$\boxed{I_E = \frac{I_c}{\alpha} = \left(\frac{\beta+1}{\beta}\right) I_c}$$

Assume $\beta \gg 1$: $\boxed{I_E = I_c}$

$$V_{CE} = V_{Th} + 5 - I_C\left(R_{Th} + \left(\frac{B+1}{B}\right)R_E\right)$$ D.C.L.L eqn.

$$\text{Slope} = \frac{-1}{R_{Th} + \left(\frac{B+1}{B}\right)R_E}$$



هناك في مجتمعي ...

اذا تقدم شاب فقير وتقي لخطبة فتاة ميرفضه أهلها ،

واذا تقدم فاسد غني لخطبتها يقبلون ويقولون: سبحان الله!

أليس الهادي هو نفسه الرزاق؟.

* Biasing of BJT :-

1) Single-Base Resistor Biasing :-

Note :

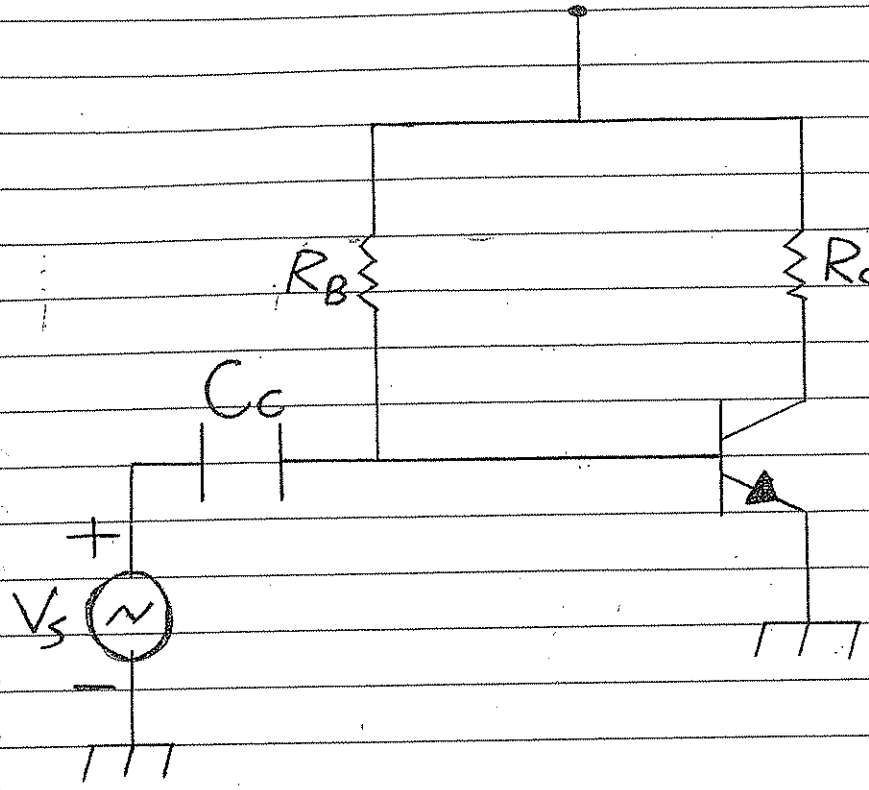
1- Biasing : Applying DC Voltage to active devices (Diode, BJT, FET, OP-Amp.) to force it to work in a certain mode.

2- $X_c = \frac{1}{2\pi f C}$

For DC Bias : $f = 0$, $X_c = \infty$

$\therefore$ C : open.

For AC Bias : $X_c \simeq 0$



C_C : Coupling Capacitor.

Coupling for A.C signal ($X_C = 0$) : S.C.

Blocking for D.C signal ($X_C = \infty$) : O.C.

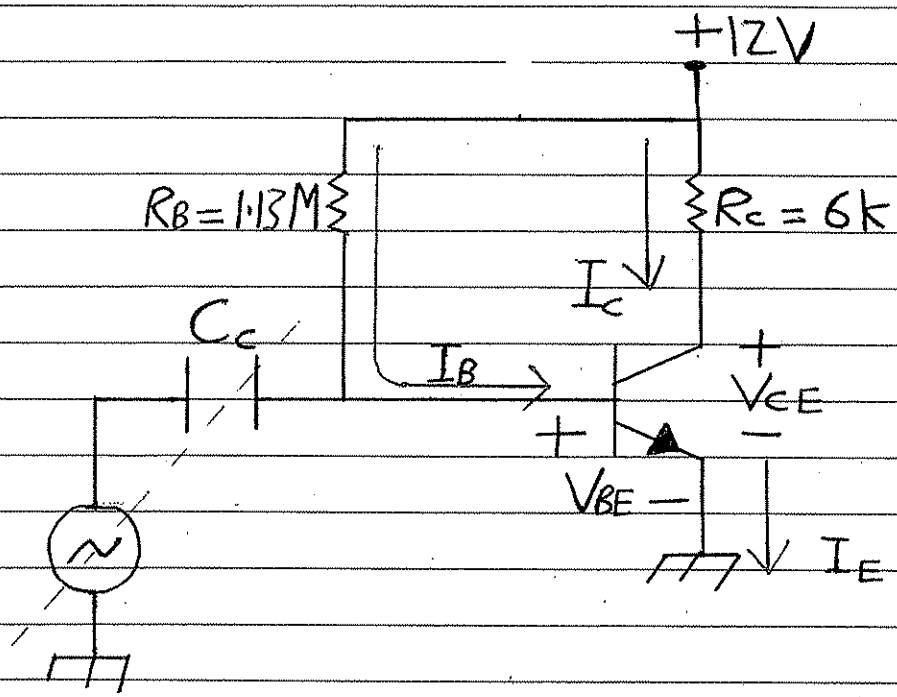
EXA:

Given: $V_{cc} = 12\,V$, $R_c = 6k\Omega$, $R_B = 1.13\,M\Omega$

$V_{BE} = 0.7V$, $V_{CE(sat)} = 0.3\,V$.

Calculate: I_{cq}, V_{CEQ}, $\Delta I_{cq}\%$, $\Delta V_{CEQ}\%$

When $B = 100, 200$ and Comment.



Sol. Assume the BJT in FAM:

$$-V_{cc} + I_B R_B + V_{BE} = 0$$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B} = \frac{(12 - 0.7)\,V}{1.13\,M\Omega}$$

$$= \frac{11.3}{1.13M} = 10\,\mu A = I_{BQ}$$

1) For $\beta = 100$:

$I_{CQ} = \beta I_{BQ} = 100 * 10 = 1mA$.

$-V_{CC} + I_{CQ}R_C + V_{CE} = 0$

$V_{CEQ} = 12 - (1*6) = 6V$.

∴ BJT In FAM .

2) For $\beta = 200$:

$I_{CQ} = 200 * 10 = 2mA$.

$V_{CEQ} = 12 - (2*6) = 0V$.

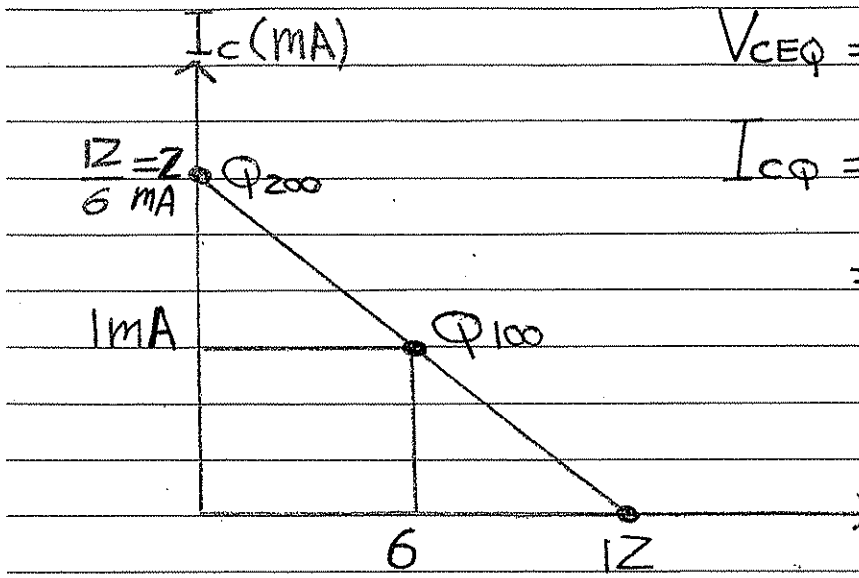
∴ BJT In Sat. .

$\Delta I_{CQ}\% = \frac{2-1}{1} * 100\% = 100\%$.

$\Delta V_{CEQ}\% = \frac{0-6}{6} * 100\% = -100\%$.

I_B ثابت $\rightarrow \beta\uparrow$ ، $I_C\uparrow$

تزيد وتقل بنفس النسبة



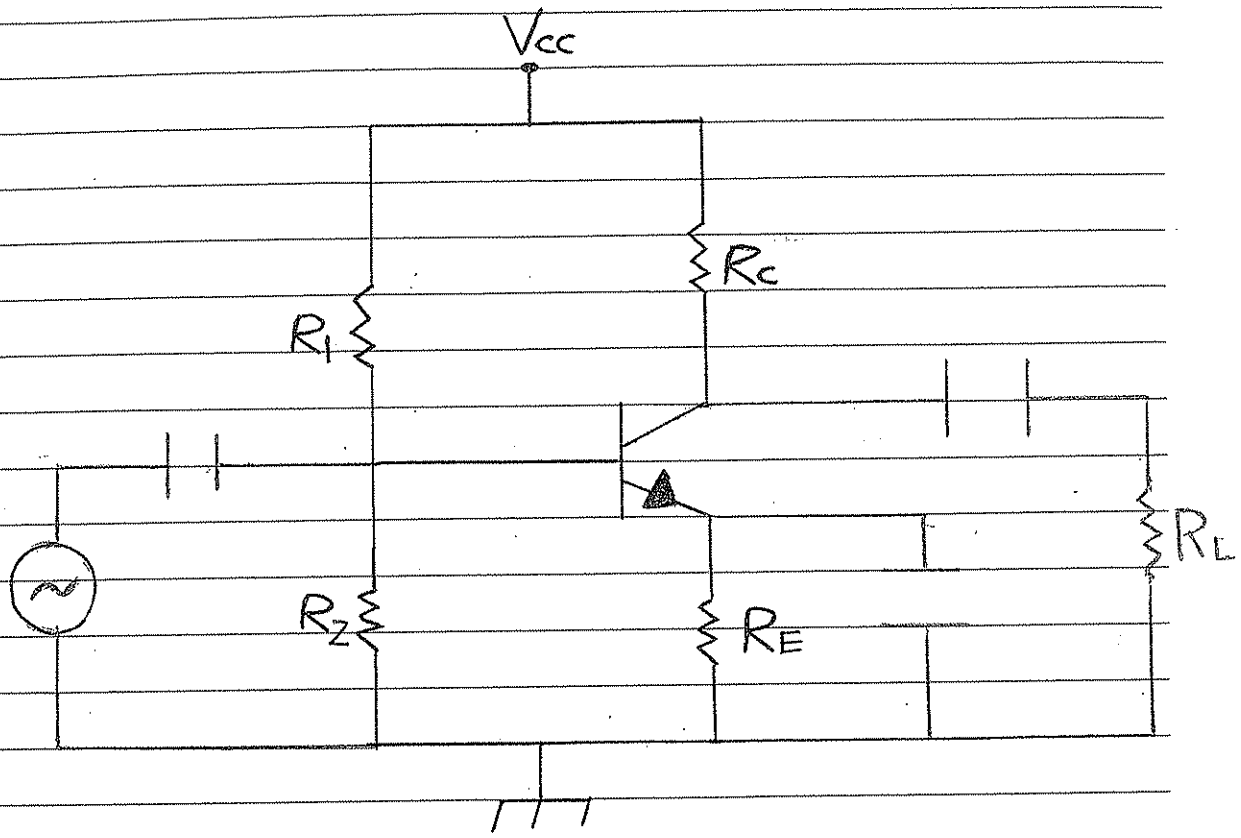
$$V_{CEQ} = V_{CE(sat)} = 0.3V$$

$$I_{CQ} = I_{C(sat)}$$

$$= \frac{12 - 0.3}{6} = 1.95 \text{ mA}$$

∴ This Circuit is Very Sencetive to β Variation, and has a bad bias-Stability.

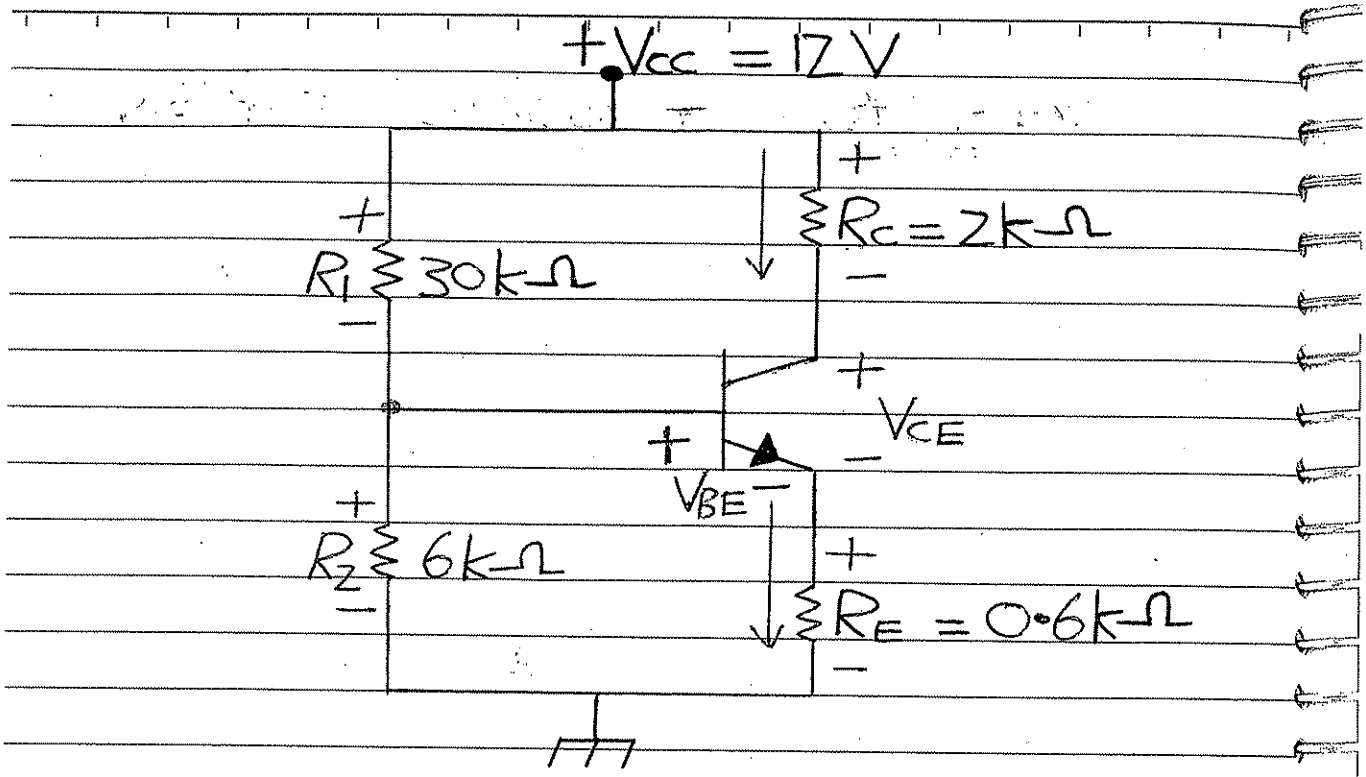
2) Voltage - Divider biasing Circuit :-



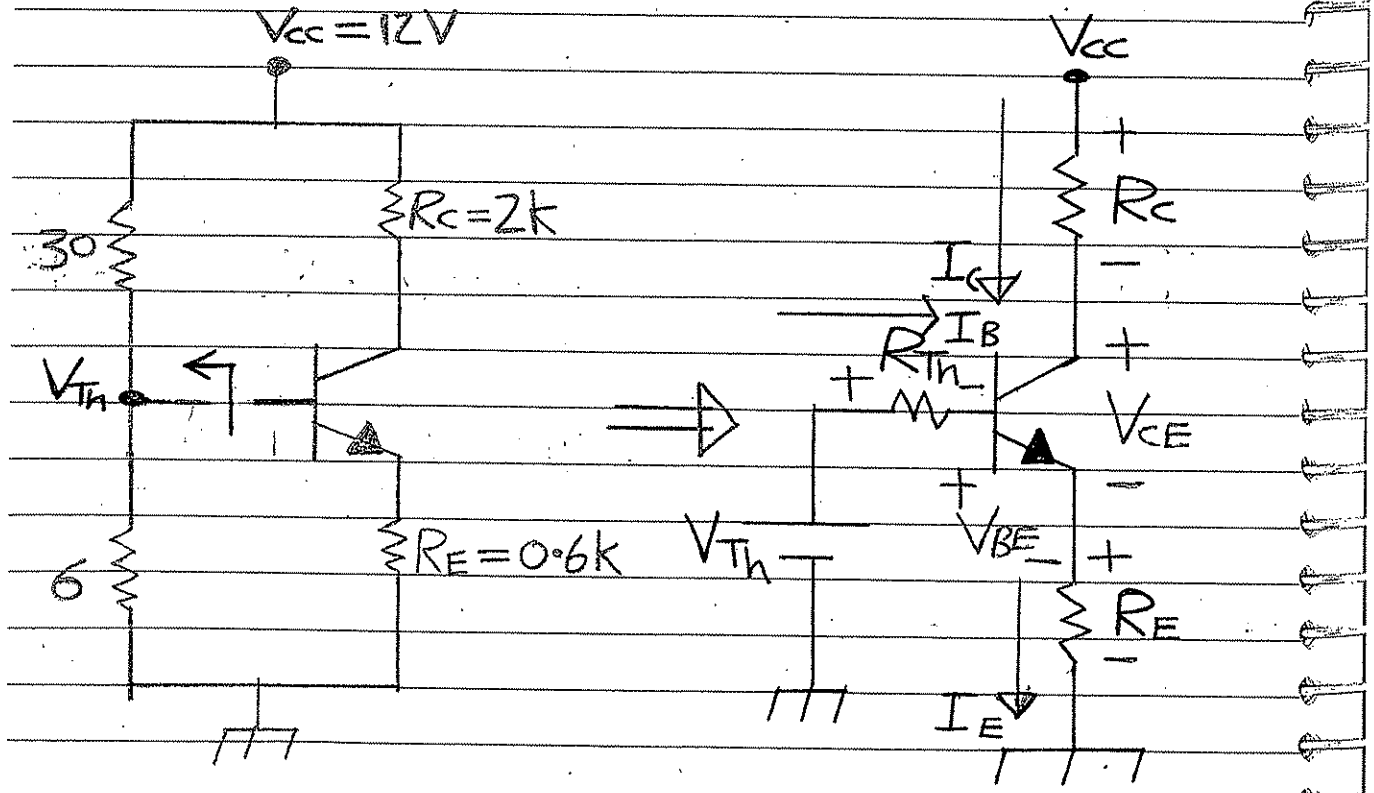
EXA:

Given : $V_{BE} = 0.7V$, $V_{CE(sat)} = 0.2V$.

Calculate : I_{CQ} , V_{CEQ} , $\Delta I_{CQ}\%$, $\Delta V_{CEQ}\%$ when β is Changed from 100 to 200 ?



Sol. For DC Analysis, all Caps : OFF.



$$V_{Th} = V_{CC} \cdot \frac{R_2}{R_1 + R_2} = \frac{12 * 6}{30 + 6} = 2\,V.$$

$$R_{Th} = R_1 \,//\, R_2$$

$$= 30 \,//\, 6 = 5\,k\Omega.$$

$$-V_{Th} + I_B R_{Th} + V_{BE} + I_E R_E = 0$$

$$\rightarrow I_E = (\beta + 1) I_B$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E} = I_{BQ}$$

$$I_{CQ} = \uparrow\beta \downarrow I_{BQ}$$

(شارت)

1) For $\beta = 100$:

$$I_{BQ} = \frac{(2 - 0.7)\,V}{5 + (101 * 0.6)} = \frac{1.3\,V}{65.6\,k} = 0.0198\,mA$$

$$I_{CQ} = 100 * 0.0198 = 1.98\,mA.$$

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0$$

$$V_{CE} = 12 - I_C R_C - I_E R_E$$

$$\rightarrow I_E = (\beta+1) I_B = 2\,mA.$$

$$V_{CE} = 12 - (1.98 * 2) - (2 * 0.6)$$

$$= 6.84\,V.$$

2) For $\beta = 200$:

$$I_B = \frac{(2-0.7)V}{5 + (201 * 0.6)} = \frac{1.3V}{126k} = 0.01\,mA.$$

$$I_C = 200 * 0.01 = 2\,mA.$$

$$I_E = (\beta+1) I_B = 2.02\,mA.$$

$$V_{CE} = 12 - (2*2) - (2.02 * 0.6)$$

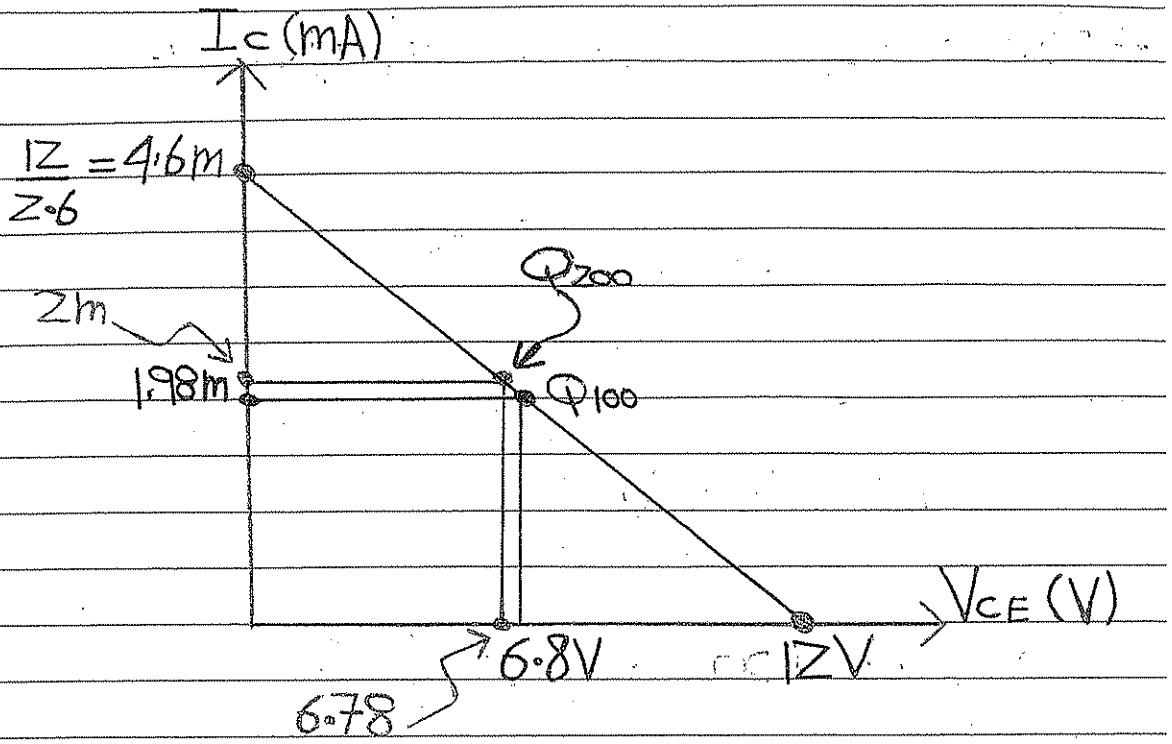
$$= 6.78\,V.$$

$$\Delta I_C = \frac{2 - 1.98}{1.98} * 100\% = \frac{0.02}{1.98} * 100\%$$

$$= 1\%$$

$$\Delta V_{CE} = \frac{6.78 - 6.8}{6.8} * 100\% = -0.3\%$$

Bipo Ample



In this Circuit, the Q.pt is Very Stable against β - Variation. The Circuit has Very Good Bias - Stablility.

* Bias-Stable Condition :-

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta+1)R_E} = I_{BQ}$$

$$I_c = \beta I_{BQ}$$

$$= \frac{\beta (V_{Th} - V_{BE})}{R_{Th} + (\beta+1) R_E}$$

if $(R_{Th} \ll (\beta+1)R_E)$ & $(\beta \gg 1)$

$$\therefore I_{cQ} \simeq \frac{V_{Th} - V_{BE}}{R_E}$$

I_c لا تعتمد على β

For Bias-Stable Condition : Choose

$$\boxed{R_{Th} = 0.1\ (\beta+1)\ R_E} \quad \therefore R_{Th} \ll (\beta+1) R_E$$

[For Design]

* To Cheak For Bias - Stable Case;

Show that:

$R_{Th} \leqslant 0.1\,(\beta+1)\,R_E$

ExA: USe a BJT with $\beta = 100$,

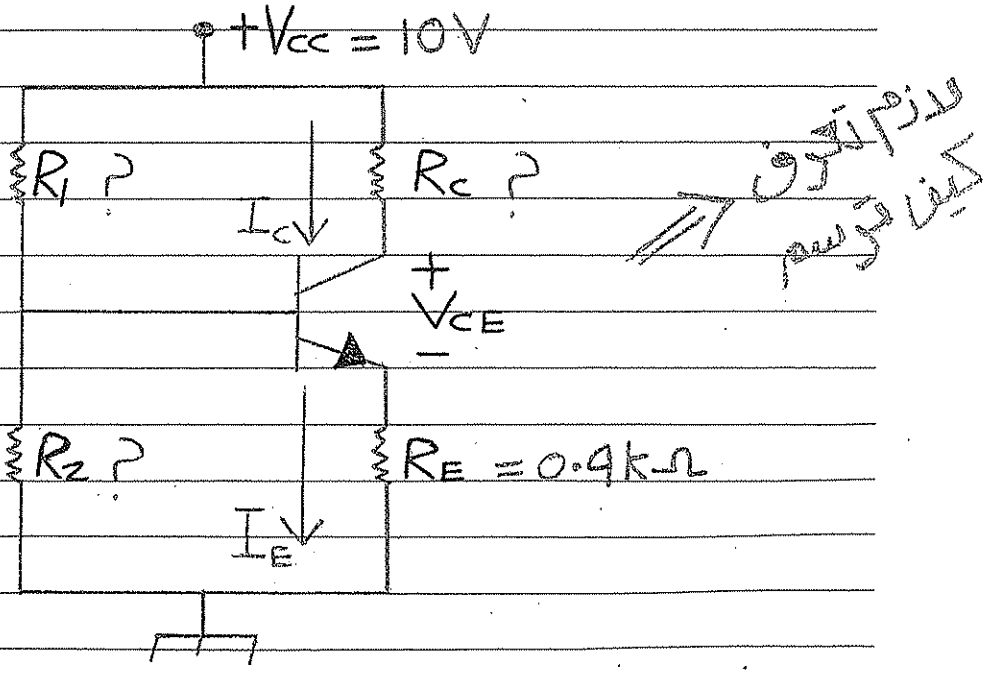
$V_{BE} = 0.7V$,

Design a bias - Stable to have

$I_{CQ} = 2mA$, $V_{CEQ} = 5V$,

USe $R_E = 0.4\,k\Omega$, $V_{cc} = 10V$.

Sol.



For bias - Stable design:

$R_{Th} = 0.1(\beta+1)R_E$ Condition

R_c ?

$-V_{cc} + I_cR_c + V_{CE} + I_ER_E = 0$

$\rightarrow I_E = \left(\frac{\beta+1}{\beta}\right) I_c = \frac{101}{100} * 2 = 2.02\ mA.$

$I_cR_c = V_{cc} - V_{CE} - I_ER_E$

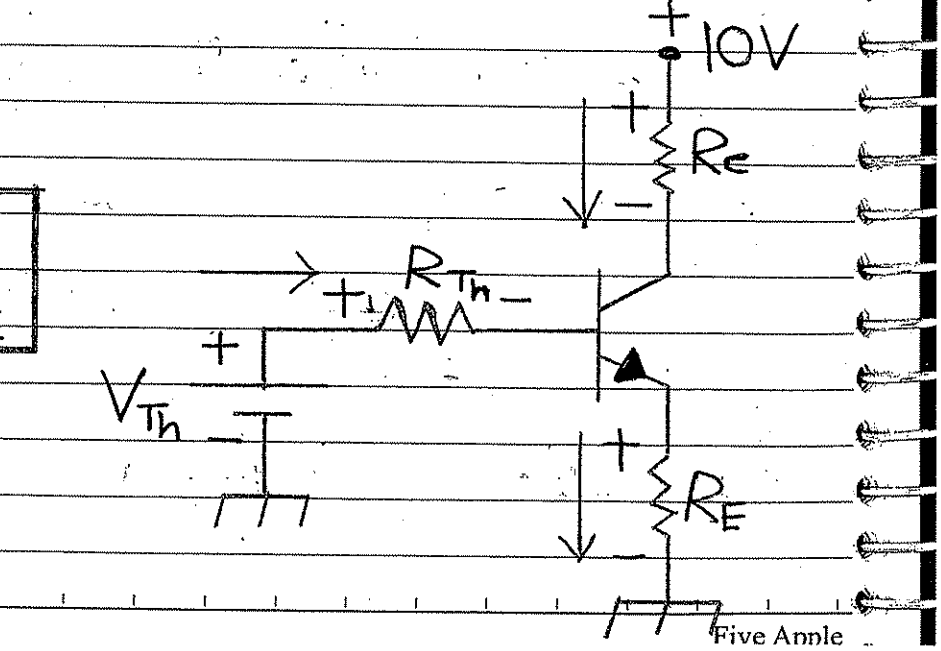
$= 10 - 5 - (2.02 * 0.4) = 4.2V.$

$R_c = \frac{4.2}{2m} = 2.1\ k\Omega.$

$R_{Th} = 0.1(101) * 0.4 = 4k\Omega.$

$R_{Th} = R_1 // R_2$

$$\boxed{R_{Th} = \frac{R_1R_2}{R_1+R_2}}$$



$$R_1 * V_{Th} = V_{cc} \frac{R_2}{R_1 + R_2} * R_1$$

$$R_1 V_{Th} = V_{cc} R_{Th}$$

$$\boxed{R_1 = \frac{V_{cc}}{V_{Th}} \cdot R_{Th}}$$

$V_{Th} = ?$

$$-V_{Th} + I_B R_{Th} + V_{BE} + I_E R_E = 0$$

$$V_{Th} = I_B R_{Th} + V_{BE} + I_E R_E$$

$$* \; I_B = \frac{I_c}{\beta} = \frac{2}{100} = 0.02 \text{ mA}.$$

$$* \; I_E = 7.02 \text{ mA}.$$

$$\rightarrow V_{Th} = 0.021 * 4 + 0.7 + 7.02 * 0.4$$

$$= 0.08 + 0.7 + 0.808$$

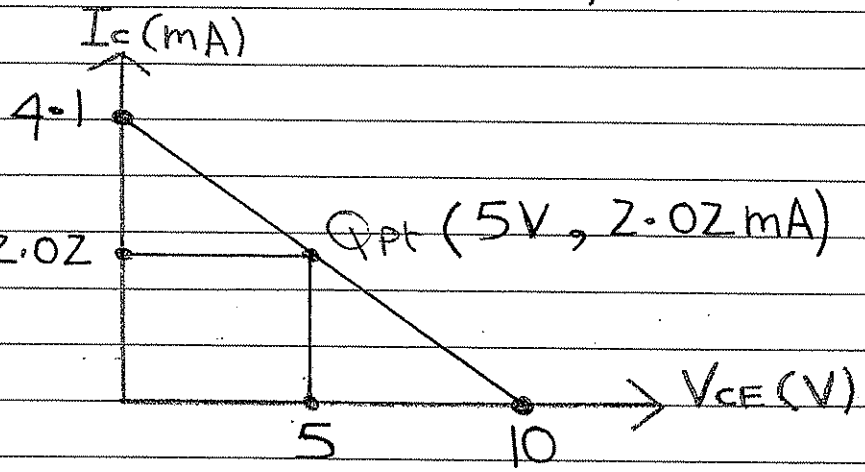
$$= 1.588 \text{ V}.$$

$$R_1 = \frac{10}{1.588} * 4 = 26 \text{ k}\Omega.$$

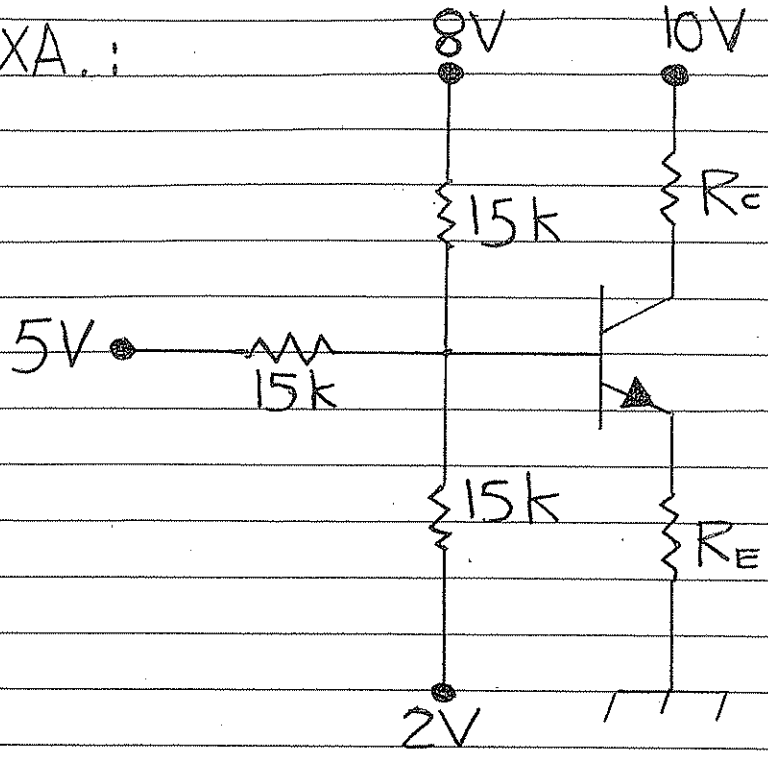
$$R_2 = \frac{R_1 \cdot R_{Th}}{R_1 - R_{Th}} = \frac{26 * 4}{26 - 4} = \frac{104}{22} = 4.7 \text{ k}\Omega.$$

$$-10 + I_C R_C + V_{CE} + \left(\frac{\beta+1}{\beta}\right) I_C R_E = 0$$

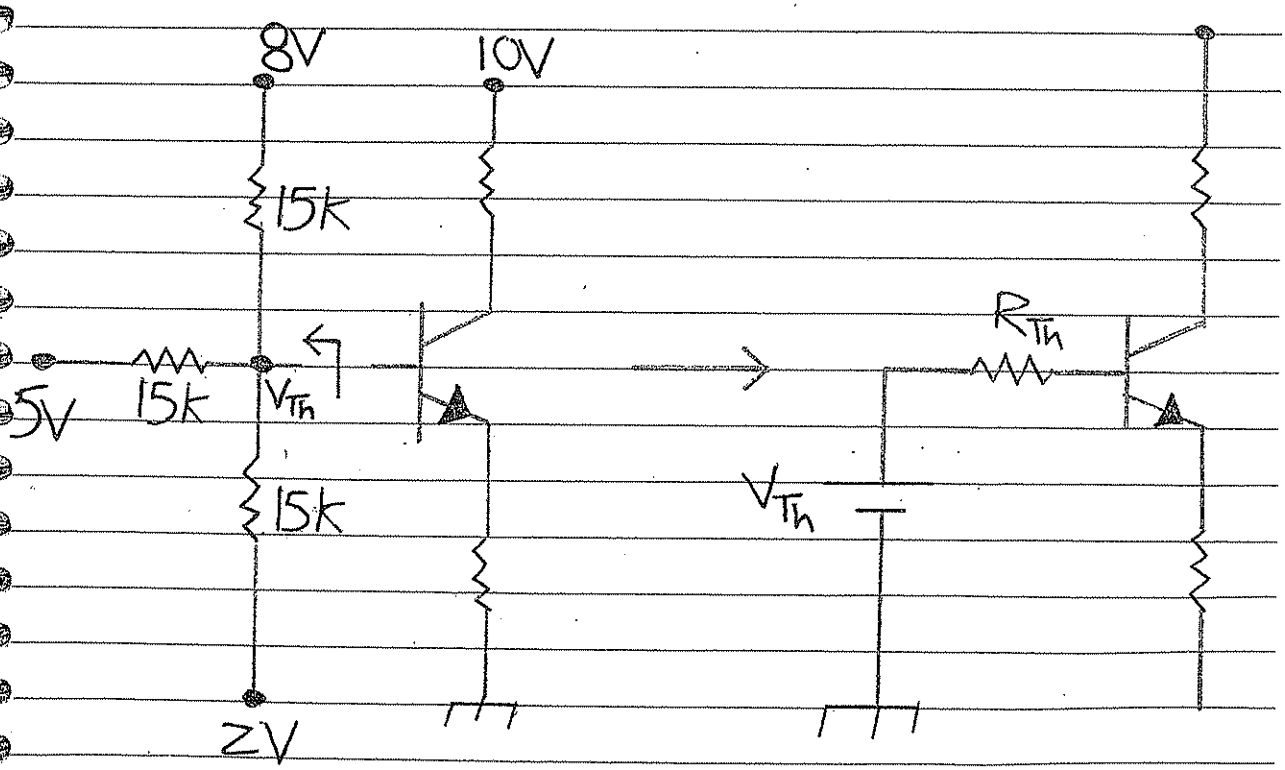
$$V_{CE} = 10 - I_C\left(R_C + \left(\frac{\beta+1}{\beta}\right) R_C\right)$$



EXA.:



Find R_{Th} , V_{Th} ?



$R_{Th} = 15 // 15 // 15 = 5\,k\Omega$.

V_{Th} :

method I : By using Super position :

$$V_{Th} = \frac{8(15 // 15)}{15 + 7.5} + \frac{5(7.5)}{15 + 7.5} + \frac{2(7.5)}{7.5 + 15}$$

$$= \frac{15(7.5)}{22.5} = 5V .$$

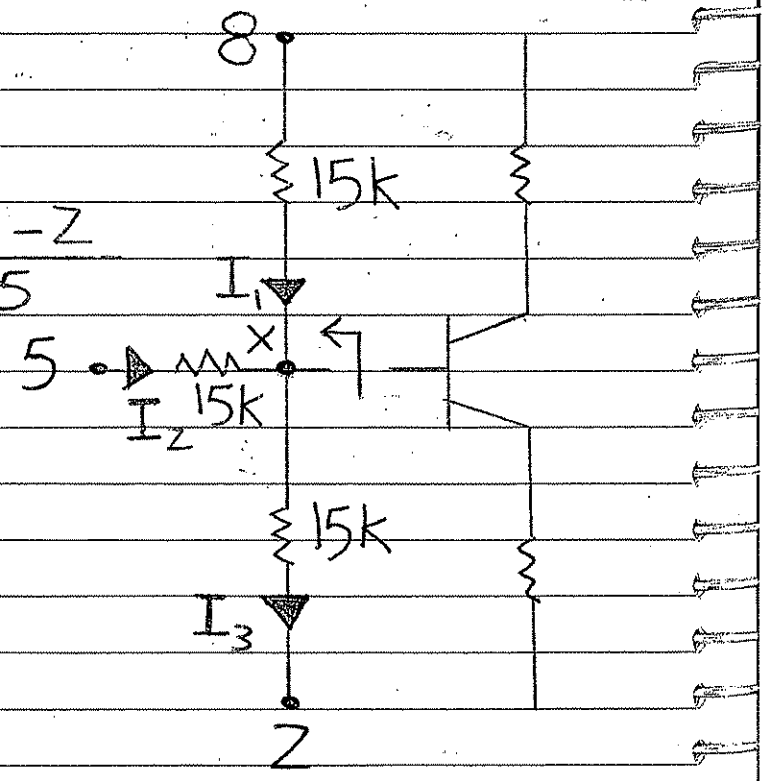
method II : KCL at node(X) :

$$I_1 + I_2 = I_3$$

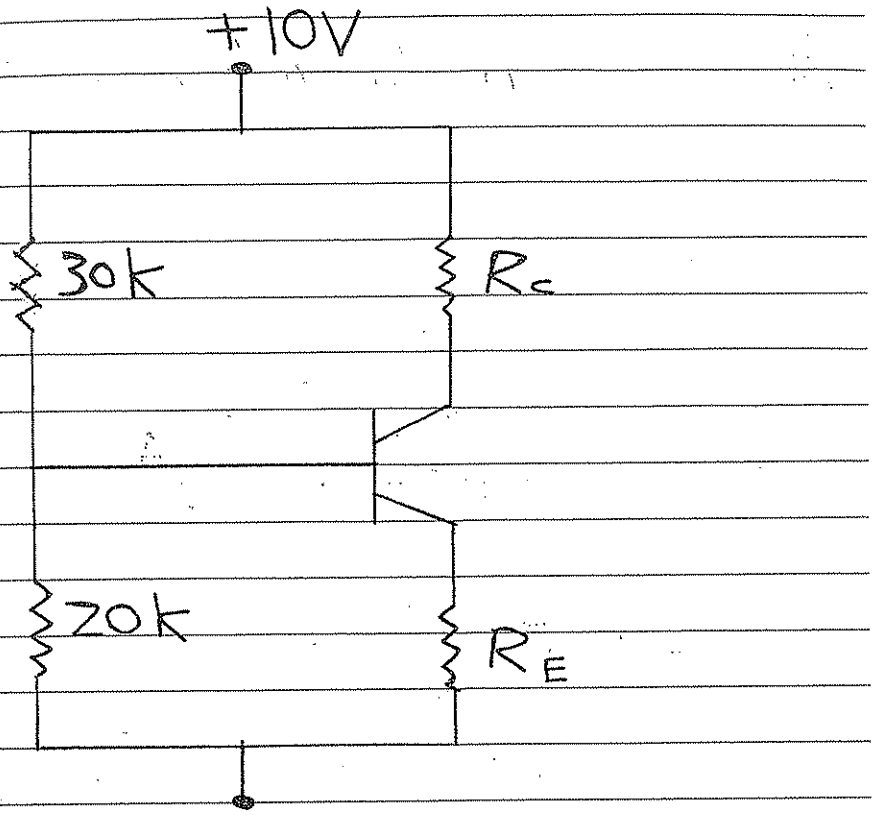
$$\frac{8 - V_x}{15} + \frac{5 - V_x}{15} = \frac{V_x - Z}{15}$$

$$3V_x = 15$$

$$V_x = 5V .$$

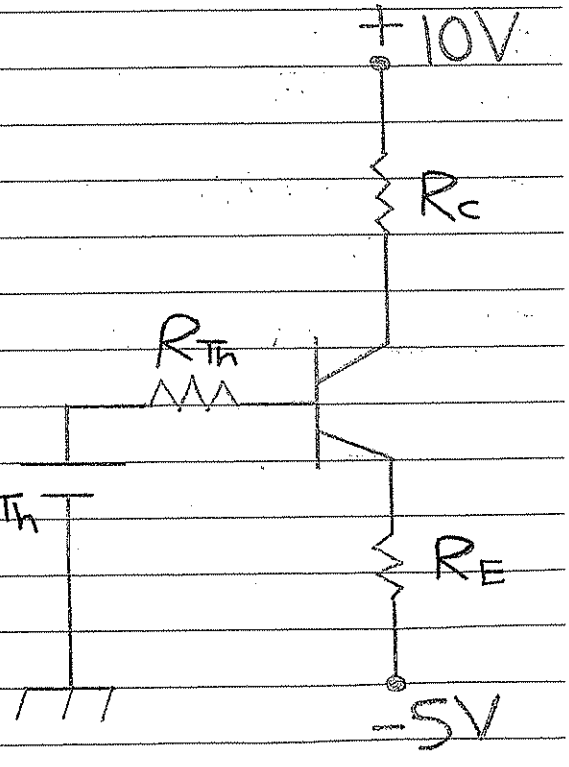


EXA :



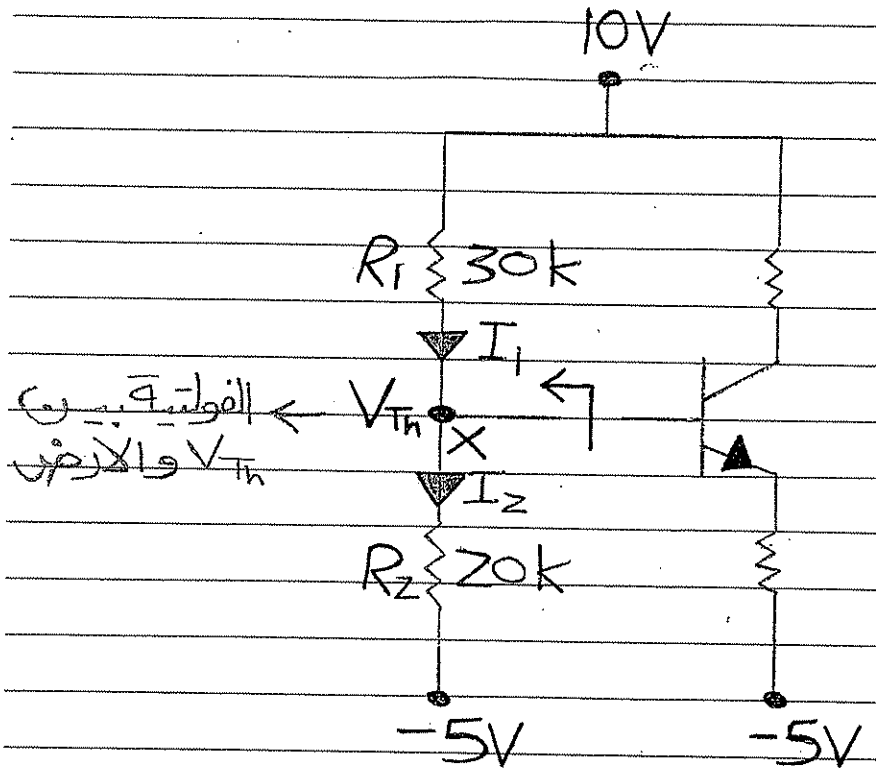
Find R_{Th}, V_{Th} ?

Sol.



$R_{Th} = 30 \| 20$

$= 12\ k\Omega$.



الفولتية بين V_{Th} والأرض.

By Super Position :-

$$V_{Th} = \frac{10 * 20}{20+30} + \frac{(-5)(30)}{20+30}$$

$$= 4 - 3 = 1V.$$

KCL at X :-

$$I_1 = I_2$$

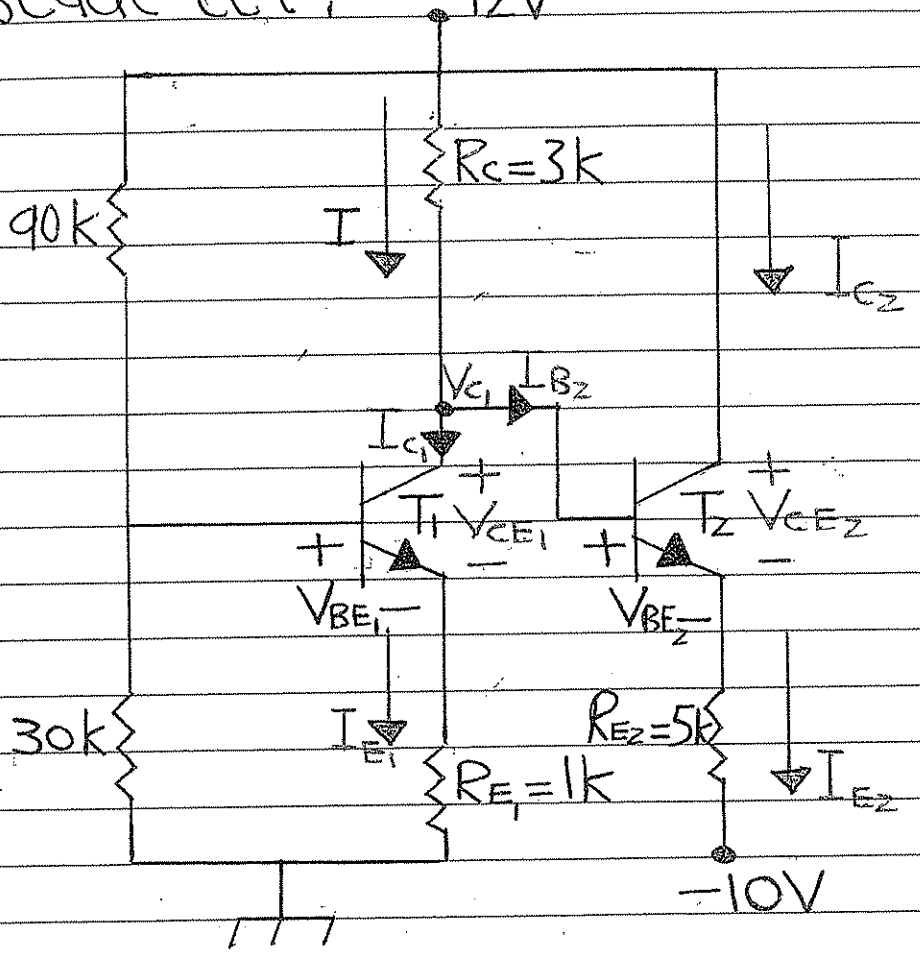
$$\frac{10 - V_{Th}}{30} = \frac{V_{Th} - (-5)}{20}$$

$$20 - 2V_{Th} = 3V_{Th} + 15 \longrightarrow V_{Th} = 1V.$$

5.5 :- Multitransistor Circuits :-

1) Cascade CCt :-

EXA.



Given T_1 & T_2 are identical,

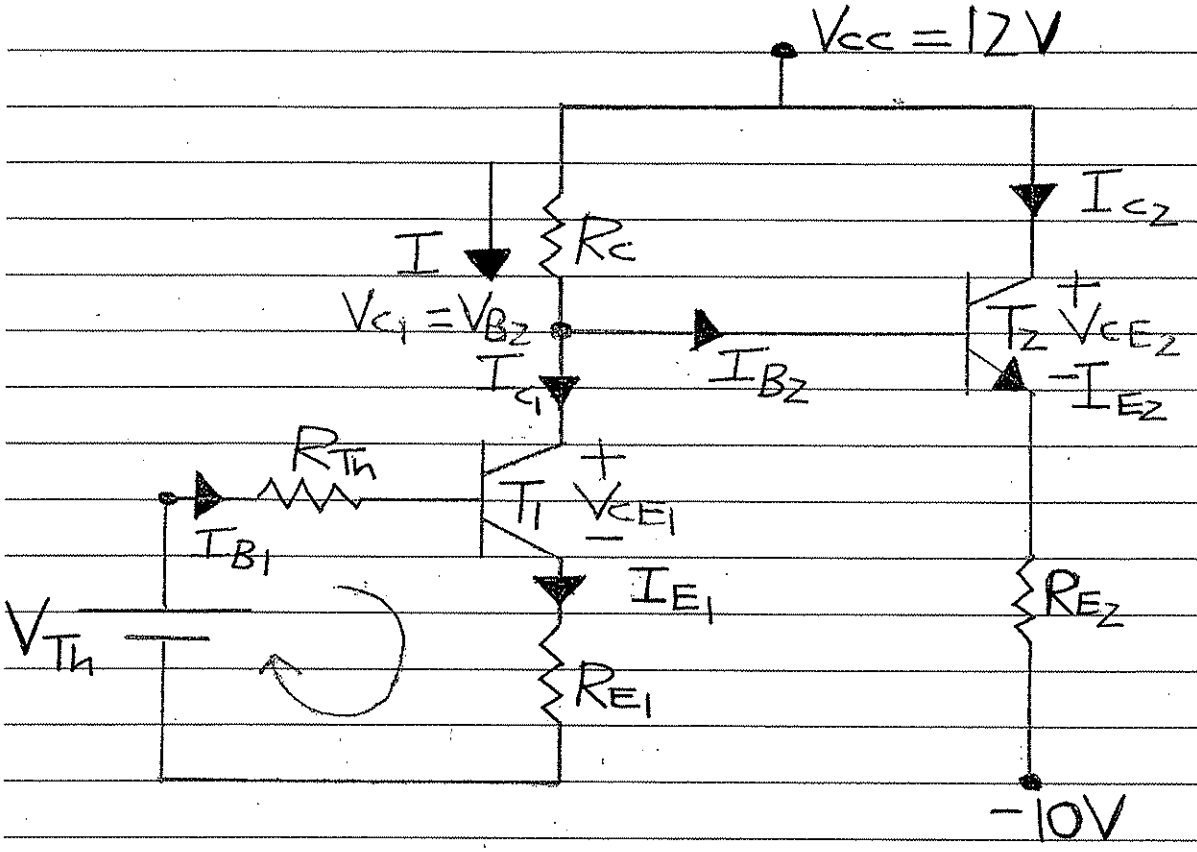
$\beta_1 = \beta_2 = 100$.

$V_{BE_1} = V_{BE_2} = 0.7\,V$.

$V_{CE_1(sat)} = V_{CE_2(sat)} = 0.2\,V$.

Find :- I_{B1}, I_{C1}, I_{E1}, V_{CE_1}, I_{B2}, I_{C2}, I_{E2}, V_{CE_2}, V_{C1}, V_{B2}, V_{E2}, V_{E1} . ?

Sol. :- Thevevnin Equ. CCt نحوّل الدّارة إلى



$$V_{cc} + I \cdot R_c + V_{CE_1} + I_{E_1} R_{E_1} = 0$$

$$V_{CE_1} = V_{cc} - I_{E_1} R_{E_1} - I \cdot R_c$$

$$= 10 \cdot 15 - 3I$$

$$I = I_{c_1} + I_{B2}$$

$$V_{Th} = \frac{12 * 30}{90 + 30} = 3V$$

$$R_{Th} = 30 // 90 = \frac{2700}{120} = 22.5 k\Omega$$

$$-V_{Th} + I_{B1} R_{Th} + V_{BE1} + (\beta + 1) I_{B1} R_{E1} = 0$$

$$I_{B1} = \frac{V_{Th} - V_{BE1}}{R_{Th} + (\beta + 1) R_{E1}} = \frac{(3 - 0.7) V}{(22.5 + 101) k}$$

$$= \frac{2.3}{123.5 k}$$

$$= 0.018 mA.$$

$$I_{C1} = \beta I_{B1} = 1.8 mA$$

$$I_{E1} = (\beta + 1) I_{B1} = 1.818 mA$$

$$-V_{C1} + V_{BE2} + ((\beta + 1) I_{B2}) R_{E2} - 10 = 0$$

$$I_{B2} = \frac{V_{C1} + 10 - 0.7}{101 * 5} = \frac{V_{C1} + 9.3}{505}$$

$$I = I_{C1} + I_{B2}$$

$$\frac{12 - V_{C1}}{3} = 1.8 + \frac{V_{C1} + 9.3}{505}$$

$$\frac{505}{3}(12 - V_{C1}) = 1.8 * 505 + V_{C1} + 9.3$$

$$2020 - 168.3 V_{C1} - V_{C1} = 918.3$$

$$-169.3 V_{C1} = -1101.7$$

$$V_{C1} = 6.5 V.$$

$$I = \frac{12 - V_{C1}}{3} = \frac{12 - 6.5}{3} = 1.8 mA$$

$$I_{B2} = \frac{V_{C1} + 9.3}{505} = 0.031 mA.$$

$$I_{C2} = \beta I_{B2} = 3.1 mA.$$

$$I_{E2} = (\beta + 1) I_{B2}$$

$$= 101 * 0.031 = 3.131 mA.$$

$$-12 + V_{CE_2} + I_{E_2} R_{E_2} - 10 = 0$$

$$V_{CE_2} = 12 - I_{E_2} R_{E_2} + 10$$

$$= 12 - 15.6 + 10 = 6.4\,V$$

#.

*For Second Stage : The DCLL equ. :

$$-V_{CE_2} = 10 + 12 - I_{C_2}\left(\frac{\beta+1}{\beta} R_{E_2}\right).$$

#.

EXA. :

Given : Q_1 & Q_2 are identical with $\beta = 100$, $V_{BE} = 0.7\,V$

Design the Circuit Such that

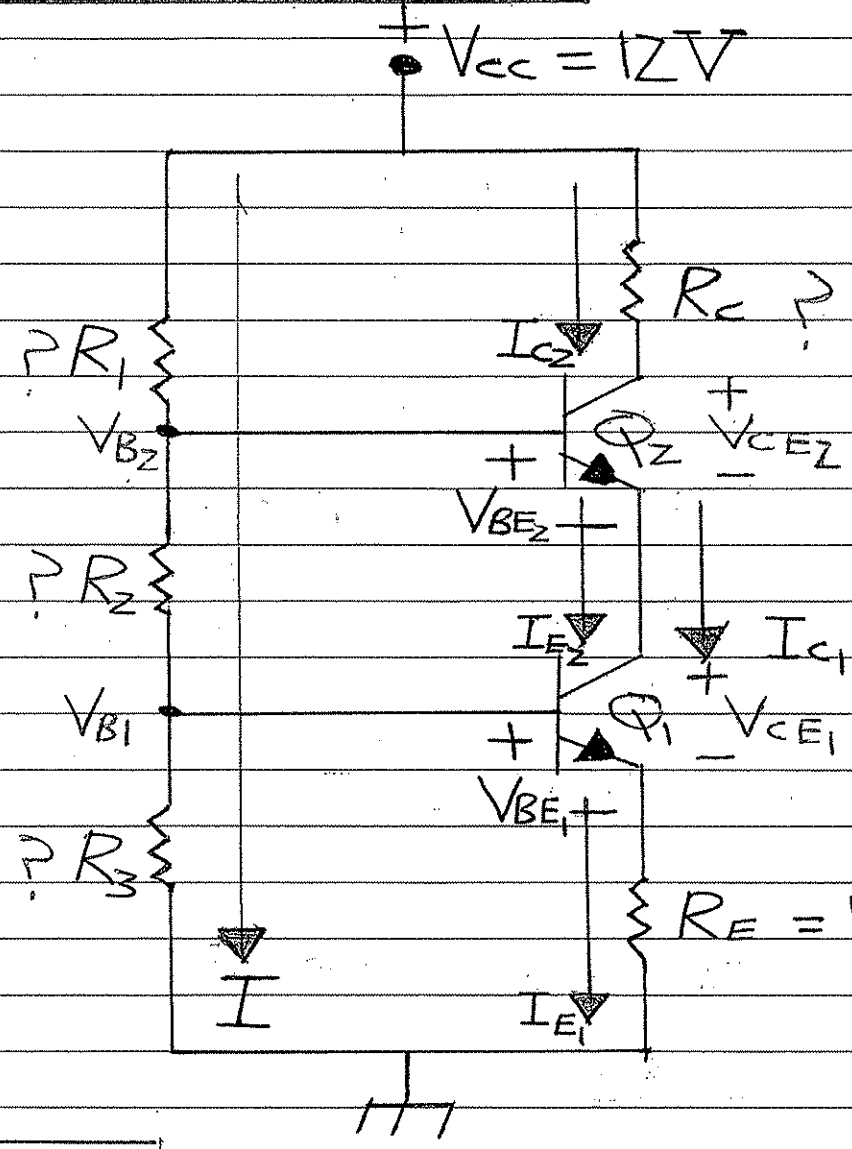
$I_{C_2} = 2\,mA$

$V_{CE_1} = V_{CE_2} = 4\,V$

$(I_{C_2} = I_{E_2} = I_{C_1})$ and Choose $R_1 + R_2 + R_3 = 300\,k\Omega$.

P

2) Cascode Circuit :-



$I_C \simeq I_E$ for D.C Analysis.

Sol.

R_C ? KVL for O/P Loop :

$$-12 + I_{C2}R_C + V_{CE_2} + V_{CE_1} + I_{E1}R_E = 0$$

$$I_C R_C = 12 - 4 - 4 - 2*1 = 10 - 8 = 2V.$$

$$R_C = \frac{2V}{2mA} = 1k\Omega.$$

$$R_3 = \frac{V_{B1}}{I} \rightarrow$$

$$I = \frac{V_{cc}}{R_T} = \frac{12}{300k} = 0.04\ mA.$$

$$-V_{B_1} + V_{BE_1} + I_{E_1}R_E = 0$$

$$V_{B_1} = 0.7 + 2*1 = 2.7V.$$

$$\therefore R_3 = \frac{2.7}{0.04} = 67.5\ k\Omega$$

$$R_2 = \frac{V_{B2} - V_{B1}}{I}$$

$$-V_{B_2} + V_{BE_2} + V_{CE_1} + I_{E_1}R_E = 0$$

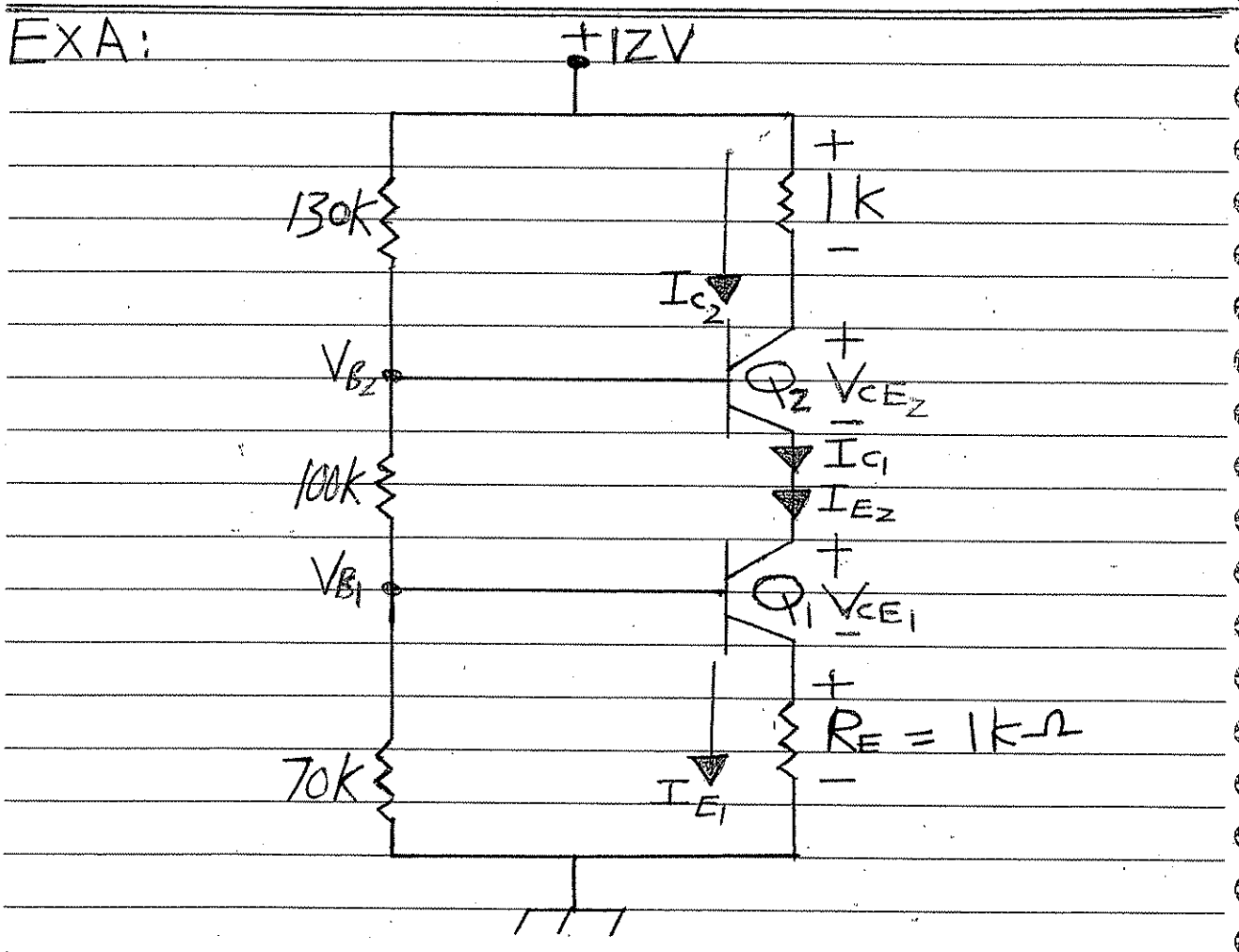
$$V_{B_2} = 0.7 + 4 + 2*1 = 6.7V.$$

$$R_2 = \frac{(6.7 - 2.7)\,V}{0.04\,m} = \frac{4\,V}{0.04} = 100\,k\Omega$$

$$R_1 = \frac{V_{CC} - V_{B2}}{I} = \frac{12 - 6.7}{0.04}$$

$$= \frac{5.3}{0.04} = 132.5\,k\Omega$$

EXA:



(DC Analysis) Equation (Design).

$I = ?$, $V_{B_1} = ?$, $V_{B_2} = ?$, $V_{CE_1} = ?$, $V_{CE_2} = ?$,

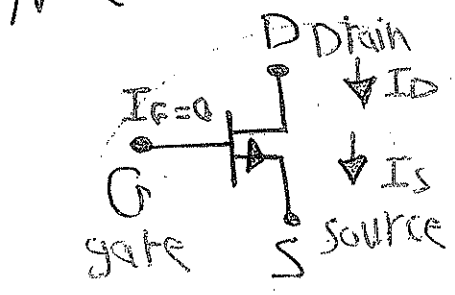
Ch.3:- Field-Effect Transistor:

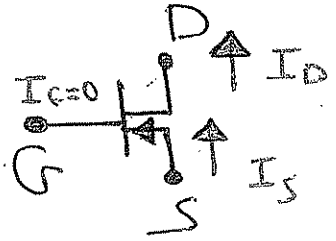
(FET):-

unipolar Device (only one Type of carrier)

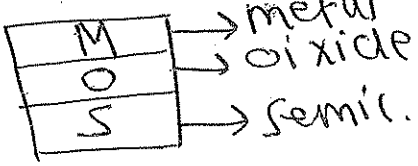
$I_G = 0$, $I_D = I_S$

- JFET
  - electrons → N-channel
  - Holes → P-channel
- MOSFET





Gate



MosFET

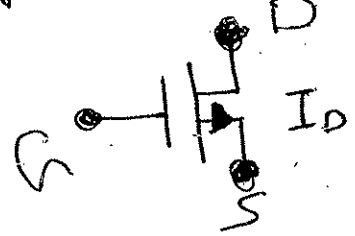
[Metal - Oxide - semiconductor Field Effect Transistor]

Normally-off

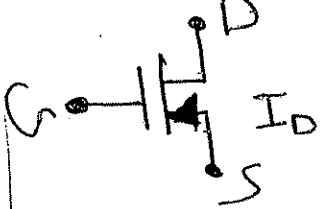
① The channel is induced electronically.

Enhancement Mos [E-Mos]

- N-channel



- P-channel

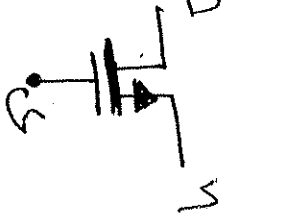


Normally ON

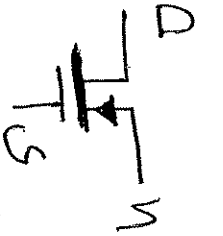
① There is a physical channel.

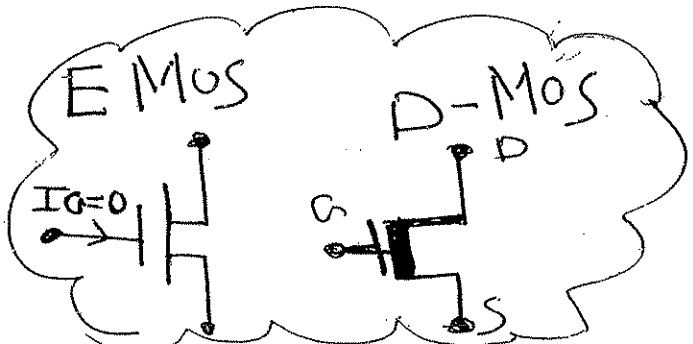
Depletion Mos [D-Mos]

- N-channel



- P-channel





* E - MOS :—

(1) N-Channel E-MOS :—

(a) structure

(b) peration.

(c) I-V characteristic.

(d) D.c Analysis of N-channel Mos.

(e) Multistage Mosfet ckts.

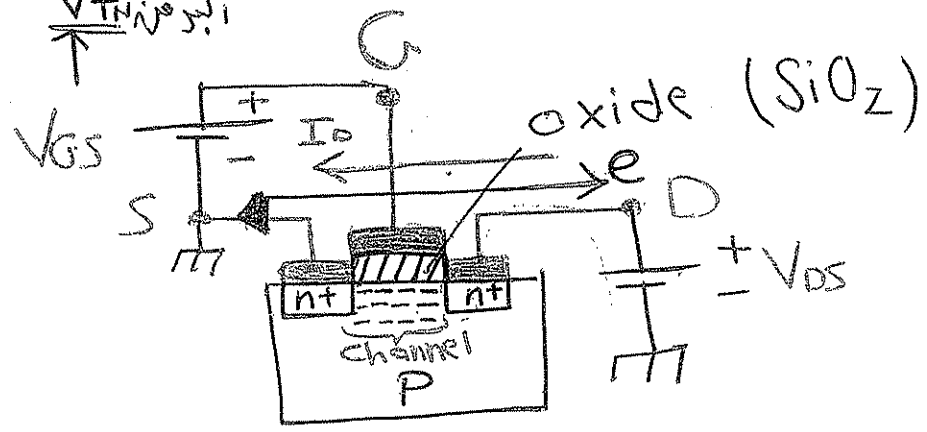
Ele. 1 : (22/12) # الإلكترونيات

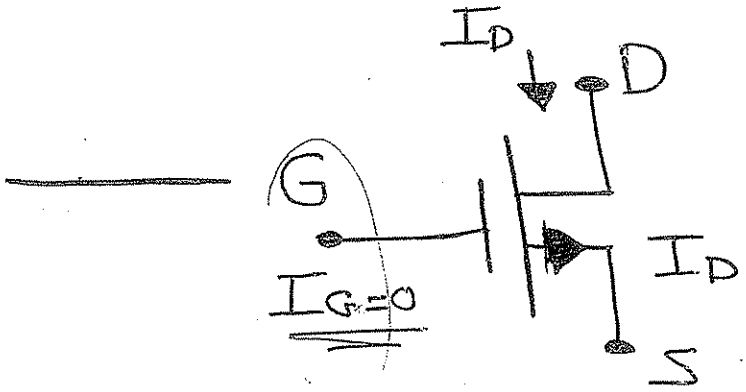
V_{TN}: Threshold Voltage for N-Channel.

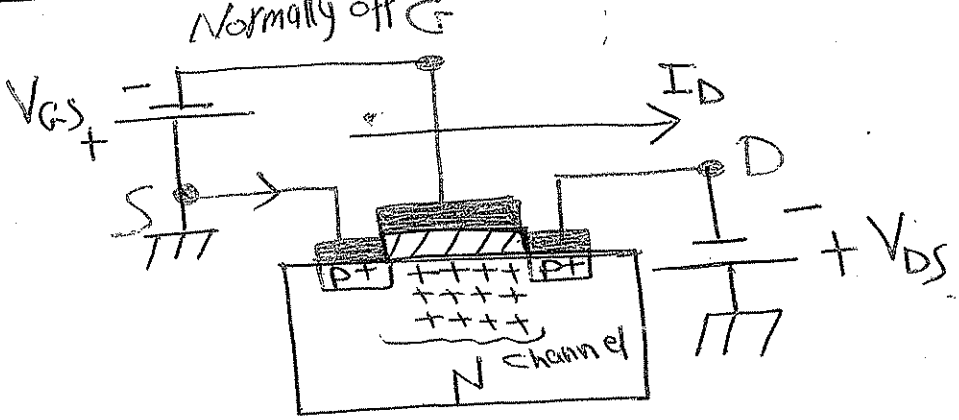
$V_{GS} > V_{TN}$

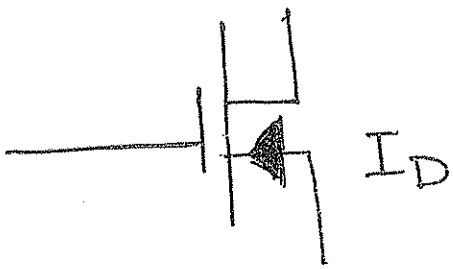
يجب أن تكون V_{GS} أكبر من V_{TN}

* N-Channel E-Mos :-

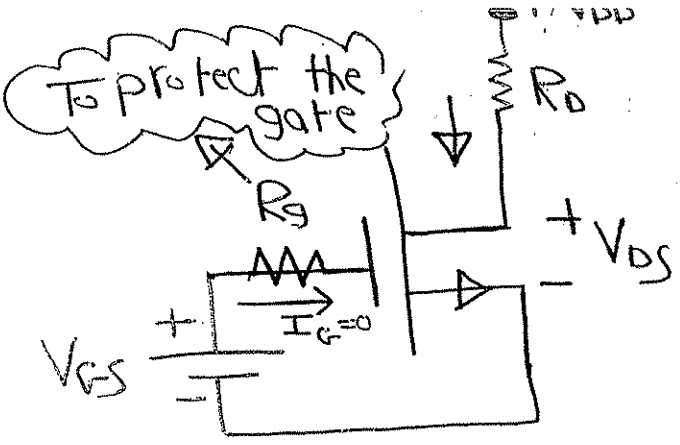




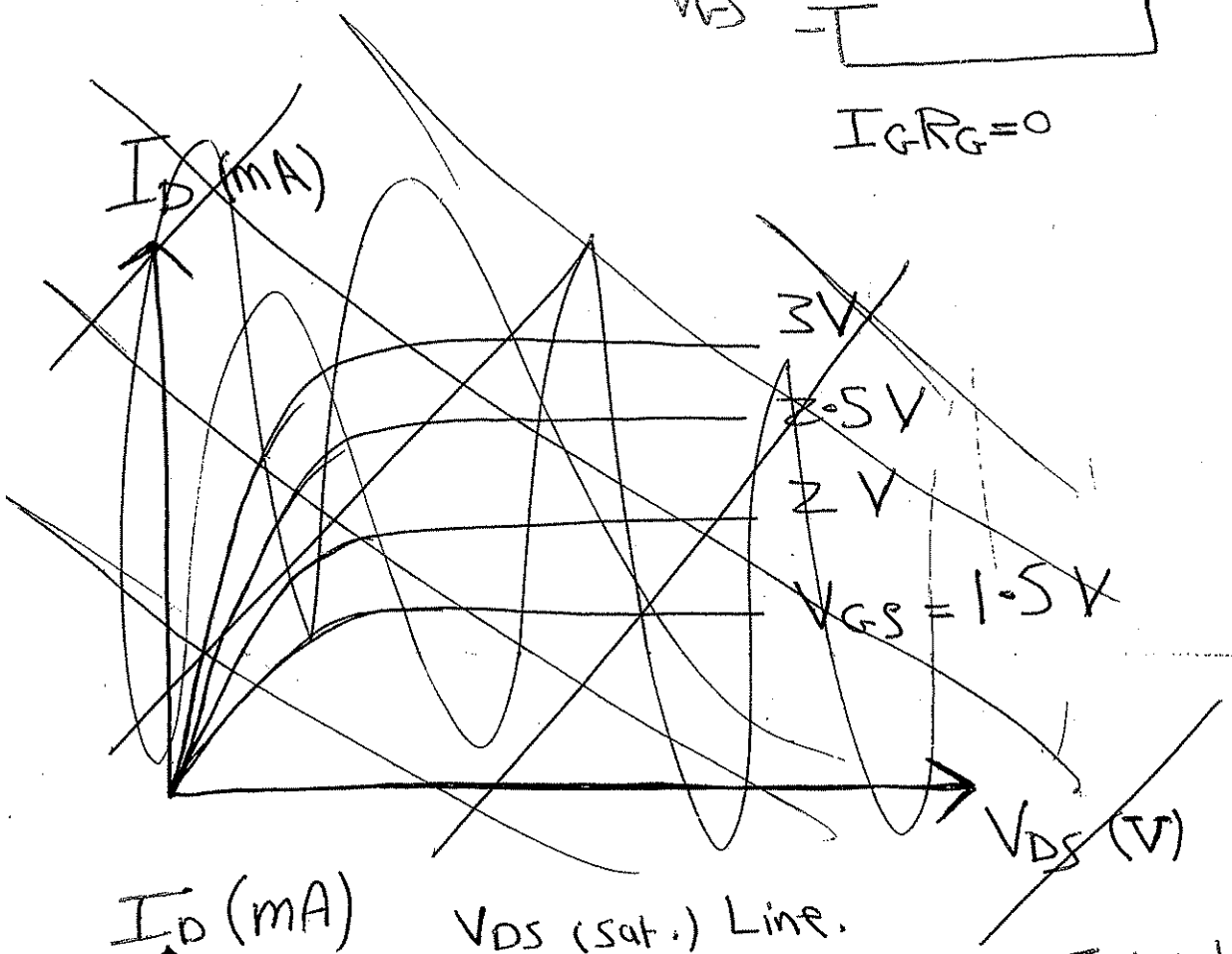


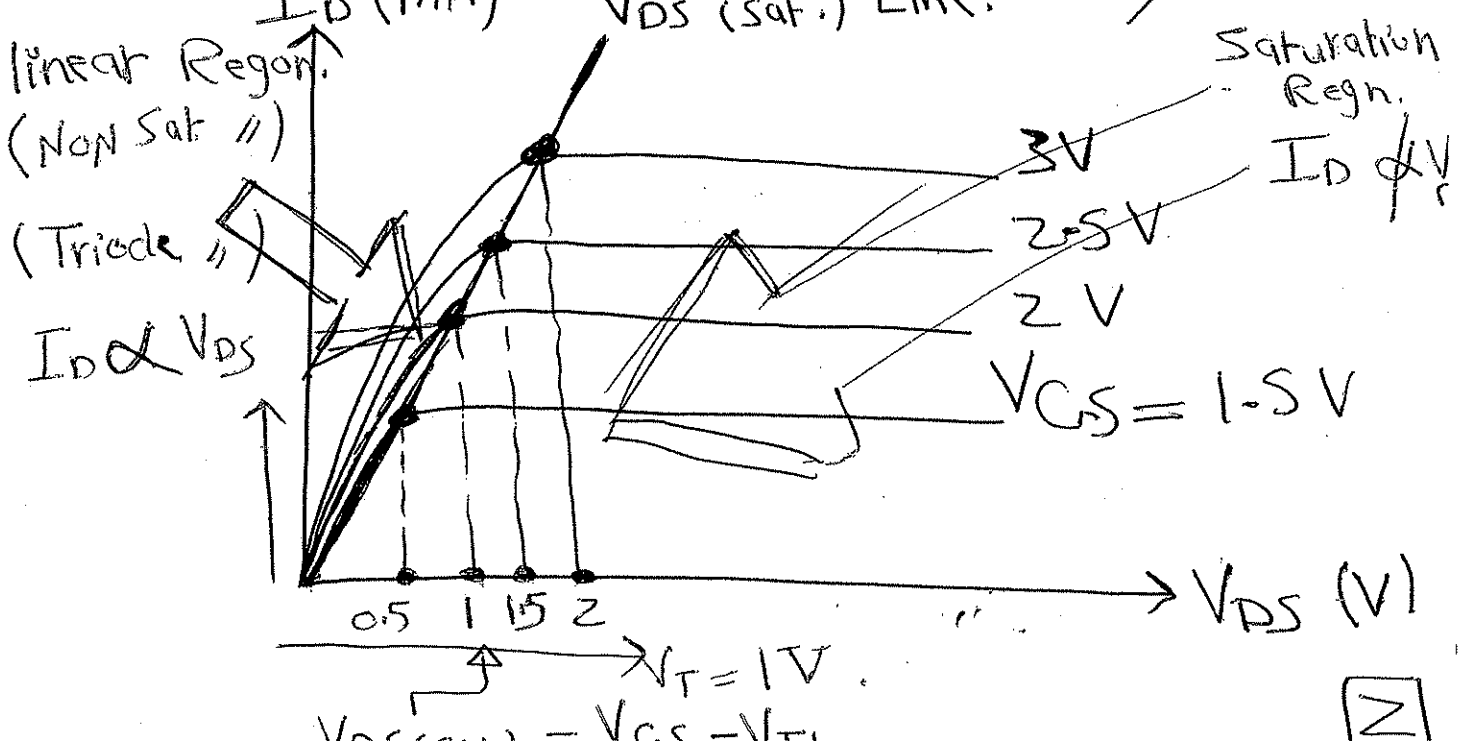


C/C :


To protect the gate
R_G
R_D
$+V_{DS}$
$I_G=0$
V_{GS}

$I_G R_G = 0$


I_D (mA)
3V
2.5V
2V
$V_{GS}=1.5V$
V_{DS} (V)


I_D (mA)
V_{DS} (sat.) Line.
linear Regon.
(Non Sat ")
(Triode ")
$I_D \propto V_{DS}$
Saturation Regn.
$I_D \not\propto V_{DS}$
3V
2.5V
2V
$V_{GS}=1.5V$
0.5
1
1.5
2
V_{DS} (V)
$V_T = 1V$
$V_{DS(sat.)} = V_{GS} - V_T$

2

*Operations Regns :- (the most important 209 works as an Amplifier)

① Saturation Regn :- (constant current source).

When $V_{DS} > V_{DS(sat)}$

where $V_{DS(sat)} = V_{GS} - V_{TN}$

$$I_D = k_n (V_{GS} - V_{TN})^2$$

k_n : (conduction parameter) $\frac{mA}{V^2}$

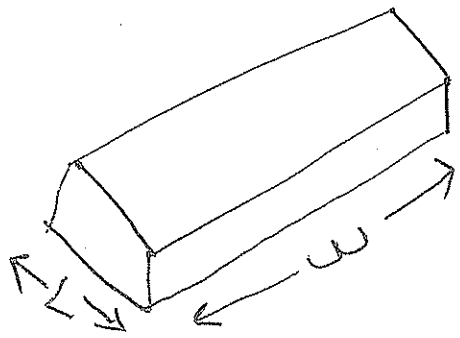
Given.

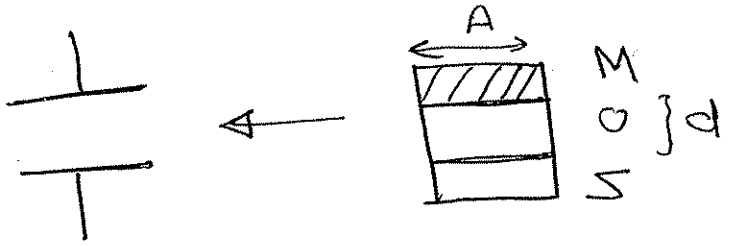
$$k_n = \frac{\mu C_{ox}' \cdot W}{2L}$$

W, L : Width & Length of channel.

μ_n : electron mobility.

C_{ox}' : gate-oxide-capacitance (Per unit Area) F/m^2





$$C_{ox} = \frac{\epsilon A}{d}$$

$$\frac{C_{ox}}{A} = \frac{\epsilon}{d} = C_{ox}'$$

---

(2) Non Sat- Regn : (Linear Regn)

When $V_{DS} < V_{DS(sat)}$

then ~~$I_D = k_n [(V_{GS} - V_{TN}) V_{DS} - V_{DS}^2]$~~

$$I_D = 2 \left[k_n (V_{GS} - V_{TN}) V_{DS} - V_{DS}^2 \right].$$

For small values of V_{DS} :-

$$I_D \cong 2 \left[k_n (V_{GS} - V_{TN}) V_{DS} \right]$$

$$\frac{V_{DS}}{I_D} = R_{mos} = \frac{1}{2 k_n (V_{GS} - V_{TN})}$$

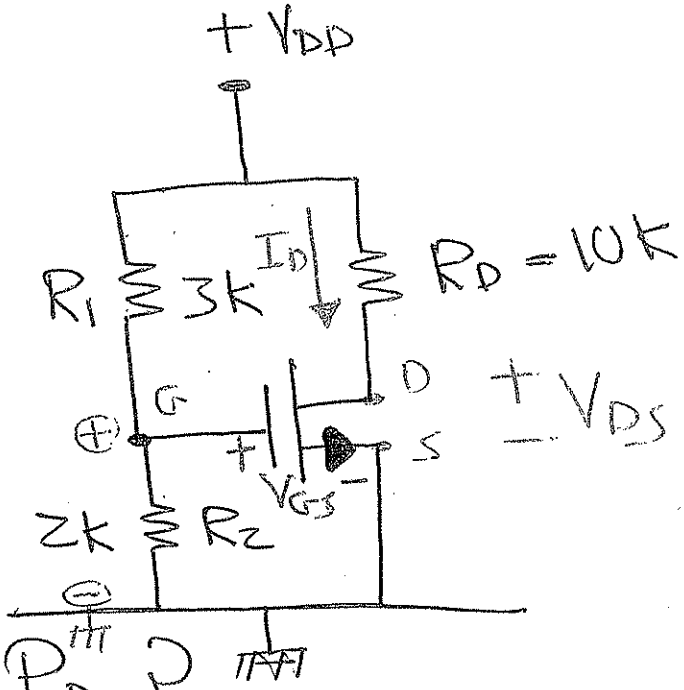
Voltage var. resistance

ثابتة ثابتة

In this Regn. The mosfet works as a Voltage Variable Resistor (VVR).

D-C Analysis of MOSFET ckts

Ex A:



Given:

$V_{TN} = 1V$.

$k_n = 0.2 mA/V^2$.

1) calculate

V_{GS}, I_D, V_{DS}, P_D ?

2) Draw D-C-Load line; find its Slope & Indicate Qpt.

Assume the MOSFET in Sat.:-

$$I_D = K_n (V_{GS} - V_{TN})^2$$

$$V_{GS} = V_G - V_S$$

$$= \frac{V_{DD} \cdot R_2}{R_1 + R_2} - 0 = \frac{5 * 2}{3+2} - 0$$

$$= 2V \#.$$

$$I_D = 0.2(2-1)^2 = 0.2mA.$$

KVL for out Loop:-

$$-V_{DD} + I_D R_D + V_{DS} = 0$$

$$V_{DS} = 5 - 0.2 * 10 = 3V$$

Cheak:

$$V_{DS(sat)} = V_{GS} - V_{TN} = 2 - 1 = 1V$$

since $V_{DS} > V_{DS(sat)}$ ∴ Mosfet in sat.

$P_D = I_D V_{DS} = 0.2 * 5 = 0.6\ mW.$

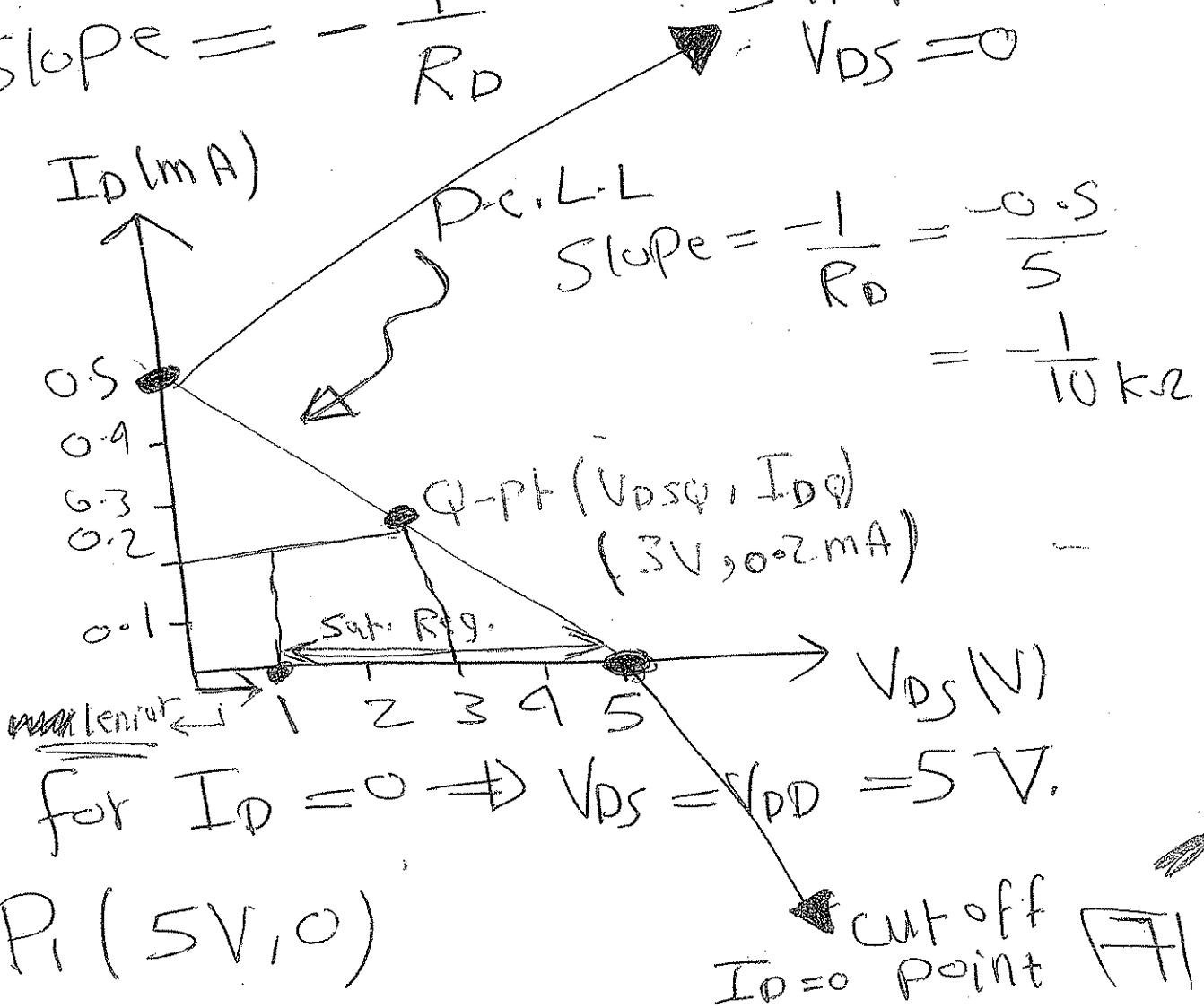
D.C.L.L :-

KVL for 'D-S Loop :-

$$-V_{DD} + I_D R_D + V_{DS} = 0$$

$$V_{DS} = V_{DD} - I_D R_D \quad \text{--- D.C.L.L eqn}$$

$$\text{Slope} = -\frac{1}{R_D}$$



① for $I_D = 0 \Rightarrow V_{DS} = V_{DD} = 5\ V.$

$P_1 (5V, 0)$

[2] For $V_{DS} = 0 \Rightarrow I_D = \frac{V_{DD}}{R_D}$

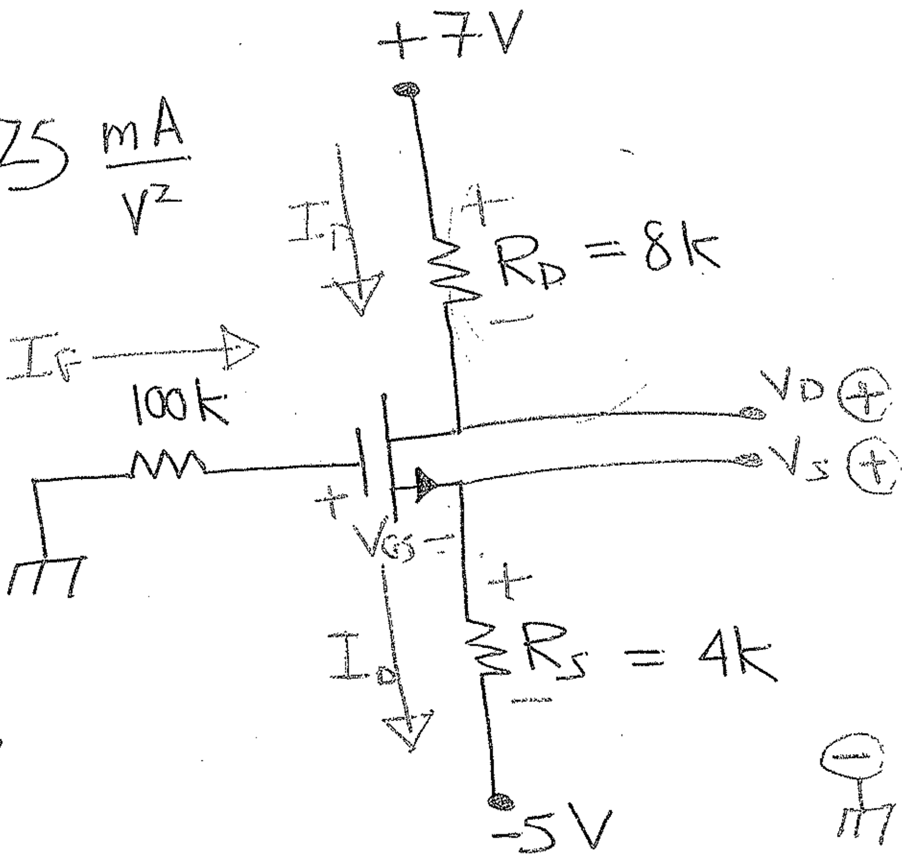
$= \frac{5}{10} = 0.5\,mA.$

$P_2 (0, 0.5\,mA)$

EXA:

Given: $K_n = 0.25 \frac{mA}{V^2}$

$V_{TN} = 1V.$



Find:

① Calculate

V_{GS}, I_D, V_D, V_S,

V_{DS}, P_D

② Write D.C.L.L Equ. & find its slope.

Sol. Assume the MOSFET in Sat. :-

$$I_D = K_n (V_{GS} - V_{TN})^2 \quad \text{——— ①}$$

$$I_G R_G + V_{GS} + I_D R_S - 5 = 0$$

$$V_{GS} = 5 - I_D R_S = 5 - 4 I_D$$

$$\therefore I_D = \frac{5 - V_{GS}}{4} \quad \text{——— ②}$$

Subs. (2) in (1):

$$\frac{5 - V_{GS}}{4} = 0.25\,(V_{GS} - 1)^2$$

$$5 - V_{GS} = (V_{GS}^2 - 2V_{GS} + 1)$$

$$V_{GS}^2 - V_{GS} - 4 = 0$$

$$V_{GS} = \frac{-(-1)^2 \pm \sqrt{(-1)^2 - (-4*1)}}{2}$$

$$= \frac{1 \pm \sqrt{17}}{2} \Rightarrow \frac{1 - 4.1}{2} = -1.6$$

$$\text{or} \Rightarrow \frac{1 + 4.1}{2} = 2.5$$

$\therefore V_{GS} = 2.5\ V$ ✓ القيمة الموجبة

$$I_D = \frac{5 - 2.5}{4} = 0.6\ mA$$

اذا كانت القيمة موجبة نأخذ الاكبر من V_{TN}

V_D ?

$-7 + R_D I_D + V_D = 0$

$V_D = 7 - 0.6 * 8 = 2.2\ V$ ✓

V_S ?

$-V_S + I_D R_S - 5 = 0$

$V_S = I_D R_S - 5 = 0.6 * 4 - 5$

$= -2.6 V.$

V_{DS} ?

~~✗~~ $-V_{DD} + I_D R_D + V_{DS} + I_D R_S - 5 = 0$

$V_{DS} = 7 * 5 - 0.6(8+4)$

$= 12 - 7.2 = 4.8\ V.$

#.

$V_{DS(sat.)} = V_{GS} - V_{TN}$

$= 2.5 - 1 = 1.5\,V$

$V_{DS} > V_{DS(sat.)}$

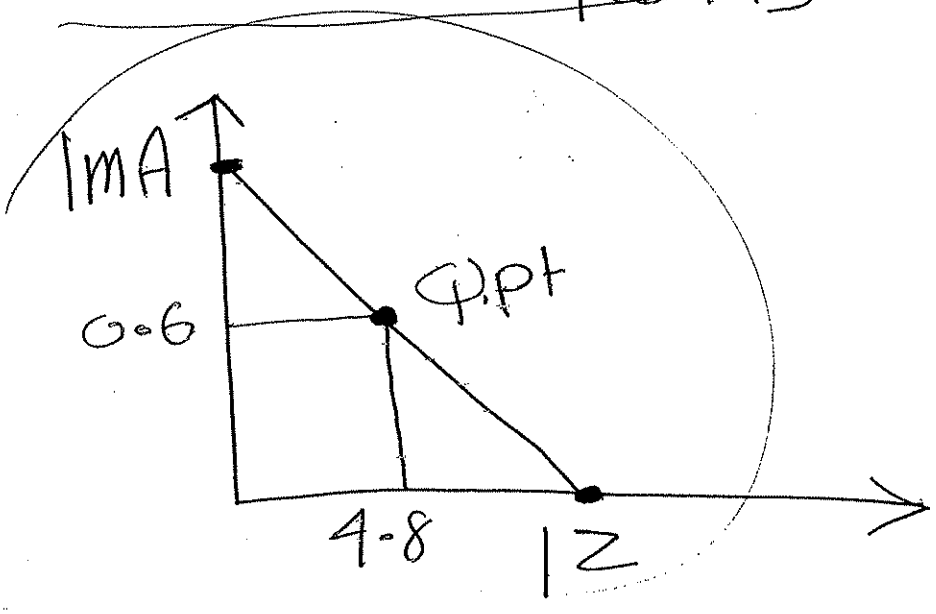
$\therefore$ MOSFET in Sat.

(2) D.C.L.L:

$-V_{DD} + I_D R_D + V_{DS} + I_D R_S - 5 = 0$

$V_{DS} = 12 - I_D (R_D + R_S)$

$Slope = -\frac{1}{R_D + R_S}$



$V_{DD} \uparrow \rightarrow$ Q-pt : right

$R_D \uparrow \rightarrow$ Q-pt : left.

R_S , V_{GS} تؤثر $\rightarrow$ V_{DS} and I_D

فتؤثر على الـ Q-pt
للأعلى والاسفل واليمين واليسار
اذا تغيرة I_D اذا تغيرة V_{DS}

---

* If $R_S = 0$, then: $V_{GS} = V_G - V_S$
$V_S = -5V$

$V_{GS} = 5V$

$I_D = 0.25(5-1)^2 = 4mA$

$V_{DS} = 12 - I_D R_D = 12 - 4*8 = -20V$

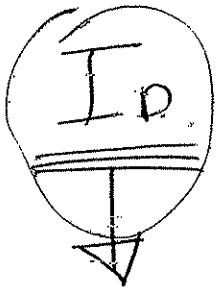
$V_{DS(sat)} = V_{GS} - V_{TN} = 5-1 = 4V$

∴ MOSFET in NON sat. (linear) S

$$I_D = K_n \left[2(V_{GS} - V_{TN}) V_{DS} - V_{DS}^2 \right]$$

$$I_D = 0.25 \left[2(5-1) V_{DS} - V_{DS}^2 \right]$$

$$I_D = 2 V_{DS} - 0.25 V_{DS}^2$$



$$-7 + I_D R_D + V_{DS} - 5 = 0$$

$$I_D = \frac{12 - V_{DS}}{8k}$$

$$\Rightarrow \frac{12 - V_{DS}}{8k} = 2V_{DS} - 0.25 V_{DS}^2$$

$$12 - V_{DS} = 16 V_{DS} - 2 V_{DS}^2$$

$$2V_{DS}^2 - 17 V_{DS} + 12 = 0$$

$$V_{DS} = \frac{17 \pm \sqrt{(17)^2 - 4 * 2 * 12}}{4}$$

$$= \frac{17 \pm \sqrt{193}}{4} = \frac{17 \mp 19}{4}$$

$$\Rightarrow 0.75$$

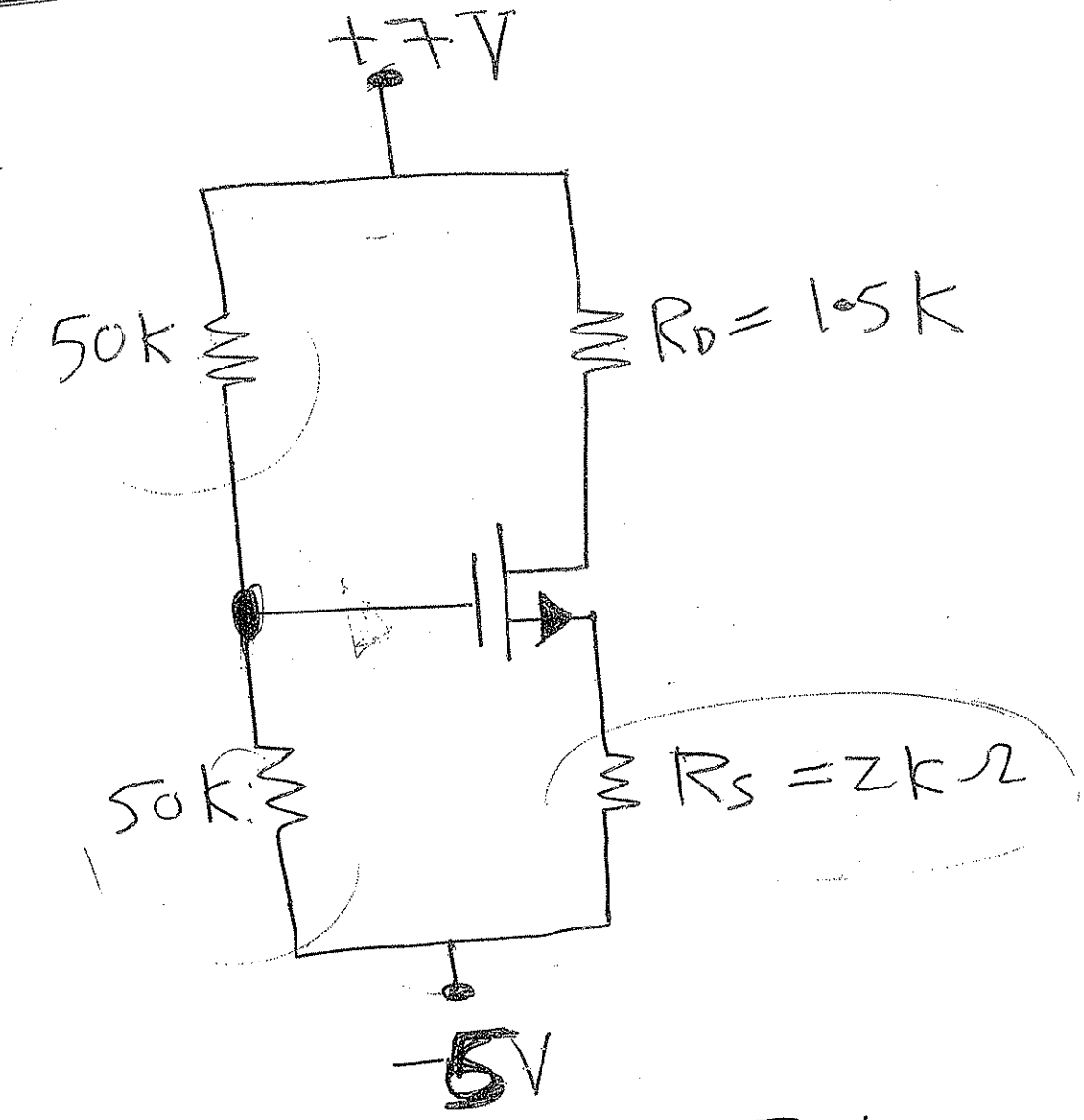
$V_{DS(Sat)}$ أو V_{DS}

or $\Rightarrow 7.5$

$$I_D = \frac{12 - 6.4}{8} = \frac{11.6}{8}$$

$$= 1.3 \text{ mA}$$

EXA:



$k_n = 0.5 \text{ mA/V}^2$, $V_{TN} = 2V$

① calculate V_{GS}, V_S, V_D, I_D, V_{DS}, P_D

② Draw D.C.L.L & indicate Q.pt

Sol:

$$I_D = K_n (V_{GS} - V_{TN})^2$$

$$V_{GS} = V_G - V_S$$

$$V_G = \frac{7 * R_2}{R_1 + R_2} + \frac{(-5) R_1}{R_1 + R_2}$$

$$= \frac{7 * 50}{100} - \frac{5 * 50}{100} = 1\,V$$

$|V_S| \neq 0$: $V_G = \frac{(7 - -5) R_2}{R_1 + R_2} + (-5)$

$$= \frac{12 * 50}{100} - 5 = 1\,V$$

$$V_S = I_D R_S - 5$$

$$V_S = 2 I_D - 5$$

$$V_{GS} = V_G - V_S$$

$$= 1 - 2I_D + 5 = 6 - 2I_D$$

$$I_D = \frac{6 - V_{GS}}{2} = 0.5\,(V_{GS}^2 - 4V_{GS} + 4)$$

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$$6 - V_{GS} = V_{GS}^2 - 4V_{GS} + 4$$

$$V_{GS}^2 - 3V_{GS} - 2 = 0$$

$$V_{GS} = \frac{3 \mp \sqrt{9 - (4*1*-2)}}{2}$$

$$\Longrightarrow V_{GS} = \boxed{3.5}\ \checkmark$$

$$\text{or} \Longrightarrow V_{GS} = \frac{3 - \sqrt{17}}{2} = \underline{-0.5}$$

$$I_D = \frac{6 - 3.5}{2} = 1.25\ \text{mA}.$$

$$V_S = 1.25 * 2.5 = -2.5\,\text{V}.$$

$$V_D = 7 - 1.25 * 1.5 = 5.2\,\text{V}.$$

$$V_{DS} = 5.2 - (-2.5) = 7.7\,\text{V}\ \#$$

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(1) $P_D = I_D V_{DS}$

$= 1.25 * \quad 7.7 = 9.5\,mW.$

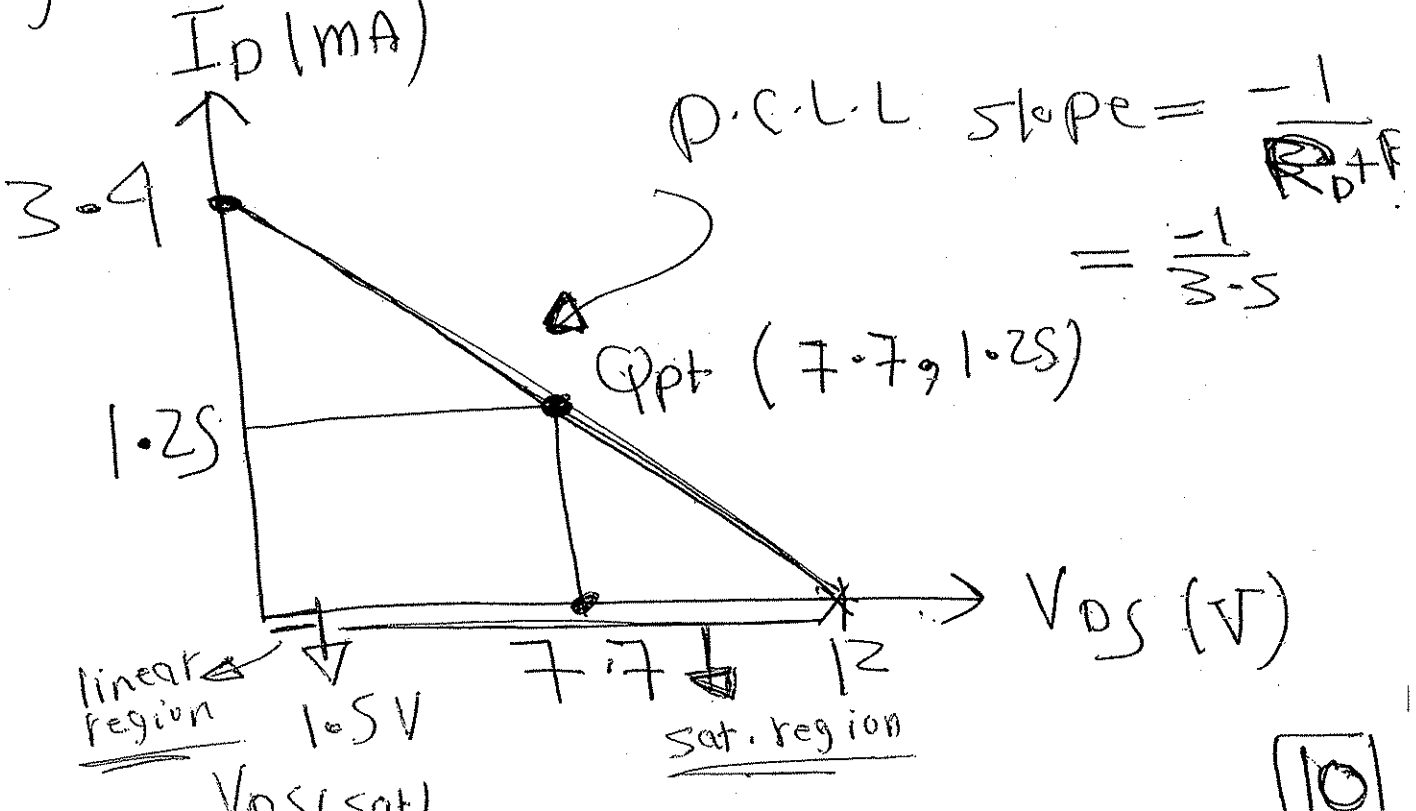
(2) D.C.L.L:.

$$-V_{DD} + I_D R_D + V_{DS} + I_D R_S - 5 = 0$$

$$V_{DS} = V_{DD} + V_{SS} - I_D * (R_D + R_S)$$

for $I_D = 0$, $V_{DS} = V_{DD} + V_{SS} = 12V$

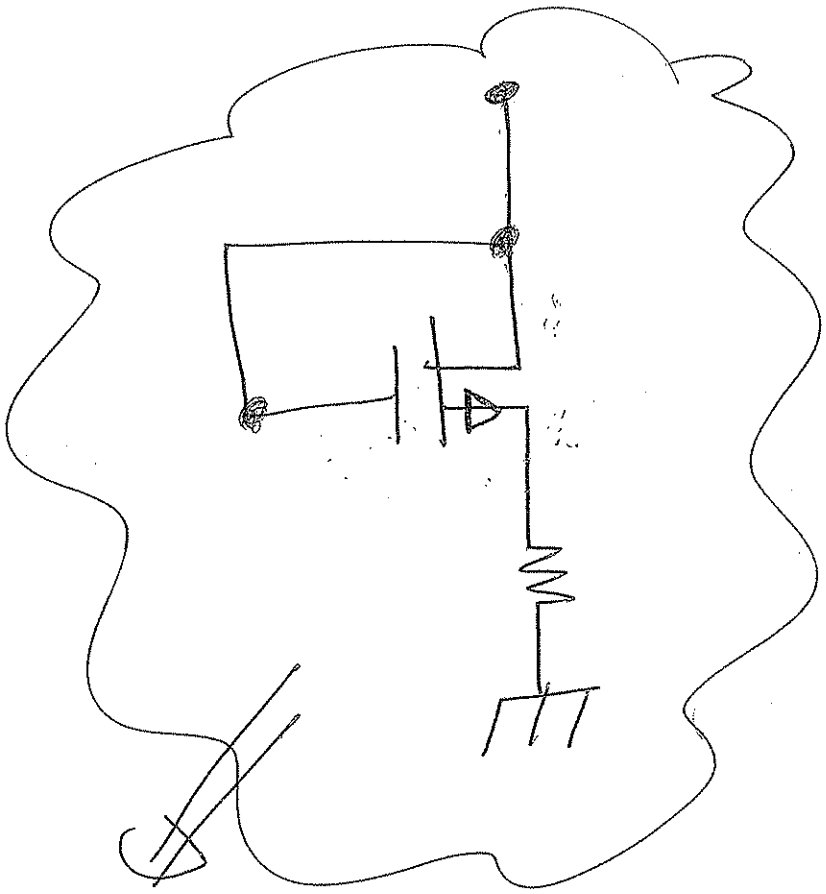
for $V_{DS} = 0$, $I_D = \frac{12}{3.5k} = 3.4$ mA



$R_2 = 0$;— $V_G = 7$

$-7 + R_1 * I_G + V_G = 0$

$V_G = 7$



Sat. Region ليش؟

$V_{DS} \geq V_{DS(sat)}$ → $V_G = V_D$

$V_{GS} = V_{DS}$

Ele 1 : ١١/٨/٦ الاسيـن

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Multitransistors CCts :

1) Cascade Config. :-

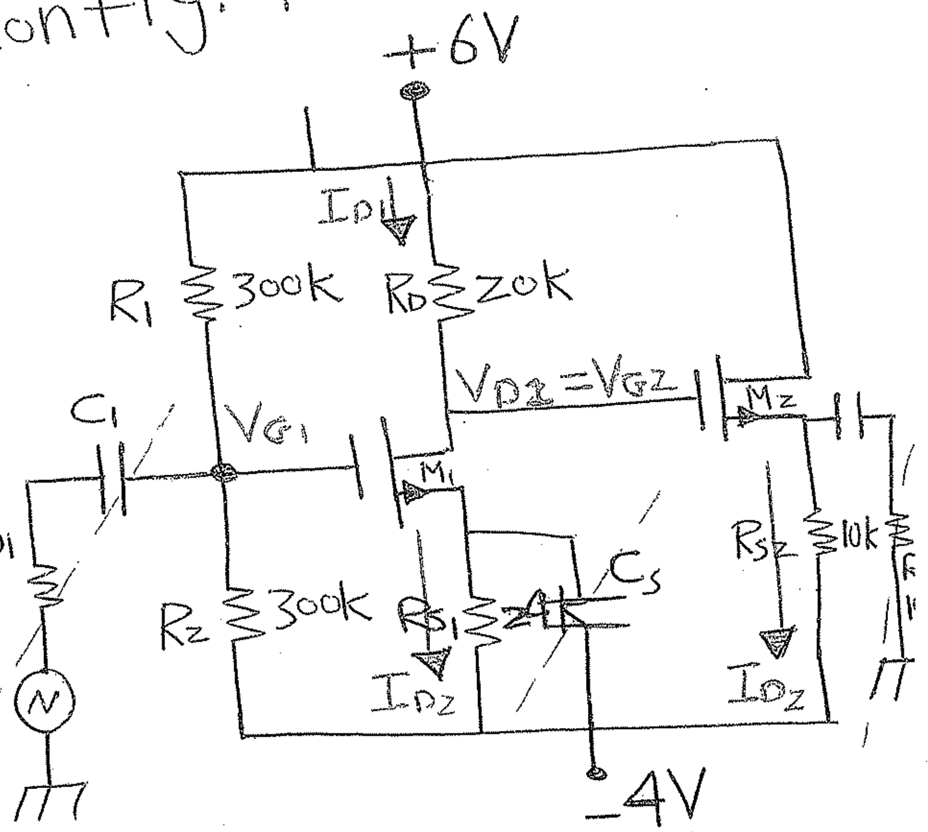
Given:

$k_{n1} = 0.5 mA/V^2$

$k_{n2} = 0.2 mA/V^2$

$V_{TN1} = V_{TN2} = 1V$

Calculate : V_{GS1} , I_{D1} , V_{S1} , V_{G1} , V_{DS1} , V_{GS2} , I_{D2} , V_{S2} , V_{DS2} .



Sol.

all cap.s are open → D.C Analysis .

Assume M_1 & M_2 in Sat. Region :-

$$I_{D1} = k_{n1} (V_{GS1} - V_{TN1})$$

$$V_{GS1} = V_{G1} - V_{S1}$$

$$V_{G1} = \frac{6 * R_2}{R_1 + R_2} + \frac{(-4) * R_1}{R_1 + R_2}$$

$$= 3 - 2 = 1V .$$

$$-V_{S1} + I_{D1} R_{S1} - 4 = 0$$

$$V_{S1} = 24\, I_{D1} - 4$$

$$V_{GS1} = 1 + 4 - 24\, I_{D1}$$

$$V_{GS1} = 5 - 24\, I_{D1}$$

$$I_{D1} = \frac{5 - V_{GS1}}{24}$$

$$* \quad \frac{5 - V_{GS1}}{24} = 0.5 (V_{GS1} - 1)^2$$

$$5 - V_{GS1} = 12 (V_{GS}^2 - 2V_{GS1} + 1)$$

$$12 V_{GS1}^2 - 23 V_{GS1} + 7 = 0$$

$$V_{GS1} = \frac{23 \mp \sqrt{(23)^2 - 4 * 12 * 7}}{24}$$

$$= \frac{23 \mp \sqrt{600 - 330}}{24}$$

$$= \frac{23 \mp \sqrt{270}}{24}$$

$$\rightarrow 1.53\ V \checkmark$$

$$\rightarrow 0.38\ V$$

$$I_{D1} = \frac{5 - 1.53}{24} = \frac{3.5}{24} = 0.14\,mA$$

[2]

$$V_{S1} = 0.14 * 24 - 4$$
$$= -0.64\,V$$

$$V_{D1} = 6 - I_{D1} R_D$$
$$= 6 - 0.14 * 20 = 6 - 2.8 = 3.2\,V$$

$$V_{DS1} = V_{D1} - V_{S1} = 3.2 - (-0.64)$$
$$= 3.8\,V.$$

$$* I_{DZ} = k_{nZ} (V_{GSZ} - V_{TNZ})$$

$$V_{GSZ} = V_{GZ} - V_{SZ}$$

$$V_{GZ} = V_{D1} = 3.2\,V$$

$$-V_{SZ} + I_{DZ} R_{SZ} - 4 = 0$$

$$\boxed{V_{SZ} = 10 I_{DZ} - 4}$$

$$V_{GSZ} = 3.2 + 4 - 10 I_{DZ}$$

$$V_{GSZ} = 7.2 - 10 I_{DZ}$$

$$I_{DZ} = \frac{7.2 - V_{GSZ}}{10}$$

$$\frac{7.2 - V_{GSZ}}{10} = 0.2\left(V_{GS}^2 - 2V_{GSZ} + 1\right)$$

$$7.2 - V_{GSZ} = 2V_{GSZ}^2 - 4V_{GSZ} + 2$$

$$2V_{GSZ}^2 - 3V_{GSZ} - 5.2 = 0$$

$$V_{GSZ} = \frac{3 \mp \sqrt{(3)^2 + 1*2*5.2}}{4}$$

$$= \frac{3 \mp 7}{4} = 2.5\ V \checkmark$$

or: $-1\ V$ ×

$$\therefore \boxed{V_{GSZ} = 2.5\ V}$$

$$I_{DZ} = \frac{7.2 - 2.5}{10} = \frac{4.7}{10} = 0.47mA$$

$$V_{SZ} = 10 * 0.47 - 4 = 0.7\ V$$

$$V_{DZ} = 6\ V$$

$$V_{DSZ} = 6 - 0.7 = 5.3\ V$$

[4]

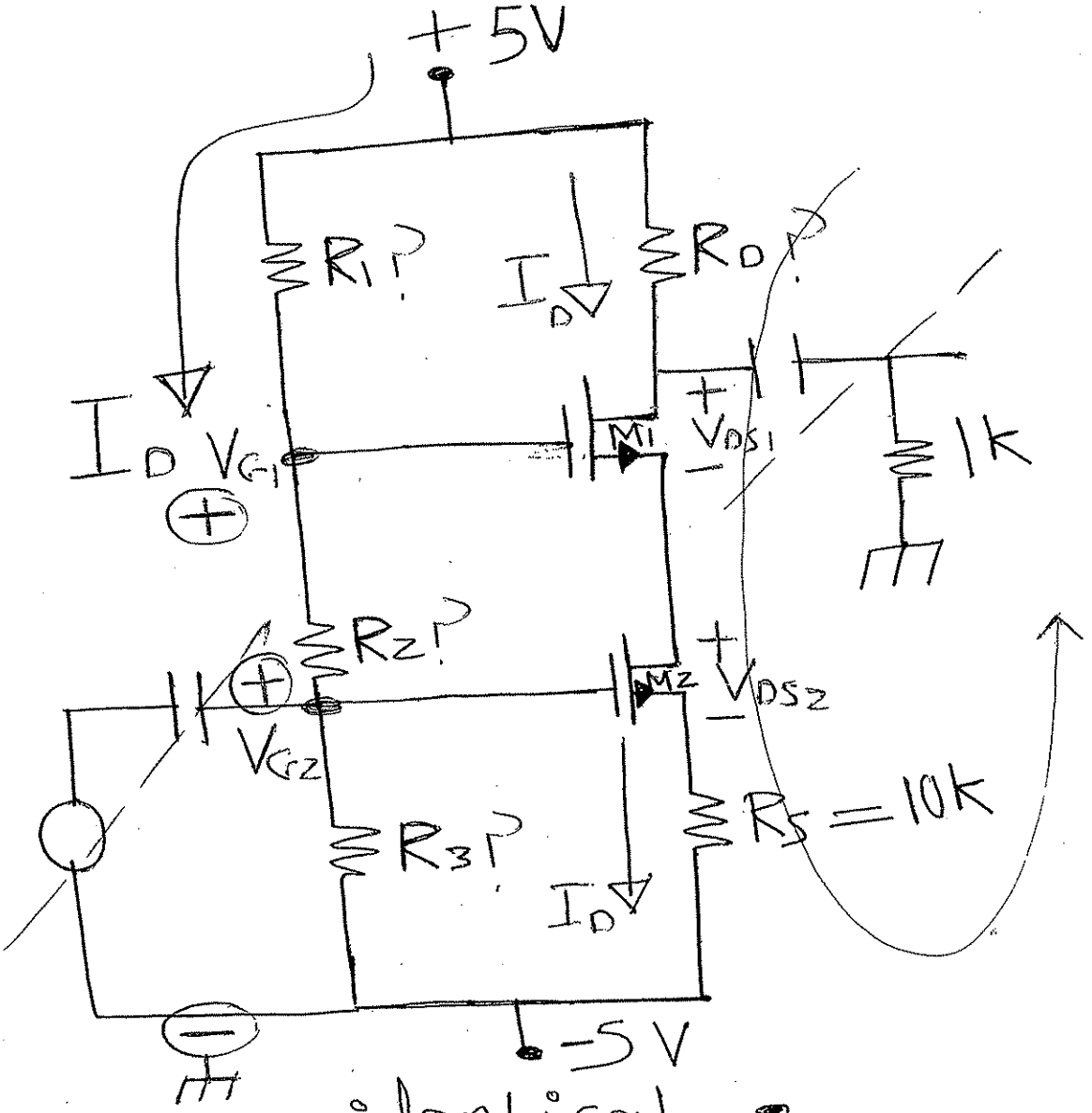
DCLL for M_2 :-

$$-6 + V_{DS_2} + I_{D_2} R_{S_2} - 4 = 0$$

$$V_{DS_2} = 10 - I_{D_2} R_{S_2}$$

$$\text{Slope} = -\frac{1}{R_{S_2}}$$

2) Cascode Config. :—



M_1 & M_2 are identical ,

$k_n = 0.5\ mA/V^2$

$V_{TN} = 1V$

Design the cct. such that :

$I_{DQ} = 0.25\ mA$.

$V_{DS1} = V_{DS2} = 3V$

(choose $R_T = R_1 + R_2 + R_3 = 500k$) [6]

Sol.

$R_D = ?$

$$-5 + I_D R_D + V_{DS_1} + V_{DS_2} + I_D R_S - 5 = 0$$

$$I_D R_D = 5 + 5 - 3 - 3 - 0.25 * 10$$

$$= 1.5\ V$$

$$R_D = \frac{1.5\ V}{0.25\ mA} = 6\ k\Omega.$$

$$R_3 = \frac{V_{G_2} + 5}{I}$$

$$I = \frac{5 - (-5)}{R_T} = \frac{10}{500k} = 0.02\ mA$$

$$-V_{G_2} + V_{GS_2} + I_D R_S - 5 = 0$$

$$V_{G_2} = V_{GS_2} + I_D R_S - 5$$

$$I_{D_2} = k_n (V_{GS_2} - V_{TN})^2$$

$$V_{GS_2} = \mp \sqrt{\frac{I_D}{k_n}} + V_{TN}$$

$$= \mp \sqrt{\frac{0.25}{0.5}} + 1 = \mp 0.7 + 1 = 1.7\ V$$

7

$$V_{G2} = 1.7 + 0.25 * 10^{-5}$$

$$= -0.8$$

$$-V_{G2} + I R_3 - 5 = 0$$

$$R_3 = \frac{V_{G2} + 5}{I} = \frac{4.2\ V}{0.02\ m} = 210k\Omega$$

$$R_2 = \frac{V_{G1} - V_{G2}}{I}$$

$$-V_{G1} + V_{GS_1} + V_{DS_2} + I_D R_S - 5 = 0$$

$$V_{G1} = V_{GS_1} + V_{DS_2} + I_D R_S - 5$$

$$R_2 =$$

$$R_1 = \frac{5 - V_{G1}}{I}$$

عدنان عبد الفتاح الحوراني

د. هادي العناوي

MOSFET

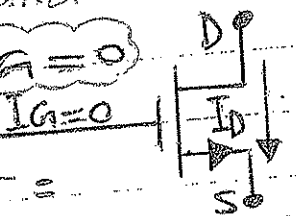
Unipolar Transistor !! (1)

MOSFET: It refers to Metal oxide Semiconductor Field Effect Transistor.

It is three terminals device Source, Drain and gate.

The distance between Drain and Source is called channel.

The gate is isolated (معزول) from drain and Source by a layer of oxide So allways $I_G = 0$ and $I_D = I_S$.



There are two types of MOSFET = Enhancement MOSFET and Depletion MOSFET.

Each type is classified into: n-channel and p-channel

In n-channel: The Carriers are electrons

In p-channel: The Carriers are Holes.

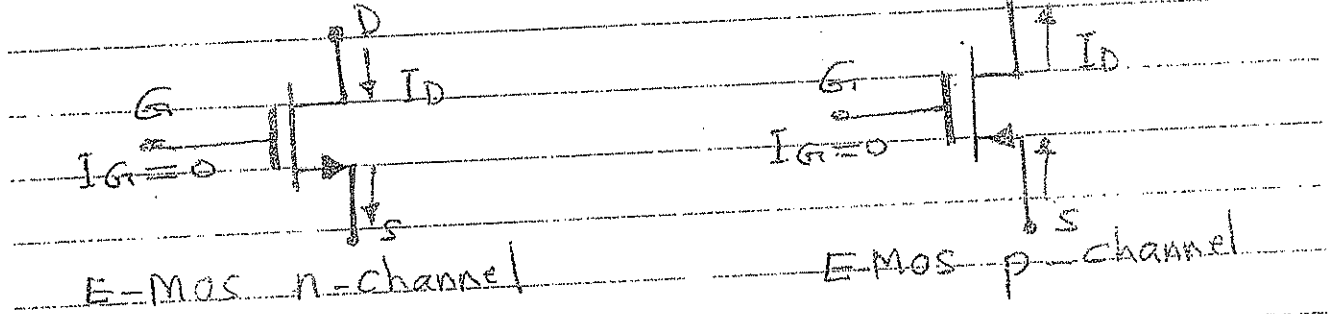
In Depletion MOSFET, there is a channel physically exists between Source & Drain, It requires only small voltage on drain to start a current So it is called "Normally ON" device (It works even when $V_{GS}=0$).

In Enhancement MOSFET, The channel is electronically induced when a certain voltage is applied between gate and Source (V_{GS}).

To establish a channel, the value of V_{GS} must be > certain voltage, Called Threshold Voltage: V_{TN} → For n-channel and is +ve

V_{TP} → For p-channel and is -ve.

The symbols for E-Mos and D-Mos are shown

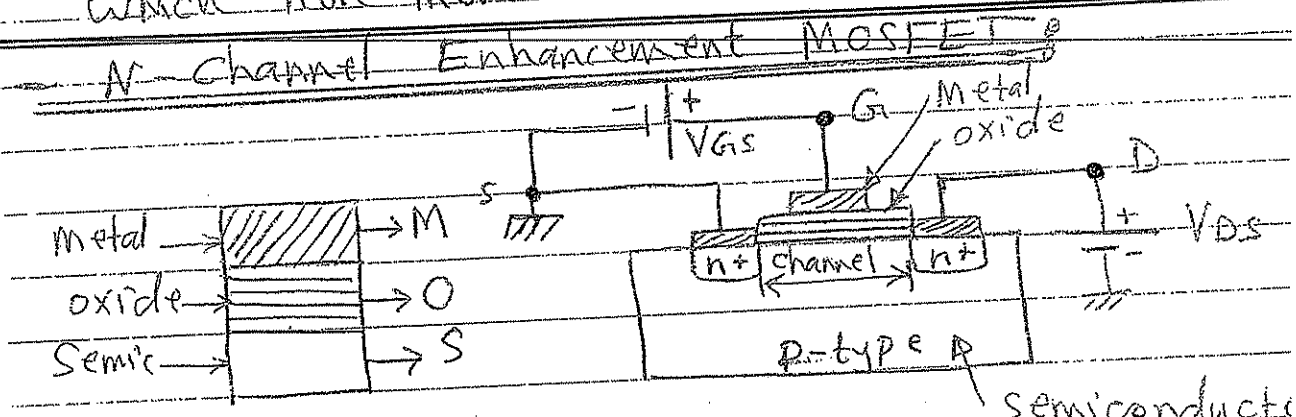


E-Mos n-channel E-Mos p-channel

D-Mos n-channel D-Mos p-channel

The direction of arrow head refers to the conventional direction of Drain Current I_D which hole movement direction.

N-Channel Enhancement MOSFET

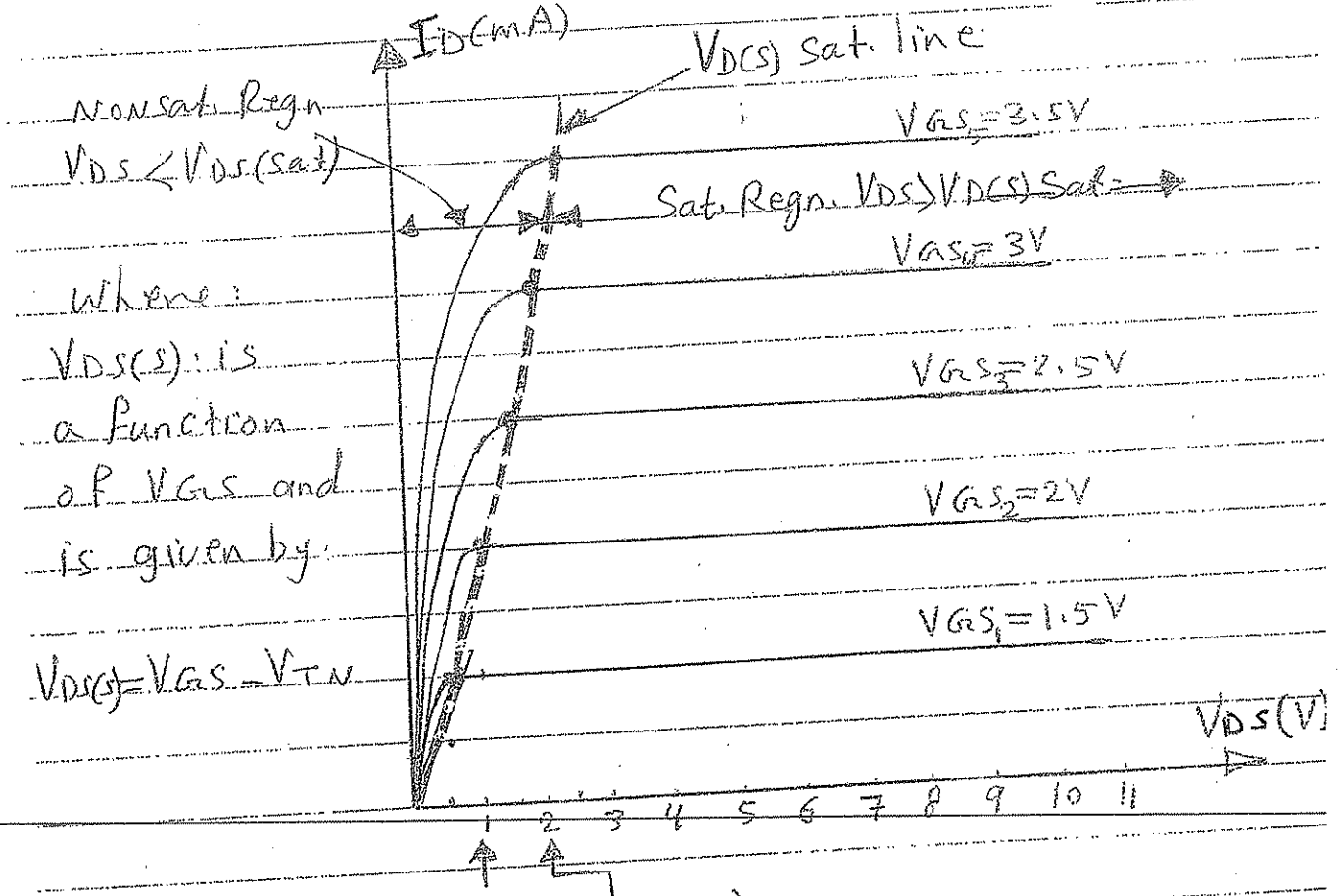


Gate structure

operation: For $V_{GS} > V_{TH}$, there is electromic channel under gate, when +ve V_{DS} is applied electrons flow from source to drain, So the conventional direction of I_D is from D → S

Ideal Current-Voltage characteristics of NMOS

The I-V characteristic for n-channel E-MOS is shown in Fig.



where:
VDS(S): is a function of VGS and is given by:

$V_{DS(S)} = V_{GS} - V_{TN}$

As shown, there are two operation regions:

① Linear Region or Nonsaturation Regn.:

The MOSFET will be in this Region when:
$V_{DS} < V_{DS(sat)}$ where $V_{DS(sat)} = V_{GS} - V_{TN}$.

The drain Current is given by:

$$I_D = K_n\left[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2\right]$$

where: K_n: Conduction parameter given in (mA/V^2) and given data sheet:

V_{TN} : Threshold voltage for n-channel (given) and it is +ve value. The MOSFET is used as a Resistor

(2) Saturation Region :

The MOSFET will be in Saturation Regn. when $V_{DS} > V_{DS(sat)}$, I_D is independant on V_{DS} and is given by : $I_D = K_n (V_{GS} - V_{TN})^2$

In this Regn. the MOSFET is used as an Amplifier

D.C Analysis OF MOSFET ccts :

EXA 1; Given the parameters for the MOSFET shown in Fig : $V_{TN} = 1V$, $K_n = 0.1 mA/V^2$

(1) Calculate V_{GS}, I_D, V_{DS} and P_D.

(2) Draw D.C.L.L and indicate Q-pt

To perform D.C Analysis :

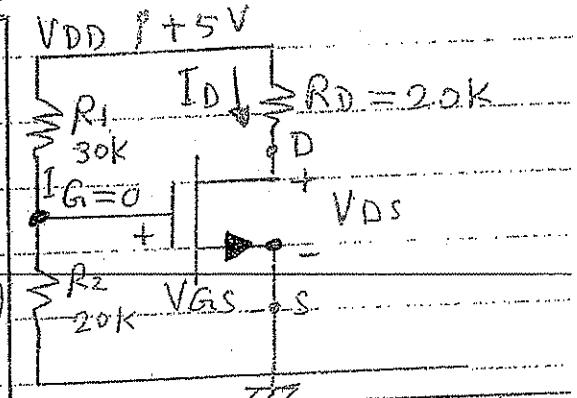
(a) Assume the MOSFET in Sat Region and find I_D, V_{DS}, $V_{DS(sat)}$

(b) Compare V_{DS} and $V_{DS(sat)}$

(c) If $V_{DS} > V_{DS(sat)}$, then the MOSFET is indeed in Sat. and the values are Correct. (Use $I_D = K_n (V_{GS} - V_{TN})^2$)

(d) If $V_{DS} < V_{DS(sat)}$, then the MOSFET is in nonsat. Regn. and you must use :

$I_D = K_n [2(V_{GS} - V_{TN}) V_{DS} - V_{DS}^2]$.



Solution : Assume the MOSFET in Sat. Regn.

$$V_{GS} = V_G - V_S = \frac{5 \times R_2}{R_1 + R_2} - 0 = \frac{5 \times 20}{50} - 0 = 2V$$

$$I_D = K_n (V_{GS} - V_{TN})^2 = 0.1 (2-1)^2 = 0.1 \times 1 = 0.1 mA$$

$V_{DD} + I_D R_D + V_{DS} = 0$

$\therefore V_{DS} = V_{DD} - I_D R_D = 5 - 0.1 \times 20 = 3V$

$V_{DS(sat)} = V_{GS} - V_{TN} = 2 - 1 = 1V$

Since $V_{DS} > V_{DS(sat)}$ $\therefore$ MOSFET is in Sat. Regn.

P_D : power dissipation in MOSFET

$P_D = I_D . V_{DS} = 0.1 \times 3 = 0.3 mW$

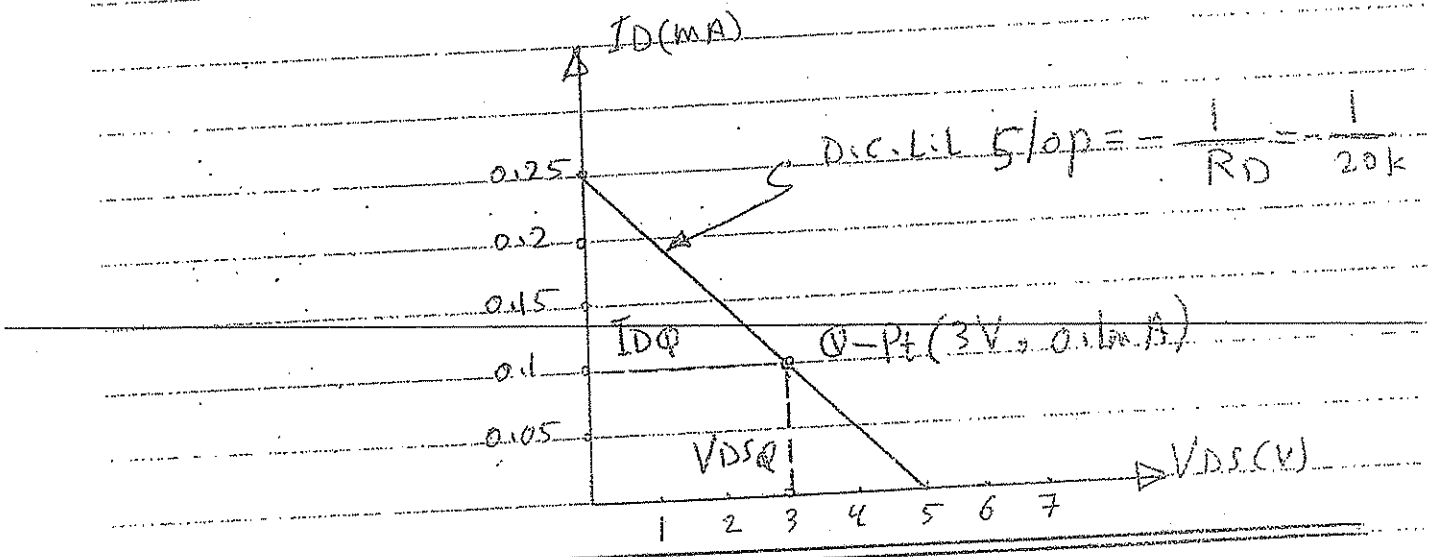
(2) D.C.L.L

$-V_{DD} + I_D R_D + V_{DS} = 0$

$\therefore V_{DS} = V_{DD} - I_D R_D$ D.C.L.L Eqn:

(i) for $I_D = 0$, $V_{DS} = V_{DD} = 5V \rightarrow P_1 (5V, 0mA)$

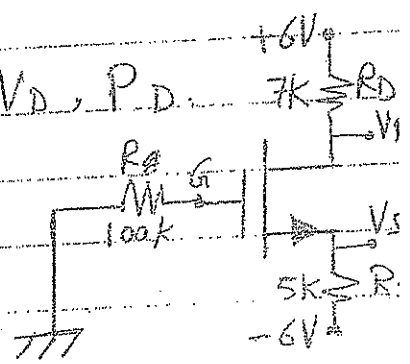
(ii) for $V_{DS} = 0$, $I_D = \frac{V_{DD}}{R_D} = \frac{5}{20} = 0.25 mA \rightarrow P_2 (0, 0.25mA)$



EXA 2: For the ckt. shown, the MOSFET shown: $V_{TN} = 1.0V$, $K_n = 0.25 mA/V^2$.

(i) Calculate V_{GS}, I_D, V_{DS}, V_S, V_D, P_D.

(ii) Draw D.C.L.L and indicate Q-pt. position.



(6) 2M

Assume the MOSFET in Sat:

$I_D = K_n (V_{GS} - V_{TN})^2$ ——— ① $\to 0$

$V_{GS} = V_G - V_S$, $V_G = I_G R_G = 0V$

$-V_S + I_D R_S - 6 = 0$

$\therefore V_S = I_D \times 5 - 6$

$\therefore V_{GS} = 0 - (5 I_D - 6)$

$\therefore V_{GS} = 6 - 5 I_D$

$\therefore I_D = \frac{6 - V_{GS}}{5}$ ——— ②

Substitute ② in Eqn. ①

$\frac{6 - V_{GS}}{5} = 0.25 (V_{GS} - 1)^2$

$6 - V_{GS} = 1.25 (V_{GS}^2 - 2V_{GS} + 1)$

$6 - V_{GS} = 1.25 V_{GS}^2 - 2.5 V_{GS} + 1.25$

$\therefore 1.25 V_{GS}^2 - 1.5 V_{GS} - 4.75 = 0$

$V_{GS} = \frac{1.5 \mp \sqrt{(-1.5)^2 - 4 \times 1.25 (-4.75)}}{2 \times 1.25} = \frac{1.5 - 5.1}{2.5}$ or $\frac{1.5 + 5.1}{2.5}$

$\therefore V_{GS} = -1.44V$ or $V_{GS} = 2.64V$

The Correct value is 2.64V (because it is +ve and $> V_{TN}$) Since the MOSFET is n-channel

$\therefore I_D = \frac{6 - 2.64}{5} = 0.672 mA$

$V_S = 0.672 \times 5 - 6 = -2.64V = -V_{GS}$

$V_D = 6 - I_D R_D = 6 - 0.672 \times 7 = 1.296 V$

$V_{DS} = V_D - V_S = 1.296 - (-2.64) = 3.936 V$

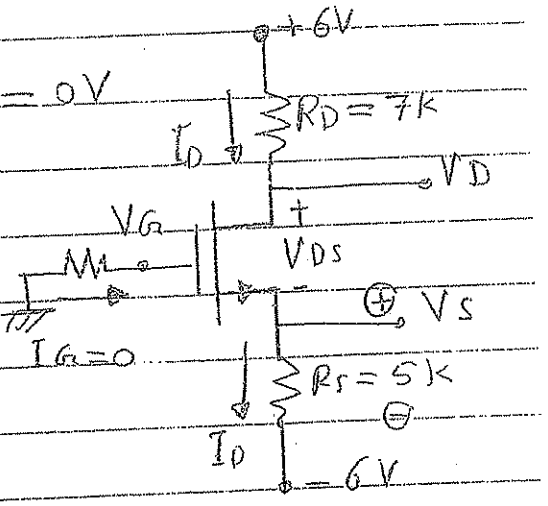
$V_{DS(sat)} = (V_{GS} - V_{TN}) = 2.64 - 1 = 1.64V$

Since $V_{DS} > V_{DS(sat)} \Longrightarrow$ MOSFET is in Sat.

$P_D = I_D . V_{DS} = 0.672 \times 3.936 = 2.644 mW$

② D.C.L.L Eqn.

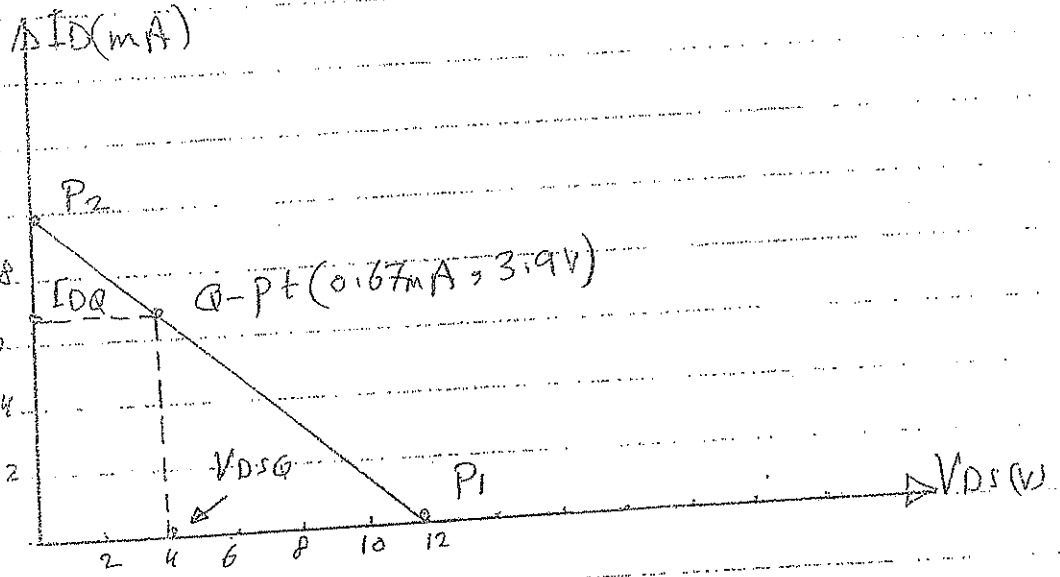
$-V_{DD} + I_D R_D + V_{DS} + I_D R_S - 6 = 0$



$V_{DS} = 6 + 6 - I_D(R_D + R_S) = 12 - I_D(R_D + R_S)$ D.C.L.L Eqn.

for $I_D = 0 \Rightarrow V_{DS} = 12V \rightarrow P_1(12V, 0mA)$

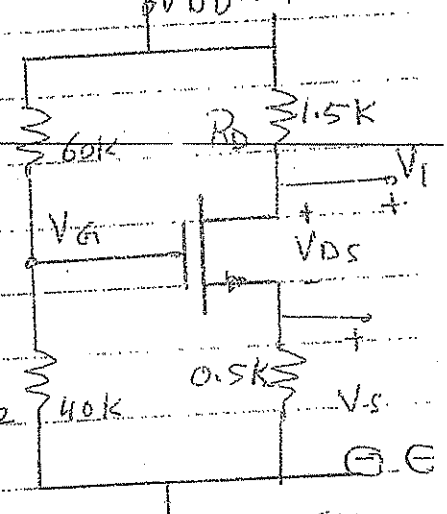
for $V_{DS} = 0 \Rightarrow I_D = \frac{12}{R_D + R_S} = \frac{12}{12} = 1mA \rightarrow P_2(0, 1mA)$



EXA. 3: For the cct. shown, the MOSFET has: $K_n = 0.5 mA/V^2$, $V_{TN} = 2V$

Calculate: V_{GS}, I_D, V_{DS}, V_D, V_S, P_D.

Assume the MOSFET in Sat. Regn.



$I_D = K_n (V_{GS} - V_{TN})^2$ ——— (1)

$V_{GS} = V_G - V_S$

$V_G = \frac{6 \times 40}{100} - \frac{6 \times 60}{100} = 2.4 - 3.6 = -1.2V$

$V_S = I_D R_S = 6 = 0.5 I_D - 6$

$\therefore V_{GS} = -1.2 - (0.5 I_D - 6)$

$V_{GS} = 4.8 - 0.5 I_D$

$\therefore I_D = \frac{4.8 - V_{GS}}{0.5}$ ——— (2)

Substitute (2) in (1) gives:

$\frac{4.8 - V_{GS}}{0.5} = 0.5 (V_{GS} - 2)^2 \Rightarrow 9.6 - 2V_{GS} = 0.5(V_{GS}^2 - 4V_{GS} + 4)$

$0.5V_{GS}^2 - 7.6 = 0$

$V_{GS}^2 = 15.2 \Rightarrow V_{GS} = \mp\sqrt{15.2} = \mp 3.9\,V$

The Correct Value is: $\boxed{3.9\,V}$

$I_D = \frac{4.8 - 3.9}{0.5k} = 1.8\,mA$

$V_S = I_D R_S = 6 = 1.8 \times 0.5 = 6 = \boxed{-5.1\,V}$

$V_D = V_{DD} - I_D R_D = 6 - 1.8 \times 1.5 = \boxed{3.3\,V}$

$V_{DS} = V_D - V_S = 3.3 - (-5.1) = \boxed{8.4\,V}$

OR: from D-S loop,

$-6 + I_D R_D + V_{DS} + I_D R_S - 6 = 0$

$\therefore V_{DS} = 12 - I_D(R_D + R_S) = 12 - 1.8(1.5 + 0.5) = \boxed{8.4\,V}$

$V_{DS(sat)} = V_{GS} - V_{TN} = 3.9 - 2 = 2.9\,V$

Since $V_{DS} > V_{DS(sat)}$ $\therefore$ MOSFET in Sat. Rgn.

$P_D = I_D V_{DS} = 1.8 \times 8.4 = 15.12\,mW$

D.C.L.L Eqn:

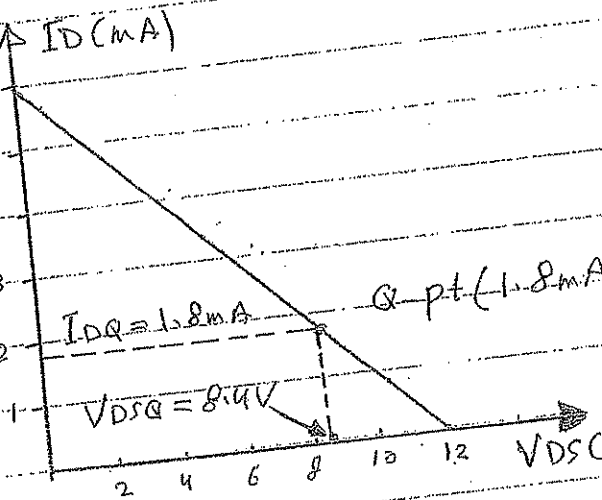
$-6 + I_D R_D + V_{DS} + I_D R_S - 6 = 0$

$\boxed{V_{DS} = 12 - I_D(R_D + R_S)} \Rightarrow$ slope $= -\frac{1}{R_D + R_S} = -\frac{1}{2k\Omega} = -0.5\,\frac{mA}{V}$

for $I_D = 0$, $V_{DS} = 12\,V \Rightarrow P_1(12V, 0)$

for $V_{DS} = 0$, $I_D = \frac{12}{R_D + R_S} = \frac{12}{2} = 6\,mA$

$\therefore P_2(6mA, 0)$



"Suggested problems" أحمد طارق الهيتاوي

D.C MOSFET circuits Analysis & design (9)

Q_1: For the circuit shown in Fig.1
the MOSFET has: $V_{TN} = 2V$, $K_n = 5 mA/V^2$
(i) Calculate V_{GS}, I_D, V_{DS} (ii) Write D.C.L.L Eqn & find slope

Q_2: Design the circuit shown in Fig.2, Such that:
$I_D = 0.5 mA$, $V_D = 1V$. assume the MOSFET has:
$K_n = 0.25 mA/V^2$, $V_{TN} = 1.4V$.

Q_3: For the circuit shown in Fig.3, the MOSFET has:
$V_{TN} = 1V$, $K_n = 0.05 mA/V^2$. calculate V_{GS}, V_{DS}, I_D, P_D

Q_4: For the cct. shown in Fig.4, the MOSFET parameters
are: $K_n = 0.5 mA/V^2$, $V_{TN} = 1V$ (i) Calculate Q-pt. position
(ii) Draw D.C.L.L indicating slope & Q-pt. position.

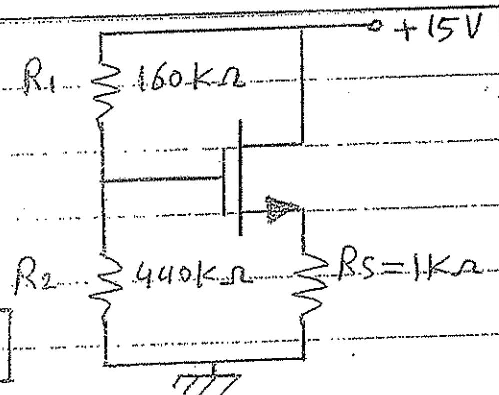


Fig.1

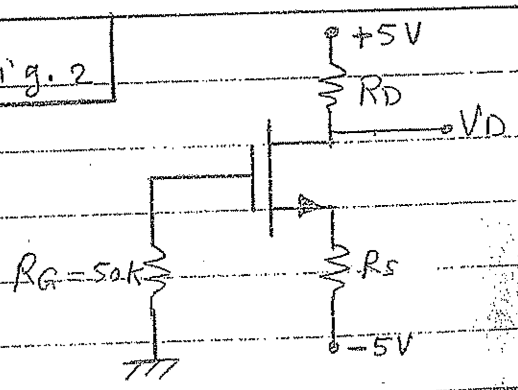


Fig.2

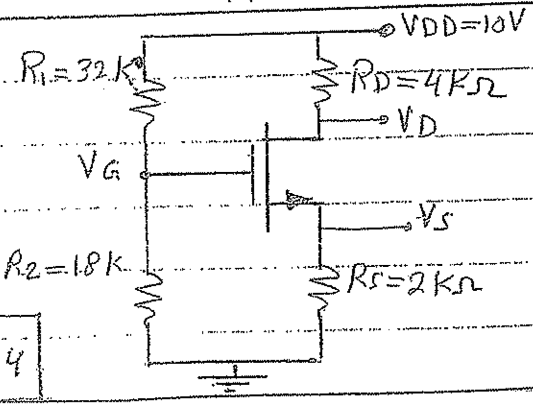


Fig.4

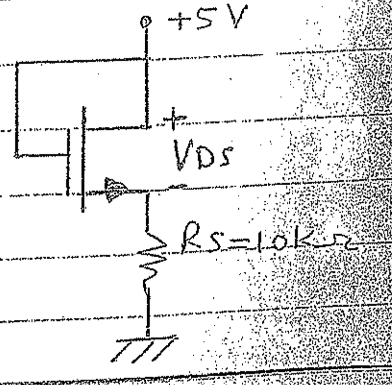


Fig.3

1.15 ZENER DIODES

The Zener region of Fig. 1.45 was discussed in some detail in Section 1.6. The characteristic drops in an almost vertical manner at a reverse-bias potential denoted V_Z. The fact that the curve drops down and away from the horizontal axis rather than up and away for the positive-V_D region reveals that the current in the Zener region has a direction opposite to that of a forward-biased diode. The slight slope to the curve in the Zener region reveals that there is a level of resistance to be associated with the Zener diode in the conduction mode.

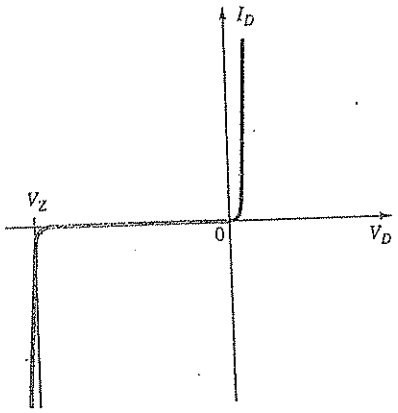


FIG. 1.45
Reviewing the Zener region.

This region of unique characteristics is employed in the design of *Zener diodes*, which have the graphic symbol appearing in Fig. 1.46a. The semiconductor diode and the Zener diode are presented side by side in Fig. 1.46 to ensure that the direction of conduction of each is clearly understood together with the required polarity of the applied voltage. For the semiconductor diode the "on" state will support a current in the direction of the arrow in the symbol. For the Zener diode the direction of conduction is opposite to that of the arrow in the symbol, as pointed out in the introduction to this section. Note also that the polarity of V_D and V_Z are the same as would be obtained if each were a resistive element as shown in Fig. 1.46c.

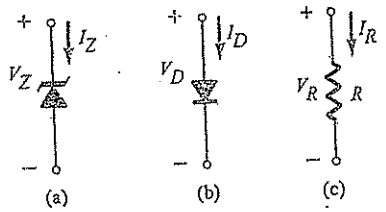


FIG. 1.46
Conduction direction: (a) Zener diode; (b) semiconductor diode; (c) resistive element.

The location of the Zener region can be controlled by varying the doping levels. An increase in doping that produces an increase in the number of added impurities, will decrease the Zener potential. Zener diodes are available having Zener potentials of 1.8 V to 200 V with power ratings from ¼ W to 50 W. Because of its excellent temperature and current capabilities, silicon is the preferred material in the manufacture of Zener diodes.

It would be nice to assume the Zener diode is ideal with a straight vertical line at the Zener potential. Under the condition of a slight slope to the characteristics requiring the piecewise equivalent model appearing in Fig. 1.47 for that region. For most of the applications appearing in this text the series resistive element can be ignored and the reduced equivalent model of just a dc battery of V_Z volts employed. Since some applications of Zener diodes

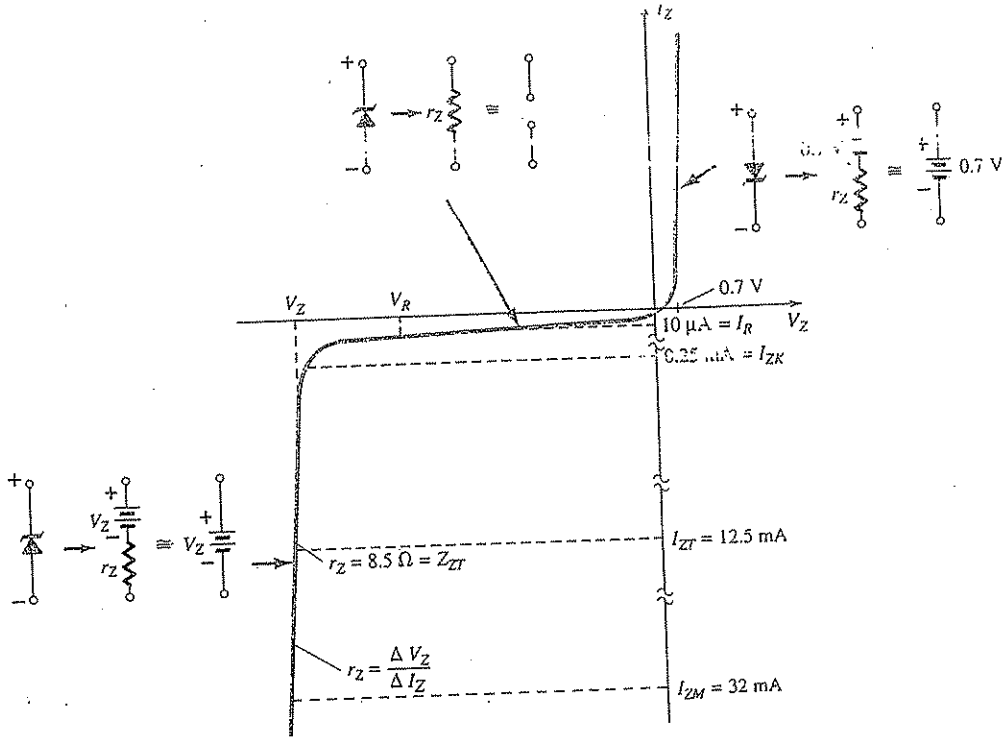


FIG. 1.47
Zener diode characteristics with the equivalent model for each region.

swing between the Zener region and the forward-bias region, it is important to understand the operation of the Zener diode in all regions. As shown in Fig. 1.47, the equivalent model for a Zener diode in the reverse-bias region below V_Z is a very large resistor (as for the standard diode). For most applications this resistance is so large it can be ignored and the open-circuit equivalent employed. For the forward-bias region the piecewise equivalent is the same as described in earlier sections.

The specification sheet for a 10-V, 500-mW, 20% Zener diode is provided as Table 1.7, and a plot of the important parameters is given in Fig. 1.48. The term *nominal* used in the specification of the Zener voltage simply indicates that it is a typical average value. Since this is a 20% diode, the Zener potential of the unit one picks out of a *lot* (a term used to describe a package of diodes) can be expected to vary as 10 V + 20%, or from 8 V to 12 V. Both 10% and 50% diodes are also readily available. The test current I_{ZT} is the current defined by the ¼-power level. It is the current that will define the dynamic resistance Z_{ZT} and appears in the general equation for the power rating of the device. That is,

$$P_{Z_{max}} = 4I_{ZT}V_Z \tag{1.10}$$

Substituting I_{ZT} into the equation with the nominal Zener voltage results in

$$P_{Z_{max}} = 4I_{ZT}V_Z = 4(12.5\,\text{mA})(10\,\text{V}) = 500\,\text{mW}$$

TABLE 1.7
Electrical Characteristics (25°C Ambient Temperature)

Zener Voltage Nominal V_Z (V)	Test Current I_{ZT} (mA)	Maximum Dynamic Impedance Z_{ZT} at I_{ZT} (Ω)	Maximum Knee Impedance Z_{ZK} at I_{ZK} (Ω)	(mA)	Maximum Reverse Current I_R at V_R (μA)	Test Voltage V_R (V)	Maximum Regulator Current I_{ZM} (mA)	Typical Temperature Coefficient (%/°C)
10	12.5	8.5	700	0.25	10	7.2	32	+0.072

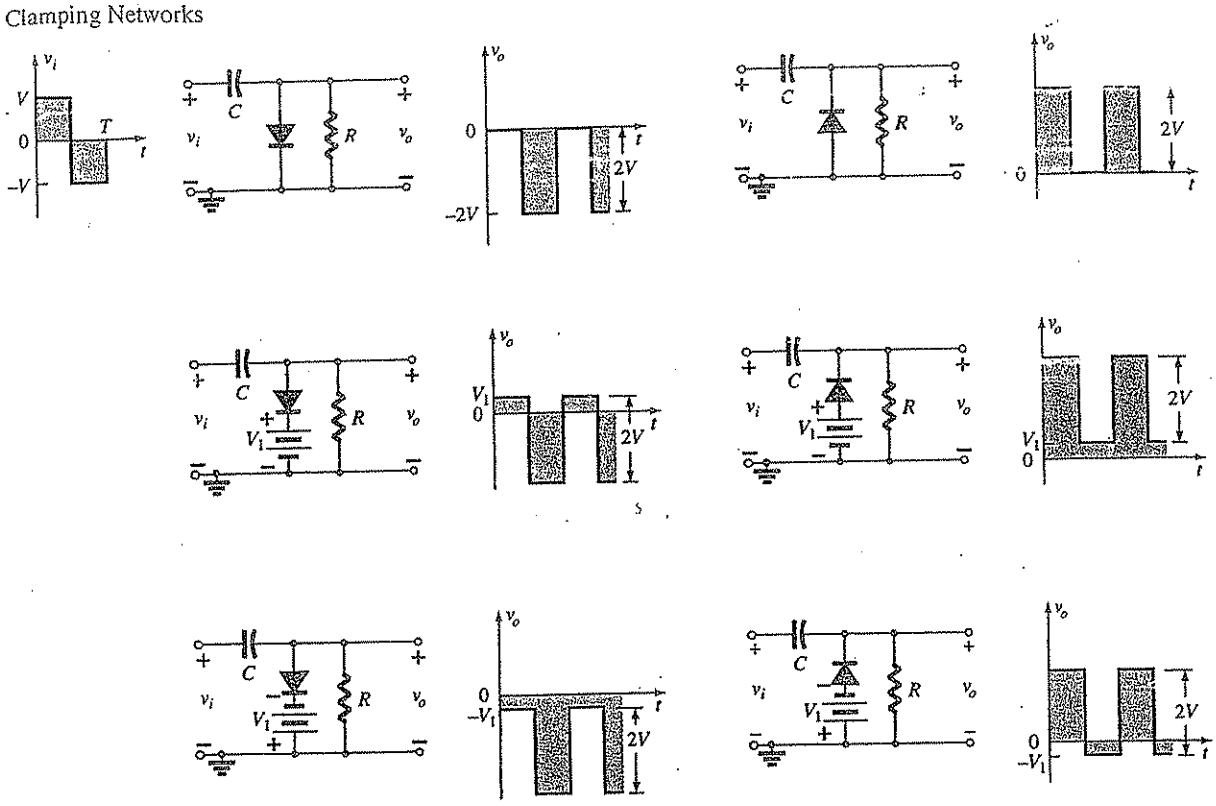


FIG. 2.100
Clamping circuits with ideal diodes ($5\tau = 5RC \gg T/2$).

A number of clamping circuits and their effect on the input signal are shown in Fig. 2.100. Although all the waveforms appearing in Fig. 2.100 are square waves, clamping networks work equally well for sinusoidal signals. In fact, one approach to the analysis of clamping networks with sinusoidal inputs is to replace the sinusoidal signal by a square wave of the same peak values. The resulting output will then form an envelope for the sinusoidal response as shown in Fig. 2.101 for a network appearing in the bottom right of Fig. 2.100.

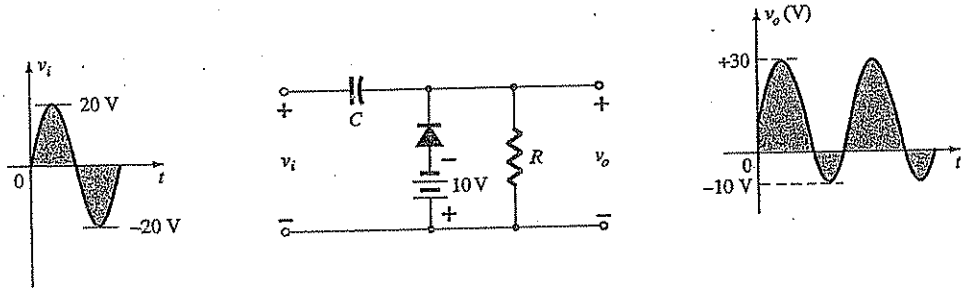


FIG. 2.101
Clamping network with a sinusoidal input.

2.10 ZENER DIODES

The analysis of networks employing Zener diodes is quite similar to the analysis of semiconductor diodes in previous sections. First the state of the diode must be determined, followed by a substitution of the appropriate model and a determination of the other unknown quantities of the network. Figure 2.102 reviews the approximate equivalent circuits for each region of a Zener diode assuming the straight-line approximations at each break point. Note that the forward-bias region is included because occasionally an application will skip into this region also.

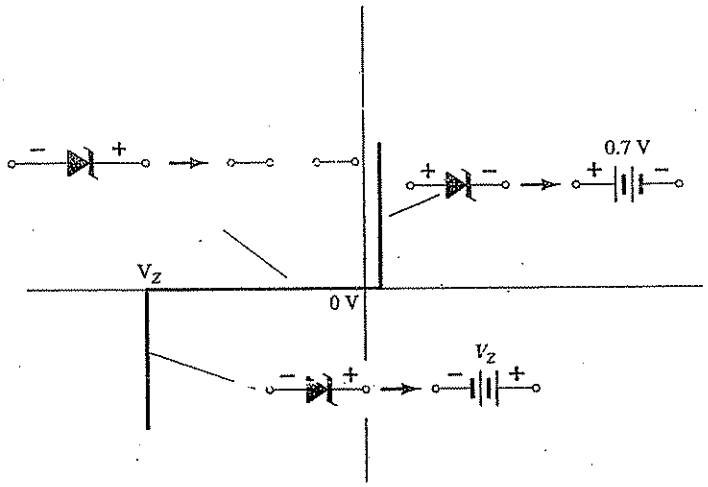


FIG. 2.102
Approximate equivalent circuits for the Zener diode in the three possible regions of application.

The first two examples will demonstrate how a Zener diode can be used to establish reference voltage levels and act as a protection device. The use of a Zener diode as a *regulator* will then be described in detail because it is one of its major areas of application. A regulator is a combination of elements designed to ensure that the output voltage of a supply remains fairly constant.

EXAMPLE 2.24 Determine the reference voltages provided by the network of Fig. 2.103, which uses a white LED to indicate that the power is on. What is the level of current through the LED and the power delivered by the supply? How does the power absorbed by the LED compare to that of the 6-V Zener diode?

Solution: First we have to check that there is sufficient applied voltage to turn on all the series diode elements. The white LED will have a drop of about 4 V across it, the 6-V and 3.3-V Zener diodes have a total of 9.3 V, and the forward-biased silicon diode has 0.7 V, for a total of 14 V. The applied 40 V is then sufficient to turn on all the elements and, one hopes, establish a proper operating current.

Note that the silicon diode was used to create a reference voltage of 4 V because

$$V_{o_1} = V_{Z_2} + V_K = 3.3\,\text{V} + 0.7\,\text{V} = \mathbf{4.0\,V}$$

Combining the voltage of the 6-V Zener diode with the 4 V results in

$$V_{o_2} = V_{o_1} + V_{Z_1} = 4\,\text{V} + 6\,\text{V} = \mathbf{10\,V}$$

Finally, the 4 V across the white LED will leave a voltage of 40 V – 14 V = 26 V across the resistor, and

$$I_R = I_{\text{LED}} = \frac{V_R}{R} = \frac{40\,\text{V} - V_{o_2} - V_{\text{LED}}}{1.3\,\text{k}\Omega} = \frac{40\,\text{V} - 10\,\text{V} - 4\,\text{V}}{1.3\,\text{k}\Omega} = \frac{26\,\text{V}}{1.3\,\text{k}\Omega} = \mathbf{20\,mA}$$

that will establish the proper brightness for the LED.

The power delivered by the supply is simply the product of the supply voltage and current drain as follows:

$$P_s = EI_s = EI_R = (40\,\text{V})(20\,\text{mA}) = \mathbf{800\,mW}$$

The power absorbed by the LED is

$$P_{\text{LED}} = V_{\text{LED}}I_{\text{LED}} = (4\,\text{V})(20\,\text{mA}) = \mathbf{80\,mW}$$

and the power absorbed by the 6-V Zener diode is

$$P_Z = V_Z I_Z = (6\,\text{V})(20\,\text{mA}) = \mathbf{120\,mW}$$

The power absorbed by the Zener diode exceeds that of the LED by 40 mW.

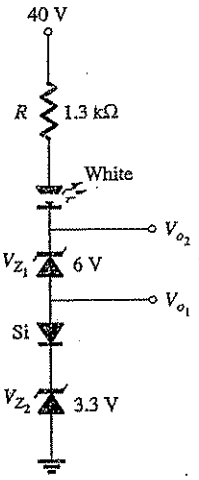


FIG. 2.103
Reference setting circuit for Example 2.24.

EXAMPLE 2.25 The network of Fig. 2.104 is designed to limit the voltage to 20 V during the positive portion of the applied voltage and to 0 V for a negative excursion of the applied voltage. Check its operation and plot the waveform of the voltage across the system for the applied signal. Assume the system has a very high input resistance so it will not affect the behavior of the network.

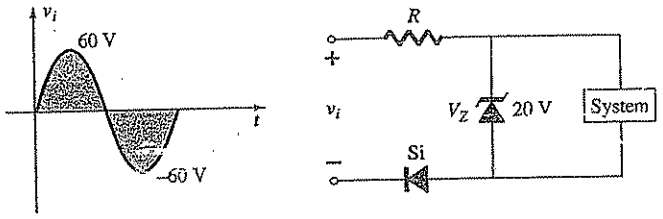


FIG. 2.104
Controlling network for Example 2.25.

Solution: For positive applied voltages less than the Zener potential of 20 V the Zener diode will be in its approximate open-circuit state, and the input signal will simply distribute itself across the elements, with the majority going to the system because it has such a high resistance level.

Once the voltage across the Zener diode reaches 20 V the Zener diode will turn on as shown in Fig. 2.105a and the voltage across the system will lock in at 20 V. Further increases in the applied voltage will simply appear across the series resistor with the voltage across the system and the forward-biased diode remaining fixed at 20 V and 0.7 V, respectively. The voltage across the system is fixed at 20 V, as shown in Fig. 2.105a, because the 0.7 V of the diode is not between the defined output terminals. The system is therefore safe from any further increases in applied voltage.

For the negative region of the applied signal the silicon diode is reverse biased and presents an open circuit to the series combination of elements. The result is that the full

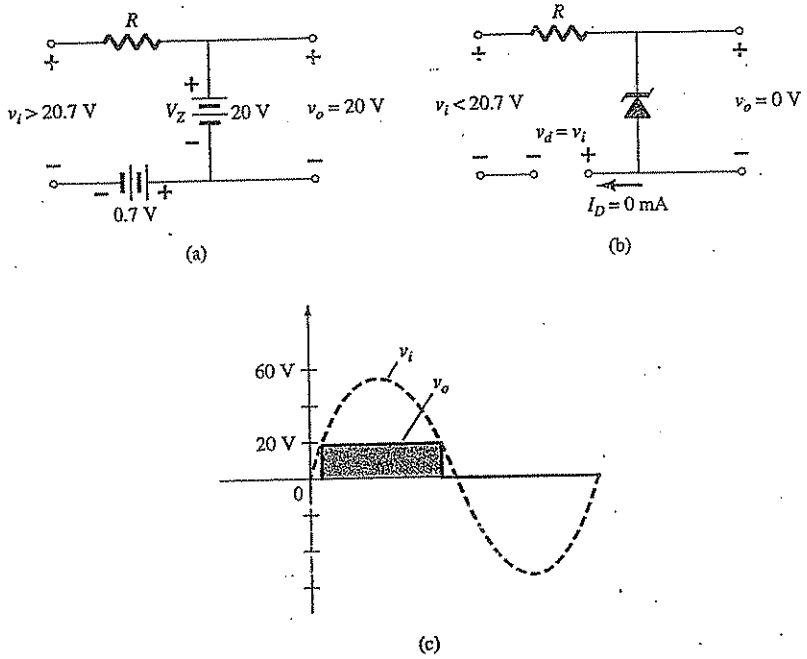


FIG. 2.105
Response of the network of Fig. 2.104 to the application of a 60-V sinusoidal signal.

negatively applied signal will appear across the open-circuited diode and the negative voltage across the system locked in at 0 V, as shown in Fig. 2.104b.

The voltage across the system will therefore appear as shown in Fig. 2.105c.

The use of the Zener diode as a regulator is so common that three conditions surrounding the analysis of the basic Zener regulator are considered. The analysis provides an excellent opportunity to become better acquainted with the response of the Zener diode to different operating conditions. The basic configuration appears in Fig. 2.106. The analysis is first for fixed quantities, followed by a fixed supply voltage and a variable load, and finally a fixed load and a variable supply.

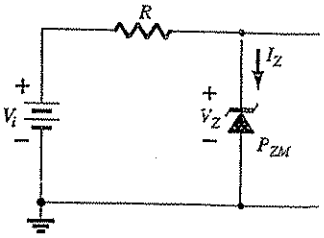


FIG. 2.106
Basic Zener regulator.

V_i and R Fixed

The simplest of Zener diode regulator networks appears in Fig. 2.106. The applied dc voltage is fixed, as is the load resistor. The analysis can fundamentally be broken down into two steps.

1. ***Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.***

Applying step 1 to the network of Fig. 2.106 results in the network of Fig. 2.107, where an application of the voltage divider rule results in

$$V = V_L = \frac{R_L V_i}{R + R_L} \tag{2.16}$$

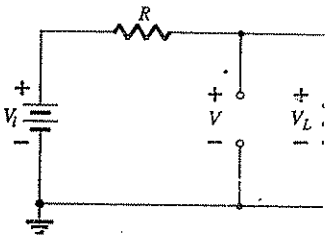


FIG. 2.107
Determining the state of the Zener diode.

If $V \geq V_Z$, the Zener diode is on, and the appropriate equivalent model can be substituted. If $V < V_Z$, the diode is off, and the open-circuit equivalence is substituted.

2. ***Substitute the appropriate equivalent circuit and solve for the desired unknowns.***

For the network of Fig. 2.106, the "on" state will result in the equivalent network of Fig. 2.108. Since voltages across parallel elements must be the same, we find that

$$V_L = V_Z \tag{2.17}$$

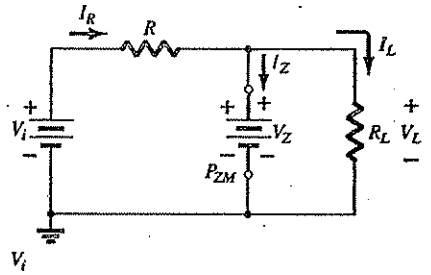


FIG. 2.108
Substituting the Zener equivalent for the "on" situation.

The Zener diode current must be determined by an application of Kirchhoff's current law. That is,

$$I_R = I_Z + I_L$$

and

$$I_Z = I_R - I_L \tag{2.18}$$

where

$$I_L = \frac{V_L}{R_L} \quad \text{and} \quad I_R = \frac{V_R}{R} = \frac{V_i - V_L}{R}$$

The power dissipated by the Zener diode is determined by

$$P_Z = V_Z I_Z \tag{2.19}$$

that must be less than the P_{ZM} specified for the device.

Before continuing, it is particularly important to realize that the first step was employed only to determine the *state of the Zener diode*. If the Zener diode is in the "on" state, the voltage across the diode is not V volts. When the system is turned on, the Zener diode will turn on as soon as the voltage across the Zener diode is V_Z volts. It will then "lock in" at this level and never reach the higher level of V volts.

Multisim
PSpice

EXAMPLE 2.26

a. For the Zener diode network of Fig. 2.109, determine V_L, V_R, I_Z, and P_Z.
b. Repeat part (a) with $R_L = 3\,\text{k}\Omega$.

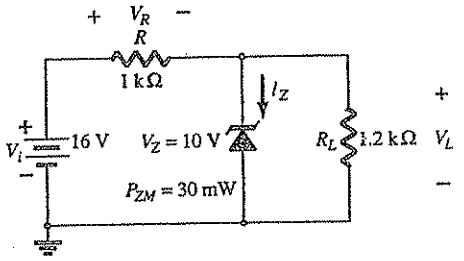


FIG. 2.109
Zener diode regulator for Example 2.26.

Solution:

a. Following the suggested procedure, we redraw the network as shown in Fig. 2.110.

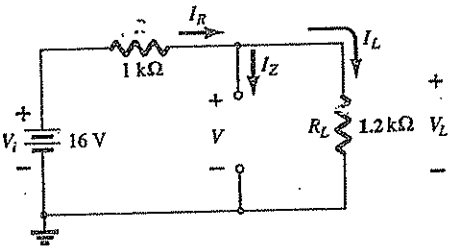


FIG. 2.110
Determining V for the regulator of Fig. 2.109.

Applying Eq. (2.16) gives

$$V = \frac{R_L V_i}{R + R_L} = \frac{1.2\,\text{k}\Omega(16\,\text{V})}{1\,\text{k}\Omega + 1.2\,\text{k}\Omega} = 8.73\,\text{V}$$

Since $V = 8.73$ V is less than $V_Z = 10$ V, the diode is in the "off" state, as shown on the characteristics of Fig. 2.111. Substituting the open-circuit equivalent results in the same network as in Fig. 2.110, where we find that

$$V_L = V = 8.73\,\text{V}$$
$$V_R = V_i - V_L = 16\,\text{V} - 8.73\,\text{V} = 7.27\,\text{V}$$
$$I_Z = 0\,\text{A}$$

and

$$P_Z = V_Z I_Z = V_Z(0\,\text{A}) = 0\,\text{W}$$

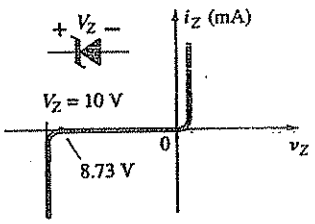


FIG. 2.111
Resulting operating point for the network of Fig. 2.109.

b. Applying Eq. (2.16) results in

$$V = \frac{R_L V_i}{R + R_L} = \frac{3\,\text{k}\Omega(16\,\text{V})}{1\,\text{k}\Omega + 3\,\text{k}\Omega} = 12\,\text{V}$$

Once the diode is in the "on" state, the voltage across R remains fixed at

$$V_R = V_i - V_Z \tag{2.22}$$

and I_R remains fixed at

$$I_R = \frac{V_R}{R} \tag{2.23}$$

The Zener current

$$I_Z = I_R - I_L \tag{2.24}$$

resulting in a minimum I_Z when I_L is a maximum and a maximum I_Z when I_L is a minimum value, since I_R is constant.

Since I_Z is limited to I_{ZM} as provided on the data sheet, it does affect the range of R_L and therefore I_L. Substituting I_{ZM} for I_Z establishes the minimum I_L as

$$I_{L_{min}} = I_R - I_{ZM} \tag{2.25}$$

and the maximum load resistance as

$$R_{L_{max}} = \frac{V_Z}{I_{L_{min}}} \tag{2.26}$$

EXAMPLE 2.27

a. For the network of Fig. 2.113, determine the range of R_L and I_L that will result in V_{RL} being maintained at 10 V.
b. Determine the maximum wattage rating of the diode.

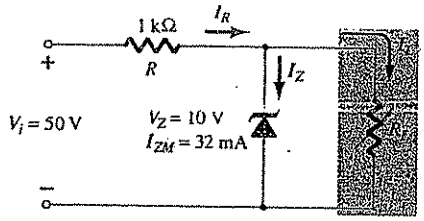


FIG. 2.113
Voltage regulator for Example 2.27.

Solution:

a. To determine the value of R_L that will turn the Zener diode on, apply Eq. (2.20):

$$R_{L_{min}} = \frac{RV_Z}{V_i - V_Z} = \frac{(1\,\text{k}\Omega)(10\,\text{V})}{50\,\text{V} - 10\,\text{V}} = \frac{10\,\text{k}\Omega}{40} = \mathbf{250\ \Omega}$$

The voltage across the resistor R is then determined by Eq. (2.22):

$$V_R = V_i - V_Z = 50\,\text{V} - 10\,\text{V} = \mathbf{40\ V}$$

and Eq. (2.23) provides the magnitude of I_R:

$$I_R = \frac{V_R}{R} = \frac{40\,\text{V}}{1\,\text{k}\Omega} = \mathbf{40\ mA}$$

The minimum level of I_L is then determined by Eq. (2.25):

$$I_{L_{min}} = I_R - I_{ZM} = 40\,\text{mA} - 32\,\text{mA} = \mathbf{8\ mA}$$

Since $V = 12$ V is greater than $V_Z = 10$ V, the diode is in the "on" state and the network of Fig. 2.112 results. Applying Eq. (2.17) yields

$$V_L = V_Z = 10\text{ V}$$

and

$$V_R = V_i - V_L = 16\text{ V} - 10\text{ V} = 6\text{ V}$$

with

$$I_L = \frac{V_L}{R_L} = \frac{10\text{ V}}{3\text{ k}\Omega} = 3.33\text{ mA}$$

and

$$I_R = \frac{V_R}{R} = \frac{6\text{ V}}{1\text{ k}\Omega} = 6\text{ mA}$$

so that

$$I_Z = I_R - I_L\,[\text{Eq. (2.18)}]$$
$$= 6\text{ mA} - 3.33\text{ mA}$$
$$= \mathbf{2.67\text{ mA}}$$

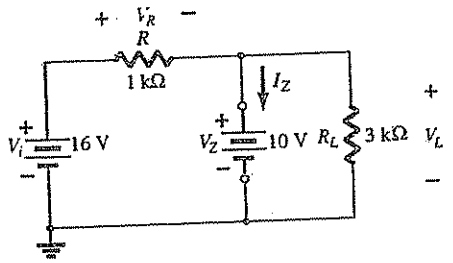


FIG. 2.112
Network of Fig. 2.109 in the "on" state.

The power dissipated is

$$P_Z = V_Z I_Z = (10\text{ V})(2.67\text{ mA}) = \mathbf{26.7\text{ mW}}$$

which is less than the specified $P_{ZM} = 30$ mW.

Fixed V_i, Variable R_L

Due to the offset voltage V_Z, there is a specific range of resistor values (and therefore load current) that will ensure that the Zener is in the "on" state. Too small a load resistance R_L will result in a voltage V_L across the load resistor less than V_Z, and the Zener device will be in the "off" state.

To determine the minimum load resistance of Fig. 2.106 that will turn the Zener diode on, simply calculate the value of R_L that will result in a load voltage $V_L = V_Z$. That is,

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

Solving for R_L, we have

$$R_L = \frac{RV_Z}{V_i - V_Z} \tag{2.20}$$

Any load resistance value greater than the R_L obtained from Eq. (2.20) will ensure that the Zener diode is in the "on" state and the diode can be replaced by its V_Z source equivalent.

The condition defined by Eq. (2.20) establishes the minimum R_L, but in turn specifies the maximum I_L as

$$I_L = \frac{V_i}{R} - \frac{V_Z}{R_L} \tag{2.21}$$

with Eq. (2.26) determining the maximum value of R_L:

$$R_{L_{max}} = \frac{V_Z}{I_{L_{min}}} = \frac{10\text{ V}}{8\text{ mA}} = 1.25\text{ k}\Omega$$

A plot of V_L versus R_L appears in Fig. 2.114a and for V_L versus I_L in Fig. 2.114b.

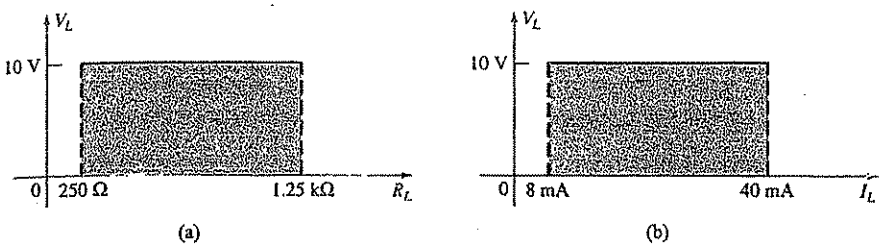


FIG. 2.114
V_L versus R_L and I_L for the regulator of Fig. 2.113.

b. $P_{max} = V_Z I_{ZM}$
$= (10\text{ V})(32\text{ mA}) = \mathbf{320\text{ mW}}$

Fixed R_L, Variable V_i

For fixed values of R_L in Fig. 2.106, the voltage V_i must be sufficiently large to turn the Zener diode on. The minimum turn-on voltage $V_i = V_{i_{min}}$ is determined by

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

and

$$V_{i_{min}} = \frac{(R_L + R)V_Z}{R_L} \tag{2.27}$$

The maximum value of V_i is limited by the maximum Zener current I_{ZM}. Since $I_{ZM} = I_R - I_L$,

$$I_{R_{max}} = I_{ZM} + I_L \tag{2.28}$$

Since I_L is fixed at V_Z/R_L and I_{ZM} is the maximum value of I_Z, the maximum V_i is defined by

$$V_{i_{max}} = V_{R_{max}} + V_Z$$

$$V_{i_{max}} = I_{R_{max}} R + V_Z \tag{2.29}$$

EXAMPLE 2.28 Determine the range of values of V_i that will maintain the Zener diode of Fig. 2.115 in the "on" state.

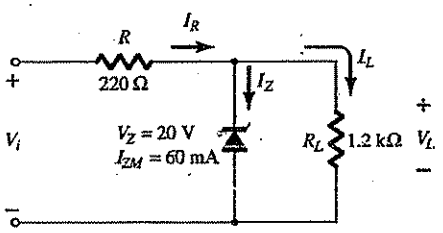


FIG. 2.115
Regulator for Example 2.28.

Solution:

Eq. (2.27): $$V_{i_{min}} = \frac{(R_L + R)V_Z}{R_L} = \frac{(1200\,\Omega + 220\,\Omega)(20\text{ V})}{1200\,\Omega} = 23.67\text{ V}$$

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{20\text{ V}}{1.2\text{ k}\Omega} = 16.67\text{ mA}$$

Eq. (2.28): $$I_{R_{max}} = I_{ZM} + I_L = 60\text{ mA} + 16.67\text{ mA}$$
$$= 76.67\text{ mA}$$

Eq. (2.29): $$V_{i_{max}} = I_{R_{max}}R + V_Z$$
$$= (76.67\text{ mA})(0.22\text{ k}\Omega) + 20\text{ V}$$
$$= 16.87\text{ V} + 20\text{ V}$$
$$= 36.87\text{ V}$$

A plot of V_L versus V_i is provided in Fig. 2.116.

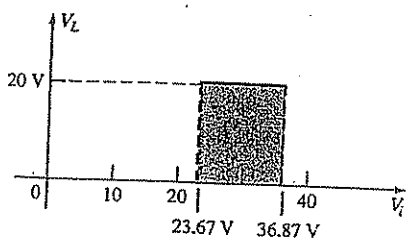


FIG. 2.116
V_L versus V_i for the regulator of Fig. 2.115.

The results of Example 2.28 reveal that for the network of Fig. 2.115 with a fixed R_L, the output voltage will remain fixed at 20 V for a range of input voltage that extends from 23.67 V to 36.87 V.

In fact, the input could appear as shown in Fig. 2.117 and the output would remain constant at 20 V, as shown in Fig. 2.116. The waveform appearing in Fig. 2.117 is obtained by *filtering* a half-wave- or full-wave-rectified output—a process described in detail in a later chapter. The net effect, however, is to establish a steady dc voltage (for a defined range of V_i) such as that shown in Fig. 2.116 from a sinusoidal source with 0 average value.

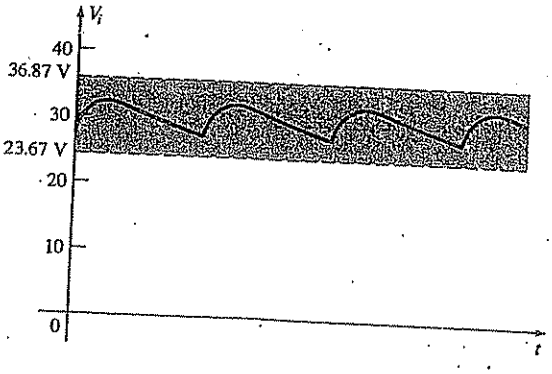


FIG. 2.117
Waveform generated by a filtered rectified signal.

2.11 VOLTAGE-MULTIPLIER CIRCUITS

Voltage-multiplier circuits are employed to maintain a relatively low transformer peak voltage while stepping up the peak output voltage to two, three, four, or more times the peak rectified voltage.